MAXIM

1997 NEW RELEASES DATA BOOK

Volume VI

Featuring

- *Product Selection Tables and Trees*
- *Data Sheets*
- *Free Sample Request Cards*

Other Data Books Available from Maxim

- *1997 Product Selector Guide*
- *1994 to 1996 New Releases Data Books*
- *Notebook Computer Applications Data Book*
- *High-Frequency ASIC Development Handbook*

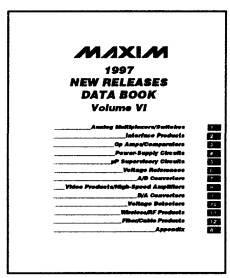
HOW TO USE THE 1997 NEW RELEASES DATA BOOK

Maxim's 1997 *New Releases Data Book* (Vol. VI) brings together over 300 new devices from 12 product families in a single, easy-to-use "Design Guide" format. Each section contains: (1) data sheets for all new products in that family of parts, (2) product-family selection tables and trees.

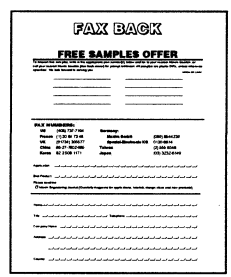
If you need samples for further evaluation, simply fill out one of the sample request cards and fax it to the nearest Maxim office, or call the nearest Maxim office (see back cover) for prompt fulfillment.

We've provided a variety of reference guides to help you locate a specific product or product family:

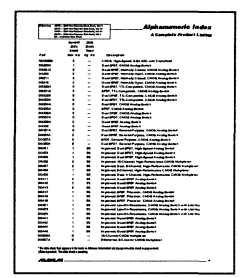
1	Analog Multiplexers/Switches
2	Interface Products
3	Op Amps/Comparators
4	Power-Supply Circuits
5	µP Supervisory Circuits
6	Voltage References
7	A/D Converters
8	Video Products/ High-Speed Amplifiers
9	D/A Converters
10	Voltage Detectors
11	Wireless/RF Products
12	Fiber/Cable Products



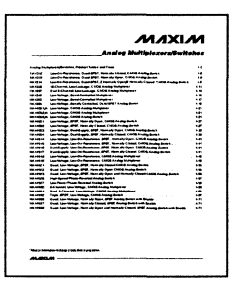
PRODUCT-FAMILY SECTIONS, INDICATED BY TAB NUMBER



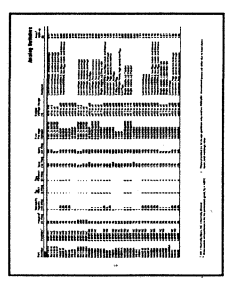
FREE SAMPLE REQUEST CARDS



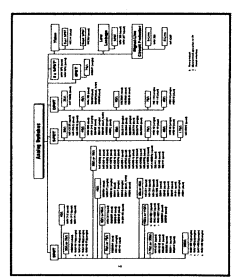
COMPLETE ALPHANUMERIC INDEX OF PART NUMBERS, CROSS REFERENCED TO OTHER MAXIM DATA BOOKS



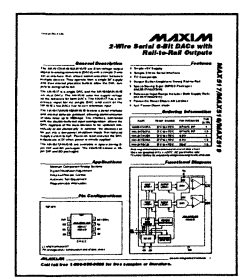
SECTION TABLES OF CONTENTS, SORTED BY PRODUCT FAMILY



PRODUCT-FAMILY SELECTION TABLES WITH SPECIFICATIONS, FEATURES, AND PRICING



PRODUCT-FAMILY SELECTION TREES



DATA SHEETS

VISIT MAXIM'S NEW SITE ON THE WORLD WIDE WEB: http://www.maxim-ic.com

MAXIM

1997 NEW RELEASES DATA BOOK Volume VI

Analog Multiplexers/Switches 1
Interface Products 2
Op Amps/Comparators 3
Power-Supply Circuits 4
µP Supervisory Circuits 5
Voltage References 6
A/D Converters 7
Video Products/High-Speed Amplifiers 8
D/A Converters 9
Voltage Detectors 10
Wireless/RF Products 11
Fiber/Cable Products 12
Appendix A

Introduction

Maxim Integrated Products designs, develops, manufactures, and markets a broad range of linear and mixed-signal integrated circuits (ICs) for use in a variety of electronic products. These ICs "connect" the real (analog) world to the digital world. They detect, measure, amplify, and convert real-world signals—such as temperature, pressure, or sound—into digital signals a computer can process. Over the past 13 years, Maxim has introduced over 1000 analog ICs—more than any other company.

Maxim is committed to meeting the needs of the industry through intensive product development and superior quality. Our product lines include the following: microprocessor supervisory circuits, data converters, references, RS-232 interface circuits, amplifiers, power-control circuits, timers and counters, display circuits, multiplexers, switches, voltage detectors, and analog filters. In addition, the acquisition of the integrated circuit division of Tektronix has expanded our product line to include high-frequency circuits.

Recognizing the growing demand for BiCMOS technology, Maxim has focused increasingly on CMOS- and BiCMOS-based products. These circuits are marketed worldwide, and are available in several different packages and temperature ranges to meet varying customer requirements.

World Wide Web

Visit our WWW site at http://www.maxim-ic.com to access our latest data sheets and free samples. Data sheets can be downloaded instantaneously, and samples that are in stock will be shipped within 24 hours.

Customer Service

If you don't have access to the WWW, call or fax your nearest Maxim location for free samples and literature. Evaluation kits or a small quantity of parts can be ordered using VISA or MasterCard by calling U.S. Headquarters at (800) 998-8800 extension 6380 (U.S. only) or (408) 737-7600 extension 6380. Outside the U.S., call your nearest Maxim location.

Customer service representatives are available during normal business hours to provide information on orders placed directly with the factory. Please see the back cover for a list of domestic and international distributors.

Technical Support

In order to provide full technical support, Maxim has a large, highly qualified group of senior applications engineers available to help you. Simply call U.S. headquarters at (408) 737-7600 extension 4000 between 8:00 a.m. and 5:00 p.m. Pacific Standard Time, or fax your questions to (408) 737-7194.

Maxim also offers a wide variety of technical publications, including the *Product Selector Guide*, *Engineering Journal* (a quarterly magazine explaining the application of our new products), *Notebook Computer Applications Data Book,* Design Guides for each product family, and the *High-Frequency ASIC Development Handbook.* Call your nearest Maxim location for any literature you may need.

Reliability

Maxim's mission is to provide reliable, innovative analog ICs that solve customer problems. Our programs offering complete lot traceability, life test, and humidity life qualification are unique in the industry.

ISO 9001/9002 Certification

In November 1993, the wafer fab at Maxim's Sunnyvale headquarters received formal ISO 9001 certification, validating that our quality system meets the worldwide standard. The wafer fab at our Beaverton, Oregon facility is also 9001 certified, as of July 1994. ISO 9001 is the most stringent of the 9000 series of specifications, because it includes review of design, test, manufacturing, and shipment processes.

In May 1995, ISO 9002 certification was granted to Maxim UK.

Information furnished by Maxim Integrated Products is believed to be accurate and reliable. However, the company cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product; nor for any infringements of patents or other rights of third parties that may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Maxim Integrated Products. Maxim reserves the right to change the circuitry and specifications without notice.

Life Support Policy: Maxim does not authorize any Maxim product for use in life support devices and/or systems without the express written approval of an officer of Maxim Integrated Products, Inc. Life support devices or systems are devices or systems which, (i) are intended for surgical implant into the body or (ii) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

Products in this book may be covered by one or more of the patents listed below. Additional patents are pending.

4,700,286, 4,679,134, 4,636,930, 4,859,963, 4,857,778, 4,897,774, 4,797,899, 4,806,875, 4,847,522, 4,812,891, 4,809,152, 4,801,888, 4,797,569, 4,777,580, 4,777,577, 4,999,761, 4,752,700, 5,142,242, 5,055,796, 4,819,147, 5,027,165, 4,217,599, 4,261,761, 4,228,447, 4,229,756, 4,260,425, 4,435,655, 4,622,736, 4,628,406, 4,701,694, 4,714,872, 4,732,865, 4,733,218, 4,767,946, 4,769,619, 4,774,497, 4,774,478, 4,786,856, 4,819,049, 4,823,028, 4,862,096, 4,876,214, 4,902,640, 4,994,400, 4,994,694, 5,017,814, 5,209,117, 5,151,775, 5,247,468, 5,268,315, 4,228,447, 4,866,314, 5,446,414, 5,414,314, 5,498,984, 5,528,132, 5,532,577, 5,508,650.

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Alphanumeric Index

A Complete Product Listing

Part	Current DS Rev. No.	Data Book Year/97 Book Page No.	Description
ADC0820	1	—	CMOS, High-Speed, 8-Bit ADC with Track/Hold
DG200A	1	—	Dual SPST, CMOS Analog Switch
DG201A	0	—	Quad SPST, Normally Closed, CMOS Analog Switch
DG202	0	—	Quad SPST, Normally Open, CMOS Analog Switch
DG211	0	—	Quad SPST, Normally Closed, CMOS Analog Switch
DG212	0	—	Quad SPST, Normally Open, CMOS Analog Switch
DG300A	0	—	Dual SPST, TTL-Compatible, CMOS Analog Switch
DG301A	0	—	SPDT, TTL-Compatible, CMOS Analog Switch
DG302A	0	—	Dual DPST, TTL-Compatible, CMOS Analog Switch
DG303A	0	—	Dual SPDT, TTL-Compatible, CMOS Analog Switch
DG304A	0	—	Dual SPST, CMOS Analog Switch
DG305A	0	—	SPDT, CMOS Analog Switch
DG306A	0	—	Dual DPST, CMOS Analog Switch
DG307A	0	—	Dual SPDT, CMOS Analog Switch
DG308A	0	—	Quad SPST Analog Switch
DG309	0	—	Quad SPST Analog Switch
DG381A	0	—	Dual SPST, General-Purpose, CMOS Analog Switch
DG384A	0	—	Dual DPST, General-Purpose, CMOS Analog Switch
DG387A	0	—	SPDT, General-Purpose, CMOS Analog Switch
DG390A	0	—	Dual SPDT, General-Purpose, CMOS Analog Switch
DG401	1	95	Improved, Dual SPST, High-Speed Analog Switch
DG403	1	95	Improved, Dual SPDT, High-Speed Analog Switch
DG405	1	95	Improved, Dual DPST, High-Speed Analog Switch
DG406	2	95	Improved, 16-Channel, High-Performance CMOS Multiplexer
DG407	2	95	Improved, Dual, 8-Channel, High-Performance CMOS Multiplexer
DG408	1	93	Improved, 8-Channel, High-Performance CMOS Multiplexer
DG409	1	93	Improved, Dual, 4-Channel, High-Performance CMOS Multiplexer
DG411	2	95	Improved, Quad SPST Analog Switch
DG412	2	95	Improved, Quad SPST Analog Switch
DG413	2	95	Improved, Quad SPST Analog Switch
DG417	1	95	Improved, SPST, Precision, CMOS Analog Switch
DG418	1	95	Improved, SPST, Precision, CMOS Analog Switch
DG419	1	95	Improved, SPDT, Precision, CMOS Analog Switch
DG421	1	95	Improved, Low-On-Resistance, CMOS Analog Switch with Latches
DG423	1	95	Improved, Low-On-Resistance, CMOS Analog Switch with Latches
DG425	1	95	Improved, Low-On-Resistance, CMOS Analog Switch with Latches
DG441	2	95	Improved, Quad SPST Analog Switch
DG442	2	95	Improved, Quad SPST Analog Switch
DG444	1	95	Improved, Quad SPST Analog Switch
DG445	1	95	Improved, Quad SPST Analog Switch
DG506A	0	—	16-Channel CMOS Multiplexer
DG507A	0	—	Differential, 8-Channel CMOS Multiplexer

*The data sheet that appears in the book is Advance Information (first page of a data sheet in preparation).
†Future product. The data sheet is pending.

Alphanumeric Index

A Complete Product Listing

Part	Current DS Rev. No.	Data Book Year/97 Book Page No.	Description
DG508A	2	—	8-Channel CMOS Multiplexer
DG509A	2	—	Differential, 4-Channel CMOS Multiplexer
DG528	0	—	8-Channel, Latchable Multiplexer
DG529	0	—	Differential, 4-Channel, Latchable Multiplexer
HI-201	0	—	Quad SPST, CMOS Analog Switch
HI-201HS	1	—	High-Speed, Quad SPST, CMOS Analog Switch
HI-508A	0	92	Fault-Protected, 8-Channel Multiplexer
HI-509A	0	92	Fault-Protected, Differential 4-Channel Multiplexer
ICL7106	0	—	3 1/2-Digit ADC with LCD Drivers
ICL7107	0	—	3 1/2-Digit ADC with LED Drivers
ICL7109	1	—	12-Bit ADC with Three-State Binary Outputs
ICL7116	0	—	3 1/2-Digit ADC with LCD Drivers and Display Hold
ICL7117	0	—	3 1/2-Digit ADC with LED Drivers and Display Hold
ICL7126	0	—	Low-Power, 3 1/2-Digit ADC with LCD Drivers
ICL7129A	0	—	Low-Noise, 4 1/2-Digit, Single-Chip ADC with Multiplexed LCD Drivers
ICL7135	1	—	4 1/2-Digit ADC with Multiplexed BCD Outputs
ICL7136	1	—	Low-Power, 3 1/2-Digit ADC with LCD Drivers
ICL7137	0	—	Low-Power, 3 1/2-Digit ADC with LED Drivers
ICL7611	0	—	Low-Power, Industry-Standard Op Amp
ICL7612	0	—	Low-Power, Industry-Standard Op Amp
ICL7614	0	—	Low-Power, Industry-Standard Op Amp
ICL7616	0	—	Low-Power Op Amp
ICL7621	0	—	Dual, Low-Power, Industry-Standard Op Amp
ICL7622	0	—	Dual, Low-Power, Industry-Standard Op Amp
ICL7631	0	—	Triple, Low-Power, Industry-Standard Op Amp
ICL7632	0	—	Triple, Low-Power, Industry-Standard Op Amp
ICL7641	0	—	Quad, Low-Power, Industry-Standard Op Amp
ICL7642	0	—	Quad, Low-Power, Industry-Standard Op Amp
ICL7650/B	1	—	Chopper-Stabilized Op Amp
ICL7652/B	0	—	Chopper-Stabilized Op Amp
ICL7660	1	93	10mA Charge-Pump Voltage Converter
ICL7662	1	—	CMOS, Switched-Capacitor Voltage Converter (Up to 20V Input)
ICL7663A	2	—	Low-Power, Adjustable-Output, Positive-Voltage Linear Regulator
ICL7664A/B	2	—	Low-Power, Adjustable-Output, Negative-Voltage Linear Regulator
ICL7665	1	—	µP Voltage Monitor with Dual Over/Undervoltage Detection
ICL7667	0	—	Dual-Power MOSFET Driver (Inverting)
ICL8069	0	—	1.2V Voltage Reference
ICM7211	1	—	4-Digit, LCD Decoder/Driver
ICM7212	1	—	4-Digit, LED Decoder/Driver
ICM7217	0	—	4-Digit, Presettable, LED Up/Down Counter
ICM7218	0	—	8-Digit, Multiplexed, LED Decoder/Driver
ICM7224	0	—	4 1/2-Digit, LCD, High-Speed Counter/Decoder/Driver

*The data sheet that appears in the book is Advance Information (first page of a data sheet in preparation).
†Future product. The data sheet is pending.

Alphanumeric Index

A Complete Product Listing

Part	Current DS Rev. No.	Data Book Year/97 Book Page No.	Description
ICM7225	0	—	4 1/2-Digit, LED, High-Speed Counter/Decoder/Driver
ICM7228	0	—	8-Digit, LED Display Driver
ICM7240	0	—	8-Bit Binary, Programmable, RC Timer/Counter
ICM7242	0	—	7-Bit Binary, Fixed, RC Timer/Counter
ICM7250	0	—	Two-Digit BCD, Programmable, RC Timer/Counter
ICM7260	0	—	Module-60, Programmable, RC Timer/Counter
ICM7555	2	—	Low-Power, General-Purpose Timer
ICM7556	2	—	Low-Power, General-Purpose Dual Timer
IH5040	1	—	SPST, Normally Open, CMOS Analog Switch
IH5041	1	—	Dual SPST, Normally Open, CMOS Analog Switch
IH5042	1	—	SPDT, CMOS Analog Switch
IH5043	1	—	Dual SPDT, CMOS Analog Switch
IH5044	1	—	DPST, Normally Open, CMOS Analog Switch
IH5045	1	—	Dual DPST, Normally Open, CMOS Analog Switch
IH5047	1	—	4PST, Normally Open, CMOS Analog Switch
IH5048	1	—	Dual SPST, 75Ω Analog Switch
IH5048A	1	—	Dual SPST, Low-On-Resistance, 25Ω Analog Switch
IH5049	1	—	Dual DPST, Low-Charge-Injection Analog Switch
IH5050	1	—	SPDT, Low-Charge-Injection Analog Switch
IH5051	1	—	Dual SPDT, Low-Charge-Injection Analog Switch
IH5108	0	92	See MAX358
IH5140	0	—	Low-Power, SPST, Fast, CMOS Analog Switch
IH5141	0	—	Dual SPST, Low-Power, Fast, CMOS Analog Switch
IH5142	0	—	SPDT, Low-Power, Fast, CMOS Analog Switch
IH5143	0	—	Dual SPDT, Low-Power, Fast, CMOS Analog Switch
IH5144	0	—	DPST, Low-Power, Fast, CMOS Analog Switch
IH5145	0	—	Dual DPST, Low-Power, Fast, CMOS Analog Switch
IH5208	0	92	See MAX359
IH5341	1	—	Dual SPST, RF/Video Switch
IH5352	1	—	Quad SPST, RF/Video Switch
IH6108	0	—	See DG508A
IH6116	0	—	See DG506A
IH6208	0	—	See DG509A
IH6216	0	—	See DG507A
LH0033/A	0	—	Fast Buffer Amplifier
LH0063	3	—	Very Fast Buffer Amplifier
LH0101	0	—	Power Op Amp
MAX038	1	95	High-Frequency Waveform Generator
MAX038EVKIT	1	—	Evaluation Kit for the MAX038
MAX100	0	96	250Msps, 8-Bit ADC with Track/Hold
MAX100EVKIT	0	—	Evaluation Kit for the MAX100
MAX101A	0	96	500Msps, 8-Bit ADC with Track/Hold

*The data sheet that appears in the book is Advance Information (first page of a data sheet in preparation).
†Future product. The data sheet is pending.

Alphanumeric Index

A Complete Product Listing

Part	Current DS Rev. No.	Data Book Year/97 Book Page No.	Description
MAX101AEVKIT	1	—	Evaluation Kit for the MAX101A
MAX104	†	**7-9***	**1Gsps, 8-Bit ADC with Track/Hold**
MAX104EVKIT	†	—	Evaluation Kit for the MAX104
MAX110	3	96	±5V, Low-Cost, 2-Channel, Serial ±14-Bit ADC
MAX110EVKIT	1	—	Evaluation Kit for the MAX110/MAX111
MAX111	3	96	5V, Low-Cost, 2-Channel, Serial ±14-Bit ADC
MAX113	**1**	**7-11**	**3V, 8-Bit, 4-Channel, Low-Power ADC**
MAX114	**1**	**7-23**	**5V, 8-Bit, 4-Channel, Low-Power ADC**
MAX117	**1**	**7-11**	**3V, 8-Bit, 8-Channel, Low-Power ADC**
MAX117EVKIT	0	—	Evaluation Kit for MAX117/MAX118
MAX118	**1**	**7-23**	**5V, 8-Bit, 8-Channel, Low-Power ADC**
MAX120	0	95	500ksps, Sampling, 12-Bit ADC with Track/Hold and Reference
MAX120EVKIT	0	—	Evaluation Kit for the MAX120/MAX122
MAX121	1	—	308ksps, Sampling, 12-Bit ADC with Track/Hold and Reference
MAX121EVKIT	0	—	Evaluation Kit for the MAX121
MAX122	0	95	333ksps, Sampling, 12-Bit ADC with Track/Hold and Reference
MAX125	†	**7-35***	**2x4-Channel, Simultaneous-Sampling 14-Bit DAS with ±5V Input Range**
MAX125EVKIT	†	—	Evaluation Kit for the MAX125/MAX126
MAX126	†	**7-35***	**2x4-Channel, Simultaneous-Sampling 14-Bit DAS with ±2.5V Input Range**
MAX130	0	—	3 1/2-Digit ADC with Bandgap Reference
MAX131	0	—	3 1/2-Digit ADC with Bandgap Reference
MAX132	2	93	±18-Bit, Low-Power ADC with Serial Interface
MAX132EVKIT	2	—	Evaluation Kit for the MAX132
MAX133	0	—	9V, 3 3/4-Digit DMM Circuit
MAX134	0	—	±5V, 3 3/4-Digit DMM Circuit
MAX134EVBRD	0	—	PC-Based Evaluation System for the MAX133/MAX134
MAX135	0	93	±15-Bit, Low-Power ADC with Parallel Interface
MAX136	0	—	Low-Power, 3 1/2-Digit ADC with Display Hold and LCD Drivers
MAX138	2	—	3 1/2-Digit ADC with Reference, Charge-Pump and LCD Drivers
MAX139	2	—	3 1/2-Digit ADC with Reference, Charge-Pump and LED Drivers
MAX140	2	—	3 1/2-Digit ADC with Reference, Charge-Pump and Low-Current LED Drivers
MAX146	†	**7-37***	**2.7V, Low-Power, 8-Channel, Serial 12-Bit ADC with Internal Reference**
MAX147	**0**	**7-39**	**2.7V, Low-Power, 8-Channel, Serial 12-Bit ADC**
MAX147EVKIT	0	—	Evaluation Kit for the MAX147
MAX148	**0**	**7-59**	**2.7V, Low-Power, 8-Channel, Serial 10-Bit ADC**
MAX149	†	**7-79***	**2.7V, Low-Power, 8-Channel, Serial 10-Bit ADC with Internal Reference**
MAX150	1	—	CMOS, 1.3µs, 8-Bit ADC with Voltage Reference and Track/Hold

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†Future product. The data sheet is pending.

Alphanumeric Index

A Complete Product Listing

Part	Current DS Rev. No.	Data Book Year/97 Book Page No.	Description
MAX151	0	92	300kHz, 10-Bit ADC with Reference and Track/Hold
MAX152	1	—	3V, 8-Bit ADC with 1µA Power-Down
MAX152EVKIT	1	—	Evaluation Kit for the MAX152/MAX153
MAX153	0	—	1Msps, µP-Compatible, 8-Bit ADC with 1µA Power-Down
MAX154	2	—	CMOS, High-Speed, 4-Channel, 8-Bit ADC with Reference
MAX155	1	93	High-Speed, 8-Channel, 8-Bit ADC with Simultaneous Track/Holds and Reference
MAX155EVKIT	0	—	Evaluation Kit for the MAX155
MAX156	1	93	High-Speed, 4-Channel, 8-Bit ADC with Simultaneous Track/Holds and Reference
MAX158	2	—	CMOS, High-Speed, 8-Channel, 8-Bit ADC with Reference
MAX160	0	—	CMOS, µP-Compatible, 4µs, 8-Bit ADC
MAX161	1	—	CMOS, 20µs, 8-Bit, 8-Channel Data-Acquisition System
MAX162	0	92	CMOS, 3µs, 12-Bit ADC with Reference
MAX163	1	92	CMOS, 5V-Input, 100ksps, 12-Bit ADC with Track/Hold and Reference
MAX164	0	92	CMOS, ±5V-Input, 100ksps, 12-Bit ADC with Track/Hold and Reference
MAX165	1	93	5µs, 8-Bit ADC with Track/Hold and Reference
MAX166	1	93	Differential Input, 5µs, 8-Bit ADC with Track/Hold and Reference
MAX167	0	92	CMOS, ±2.5V Input, 100ksps, 12-Bit ADC with Track/Hold and Reference
MAX170	0	—	Serial-Output, 5.6µs, 12-Bit ADC with Reference
MAX172	0	92	CMOS, 10µs, 12-Bit ADC with Reference
MAX173	0	—	CMOS, 5µs, 10-Bit ADC with Reference
MAX174	2	—	Industry-Standard, 12-Bit ADC with Reference
MAX176	1	94	250ksps, Serial, 12-Bit ADC with Track/Hold and Reference
MAX176EVKIT	1	—	Evaluation Kit for the MAX176
MAX177	0	—	CMOS, 12-Bit ADC with Track/Hold and Reference
MAX178	0	92	Calibrated, 12-Bit ADC with Track/Hold and Reference
MAX180	0	92	Complete, 100ksps, 8-Channel, 12-Bit Data-Acquisition System
MAX180EVKIT	0	—	Evaluation Kit for the MAX180/MAX181
MAX181	0	92	Complete, 100ksps, 6-Channel, 12-Bit Data-Acquisition System
MAX182	0	92	Calibrated, 4-Channel, 12-Bit ADC with Track/Hold and Reference
MAX183	0	92	3µs, 12-Bit ADC
MAX184	0	92	5µs, 12-Bit ADC
MAX185	0	92	10µs, 12-Bit ADC
MAX186	4	—	Low-Power, 8-Channel, 133ksps, Serial 12-Bit ADC with Track/Hold and Reference
MAX186EVKIT	1	—	Evaluation Kit for the MAX186/MAX188
MAX187	0	95	Low-Power, Serial 12-Bit ADC with Track/Hold and Reference (8-Pin)
MAX187EVKIT	0	—	Evaluation Kit for the MAX187/MAX189
MAX188	3	—	Low-Power, 8-Channel, 133ksps, Serial 12-Bit ADC with Track/Hold
MAX189	0	95	Low-Power, Serial 12-Bit ADC with Track/Hold (8-Pin)
MAX190	2	—	75ksps, 5V, 12-Bit ADC with Track/Hold and Reference

*The data sheet that appears in the book is Advance Information (first page of a data sheet in preparation).
†Future product. The data sheet is pending.

Alphanumeric Index

A Complete Product Listing

Part	Current DS Rev. No.	Data Book Year/97 Book Page No.	Description
MAX190EVKIT	2	—	Evaluation Kit for the MAX190
MAX191	3	94	Low-Power, Sampling, 12-Bit ADC with Reference and Power-Down
MAX191EVKIT	3	—	Evaluation Kit for the MAX191
MAX192	0	95	Low-Power, 8-Channel, Serial 10-Bit ADC
MAX194	3	96	85ksps, Serial 14-Bit ADC with 10µA Shutdown
MAX194EVKIT	1	—	Evaluation Kit for the MAX194
MAX195	0	96	16-Bit, 85ksps ADC with 10µA Shutdown
MAX195EVKIT	1	—	Evaluation Kit for the MAX195
MAX196	**0**	**7-81**	**6-Channel, Multi-Range, 5V, 12-Bit DAS with 12-Bit Bus Interface and Fault Protection**
MAX196EVKIT	0	—	Evaluation Kit for the MAX196/MAX198
MAX197	**1**	**7-97**	**8-Channel, Multi-Range, 5V, 12-Bit DAS with 8+4 Bus Interface and Fault Protection**
MAX197EVKIT	1	—	Evaluation Kit for the MAX197/MAX199
MAX198	**0**	**7-81**	**6-Channel, Multi-Range, 5V, 12-Bit DAS with 12-Bit Bus Interface and Fault Protection**
MAX199	0	96	8-Channel, Multi-Range, 5V, 12-Bit DAS with 8+4 Bus Interface and Fault Protection
MAX200	4	95	5V, 5-Channel RS-232 Transmitter with 0.1µF External Capacitors
MAX201	4	95	5V/9V to 13.2V, Dual RS-232 Transceiver with 0.1µF External Capacitors
MAX202	4	95	5V, Dual RS-232 Transceiver with 0.1µF External Capacitors
MAX202E	**3**	**2-9**	**±15kV ESD-Protected, 5V RS-232 Transceiver**
MAX203	4	95	Complete, 5V, Dual RS-232 Transceiver
MAX203E	**3**	**2-9**	**±15kV ESD-Protected, Complete, 5V, Dual RS-232 Transceiver**
MAX204	4	95	5V, Quad RS-232 Transmitter with 0.1µF External Capacitors
MAX205	4	95	Complete, 5V, 5-Channel RS-232 Transceiver
MAX205E	**3**	**2-9**	**±15kV ESD-Protected, 5-Driver/5-Receiver, +5V, RS-232 Transceiver with Shutdown**
MAX206	4	95	5V RS-232 Transceiver with 0.1µF External Capacitors
MAX206E	**3**	**2-9**	**±15kV ESD-Protected, 4-Driver/3-Receiver, +5V, RS-232 Transceiver with Shutdown**
MAX207	4	95	5V RS-232 Transceiver with 0.1µF External Capacitors
MAX207E	**3**	**2-9**	**±15kV ESD-Protected, 5-Driver/3-Receiver, +5V, RS-232 Transceiver**
MAX208	4	95	5V, Quad RS-232 Transceiver with 0.1µF External Capacitors
MAX208E	**3**	**2-9**	**±15kV ESD-Protected, 4-Driver/4-Receiver, +5V, RS-232 Transceiver**
MAX209	4	95	5V RS-232 Transceiver with 0.1µF External Capacitors
MAX211	4	95	5V RS-232 Transceiver with 0.1µF External Capacitors
MAX211E	**3**	**2-9**	**±15kV ESD-Protected, 5V RS-232 Transceiver**
MAX212	2	95	3V, 3-Driver/5-Receiver, True RS-232 Serial Port
MAX212EVKIT	n/a	—	Evaluation Kit for the MAX212
MAX213	4	95	5V RS-232 Transceiver with 0.1µF External Capacitors
MAX213E	**3**	**2-9**	**±15kV ESD-Protected, 5V RS-232 Transceiver**

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Alphanumeric Index

A Complete Product Listing

Part	Current DS Rev. No.	Data Book Year/97 Book Page No.	Description
MAX214	1	95	5V, Programmable, DTE/DCE RS-232 Transceiver
MAX216	0	94	Low-Power, AppleTalk Interface Transceiver
MAX218	1	95	1.8V to 4.25V Input, Dual RS-232 Transceiver
MAX220	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX222	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX223	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX225	6	—	5V, Multi-Channel RS-232 Driver/Receiver
MAX230	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX231	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX232	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX232A	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX232E	**3**	**2-9**	**±15kV ESD-Protected, 5V RS-232 Transceiver**
MAX233	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX233A	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX234	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX235	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX236	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX237	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX238	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX239	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX240	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX241	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX241E	**3**	**2-9**	**±15kV ESD-Protected, 5V RS-232 Transceiver**
MAX242	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX243	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX244	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX245	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX246	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX247	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX248	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX249	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX250	0	92	5V, Isolated, RS-232 Driver/Receiver
MAX251	0	92	5V, Isolated, RS-232 Driver/Receiver
MAX252	2	92	Complete, 5V, Isolated, Dual RS-232 Transceiver Module
MAX253	0	95	Isolated RS-485 Power Driver
MAX260	0	92	µP-Programmable, Universal Switched-Capacitor Filter
MAX260SOFT	n/a	—	Filter Design Software for the MAX260
MAX261	0	92	µP-Programmable, Universal Switched-Capacitor Filter
MAX262	0	92	µP-Programmable, Universal Switched-Capacitor Filter
MAX263	1	92	Pin-Programmable, Universal Switched-Capacitor Filter
MAX264	1	92	Pin-Programmable, Universal Switched-Capacitor Filter
MAX265	0	—	Resistor/Pin-Programmable, Universal Switched-Capacitor Filter

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Alphanumeric Index

A Complete Product Listing

Part	Current DS Rev. No.	Data Book Year/97 Book Page No.	Description
MAX266	0	—	Resistor/Pin-Programmable, Universal Switched-Capacitor Filter
MAX267	1	92	Pin-Programmable, Bandpass Switched-Capacitor Filter
MAX268	1	92	Pin-Programmable, Bandpass Switched-Capacitor Filter
MAX270	1	92	Digitally Programmable, Dual, 2nd-Order, Continuous Lowpass Filter
MAX271	1	92	Digitally Programmable, Dual, 2nd-Order, Continuous Lowpass Filter with Track/Hold
MAX274	3	93	8th-Order, Continuous Analog Filter
MAX274SOFT	2	—	Filter Design Software for the MAX274/MAX275
MAX274EVKIT	2	—	Evaluation Kit for the MAX274/MAX275
MAX275	3	93	4th-Order, Continuous Analog Filter
MAX280	3	—	5th-Order, Zero DC Error, Butterworth, Switched-Capacitor Lowpass Filter
MAX281	0	92	5th-Order, Zero DC Error, Bessel, Switched-Capacitor Lowpass Filter
MAX291	2	93	8th-Order, Butterworth, Clock-Tunable, 100:1 Lowpass Filter
MAX292	2	93	8th-Order, Bessel, Clock-Tunable, 100:1 Lowpass Filter
MAX293	0	93	8th-Order, Elliptic, 1.5 Transition Ratio, Clock-Tunable, 100:1 Lowpass Filter
MAX294	0	93	8th-Order, Elliptic, 1.2 Transition Ratio, Clock-Tunable, 100:1 Lowpass Filter
MAX295	2	93	8th-Order, Butterworth, Clock-Tunable, 50:1 Lowpass Filter
MAX296	2	93	8th-Order, Bessel, Clock-Tunable, 50:1 Lowpass Filter
MAX297	0	93	8th-Order, Elliptic, 1.5 Transition Ratio, Clock-Tunable, 50:1 Lowpass Filter
MAX301	0	95	Low-On-Resistance, Precision, Dual, SPST, High-Speed Analog Switch
MAX303	0	95	Low-On-Resistance, Precision, Dual, SPST, High-Speed Analog Switch
MAX305	0	95	Low-On-Resistance, Precision, Dual, SPST, High-Speed Analog Switch
MAX306	0	95	Precision, 16-Channel, High-Performance, CMOS Analog Multiplexer
MAX307	0	95	Precision, 8-Channel, High-Performance, CMOS Analog Multiplexer
MAX308	0	95	Precision, 8-Channel, High-Performance, CMOS Analog Multiplexer
MAX309	0	95	Precision, Dual 4-Channel, High-Performance, CMOS Analog Multiplexer
MAX310	0	92	8-Channel, CMOS RF/Video Multiplexer
MAX311	0	92	Differential 4-Channel, CMOS RF/Video Multiplexer
MAX312	**0**	**1-9**	**Low-On-Resistance, Quad SPST, Normally Closed, CMOS Analog Switch**
MAX313	**0**	**1-9**	**Low-On-Resistance, Quad SPST, Normally Open, CMOS Analog Switch**
MAX314	**0**	**1-9**	**Low-On-Resistance, Quad SPST, 2 Normally Open/2 Normally Closed, CMOS Analog Switch**
MAX317	1	95	Precision, SPST, CMOS Analog Switch
MAX318	1	95	Precision, SPST, CMOS Analog Switch
MAX319	1	95	Precision, SPST, CMOS Analog Switch
MAX320	0	96	Precision, Dual-Supply, Dual SPST, Normally Open, CMOS Analog Switch

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Alphanumeric Index

A Complete Product Listing

Part	Current DS Rev. No.	Data Book Year/97 Book Page No.	Description
MAX321	0	96	Precision, Dual-Supply, Dual SPST, Normally Closed, CMOS Analog Switch
MAX322	0	96	Precision, Dual-Supply, Dual SPST, CMOS Analog Switch
MAX323	0	96	Precision, Single-Supply, SPST, Normally Open Analog Switch
MAX324	0	96	Precision, Single-Supply, SPST, Normally Closed Analog Switch
MAX325	0	96	Precision, Single-Supply, SPST Analog Switch
MAX326	2	92	Quad SPST, Ultra-Low-Leakage, CMOS Analog Switch
MAX327	2	92	Quad SPST, Ultra-Low-Leakage, CMOS Analog Switch
MAX328	1	92	Ultra-Low-Leakage, Single-Ended, Monolithic, CMOS Analog Multiplexer
MAX329	1	92	Ultra-Low-Leakage, Differential, Monolithic, CMOS Analog Multiplexer
MAX331	0	—	Quad SPST, Normally Closed, CMOS Analog Switch
MAX332	0	—	Quad SPST, Normally Open, CMOS Analog Switch
MAX333	0	—	Quad SPDT, CMOS Analog Switch
MAX333A	0	95	Improved, Low-On-Resistance, Quad SPDT, CMOS Analog Switch
MAX334	0	—	Quad SPST, High-Speed, Break-Before-Make Analog Switch
MAX335	2	95	Serial-Controlled, Octal SPST Analog Switch
MAX336	†	**1-19***	**16-Channel, Low-Leakage, CMOS Analog Multiplexer**
MAX337	†	**1-19***	**Dual 8-Channel, Low-Leakage, CMOS Analog Multiplexer**
MAX338	0	95	8-Channel, Low-Leakage, CMOS Analog Multiplexer
MAX339	0	95	Dual 4-Channel, Low-Leakage, CMOS Analog Multiplexer
MAX349	**0**	**1-21**	**Low-Voltage, Serial-Controlled Multiplexer**
MAX350	**0**	**1-21**	**Low-Voltage, Serial-Controlled Multiplexer**
MAX351	1	95	Precision, Quad SPST Analog Switch
MAX352	1	95	Precision, Quad SPST Analog Switch
MAX353	1	95	Precision, Quad SPST, Normally Closed Analog Switch
MAX354	2	96	Single, 8-Channel, Fault-Protected CMOS Multiplexer—Improved MAX358
MAX355	2	96	Dual, 4-Channel, Fault-Protected CMOS Multiplexer
MAX358	0	92	8-Channel, Fault-Protected Multiplexer
MAX359	0	92	Differential 4-Channel, Fault-Protected Multiplexer
MAX361	0	95	Precision, Quad SPST Analog Switch
MAX362	0	95	Precision, Quad SPST Analog Switch
MAX364	0	95	Precision, Quad SPST Analog Switch
MAX365	0	95	Precision, Quad SPST Analog Switch
MAX366	†	96	Signal-Line Circuit Protector with Three Independent Protectors
MAX367	†	96	Signal-Line Circuit Protector with Eight Independent Protectors
MAX368	1	92	8-Channel, Fault-Protected, Latched Multiplexer
MAX369	1	92	Differential 4-Channel, Fault-Protected, Latched Multiplexer
MAX378	1	92	8-Channel, High-Voltage, Fault-Protected Multiplexer
MAX379	1	92	Differential 4-Channel, High-Voltage, Fault-Protected Multiplexer
MAX381	0	96	Precision, Dual, Low-Voltage, SPST CMOS Analog Switch
MAX382	0	96	Low-Voltage, 1-of-8 CMOS Multiplexer with Latchable Inputs
MAX383	0	96	Precision, Dual, Low-Voltage, SPDT CMOS Analog Switch

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Part	Current DS Rev. No.	Data Book Year/97 Book Page No.	Description
MAX384	0	96	Low-Voltage, Dual, 4-Channel CMOS Multiplexer with Latchable Inputs
MAX385	0	96	Precision, Dual, Low-Voltage, DPST CMOS Analog Switch
MAX388	2	93	8-Channel, High-Voltage, Fault-Protected Multiplexer
MAX389	2	93	Differential 4-Channel, High-Voltage, Fault-Protected Multiplexer
MAX391	0	95	Low-Voltage, 5V/±5V Quad, CMOS Analog Switch
MAX392	0	95	Low-Voltage, 5V/±5V Quad, CMOS Analog Switch
MAX393	0	95	Low-Voltage, 5V/±5V Quad, CMOS Analog Switch
MAX394	0	96	Low-Voltage, Quad SPDT, CMOS Analog Switch—Replaces MAX333A
MAX395	**0**	**1-41**	**Low-Voltage, Serially Controlled, Octal SPST Analog Switch**
MAX396	1	96	Precision, 16-Channel, Low-Voltage, CMOS Analog Multiplexer—DG406 Pinout
MAX397	1	96	Precision, Dual, 8-Channel, Low-Voltage, CMOS Analog Multiplexer—DG407 Pinout
MAX398	2	96	Precision, 8-Channel, Low-Voltage, CMOS Analog Multiplexer—DG408 Pinout
MAX399	2	96	Precision, Dual, 4-Channel, Low-Voltage, CMOS Analog Multiplexer
MAX400	0	—	Ultra-Low-Offset Op Amp
MAX402	2	94	High-Speed, Low-Voltage, Micropower Op Amp
MAX403	2	94	High-Speed, Low-Voltage, Micropower Op Amp
MAX404	0	92	Video Op Amp
MAX405	1	92	Precision Video Buffer Amplifier
MAX406	2	94	Single, 1.2µA Max, Single-Supply Op Amp
MAX407	2	94	Dual, 1.2µA Max, Single-Supply Op Amp
MAX408	0	—	High-Speed, High Output Current Op Amp
MAX409	2	94	Single, 1.2µA Max, 150kHz, Single-Supply Op Amp
MAX410	1	94	Single, 28MHz, Low-Noise, Low-Voltage, Precision Op Amp
MAX412	1	94	Dual, 28MHz, Low-Noise, Low-Voltage, Precision Op Amp
MAX414	1	94	Quad, 28MHz, Low-Noise, Low-Voltage, Precision Op Amp
MAX417	2	94	Dual, 1.2µA Max, Single-Supply Op Amp
MAX418	2	94	Quad, 1.2µA Max, Single-Supply Op Amp
MAX419	2	94	Quad, 1.2µA Max, Single-Supply Op Amp
MAX420	1	—	±15V Chopper-Stabilized Op Amp
MAX421	1	—	±15V Chopper-Stabilized Op Amp
MAX422	1	—	Low-Power, ±15V Chopper-Stabilized Op Amp
MAX423	1	—	Low-Power, ±15V Chopper-Stabilized Op Amp
MAX427	0	94	Low-Noise, High-Precision Op Amp
MAX428	0	—	Dual, High-Speed, High-Output-Current Op Amp
MAX430	1	—	±15V Chopper-Stabilized Op Amp
MAX432	1	—	Low-Power, ±15V Chopper-Stabilized Op Amp
MAX435	1	94	275MHz Wideband Transconductance Amplifier with Differential Output
MAX436	1	94	200MHz Wideband Transconductance Amplifier with Single-Ended Output

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Alphanumeric Index

A Complete Product Listing

Part	Current DS Rev. No.	Data Book Year/97 Book Page No.	Description
MAX437	0	94	Low-Noise, High-Precision Op Amp
MAX438	2	94	High-Speed, Low-Voltage, Micropower Op Amp
MAX439	2	94	High-Speed, Low-Voltage, Micropower Op Amp
MAX440	1	93	8-Channel, High-Speed, Video Multiplexer/Amplifier
MAX441	1	93	4-Channel, High-Speed, Video Multiplexer/Amplifier
MAX442	1	93	2-Channel, 140MHz, Video Multiplexer/Amplifier
MAX445	0	95*	High-Voltage, 200MHz Video CRT Driver
MAX448	0	—	Quad, High-Speed, High-Output-Current Op Amp
MAX451	0	—	Low-Bias-Current, 10MHz Video Amplifier
MAX452	0	92	50MHz Video Amplifier and Multiplexer/Amplifier
MAX453	0	92	50MHz Video Amplifier and Multiplexer/Amplifier
MAX454	0	92	50MHz Video Amplifier and Multiplexer/Amplifier
MAX455	0	92	50MHz Video Amplifier and Multiplexer/Amplifier
MAX456	2	—	8x8 Crosspoint Video Switch
MAX457	0	92	Dual, 70MHz Video Amplifier
MAX458	2	95	8x4 Video Crosspoint Switches with Buffers
MAX459	2	95	8x4 Video Crosspoint Switches with Buffers
MAX459EVKIT	2	—	Evaluation Kit for the MAX458/MAX459
MAX460	0	—	High-Accuracy Fast Buffer
MAX463	2	95	100MHz, Triple RGB Video Switch with Gain of +1 Buffer
MAX464	2	95	100MHz, Quad RGB Video Switch with Gain of +1 Buffer
MAX465	2	95	90MHz, Triple RGB Video Switch with Gain of +2 Buffer
MAX466	2	95	90MHz, Quad RGB Video Switch with Gain of +2 Buffer
MAX466EVKIT	2	—	Evaluation Kit for the MAX464/MAX466
MAX467	2	95	100MHz, Triple RGB Video Gain of +1 Buffer
MAX468	2	95	100MHz, Quad Gain of +1 Video Buffer
MAX469	2	95	90MHz, Triple RGB Video Gain of +2 Buffer
MAX470	2	95	90MHz, Quad Gain of +2 Video Buffer
MAX471	1	96	Precision, High-Side Current-Sense Amplifier
MAX472	1	96	Precision, High-Side Current-Sense Amplifier
MAX473	1	96	Single, 10MHz, 15V/µs, Single-Supply Op Amp
MAX474	1	96	Dual, 10MHz, 15V/µs, Single-Supply Op Amp
MAX475	1	96	Quad, 10MHz, 15V/µs, Single-Supply Op Amp
MAX476	†	**8-7***	**375MHz High-Speed Op Amp with Shutdown**
MAX477	**1**	**8-9**	**300MHz High-Speed Amplifier**
MAX477EVKIT	0	—	Evaluation Kit for the MAX477
MAX478	0	94	Dual, 17µA Max, Single-Supply, Precision Op Amp
MAX479	0	94	Quad, 17µA Max, Single-Supply, Precision Op Amp
MAX480	2	92	High-Precision, Low-Voltage, Micropower Op Amp
MAX481	5	95	500µA RS-485 Transceiver with Low-Power Shutdown
MAX481E	**3**	**2-31**	**2.5Mbps, ±15kV ESD-Protected, Low-Power RS-485/RS-422 Transceiver**

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Alphanumeric Index

A Complete Product Listing

Part	Current DS Rev. No.	Data Book Year/97 Book Page No.	Description
MAX483	5	95	Slew-Rate-Limited, 350µA RS-485 Transceiver with Low-Power Shutdown
MAX483E	**3**	**2-31**	**250kbps, ±15kV ESD-Protected, Low-Power RS-485/RS-422 Transceiver with Shutdown**
MAX485	5	95	500µA, RS-485 Transceiver—Direct LTC485 Replacement
MAX485E	**3**	**2-31**	**2.5Mbps, ±15kV ESD-Protected, Low-Power RS-485/RS-422 Transceiver**
MAX487	5	95	Slew-Rated-Limited, 350µA RS-485 Transceiver with 1/4-Unit Load
MAX487E	**3**	**2-31**	**250kbps, ±15kV ESD-Protected, Low-Power RS-485/RS-422 Transceiver with 1/4-Unit Load**
MAX488	5	95	Slew-Rated-Limited, 350µA, Full-Duplex RS-485 Transceiver
MAX488E	**3**	**2-31**	**250kbps, ±15kV ESD-Protected, Low-Power, Full-Duplex RS-485/RS-422 Transceiver**
MAX489	5	95	Slew-Rated-Limited, 350µA, Full-Duplex RS-485 Transceiver
MAX489E	**3**	**2-31**	**250kbps, ±15kV ESD-Protected, Low-Power, Full-Duplex RS-485/RS-422 Transceiver**
MAX490	5	95	500µA, Full-Duplex RS-485 Transceiver
MAX490E	**3**	**2-31**	**2.5Mbps, ±15kV ESD-Protected, Low-Power RS-485/RS-422 Transceiver**
MAX491	5	95	500µA, Full-Duplex RS-485 Transceiver
MAX491E	**3**	**2-31**	**2.5Mbps, ±15kV ESD-Protected, Low-Power RS-485/RS-422 Transceiver**
MAX492	1	96	Dual, Micropower, Single-Supply, Rail-to-Rail, I/O Op Amp
MAX494	1	96	Quad, Micropower, Single-Supply, Rail-to-Rail, I/O Op Amp
MAX495	1	96	Single, Micropower, Single-Supply, Rail-to-Rail, I/O Op Amp
MAX496	**0**	**8-21**	**375MHz, Quad, Gain of +1 Video Buffer**
MAX497	**0**	**8-21**	**275MHz, Quad, Gain of +2 Video Buffer**
MAX497EVKIT	0	—	Evaluation Kit for the MAX496/MAX497
MAX498	**0**	**8-33**	**310MHz, RGB + Sync Video Multiplexer with High-Speed Amplifier**
MAX499	**0**	**8-33**	**310MHz, RGB + Sync Video Multiplexer with High-Speed Amplifier**
MAX500	2	—	CMOS, Quad, Serial 8-Bit DAC
MAX501	0	93	Voltage-Output, Multiplying, 12-Bit DAC with 8+4 Interface
MAX502	0	93	Voltage-Output, Multiplying, 12-Bit DAC with 12-Bit Interface
MAX503	0	96	5V, Low-Power, Parallel-Input, Voltage-Output, 10-Bit DAC
MAX504	1	96	5V, Low-Power, Voltage-Output, Serial, 10-Bit DAC with Internal Reference
MAX505	2	—	Quad, 8-Bit DAC with Rail-to-Rail Outputs
MAX506	2	—	Quad, 8-Bit DAC with Rail-to-Rail Outputs
MAX507	A	93	Voltage-Output, 12-Bit DAC with Internal Reference and 12-Bit Interface
MAX508	A	93	Voltage-Output, 12-Bit DAC with Internal Reference and 8+4 Interface
MAX509	2	—	Quad, Serial, 8-Bit DAC with Rail-to-Rail Outputs
MAX510	2	—	Quad, Serial, 8-Bit DAC with Rail-to-Rail Outputs
MAX512	2	95	5V, Triple, Voltage-Output, Serial, 8-Bit DAC
MAX513	2	95	3V, Triple, Voltage-Output, Serial, 8-Bit DAC

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Alphanumeric Index

A Complete Product Listing

Part	Current DS Rev. No.	Data Book Year/97 Book Page No.	Description
MAX514	0	93	Quad, CMOS, Serial, Multiplying, 12-Bit DAC
MAX515	1	96	5V, Low-Power, Voltage-Output, Serial, 10-Bit DAC
MAX516	1	92	Quad, DAC-Programmed, CMOS Comparator
MAX517	0	96	Single, 2-Wire, Serial, 8-Bit DAC with Rail-to-Rail Outputs
MAX518	0	96	Dual, 2-Wire, Serial, 8-Bit DAC with Rail-to-Rail Outputs in 8-Pin Package
MAX519	0	96	Dual, 2-Wire, Serial, 8-Bit DAC with Rail-to-Rail Outputs
MAX520A/B	**2**	**9-7**	**Quad, 2-Wire, Serial, 8-Bit DAC with Unbuffered Outputs**
MAX521	**2**	**9-7**	**Octal, 2-Wire, Serial, 8-Bit DAC with Rail-to-Rail Outputs**
MAX522	0	96	Dual, Voltage-Output, Serial, 8-Bit DAC in 8-Pin Package
MAX525	**1**	**9-25**	**Lowest Power, +5V, Serial, Quad 12-Bit DAC**
MAX526	3	93	Calibrated, Quad, Voltage-Output, 12-Bit DAC
MAX527	3	93	±5V, Calibrated, Quad, Voltage-Output, 12-Bit DAC
MAX528	2	93	Octal, Serial, 8-Bit DAC with Output Buffers
MAX529	2	93	±5V, Octal, Serial, 8-Bit DAC with Output Buffers
MAX530	3	95	5V, Low-Power, Voltage-Output, Parallel, 12-Bit DAC with Reference
MAX531	4	95	5V, Low-Power, Voltage-Output, Serial, 12-Bit DAC with Reference
MAX532	1	95	Dual, Serial-Input, Voltage-Output, Multiplying, 12-Bit DAC
MAX533	**0**	**9-41**	**+3V, Serial, Quad 8-Bit DAC in QSOP Package**
MAX534	**0**	**9-57**	**+5V, Serial, Quad 8-Bit DAC in QSOP Package**
MAX535	**0**	**9-71**	**+5V, 13-Bit, Serial, Voltage-Output DAC in 8-Pin µMAX Package**
MAX536	1	95	Quad, Serial, Voltage-Output, 12-Bit DAC
MAX537	1	95	Quad, Serial, Voltage-Output, ±5V, 12-Bit DAC
MAX538	4	95	5V, Low-Power, Voltage-Output, Serial, 12-Bit DAC, 0V to 2.6V Output
MAX539	4	95	5V, Low-Power, Voltage-Output, Serial, 12-Bit DAC, 0V to 4.5V Output
MAX541	**1**	**9-83**	**+5V, 16-Bit, Serial, Voltage-Output DAC in 8-Pin Package**
MAX542	**1**	**9-83**	**+5V, 16-Bit, Serial, Voltage-Output DAC with Bipolar Output Configuration**
MAX543	1	—	Serial, CMOS, Multiplying, 12-Bit DAC in 8-Pin Package
MAX544	**2**	**9-95**	**+5V, 14-Bit, Serial, Voltage-Output DAC in 8-Pin Package**
MAX545	**2**	**9-95**	**+5V, 14-Bit, Serial, Voltage-Output DAC with Bipolar Output Configuration**
MAX547	3	95	Octal, Voltage-Output, 13-Bit DAC with Parallel Interface
MAX549	**1**	**9-107**	**2.7V to 5.5V, 8-Bit, Dual, Voltage-Output DAC in 8-Pin Package**
MAX550B	**0**	**9-115**	**2.7V to 5.5V, 8-Bit, Single, Serial, Voltage-Output DAC in 8-Pin Package**
MAX555	1	96	300Msps, 12-Bit DAC with Complementary Voltage Outputs
MAX555EVKIT	1	—	Evaluation Kit for the MAX555
MAX560	0	93	3.3V Transceiver with Two EIA/TIA-562 Receivers Active in Shutdown
MAX561	0	93	3.3V Transceiver with Two EIA/TIA-562 Receivers Active in Shutdown
MAX562	0	95	2.7V to 5.25V, High-Speed RS-232 Serial Port
MAX563	0	95	3.3V, Dual EIA/TIA-562 Transceiver
MAX603	0	96	5V or Adjustable, Low-Dropout, Low I_Q, 500mA Linear Regulator

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Alphanumeric Index

A Complete Product Listing

Part	Current DS Rev. No.	Data Book Year/97 Book Page No.	Description
MAX604	0	96	3.3V or Adjustable, Low-Dropout, Low I_Q, 500mA Linear Regulator
MAX606	**0**	**4-11**	**Low-Profile, 0.8MHz, Step-Up DC-DC Converter for Type 1 Flash Memory/PCMCIA Cards**
MAX606EVKIT	0	—	Evaluation Kit for the MAX606/MAX607
MAX607	**0**	**4-11**	**Low-Profile, 0.4MHz, Step-Up DC-DC Converter for Type 2 and 3 Flash Memory/PCMCIA Cards**
MAX608	**0**	**4-23**	**Low-Input-Voltage, High-Efficiency, Step-Up DC-DC Controller**
MAX608EVKIT	0	—	Evaluation Kit for the MAX608
MAX613	0	95	Dual-Slot, PCMCIA Analog Power Controller
MAX614	0	95	Single-Slot, PCMCIA Analog Power Controller
MAX619	2	95	Regulated 5V Charge-Pump DC-DC Converter
MAX619EVKIT	1	—	Evaluation Kit for the MAX619
MAX620	2	—	Quad, High-Side MOSFET Driver
MAX621	2	—	Quad, High-Side MOSFET Driver
MAX622	0	92	High-Side Power Supply
MAX623	0	92	High-Side Power Supply
MAX624	1	96	Dual-Output, 1MHz, DC-DC Boost Converter for PCMCIA Applications
MAX625	1	93	See MAX620
MAX626	1	—	Dual-Power MOSFET Driver (Inverting)
MAX627	1	—	Dual-Power MOSFET Driver (Noninverting)
MAX628	1	—	Dual-Power MOSFET Driver (Inverting & Noninverting)
MAX630	0	92	CMOS, Micropower, Step-Up Switching Regulator
MAX631	0	92	5V/Adjustable, Step-Up Switching Regulator
MAX632	0	92	12V/Adjustable, CMOS, Step-Up Switching Regulator
MAX633	0	92	15V/Adjustable, CMOS, Step-Up Switching Regulator
MAX634	0	92	CMOS, Micropower, Inverting Switching Regulator
MAX635	1	92	-5V/Adjustable, CMOS, Inverting Switching Regulator
MAX636	1	92	-12V/Adjustable, CMOS, Inverting Switching Regulator
MAX637	1	92	-15V/Adjustable, CMOS, Inverting Switching Regulator
MAX638	0	92	5V/Adjustable, CMOS, Step-Down Switching Regulator
MAX639	2	95	5V/Adjustable, High-Efficiency, Low I_Q, Step-Down DC-DC Converter
MAX639EVKIT	0	—	Evaluation Kit for the MAX639/MAX640/MAX653
MAX640	2	95	3.3V/Adjustable, High-Efficiency, Low I_Q, Step-Down DC-DC Converter
MAX641	0	92	5V/Adjustable, 10W, CMOS, Step-Up, Switching Regulator Controller
MAX642	0	92	12V/Adjustable, 10W, CMOS, Step-Up, Switching Regulator Controller
MAX643	0	92	15V/Adjustable, 10W, CMOS, Step-Up, Switching Regulator Controller
MAX649	2	95	5V/Adjustable, High-Efficiency, Low I_Q, Step-Down DC-DC Controller
MAX651	2	95	3.3V/Adjustable, High-Efficiency, Low I_Q, Step-Down DC-DC Controller
MAX652	2	95	3V/Adjustable, High-Efficiency, Low I_Q, Step-Down DC-DC Controller
MAX653	2	95	3V/Adjustable, High-Efficiency, Low I_Q, Step-Down DC-DC Converter
MAX660	2	92	100mA, Charge-Pump Voltage Converter
MAX662	1	94	Replaced by MAX662A

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Alphanumeric Index

A Complete Product Listing

Part	Current DS Rev. No.	Data Book Year/97 Book Page No.	Description
MAX662A	1	95	12V, 30mA Flash Memory Programming Supply
MAX662EVKIT	1	—	Evaluation Kit for the MAX662A
MAX663	0	92	CMOS, 5V/Adjustable, Micropower, Positive Linear Regulator
MAX664	0	92	CMOS, -5V/Adjustable, Micropower, Negative Linear Regulator
MAX665	0	93	100mA, 1.5V to 8V, CMOS, Switched-Capacitor Voltage Converter
MAX666	0	92	5V/Adjustable, Micropower, Positive Linear Regulator with Low-Battery Detector
MAX667	3	95	5V/Programmable, Low-Dropout Voltage Regulator
MAX670	0	—	Precision, 3ppm/°C, 10V Kelvin-Sensed Reference
MAX671	0	—	Precision, 1ppm/°C, 10V Kelvin-Sensed Reference
MAX672	0	—	Replaced by MAX674
MAX673	0	—	Replaced by MAX675
MAX674	0	92	Precision, 10V Voltage Reference
MAX675	0	92	Precision, 5V Voltage Reference
MAX676	2	95*	Calibrated, 1ppm/°C, Low-Drift, 4.096V Precision Voltage Reference
MAX677	2	95*	Calibrated, 1ppm/°C, Low-Drift, 5V Precision Voltage Reference
MAX678	1	95*	Calibrated, 1ppm/°C, Low-Drift, 10V Precision Voltage Reference
MAX680	0	92	5V to ±10V, Switched-Capacitor Voltage Converter
MAX681	0	92	5V to ±10V, Switched-Capacitor Voltage Converter
MAX687	0	96	3.3V, Low-Noise, Linear Regulator Controller with Automatic Shutdown
MAX688	0	96	3.3V, Low-Noise, Linear Regulator Controller
MAX688EVKIT	0	—	Evaluation Kit for the MAX688/MAX689
MAX689	0	96	3V, Low-Noise, Linear Regulator Controller
MAX690	2	—	µP Reset IC with Watchdog and Battery Switchover
MAX690A	3	95	µP Reset IC with Watchdog and Battery Switchover
MAX690R/S/T	1	95	µP Reset IC with Watchdog and Battery Switchover
MAX691	2	—	µP Reset IC with Watchdog and Battery Switchover
MAX691A	6	95	µP Reset IC with Watchdog, Chip Enable, and Battery Backup
MAX692	2	—	µP Reset IC with Watchdog and Battery Switchover
MAX692A	3	95	µP Reset IC with Watchdog and Battery Switchover
MAX693	2	—	µP Reset IC with Watchdog and Battery Switchover
MAX693A	6	—	µP Reset IC with Watchdog, Chip Enable, and Battery Backup
MAX694	2	—	µP Reset IC with Watchdog and Battery Switchover
MAX695	2	—	µP Reset IC with Watchdog and Battery Switchover
MAX696	0	92	µP Supervisor with Battery Switchover and Programmable Reset
MAX697	0	92	µP Supervisor with Programmable Reset
MAX698	0	92	Low-Cost Power-On Reset IC
MAX699	0	92	Low-Cost Power-On Reset IC with Watchdog Controller
MAX700	0	92	Adjustable-Threshold Power-Supply Monitor with Reset
MAX701	0	92	Power-Supply Monitor with Reset
MAX702	0	92	Power-Supply Monitor with Reset
MAX703	1	94	µP Reset IC with Battery Backup

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Alphanumeric Index

A Complete Product Listing

Part	Current DS Rev. No.	Data Book Year / 97 Book Page No.	Description
MAX704	1	94	µP Reset IC with Battery Backup
MAX704R/S/T	0	95	3V µP Reset IC with Battery Backup
MAX705	5	95	µP Reset IC with Watchdog
MAX706	5	95	µP Reset IC with Watchdog
MAX706P/R/S/T	2	95	3V µP Reset IC with Watchdog
MAX707	5	95	µP Reset IC with Power-Fail Warning
MAX708	5	95	µP Reset IC with Power-Fail Warning
MAX708R/S/T	2	95	3V µP Reset IC with Power-Fail Warning
MAX709L/M/R/S/T	1	94	Power-Supply Monitor with Reset
MAX710	†	**4-35***	**3V/5V-Output, Step-Up DC-DC Converter**
MAX710EVKIT	†	—	Evaluation Kit for the MAX710/MAX711
MAX711	†	**4-35***	**Adjustable-Output, Step-Up DC-DC Converter**
MAX712	2	94	Battery Fast-Charge Controller (NiMH)
MAX712EVKIT	2	—	Evaluation Kit for the MAX712/MAX713
MAX713	2	94	Battery Fast-Charge Controller (NiCd)
MAX714	2	93	3-Output, Battery-Powered Supply System
MAX715	2	93	6-Output, Battery-Powered Supply System
MAX716	2	93	7-Output, Battery-Powered Supply System
MAX717	0	94	3.3V Palmtop Computer and Flash Memory Power-Supply Regulator
MAX718	0	94	3.3V/5V Palmtop Computer and Flash Memory Power-Supply Regulator
MAX718EVKIT	0	—	Evaluation Kit for the MAX717/MAX718/MAX719
MAX719	0	94	3V/5V Palmtop Computer and Flash Memory Power-Supply Regulator
MAX720	0	94	3.3V/5V Palmtop Computer and Flash Memory Power-Supply Regulator
MAX721	0	94	3V/5V Palmtop Computer and Flash Memory Power-Supply Regulator
MAX722	0	93	3.3V/5V Palmtop Computer and LCD Power-Supply Regulator
MAX722EVKIT	0	—	Evaluation Kit for the MAX722/MAX723
MAX723	0	93	3V Palmtop Computer and LCD Power-Supply Regulator
MAX724	3	94	5A, Step-Down, PWM, Switch-Mode DC-DC Converter
MAX726	3	94	2A, Step-Down, PWM, Switch-Mode DC-DC Converter
MAX727	2	94	2A, 5V, Step-Down, PWM, Switch-Mode DC-DC Converter
MAX728	2	94	2A, 3.3V, Step-Down, PWM, Switch-Mode DC-DC Converter
MAX729	2	94	2A, 3V, Step-Down, PWM, Switch-Mode DC-DC Converter
MAX730	0	94	Replaced by MAX730A
MAX730A	2	95	5V, Step-Down, Current-Mode, PWM DC-DC Converter
MAX731	2	—	5V, Step-Up, Current-Mode, PWM DC-DC Converter
MAX731EVKIT	0	—	Evaluation Kit for the MAX731
MAX732	1	93	12V, Step-Up, Current-Mode, PWM DC-DC Converter
MAX732EVKIT	1	—	Evaluation Kit for the MAX732
MAX733	1	93	15V, Step-Up, Current-Mode, PWM DC-DC Converter
MAX734	2	94	12V, 120mA Flash Memory Programming Supply
MAX734EVKIT	2	—	Evaluation Kit for the MAX734
MAX735	1	94	-5V, Inverting, PWM DC-DC Converter

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Alphanumeric Index

A Complete Product Listing

Part	Current DS Rev. No.	Data Book Year/97 Book Page No.	Description
MAX736	3	—	-12V, Inverting, PWM, Current-Mode DC-DC Converter
MAX737	3	—	-15V, Inverting, PWM, Current-Mode DC-DC Converter
MAX738	0	93	Replaced by MAX738A
MAX738EVKIT	n/a	—	Evaluation Kit for the MAX730A/MAX738A/MAX744A/MAX748A/MAX763A
MAX738A	2	95	5V, Step-Down, PWM, Current-Mode DC-DC Converter
MAX739	3	93	-5V, Inverting, PWM, Current-Mode DC-DC Converter
MAX739EVKIT	3	—	Evaluation Kit for the MAX736/MAX737/MAX739/MAX759
MAX741	1	94	Pin-Programmed, Low-Voltage, PWM Current-Mode Controller
MAX742	1	92	Switch-Mode Regulator with 5V to ±1V or ±15V Dual Output
MAX742EVKIT	1	—	Evaluation Kit for the MAX742
MAX743	0	92	Dual-Output, PWM Switch-Mode Regulator (5V to ±15V or ±12V)
MAX743EVKIT	0	—	Evaluation Kit for the MAX743
MAX744A	2	95	5V, Step-Down, PWM, Current-Mode DC-DC Converter
MAX746	1	—	High-Efficiency, PWM, Step-Down, N-Channel DC-DC Controller
MAX747	1	94	High-Efficiency, PWM, Step-Down Controller (External P-Channel Driver)
MAX748A	0	95	3.3V, PWM, Step-Down DC-DC Converter
MAX749	1	94	Digitally Adjustable LCD Bias Supply
MAX749EVKIT	1	—	Evaluation Kit for the MAX749
MAX750	0	93	Replaced by MAX750A
MAX750A	0	95	Adjustable, PWM, Step-Down Regulator
MAX751	0	94	5V, Step-Up, PWM, Current-Mode DC-DC Converter
MAX752	2	93	Adjustable, Step-Up, PWM, Current-Mode DC-DC Converter
MAX752EVKIT	0	—	Evaluation Kit for the MAX732/MAX733/MAX752
MAX753	1	—	CCFT Backlight and LCD Negative Contrast Controller
MAX754	1	—	CCFT Backlight and LCD Positive Contrast Controller
MAX755	1	94	Adjustable, PWM, Inverting DC-DC Converter
MAX756	2	—	3.3V/5V, High-Efficiency, Step-Up DC-DC Converter
MAX756EVKIT	2	—	Evaluation Kit for the MAX756/MAX757
MAX757	2	—	3.3V/5V, High-Efficiency, Step-Up DC-DC Converter
MAX758	0	93	Replaced by MAX758A
MAX758EVKIT	n/a	—	Evaluation Kit for the MAX750A/MAX758A
MAX758A	0	95	Adjustable, PWM, Step-Down DC-DC Converter
MAX759	3	—	Adjustable, Inverting, PWM, Current-Mode DC-DC Converter
MAX759LCDEVKIT	3	—	Evaluation Kit for the MAX759
MAX761	0	95	12V/Adjustable, High-Efficiency, Low I_Q, Step-Up DC-DC Converter
MAX761EVKIT	0	—	Evaluation Kit for the MAX761/MAX762
MAX762	0	95	15V/Adjustable, High-Efficiency, Low I_Q, Step-Up DC-DC Converter
MAX763A	0	95	3.3V, PWM, Step-Down DC-DC Converter
MAX764	0	95	-5V/Adjustable, High-Efficiency, Low I_Q, Inverting DC-DC Converter
MAX764EVKIT	0	—	Evaluation Kit for the MAX764/MAX765/MAX766
MAX765	0	95	-12V/Adjustable, High-Efficiency, Low I_Q, Inverting DC-DC Converter
MAX766	0	95	-15V/Adjustable, High-Efficiency, Low I_Q, Inverting DC-DC Converter

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Alphanumeric Index

A Complete Product Listing

Part	Current DS Rev. No.	Data Book Year/97 Book Page No.	Description
MAX767	2	95	5V Supply to 3.3V Output, Synchronous, Step-Down Power-Supply Controller
MAX767EVKIT	1	—	Evaluation Kit for the MAX767
MAX770	1	95	5V/Adjustable, High-Efficiency, Low I_Q, Step-Up DC-DC Controller
MAX770EVKIT	0	—	Evaluation Kit for the MAX770/MAX771/MAX772
MAX771	0	95	12V/Adjustable, High-Efficiency, Low I_Q, Step-Up DC-DC Controller
MAX772	0	95	15V/Adjustable, High-Efficiency, Low I_Q, Step-Up DC-DC Controller
MAX773	0	95	5V/12V/15V/Adjustable, High-Voltage, High-Efficiency, Low I_Q, Step-Up DC-DC Controller
MAX774	1	95	-5V or Adjustable, High-Efficiency, Low I_Q, Inverting DC-DC Controller
MAX774EVKIT	0	—	Evaluation Kit for the MAX774/MAX775/MAX776
MAX775	1	95	-12V or Adjustable, High-Efficiency, Low I_Q, Inverting DC-DC Controller
MAX776	1	95	-15V or Adjustable, High-Efficiency, Low I_Q, Inverting DC-DC Controller
MAX777	—	95	Replaced by MAX777L
MAX777L	2	—	1V-Input, 5V-Output, Step-Up DC-DC Converter
MAX778	—	95	Replaced by MAX778L
MAX778L	2	—	1V-Input, 3V/3.3V-Output, Step-Up DC-DC Converter
MAX778LEVKIT	2	—	Evaluation Kit for the MAX777L/MAX778L/MAX779L
MAX779	—	95	Replaced by MAX779L
MAX779L	2	—	1V-Input, Adjustable-Output, Step-Up DC-DC Converter
MAX780	1	—	Dual-Slot, PCMCIA Analog Power Controller
MAX781	0	—	PDA/Hand-Held Computer Power Controller
MAX782	2	—	Triple-Output Power-Supply Controller for Notebook Computers
MAX782EVKIT	n/a	—	Evaluation Kit for the MAX782
MAX783	1	—	3.3V/5V Notebook Computer Power Supply, Dual PCMCIA VPP Outputs (6-Cell Input)
MAX783EVKIT	1	—	Evaluation Kit for the MAX783
MAX786	1	95	3.3V/5V Notebook Computer Power Supply with 25µA Shutdown
MAX786EVKIT	1	—	Evaluation Kit for the MAX786
MAX787	3	95	5V, 5A Step-Down, PWM, Switch-Mode DC-DC Regulator
MAX788	3	95	3.3V, 5A Step-Down, PWM, Switch-Mode DC-DC Regulator
MAX789	3	95	3V, 5A Step-Down, PWM, Switch-Mode DC-DC Regulator
MAX791	5	—	µP Supervisory Circuit
MAX792L/M/R/S/T	1	—	µP and Non-Volatile Memory Supervisory Circuit
MAX793R/S/T	1	96	3V/3.3V µP Supervisory Circuit
MAX794	1	96	3V/3.3V Adjustable, µP Supervisory Circuit
MAX795R/S/T	1	96	3V/3.3V µP Supervisory Circuit
MAX796	2	96	Step-Down, PWM Controller with Synchronous Rectifier for CPU Power with Positive Secondary
MAX796EVKIT	2	—	Evaluation Kit for the MAX796/MAX799
MAX797	2	96	Step-Down, PWM Controller with Synchronous Rectifier for CPU Power with Low-Noise Pin

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Alphanumeric Index

A Complete Product Listing

Part	Current DS Rev. No.	Data Book Year/97 Book Page No.	Description
MAX797EVKIT	2	—	Evaluation Kit for the MAX797
MAX798	†	**4-37***	**Step-Down, PWM Controller with Synchronous Rectifier for CPU Power, Adjustable from 5.5V to 1.6V**
MAX799	2	96	Step-Down, PWM Controller with Synchronous Rectifier for CPU Power with Negative Secondary
MAX800L/M	6	—	µP Reset IC with Watchdog, Battery Switchover, and ±2% Power-Fail Accuracy
MAX801L/M/N	**0**	**5-5**	**8-Pin µP Supervisory Circuit with ±1.5% Accuracy and Watchdog Timer**
MAX802L/M	3	95	High-Accuracy µP Reset IC with Watchdog and Battery Backup
MAX802R/S/T	0	95	3V, High-Accuracy µP Reset IC with Watchdog and Battery Backup
MAX804R/S/T	0	95	3V, High-Accuracy µP Reset IC (asserted high) with Watchdog and Battery Backup
MAX805L	3	95	µP Reset IC (asserted high) with Watchdog and Battery Backup
MAX805R/S/T	0	95	3V µP Reset IC (asserted high) with Watchdog and Battery Backup
MAX806R/S/T	0	95	3V, High-Accuracy µP Reset IC with Battery Backup
MAX807L/M/N	0	96*	µP Supervisory Circuit with ±1.5% Reset Accuracy
MAX808L/M/N	**0**	**5-5**	**8-Pin µP Supervisory Circuit with ±1.5% Reset Accuracy and On-Board Gating of Chip Enable**
MAX809L/M/R/S/T	2	96*	3-Pin µP Reset Circuit
MAX810L/M/R/S/T	2	96*	3-Pin µP Reset Circuit
MAX811L/M/R/S/T	1	96	4-Pin µP Voltage Monitor with Manual RESET Output
MAX812L/M/R/S/T	1	96*	4-Pin µP Voltage Monitor with Manual RESET Output
MAX813L	5	95	µP Reset IC (asserted high) with Watchdog
MAX814K/L/N/T	0	96	High-Accuracy, 1%, Low-Power, 3V and 5V µP Supervisory Circuit
MAX815K/L/N/T	0	96	High-Accuracy, 1%, Low-Power, 3V and 5V µP Supervisory Circuit
MAX816	0	96	High-Accuracy, 1%, Low-Power, Adjustable µP Supervisory Circuit
MAX817L/M	**1**	**5-17**	**5V µP Supervisory Circuit**
MAX818L/M	**1**	**5-17**	**5V µP Supervisory Circuit in a µMAX Package**
MAX819L/M	**1**	**5-17**	**5V µP Supervisory Circuit with Manual Reset Input**
MAX820L/M/R/S/T	1	—	µP and Non-Volatile Memory Supervisory Circuit
MAX821L/M/R/S/T	**0**	**5-33**	**4-Pin µP Supervisory Circuit with Active-Low Reset**
MAX822L/M/R/S/T	**0**	**5-33**	**4-Pin µP Supervisory Circuit with Active-High Reset**
MAX823L/M/R/S/T	**0**	**5-41**	**5-Pin µP Supervisory Circuit with Watchdog Input and Manual-Reset Input**
MAX824L/M/R/S/T	**0**	**5-41**	**5-Pin µP Supervisory Circuit with Watchdog Input and Active-High Reset**
MAX825L/M/R/S/T	**0**	**5-41**	**5-Pin µP Supervisory Circuit with Manual-Reset Input and Active-High Reset**
MAX828	**2**	**4-39**	**Ultra-Small, 25mA Inverting Charge Pumps in SOT23**
MAX829	**2**	**4-39**	**Ultra-Small, 25mA Inverting Charge Pumps in SOT23**

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Alphanumeric Index

A Complete Product Listing

Part	Current DS Rev. No.	Data Book Year/97 Book Page No.	Description
MAX830	2	96	1A, Adjustable V_{OUT}, Step-Down, PWM DC-DC Converter— Surface Mountable
MAX831	2	96	1A, 5V, Step-Down, PWM DC-DC Converter—Surface Mountable
MAX831EVKIT	2	—	Evaluation Kit for the MAX830–MAX833
MAX832	2	96*	1A, 3.3V, Step-Down, PWM DC-DC Converter—Surface Mountable
MAX833	2	96*	1A, 3V, Step-Down, PWM DC-DC Converter—Surface Mountable
MAX834	**0**	**10-3***	**5-Pin, Micropower, Latching Voltage Monitor with Open-Drain Output**
MAX835	**0**	**10-3***	**5-Pin, Micropower, Latching Voltage Monitor with Push/Pull Output**
MAX836	**0**	**10-5**	**4-Pin, Micropower Voltage Monitor with Open-Drain Output**
MAX837	**0**	**10-5**	**4-Pin, Micropower Voltage Monitor with Push/Pull Output**
MAX840	1	96	Low-Noise, Regulated, -2V GaAsFET Bias
MAX840EVKIT	1	—	Evaluation Kit for the MAX840/MAX843/MAX844
MAX843	1	96	Low-Noise, Regulated, -2V GaAsFET Bias with Adjustable Reference
MAX844	1	96	Low-Noise, Regulated, -2V GaAsFET Bias with LCD Output
MAX845	3	96	750mW Isolated Transformer Driver for PCMCIA Applications
MAX845EVKIT	3	—	Evaluation Kit for the MAX845
MAX846A	**0**	**4-47**	**Cost-Saving, Chemistry-Independent Battery-Charger System**
MAX846EVKIT	†	—	Evaluation Kit for the MAX846
MAX848	**1**	**4-59**	**1 to 3 Cell, High Power, Low-Noise, Step-Up DC-DC Converter with 0.5A MOSFET Power Switch**
MAX848EVKIT	†	—	Evaluation Kit for the MAX848/MAX849
MAX849	**1**	**4-59**	**1 to 3 Cell, High Power, Low-Noise, Step-Up DC-DC Converter with 1A MOSFET Power Switch**
MAX850	2	95	-4.1V/Adjustable, GaAsFET Bias Supply
MAX850EVKIT	2	—	Evaluation Kit for the MAX850–MAX853
MAX851	2	95	-4.1V/Adjustable, GaAsFET Bias Supply
MAX852	2	95	-4.1V/Adjustable, GaAsFET Bias Supply with Adjustable Oscillator
MAX853	2	95	Adjustable-Output GaAsFET Bias Supply with Adjustable Reference Level
MAX856	4	95	3.3V/5V, High-Efficiency, Low I_Q, DC-DC Step-Up Converter
MAX856EVKIT	4	—	Evaluation Kit for the MAX856–MAX859
MAX857	4	95	Adjustable-Output, High-Efficiency, Low I_Q, DC-DC Step-Up Converter
MAX858	4	95	3.3V/5V, High-Efficiency, Low I_Q, DC-DC Step-Up Converter
MAX859	4	95	Adjustable-Output, High-Efficiency, Low I_Q, DC-DC Step-Up Converter
MAX860	1	95	50mA, Frequency-Selectable, Switched-Capacitor Voltage Converter
MAX861	0	95	50mA, Frequency-Selectable, Switched-Capacitor Voltage Converter
MAX863	**†**	**4-75***	**Dual-Output, High-Efficiency, PFM, Step-Up DC-DC Controller**
MAX863EVKIT	†	—	Evaluation Kit for the MAX863
MAX864	**0**	**4-77**	**Dual-Output, Doubling/Inverting Charge-Pump Voltage Converter with Shutdown**
MAX865	**0**	**4-87**	**Dual-Output, Doubling/Inverting Charge-Pump Voltage Converter in µMAX**

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Alphanumeric Index

A Complete Product Listing

Part	Current DS Rev. No.	Data Book Year/97 Book Page No.	Description
MAX866	1	96	3.3V/5V-Output, Single-Cell DC-DC Converter for Pagers
MAX866EVKIT	0	—	Evaluation Kit for the MAX866/MAX867
MAX867	1	96	Adjustable-Output, Single-Cell DC-DC Converter for Pagers
MAX872	1	94	10µA, Low-Dropout, 2.5V Precision Voltage Reference
MAX873	1	94	Low-Power, Low-Drift, 2.5V Precision Voltage Reference
MAX874	1	94	10µA, Low-Dropout, 4.096V Precision Voltage Reference
MAX875	1	94	Low-Power, Low-Drift, 5V Precision Voltage Reference
MAX876	1	94	Low-Power, Low-Drift, 10V Precision Voltage Reference
MAX877	2	95	Replaced by MAX877L
MAX877L	2	—	5V-Output, 1.8V to 6V-Input, Step-Up/Step-Down DC-DC Converter
MAX877EVKIT	2	—	Evaluation Kit for the MAX877L/MAX878L/MAX879L
MAX878	2	95	Replaced by MAX878L
MAX878L	2	—	3.3V/3V-Output, 1.8V to 6V-Input, Step-Up/Step-Down DC-DC Converter
MAX879	2	95	Replaced by MAX879L
MAX879L	2	—	Adjustable-Output, 1.8V to 6V-Input, Step-Up/Step-Down DC-DC Converter
MAX882	0	96	3.3V or Adjustable, Low-Dropout, Low I_Q, 200mA Linear Regulator with Standby Mode
MAX883	0	96	5V or Adjustable, Low-Dropout, Low I_Q, 200mA Linear Regulator with Shutdown Mode
MAX884	0	96	3.3V or Adjustable, Low-Dropout, Low I_Q, 200mA Linear Regulator with Shutdown Mode
MAX887	**0**	**4-95**	**Low-Noise, Adjustable-Output, Step-Down DC-DC Converter with Synching Capability**
MAX887EVKIT	0	—	Evaluation Kit for the MAX887
MAX890L	**0**	**4-107**	**90mΩ, 1A, Current-Limited Power Switch**
MAX891L	†	**4-115***	**150mΩ, 0.5A, Current-Limited Power Switch**
MAX892L	†	**4-115***	**300mΩ, 0.25A, Current-Limited Power Switch**
MAX894L	**0**	**4-117**	**150mΩ, 0.5A, Dual Current-Limited Power Switch**
MAX895L	**0**	**4-117**	**300mΩ, 0.25A, Dual Current-Limited Power Switch**
MAX900	3	92	Quad, High-Speed, Low-Power, Single-Supply Voltage Comparator
MAX901	3	92	Quad, High-Speed, Low-Power, Single-Supply Voltage Comparator
MAX902	3	92	Dual, High-Speed, Low-Power, Single-Supply Voltage Comparator
MAX903	3	92	Single, High-Speed, Low-Power, Single-Supply Voltage Comparator
MAX905	0	93	High-Speed, Clocked, Master/Slave, ECL Voltage Comparator
MAX906	0	93	Dual, High-Speed, Clocked, Master/Slave, ECL Voltage Comparator
MAX907	3	94	Dual, High-Speed, Low-Power, Single 5V TTL Comparator
MAX908	3	94	Quad, High-Speed, Low-Power, Single 5V TTL Comparator
MAX909	3	94	Single, High-Speed, Low-Power, Single 5V TTL Comparator
MAX910	1	93	High-Speed, Threshold-Programmable Voltage Comparator
MAX911	1	93	High-Speed, Threshold-Programmable Voltage Comparator
MAX912	1	95	Dual, Ultra-Fast, Low-Power, Single-Supply, TTL Comparator

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Alphanumeric Index

A Complete Product Listing

Part	Current DS Rev. No.	Data Book Year/97 Book Page No.	Description
MAX913	1	95	Single, Ultra-Fast, Low-Power, Single-Supply, TTL Comparator
MAX915	0	—	Single, Ultra-High-Speed, Master/Slave TTL Comparator
MAX916	0	—	Dual, Ultra-High-Speed, Master/Slave TTL Comparator
MAX921	3	94	Single, Ultra-Low-Power, Single-Supply Comparator with 1% Precision Reference
MAX922	3	94	Dual, Ultra-Low-Power, Single-Supply Comparator
MAX923	3	94	Dual, Ultra-Low-Power, Single-Supply Comparator with 1% Precision Reference
MAX924	3	94	Quad, Ultra-Low-Power, Single-Supply Comparator with 1% Precision Ref.
MAX931	0	95	Single, Ultra-Low-Power, Low-Cost, Single-Supply Comparator with 2%-Accurate Reference
MAX932	0	95	Dual, Ultra-Low-Power, Low-Cost, Single-Supply Comparator with 2%-Accurate Reference
MAX933	0	95	Dual, Ultra-Low-Power, Low-Cost, Single-Supply Comparator with 2%-Accurate Reference
MAX934	0	95	Quad, Ultra-Low-Power, Low-Cost, Single-Supply Comparator with 2%-Accurate Reference
MAX941	2	95	Single, 3V and 5V, Single-Supply, 75ns, Rail-to-Rail Input Comparator
MAX942	2	95	Dual, 3V and 5V, Single-Supply, 75ns, Rail-to-Rail Input Comparator
MAX944	2	95	Quad, 3V and 5V, Single-Supply, 75ns, Rail-to-Rail Input Comparator
MAX951	**0**	**3-9**	**7µA, Single-Supply Op Amp + Comparator + Reference**
MAX952	**0**	**3-9**	**7µA, Single-Supply Op Amp + Comparator + Reference**
MAX953	**0**	**3-9**	**5µA, Single-Supply Op Amp + Comparator**
MAX954	**0**	**3-9**	**5µA, Single-Supply Op Amp + Comparator**
MAX961	**0**	**3-21**	**Single-Supply, Operation Down to 2.7V, 4.5ns Comparator**
MAX962	**0**	**3-21**	**Single-Supply, Operation Down to 2.7V, 4.5ns Comparator**
MAX971	**0**	**3-31**	**Single, Ultra-Low-Power, Open-Drain-Output Comparator with 1% Accurate Reference**
MAX972	**0**	**3-31**	**Dual, Ultra-Low-Power, Open-Drain-Output Comparator with 1% Accurate Reference**
MAX973	**0**	**3-31**	**Dual, Ultra-Low-Power, Open-Drain-Output Comparator with 1% Accurate Reference**
MAX974	**0**	**3-31**	**Quad, Ultra-Low-Power, Open-Drain-Output Comparator with 1% Accurate Reference**
MAX975	**0**	**3-45**	**+3V/+5V Dual-Speed Comparator with Auto-Standby**
MAX976	†	**3-61***	**Dual, +3V/+5V-Powered, High-Speed Comparator**
MAX977	**0**	**3-45**	**Dual, +3V/+5V Dual-Speed Comparator with Auto-Standby**
MAX978	†	**3-61***	**Quad, +3V/+5V-Powered, High-Speed Comparator**
MAX981	**0**	**3-31**	**Single, Ultra-Low-Power, Open-Drain-Output Comparator with 2% Accurate Reference**
MAX982	**0**	**3-31**	**Dual, Ultra-Low-Power, Open-Drain-Output Comparator with 2% Accurate Reference**

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Alphanumeric Index

A Complete Product Listing

Part	Current DS Rev. No.	Data Book Year/97 Book Page No.	Description
MAX983	**0**	**3-31**	**Dual, Ultra-Low-Power, Open-Drain-Output Comparator with 2% Accurate Reference**
MAX984	**0**	**3-31**	**Quad, Ultra-Low-Power, Open-Drain-Output Comparator with 2% Accurate Reference**
MAX1002	†	**7-113***	**Dual, 6-Bit, 60Msps ADC**
MAX1002EVKIT	†	—	Evaluation Kit for the MAX1002/MAX1003
MAX1003	†	**7-113***	**Dual, 6-Bit, 90Msps ADC**
MAX1044	1	93	10µA Charge-Pump Voltage Converter
MAX1110	†	**7-115***	**+2.7V, 8-Channel, 8-Bit ADC with Serial Interface**
MAX1110EVKIT	†	—	Evaluation Kit for the MAX1110/MAX1112
MAX1111	†	**7-115***	**+2.7V, 4-Channel, 8-Bit ADC with Serial Interface**
MAX1112	†	**7-117***	**+5V, 8-Channel, 8-Bit ADC with Serial Interface**
MAX1113	†	**7-117***	**+5V, 4-Channel, 8-Bit ADC with Serial Interface**
MAX1114	**0**	**7-119**	**8-Bit, 150Msps ADC**
MAX1114EVKIT	†	—	Evaluation Kit for the MAX1114/MAX1125
MAX1125	**0**	**7-131**	**8-Bit, 300Msps ADC**
MAX1150	**0**	**7-143**	**8-Bit, 500Msps ADC**
MAX1151	**0**	**7-151**	**8-Bit, 750Msps ADC**
MAX1150EVKIT	†	—	Evaluation Kit for the MAX1150/MAX1151
MAX1160	†	**7-159***	**10-Bit, 20Msps ADC**
MAX1160EVKIT	†	—	Evaluation Kit for the MAX1160/MAX1161
MAX1161	†	**7-161***	**10-Bit, 40Msps ADC**
MAX1170	**0**	**7-163**	**12-Bit, 10Msps ADC**
MAX1171	**0**	**7-175**	**12-Bit, 20Msps ADC**
MAX1172	**0**	**7-187**	**12-Bit, 30Msps ADC**
MAX1170EVKIT	†	—	Evaluation Kit for MAX1170/MAX1171/MAX1172
MAX1202	†	**7-199***	**Low-Power, 8-Channel, Serial 12-Bit ADC with Programmable Output Logic Level**
MAX1202EVKIT	†	—	Evaluation Kit for the MAX1202
MAX1204	†	**7-201***	**Low-Power, 8-Channel, Serial 10-Bit ADC with Programmable Output Logic Level**
MAX1232	1	92	µP Monitor
MAX1241	**0**	**7-203**	**2.7V, 1-Channel, Serial 12-Bit ADC**
MAX1241EVKIT	†	—	Evaluation Kit for the MAX1241
MAX1243	**0**	**7-215**	**2.7V, 1-Channel, Serial 10-Bit ADC**
MAX1245	**0**	**7-227**	**2.375V, 8-Channel, Serial 12-Bit ADC**
MAX1247	**0**	**7-247**	**2.7V, Low-Power, 4-Channel, Serial 12-Bit ADC**
MAX1247EVKIT	†	—	Evaluation Kit for the MAX1247
MAX1249	**0**	**7-267**	**2.7V, Low-Power, 4-Channel, Serial 10-Bit ADC**
MAX1259	1	92	Battery Manager
MAX1406	**0**	**2-47**	**±15kV ESD-Protected, EMC-Compliant, 230kbps, 3-Tx/3-Rx RS-232 IC**
MAX1480A/B	**1**	**2-55**	**Complete, Isolated RS-485/RS-422 Data Interface IC**

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Part	Current DS Rev. No.	Data Book Year/97 Book Page No.	Description
MAX1482	0	96	20µA, 1/8-Unit-Load, Slew-Rate-Limited, Full-Duplex RS-485 Transceiver
MAX1483	0	96	20µA, 1/8-Unit-Load, Slew-Rate-Limited, Half-Duplex RS-485 Transceiver
MAX1487	5	—	1/4-Unit Load, Half-Duplex RS-485/RS-422 Transceiver
MAX1487E	**3**	**2-31**	**2.5Mbps, ±15kV ESD-Protected, Low-Power, RS-485/RS-422 Transceiver**
MAX1488E	**0**	**2-75**	**±15kV ESD-Protected, Quad, Low-Power RS-232 Line Driver**
MAX1489E	**0**	**2-81**	**±15kV ESD-Protected, Quad, Low-Power RS-232 Line Receiver**
MAX1490A/B	**1**	**2-55**	**Complete, Isolated, Full-Duplex RS-485/RS-422 Data Interface IC**
MAX1600	**1**	**4-125**	**Dual-Channel CardBus and PCMCIA VCC/VPP Power-Switching Network**
MAX1601	**1**	**4-137**	**Dual-Channel CardBus and PCMCIA Power-Switch with SMBus Serial Interface**
MAX1602	**0**	**4-153**	**Single-Channel PCMCIA VCC/VPP Power-Switching Network**
MAX1603	**1**	**4-125**	**Dual-Channel CardBus and PCMCIA VCC/VPP Power-Switching Network**
MAX1604	**1**	**4-137**	**Dual-Channel CardBus and PCMCIA Power-Switch with SMBus Serial Interface**
MAX1610	**0**	**4-165**	**Digitally Controlled CCFL Backlight Power Supply**
MAX1611	**0**	**4-165**	**Digitally Controlled CCFL Backlight Power Supply with SMBus Interface**
MAX1611EVKIT	†	—	Evaluation Kit for the MAX1610/MAX1611
MAX1620	†	**4-185***	**Digitally Adjustable LCD Bias Supply**
MAX1621	†	**4-185***	**Digitally Adjustable LCD Bias Supply with SMBus Interface**
MAX1624	†	**4-187***	**High-Speed Step-Down Controller with Synchronous Rectification for CPU Power**
MAX1624EVKIT	†	—	Evaluation Kit for the MAX1624/MAX1625
MAX1625	†	**4-187***	**High-Speed Step-Down Controller with Synchronous Rectification for CPU Power**
MAX1626	**0**	**4-189**	**100% Duty Cycle, PFM, 5V or 3.3V, Pin-Selectable, Step-Down DC-DC Controller**
MAX1626EVKIT	0	—	Evaluation Kit for the MAX1626/MAX1627
MAX1627	**0**	**4-189**	**100% Duty Cycle, PFM, 1.3V to Input Adjustable, Step-Down DC-DC Controller**
MAX1630	**1**	**4-205**	**High-Efficiency, 3.3V/5V (or adj.), 12V-Output Controller for Notebooks**
MAX1630EVKIT	n/a	—	Evaluation Kit for the MAX1630/MAX1633
MAX1631	**1**	**4-205**	**High-Efficiency, 3.3V/5V (or adj.), 12V-Output Controller for Notebooks**
MAX1631EVKIT	n/a	—	Evaluation Kit for the MAX1631/MAX1634
MAX1632	**1**	**4-205**	**High-Efficiency, 3.3V/5V (or adj.), 12V-Output Controller for Notebooks**
MAX1632EVKIT	n/a	—	Evaluation Kit for the MAX1632/MAX1635

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Part	Current DS Rev. No.	Data Book Year/97 Book Page No.	Description
MAX1633	**1**	**4-205**	**High-Efficiency, 3.3V/5V (or adj.), 12V-Output Controller for Notebooks**
MAX1634	**1**	**4-205**	**High-Efficiency, 3.3V/5V (or adj.), 12V-Output Controller for Notebooks**
MAX1635	**1**	**4-205**	**High-Efficiency, 3.3V/5V (or adj.), 12V-Output Controller for Notebooks**
MAX1640	†	**4-233***	**PWM Current Source with High-Side Sense**
MAX1640EVKIT	†	—	Evaluation Kit for the MAX1640
MAX1641	†	**4-233***	**PWM Current Source with Low-Side Sense**
MAX1642	†	**4-235***	**1-Cell, High-Efficiency, Step-Up DC-DC Converter with Shutdown**
MAX1642EVKIT	†	—	Evaluation Kit for the MAX1642/MAX1643
MAX1643	†	**4-235***	**1-Cell, High-Efficiency, Step-Up DC-DC Converter with 2 LBI/LBOs**
MAX1647	†	**4-237***	**Chemistry-Independent Battery Charger with SMBus Serial Interface**
MAX1647EVKIT	†	—	Evaluation Kit for the MAX1647/MAX1648
MAX1648	†	**4-237***	**Chemistry-Independent Battery Charger**
MAX1649	2	96	5V or Adjustable, High-Efficiency, Low-Dropout, Step-Down DC-DC Controller
MAX1649EVKIT	†	—	Evaluation Kit for the MAX1649/MAX1651
MAX1651	2	96	3.3V or Adjustable, High-Efficiency, Low-Dropout, Step-Down DC-DC Controller
MAX1691	2	96	Integrated µP Supervisory Module with Lithium Backup Battery
MAX1732	—	94	12V, 120mA Flash Memory Programmer Module
MAX1738	—	94	See MAX738A
MAX1743	—	94	See MAX743
MAX1771	1	95	12V or Adjustable, High-Efficiency, Low IQ, Step-Up DC-DC Controller
MAX1771EVKIT	1	—	Evaluation Kit for the MAX1771
MAX2003	1	96	NiCd/NiMH Battery Fast-Charge Controller
MAX2003A	1	96	NiCd/NiMH Battery Fast-Charge Controller with Pulse Trickle
MAX2003AEVKIT	1	—	Evaluation Kit for the MAX2003/MAX2003A
MAX2100 Cells	0	96	Quadrature Digitizer Circuits
MAX2101	4	96	6-Bit Quadrature Digitizer
MAX2101EVKIT	1	—	Evaluation Kit for the MAX2101
MAX2402	1	96	800MHz to 1000MHz Spread-Spectrum Transmitter
MAX2402EVKIT	0	—	Evaluation Kit for the MAX2402
MAX2430	**0**	**11-5**	**900MHz, 100mW Power Amplifier/Predriver**
MAX2430EVKIT	†	—	Evaluation Kit for the MAX2430
MAX2450	**0**	**11-13**	**70MHz Quadrature Modulator/Demodulator**
MAX2450EVKIT	1	—	Evaluation Kit for the MAX2450/MAX2451/MAX2452
MAX2451	**0**	**11-21**	**70MHz Quadrature Demodulator**
MAX2452	**1**	**11-27**	**70MHz Quadrature Modulator**
MAX2601	†	**11-33***	**3V, 1W RF Power Transistor**
MAX2602	†	**11-33***	**3V, 1W RF Power Transistor with On-Chip Diode**

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Alphanumeric Index

A Complete Product Listing

Part	Current DS Rev. No.	Data Book Year/97 Book Page No.	Description
MAX2611	**0**	**11-35**	**DC-to-Microwave, Low-Noise Amplifier**
MAX2611PCB	†	—	Circuit Board to Evaluate MAX2611
MAX2620	**†**	**11-41***	**650MHz to 1050MHz Integrated Oscillator with Buffered Outputs**
MAX2630	**†**	**11-43***	**VHF-to-Microwave, 3V, Low-Noise Amplifier**
MAX2631	**†**	**11-43***	**VHF-to-Microwave, 3V, Low-Noise Amplifier with Shutdown**
MAX2632	**†**	**11-43***	**VHF-to-Microwave, 3V, Low-Noise Amplifier with Bias Control**
MAX2633	**†**	**11-43***	**VHF-to-Microwave, 3V, Low-Noise Amplifier with Shutdown and Bias Control**
MAX2633PCB	†	—	Circuit Board to Evaluate MAX2630–MAX2633
MAX2650	**0**	**11-45**	**5V, 1GHz, Low-Noise Amplifier**
MAX2650PCB	†	—	Circuit Board to Evaluate MAX2650
MAX3080	**0**	**2-87**	**Fail-Safe, 115kbps, Slew-Rate-Limited, Full-Duplex RS-485/RS-422 Transceiver**
MAX3081	**0**	**2-87**	**Fail-Safe, 115kbps, Slew-Rate-Limited, Full-Duplex RS-485/RS-422 Transceiver**
MAX3082	**0**	**2-87**	**Fail-Safe, 115kbps, Slew-Rate-Limited, Half-Duplex RS-485/RS-422 Transceiver**
MAX3083	**0**	**2-87**	**Fail-Safe, 500kbps, Slew-Rate-Limited, Full-Duplex RS-485/RS-422 Transceiver**
MAX3084	**0**	**2-87**	**Fail-Safe, 500kbps, Slew-Rate-Limited, Full-Duplex RS-485/RS-422 Transceiver**
MAX3085	**0**	**2-87**	**Fail-Safe, 500kbps, Slew-Rate-Limited, Half-Duplex RS-485/RS-422 Transceiver**
MAX3086	**0**	**2-87**	**Fail-Safe, 10Mbps, Full-Duplex RS-485/RS-422 Transceiver**
MAX3087	**0**	**2-87**	**Fail-Safe, 10Mbps, Full-Duplex RS-485/RS-422 Transceiver**
MAX3088	**0**	**2-87**	**Fail-Safe, 10Mbps, Half-Duplex RS-485/RS-422 Transceiver**
MAX3089	**0**	**2-87**	**Fail-Safe, 115kbps/500kbps/10Mbps, Half or Full-Duplex RS-485/RS-422 Transceiver**
MAX3185	**0**	**2-107**	**±15kV ESD-Protected, EMC-Compliant, 230kbps, RS-232 Serial Port for Motherboards/Desktop PCs**
MAX3186	**0**	**2-115**	**±15kV ESD-Protected, EMC-Compliant, 230kbps, RS-232 Serial Port for Modems**
MAX3212	0	96	1µA, 2.7V to 3.6V, 3-Driver/5-Receiver, True RS-232 Transceiver
MAX3218	0	96	1µA, 1.8V to 4.25V RS-232 Transceiver with AutoShutdown
MAX3221	**4**	**2-123**	**True 3V to 5.5V, RS-232 Transceiver with AutoShutdown Draws 1µA**
MAX3222	**4**	**2-137**	**300µA, 2-Driver/2-Receiver, True RS-232 Transceiver Using Four 0.1µF Capacitors**
MAX3223	**4**	**2-123**	**1µA, 3V to 5.5V, True RS-232 Transceiver with AutoShutdown**
MAX3232	**4**	**2-137**	**300µA, 2-Driver/2-Receiver, True RS-232 Transceiver Using Four 0.1µF Capacitors**
MAX3237	**4**	**2-137**	**500µA, 5-Driver/3-Receiver, True RS-232 Transceiver with 1Mbps Data Rate, Using Four 0.1µF Capacitors**

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Alphanumeric Index

A Complete Product Listing

Part	Current DS Rev. No.	Data Book Year/97 Book Page No.	Description
MAX3238	**0**	**2-153**	**Low-Power, 250kbps, True RS-232 Transceiver with AutoShutdown Plus**
MAX3241	**4**	**2-137**	**300µA, 3-Driver/5-Receiver, True RS-232 Transceiver Using Four 0.1µF Capacitors**
MAX3243	**4**	**2-123**	**1µA, 3V to 5.5V, True RS-232 Transceiver with AutoShutdown**
MAX3260	0	96	1GHz Transimpedance Preamplifier with 25dB Dynamic Range
MAX3261	2	96	Single 5V, Fully Integrated, 1.2Gbps Laser Diode Driver
MAX3262	1	96	1Gbps, High-Speed Limiting Amplifier with Chatter-Free Loss-of-Signal Detection
MAX3263	**0**	**12-3**	**Single 5V, Fully Integrated, 155Mbps Laser Diode Driver**
MAX3270	0	96	155Mbps/622Mbps Clock Recovery and Data Retiming IC with Fully Integrated Phase/Frequency Detector
MAX3480A/B	**0**	**2-165**	**Complete, Isolated, 3.3V RS-485/RS-422 Data Interface IC**
MAX3483	0	96	3.3V, Slew-Rate-Limited, True RS-485/RS-422 Transceiver
MAX3485	0	96	3.3V, 10Mbps, True RS-485/RS-422 Transceiver
MAX3486	0	96	3.3V, 2.5Mbps, True RS-485/RS-422 Transceiver
MAX3488	0	96	3.3V, Slew-Rate-Limited, True RS-485/RS-422 Transceiver
MAX3490	0	96	3.3V, 10Mbps, True RS-485/RS-422 Transceiver
MAX3491	0	96	3.3V, 10Mbps, True RS-485/RS-422 Transceiver
MAX3664	**0**	**12-11**	**622Mbps, Ultra-Low-Power, 3.3V Transimpedance Preamp for SDH/SONET**
MAX3681	**0**	**12-23**	**+3.3V, 622Mbps, SDH/SONET 1:4 Deserializer with LVDS Outputs**
MAX3761	**1**	**12-31**	**Low-Power, 622Mbps Limiting Amplifier with TTL Outputs and Chatter-Free Power Detector for LANs**
MAX3762	**1**	**12-31**	**Low-Power, 622Mbps Limiting Amplifier with PECL Outputs and Chatter-Free Power Detector for LANs**
MAX4005	0	96	950MHz FET-Input Buffer with 75Ω Output
MAX4051/A	**0**	**1-57**	**Low-Voltage, CMOS Analog Multiplexer**
MAX4052/A	**0**	**1-57**	**Low-Voltage, CMOS Analog Multiplexer**
MAX4053/A	**0**	**1-57**	**Low-Voltage, CMOS Analog Switch**
MAX4066/A	1	—	Low-Cost, Low-Voltage, Quad SPST, CMOS Analog Switch
MAX4100	**1**	**8-49**	**500MHz, High-Speed, Low-Power Op Amp**
MAX4100EVKIT	0	—	Evaluation Kit for the MAX4100/MAX4101
MAX4101	**1**	**8-49**	**200MHz, A_{VCL} = 2V/V, High-Speed, Low-Power Op Amp**
MAX4102	**0**	**8-61**	**250MHz, High-Speed, Low-Power, Video Op Amp**
MAX4103	**0**	**8-61**	**180MHz, A_{VCL} = 2V/V, High-Speed, Low-Power Op Amp**
MAX4103EVKIT	0	—	Evaluation Kit for the MAX4102/MAX4103
MAX4106	**1**	**8-73**	**350MHz, A_{VCL} = 5V/V, High-Speed, Ultra-Low-Noise Op Amp**
MAX4106EVKIT	0	—	Evaluation Kit for the MAX4106/MAX4107
MAX4107	**1**	**8-73**	**300MHz, A_{VCL} = 10V/V, High-Speed, Ultra-Low-Noise Op Amp**
MAX4108	**1**	**8-83**	**400MHz, High-Speed, Ultra-Low-Distortion Op Amp**
MAX4108EVKIT	0	—	Evaluation Kit for the MAX4108/MAX4109

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Alphanumeric Index

A Complete Product Listing

Part	Current DS Rev. No.	Data Book Year / 97 Book Page No.	Description
MAX4109	**1**	**8-83**	**225MHz, A_{VCL} = 2V/V, High-Speed, Ultra-Low-Distortion Op Amp**
MAX4111	0	96	330MHz Multiplexer/Crosspoint Building Block IC
MAX4112	**1**	**8-95**	**500MHz, High-Speed, Current-Mode Feedback Op Amp**
MAX4112EVKIT	0	—	Evaluation Kit for the MAX4112/MAX4113
MAX4113	**1**	**8-95**	**275MHz, A_{VCL} = 8V/V, High-Speed, Current-Mode Feedback Op Amp**
MAX4117	**1**	**8-95**	**500MHz, A_{VCL} = 2V/V, High-Speed, Current-Mode Feedback Op Amp**
MAX4117EVKIT	0	—	Evaluation Kit for the MAX4117/MAX4118
MAX4118	**1**	**8-95**	**275MHz, A_{VCL} = 8V/V, High-Speed, Current-Mode Feedback Op Amp**
MAX4119	†	**8-107***	**Quad, 500MHz, Low-Power, Current-Mode Feedback Amplifier**
MAX4120	†	**8-107***	**Quad, 275MHz, Low-Power, Current-Mode Feedback Amplifier**
MAX4121	0	96	330MHz Multiplexer/Crosspoint Building Block IC
MAX4121EVKIT	0	—	Evaluation Kit for the MAX4111/MAX4121
MAX4122	**0**	**3-63**	**Single, 5MHz, Single-Supply Op Amp**
MAX4123	**0**	**3-63**	**Single, 5MHz, Single-Supply Op Amp with Shutdown**
MAX4124	**0**	**3-63**	**Single, 10V/µs, Single-Supply Op Amp**
MAX4125	**0**	**3-63**	**Single, 10V/µs, Single-Supply Op Amp with Shutdown**
MAX4126	**0**	**3-63**	**Dual, 5MHz, Single-Supply Op Amp**
MAX4127	**0**	**3-63**	**Dual, 5MHz, Single-Supply Op Amp with Shutdown**
MAX4128	**0**	**3-63**	**Dual, 10V/µs, Single-Supply Op Amp**
MAX4129	**0**	**3-63**	**Quad, 5MHz, Single-Supply Op Amp**
MAX4130	**1**	**3-79**	**Single, 10MHz, Single-Supply Op Amp**
MAX4131	**1**	**3-79**	**Single, 10MHz, Single-Supply Op Amp with Shutdown**
MAX4132	**1**	**3-79**	**Dual, 10MHz, Single-Supply Op Amp**
MAX4133	**1**	**3-79**	**Dual, 10MHz, Single-Supply Op Amp with Shutdown**
MAX4134	**1**	**3-79**	**Quad, 10MHz, Single-Supply Op Amp**
MAX4135	**0**	**8-109**	**1-Input/6-Output Video Distribution Amplifier**
MAX4135EVKIT	0	—	Evaluation Kit for the MAX4135–MAX4138
MAX4136	**0**	**8-109**	**1-Input/6-Output Video Distribution Amplifier**
MAX4137	**0**	**8-121**	**1-Input/4-Output Video Distribution Amplifier**
MAX4138	**0**	**8-121**	**1-Input/4-Output Video Distribution Amplifier**
MAX4141	0	96	330MHz, 4x1, Multiplexer/Crosspoint Building Block IC
MAX4141EVKIT	0	—	Evaluation Kit for the MAX4141
MAX4144	**0**	**8-133**	**High-Speed Instrumentation Amplifier**
MAX4144EVKIT	†	—	Evaluation Kit for the MAX4144
MAX4146	**0**	**8-133**	**High-Speed Instrumentation Amplifier**
MAX4147	**0**	**8-145**	**350MHz, Low Power, High-Output-Current, Differential Line Driver**
MAX4147EVKIT	0	—	Evaluation Kit for the MAX4147
MAX4158	**0**	**8-153***	**330MHz, 2-Channel, High-Speed, Video Multiplexer/Amplifier**
MAX4159	**0**	**8-153***	**330MHz, 2-Channel, High-Speed, Video Multiplexer/Amplifier**
MAX4177	†	**8-155***	**380MHz, Unity-Gain, High-Speed Buffer**
MAX4178	**0**	**8-157**	**330MHz, Precision, Closed-Loop, Fixed Gain of +1 Buffer**
MAX4180	†	**8-167***	**Low-Power, 340MHz, Single Current-Mode Feedback Amplifier**

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†Future product. The data sheet is pending.

Alphanumeric Index

A Complete Product Listing

Part	Current DS Rev. No.	Data Book Year/97 Book Page No.	Description
MAX4181	†	**8-167***	**Low-Power, 400MHz, Single Current-Mode Feedback Amplifier**
MAX4182	†	**8-167***	**Low-Power, 340MHz, Dual Current-Mode Feedback Amplifier**
MAX4183	†	**8-167***	**Low-Power, 340MHz, Dual Current-Mode Feedback Amplifier**
MAX4184	†	**8-167***	**Low-Power, 400MHz, Dual Current-Mode Feedback Amplifier**
MAX4185	†	**8-167***	**Low-Power, 400MHz, Dual Current-Mode Feedback Amplifier**
MAX4186	†	**8-167***	**Low-Power, 340MHz, Quad Current-Mode Feedback Amplifier**
MAX4187	†	**8-167***	**Low-Power, 400MHz, Quad Current-Mode Feedback Amplifier**
MAX4193	0	92	CMOS, Micropower, Step-Up Switching Regulator
MAX4221	0	96	330MHz Multiplexer/Crosspoint Building Block IC
MAX4221EVKIT	0	—	Evaluation Kit for the MAX4221
MAX4258	**0**	**8-153***	**275MHz, A_{VCL} = 2V/V, 2-Channel, High-Speed, Video Multiplexer/Amplifier**
MAX4259	**0**	**8-153***	**275MHz, A_{VCL} = 2V/V, 2-Channel, High-Speed, Video Multiplexer/Amplifier**
MAX4277	†	**8-155***	**350MHz, Gain of +2, High-Speed Buffer**
MAX4278	**0**	**8-157**	**310MHz, Precision, Closed-Loop, Fixed Gain of +2 Buffer**
MAX4278EVKIT	0	—	Evaluation Kit for the MAX4187/MAX4278
MAX4308	†	**8-169***	**225MHz, Ultra-Low-Distrortion Op Amp**
MAX4309	†	**8-169***	**200MHz, Ultra-Low-Distortion Op Amp**
MAX4391	0	92	CMOS, Micropower, Inverting Switching Regulator
MAX4420	0	94	High-Speed, 6A MOSFET Driver (Noninverting)
MAX4426	0	—	Dual, High-Speed, 1.5A MOSFET Driver (Inverting)
MAX4427	0	—	Dual, High-Speed, 1.5A MOSFET Driver (Noninverting)
MAX4428	0	—	Dual, High-Speed, 1.5A MOSFET Driver (Inverting & Noninverting)
MAX4429	0	94	High-Speed, 6A MOSFET Driver (Inverting)
MAX4501	**0**	**1-75**	**Low-Voltage, SPST, Normally Open, CMOS Analog Switch**
MAX4502	**0**	**1-75**	**Low-Voltage, SPST, Normally Closed, CMOS Analog Switch**
MAX4503	**0**	**1-85**	**Low-Voltage, Dual-Supply, SPST, Normally Open, CMOS Analog Switch**
MAX4504	**0**	**1-85**	**Low-Voltage, Dual-Supply, SPST, Normally Closed, CMOS Analog Switch**
MAX4514	**0**	**1-95**	**Low-Voltage, Low-On-Resistance, SPST, Normally Open, CMOS Analog Switch**
MAX4515	**0**	**1-95**	**Low-Voltage, Low-On-Resistance, SPST, Normally Closed, CMOS Analog Switch**
MAX4516	**0**	**1-103**	**Dual-Supply, Low-On-Resistance, SPST, Normally Open, CMOS Analog Switch**
MAX4517	**0**	**1-103**	**Dual-Supply, Low-On-Resistance, SPST, Normally Closed, CMOS Analog Switch**
MAX4518	**0**	**1-111**	**Low-Voltage, Low-On-Resistance, CMOS Analog Multiplexer**
MAX4519	**0**	**1-111**	**Low-Voltage, Low-On-Resistance, CMOS Analog Multiplexer**
MAX4521	**0**	**1-123**	**Quad, Low-Voltage, SPST, Normally Closed CMOS Analog Switch**

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Alphanumeric Index

A Complete Product Listing

Part	Current DS Rev. No.	Data Book Year/97 Book Page No.	Description
MAX4522	0	1-123	Quad, Low-Voltage, SPST, Normally Open CMOS Analog Switch
MAX4523	0	1-123	Quad, Low-Voltage, SPST, Normally Open and Normally Closed CMOS Analog Switch
MAX4526	†	1-135*	High-Speed Phase-Reversal Analog Switch
MAX4527	†	1-135*	Low-Power Phase-Reversal Analog Switch
MAX4530	†	1-137*	8-Channel, Low-Voltage, CMOS Analog Multiplexer
MAX4531	†	1-137*	Dual, 4-Channel, Low-Voltage, CMOS Analog Multiplexer
MAX4532	†	1-137*	Triple, SPDT, Low-Voltage, CMOS Analog Switch
MAX4536	0	1-139*	Quad, Low-Voltage, Normally Open, SPST Analog Switch with Enable
MAX4537	0	1-139*	Quad, Low-Voltage, Normally Closed, SPST Analog Switch with Enable
MAX4538	0	1-139*	Quad, Low-Voltage, Normally Open and Normally Closed, SPST Analog Switch with Enable
MAX5018	†	9-125*	165/275Msps Video DAC with Controls
MAX5140	†	9-127*	400Msps High-Resolution Video DAC
MAX5250	†	9-129*	+5V, Quad, 10-Bit Voltage-Output DAC with Serial Interface
MAX5251	†	9-131*	+3V, Quad, 10-Bit Voltage-Output DAC with Serial Interface
MAX5253	0	9-133	+3V, Quad, 12-Bit Voltage-Output DAC with Serial Interface
MAX5351	†	9-149*	+3.3V, Low-Power, 13-Bit Voltage-Output DAC with Serial Interface
MAX5352	†	9-151*	+5V, 12-Bit Voltage-Output DAC with Serial Interface
MAX5353	†	9-151*	+3.3V, 12-Bit Voltage-Output DAC with Serial Interface
MAX5354	†	9-153*	+5V, 10-Bit Voltage-Output DAC with Serial Interface
MAX5355	†	9-153*	+3.3V, 10-Bit Voltage-Output DAC with Serial Interface
MAX6120	1	6-5	Low-Cost, Micropower, Precision 3-Terminal, 1.2V Voltage Reference
MAX6125	†	6-11*	2.5V-Output, Low-Dropout, Micropower, Precision 3-Terminal Voltage Reference
MAX6141	†	6-11*	4.096V-Output, Low-Dropout, Micropower, Precision 3-Terminal Voltage Reference
MAX6145	†	6-11*	4.5V-Output, Low-Dropout, Micropower, Precision 3-Terminal Voltage Reference
MAX6150	†	6-11*	5V-Output, Low-Dropout, Micropower, Precision 3-Terminal Voltage Reference
MAX6160	†	6-11*	Adjustable-Output, Low-Dropout, Micropower, Precision 3-Terminal Voltage Reference
MAX6225	0	6-13	Low-Drift, Low-Noise, 2.5V Precision Voltage Reference
MAX6241	0	6-13	Low-Drift, Low-Noise, 4.096V Precision Voltage Reference
MAX6250	0	6-13	Low-Drift, Low-Noise, 5.0V Precision Voltage Reference
MAX6301	0	5-49	5V, Low-Power µP Supervisory Circuit with Active-Low, Adjustable Reset
MAX6302	0	5-49	5V, Low-Power µP Supervisory Circuit with Active-High, Adjustable Reset
MAX6303	0	5-49	5V, Low-Power µP Supervisory Circuit with Push/Pull Reset Output

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†Future product. The data sheet is pending.

Alphanumeric Index

A Complete Product Listing

Part	Current DS Rev. No.	Data Book Year/97 Book Page No.	Description
MAX6304	**0**	**5-49**	**5V, Low-Power µP Supervisory Circuit with Active-High, Push/Pull Reset Output**
MAX6305	**0**	**5-61**	**5-Pin, Multiple-Input, Programmable Reset IC**
MAX6306	**0**	**5-61**	**5-Pin, Multiple-Input, Programmable Reset IC**
MAX6307	**0**	**5-61**	**5-Pin, Multiple-Input, Programmable Reset IC**
MAX6308	**0**	**5-61**	**5-Pin, Multiple-Input, Programmable Reset IC**
MAX6309	**0**	**5-61**	**5-Pin, Multiple-Input, Programmable Reset IC**
MAX6310	**0**	**5-61**	**5-Pin, Multiple-Input, Programmable Reset IC**
MAX6311	**0**	**5-61**	**5-Pin, Multiple-Input, Programmable Reset IC**
MAX6312	**0**	**5-61**	**5-Pin, Multiple-Input, Programmable Reset IC**
MAX6313	**0**	**5-61**	**5-Pin, Multiple-Input, Programmable Reset IC**
MAX6314	**0**	**5-75**	**68HC11/Bidirectional-Compatible µP Reset Circuit**
MAX6315	**0**	**5-85**	**Open-Drain SOT µP Reset Circuit**
MAX6520	**0**	**6-23**	**Low-Cost, Micropower, Precision 3-Terminal, 1.2V Voltage Reference**
MAX7219	1	—	Serially Interfaced, 8-Digit, LED Display Driver
MAX7231	0	—	8-Digit, Triplexed LCD Decoder/Driver
MAX7232	0	—	10-Digit, Triplexed LCD Decoder/Driver
MAX7233	0	—	4-Character, Triplexed LCD Decoder/Driver
MAX7234	0	—	5-Character, Triplexed LCD Decoder/Driver
MAX7624	1	—	Improved MX7524
MAX7645	1	—	Improved MX7545
MAX7705	0	—	µP Power-Supply Monitor with Reset
MAX8211	3	—	µP Voltage Monitor with Programmable Voltage Detection
MAX8212	3	—	µP Voltage Monitor with Programmable Voltage Detection
MAX8213	1	—	Five Universal Voltage Monitors, Complete µP Voltage Monitoring
MAX8214	1	—	Five Universal Voltage Monitors with Active Pull-Ups
MAX8215	0	—	±5V, ±12V Dedicated µP Voltage Monitor
MAX8216	0	—	±5V, ±12V Dedicated µP Voltage Monitor
MAX8862	**0**	**4-239**	**Low-Cost, Low-Dropout, Dual Linear Regulator**
MAX8863	**1**	**4-251**	**Low-Noise 50mA LDO Linear Regulator in SOT23**
MAX8864	**1**	**4-251**	**Low-Noise 50mA LDO Linear Regulator in SOT23 with C_{OUT} Discharge**
MAX8865	**0**	**4-261**	**Dual, Low-Dropout, 100mA Linear Regulator**
MAX8866	**0**	**4-261**	**Dual, Low-Dropout, 100mA Linear Regulator with Auto-Discharge**
MAX9685	1	—	Ultra-Fast ECL-Output Comparator with Latch Enable
MAX9686	0	—	Single, Very-Fast TTL-Latched Output Comparator
MAX9687	1	—	Dual, Ultra-Fast ECL-Output Comparator
MAX9690	2	—	Ultra-Fast ECL-Output Comparator
MAX9698	0	—	Dual, Very-Fast, TTL-Latched Output Comparator
MAXC001	0	—	150µF, Low-ESR Aluminum Electrolytic Capacitor
MAXL001	0	92	100µH Toroid Inductor
MF10	1	—	Dual, Second-Order, Universal Switched-Capacitor Filter

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Alphanumeric Index

A Complete Product Listing

Part	Current DS Rev. No.	Data Book Year/97 Book Page No.	Description
MX390	0	—	Quad, CMOS 12-Bit DAC
MX536A	2	—	True RMS-to-DC Converter
MX565A	0	—	High-Speed, 12-Bit, Monolithic DAC with Voltage Reference
MX566A	0	—	High-Speed, 12-Bit, Monolithic DAC
MX574A	2	—	Industry-Standard, Complete 12-Bit ADC
MX578	0	—	High-Speed, 3µs, 12-Bit ADC
MX580	0	—	Precision 2.5V Voltage Reference
MX581	0	—	Precision 10V Voltage Reference
MX584	0	—	Pin-Programmable 10V, 7.5V, 5V, 2.5V, Precision Voltage Reference
MX636	2	—	True RMS-to-DC Converter
MX674A	2	—	Industry-Standard, Complete, 12-Bit ADC
MX2700	0	—	Precision, 3ppm/°C, 10V Reference
MX2701	0	—	Precision, 3ppm/°C, -10V Reference
MX2702	0	—	Precision, 1ppm/°C, 10V Reference
MX7224	1	—	CMOS, Double-Buffered, 8-Bit Voltage-Output DAC
MX7225	1	—	CMOS, Quad, 8-Bit DAC with Voltage Outputs
MX7226	1	—	CMOS, Quad, 8-Bit DAC with Voltage Outputs
MX7228	0	—	CMOS, Octal, 8-Bit DAC
MX7245	0	—	Complete, 12-Bit, Voltage-Output Multiplying DAC
MX7248	0	—	Complete, 12-Bit, Voltage-Output Multiplying DAC
MX7501	0	—	8-Channel, Low-Power, Monolithic, CMOS Multiplexer
MX7502	0	—	Differential, 4-Channel, Low-Power, Monolithic, CMOS Multiplexer
MX7503	0	—	8-Channel, Low-Power, Monolithic, CMOS Multiplexer
MX7506	0	—	Monolithic CMOS Multiplexer
MX7507	0	—	Monolithic CMOS Multiplexer
MX7520	1	—	CMOS, 10-Bit Multiplying DAC
MX7521	1	—	CMOS, 12-Bit Multiplying DAC
MX7523	0	—	CMOS, 8-Bit Multiplying DAC
MX7524	1	—	CMOS, Buffered, 8-Bit Multiplying DAC
MX7528	3	—	CMOS, Dual, Buffered, 8-Bit Multiplying DAC
MX7530	1	—	CMOS, 10-Bit Multiplying DAC
MX7531	1	—	CMOS, 12-Bit Multiplying DAC
MX7533	1	—	CMOS, Low-Cost, 10-Bit Multiplying DAC
MX7534	0	—	µP-Compatible, 14-Bit DAC
MX7535	0	—	µP-Compatible, 14-Bit DAC
MX7536	0	—	µP-Compatible, 14-Bit DAC
MX7537	1	—	CMOS, Parallel-Loading, Dual, 12-Bit Multiplying DAC
MX7538	1	—	CMOS, µP-Compatible, 14-Bit DAC
MX7541	1	—	CMOS, 12-Bit Multiplying DAC
MX7541A	2	—	CMOS, 12-Bit Multiplying DAC
MX7542	1	—	CMOS, 12-Bit, µP-Compatible DAC
MX7543	2	—	CMOS, 12-Bit, Serial-Input DAC

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Alphanumeric Index

A Complete Product Listing

Part	Current DS Rev. No.	Data Book Year/97 Book Page No.	Description
MX7545	1	—	CMOS, Buffered, 12-Bit Multiplying DAC
MX7545A	1	—	CMOS, Buffered, 12-Bit Multiplying DAC
MX7547	1	—	CMOS, Parallel-Loading, Dual, 12-Bit Multiplying DAC
MX7548	0	—	CMOS, 8-Bit-Compatible, 12-Bit DAC
MX7549	1	—	CMOS, Dual, Double-Buffered, 12-Bit, µP-Compatible DAC
MX7572	0	92	CMOS, Complete, High-Speed, 12-Bit ADC
MX7574	0	—	CMOS, µP-Compatible, 8-Bit ADC
MX7575	1	—	CMOS, µP-Compatible, 5µs, 8-Bit ADC
MX7576	1	—	CMOS, µP-Compatible, 10µs, 8-Bit ADC
MX7578	0	—	Calibrated, 12-Bit ADC
MX7581	1	—	CMOS, 8-Bit, 8-Channel Data-Acquisition System
MX7582	1	—	Calibrated, 4-Channel, 12-Bit ADC
MX7628	3	—	CMOS, Dual, Buffered, 8-Bit, Multiplying DAC
MX7672	0	—	High-Speed 12-Bit ADC with External Reference Input
MX7820	1	—	CMOS, 1.3µs, 8-Bit ADC with Track/Hold
MX7821	1	92	µP-Compatible, 660ns, 8-Bit ADC with Track/Hold
MX7824	2	—	CMOS, High-Speed, 8-Bit ADC with 4-Channel Multiplexer
MX7828	2	—	CMOS, High-Speed, 8-Bit ADC with 8-Channel Multiplexer
MX7837	0	—	Complete, Dual, 12-Bit Multiplying DAC with 8-Bit Bus Interface
MX7845	0	—	Complete, 12-Bit Multiplying DAC
MX7847	0	—	Complete, Dual, 12-Bit Multiplying DAC with 12-Bit Bus Interface
MXD1000	†	94*	5-Tap Silicon Delay Line
MXD1013	†	94*	3-in-1 Silicon Delay Line
MXD1210	1	—	Nonvolatile RAM Controller
MXL1001	1	—	Low-Offset, Precision Op Amp
MXL1007	1	—	Low-Noise, Precision Op Amp
MXL1013	2	—	Dual, Precision Op Amp
MXL1014	2	—	Quad, Precision Op Amp
MXL1016	2	—	Ultra-Fast, Precision TTL Comparator
MXL1062	3	—	5th-Order, Zero-Error, Butterworth, Switched-Capacitor Lowpass Filter
MXL1074	3	—	5A, Step-Down, PWM, Switch-Mode DC-DC Regulator
MXL1076	3	—	2A, Step-Down, PWM, Switch-Mode DC-DC Regulator
MXL1116	2	—	Ultra-Fast, Single-Supply, Precision TTL Comparator
MXL1178	1	—	Dual, Single-Supply, Micropower, Precision Op Amp
MXL1179	1	—	Quad, Single-Supply, Micropower, Precision Op Amp
MXT429	0	—	High-Speed, 6A MOSFET Driver (Inverting)
OP07	1	—	Precision Op Amp
OP27	0	—	Low-Noise, Precision Op Amp
OP37	0	—	Low-Noise, Precision Op Amp
OP90	0	—	Precision, Low-Voltage, Micropower Op Amp
REF01	0	—	Precision, 10V Voltage Reference
REF02	0	—	Precision, 5V Voltage Reference

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†Future product. The data sheet is pending.

Part	Current DS Rev. No.	Data Book Year/97 Book Page No.	Description
Si7661	1	—	CMOS, Switched-Capacitor Voltage Converter (Up to 20V Input)
TSC426	1	—	Dual-Power MOSFET Driver (Inverting)
TSC427	1	—	Dual-Power MOSFET Driver (Noninverting)
TSC428	1	—	Dual-Power MOSFET Driver (Inverting and Noninverting)

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MAXIM

Analog Multiplexers/Switches

Analog Multiplexers/Switches, Product Tables and Trees 1-2

MAX312	Low-On-Resistance, Quad SPST, Normally Closed, CMOS Analog Switch	1-9
MAX313	Low-On-Resistance, Quad SPST, Normally Open, CMOS Analog Switch	1-9
MAX314	Low-On-Resistance, Quad SPST, 2 Normally Open/2 Normally Closed, CMOS Analog Switch	1-9
MAX336	16-Channel, Low-Leakage, CMOS Analog Multiplexer	1-19*
MAX337	Dual 8-Channel, Low-Leakage, CMOS Analog Multiplexer	1-19*
MAX349	Low-Voltage, Serial-Controlled Multiplexer	1-21
MAX350	Low-Voltage, Serial-Controlled Multiplexer	1-21
MAX395	Low-Voltage, Serially Controlled, Octal SPST Analog Switch	1-41
MAX4051/A	Low-Voltage, CMOS Analog Multiplexer	1-57
MAX4052/A	Low-Voltage, CMOS Analog Multiplexer	1-57
MAX4053/A	Low-Voltage, CMOS Analog Switch	1-57
MAX4501	Low-Voltage, SPST, Normally Open, CMOS Analog Switch	1-75
MAX4502	Low-Voltage, SPST, Normally Closed, CMOS Analog Switch	1-75
MAX4503	Low-Voltage, Dual-Supply, SPST, Normally Open, CMOS Analog Switch	1-85
MAX4504	Low-Voltage, Dual-Supply, SPST, Normally Closed, CMOS Analog Switch	1-85
MAX4514	Low-Voltage, Low-On-Resistance, SPST, Normally Open, CMOS Analog Switch	1-95
MAX4515	Low-Voltage, Low-On-Resistance, SPST, Normally Closed, CMOS Analog Switch	1-95
MAX4516	Dual-Supply, Low-On-Resistance, SPST, Normally Open, CMOS Analog Switch	1-103
MAX4517	Dual-Supply, Low-On-Resistance, SPST, Normally Closed, CMOS Analog Switch	1-103
MAX4518	Low-Voltage, Low-On-Resistance, CMOS Analog Multiplexer	1-111
MAX4519	Low-Voltage, Low-On-Resistance, CMOS Analog Multiplexer	1-111
MAX4521	Quad, Low-Voltage, SPST, Normally Closed CMOS Analog Switch	1-123
MAX4522	Quad, Low-Voltage, SPST, Normally Open CMOS Analog Switch	1-123
MAX4523	Quad, Low-Voltage, SPST, Normally Open and Normally Closed CMOS Analog Switch	1-123
MAX4526	High-Speed Phase-Reversal Analog Switch	1-135*
MAX4527	Low-Power Phase-Reversal Analog Switch	1-135*
MAX4530	8-Channel, Low-Voltage, CMOS Analog Multiplexer	1-137*
MAX4531	Dual, 4-Channel, Low-Voltage, CMOS Analog Multiplexer	1-137*
MAX4532	Triple, SPDT, Low-Voltage, CMOS Analog Switch	1-137*
MAX4536	Quad, Low-Voltage, Normally Open, SPST Analog Switch with Enable	1-139*
MAX4537	Quad, Low-Voltage, Normally Closed, SPST Analog Switch with Enable	1-139*
MAX4538	Quad, Low-Voltage, Normally Open and Normally Closed, SPST Analog Switch with Enable	1-139*

*Advance Information–first page of data sheet in preparation.

Analog Switches

SPST

10Ω
MAX312 (quad)
MAX313 (quad)
MAX314 (quad)

20Ω or 25Ω
IH5048A (dual)
★ MAX4514‡ (single)
★ MAX4515‡ (single)
★ MAX4516‡ (single)
★ MAX4517‡ (single)

30Ω or 35Ω
MAX320‡ (dual)
MAX321‡ (dual)
MAX322‡ (dual)
MAX323‡ (dual)
MAX324‡ (dual)
MAX325‡ (dual)
MAX351 (quad)
MAX352 (quad)
MAX353 (quad)
MAX381‡ (dual)
MAX391‡ (quad)
MAX392‡ (quad)
MAX393‡ (quad)
MAX4066‡ (quad)
MAX4066A‡ (quad)
DG411 (quad)
DG412 (quad)
DG413 (quad)

45Ω
MAX301 (dual)
MAX317 (single)
MAX318 (single)
DG401 (dual)
DG417 (single)
DG418 (single)
DG421 (dual, latch)
IH5048 (dual)

50Ω or 55Ω
MAX334 (quad)
DG300A (dual)
DG304A (dual)
DG381A (dual)
HI-201HS (quad)

70Ω or 75Ω
DG200A (dual)
IH5140 (single)
IH5141 (dual)

80Ω or 85Ω
MAX361 (quad)
MAX362 (quad)
MAX364 (quad)
MAX365 (quad)
DG441 (quad)
DG442 (quad)
DG444 (quad)
DG445 (quad)
HI-201 (quad)
IH5040 (single)
IH5041 (dual)

100Ω or 110Ω
★ MAX4521 (quad) ‡
★ MAX4522 (quad) ‡
★ MAX4523 (quad) ‡
★ MAX4536 (quad) ‡
★ MAX4537 (quad) ‡
★ MAX4538 (quad) ‡
DG308A (quad)
DG309 (quad)

175Ω or 200Ω
MAX331 (quad)
MAX332 (quad)
DG201A (quad)
DG202 (quad)
DG211 (quad)
DG212 (quad)

250Ω
★ MAX4501‡ (single)
★ MAX4502‡ (single)
★ MAX4503‡ (single)
★ MAX4504‡ (single)

SPDT

35Ω
MAX333A (quad)
MAX383‡ (dual)
MAX394‡ (quad)

45Ω
MAX303 (dual)
MAX319 (single)
DG403 (dual)
DG419 (single)
DG423 (dual, latch)
IH5050 (single)
IH5051 (dual)

50Ω
DG301A (single)
DG303A (dual)
DG305A (single)
DG307A (dual)
DG387A (single)
DG390A (dual)

75Ω
IH5142 (single)
IH5143 (dual)

80Ω
IH5042 (single)
IH5043 (dual)

175Ω
MAX333 (quad)

DPST

35Ω
MAX385‡ (dual)

45Ω
MAX305 (dual)
DG405 (dual)
DG425 (dual, latch)
IH5049 (dual)

50Ω
DG302A (dual)
DG306A (dual)
DG384A (dual)

75Ω
IH5144 (single)
IH5145 (dual)

80Ω
IH5044 (single)
IH5045 (dual)

8 x SPST*
MAX335 (octal)
MAX395‡ (octal)

4PST

75Ω
IH5047 (single)

Video

Dual SPST
IH5341 (dual)

Quad SPST
IH5352 (quad)

Low Leakage

SPST
MAX326 (quad)
MAX327 (quad)

Signal-Line Circuit Protectors

3-Line
MAX366

8-Line
MAX367

Phase-Reversal Switches
† MAX4526
† MAX4527

★ New product
† Future product
‡ Guaranteed operation at 3V
* Serial interface

Part Number	Function[1]	$R_{DS(ON)}$[2] (Ω max)	$I_{COM(OFF)}$ $I_{D(OFF)}$ (nA max)	R_{ON} Match (Ω max)	R_{ON} Flatness (Ω max)	$t_{(ON)}$ (ns max)	$t_{(OFF)}$ (ns max)	Pins-Package Options	Supply Voltage Range (V)	Features	Price† 1000-up ($)
SPST											
MAX4514	SPST NO	20	1	–	–	150	100	8-SO, 5-SOT23	+2 to +12	Low on-resistance, smallest package	0.47
MAX4515	SPST NC	20	1	–	–	150	100	8-SO, 5-SOT23	+2 to +12	Low on-resistance, smallest package	0.47
MAX4516	SPST NO	20	1	–	–	100	75	8-SO, 5-SOT23	±1 to ±6	Low on-resistance, smallest package	0.47
MAX4517	SPST NC	20	1	–	–	100	75	8-SO, 5-SOT23	±1 to ±6	Low on-resistance, smallest package	0.47
MAX317	SPST NC	45	0.25	–	3	175	145	8-SO/DIP	±4.5 to ±20	Improved DG417, low R_{ON} match and flatness	0.96
MAX318	SPST NO	45	0.25	–	3	175	145	8-SO/DIP	±4.5 to ±20	Improved DG418, low R_{ON} match and flatness	0.96
DG417	SPST NC	45	0.25	–	4	175	145	8-SO/DIP	±4.5 to ±20		0.96
DG418	SPST NO	45	0.25	–	4	175	145	8-SO/DIP	±4.5 to ±20		0.96
IH5140	SPST NO	75	1			150	125	16-SO/DIP	±4.5 to ±20		2.89
IH5040	SPST NO	80	5			400	200	16-SO/DIP	±4.5 to ±20		2.06
MAX4501	SPST NO	250	1	–	–	75	50	8-SO, 5-SOT23	+2 to +12	Low voltage, smallest package	0.42
MAX4502	SPST NC	250	1	–	–	75	50	8-SO, 5-SOT23	+2 to +12	Low voltage, smallest package	0.42
MAX4503	SPST NO	250	1	–	–	150	100	8-SO, 5-SOT23	±1 to ±6	Low voltage, smallest package	0.42
MAX4504	SPST NC	250	1	–	–	150	100	8-SO, 5-SOT23	±1 to ±6	Low voltage, smallest package	0.42
IH5048A	2 SPST NO	25	5			1000	500	16-SO/DIP	±4.5 to ±20	Low power, low R_{ON}	4.49
MAX320	2 SPST NO	35	0.1	2	4	150	100	8-DIP/SO/µMAX	±2.7 to ±8	Low voltage, low on-resistance	0.89
MAX321	2 SPST NC	35	0.1	2	4	150	100	8-DIP/SO/µMAX	±2.7 to ±8	Low voltage, low on-resistance	0.89
MAX322	2 SPST NO, NC	35	0.1	2	4	150	100	8-DIP/SO/µMAX	±2.7 to ±8	Low voltage, low on-resistance	0.89
MAX381	2 SPST NO	35	0.1	2	4	175	100	16-DIP/SO	±2.7 to ±8	Single supply, +2.7V to +16V	1.23
MAX301	2 SPST NO	45	0.25	2	3	150	100	16-DIP/SO	±4.5 to ±20	Improved DG401, low R_{ON} match and flatness	1.23
DG401	2 SPST NO	45	0.5	2	3	150	100	16-DIP/SO	±4.5 to ±20	Low power, high speed, low leakage	1.23
DG421	2 SPST NO	45	0.25	3	4	250	200	16-DIP/SO	±4.5 to ±20	Low power, high speed, has latches	1.59
IH5048	2 SPST NO	45	5			1000	500	16-DIP/SO	±4.5 to ±20	Low power, low R_{ON}	4.49
DG300A	2 SPST NC	50	1			300	250	14-DIP	±4.5 to ±20	2.4V_{IH}, low R_{ON}	1.94
DG304A	2 SPST NC	50	1			250	150	14-DIP	±4.5 to ±20	CMOS logic levels, high speed, low R_{ON}	2.18
DG381A	2 SPST NO	50	1			300	250	14-DIP	±4.5 to ±20	Low R_{ON}	2.08
MAX323	2 SPST NO	60	0.1	2	6	150	100	8-DIP/SO/µMAX	+2.7 to +16	Single supply, +2.7V/+5V	0.89
MAX324	2 SPST NC	60	0.1	2	6	150	100	8-DIP/SO/µMAX	+2.7 to +16	Single supply, +2.7V/+5V	0.89
MAX325	2 SPST NO, NC	60	0.1	2	6	150	100	8-DIP/SO/µMAX	+2.7 to +16	Single supply, +2.7V/+5V	0.89
DG200A	2 SPST NC	70	2			1000	500	14-DIP/SO	±4.5 to ±20		0.93
IH5141	2 SPST NO	75	1			150	125	16-DIP/SO	±4.5 to ±20		3.23
IH5041	2 SPST NC	80	1			400	200	16-DIP/SO	±4.5 to ±20		1.84
MAX312	4 SPST NC	10	0.25	2	4	175	145	16-DIP/SO	±4.5 to ±20	Low on-resistance	2.49
MAX313	4 SPST NO	10	0.25	2	4	175	145	16-DIP/SO	±4.5 to ±20	Low on-resistance	2.49
MAX314	4 SPST NO, NC	10	0.25	2	4	175	145	16-DIP/SO	±4.5 to ±20	Low on-resistance	2.49
MAX351	4 SPST NC	35	0.25	2	3	175	145	16-DIP/SO	±4.5 to ±20	Improved DG411, low R_{ON} match and flatness	1.76
MAX352	4 SPST NO	35	0.25	2	3	175	145	16-DIP/SO	±4.5 to ±20	Improved DG412, low R_{ON} match and flatness	1.76
MAX353	4 SPST NO, NC	35	0.25	2	3	175	145	16-DIP/SO	±4.5 to ±20	Improved DG413, low R_{ON} match and flatness	1.76
MAX391	4 SPST NC	35	0.1	2	4	130	75	16-DIP/SO	±2.7 to ±8	Single supply, +3V/+5V/+12V	1.87
MAX392	4 SPST NO	35	0.1	2	4	130	75	16-DIP/SO	±2.7 to ±8	Single supply, +3V/+5V/+12V	1.87
MAX393	4 SPST NO, NC	35	0.1	2	4	130	75	16-DIP/SO	±2.7 to ±8	Single supply, +3V/+5V/+12V	1.87
MAX4066A	4 SPST NO	35	0.1	2	4	130	75	14-DIP/SO	+2.7 to +16	Low leakage	1.87
DG411	4 SPST NC	35	0.25	2	4	175	145	16-DIP/SO	±4.5 to ±20	Low power, high speed, low leakage	1.85
DG412	4 SPST NO	35	0.25	2	4	175	145	16-DIP/SO	±4.5 to ±20	Low power, high speed, low leakage	1.85
DG413	4 SPST NO, NC	35	0.25	3	4	175	145	16-DIP/SO	±4.5 to ±20	Low power, high speed, low leakage	1.85
MAX4066	4 SPST	45	1	4	6	130	75	14-DIP/SO, 16-QSOP	+2.7 to +16	Low voltage, 74HC4066 upgrade	0.99
MAX334	4 SPST NC	50	1			100	50	16-DIP/SO	±4.5 to ±20	High speed, low on-resistance	2.88
HI-201HS	4 SPST NC	50	1			50	50	16-DIP/SO	±4.5 to ±20	Low R_{ON}, high speed	2.64
HI-201	4 SPST NC	80	5			400	300	16-DIP/SO	±4.5 to ±20	Low R_{ON}	2.00

[1] NO = Normally Open, NC = Normally Closed

[2] Drain-source on-resistance is for the commercial grade, T_A = +25°C.

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Part Number	Function[1]	$R_{DS(ON)}$[2] (Ω max)	$I_{COM(OFF)}$/ $I_{D(OFF)}$ (nA max)	R_{ON} Match (Ω max)	R_{ON} Flatness (Ω max)	$t_{(ON)}$ (ns max)	$t_{(OFF)}$ (ns max)	Pins-Package Options	Supply Voltage Range (V)	Features	Price† 1000-up ($)
MAX361	4 SPST NC	85	0.5	2	5	250	120	16-DIP/SO	±4.5 to ±20	Improved DG441, low R_{ON} match and flatness	1.29
MAX362	4 SPST NO	85	0.5	2	5	250	120	16-DIP/SO	±4.5 to ±20	Improved DG442, low R_{ON} match and flatness	1.29
MAX364	4 SPST NC	85	0.5	2	5	250	120	16-DIP/SO	±4.5 to ±20	Improved DG444, low R_{ON} match and flatness	1.03
MAX365	4 SPST NO	85	0.5	2	5	250	120	16-DIP/SO	±4.5 to ±20	Improved DG445, low R_{ON} match and flatness	1.03
DG441	4 SPST NC	85	0.5	4	9	250	120	16-DIP/SO	±4.5 to ±20		1.29
DG442	4 SPST NO	85	0.5	4	9	250	120	16-DIP/SO	±4.5 to ±20		1.29
DG444	4 SPST NC	85	0.5	4	9	250	120	16-DIP/SO	±4.5 to ±20		1.03
DG445	4 SPST NO	85	0.5	4	9	250	120	16-DIP/SO	±4.5 to ±20		1.03
MAX4521	4 SPST NC	100	1	4	12	80	30	16-DIP/SO/QSOP	+2 to +12	Improved, low-voltage DG211	0.69
MAX4522	4 SPST NC	100	1	4	12	80	30	16-DIP/SO/QSOP	+2 to +12	Improved, low-voltage DG212	0.69
MAX4523	4 SPST	100	1	4	12	80	30	16-DIP/SO/QSOP	+2 to +12	Improved, low-voltage DG213	0.69
MAX4536	4 SPST NO	100	1	4	10	100	50	16-DIP/SO/QSOP	+2 to +12	Improved 74HC4316	0.98
MAX4537	4 SPST NC	100	1	4	10	100	50	16-DIP/SO/QSOP	+2 to +12	Improved 74HC4316	0.98
MAX4538	4 SPST NO, NC	100	1	4	10	100	50	16-DIP/SO/QSOP	+2 to +12	Improved 74HC4316	0.98
DG308A	4 SPST NO	100	1			200	150	16-DIP/SO	±4.5 to ±20	CMOS logic levels, high speed, low R_{ON}	0.95
DG309	4 SPST NC	100	1			200	150	16-DIP/SO	±4.5 to ±20	CMOS logic levels, high speed, low R_{ON}	0.95
MAX331	4 SPST NC	175	1			600	450	16-DIP/SO	±4.5 to ±20	Improved DG201	3.37
MAX332	4 SPST NO	175	1			600	450	16-DIP/SO	±4.5 to ±20	Improved DG201	3.37
DG211	4 SPST NC	175	5			1000	500	16-DIP/SO	±4.5 to ±20	No V_{LOGIC} supply	0.91
DG212	4 SPST NO	175	5			1000	500	16-DIP/SO	±4.5 to ±20	No V_{LOGIC} supply	0.91
DG201A	4 SPST NC	200	1			600	450	16-DIP/SO	±4.5 to ±20	Low power, no V_{LOGIC} supply	0.95
DG202	4 SPST NO	200	1			600	450	16-DIP/SO	±4.5 to ±20	No V_{LOGIC} supply	0.95
MAX326	4 SPST NC	3500	0.01			1000	500	16-DIP/SO	±4.5 to ±20	Ultra-low leakage, low charge injection	2.78
MAX327	4 SPST NO	3500	0.01			1000	500	16-DIP/SO	±4.5 to ±20	Ultra-low leakage, low charge injection	2.78
MAX395	8 SPST	100	1	4		400	400	24-DIP/SO/SSOP	±2.7 to ±8	Low voltage, serial interface with break-before-make	2.98
MAX335	8 SPST	175	1			400	400	24-DIP/SO	±4.5 to ±20	Serial interface with break-before-make	2.84
SPDT											
MAX319	SPDT	45	0.25	2	3	175	145	8-SO/DIP	±4.5 to ±20	Improved DG419, low R_{ON} match and flatness	1.19
DG419	SPDT	45	0.25	3	4	175	145	8-SO/DIP	±4.5 to ±20		1.19
IH5050	SPDT	45	5			1000	500	16-SO/DIP	±4.5 to ±20		3.94
DG301A	SPDT	50	1			300	250	14-DIP	±4.5 to ±20	2.4V_{IH}, low R_{ON}	1.94
DG305A	SPDT	50	1			250	150	14-DIP	±4.5 to ±20	CMOS logic levels, high speed, low R_{ON}	2.55
DG387A	SPDT	50	1			300	250	14-DIP	±4.5 to ±20	Low R_{ON}	2.08
IH5142	SPDT	75	1			200	125	16-DIP/SO	±4.5 to ±20		3.23
IH5042	SPDT	80	5			400	200	16-DIP/SO	±4.5 to ±20		1.84
MAX383	2 SPDT	35	0.1	2	4	175	100	16-DIP/SO	±2.7 to ±8	Single supply, +2.7V to +16V	2.57
MAX303	2 SPDT	45	0.25	2	3	150	100	16-DIP/SO	±4.5 to ±20	Improved DG403, low R_{ON} match and flatness	2.57
DG403	2 SPDT	45	0.5	2	3	150	100	16-DIP/SO	±4.5 to ±20	Low power, high speed, low leakage	2.57
DG423	2 SPDT	45	0.25	3	4	250	200	16-DIP/SO	±4.5 to ±20	Low power, high speed, has latches	3.30
IH5051	2 SPDT	45	5			1000	500	16-DIP/SO	±4.5 to ±20	Low power, low R_{ON}	4.73
DG303A	2 SPDT	50	1			300	250	14-DIP	±4.5 to ±20	2.4V_{IH}, low R_{ON}	2.36
DG307A	2 SPDT	50	1			250	150	14-DIP	±4.5 to ±20	CMOS logic levels, high speed, low R_{ON}	2.36
DG390A	2 SPDT	50	1			300	250	14-DIP	±4.5 to ±20	Low R_{ON}	2.60
IH5143	2 SPDT	75	1			200	125	16-DIP/SO	±4.5 to ±20		3.49
IH5043	2 SPDT	80	1			400	200	16-DIP/SO	±4.5 to ±20		2.36
MAX333A	4 SPDT	35	0.25	2	3	175	145	18-DIP/SO	±4.5 to ±20	Improved MAX333, low R_{ON}	3.60
MAX394	4 SPDT	35	0.25	2	3	175	145	18-DIP/SO, 20-SSOP	±2.7 to ±8	MAX333A replacement, low-voltage, +2.7V to +16V	3.19
MAX333	4 SPDT	175	5			1000	500	18-DIP/SO	±4.5 to ±20		2.87

[1] NO = Normally Open, NC = Normally Closed

[2] Drain-source on-resistance is for the commercial grade, T_A = +25°C.

† Prices provided are for design guidance only and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

Analog Switches (continued)

Part Number	Function[1]	$R_{DS(ON)}$[2] (Ω max)	$I_{COM(OFF)}$/ $I_{D(OFF)}$ (nA max)	R_{ON} Match (Ω max)	R_{ON} Flatness (Ω max)	$t_{(ON)}$ (ns max)	$t_{(OFF)}$ (ns max)	Pins-Package Options	Supply Voltage Range (V)	Features	Price† 1000-up ($)
DPST											
IH5144	DPST NO	75	1			200	125	16-DIP/SO	±4.5 to ±20		3.23
IH5044	DPST NO	80	5			400	200	16-DIP/SO	±4.5 to ±20		2.29
MAX385	2 DPST	35	0.1	2	4	175	100	16-DIP/SO	±2.7 to ±8	Single supply, +2.7V to +16V	2.57
MAX305	2 DPST NO	45	0.25	2	3	150	100	16-DIP/SO	±4.5 to ±20	Improved DG405, low R_{ON} match and flatness	2.57
DG405	2 DPST NO	45	0.25	2	3	150	100	16-DIP/SO	±4.5 to ±20	High speed, low leakage	2.57
DG425	2 DPST	45	0.25	2	3	250	200	16-DIP/SO	±4.5 to ±20	High speed, has latches	3.30
IH5049	2 DPST NO	45	5			1000	500	16-DIP/SO	±4.5 to ±20	Low R_{ON}	5.35
DG302A	2 DPST NC	50	1			300	250	14-DIP	±4.5 to ±20	2.4V_{IH}, low R_{ON}	2.50
DG306A	2 DPST NC	50	1			250	150	14-DIP	±4.5 to ±20	CMOS logic levels, high speed, low R_{ON}	2.53
DG384A	2 DPST NC	50	1			300	250	14-DIP	±4.5 to ±20		2.92
IH5145	2 DPST NC	75	1			200	125	16-DIP/SO	±4.5 to ±20		3.82
IH5045	2 DPST NC	80	1			400	200	16-DIP/SO	±4.5 to ±20		2.44
IH5047	4PST NC	75	1			400	200	16-DIP/SO	±4.5 to ±20		2.44

Video Switches

Part Number	Function[1]	$R_{DS(ON)}$[2] (Ω max)	$I_{D(OFF)}$ (nA max)	$t_{(ON)}$ (µs max)	V_{IL}/V_{IH} (V)	Analog-Signal Voltage Range (V)	Features	Price† 1000-up ($)
IH5341	2 SPST NO	75	0.5	0.300	0.8/2.4	±10	70dB isolation at 10MHz	2.48
IH5352	4 SPST NO	75	0.5	0.300	0.8/2.4	±10	70dB isolation at 10MHz	4.50

Signal-Line Circuit Protectors

Part Number	Function	$R_{DS(ON)}$[2] (Ω max)	$I_{D(OFF)}$ (nA max)	Analog-Signal Voltage Range (V)	Features	Price† 1000-up ($)
MAX366‡	3-line	100	1.0	-12.5 to 13.5	±35V overvoltage protected	1.42
MAX367‡	8-line	100	1.0	-12.5 to 13.5	±35V overvoltage protected	2.43

Phase-Reversal Switches

Part Number	Function	$R_{DS(ON)}$[2] (Ω max)	On-Leakage (nA)	t_{ON}/t_{OFF} (ns max)	Supply Voltage Range (V)	Features	Price† 1000-up ($)
MAX4526	Dual SPDT	175	0.5	0.1/0.1	±4.5 to ±20	High speed, 8-pin DIP/SO	††
MAX4527	Dual SPDT	175	0.5	0.2/0.2	±4.5 to ±20	Low power	††

1 NO = Normally Open, NC = Normally Closed
2 Drain-source on resistance is for the commercial grade, T_A = + 25°C.
† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
‡ No control required. Switches are always on when power is on.
†† Future product—contact factory for pricing and availability. Specifications are preliminary.

Analog Multiplexers

Fault Protected

8-Channel

MAX354 (±35V)*
MAX355 (diff ±35V)*
MAX358 (±35V)*
MAX359 (diff ±35V)*
MAX368 (latch ±35V)*
MAX369 (latch, diff ±35V)*
MAX378 (±75V)*
MAX379 (diff ±75V)*
MAX388 (latch ±100V)*
MAX389 (latch, diff ±100V)*
HI-508A (±35V)*
HI-509A (diff ±35V)*

Standard

4-Channel

★ MAX4518‡
★ MAX4519 (dual 2:1)‡

8-Channel

MAX308
MAX309 (diff)
MAX349‡
MAX350 (diff)‡
MAX382 (latch)‡
MAX384 (latch, diff)‡
MAX398‡
MAX399 (diff)‡
MAX4051‡
MAX4051A‡
MAX4052‡
MAX4052A (diff)‡
MAX4053‡
MAX4053A‡
† MAX4530‡
† MAX4531 (diff)‡
† MAX4532 (triple 2:1)‡
DG408
DG409 (diff)
DG508A
DG509A (diff)
DG528 (latch)
DG529 (latch, diff)
MX7501
MX7502 (diff)
MX7503

16-Channel

MAX306
MAX307 (diff)
MAX396‡
MAX397 (diff)‡
DG406
DG407 (diff)
DG506A
DG507A (diff)
MX7506
MX7507 (diff)

Video

8-Channel

MAX310 (70dB at 10MHz)
MAX311 (diff 70dB at 10MHz)

Mux/Amplifier

MAX440
MAX441
MAX442
MAX453 (1 of 2, drives 75Ω)
MAX454 (1 of 4, drives 75Ω)
MAX455 (1 of 8, drives 75Ω)

Crosspoint

MAX4111 (1x1)
MAX4121 (2x1)
MAX4221 (Dual 2x1)
MAX4141 (4x1)
MAX456 (8x8)
MAX458 (8x4)
MAX459 (8x4)

Low Leakage

8-Channel

MAX328 (10pA)
MAX329 (diff, 10pA)
MAX338 (20pA)
MAX339 (diff, 10pA)

16-Channel

† MAX336 (20pA)
† MAX337 (diff, 10pA)

★ New product
† Future product
* Withstands quoted input or output voltage indefinitely with/without supply voltage present
‡ Guaranteed 3V operation

Part Number	Function	$R_{DS(ON)}$* (Ω max)	$I_{D(OFF)}/I_{COM(OFF)}$ (nA max)	R_{ON} Match (Ω max)	$t_{(ON)}/t_{(OFF)}$ (µs max)	Supply Voltage Range (V)	Features	Price† 1000-up ($)
MAX4518	1-of-4	100	0.2	4	0.15/0.15	±2.7 to ±8	Low voltage, guaranteed R_{ON} match	1.15
MAX308	1-of-8	100	0.75	5	0.225/0.150	±4.5 to ±20	Improved DG408, guaranteed R_{ON} match and flatness	2.59
MAX382	1-of-8	100	0.2	4	0.15/0.15	+3, +5, ±5	Low-voltage, latchable address inputs	3.00
MAX398	1-of-8	100	0.1	4	0.15/0.15	+3, +5, ±5	Low-voltage, DG408 pinout	2.59
MAX4051A	1-of-8	100	0.1	4	0.15/0.15	+2.7 to +16	Improved 74HC4051, low voltage, improved R_{ON}	1.87
DG408	1-of-8	100	1		0.225/0.150	±4.5 to ±20	Industry standard	2.59
MAX349	1-of-8	100	0.1	5	0.275/0.150	+3, +5, ±5	Serial interface	2.98
MAX4530	1-of-8	100	1	10	—	+2 to +12	Improved 74HC4351	††
MAX4051	1-of-8	125	1	10	0.15/0.15	+2.7 to +16	Low-voltage, 74HC4051 upgrade	1.46
MAX354	1-of-8	350	0.5	12	0.25/0.20	±4.5 to ±20	Improved MAX358, improved R_{ON}, ±35V fault protection	2.45
DG508A	1-of-8	350	2		1.0/1.7	±15	Industry standard	2.39
MX7501	1-of-8	350	5		1.5/1.0	±15	Industry standard	5.58
MX7503	1-of-8	350	5		1.5/1.0	±15	Industry standard	5.58
MAX338	1-of-8	400	0.02	10	0.50/0.50	±4.5 to ±20	Improved DG508A, low-leakage upgrade, QSOP	2.39
DG528	1-of-8	450	10		1.5	±15	Industry standard with latches	2.28
MAX358	1-of-8	1800	1		0.5	±15	Fault protected to ±35V	2.45
MAX368	1-of-8	1800	2		1.5/1.0	±15	Fault protected with latches to ±35V	3.50
HI-508A	1-of-8	1800	2		0.5	±15	Fault protected to ±35V	2.75
MAX378	1-of-8	3500	1		0.75/0.5	±15	Fault protected to ±75V	3.50
MAX388	1-of-8	3000	1		1	±15	Fault protected with latches to ±100V	4.50
MAX328	1-of-8	5000	0.02		1	±15	Ultra-low leakage	3.61
IH5108	Use MAX358 (pin-for-pin compatible upgrade)							–
IH6108	Use DG508A (pin-for-pin compatible upgrade)							–
MAX4519	2-of-4	100	0.1	4	0.15/0.15	±2.7 to ±8	Low-voltage, guaranteed R_{ON} match	1.15
MAX309	2-of-8	100	1	5	0.225/0.150	±4.5 to ±20	Improved DG409, guaranteed R_{ON} match and flatness	2.59
MAX384	2-of-8	100	0.2	4	0.15/0.15	+3, +5, ±5	Low-voltage, latchable address inputs	3.00
MAX399	2-of-8	100	0.1	4	0.15/0.15	+3, +5, ±5	Low-voltage, DG409 pinout	2.59
MAX4052A	2-of-8	100	0.1	4	0.15/0.15	+2.7 to +16	Improved 74HC4051, low voltage, improved R_{ON}	1.87
DG409	2-of-8	100	1		0.225/0.150	±4.5 to ±20	Industry standard	2.59
MAX4531	2-of-8	100	1	10	—	+2 to +12	Improved 74HC4352	††
MAX350	2-of-8	125	1	10	0.275/0.150	+3, +5, ±5	Low-voltage, serial interface	2.98
MAX4052	2-of-8	125	1	10	0.15/0.15	+2.7 to +16	Low-voltage, 74HC4052 upgrade	1.46
MAX4053	1-of-2	125	1	10	0.15/0.15	+2.7 to +16	Low-voltage, 74HC4053 upgrade	1.46
MAX4532	1-of-2	100	1	10	—	+2 to +12	Improved 74HC4353	††
MAX4053A	1-of-2	100	0.1	4	0.15/0.15	+2.7 to +16	Improved 74HC4051, low voltage, improved R_{ON}	1.87
MAX355	2-of-8	350	0.5	12	0.25/0.20	±4.5 to ±20	Improved MAX359, improved R_{ON}, ±35V fault protection	2.45
DG509A	2-of-8	350	2		1.0/1.7	±15	Industry standard	2.39
MX7502	2-of-8	350	3		1.5/1.0	±15	Industry standard	5.58
MAX339	2-of-8	400	0.02	10	0.50/0.50	±4.5 to ±20	Improved DG509A, low-leakage upgrade, QSOP	2.39
DG529	2-of-8	450	10		1.5	±15	Industry standard with latches	2.28
MAX359	2-of-8	1800	1		0.5	±15	Fault protected to ±35V	2.45
MAX369	2-of-8	1800	1		1.5/1.0	±15	Fault protected with latches to ±35V	3.50
HI-509A	2-of-8	1800	2		0.5	±15	Fault protected to ±35V	2.75
MAX379	2-of-8	3500	1		0.75/0.5	±15	Fault protected to ±75V	3.50
MAX389	2-of-8	3000	1		1	±15	Fault protected with latches to ±100V	4.50
MAX329	2-of-8	5000	0.02		1	±15	Ultra-low leakage	3.61
IH5208	Use MAX359 (pin-for-pin compatible upgrade)							–
IH6208	Use DG509A (pin-for-pin compatible upgrade)							–
MAX306	1-of-16	100	2	5	0.2/0.15	±4.5 to ±20	Improved DG406, guaranteed R_{ON} match and flatness	3.87
MAX336	1-of-16	400	0.02	10	0.5/0.5	±4.5 to ±20	Improved DG506A, low leakage, SSOP	††
MAX396	1-of-16	100	0.1	4	0.15/0.15	+3, +5, ±5	Low-voltage, DG406 pinout	4.04
DG406	1-of-16	100	2		0.2/0.15	±4.5 to ±20	Industry standard	4.53
DG506A	1-of-16	450	5		1.0/0.4(typ)	±15	Industry standard	3.68
MX7506	1-of-16	450	5		15/1.0	±15	Industry standard	10.25

* Drain-source on-resistance is for the commercial grade, T_A = +25°C.
† Prices provided are for design guidance only and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future product—contact factory for pricing and availability. Specifications are preliminary.

Analog Multiplexers (continued)

Part Number	Function	$R_{DS(ON)}$* (Ω max)	$I_{D(OFF)}/I_{COM(OFF)}$ (nA max)	R_{ON} Match (Ω max)	$t_{(ON)}/t_{(OFF)}$ (µs max)	Supply Voltage Range (V)	Features	Price† 1000-up ($)
IH6116	Use MAX506A (pin-for-pin compatible upgrade)							–
MAX307	2-of-16	100	2	5	0.2/0.15	±4.5 to ±20	Improved DG407, guaranteed R_{ON} match and flatness	3.87
MAX337	2-of-16	400	0.02	10	0.5/0.5	±4.5 to ±20	Improved DG507A, low leakage, SSOP	††
MAX397	1-of-16	100	0.1	4	0.15/0.15	+3, +5, ±5	Low-voltage, DG407 pinout	4.04
DG407	2-of-16	100	2		0.2/0.15	±15	Industry standard	4.53
MX7507	2-of-16	450	5		1.5/1.0	±15	Industry standard	10.25
DG507A	2-of-16	450	5		1.0/0.4(typ)	±15	Industry standard	3.68
IH6216	Use DG507A (pin-for-pin compatible upgrade)							–

Video Multiplexers

Part Number	Unity GBW (MHz)	Slew Rate (V/µs)	DP/DG (degrees/%)	Output Current (mA max)	Supply Voltage (V)	Supply Current (mA)	Features	Price† 1000-up ($)
MAX440	160 110 ($A_V \geq 2$)	370	0.03/0.04	35	±5	40	Video amp with 8-channel mux, 0.03°/0.04% diff phase/gain error, 15ns switch time, high-Z output state	8.95
MAX441	160 110 ($A_V \geq 2$)	370	0.03/0.04	35	±5	40	Video amp with 4-channel mux 0.03°/0.04% diff phase/gain error, 15ns switch time	5.90
MAX442	140	250	0.03/0.04	35	±5	40	Video amp with 4-channel mux, 15ns switch time, 8-pin DIP/SO	4.45

Part Number	Function[1]	$R_{DS(ON)}$[2] (Ω max)	$I_{D(OFF)}$ (nA max)	$t_{(ON)}$ (µs max)	V_{IL}/V_{IH} (V)	Analog-Signal Voltage Range (V)	Features	Price† 1000-up ($)
MAX453	1-of-2 mux	Buffered output	10	0.12	0.8/2.4	±2	On-chip output amp	3.94
MAX454	1-of-4 mux	Buffered output	10	0.12	0.8/2.4	±2	On-chip output amp	5.25
MAX455	1-of-8 mux	Buffered output	10	0.12	0.8/2.4	±2	On-chip output amp	8.75
MAX310	1-of-8 mux	250	10	1.5	0.8/2.4	-12.5 to +13.5	70dB isolation at 10MHz	5.18
MAX311	2-of-8 mux	250	10	1.5	0.8/2.4	-12.5 to +13.5	70dB isolation at 10MHz	7.20

Part Number	Unity GBW (MHz)	Slew Rate (V/µs)	DP/DG (degrees/%)	Off Isolation (dB typ)	Crosstalk (dB typ)	EV Kit	Features	Price† 1000-up ($)
VIDEO CROSSPOINT SWITCHES								
MAX4111	330	700	0.01/0.01	74 (30MHz)	N/A	Yes	1x1 video crosspoint building block, 0.1dB gain flatness of 150MHz	1.70
MAX4121	330	700	0.01/0.01	74 (30MHz)	66	Yes	2x1 video crosspoint building block, 0.1dB gain flatness of 150MHz	2.10
MAX4221	330	700	0.01/0.01	74 (30MHz)	66	Yes	Dual 2x1 video crosspoint building block, 0.1dB gain flatness of 150MHz	4.50
MAX4141	330	700	0.01/0.01	74 (30MHz)	66	Yes	4x1 video crosspoint building block, 0.1dB gain flatness of 150MHz	4.50
MAX456	35	250	1/0.5	80 (5MHz)	70 (5MHz)		8x8 crosspoint switch array with eight output buffers, high-Z output capability	19.98
MAX458/459	100/90	300	0.05/0.01	60 (10MHz)	55 (10MHz)	Yes	8x4 crosspoint switch array with four 75Ω cable drivers, high-Z output capability	21.85

1 NO = Normally Open, NC = Normally Closed
2 Drain-source on resistance is for the commercial grade, T_A = +25°C.
† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future product—contact factory for pricing and availability. Specifications are preliminary.

19-0420; Rev 0; 9/95

MAXIM

10Ω, Quad, SPST, CMOS Analog Switches

General Description

Maxim's MAX312/MAX313/MAX314 analog switches feature low on-resistance (10Ω max) and 1.5Ω on-resistance matching between channels. These switches conduct equally well in either direction. They offer low leakage over temperature (2.5nA at +85°C). Low power consumption and ESD tolerance greater than 2000V per Method 3015.7 are guaranteed.

The MAX312/MAX313/MAX314 are quad, single-pole/single-throw (SPST) analog switches. The MAX312 is normally closed (NC), and the MAX313 is normally open (NO). The MAX314 has two NC switches and two NO switches. All three devices operate from a single supply of +4.5V to +30V or from dual supplies of ±4.5V to ±20V.

Features

- **Pin Compatible with DG411/DG412/DG413**
- **Low On-Resistance (6.5Ω typical)**
- **Guaranteed R_{ON} Match Between Channels (1.5Ω max)**
- **Guaranteed R_{ON} Flatness over Specified Signal Range (2Ω max)**
- **Guaranteed ESD Protection > 2000V per Method 3015.7**
- **Crosstalk > 96dB at 20kHz**
- **Single-Supply Operation: +4.5V to +30V**
  Dual-Supply Operation: ±4.5V to ±20V
- **Rail-to-Rail Signal Handling**

Applications

Test Equipment
Communication Systems
PBX, PABX Systems
Audio Signal Routing
Avionics
Sample-and-Hold Circuits
Data Acquisition Systems

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX312CPE	0°C to +70°C	16 Plastic DIP
MAX312CSE	0°C to +70°C	16 Narrow SO
MAX312C/D	0°C to +70°C	Dice*
MAX312EPE	-40°C to +85°C	16 Plastic DIP
MAX312ESE	-40°C to +85°C	16 Narrow SO
MAX312MJE	-55°C to +125°C	16 CERDIP**

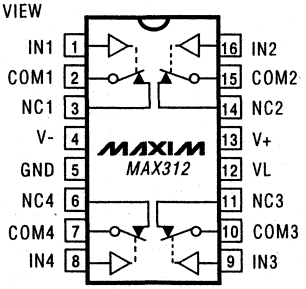
Ordering Information continued at end of data sheet.

** Contact factory for dice specifications.*

***Contact factory for availability.*

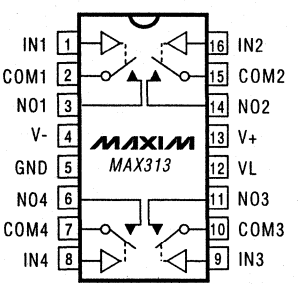
Pin Configurations/Functional Diagrams/Truth Tables

TOP VIEW



DIP/SO

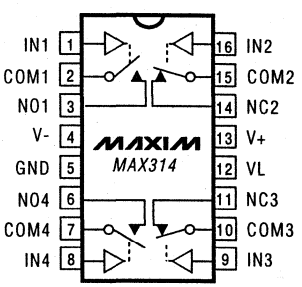
MAX312	
LOGIC	SWITCH
0	ON
1	OFF



DIP/SO

MAX313	
LOGIC	SWITCH
0	OFF
1	ON

SWITCHES SHOWN FOR LOGIC "0" INPUT



DIP/SO

MAX314		
LOGIC	SWITCHES 1, 4	SWITCHES 2, 3
0	OFF	ON
1	ON	OFF

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10Ω, Quad, SPST, CMOS Analog Switches

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to GND
V+ .....-0.3V to +44V
V- .....+0.3V to -44V
V+ to V- .....-0.3V to +44V
VL .....(GND - 0.3V) to (V+ + 0.3V)
All Other Pins (Note 1) .....(V- - 2V) to (V+ + 2V)
or 30mA (whichever occurs first)
Continuous Current (COM_, NO_, NC_) .....±100mA
Peak Current (COM_, NO_, NC_) .....±300mA

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
Narrow SO (derate 8.70mW/°C above +70°C) 696mW
CERDIP (derate 10.00mW/°C above +70°C) 800mW
Operating Temperature Ranges
MAX31_C_ .....0°C to +70°C
MAX31_E_ .....-40°C to +85°C
MAX31_M_ .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: Signals on NC_, NO_, COM_, or IN_ exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current rating.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = 15V, V- = -15V, VL = 5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	$V_{COM_}$, $V_{NO_}$, $V_{NC_}$	(Note 3)			V-		V+	V
On-Resistance	R_{ON}	I_{COM} = 10mA, $V_{NO_}$ or $V_{NC_}$ = ±10V	T_A = +25°C	C, E		6.5	10	Ω
				M			9	
			T_A = T_{MIN} to T_{MAX}				15	
On-Resistance Match Between Channels (Note 4)	ΔR_{ON}	I_{COM} = 10mA, $V_{NO_}$ or $V_{NC_}$ = ±10V	T_A = +25°C			0.3	1.5	Ω
			T_A = T_{MIN} to T_{MAX}				3	
On-Resistance Flatness (Note 5)	$R_{FLAT(ON)}$	I_{COM} = 10mA, $V_{NO_}$ or $V_{NC_}$ = -5V, 0V, 5V	T_A = +25°C			0.2	2	Ω
			T_A = T_{MIN} to T_{MAX}				4	
Off Leakage Current (NO_ or NC_) (Note 6)	I_{NO} I_{NC}	V_{COM} = ∓10V, $V_{NO_}$ or $V_{NC_}$ = ±10V	T_A = +25°C		-0.5	-0.02	0.5	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-2.5		2.5	
				M	-40		40	
COM Off Leakage Current (Note 6)	$I_{NC(OFF)}$	V_{COM} = ±10V, $V_{NO_}$ or $V_{NC_}$ = ∓10V	T_A = +25°C		-0.5	-0.02	0.5	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-2.5		2.5	
				M	-40		40	
COM On Leakage Current (Note 6)	$I_{COM(ON)}$	V_{COM} = ±10V, $V_{NO_}$ or $V_{NC_}$ = ±10V	T_A = +25°C		-1	-0.04	1	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-5		5	
				M	-100		100	

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = 15V, V- = -15V, VL = 5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
LOGIC INPUT							
Input Current with Input Voltage High	I_{INH}	IN_ = 2.4V, all others = 0.8V		-0.500	0.005	0.500	µA
Input Current with Input Voltage Low	I_{INL}	IN_ = 0.8V, all others = 2.4V		-0.500	0.005	0.500	µA
POWER SUPPLY							
Power-Supply Range				±4.5		±20.0	V
Positive Supply Current	I+	All channels on or off, V_{IN} = 0V or 5V, V+ = 16.5V, V- = -16.5V	T_A = +25°C	-1	0.0001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Negative Supply Current	I-	All channels on or off, V_{IN} = 0V or 5V, V+ = 16.5V, V- = -16.5V	T_A = +25°C	-1	0.0001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Logic Supply Current	I_L	All channels on or off, V_{IN} = 0V or 5V, V+ = 16.5V, V- = -16.5V	T_A = +25°C	-1	0.0001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Ground Current	I_{GND}	All channels on or off, V_{IN} = 0V or 5V, V+ = 16.5V, V- = -16.5V	T_A = +25°C	-1	-0.0001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
DYNAMIC							
Turn-On Time	t_{ON}	Figure 2, V_{COM} = ±10V	T_A = +25°C		70	225	ns
			T_A = T_{MIN} to T_{MAX}			275	
Turn-Off Time	t_{OFF}	Figure 2, V_{COM} = ±10V	T_A = +25°C		65	185	ns
			T_A = T_{MIN} to T_{MAX}			235	
Break-Before-Make Time Delay	t_D	MAX314 only, Figure 3, R_L = 300Ω, C_L = 35pF	T_A = +25°C	1	5		ns
Charge Injection (Note 3)	V_{CTE}	C_L = 1.0nF, V_{GEN} = 0V, R_{GEN} = 0Ω, Figure 4	T_A = +25°C	-30	20	30	pC
Off Isolation (Note 7)	V_{ISO}	R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 5	T_A = +25°C		-65		dB
Crosstalk (Note 8)	V_{CT}	R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 6	T_A = +25°C		-85		dB
NC or NO Capacitance	$C_{(OFF)}$	f = 1MHz, Figure 7	T_A = +25°C		15		pF
COM Off Capacitance	$C_{(COM)}$	f = 1MHz, Figure 7	T_A = +25°C		15		pF
On Capacitance	$C_{(COM)}$	f = 1MHz, Figure 7	T_A = +25°C		47		pF

10Ω, Quad, SPST, CMOS Analog Switches

ELECTRICAL CHARACTERISTICS—Single Supply

(V+ = 12V, V- = 0V, VL = 5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

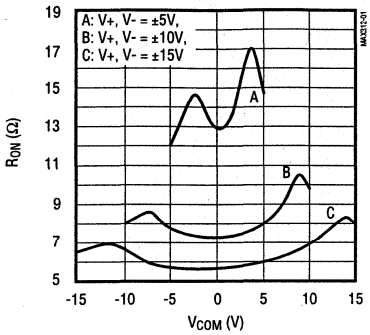
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{COM_}$, $V_{NO_}$, $V_{NC_}$	(Note 3)		0		V+	V
Channel On-Resistance	R_{ON}	I_{COM} = 10mA, $V_{NC_}$ or $V_{NO_}$ +10V	T_A = +25°C		12.5	25	Ω
			T_A = T_{MIN} to T_{MAX}			35	
POWER SUPPLY							
Positive Supply Current	I+	V+ = 13.2V all channels on or off, V_{IN} = 0V or 5V	T_A = +25°C	-1	0.0001	1	µA
			T_A = T_{MAX}	-5		5	
Logic Supply Current	I_L	V_L = 5.5V all channels on or off, V_{IN} = 0V or 5V	T_A = +25°C	-1	0.0001	1	µA
			T_A = T_{MAX}	-5		5	
Ground Current	I_{GND}	V_L = 5.5V all channels on or off, V_{IN} = 0V or 5V	T_A = +25°C	-1	-0.0001	1	µA
			T_A = T_{MAX}	-5		5	
DYNAMIC							
Turn-On Time (Note 3)	t_{ON}	Figure 2, $V_{NO_}$ or $V_{NC_}$ = 8V	T_A = +25°C		100	325	ns
			T_A = T_{MIN} to T_{MAX}			425	
Turn-Off Time (Note 3)	t_{OFF}	Figure 2, $V_{NO_}$ or $V_{NC_}$ = 8V	T_A = +25°C		95	175	ns
			T_A = T_{MIN} to T_{MAX}			225	
Break-Before-Make Time Delay (Note 3)	t_D	MAX314 only, Figure 3 R_L = 300Ω, C_L = 35pF	T_A = +25°C		5		ns
Charge Injection (Note 3)	V_{CTE}	Figure 4, C_L = 1.0nF, V_{GEN} = 0V, R_{GEN} = 0V	T_A = +25°C		-5		pC

Note 2: The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.
Note 3: Guaranteed by design.
Note 4: $\Delta R_{ON} = \Delta R_{ON}$ max - ΔR_{ON} min.
Note 5: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.
Note 6: Leakage parameters are 100% tested at maximum-rated hot temperature and guaranteed by correlation at +25°C.
Note 7: Off isolation = $20\log_{10}$ [V_{COM} / (V_{NC} or V_{NO})], V_{COM} = output, V_{NC} or V_{NO} = input to off switch.
Note 8: Between any two switches.
Note 9: Leakage testing at single supply is guaranteed by testing with dual supplies.

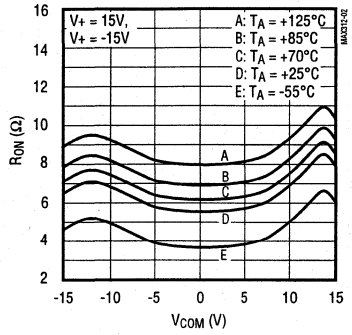
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

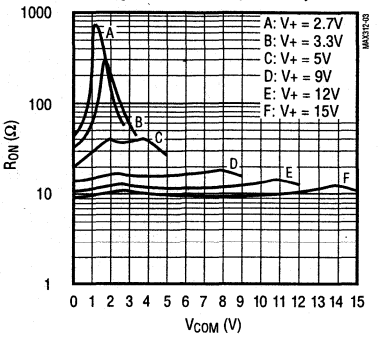
ON-RESISTANCE vs. V_{COM} (BIPOLAR SUPPLIES)



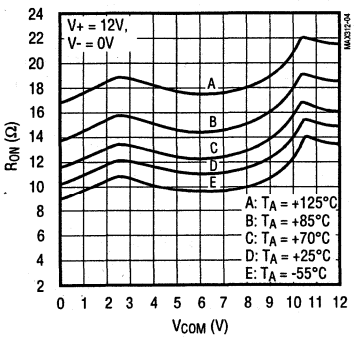
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE



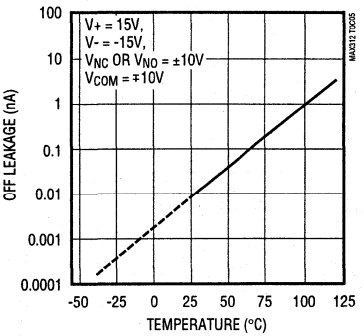
ON-RESISTANCE vs. V_{COM} (SINGLE SUPPLY, V- = 0V)



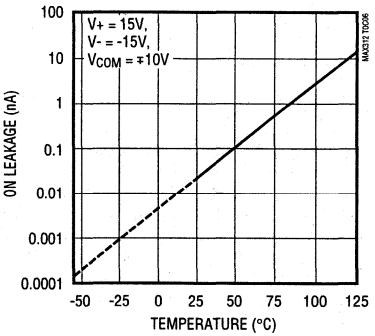
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE



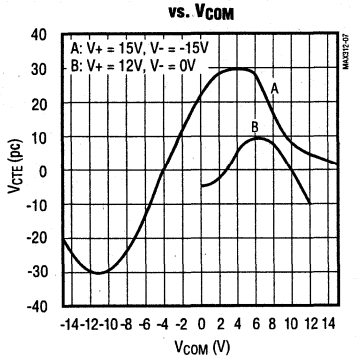
OFF LEAKAGE CURRENT vs. TEMPERATURE



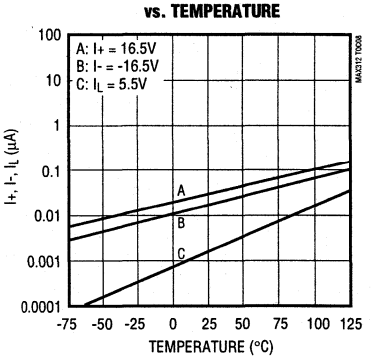
ON LEAKAGE CURRENT vs. TEMPERATURE



CHARGE INJECTION vs. V_{COM}



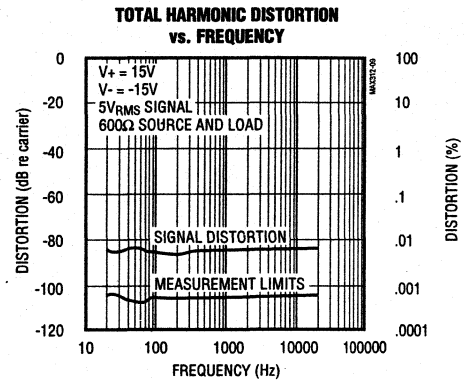
SUPPLY CURRENT vs. TEMPERATURE

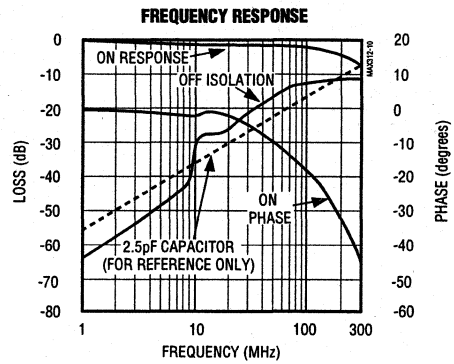


10Ω, Quad, SPST, CMOS Analog Switches

Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)





Pin Description

PIN			NAME	FUNCTION
MAX312	MAX313	MAX314		
1, 8, 9, 16	1, 8, 9, 16	1, 8, 9, 16	IN2, IN4, IN3, IN2	Logic Level Inputs
2, 7, 10, 15	2, 7, 10, 15	2, 7, 10, 15	COM1, COM4, COM3, COM2	Analog Signal Common Terminals
3, 6, 11, 14	—	—	NC1, NC4, NC3, NC2	Analog Signal Normally Closed Terminals
—	3, 6, 11, 14	—	NO1, NO4, NO3, NO2	Analog Signal Normally Open Terminals
—	—	3, 6	NO1, NO4	Analog Signal Normally Open Terminals
—	—	11, 14	NC3, NC2	Analog Signal Normally Closed Terminals
4	4	4	V-	Negative Analog Supply Input (connect to GND for single-supply operation)
5	5	5	GND	Logic Level Ground
12	12	12	VL	Logic Supply Voltage
13	13	13	V+	Positive Analog Supply Input

Applications Information

Low-Distortion Audio

The MAX312/MAX313/MAX314, having very low RON and very low RON variation with signal amplitude, are well suited for low-distortion audio applications. The *Typical Operating Characteristics* show Total Harmonic Distortion (THD) vs. Frequency graphs for several signal amplitudes and impedances. Higher source and load impedances improve THD, but reduce off isolation.

Off Isolation at High Frequencies

In 50Ω systems, the high-frequency on-response of these parts extends from DC to above 100MHz with a typical loss of -2dB. When the switch is turned off, however, it behaves like a capacitor, and off isolation decreases with increasing frequency. (Above 300MHz, the switch actually passes more signal turned off than turned on.) This effect is more pronounced with higher source and load impedances.

Above 5MHz, circuit board layout becomes critical, and it becomes difficult to characterize the response of the switch independent of the circuit. The graphs shown in the *Typical Operating Characteristics* were taken using a 50Ω source and load connected with BNC connectors to a circuit board deemed "average"; that is, designed with isolation in mind, but not using strip-line or other special RF circuit techniques. For critical applications above 5MHz, use the MAX440, MAX441, and MAX442, which are fully characterized up to 160MHz.

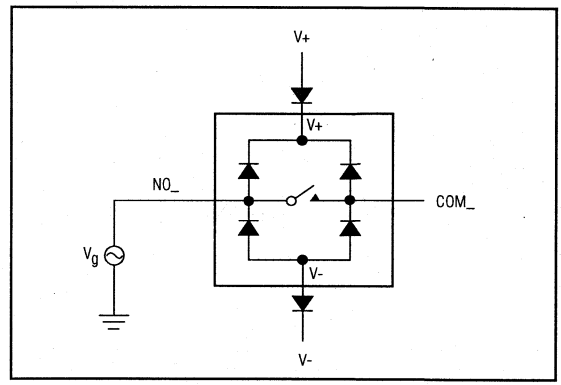


Figure 1. Overvoltage Protection Using External Blocking Diodes

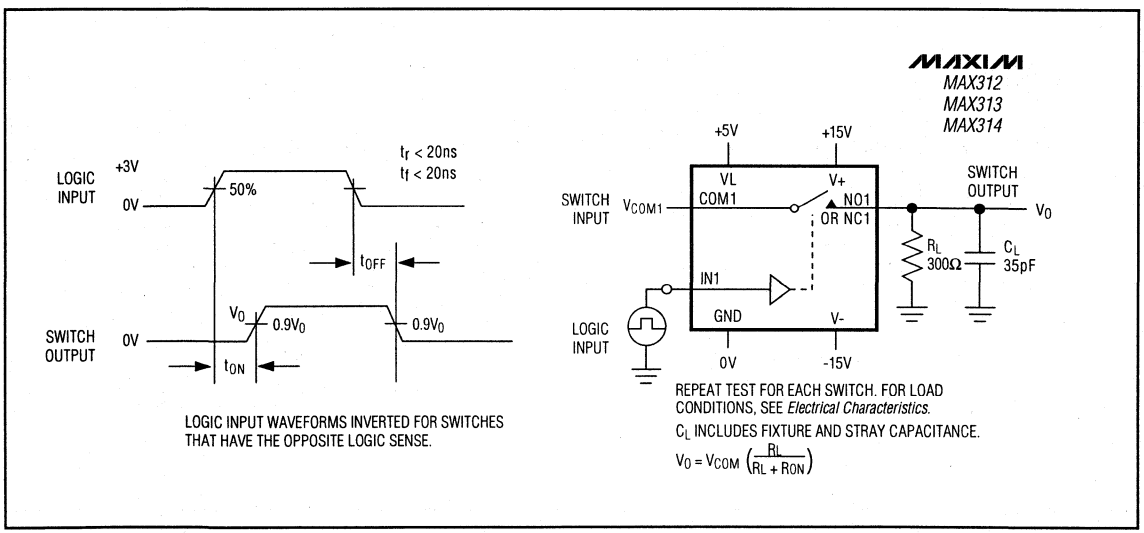


Figure 2. Switching-Time Test Circuit

10Ω, Quad, SPST, CMOS Analog Switches

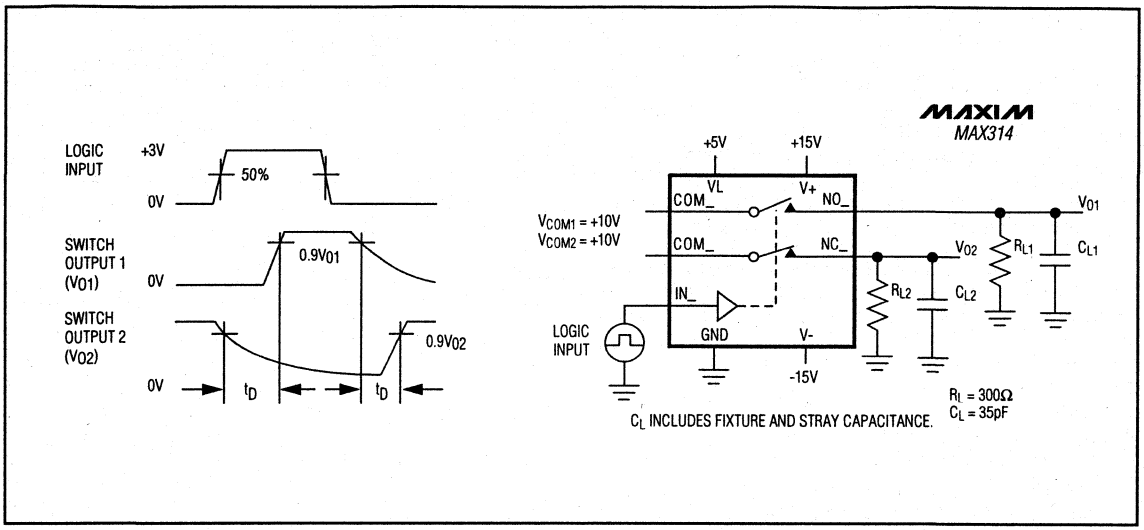


Figure 3. Break-Before-Make Test Circuit (MAX314 only)

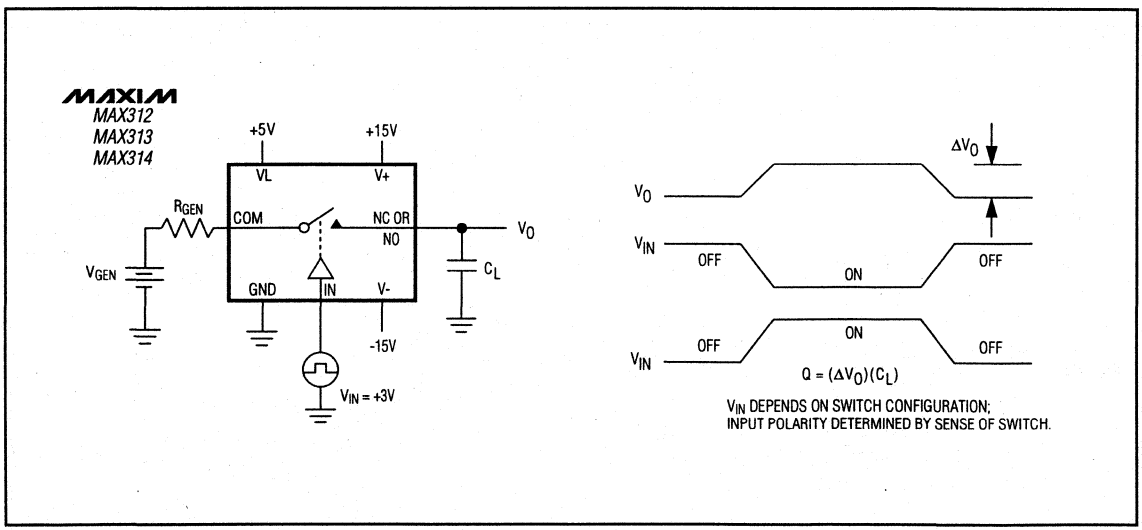


Figure 4. Charge Injection Test Circuit

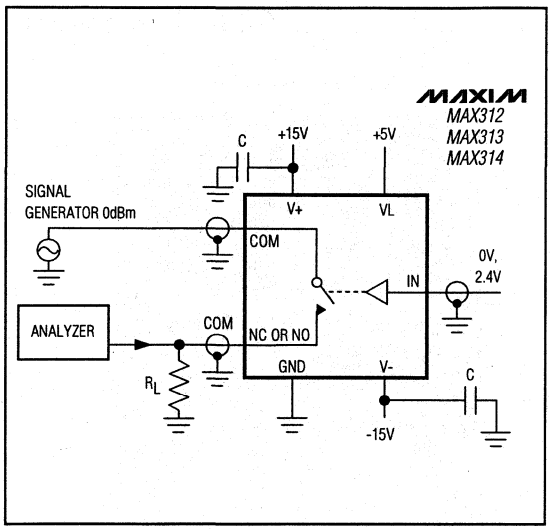


Figure 5. Off-Isolation Test Circuit

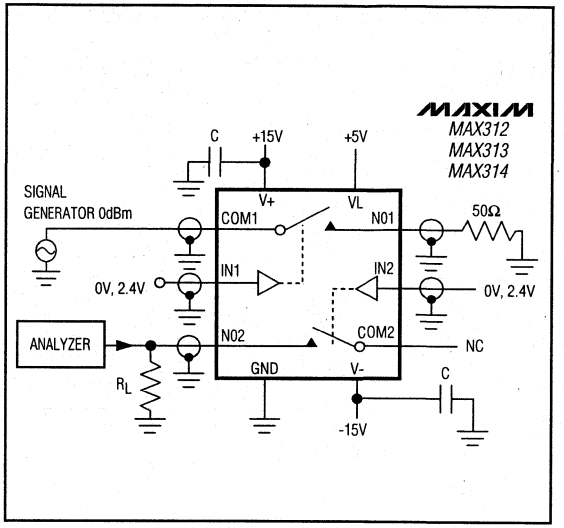


Figure 6. Crosstalk Test Circuit

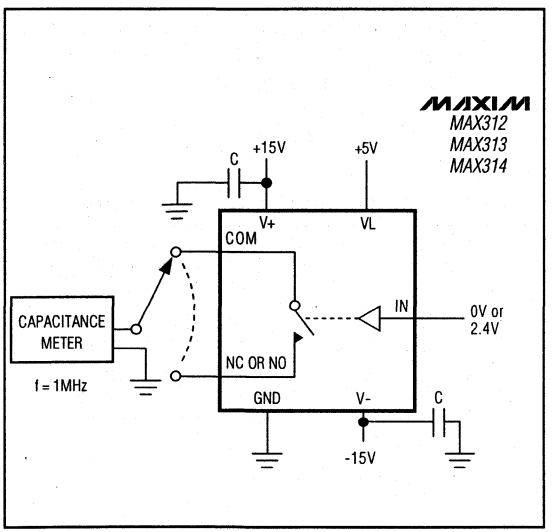


Figure 7. Channel-Off Capacitance Test Circuit

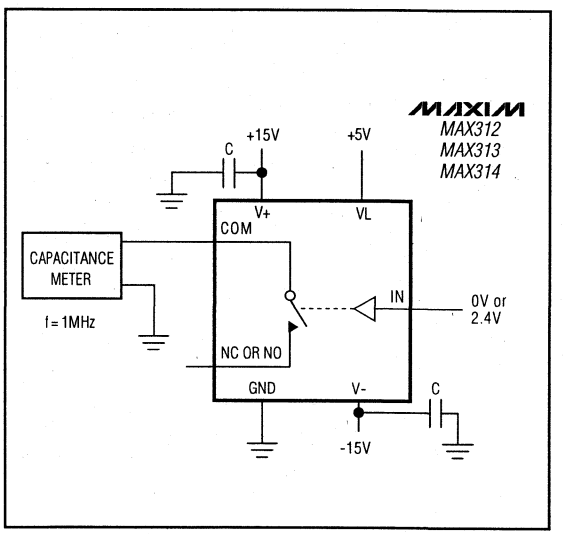


Figure 8. Channel-On Capacitance Test Circuit

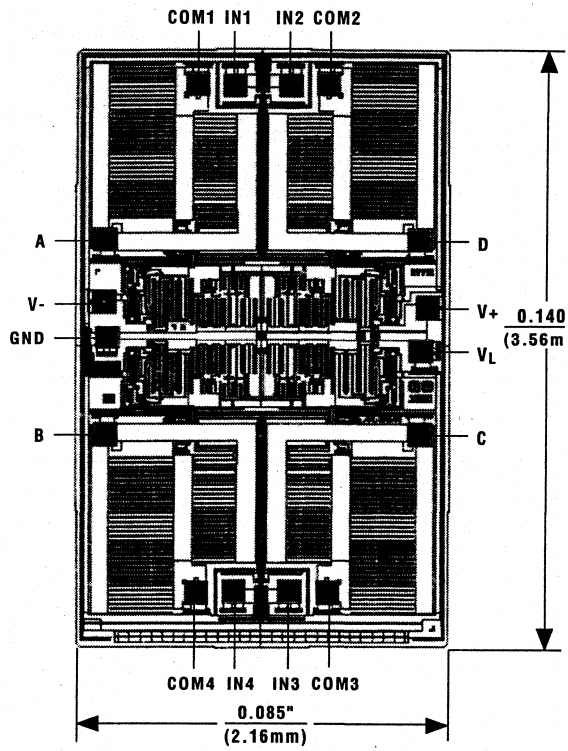
10Ω, Quad, SPST, CMOS Analog Switches

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX313CPE	0°C to +70°C	16 Plastic DIP
MAX313CSE	0°C to +70°C	16 Narrow SO
MAX313C/D	0°C to +70°C	Dice*
MAX313EPE	-40°C to +85°C	16 Plastic DIP
MAX313ESE	-40°C to +85°C	16 Narrow SO
MAX313MJE	-55°C to +125°C	16 CERDIP**
MAX314CPE	0°C to +70°C	16 Plastic DIP
MAX314CSE	0°C to +70°C	16 Narrow SO
MAX314C/D	0°C to +70°C	Dice*
MAX314EPE	-40°C to +85°C	16 Plastic DIP
MAX314ESE	-40°C to +85°C	16 Narrow SO
MAX314MJE	-55°C to +125°C	16 CERDIP**

** Contact factory for dice specifications.*
***Contact factory for availability.*

Chip Topography



MAX312		MAX313		MAX314	
PIN	NAME	PIN	NAME	PIN	NAME
A	NC1	A	NO1	A	NC1
B	NC4	B	NO4	B	NC4
C	NC3	C	NO3	C	NC3
D	NC2	D	NO2	D	NC2

TRANSISTOR COUNT: 100
SUBSTRATE CONNECTED TO V+

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

10/96

MAXIM

16-Channel/Dual 8-Channel, Low-Leakage, CMOS Analog Multiplexers

General Description

The MAX336/MAX337 are monolithic, CMOS analog multiplexers (muxes). The 16-channel MAX336 is designed to connect one of 16 inputs to a common output by control of a 4-bit binary address. The dual, 8-channel MAX337 is designed to connect one of eight inputs to a common output by control of a 3-bit binary address. Both devices can be used as either a mux or a demux. On-resistance is 400Ω max, and the devices conduct current equally well in both directions.

These muxes feature extremely low off leakages (less than 20pA at +25°C), and extremely low on-channel leakages (less than 50pA at +25°C). The new design offers guaranteed low charge injection (1.5pC typ) and electrostatic discharge (ESD) protection greater than 2000V, per method 3015.7. These improved muxes are pin-compatible upgrades for the industry-standard DG506A and DG507A.

The MAX336/MAX337 operate from a single +4.5V to +30V supply or from dual supplies of ±4.5V to ±20V. All control inputs (whether address or enable) are TTL compatible (+0.8V to +2.4V) over the full specified temperature range and over the ±4.5V to ±18V supply range. These parts are fabricated with Maxim's 44V silicon-gate process.

Features

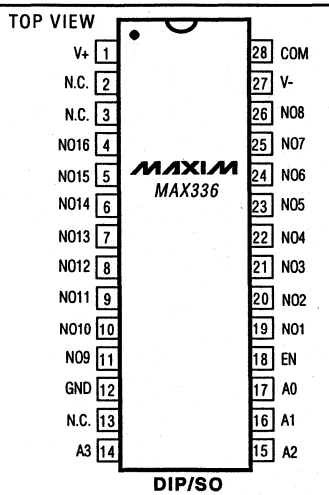
- ♦ **On-Resistance, <400Ω max**
- ♦ **Transition Time, <500ns**
- ♦ **On-Resistance Match, <10Ω**
- ♦ **NO-Off Leakage Current, <20pA at +25°C**
- ♦ **1.5pC Charge Injection**
- ♦ **Single-Supply Operation (+4.5V to +30V)**
  Bipolar-Supply Operation (±4.5V to ±20V)
- ♦ **Plug-In Upgrade for Industry-Standard DG506A/DG507A**
- ♦ **Rail-to-Rail Signal Handling**
- ♦ **TTL/CMOS-Logic Compatible**
- ♦ **>2000V ESD Protection, per Method 3015.7**

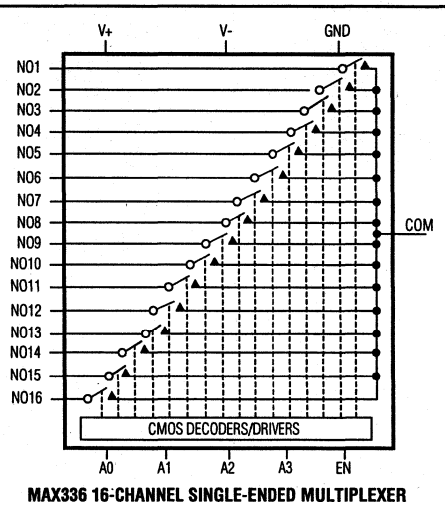
Applications

Data-Acquisition Systems	Sample-and-Hold Circuits
Test Equipment	Heads-Up Displays
Military Radios	Communications Systems
Guidance and Control Systems	
PBX, PABX	

Ordering Information appears on next page.

Pin Configurations/Functional Diagrams/Truth Tables





MAX336 16-CHANNEL SINGLE-ENDED MULTIPLEXER

MAX336					
A3	A2	A1	A0	EN	ON SWITCH
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

LOGIC "0" = $V_{AL} \leq 0.8V$, LOGIC "1" = $V_{AH} \geq 2.4V$

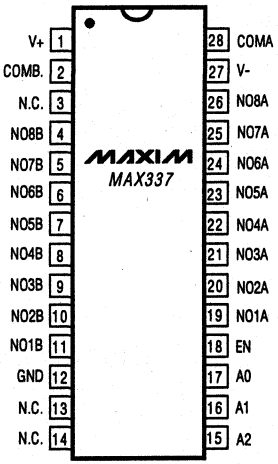
Continued on next page.

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

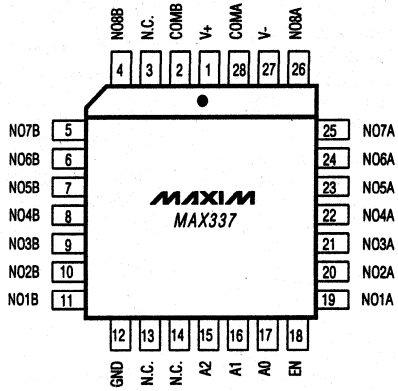
16-Channel/Dual 8-Channel, Low-Leakage, CMOS Analog Multiplexers

Pin Configurations/Functional Diagrams/Truth Tables (continued)

TOP VIEW



DIP/SO/SSOP

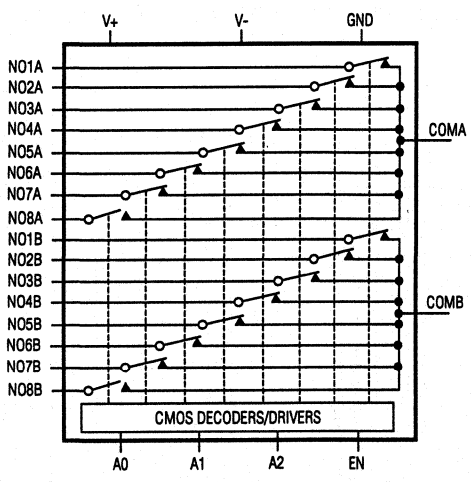


PLCC

N.C. = NO INTERNAL CONNECTION

MAX337				
A2	A1	A0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

LOGIC "0" = $V_{AL} \leq 0.8V$, LOGIC "1" = $V_{AH} \geq 2.4V$



MAX337 8-CHANNEL DIFFERENTIAL MULTIPLEXER

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX336CPI	0°C to +70°C	28 Plastic DIP
MAX336CWI	0°C to +70°C	28 Wide SO
MAX336CAI	0°C to +70°C	28 SSOP
MAX336CQI	0°C to +70°C	28 PLCC**
MAX336C/D	0°C to +70°C	Dice*
MAX336EPI	-40°C to +85°C	28 Plastic DIP
MAX336EWI	-40°C to +85°C	28 Wide SO
MAX336EQI	-40°C to +85°C	28 PLCC**
MAX336MJI	-55°C to +125°C	28 CERDIP**
MAX337CPI	0°C to +70°C	28 Plastic DIP
MAX337CWI	0°C to +70°C	28 Wide SO
MAX337CAI	0°C to +70°C	28 SSOP
MAX337CQI	0°C to +70°C	28 PLCC**
MAX337C/D	0°C to +70°C	Dice*
MAX337EPI	-40°C to +85°C	28 Plastic DIP
MAX337EWI	-40°C to +85°C	28 Wide SO
MAX337EQI	-40°C to +85°C	28 PLCC**
MAX337MJI	-55°C to +125°C	28 CERDIP**

** Contact factory for dice specifications.*
*** Contact factory for package availability.*

19-0451; Rev 0; 12/95

MAXIM

Serially Controlled, Low-Voltage, 8-Channel/Dual 4-Channel Multiplexers

General Description

The MAX349/MAX350 are 8-channel and dual 4-channel serially controlled multiplexers (muxes). These muxes conduct equally well in either direction. On-resistance (100Ω max) is matched between switches to 16Ω max and is flat (10Ω max) over the specified signal range.

These CMOS devices can operate continuously with dual power supplies ranging from ±2.7V to ±8V or a single supply between +2.7V and +16V. Each mux can handle rail-to-rail analog signals. The off leakage current is only 0.1nA at +25°C or 5nA at +85°C.

Upon power-up, all switches are off, and the internal shift registers are reset to zero.

The serial interface is compatible with SPI™/QSPI™ and Microwire™. Functioning as a shift register, it allows data (at DIN) to be clocked in synchronously with the rising edge of clock (SCLK). The shift register's output (DOUT) enables several MAX349s or MAX350s to be daisy chained.

All digital inputs have 0.8V or 2.4V logic thresholds, ensuring both TTL and CMOS-logic compatibility when using ±5V supplies or a single +5V supply.

Applications

Serial Data-Acquisition Systems
Avionics
Audio Signal Routing
Industrial and Process-Control Systems
ATE Equipment
Networking

Features

- **SPI™/QSPI™, Microwire™-Compatible Serial Interface**
- **8 Separately Controlled SPST Switches**
- **Single 8-to-1 Mux (MAX349)**
  Dual 4-to-1 Mux (MAX350)
- **100Ω Signal Paths with ±5V Supplies**
- **Rail-to-Rail Signal Handling**
- **Asynchronous $\overline{\text{RESET}}$ Input**
- **±2.7V to ±8V Dual Supplies**
  +2.7V to +16V Single Supply
- **>2kV ESD Protection per Method 3015.7**
- **TTL/CMOS-Compatible Inputs (with +5V or ±5V Supplies)**

Ordering Information

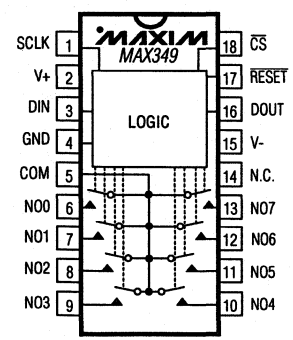
PART	TEMP. RANGE	PIN-PACKAGE
MAX349CPN	0°C to +70°C	18 Plastic DIP
MAX349CWN	0°C to +70°C	18 Wide SO
MAX349CAP	0°C to +70°C	20 SSOP
MAX349C/D	0°C to +70°C	Dice*

Ordering Information continued at end of data sheet.

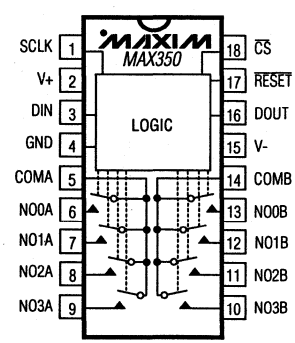
* *Contact factory for dice specifications.*

Pin Configurations/Functional Diagrams

TOP VIEW



DIP/SO



DIP/SO

N.C. = NOT INTERNALLY CONNECTED

Pin Configurations continued at end of data sheet.

SPI and QSPI are trademarks of Motorola, Inc. Microwire is a trademark of National Semiconductor Corp.

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Serially Controlled, Low-Voltage, 8-Channel/Dual 4-Channel Multiplexers

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to GND
- V+ ..... -0.3V, +17V
- V- ..... -17V, +0.3V
- V+ to V- ..... -0.3V, +17V
- SCLK, $\overline{CS}$, DIN, DOUT, $\overline{RESET}$ ..... -0.3V to (V+ + 0.3V)
- NO, COM ..... (V- - 2V) to (V+ + 2V)

Continuous Current into Any Terminal ..... ±30mA
Peak Current, NO or COM
- (pulsed at 1ms, 10% duty cycle) ..... ±100mA

Continuous Power Dissipation (T_A = +70°C)
- 18-Pin Plastic DIP (derate 11.11mW/°C above +70°C) ..889mW
- 18-Pin SO (derate 9.52mW/°C above +70°C) 762mW
- 20-Pin SSOP (derate 8.00mW/°C above +70°C) 640mW
- 18-Pin CERDIP (derate 10.53mW/°C above +70°C) 842mW

Operating Temperature Ranges
- MAX349C_ _, MAX350C_ _ ..... 0°C to +70°C
- MAX349E_ _ MAX350E_ _ ..... -40°C to +85°C
- MAX349M_ _ MAX350M_ _ ..... -55°C to +125°C

Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 1)	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	V_{COM}, V_{NO}			C, E, M	V-		V+	V
COM-NO On-Resistance	R_{ON}	V+ = 5V, V- = -5V, V_{COM} = ±3V, I_{NO} = 1mA		T_A = +25°C		60	100	Ω
				C, E, M			125	
COM-NO On-Resistance Match Between Channels (Note 2)	ΔR_{ON}	V+ = 5V, V- = -5V, V_{COM} = ±3V, I_{NO} = 1mA		T_A = +25°C			16	Ω
				C, E, M			20	
COM-NO On-Resistance Flatness (Note 2)	$R_{FLAT(ON)}$	V+ = 5V, V- = -5V, I_{NO} = 1mA, V_{COM} = -3V, 0V, 3V		T_A = +25°C			10	Ω
				C, E, M			15	
NO Off Leakage Current (Note 3)	$I_{NO(OFF)}$	V+ = 5.5V, V- = -5.5V, V_{COM} = -4.5V, V_{NO} = 4.5V		T_A = +25°C	-0.1	0.002	0.1	nA
				C, E	-5		5	
				M	-10		10	
		V+ = 5.5V, V- = -5.5V, V_{COM} = 4.5V, V_{NO} = -4.5V		T_A = +25°C	-0.1	0.002	0.1	
				C, E	-5		5	
				M	-10		10	
COM Off Leakage Current (Note 3)	$I_{COM(OFF)}$	V+ = 5.5V, V- = -5.5V, V_{COM} = ±4.5V, V_{NO} = ±4.5V	MAX349	T_A = +25°C	-0.1	0.002	0.1	nA
				C, E	-10		10	
				M	-100		100	
			MAX350	T_A = +25°C	-0.1	0.002	0.1	
				C, E	-5		5	
				M	-50		50	
		V+ = 5.5V, V- = -5.5V, V_{COM} = -4.5V, V_{NO} = 4.5V	MAX349	T_A = +25°C	-0.2	0.002	0.2	
				C, E	-10		10	
				M	-100		100	
			MAX350	T_A = +25°C	-0.2	0.002	0.2	
				C, E	-5		5	
				M	-50		50	

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 1)	MAX	UNITS
ANALOG SWITCH (continued)								
COM On Leakage Current (Note 3)	$I_{COM(ON)}$	V+ = 5.5V, V- = -5.5V, $V_{COM} = V_{NO}$ = ±4.5	MAX349	T_A = +25°C	-0.2	0.001	0.2	nA
				C, E	-10		10	
				M	-100		100	
			MAX350	T_A = +25°C	-0.2	0.02	0.2	
				C, E	-5		5	
				M	-50		50	
DIGITAL I/O								
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Voltage Logic Threshold High	V_{IH}			C, E, M	2.4			V
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Voltage Logic Threshold Low	V_{IL}			C, E, M			0.8	V
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Current Logic High or Low	I_{IH}, I_{IL}	V_{DIN}, V_{SCLK}, $V_{\overline{CS}}$ = 0.8V or 2.4V		C, E, M	-1	0.03	1	µA
DOUT Output Voltage Logic High	V_{DOUT}	I_{DOUT} = 0.8mA		C, E, M	2.8		V+	V
DOUT Output Voltage Logic Low	V_{DOUT}	I_{DOUT} = -1.6mA		C, E, M	0		0.4	V
SCLK Input Hysteresis	$SCLK_{HYST}$			C, E, M		100		mV
SWITCH DYNAMIC CHARACTERISTICS								
Turn-On Time	t_{ON}	From rising edge of $\overline{CS}$		T_A = +25°C		200	275	ns
				C, E, M			400	
Turn-Off Time	t_{OFF}	From rising edge of $\overline{CS}$		T_A = +25°C		90	150	ns
				C, E, M			300	
Break-Before-Make Delay	t_{BBM}	From rising edge of $\overline{CS}$		T_A = +25°C	5	40		ns
Charge Injection (Note 4)	V_{CTE}	C_L = 1nF, V_{NO} = 0V, R_S = 0Ω		T_A = +25°C		1	10	pC
NO Off Capacitance	$C_{NO(OFF)}$	V_{NO} = GND, f = 1MHz		T_A = +25°C		2		pF
COM Off Capacitance	$C_{COM(OFF)}$	V_{COM} = GND, f = 1MHz		T_A = +25°C		2		pF
Switch On Capacitance	$C_{(ON)}$	$V_{COM} = V_{NO}$ = GND, f = 1MHz		T_A = +25°C		8		pF
Off Isolation	V_{ISO}	R_L = 50Ω, C_L = 15pF, V_{NO} = $1V_{RMS}$, f = 100kHz		T_A = +25°C		> 90		dB
Channel-to-Channel Crosstalk	V_{CT}	R_L = 50Ω, C_L = 15pF, V_{NO} = $1V_{RMS}$, f = 100kHz		T_A = +25°C		< -90		dB
POWER SUPPLY								
Power-Supply Range	V+, V-			C, E, M	±3		±8	V
V+ Supply Current	I+	DIN = $\overline{CS}$ = SCLK = 0V or V+, $\overline{RESET}$ = 0V or V+		T_A = +25°C		7	20	µA
				C, E, M			30	
V- Supply Current	I-	DIN = $\overline{CS}$ = SCLK = 0V or V+, $\overline{RESET}$ = 0V or V+		T_A = +25°C	-1	0.1	1	µA
				C, E, M	-2		2	

Serially Controlled, Low-Voltage, 8-Channel/Dual 4-Channel Multiplexers

TIMING CHARACTERISTICS—Dual Supplies (Figure 1)

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 1)	MAX	UNITS
SERIAL DIGITAL INTERFACE							
SCLK Frequency	f_{SCLK}		C, E, M	0		2.1	MHz
Cycle Time	$t_{CH} + t_{CL}$		C, E, M	480			ns
$\overline{CS}$ Lead Time	t_{CSS}		C, E, M	240			ns
$\overline{CS}$ Lag Time	t_{CSH2}		C, E, M	240			ns
SCLK High Time	t_{CH}		C, E, M	190			ns
SCLK Low Time	t_{CL}		C, E, M	190			ns
Minimum Data Setup Time	t_{DS}		C, E, M		17	100	ns
Data Hold Time	t_{DH}		C, E, M	0	-17		ns
DIN Data Valid after Falling SCLK (Note 4)	t_{DO}	50% of SCLK to 10% of DOUT, C_L = 10pF	T_A = +25°C		85		ns
			C, E, M			400	
Rise Time of DOUT (Note 4)	t_{DR}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			100	ns
Allowable Rise Time at DIN, SCLK (Note 4)	t_{SCR}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			2	µs
Fall Time of DOUT (Note 4)	t_{DF}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			100	ns
Allowable Fall Time at DIN, SCLK (Note 4)	t_{SCF}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			2	µs
$\overline{RESET}$ Minimum Pulse Width	t_{RW}		T_A = +25°C		70		ns

Note 1: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Note 2: $\Delta R_{ON} = R_{ON(max)} - R_{ON(min)}$. On-resistance match between channels and on-resistance flatness are guaranteed only with specified voltages. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.

Note 3: Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at room temp.

Note 4: Guaranteed by design.

Note 5: Leakage testing at single supply is guaranteed by testing with dual supplies.

Note 6: See Figure 6. Off isolation = $20\log_{10} V_{COM}/V_{NO}$, V_{COM} = output. NO = input to off switch.

Note 7: Between any two switches. See Figure 3.

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +4.5V to +5.5V, V- = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 1)	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	V_{COM}, V_{NO}			C, E, M	V-		V+	V
COM-NO On-Resistance	R_{ON}	V+ = 5V, V_{COM} = 3.5V, I_{NO} = 1mA		T_A = +25°C		125	175	Ω
				C, E, M			225	
NO Off Leakage Current (Notes 4, 5)	$I_{NO(OFF)}$	V+ = 5.5V, V_{COM} = 4.5V, V_{NO} = 0V		T_A = +25°C	-0.1	0.002	0.1	nA
				C, E	-5		5	
				M	-10		10	
		V+ = 5.5V, V_{COM} = 0V, V_{NO} = 4.5V		T_A = +25°C	-0.1	0.002	0.1	
				C, E	-5		5	
				M	-10		10	
COM Off Leakage Current (Notes 4, 5)	$I_{COM(OFF)}$	V+ = 5.5V, V_{COM} = 4.5V, V_{NO} = 0V	MAX349	T_A = +25°C	-0.1	0.002	0.1	nA
				C, E	-10		10	
				M	-100		100	
			MAX350	T_A = +25°C	-0.1	0.002	0.1	
				C, E	-5		5	
				M	-50		50	
		V+ = 5.5V, V_{COM} = 0V, V_{NO} = 4.5V	MAX349	T_A = +25°C	-0.2	0.002	0.2	
				C, E	-10		10	
				M	-100		100	
			MAX350	T_A = +25°C	-0.2	0.002	0.2	
				C, E	-5		5	
				M	-50		50	
COM On Leakage Current (Notes 4, 5)	$I_{COM(ON)}$	V+ = 5.5V, V_{COM} = V_{NO} = ±4.5V	MAX349	T_A = +25°C	-0.2	0.01	0.2	nA
				C, E	-10		10	
				M	-100		100	
			MAX350	T_A = +25°C	-0.2	0.02	0.2	
				C, E	-5		5	
				M	-50		50	
DIGITAL I/O								
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Voltage Logic Threshold High	V_{IH}			C, E, M	2.4			V
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Voltage Logic Threshold Low	V_{IL}			C, E, M			0.8	V
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Current Logic High or Low	I_{IH}, I_{IL}	V_{DIN}, V_{SCLK}, $V_{\overline{CS}}$ = 0.8V or 2.4V		C, E, M	-1	0.03	1	µA
DOUT Output Voltage Logic High	V_{DOUT}	I_{DOUT} = 0.8mA		C, E, M	2.8		V+	V
DOUT Output Voltage Logic Low	V_{DOUT}	I_{DOUT} = -1.6mA		C, E, M	0		0.4	V
SCLK Input Hysteresis	$SCLK_{HYST}$			C, E, M		100		mV
POWER SUPPLY								
V+ Supply Current	I+	DIN = $\overline{CS}$ = SCLK = 0V or V+, $\overline{RESET}$ = 0V or V+		T_A = +25°C		7	20	µA
				C, E, M			30	

Serially Controlled, Low-Voltage, 8-Channel/Dual 4-Channel Multiplexers

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V+ = +4.5V to +5.5V, V- = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 1)	MAX	UNITS
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	From rising edge of $\overline{CS}$	T_A = +25°C		160	400	ns
			C, E, M			500	
Turn-Off Time	t_{OFF}	From rising edge of $\overline{CS}$	T_A = +25°C		60	200	ns
			C, E, M			300	
Break-Before-Make Delay	t_{BBM}	From rising edge of $\overline{CS}$	T_A = +25°C		15		ns
Charge Injection (Note 4)	V_{CTE}	C_L = 1nF, V_{NO} = 0V, R_S = 0Ω	T_A = +25°C		1	10	pC
Off Isolation (Note 6)	V_{ISO}	R_L = 50Ω, C_L = 15pF, V_{NO} = $1V_{RMS}$, f = 100kHz	T_A = +25°C		> 90		dB
Channel-to-Channel Crosstalk (Note 7)	V_{CT}	R_L = 50Ω, C_L = 15pF, V_{NO} = $1V_{RMS}$, f = 100kHz	T_A = +25°C		< -90		dB

TIMING CHARACTERISTICS—Single +5V Supply (Figure 1)

(V+ = +4.5V to +5.5V, V- = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 1)	MAX	UNITS
SERIAL DIGITAL INTERFACE							
SCLK Frequency	f_{SCLK}		C, E, M	0		2.1	MHz
Cycle Time (Note 4)	$t_{CH} + t_{CL}$		C, E, M	480			ns
$\overline{CS}$ Lead Time (Note 4)	t_{CSS}		C, E, M	240			ns
$\overline{CS}$ Lag Time (Note 4)	t_{CSH2}		C, E, M	240			ns
SCLK High Time (Note 4)	t_{CH}		C, E, M	190			ns
SCLK Low Time (Note 4)	t_{CL}		C, E, M	190			ns
Minimum Data Setup Time (Note 4)	t_{DS}		C, E, M		17	100	ns
Data Hold Time (Note 4)	t_{DH}		C, E, M		-17		ns
DIN Data Valid after Falling SCLK (Note 4)	t_{DO}	50% of SCLK to 10% of DOUT, C_L = 10pF	T_A = +25°C		85		ns
			C, E, M			400	
Rise Time of DOUT (Note 4)	t_{DR}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			100	ns
Allowable Rise Time at DIN, SCLK (Note 4)	t_{SCR}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			2	µs
Fall Time of DOUT (Note 4)	t_{DF}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			100	ns
Allowable Fall Time at DIN, SCLK (Note 4)	t_{SCF}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			2	µs
$\overline{RESET}$ Minimum Pulse Width	t_{RW}		T_A = +25°C		70		ns

Note 1: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Note 2: $\Delta R_{ON} = R_{ON(max)} - R_{ON(min)}$. On-resistance match between channels and on-resistance flatness are guaranteed only with specified voltages. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.

Note 3: Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at room temp.

Note 4: Guaranteed by design.

Note 5: Leakage testing at single supply is guaranteed by testing with dual supplies.

Note 6: See Figure 6. Off isolation = $20\log_{10} V_{COM}/V_{NO}$, V_{COM} = output. NO = input to off switch.

Note 7: Between any two switches. See Figure 3.

Serially Controlled, Low-Voltage, 8-Channel/Dual 4-Channel Multiplexers

ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +3.0V to +3.6V, V- = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 1)	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	V_{COM}, V_{NO}			C, E, M	V-		V+	V
COM-NO On-Resistance	R_{ON}	V+ = 3.0V, V_{COM} = 1.5V, I_{NO} = 1mA		T_A = +25°C		270	500	Ω
				C, E, M			600	
COM Off Leakage Current (Notes 4, 5)	$I_{COM(OFF)}$	V+ = 3.6V, V_{COM} = 3V, V_{NO} = 0V	MAX349	T_A = +25°C	-0.1	0.002	0.1	nA
				C, E	-10		10	
				M	-100		100	
			MAX350	T_A = +25°C	-0.1	0.002	0.1	
				C, E	-5		5	
				M	-50		50	
		V+ = 3.6V, V_{COM} = 0V, V_{NO} = 3V	MAX349	T_A = +25°C	-0.2	0.002	0.2	
				C, E	-10		10	
				M	-100		100	
			MAX350	T_A = +25°C	-0.2	0.002	0.2	
				C, E	-5		5	
				M	-50		50	
COM On Leakage Current (Notes 4, 5)	$I_{COM(ON)}$	V+ = 3.6V, V_{COM} = V_{NO} = 3V	MAX349	T_A = +25°C	-0.2	0.01	0.2	nA
				C, E	-10		10	
				M	-100		100	
			MAX350	T_A = +25°C	-0.2	0.02	0.2	
				C, E	-5		5	
				M	-50		50	
DIGITAL I/O								
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Voltage Logic Threshold High	V_{IH}			C, E	2.4			V
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Voltage Logic Threshold Low	V_{IL}			C, E			0.8	V
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Current Logic High or Low	I_{IH}, I_{IL}	V_{DIN}, V_{SCLK}, $V_{\overline{CS}}$ = 0.8V or 2.4V		C, E	-1	0.03	1	µA
DOUT Output Voltage Logic High	V_{DOUT}	I_{DOUT} = 0.1mA		C, E, M	2.8		V+	V
DOUT Output Voltage Logic Low	V_{DOUT}	I_{DOUT} = -1.6mA		C, E, M	0		0.4	V
SCLK Input Hysteresis	$SCLK_{HYST}$			C, E, M		100		mV
POWER SUPPLY								
V+ Supply Current	I+	DIN = $\overline{CS}$ = SCLK = 0V or V+, $\overline{RESET}$ = 0V or 5V		T_A = +25°C		6	20	µA
				C, E, M			30	

ELECTRICAL CHARACTERISTICS—Single +3V Supply (continued)

(V+ = +3.0V to +3.6V, V- = 0V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 1)	MAX	UNITS
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time (Note 4)	t_{ON}	From rising edge of $\overline{CS}$	T_A = +25°C		275	600	ns
			C, E, M			700	
Turn-Off Time (Note 4)	t_{OFF}	From rising edge of $\overline{CS}$	T_A = +25°C		120	300	ns
			C, E, M			400	
Break-Before-Make Delay (Note 4)	t_{BBM}	From rising edge of $\overline{CS}$	T_A = +25°C	5	15		ns
Charge Injection (Note 4)	V_{CTE}	C_L = 1nF, V_{NO} = 0V, R_S = 0Ω	T_A = +25°C		1	10	pC
Off Isolation (Note 6)	V_{ISO}	R_L = 50Ω, C_L = 15pF, V_{NO} = $1V_{RMS}$, f = 100kHz	T_A = +25°C		> 90		dB
Channel-to-Channel Crosstalk (Note 7)	V_{CT}	R_L = 50Ω, C_L = 15pF, V_{NO} = $1V_{RMS}$, f = 100kHz	T_A = +25°C		< –90		dB

Serially Controlled, Low-Voltage, 8-Channel/Dual 4-Channel Multiplexers

TIMING CHARACTERISTICS—Single +3V Supply (Figure 1)

(V+ = +3.0V to +3.6V, V- = 0V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 1)	MAX	UNITS
SERIAL DIGITAL INTERFACE							
SCLK Frequency	f_{SCLK}		C, E, M	0		2.1	MHz
Cycle Time (Note 4)	$t_{CH} + t_{CL}$		C, E, M	480			ns
$\overline{CS}$ Lead Time (Note 4)	t_{CSS}		C, E, M	240			ns
$\overline{CS}$ Lag Time (Note 4)	t_{CSH2}		C, E, M	240			ns
SCLK High Time (Note 4)	t_{CH}		C, E, M	190			ns
SCLK Low Time (Note 4)	t_{CL}		C, E, M	190			ns
Minimum Data Setup Time (Note 4)	t_{DS}		C, E, M		38	120	ns
Data Hold Time (Note 4)	t_{DH}		C, E, M		-38		ns
DIN Data Valid after Falling SCLK (Note 4)	t_{DO}	50% of SCLK to 10% of DOUT, C_L = 10pF	T_A = +25°C		150		ns
			C, E, M			400	
Rise Time of DOUT (Note 4)	t_{DR}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			100	ns
Allowable Rise Time at DIN, SCLK (Note 4)	t_{SCR}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			2	µs
Fall Time of DOUT (Note 4)	t_{DF}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			100	ns
Allowable Fall Time at DIN, SCLK (Note 4)	t_{SCF}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			2	µs
$\overline{RESET}$ Minimum Pulse Width (Note 4)	t_{RW}		T_A = +25°C		105		ns

Note 1: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Note 2: $\Delta R_{ON} = R_{ON(max)} - R_{ON(min)}$. On-resistance match between channels and on-resistance flatness are guaranteed only with specified voltages. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.

Note 3: Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at room temp.

Note 4: Guaranteed by design.

Note 5: Leakage testing at single supply is guaranteed by testing with dual supplies.

Note 6: See Figure 6. Off isolation = $20\log_{10} V_{COM}/V_{NO}$, V_{COM} = output. NO = input to off switch.

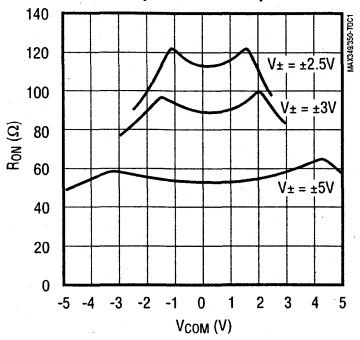
Note 7: Between any two switches. See Figure 3.

Serially Controlled, Low-Voltage, 8-Channel/Dual 4-Channel Multiplexers

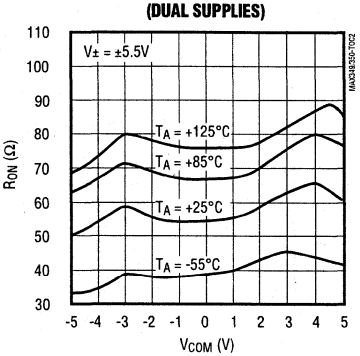
Typical Operating Characteristics

(V+ = +5V, V- = -5V, GND = 0V, T_A = +25°C, unless otherwise noted.)

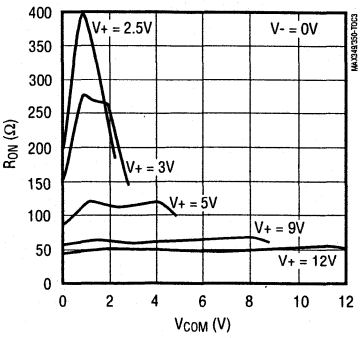
ON-RESISTANCE vs. VCOM (DUAL SUPPLIES)



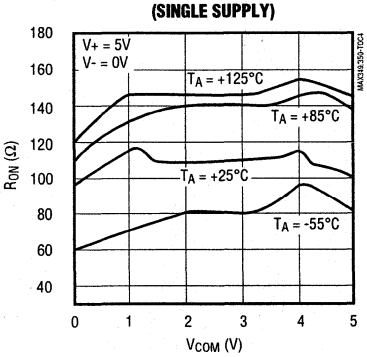
ON-RESISTANCE vs. VCOM AND TEMPERATURE (DUAL SUPPLIES)



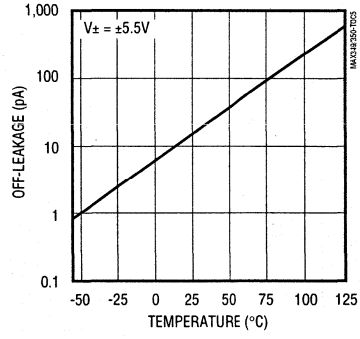
ON-RESISTANCE vs. VCOM (SINGLE SUPPLY)



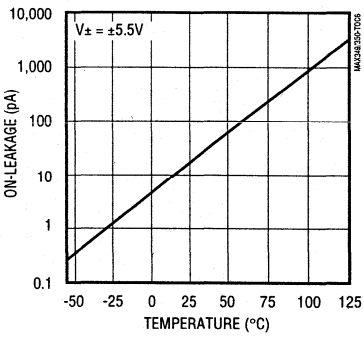
ON-RESISTANCE vs. VCOM AND TEMPERATURE (SINGLE SUPPLY)



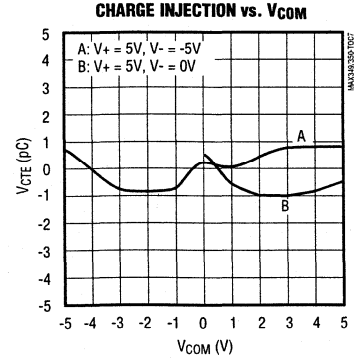
OFF-LEAKAGE vs. TEMPERATURE



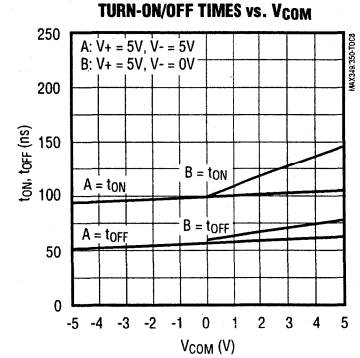
ON-LEAKAGE vs. TEMPERATURE



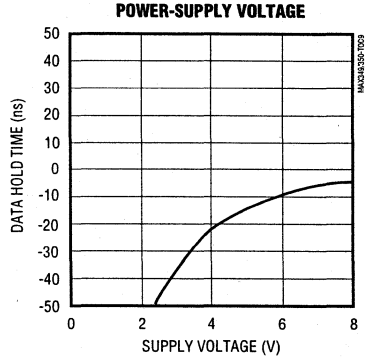
CHARGE INJECTION vs. VCOM



TURN-ON/OFF TIMES vs. VCOM



DATA HOLD TIME vs. POWER-SUPPLY VOLTAGE

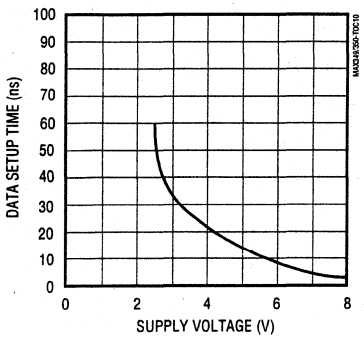


Serially Controlled, Low-Voltage, 8-Channel/Dual 4-Channel Multiplexers

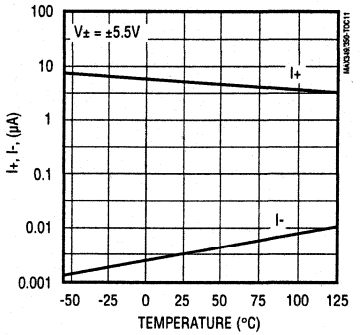
Typical Operating Characteristics (continued)

(V+ = +5V, V- = -5V, GND = 0V, T_A = +25°C, unless otherwise noted.)

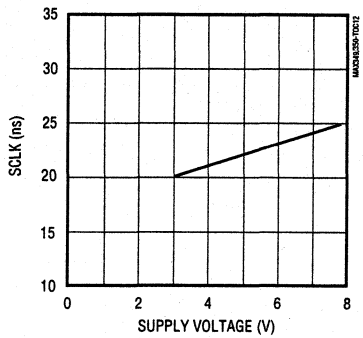
DATA SETUP TIME vs. POSITIVE SUPPLY VOLTAGE



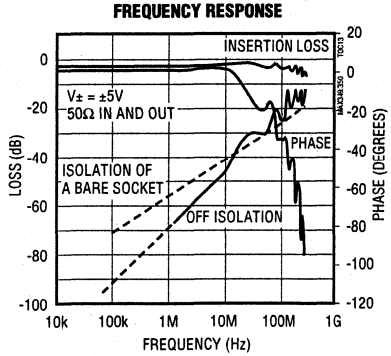
POWER-SUPPLY CURRENT vs. TEMPERATURE



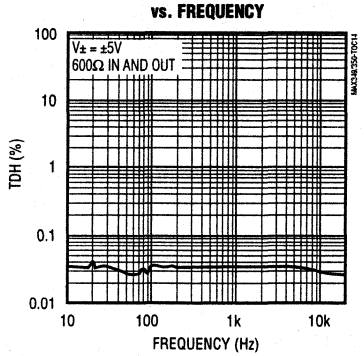
MINIMUM SCLK PULSE WIDTH vs. POSITIVE SUPPLY VOLTAGE



FREQUENCY RESPONSE



TOTAL HARMONIC DISTORTION vs. FREQUENCY



Pin Description

PIN				NAME	FUNCTION
MAX349		MAX350			
DIP/SO	SSOP	DIP/SO	SSOP		
1	1	1	1	SCLK	Serial Clock Digital Input
2	2	2	2	V+	Positive Analog Supply Voltage Input
3	3	3	3	DIN	Serial Data Digital Input
4	4	4	4	GND	Ground. Connect to digital ground. (Analog signals have no ground reference; they are limited to V+ and V-.)
5	5	—	—	COM	Common Analog Switch (mux output)
6–13	6–9, 11–14	—	—	NO0–NO7	Normally Open Analog Switch Inputs 0–7
—	—	5	5	COMA	Common Analog Switch "A" (mux output)
—	—	6–9	6–9	NO0A–NO3A	Normally Open Analog Switch "A" Inputs 0–3
—	—	10–13	11–14	NO3B–NO0B	Normally Open Analog Switch "B" Inputs 0–3
—	—	14	15	COMB	Common Analog Switch "B" (mux output)
14	10, 15, 16	—	10, 16	N.C.	No Connect, not internally connected.
15	17	15	17	V-	Negative Analog Supply Voltage Input. Connect to GND for single-supply operation.
16	18	16	18	DOUT	Serial Data Digital Output. Output high is V+.
17	19	17	19	$\overline{RESET}$	RESET Input. Connect to logic high (or V+) for normal operation. Drive low to set all switches off and set internal shift registers to 0.
18	20	18	20	$\overline{CS}$	Chip-Select Digital Input (Figure 1)

Note: NO and COM pins are identical and interchangeable. Either may be considered as an input or an output; signals pass equally well in either direction.

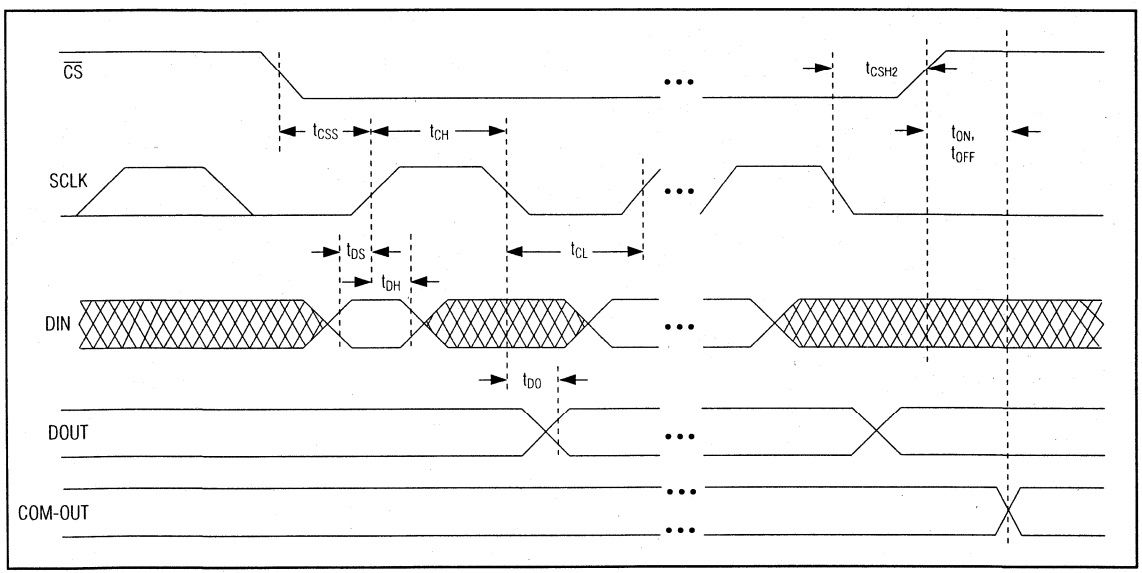


Figure 1. Timing Diagram

Serially Controlled, Low-Voltage, 8-Channel/Dual 4-Channel Multiplexers

Detailed Description

Basic Operation

The MAX349/MAX350 are 8-channel and dual 4-channel, serially controlled multiplexers (muxes). These muxes are unusual in that any, all, or none of the input channels can be directed to the output. All switches are bidirectional, so inputs and outputs are interchangeable. When multiple inputs are connected to an output, they are also connected to one another, separated from each other only by the on-resistance of two switches. Both parts require eight bits of serial data to set all eight switches.

Serial Digital Interface

The MAX349/MAX350 interface can be thought of as an 8-bit shift register controlled by $\overline{CS}$ (Figure 2). While $\overline{CS}$ is low, input data appearing at DIN is clocked into the shift register synchronously with SCLK's rising edge. The input is an 8-bit word, each bit controlling one of the eight switches (Tables 1 and 2). DOUT is the output of the shift register, with data appearing synchronously with SCLK's falling edge. Data at DOUT is simply the input data delayed by eight clock cycles.

When shifting the input data, D7 is the first bit in and out of the shift register. While shifting data, the switches remain in their previous configuration. When the eight bits of data have been shifted in, $\overline{CS}$ is driven high. This updates the new switch configuration and inhibits further data from entering the shift register. Transitions at DIN and SCLK have no effect when CS is high, and DOUT holds the first input bit (D7) at its output.

More or fewer than eight clock cycles can be entered during the $\overline{CS}$ low period. When this happens, the shift register contains only the last eight serial data bits, regardless of when they were entered. On the rising edge of $\overline{CS}$, all switches are set to the corresponding states.

The MAX349/MAX350 three-wire serial interface is compatible with SPI, QSPI, and Microwire standards. If interfacing with a Motorola processor serial interface, set CPOL = 0. The MAX349/MAX350 are considered to be slave devices (Figures 2 and 3). At power-up, the shift register contains all zeros, and all switches are off.

The latch that drives the analog switch is updated on the rising edge of $\overline{CS}$, regardless of SCLK's state. This meets all SPI and QSPI requirements.

Daisy Chaining

For a simple interface using several MAX349s and MAX350s, "daisy chain" the shift registers as shown in Figure 5. The $\overline{CS}$ pins of all devices are connected, and a stream of data is shifted through the MAX349s or MAX350s in series. When $\overline{CS}$ is brought high, all switches are updated simultaneously. Additional shift registers may be included anywhere in series with the MAX349/MAX350 data chain. Note that the DOUT high level is V+, which may not be compatible with TTL/CMOS devices if V+ differs from the logic supply for these other devices.

Addressable Serial Interface

When several serial devices are configured as slaves, addressable by the processor, DIN pins of each decode logic individually control $\overline{CS}$ of each slave device. When a slave is selected, its $\overline{CS}$ pin is driven low, data is shifted in, and $\overline{CS}$ is driven high to latch the data. Typically, only one slave is addressed at a time. DOUT is not used.

Applications Information

8x1 Multiplexer

The MAX349 can be programmed normally, with only one channel selected for every eight clock pulses, or it can be programmed in a fast mode, where channel changing occurs on each clock pulse.

In fast mode, select the channels by sending a single high pulse (corresponding to the selected channel) at DIN, and a corresponding $\overline{CS}$ low pulse for every eight clock pulses. As SCLK clocks this through the register, each switch sequences one channel at a time, starting with Channel 0.

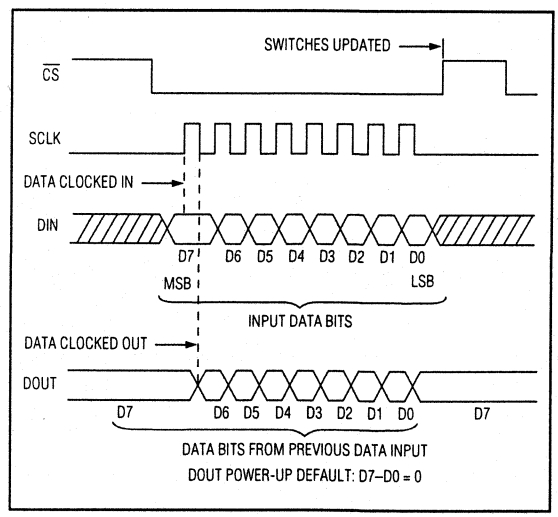


Figure 2. Three-Wire Interface Timing

Table 1. MAX349 Serial-Interface Switch Programming

$\overline{RESET}$	DATA BITS								MAX349 FUNCTION
	D7	D6	D5	D4	D3	D2	D1	D0	
0	X	X	X	X	X	X	X	X	All switches open, D7–D0 = 0
1	0	0	0	0	0	0	0	0	All switches open, D7–D0 = 0
1	1	1	1	1	1	1	1	1	All switches closed to COM, D7–D0 = 1
1	**0**	X	X	X	X	X	X	X	Switch 7 open (off)
1	**1**	X	X	X	X	X	X	X	Switch 7 closed to COM
1	X	**0**	X	X	X	X	X	X	Switch 6 open (off)
1	X	**1**	X	X	X	X	X	X	Switch 6 closed to COM
1	X	X	**0**	X	X	X	X	X	Switch 5 open (off)
1	X	X	**1**	X	X	X	X	X	Switch 5 closed to COM
1	X	X	X	**0**	X	X	X	X	Switch 4 open (off)
1	X	X	X	**1**	X	X	X	X	Switch 4 closed to COM
1	X	X	X	X	**0**	X	X	X	Switch 3 open (off)
1	X	X	X	X	**1**	X	X	X	Switch 3 closed to COM
1	X	X	X	X	X	**0**	X	X	Switch 2 open (off)
1	X	X	X	X	X	**1**	X	X	Switch 2 closed to COM
1	X	X	X	X	X	X	**0**	X	Switch 1 open (off)
1	X	X	X	X	X	X	**1**	X	Switch 1 closed to COM
1	X	X	X	X	X	X	X	**0**	Switch 0 open (off)
1	X	X	X	X	X	X	X	**1**	Switch 0 closed to COM

$\overline{RESET}$	DATA BITS								MAX350 FUNCTION
	D7	D6	D5	D4	D3	D2	D1	D0	
0	X	X	X	X	X	X	X	X	All switches open, D7–D0 = 0
1	0	0	0	0	0	0	0	0	All switches open, D7–D0 = 0
1	1	1	1	1	1	1	1	1	All "A" switches closed to COMA; All "B" switches closed to COMB, D7–D0 = 1
1	**0**	X	X	X	X	X	X	X	Switch 3A open (off)
1	**1**	X	X	X	X	X	X	X	Switch 3A closed to COMA
1	X	**0**	X	X	X	X	X	X	Switch 2A open (off)
1	X	**1**	X	X	X	X	X	X	Switch 2A closed to COMA
1	X	X	**0**	X	X	X	X	X	Switch 1A open (off)
1	X	X	**1**	X	X	X	X	X	Switch 1A closed to COMA
1	X	X	X	**0**	X	X	X	X	Switch 0A open (off)
1	X	X	X	**1**	X	X	X	X	Switch 0A closed to COMA
1	X	X	X	X	**0**	X	X	X	Switch 3B open (off)
1	X	X	X	X	**1**	X	X	X	Switch 3B closed to COMB
1	X	X	X	X	X	**0**	X	X	Switch 2B open (off)
1	X	X	X	X	X	**1**	X	X	Switch 2B closed to COMB
1	X	X	X	X	X	X	**0**	X	Switch 1B open (off)
1	X	X	X	X	X	X	**1**	X	Switch 1B closed to COMB
1	X	X	X	X	X	X	X	**0**	Switch 0B open (off)
1	X	X	X	X	X	X	X	**1**	Switch 0B closed to COMB

X = Don't care. Data bit D7 is first bit in; data bit D0 is last in.

Serially Controlled, Low-Voltage, 8-Channel/Dual 4-Channel Multiplexers

Dual, Differential 4-Channel Multiplexer

The MAX350 can be programmed normally, with only one differential channel selected for every eight clock pulses, or it can be programmed in a fast mode, where channel changing occurs on each clock pulse.

In fast mode, select the channels by sending two high pulses, spaced four clock pulses apart (corresponding to the two selected channels) at DIN, and a corresponding $\overline{CS}$ low pulse for each of the first eight clock pulses. As SCLK clocks this through the register, each switch sequences one differential channel at a time, starting with channel 0. Repeat this process for subsequent channel sequencing after the first eight bits have been sent. For even faster channel sequencing, send only one DIN high pulse and one $\overline{CS}$ low pulse for every four clock pulses.

Reset Function

$\overline{RESET}$ is the internal reset pin. It is usually connected to a logic signal or V+. Drive $\overline{RESET}$ low to open all switches and set the contents of the internal shift register to zero simultaneously. When $\overline{RESET}$ is high, the part functions normally and DOUT is sourced from V+. $\overline{RESET}$ must not be driven beyond V+ or GND.

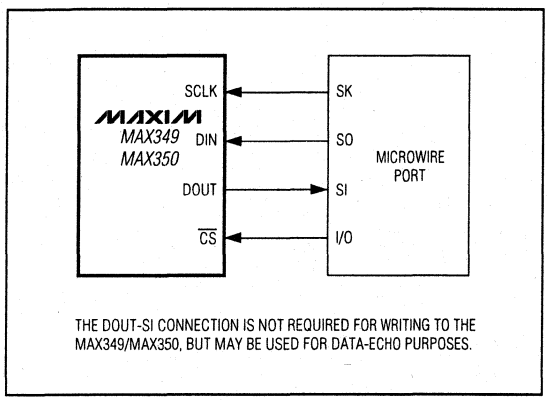


Figure 3. Connections for Microwire

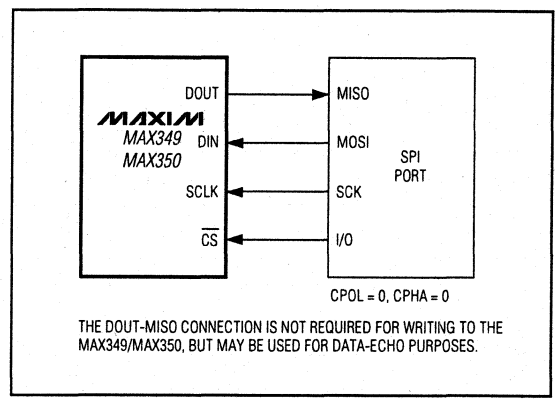


Figure 4. Connections for SPI and QSPI

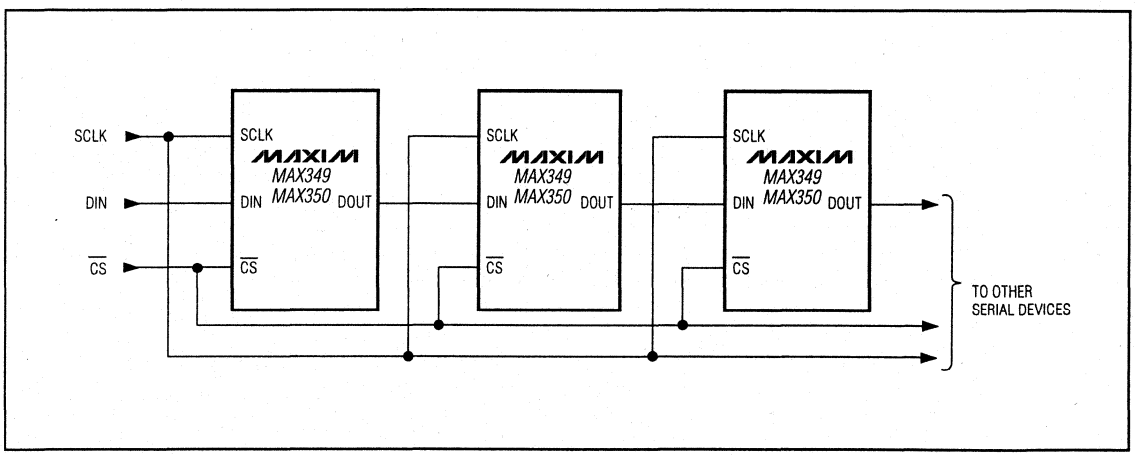


Figure 5. Daisy-Chained Connection

Serially Controlled, Low-Voltage, 8-Channel/Dual 4-Channel Multiplexers

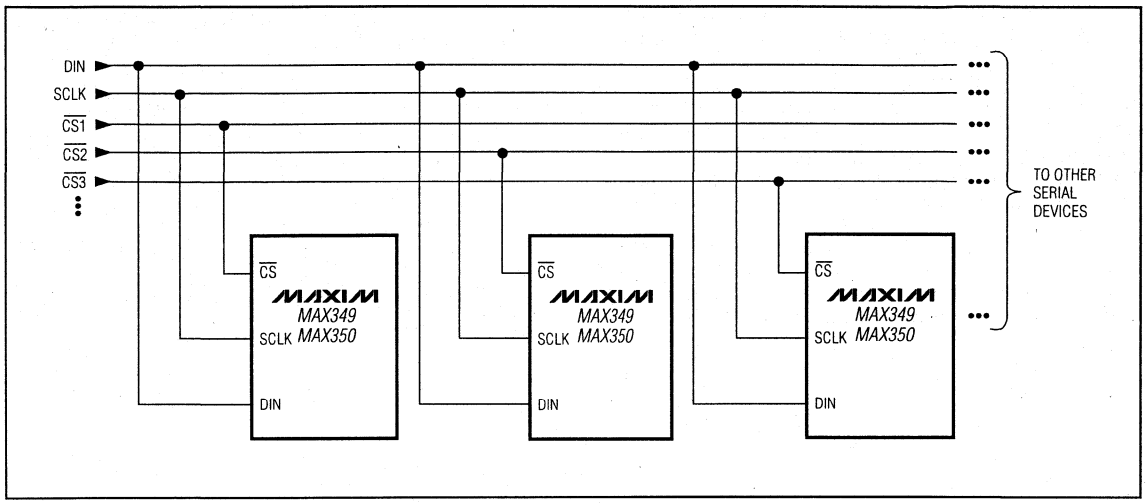


Figure 6. Addressable Serial Interface

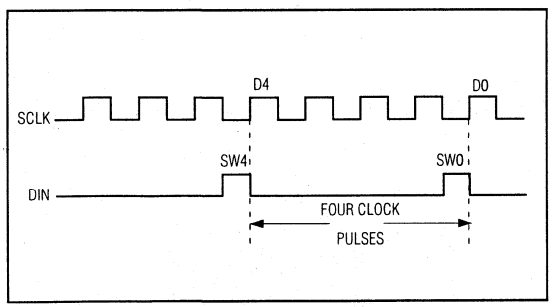


Figure 7. Differential Multiplexer Input Control

Power-Supply Considerations

Overview

The MAX349/MAX350 construction is typical of most CMOS analog switches. It has three supply pins: V+, V- and GND. V+ and V- are used to drive the internal CMOS switches, and they set the limits of the analog voltage on any switch. Reverse ESD-protection diodes are internally connected between each analog signal pin and both V+ and V-. If any analog signal exceeds V+ or V-, one of these diodes will conduct. During normal operation, these (and other) reverse-biased ESD diodes leak, forming the only current drawn from V+ or V-.

Virtually all the analog leakage current is through the ESD diodes. Although the ESD diodes on a given signal pin are identical, and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or V- and the analog signal. This means their leakages vary as the signal varies. The *difference* in the two diode leakages to the V+ and V- pins constitutes the analog signal-path leakage current. All analog leakage current flows to the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of either the same or opposite polarity.

There is no connection between the analog signal paths and GND.

V+ and GND power the internal logic and logic-level translators, and set both the input and output logic limits. The logic-level translators convert the logic levels to switched V+ and V- signals to drive the analog signal gates. This drive signal is the only connection between the logic supplies (and signals) and the analog supplies. V+ and V- have ESD-protection diodes to GND. The logic-level inputs and output have ESD protection to V+ and to GND.

The logic-level thresholds are CMOS and TTL compatible when V+ is +5V. As V+ rises, the threshold increases slightly. Therefore, when V+ reaches +12V, the threshold is about 3.1V; above the TTL-guaranteed high-level minimum of 2.8V, but still compatible with CMOS outputs.

Serially Controlled, Low-Voltage, 8-Channel/Dual 4-Channel Multiplexers

Bipolar Supplies

The MAX349/MAX350 operate with bipolar supplies from ±3.0V and ±8V. The V+ and V- supplies need not be symmetrical, but their sum cannot exceed the absolute maximum rating of 17V. **Do not connect the MAX349/MAX350 V+ to +3V and connect the logic-level pins to TTL logic-level signals. This exceeds the absolute maximum ratings and can damage the part and/or external circuits.**

Single Supply

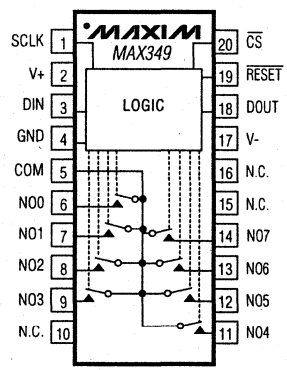
The MAX349/MAX350 operate from single supplies between +3V and +16V when V- is connected to GND. All of the bipolar precautions must be observed.

High-Frequency Performance

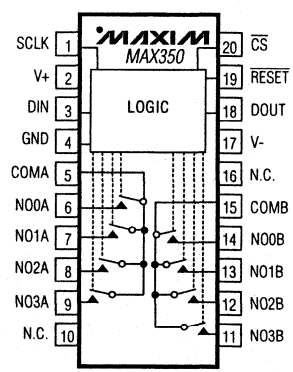
In 50Ω systems, signal response is reasonably flat up to 50MHz (see *Typical Operating Characteristics).* Above 20MHz, the on response has several minor peaks that are highly layout dependent. The problem is not turning the switch on, but turning it off. The off-state switch acts like a capacitor and passes higher frequencies with less attenuation. At 10MHz, off isolation is about -45dB in 50Ω systems, becoming worse (approximately 20dB per decade) as frequency increases. Higher circuit impedances also make off isolation worse. Adjacent channel attenuation is about 3dB above that of a bare IC socket, and is entirely due to capacitive coupling.

Pin Configurations/Functional Diagrams (continued)

TOP VIEW



SSOP



SSOP

N.C. = NOT INTERNALLY CONNECTED

Serially Controlled, Low-Voltage, 8-Channel/Dual 4-Channel Multiplexers

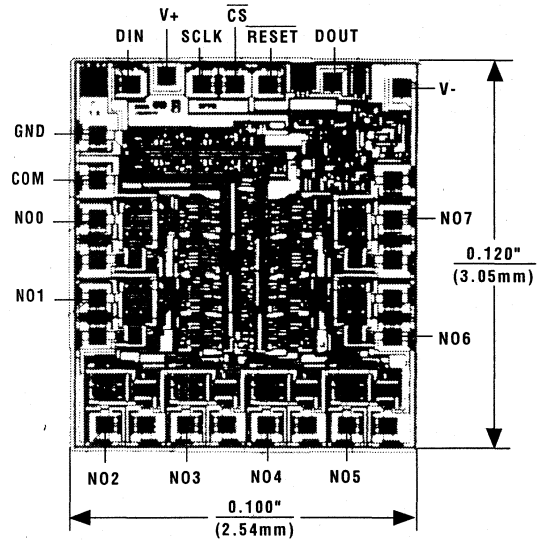
_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX349EPN	-40°C to +85°C	18 Plastic DIP
MAX349EWN	-40°C to +85°C	18 Wide SO
MAX349EAP	-40°C to +85°C	20 SSOP
MAX349MJN	-55°C to +125°C	18 CERDIP**
MAX350CPN	0°C to +70°C	18 Plastic DIP
MAX350CWN	0°C to +70°C	18 Wide SO
MAX350CAP	0°C to +70°C	20 SSOP
MAX350C/D	0°C to +70°C	Dice*
MAX350EPN	-40°C to +85°C	18 Plastic DIP
MAX350EWN	-40°C to +85°C	18 Wide SO
MAX350EAP	-40°C to +85°C	20 SSOP
MAX350MJN	-55°C to +125°C	18 CERDIP**

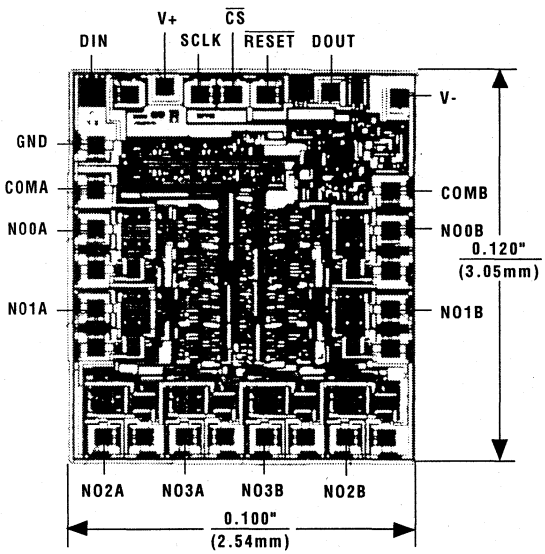
* *Contact factory for dice specifications.*
** *Contact factory for availability.*

Chip Topographies

MAX349



MAX350



TRANSISTOR COUNT: 500
SUBSTRATE CONNECTED TO V+.

19-0448; Rev 0; 11/95

MAXIM

Serially Controlled, Low-Voltage, 8-Channel SPST Switch

General Description

The MAX395 8-channel, serially controlled, single-pole/single-throw (SPST) analog switch offers eight separately controlled switches. The switches conduct equally well in either direction. On-resistance (100Ω max) is matched between switches to 5Ω max and is flat (10Ω max) over the specified signal range.

These CMOS devices can operate continuously with dual power supplies ranging from ±2.7V to ±8V or a single supply between +2.7V and +16V. Each switch can handle rail-to-rail analog signals. The off leakage current is only 0.1nA at +25°C or 5nA at +85°C.

Upon power-up, all switches are off, and the internal shift registers are reset to zero. The MAX395 is electrically equivalent to two MAX391 quad switches controlled by a serial interface, and is pin compatible with the MAX335.

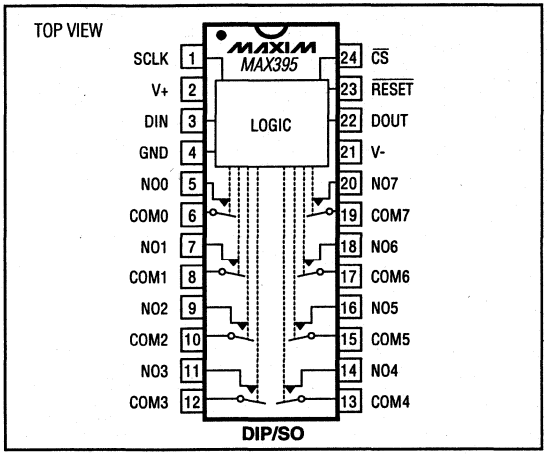
The serial interface is compatible with SPI™/QSPI™ and Microwire™. Functioning as a shift register, it allows data (at DIN) to be clocked in synchronously with the rising edge of clock (SCLK). The shift register's output (DOUT) enables several MAX395s to be daisy chained.

All digital inputs have 0.8V to 2.4V logic thresholds, ensuring both TTL- and CMOS-logic compatibility when using ±5V supplies or a single +5V supply.

Applications

Serial Data-Acquisition Systems	Industrial and Process-Control Systems
Avionics	ATE Equipment
Audio Signal Routing	Networking

Pin Configuration



Features

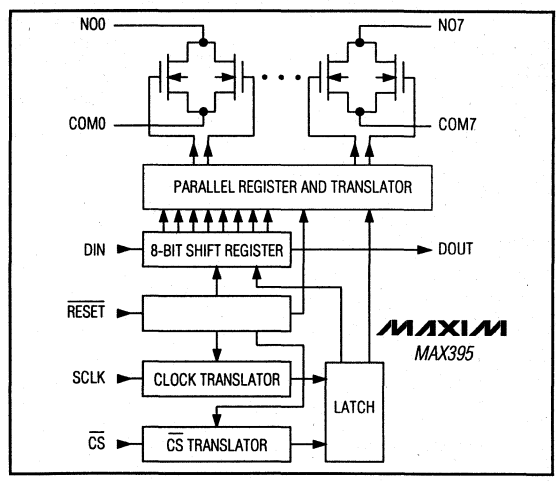
- ♦ SPI™/QSPI™, Microwire™-Compatible Serial Interface
- ♦ 8 Separately Controlled SPST Switches
- ♦ 100Ω Signal Paths with ±5V Supplies
- ♦ Rail-to-Rail Signal Handling
- ♦ Asynchronous $\overline{\text{RESET}}$ Input
- ♦ Pin Compatible with Industry-Standard MAX335
- ♦ ±2.7V to ±8V Dual Supplies
  +2.7V to +16V Single Supply
- ♦ >2kV ESD Protection per Method 3015.7
- ♦ TTL/CMOS-Compatible Inputs (with +5V or ±5V Supplies)

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX395CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX395CWG	0°C to +70°C	24 Wide SO
MAX395C/D	0°C to +70°C	Dice*
MAX395ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX395EWG	-40°C to +85°C	24 Wide SO
MAX395MRG	-55°C to +125°C	24 Narrow CERDIP**

* *Contact factory for dice specifications.*
** *Contact factory for availability.*

Functional Diagram



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Serially Controlled, Low-Voltage, 8-Channel SPST Switch

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to GND
- V+ ..... -0.3V, +17V
- V- ..... -17V, +0.3V
- V+ to V- ..... -0.3V, +17V
- SCLK, $\overline{CS}$, DIN, DOUT, $\overline{RESET}$ ..... -0.3V to (V+ + 0.3V)
- NO, COM ..... (V- - 2V) to (V+ + 2V)

Continuous Current into Any Terminal ..... ±30mA
Peak Current, NO_ or COM_
(pulsed at 1ms,10% duty cycle) ..... ±100mA

Continuous Power Dissipation (T_A = +70°C)
- Narrow Plastic DIP (derate 13.33mW/°C above +70°C) ... 1067mW
- Wide SO (derate 11.76mW/°C above +70°C) 941mW
- Narrow CERDIP (derate 12.50mW/°C above +70°C) 1000mW

Operating Temperature Ranges
- MAX395C_ G ..... 0°C to +70°C
- MAX395E_ G ..... -40°C to +85°C
- MAX395MRG ..... -55°C to +125°C

Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 1)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	V_{COM}, V_{NO}		C, E, M	V-		V+	V
COM, NO On-Resistance	R_{ON}	V+ = 5V, V- = -5V, V_{COM} = ±3V, I_{NO} = 1mA	T_A = +25°C		60	100	Ω
			C, E, M			125	
COM, NO On-Resistance Match Between Channels (Note 2)	ΔR_{ON}	V+ = 5V, V- = -5V, V_{COM} = ±3V, I_{NO} = 1mA	T_A = +25°C			5	Ω
			C, E, M			10	
COM, NO On-Resistance Flatness (Note 2)	$R_{FLAT(ON)}$	V+ = 5V, V- = -5V, I_{NO} = 1mA, V_{COM} = -3V, 0V, 3V	T_A = +25°C			10	Ω
			C, E, M			15	
NO Off Leakage Current (Note 3)	$I_{NO(OFF)}$	V+ = 5.5V, V- = -5.5V, V_{COM} = -4.5V, V_{NO} = 4.5V	T_A = +25°C	-0.1	0.002	0.1	nA
			C, E, M	-10		10	
		V+ = 5.5V, V- = -5.5V, V_{COM} = 4.5V, V_{NO} = -4.5V	T_A = +25°C	-0.1	0.002	0.1	
			C, E, M	-10		10	
COM Off Leakage Current (Note 3)	$I_{COM(OFF)}$	V+ = 5.5V, V- = -5.5V, V_{COM} = -4.5V, V_{NO} = 4.5V	T_A = +25°C	-0.1	0.002	0.1	nA
			C, E, M	-10		10	
		V+ = 5.5V, V- = -5.5V, V_{COM} = 4.5V, V_{NO} = -4.5V	T_A = +25°C	0.1	0.002	0.1	
			C, E, M	-10		10	
COM On Leakage Current (Note 3)	$I_{COM(ON)}$	V+ = 5.5V, V- = -5.5V, V_{COM} = V_{NO} = ±4.5V	T_A = +25°C	-0.2	0.01	0.2	nA
			C, E, M	-20		20	
DIGITAL I/O							
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Voltage Logic Threshold High	V_{IH}		C, E, M	2.4			V
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Voltage Logic Threshold Low	V_{IL}		C, E, M			0.8	V
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Current Logic High or Low	I_{IH}, I_{IL}	V_{DIN}, V_{SCLK}, $V_{\overline{CS}}$ = 0.8V or 2.4V	C, E, M	-1	0.03	1	µA
DOUT Output Voltage Logic High	V_{DOUT}	I_{DOUT} = 0.8mA	C, E, M	2.8		V+	V
DOUT Output Voltage Logic Low	V_{DOUT}	I_{DOUT} = -1.6mA	C, E, M	0		0.4	V
SCLK Input Hysteresis	$SCLK_{HYST}$		C, E, M		100		mV

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 1)	MAX	UNITS
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	From rising edge of $\overline{CS}$	T_A = +25°C		200	400	ns
			C, E, M			500	
Turn-Off Time	t_{OFF}	From rising edge of $\overline{CS}$	T_A = +25°C		90	400	ns
			C, E, M			500	
Break-Before-Make Delay	t_{BBM}	From rising edge of $\overline{CS}$	T_A = +25°C	5	15		ns
Charge Injection (Note 4)	V_{CTE}	C_L = 1nF, V_{NO} = 0V, R_S = 0Ω	T_A = +25°C		2	10	pC
NO Off Capacitance	$C_{NO(OFF)}$	V_{NO} = GND, f = 1MHz	T_A = +25°C		2		pF
COM Off Capacitance	$C_{COM(OFF)}$	V_{COM} = GND, f = 1MHz	T_A = +25°C		2		pF
Switch On Capacitance	$C_{(ON)}$	$V_{COM} = V_{NO}$ = GND, f = 1MHz	T_A = +25°C		8		pF
Off Isolation	V_{ISO}	R_L = 50Ω, C_L = 15pF, $V_{NO} = 1V_{RMS}$, f = 100kHz	T_A = +25°C		-90		dB
Channel-to-Channel Crosstalk	V_{CT}	R_L = 50Ω, C_L = 15pF, $V_{NO} = 1V_{RMS}$, f = 100kHz	T_A = +25°C		<-90		dB
POWER SUPPLY							
Power-Supply Range	V+, V-		C, E, M	±3		±8	V
V+ Supply Current	I+	DIN = $\overline{CS}$ = SCLK = 0V or V+, $\overline{RESET}$ = 0V or V+	T_A = +25°C		7	20	µA
			C, E, M			30	
V- Supply Current	I-	DIN = $\overline{CS}$ = SCLK = 0V or V+, $\overline{RESET}$ = 0V or V+	T_A = +25°C	-1	0.1	1	µA
			C, E, M	-2		2	

Serially Controlled, Low-Voltage, 8-Channel SPST Switch

TIMING CHARACTERISTICS—Dual Supplies (Figure 1)

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 1)	MAX	UNITS
SERIAL DIGITAL INTERFACE							
SCLK Frequency	f_{SCLK}		C, E, M	0		2.1	MHz
Cycle Time	$t_{CH} + t_{CL}$		C, E, M	480			ns
$\overline{CS}$ Lead Time	t_{CSS}		C, E, M	240			ns
$\overline{CS}$ Lag Time	t_{CSH2}		C, E, M	240			ns
SCLK High Time	t_{CH}		C, E, M	190			ns
SCLK Low Time	t_{CL}		C, E, M	190			ns
Data Setup Time	t_{DS}		C, E, M	200	17		ns
Data Hold Time	t_{DH}		C, E, M	0	-17		ns
DIN Data Valid after Falling SCLK (Note 4)	t_{DO}	50% of SCLK to 10% of DOUT, C_L = 10pF	T_A = +25°C		85		ns
			C, E, M			400	
Rise Time of DOUT (Note 4)	t_{DR}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			100	ns
Allowable Rise Time at DIN, SCLK (Note 4)	t_{SCR}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			2	µs
Fall Time of DOUT (Note 4)	t_{DF}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			100	ns
Allowable Fall Time at DIN, SCLK (Note 4)	t_{SCF}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			2	µs
$\overline{RESET}$ Minimum Pulse Width	t_{RW}		T_A = +25°C		70		ns

Note 1: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Note 2: $\Delta R_{ON} = R_{ON(max)} - R_{ON(min)}$. On-resistance match between channels and on-resistance flatness are guaranteed only with specified voltages. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.

Note 3: Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at room temp.

Note 4: Guaranteed by design.

Note 5: Leakage testing at single supply is guaranteed by testing with dual supplies.

Note 6: See Figure 6. Off isolation = $20\log_{10} V_{COM}/V_{NO}$, V_{COM} = output. NO = input to off switch.

Note 7: Between any two switches. See Figure 3.

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +4.5V to +5.5V, V- = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	V_{COM}, V_{NO}		C, E, M	V-		V+	V
COM, NO On-Resistance	R_{ON}	V+ = 5V, V_{COM} = 3.5V, I_{NO} = 1mA	T_A = +25°C		125	175	Ω
			C, E, M			225	
NO Off Leakage Current (Notes 4, 5)	$I_{NO(OFF)}$	V+ = 5.5V, V_{COM} = 4.5V, V_{NO} = 0V	T_A = +25°C	-0.1	0.002	0.1	nA
			C, E, M	-10		10	
		V+ = 5.5V, V_{COM} = 0V, V_{NO} = 4.5V	T_A = +25°C	-0.1	0.002	0.1	
			C, E, M	-10		10	
COM Off Leakage Current (Notes 4, 5)	$I_{COM(OFF)}$	V+ = 5.5V, V_{COM} = 4.5V, V_{NO} = 0V	T_A = +25°C	-0.1	0.002	0.1	nA
			C, E, M	-10		10	
		V+ = 5.5V, V_{COM} = 0V, V_{NO} = 4.5V	T_A = +25°C	-0.1	0.002	0.1	
			C, E, M	-10		10	
COM On Leakage Current (Notes 4, 5)	$I_{COM(ON)}$	V+ = 5.5V, V_{COM} = V_{NO} = 4.5V	T_A = +25°C	-0.2	0.002	0.2	nA
			C, E, M	-20		20	
DIGITAL I/O							
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Voltage Logic Threshold High	V_{IH}		C, E, M	2.4			V
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Voltage Logic Threshold Low	V_{IL}		C, E, M			0.8	V
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Current Logic High or Low	I_{IH}, I_{IL}	V_{DIN}, V_{SCLK}, $V_{\overline{CS}}$ = 0.8V or 2.4V	C, E, M	-1	0.03	1	µA
DOUT Output Voltage Logic High	V_{DOUT}	I_{DOUT} = -0.8mA	C, E, M	2.8		V+	V
DOUT Output Voltage Logic Low	V_{DOUT}	I_{DOUT} = 1.6mA	C, E, M	0		0.4	V
SCLK Input Hysteresis	$SCLK_{HYST}$		C, E, M		100		mV
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	From rising edge of $\overline{CS}$	T_A = +25°C		200	400	ns
			C, E, M			500	
Turn-Off Time	t_{OFF}	From rising edge of $\overline{CS}$	T_A = +25°C		90	400	ns
			C, E, M			500	
Break-Before-Make Delay	t_{BBM}	From rising edge of $\overline{CS}$	T_A = +25°C		15		ns
Charge Injection (Note 4)	V_{CTE}	C_L = 1nF, V_{NO} = 0V, R_S = 0Ω	T_A = +25°C		2	10	pC
Off Isolation (Note 6)	V_{ISO}	R_L = 50Ω, C_L = 15pF, V_{NO} = $1V_{RMS}$, f = 100kHz	T_A = +25°C		-90		dB
Channel-to-Channel Crosstalk (Note 7)	V_{CT}	R_L = 50Ω, C_L = 15pF, V_{NO} = $1V_{RMS}$, f = 100kHz	T_A = +25°C		<-90		dB
POWER SUPPLY							
V+, V- Supply Current	I+	DIN = $\overline{CS}$ = SCLK = 0V or V+, $\overline{RESET}$ = 0V or V+	T_A = +25°C		7	20	µA
			C, E, M			30	

Serially Controlled, Low-Voltage, 8-Channel SPST Switch

TIMING CHARACTERISTICS—Single +5V Supply (Figure 1)

(V+ = +4.5V to +5.5V, V- = 0V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SERIAL DIGITAL INTERFACE							
SCLK Frequency	f_{SCLK}		C, E, M	0		2.1	MHz
Cycle Time (Note 4)	$t_{CH} + t_{CL}$		C, E, M	480			ns
$\overline{CS}$ Lead Time (Note 4)	t_{CSS}		C, E, M	240			ns
$\overline{CS}$ Lag Time (Note 4)	t_{CSH2}		C, E, M	240			ns
SCLK High Time (Note 4)	t_{CH}		C, E, M	190			ns
SCLK Low Time (Note 4)	t_{CL}		C, E, M	190			ns
Data Setup Time (Note 4)	t_{DS}		C, E, M	200	17		ns
Data Hold Time (Note 4)	t_{DH}		C, E, M	0	-17		ns
DIN Data Valid after Falling SCLK (Note 4)	t_{DO}	50% of SCLK to 10% of DOUT, C_L = 10pF	T_A = +25°C		85		ns
			C, E, M			400	
Rise Time of DOUT (Note 4)	t_{DR}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			100	ns
Allowable Rise Time at DIN, SCLK (Note 4)	t_{SCR}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			2	µs
Fall Time of DOUT (Note 4)	t_{DF}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			100	ns
Allowable Fall Time at DIN, SCLK (Note 4)	t_{SCF}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			2	µs
$\overline{RESET}$ Minimum Pulse Width	t_{RW}		T_A = +25°C		70		ns

Note 1: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Note 2: $\Delta R_{ON} = R_{ON(max)} - R_{ON(min)}$. On-resistance match between channels and on-resistance flatness are guaranteed only with specified voltages. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.

Note 3: Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at room temp.

Note 4: Guaranteed by design.

Note 5: Leakage testing at single supply is guaranteed by testing with dual supplies.

Note 6: See Figure 6. Off isolation = $20\log_{10} V_{COM}/V_{NO}$, V_{COM} = output. NO = input to off switch.

Note 7: Between any two switches. See Figure 3.

ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +3.0V to +3.6V, V- = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	V_{COM}, V_{NO}		C, E, M	V-		V+	V
COM, NO On-Resistance	R_{ON}	V+ = 3.0V, V_{COM} = 1.5V, I_{NO} = 1mA	T_A = +25°C		270	500	Ω
			C, E, M			600	
NO Off Leakage Current (Notes 4, 5)	$I_{NO(OFF)}$	V+ = 3.0V, V_{COM} = 3V, V_{NO} = 0V	T_A = +25°C	-0.1	0.002	0.1	nA
			C, E, M	-5		5	
		V+ = 3.6V, V_{COM} = 0V, V_{NO} = 3V	T_A = +25°C	-0.1	0.002	0.1	
			C, E, M	-5		5	
COM Off Leakage Current (Notes 4, 5)	$I_{COM(OFF)}$	V+ = 3.6V, V_{COM} = 3V, V_{NO} = 0V	T_A = +25°C	-0.1	0.002	0.1	nA
			C, E, M	-5		5	
		V+ = 3.6V, V_{COM} = 0V, V_{NO} = 3V	T_A = +25°C	0.1	0.002	0.1	
			C, E, M	-5		5	
COM On Leakage Current (Notes 4, 5)	$I_{COM(ON)}$	V+ = 3.6V, V_{COM} = 3V, V_{NO} = 0V	T_A = +25°C	-0.1	0.002	0.1	nA
			C, E, M	-10		10	
		V+ = 3.6V, V_{COM} = 0V, V_{NO} = 3V	T_A = +25°C	-0.1	0.002	0.1	
			C, E, M	-10		10	
DIGITAL I/O							
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Voltage Logic Threshold High	V_{IH}		C, E	2.4			V
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Voltage Logic Threshold Low	V_{IL}		C, E			0.8	V
DIN, SCLK, $\overline{CS}$, Input Current Logic High or Low	I_{IH}, I_{IL}	V_{DIN}, V_{SCLK}, $V_{\overline{CS}}$ = 0.8V or 2.4V	C, E	-1	0.03	1	µA
DOUT Output Voltage Logic High	V_{DOUT}	I_{DOUT} = 0.1mA	C, E, M	2.8		V+	V
DOUT Output Voltage Logic Low	V_{DOUT}	I_{DOUT} = -1.6mA	C, E, M	0		0.4	V
SCLK Input Hysteresis	$SCLK_{HYST}$		C, E, M		100		mV
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	From rising edge of $\overline{CS}$	T_A = +25°C		260	600	ns
			C, E, M			800	
Turn-Off Time	t_{OFF}	From rising edge of $\overline{CS}$	T_A = +25°C		90	300	ns
			C, E, M			400	
Break-Before-Make Delay	t_{BBM}	From rising edge of $\overline{CS}$	T_A = +25°C		15		ns
Charge Injection (Note 4)	V_{CTE}	C_L = 1nF, V_{NO} = 0V, R_S = 0Ω	T_A = +25°C		2	10	pC
Off Isolation (Note 6)	V_{ISO}	R_L = 50Ω, C_L = 15pF, V_{NO} = $1V_{RMS}$, f = 100kHz	T_A = +25°C		-90		dB
Channel-to-Channel Crosstalk (Note 7)	V_{CT}	R_L = 50Ω, C_L = 15pF, V_{NO} = $1V_{RMS}$, f = 100kHz	T_A = +25°C		<-90		dB
POWER SUPPLY							
V+ Supply Current	I+	DIN = $\overline{CS}$ = SCLK = 0V or V+, $\overline{RESET}$ = 0V or 5V	T_A = +25°C		6	20	µA
			C, E, M			30	

Serially Controlled, Low-Voltage, 8-Channel SPST Switch

TIMING CHARACTERISTICS—Single +3V Supply (Figure 1)

(V+ = +3.0V to +3.6V, V- = 0V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SERIAL DIGITAL INTERFACE							
SCLK Frequency	f_{SCLK}		C, E, M	0		2.1	MHz
Cycle Time (Note 4)	$t_{CH} + t_{CL}$		C, E, M	480			ns
$\overline{CS}$ Lead Time (Note 4)	t_{CSS}		C, E, M	240			ns
$\overline{CS}$ Lag Time (Note 4)	t_{CSH2}		C, E, M	240			ns
SCLK High Time (Note 4)	t_{CH}		C, E, M	190			ns
SCLK Low Time (Note 4)	t_{CL}		C, E, M	190			ns
Data Setup Time (Note 4)	t_{DS}		C, E, M	200	38		ns
Data Hold Time (Note 4)	t_{DH}		C, E, M	0	-38		ns
DIN Data Valid after Falling SCLK (Note 4)	t_{DO}	50% of SCLK to 10% of DOUT, C_L = 10pF	T_A = +25°C		150		ns
			C, E, M			400	
Rise Time of DOUT (Note 4)	t_{DR}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			300	ns
Allowable Rise Time at DIN, SCLK (Note 4)	t_{SCR}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			2	µs
Fall Time of DOUT (Note 4)	t_{DF}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			300	ns
Allowable Fall Time at DIN, SCLK (Note 4)	t_{SCF}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			2	µs
$\overline{RESET}$ Minimum Pulse Width	t_{RW}		T_A = +25°C		105		ns

Note 1: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Note 2: $\Delta R_{ON} = R_{ON(max)} - R_{ON(min)}$. On-resistance match between channels and on-resistance flatness are guaranteed only with specified voltages. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.

Note 3: Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at room temp.

Note 4: Guaranteed by design.

Note 5: Leakage testing at single supply is guaranteed by testing with dual supplies.

Note 6: See Figure 6. Off isolation = $20\log_{10} V_{COM}/V_{NO}$, V_{COM} = output. NO = input to off switch.

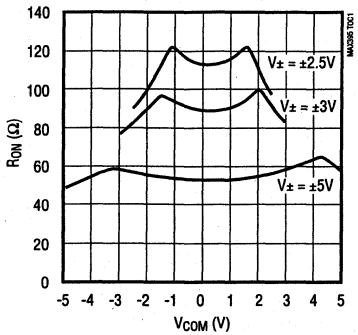
Note 7: Between any two switches. See Figure 3.

Serially Controlled, Low-Voltage, 8-Channel SPST Switch

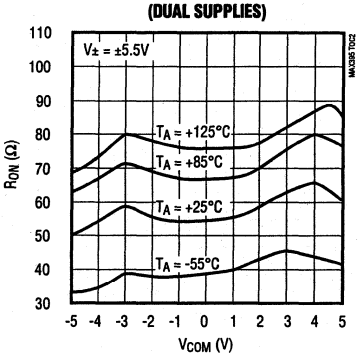
Typical Operating Characteristics

(V+ = +5V, V- = -5V, GND = 0V, T_A = +25°C, unless otherwise noted.)

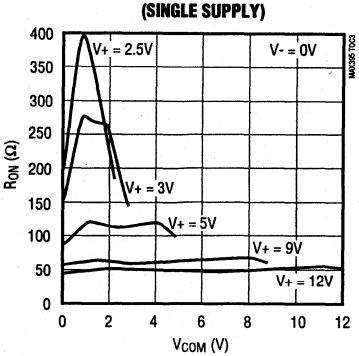
ON-RESISTANCE vs. V_{COM} (DUAL SUPPLIES)



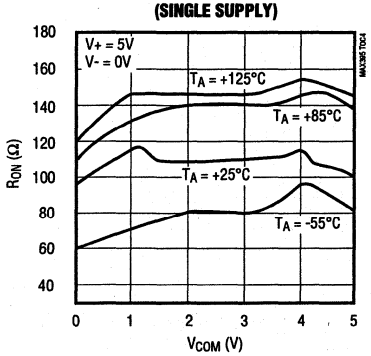
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (DUAL SUPPLIES)



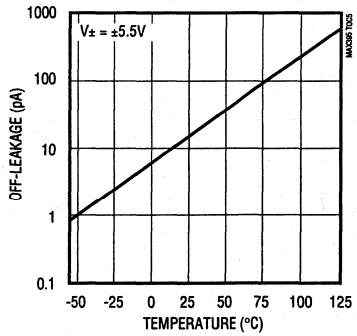
ON-RESISTANCE vs. V_{COM} (SINGLE SUPPLY)



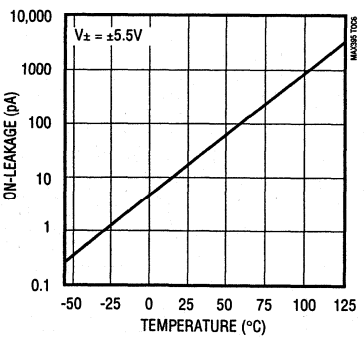
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (SINGLE SUPPLY)



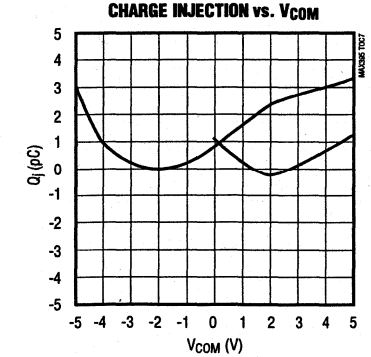
OFF-LEAKAGE vs. TEMPERATURE



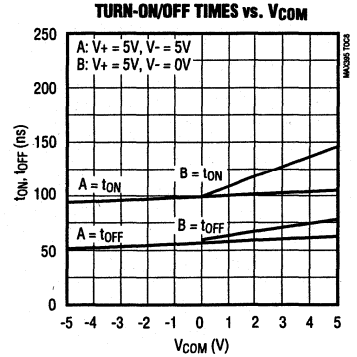
ON-LEAKAGE vs. TEMPERATURE



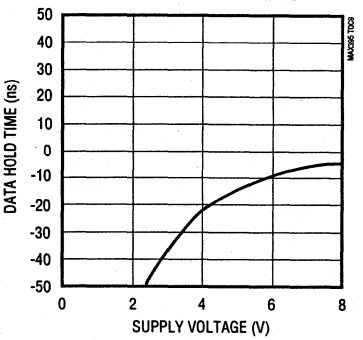
CHARGE INJECTION vs. V_{COM}



TURN-ON/OFF TIMES vs. V_{COM}



DATA HOLD TIME vs. POWER-SUPPLY VOLTAGE

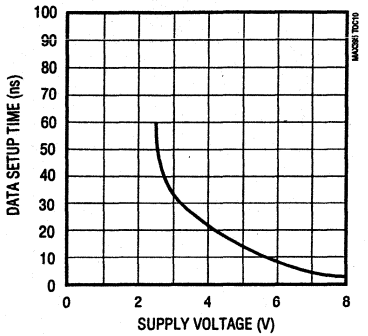


Serially Controlled, Low-Voltage, 8-Channel SPST Switch

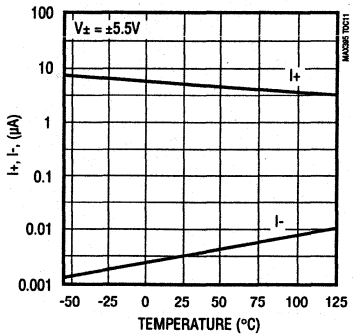
Typical Operating Characteristics (continued)

(V+ = +5V, V- = -5V, GND = 0V, T_A = +25°C, unless otherwise noted.)

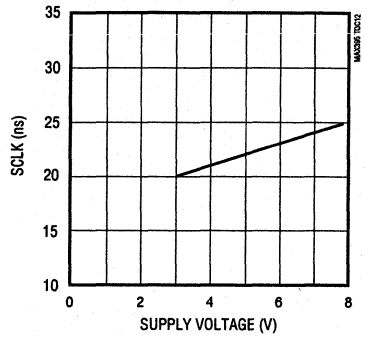
DATA SETUP TIME vs. POSITIVE SUPPLY VOLTAGE



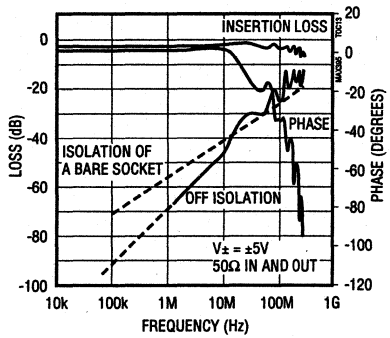
POWER-SUPPLY CURRENT vs. TEMPERATURE



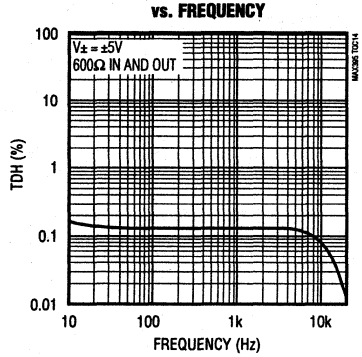
MINIMUM SCLK PULSE WIDTH vs. POSITIVE SUPPLY VOLTAGE



FREQUENCY RESPONSE



TOTAL HARMONIC DISTORTION vs. FREQUENCY



Pin Description

PIN	NAME	FUNCTION
1	SCLK	Serial Clock Digital Input
2	V+	Positive Analog Supply Voltage Input
3	DIN	Serial Data Digital Input
4	GND	Ground. Connect to digital ground. (Analog signals have no ground reference; they are limited to V+ and V-.)
5, 7, 9, 11, 14, 16, 18, 20	NO0–NO7	Normally Open Analog Switches 0–7
6, 8, 10, 12, 13, 15, 17, 19	COM0–COM7	Common Analog Switches 0–7
21	V-	Negative Analog Supply Voltage Input. Connect to GND for single-supply operation
22	DOUT	Serial Data Digital Output. (High is sourced from V+.)
23	$\overline{\text{RESET}}$	Reset Input. Connect to digital (logic) supply (or V+). Drive low to set all switches off and set internal shift registers to 0.
24	$\overline{\text{CS}}$	Chip-Select Digital Input (Figure 1)

Note: NO_ and COM_ pins are identical and interchangeable. Either may be considered as an input or an output; signals pass equally well in either direction.

Detailed Description

Basic Operation

The MAX395's interface can be thought of as an 8-bit shift register controlled by $\overline{CS}$ (Figure 2). While $\overline{CS}$ is low, input data appearing at DIN is clocked into the shift register synchronously with SCLK's rising edge. The data is an 8-bit word, each bit controlling one of eight switches in the MAX395 (Table 1). DOUT is the shift register's output, with data appearing synchronously with SCLK's falling edge. Data at DOUT is simply the input data delayed by eight clock cycles.

When shifting the input data, D7 is the first bit in and out of the shift register. While shifting data, the switches remain in their previous configuration. When the eight bits of data have been shifted in, $\overline{CS}$ is driven high. This updates the new switch configuration and inhibits further data from entering the shift register. Transitions at DIN and SCLK have no effect when $\overline{CS}$ is high, and DOUT holds the first input bit (D7) at its output.

More or less than eight clock cycles can be entered during the $\overline{CS}$ low period. When this happens, the shift register will contain only the last eight serial data bits, regardless of when they were entered. On the rising edge of $\overline{CS}$, all the switches will be set to the corresponding states.

The MAX395's three-wire serial interface is compatible with SPI™, QSPI™, and Microwire™ standards. If interfacing with a Motorola processor serial interface, set CPOL = 0. The MAX395 is considered a slave device (Figures 2 and 3). Upon power-up, the shift register contains all zeros, and all switches are off.

The latch that drives the analog switch is updated on the rising edge of $\overline{CS}$, regardless of SCLK's state. This meets all the SPI and QSPI requirements.

Daisy Chaining

For a simple interface using several MAX395s, "daisy chain" the shift registers as shown in Figure 5. The $\overline{CS}$ pins of all devices are connected together, and a stream of data is shifted through the MAX395s in series. When $\overline{CS}$ is brought high, all switches are updated simultaneously. Additional shift registers may be included anywhere in series with the MAX395 data chain.

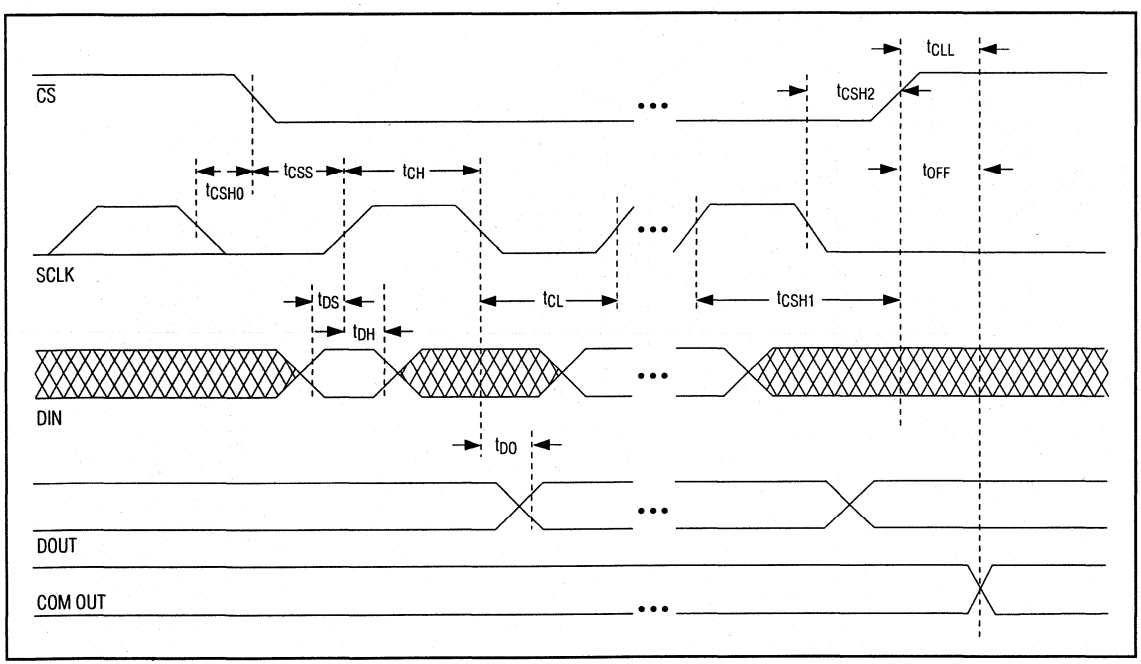


Figure 1. Timing Diagram

Serially Controlled, Low-Voltage, 8-Channel SPST Switch

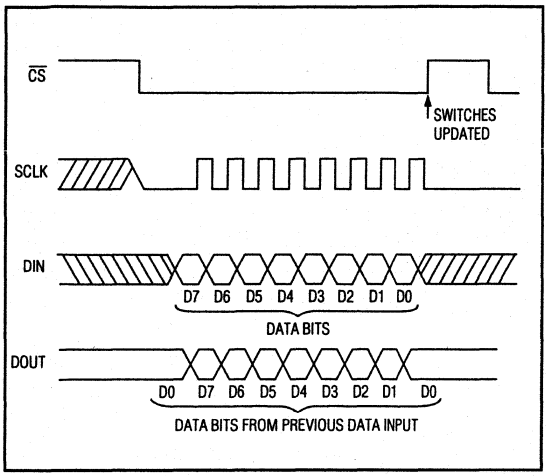


Figure 2. Three-Wire Interface Timing

Addressable Serial Interface

When several serial devices are configured as slaves, addressable by the processor, DIN pins of each decode logic individually control $\overline{CS}$ of each slave device. When a slave is selected, its $\overline{CS}$ pin is driven low, data is shifted in, and $\overline{CS}$ is driven high to latch the data. Typically, only one slave is addressed at a time. DOUT is not used.

Applications Information

Multiplexers

The MAX395 can be used as a multiplexer, but to obtain the same electrical performance with slightly improved programming speed, use the MAX349 8-channel mux or the MAX350 dual 4-channel mux, both in 18-pin packages.

Table 1. Serial-Interface Switch Programming

$\overline{RESET}$	DATA BITS								FUNCTION
	D7	D6	D5	D4	D3	D2	D1	D0	
0	X	X	X	X	X	X	X	X	All switches open, D7–D0 = 0
1	0	X	X	X	X	X	X	X	Switch 7 open (off)
1	1	X	X	X	X	X	X	X	Switch 7 closed (on)
1	X	0	X	X	X	X	X	X	Switch 6 open (off)
1	X	1	X	X	X	X	X	X	Switch 6 closed (on)
1	X	X	0	X	X	X	X	X	Switch 5 open (off)
1	X	X	1	X	X	X	X	X	Switch 5 closed (on)
1	X	X	X	0	X	X	X	X	Switch 4 open (off)
1	X	X	X	1	X	X	X	X	Switch 4 closed (on)
1	X	X	X	X	0	X	X	X	Switch 3 open (off)
1	X	X	X	X	1	X	X	X	Switch 3 closed (on)
1	X	X	X	X	X	0	X	X	Switch 2 open (off)
1	X	X	X	X	X	1	X	X	Switch 2 closed (on)
1	X	X	X	X	X	X	0	X	Switch 1 open (off)
1	X	X	X	X	X	X	1	X	Switch 1 closed (on)
1	X	X	X	X	X	X	X	0	Switch 0 open (off)
1	X	X	X	X	X	X	X	1	Switch 0 closed (on)

Serially Controlled, Low-Voltage, 8-Channel SPST Switch

8x1 Multiplexer

To use the MAX395 as an 8x1 multiplexer, connect all common pins together (COM0–COM7) to form the mux output; the mux inputs are NO0–NO7.

The mux can be programmed normally, with only one channel selected for every eight clock pulses, or it can be programmed in a fast mode, where channel changing occurs on each clock pulse. In this mode, the channels are selected by sending a single high pulse (corresponding to the selected channel) at DIN, and a corresponding $\overline{CS}$ low pulse for every eight clock pulses. As this is clocked through the register by SCLK, each switch sequences one channel at a time, starting with Channel 7.

Dual, Differential 4-Channel Multiplexer

To use the MAX395 as a dual (4x2) mux, connect COM0–COM3 together and connect COM4–COM7 together, forming the two outputs. The mux input pairs become NO0/NO4, NO1/NO5, NO2/NO6, and NO3/NO7.

The mux can be programmed normally, with only one differential channel selected for every eight clock pulses, or it can be programmed in a fast mode, where channel changing occurs on each clock pulse.

In fast mode, the channels are selected by sending two high pulses spaced four clock pulses apart (corresponding to the two selected channels) at DIN, and a corresponding $\overline{CS}$ low pulse for each of the first eight clock pulses. As this is clocked through the register by

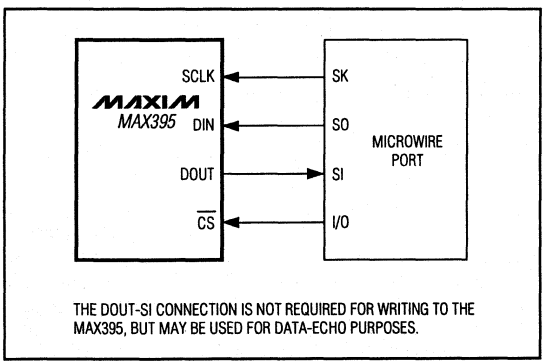


Figure 3. Connections for Microwire

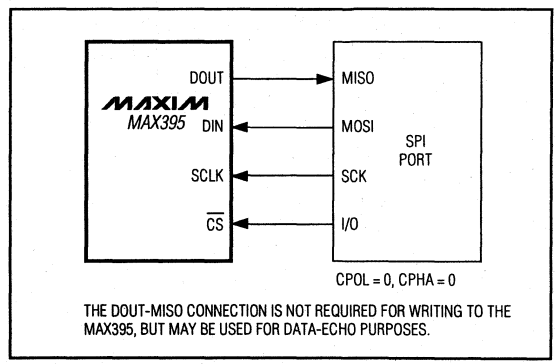


Figure 4. Connections for SPI and QSPI

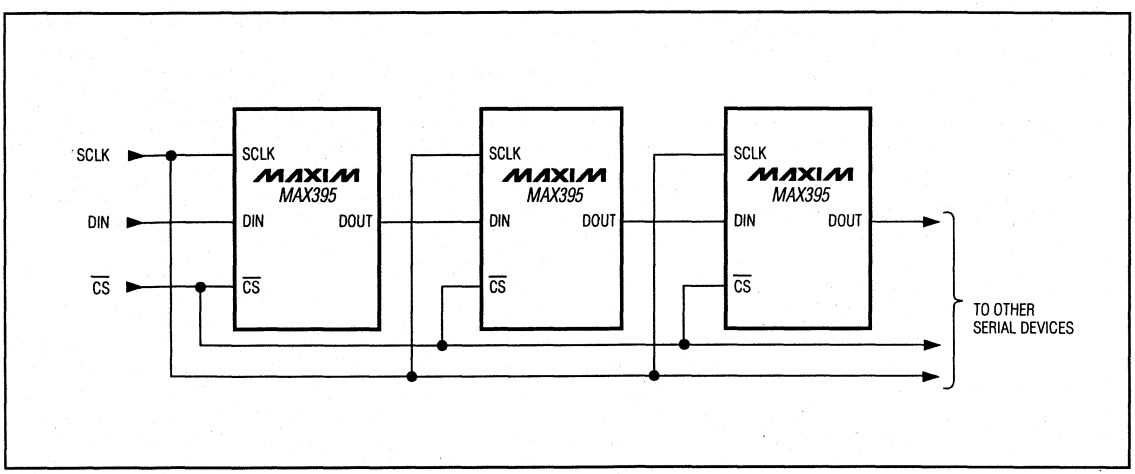


Figure 5. Daisy-Chained Connection

Serially Controlled, Low-Voltage, 8-Channel SPST Switch

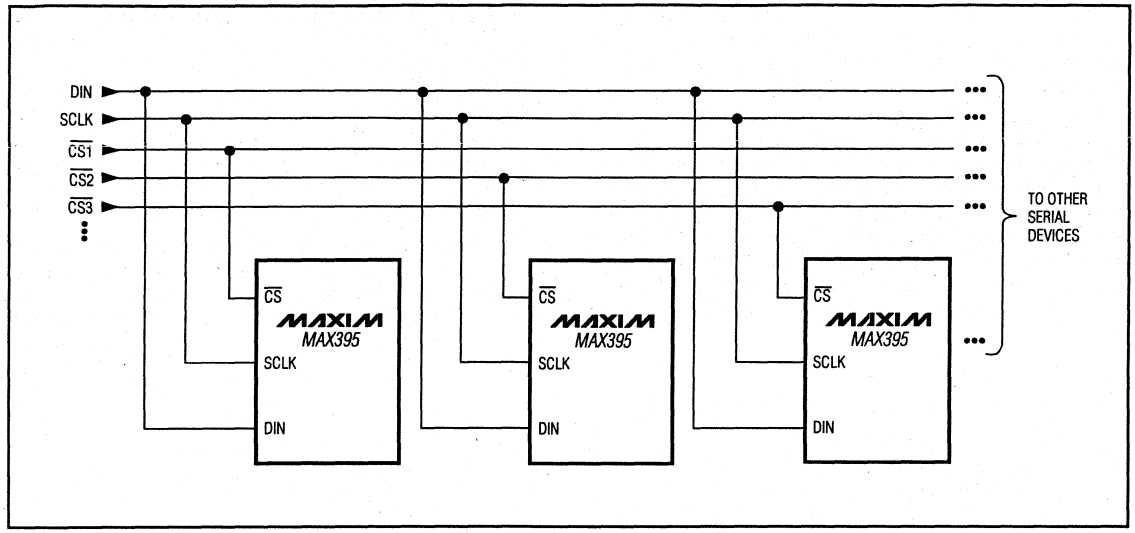


Figure 6. Addressable Serial Interface

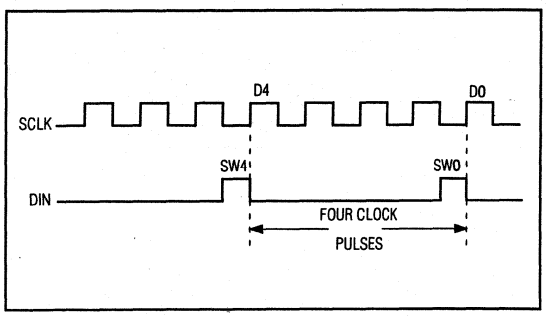


Figure 7. Differential Multiplexer Input Control

SCLK, each switch sequences one differential channel at a time, starting with channel 7/0. After the first eight bits have been sent, subsequent channel sequencing can occur by repeating this sequence or, even faster, by sending only one DIN high pulse and one $\overline{CS}$ low pulse for each four clock pulses.

SPDT Switches

To use the MAX395 as a quad, single-pole/double-throw (SPDT) switch, connect COM0 to NO1, COM2 to NO3, COM4 to NO5, and COM6 to NO7, forming the four "common" pins. Program these four switches with pairs of instructions, as shown in Table 2.

Reset Function

$\overline{RESET}$ is the internal reset pin. It is usually connected to a logic signal or V+. Drive $\overline{RESET}$ low to open all switches and set the contents of the internal shift register to zero simultaneously. When $\overline{RESET}$ is high, the part functions normally and DOUT is sourced from V+. $\overline{RESET}$ must not be driven beyond V+ or GND.

Power-Supply Considerations

Overview

The MAX395 construction is typical of most CMOS analog switches. It has three supply pins: V+, V-, and GND. V+ and V- are used to drive the internal CMOS switches and to set the limits of the analog voltage on any switch. Reverse ESD-protection diodes are internally connected between each analog signal pin and both V+ and V-. If any analog signal exceeds V+ or V-, one of these diodes will conduct. During normal operation, these (and other) reverse-biased ESD diodes leak, forming the only current drawn from V+ or V-.

Virtually all the analog leakage current is through the ESD diodes. Although the ESD diodes on a given signal pin are identical, and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or V- and the analog signal. This means their leakages vary as the signal varies. The difference in the two diode leakages to the V+ and V- pins constitutes the analog signal-path leakage current. All analog leak-

Table 2. SPDT Switch Programming

$\overline{RESET}$	DATA BITS								FUNCTION
	D7	D6	D5	D4	D3	D2	D1	D0	
0	X	X	X	X	X	X	X	X	All switches open, D7–D0 = 0
1	0	1	X	X	X	X	X	X	Switch 7 off and 6 on
1	1	0	X	X	X	X	X	X	Switch 6 off and 7 on
1	X	X	0	1	X	X	X	X	Switch 5 off and 4 on
1	X	X	1	0	X	X	X	X	Switch 4 off and 5 on
1	X	X	X	X	0	1	X	X	Switch 3 off and 2 on
1	X	X	X	X	1	0	X	X	Switch 2 off and 3 on
1	X	X	X	X	X	X	0	1	Switch 1 off and 0 on
1	X	X	X	X	X	X	1	0	Switch 0 off and 1 on

age current flows to the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of either the same or opposite polarity.

There is no connection between the analog signal paths and GND.

V+ and GND power the internal logic and logic-level translators, and set both the input and output logic limits. The logic-level translators convert the logic levels to switched V+ and V- signals to drive the analog signal gates. This drive signal is the only connection between the logic supplies (and signals) and the analog supplies. V+, and V- have ESD-protection diodes to GND. The logic-level inputs and output have ESD protection to V+ and to GND.

The logic-level thresholds are CMOS and TTL compatible when V+ is +5V. As V+ is raised, the threshold increases slightly. So when V+ reaches +12V, the threshold is about 3.1V; slightly above the TTL guaranteed high-level minimum of 2.8V, but still compatible with CMOS outputs.

Bipolar Supplies

The MAX395 operates with bipolar supplies between ±3.0V and ±8V. The V+ and V- supplies need not be symmetrical, but their sum cannot exceed the absolute maximum rating of 17V. **Do not connect the MAX395 V+ to +3V and connect the logic-level pins to TTL logic-level signals. This exceeds the absolute maximum ratings and can damage the part and/or external circuits.**

Single Supply

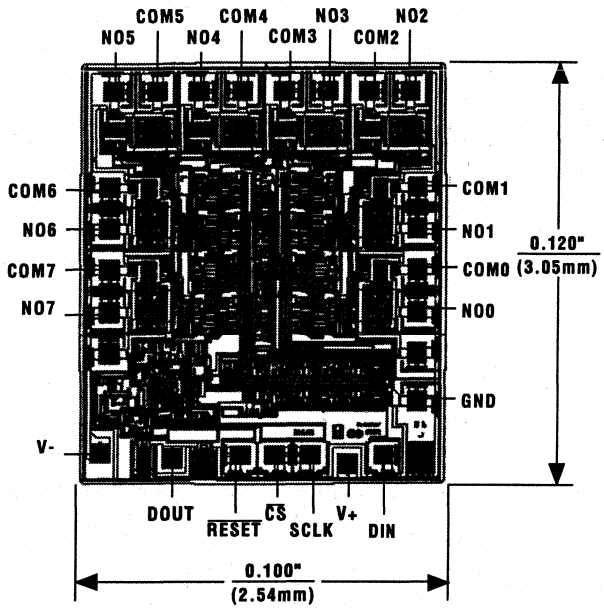
The MAX395 operates from a single supply between +3V and +16V when V- is connected to GND. All of the bipolar precautions must be observed.

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat up to 50MHz (see *Typical Operating Characteristics).* Above 20MHz, the on-response has several minor peaks that are highly layout dependent. The problem is not turning the switch on, but turning it off. The off-state switch acts like a capacitor and passes higher frequencies with less attenuation. At 10MHz, off isolation is about -45dB in 50Ω systems, becoming worse (approximately 20dB per decade) as frequency increases. Higher circuit impedances also make off isolation worse. Adjacent channel attenuation is about 3dB above that of a bare IC socket, and is due entirely to capacitive coupling.

Serially Controlled, Low-Voltage, 8-Channel SPST Switch

Chip Topography



TRANSISTOR COUNT: 500

SUBSTRATE CONNECTED TO V+.

19-0463; Rev 0; 1/96

MAXIM

Low-Voltage, CMOS Analog Multiplexers/Switches

General Description

The MAX4051/MAX4052/MAX4053 and MAX4051A/MAX4052A/MAX4053A are low-voltage, CMOS analog ICs configured as an 8-channel multiplexer (MAX4051/A), two 4-channel multiplexers (MAX4052/A), and three single-pole/double-throw (SPDT) switches (MAX4053/A). The A-suffix parts are fully characterized for on-resistance match, on-resistance flatness, and low leakage.

These CMOS devices can operate continuously with dual power supplies ranging from ±2.7V to ±8V or a single supply between +2.7V and +16V. Each switch can handle rail-to-rail analog signals. The off leakage current is only 0.1nA at +25°C or 5nA at +85°C (MAX4051A/MAX4052A/4053A).

All digital inputs have 0.8V to 2.4V logic thresholds, ensuring TTL/CMOS-logic compatibility when using ±5V or a single +5V supply.

Applications

Battery-Operated Equipment

Audio and Video Signal Routing

Low-Voltage Data-Acquisition Systems

Communications Circuits

Features

- **Pin Compatible with Industry-Standard 74HC4051/74HC4052/74HC4053**
- **Guaranteed On-Resistance: 100Ω with ±5V Supplies**
- **Guaranteed Match Between Channels: 6Ω (MAX4051A–MAX4053A) 12Ω (MAX4051–MAX4053)**
- **Guaranteed Low Off Leakage Currents: 0.1nA at +25°C (MAX4051A–MAX4053A) 1nA at +25°C (MAX4051–MAX4053)**
- **Guaranteed Low On Leakage Currents: 0.1nA at +25°C (MAX4051A–MAX4053A) 1nA at +25°C (MAX4051–MAX4053)**
- **Single-Supply Operation from +2.0V to +16V Dual-Supply Operation from ±2.7V to ±8V**
- **TTL/CMOS-Logic Compatible**
- **Low Distortion: < 0.04% (600Ω)**
- **Low Crosstalk: < -90dB (50Ω)**
- **High Off Isolation: < -90dB (50Ω)**

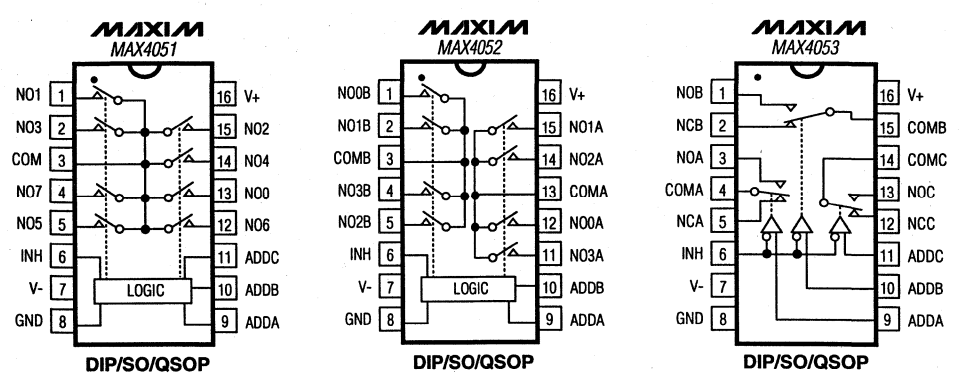
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4051ACPE	0°C to +70°C	16 Plastic DIP
MAX4051ACSE	0°C to +70°C	16 Narrow SO
MAX4051ACEE	0°C to +70°C	16 QSOP

Ordering Information continued at end of data sheet.

Pin Configurations/Functional Diagrams

TOP VIEW



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Low-Voltage, CMOS Analog Multiplexers/Switches

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to GND
V+ .....-0.3V to +17V
V- .....+0.3V to -17V
V+ to V- .....-0.3V to +17V
Voltage into Any Terminal (Note 1) .....(V- - 2V) to (V+ + 2V)
or 30mA (whichever occurs first)
Continuous Current into Any Terminal .....±30mA
Peak Current, NO or COM
(pulsed at 1ms, 10% duty cycle) .....±100mA

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
Narrow SO (derate 8.70mW/°C above +70°C) 696mW
QSOP (derate 8.00mW/°C above +70°C) 640mW
CERDIP (derate 10.00mW/°C above +70°C) 800mW
Operating Temperature Ranges
MAX405_C_ E/MAX405_AC_E .....0°C to +70°C
MAX405_E_ E/MAX405_AE_E .....-40°C to +85°C
MAX405_MJE/MAX405_AMJE .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: Signals on any terminal exceeding V+ or V- are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	V_{COM}, V_{NO}			C, E, M	V-		V+	V
COM–NO On-Resistance	R_{ON}	V+ = 5V, V- = -5V, I_{NO} = 1mA, V_{COM} = ±3V		T_A = +25°C		60	100	Ω
				C, E, M			125	
COM–NO On-Resistance Match Between Channels (Note 3)	ΔR_{ON}	V+ = 5V, V- = -5V, I_{NO} = 1mA, V_{COM} = ±3V	MAX4051A, MAX4052A, MAX4053A	T_A = +25°C			6	Ω
				C, E, M			12	
			MAX4051, MAX4052, MAX4053	T_A = +25°C			12	
				C, E, M			18	
COM–NO On-Resistance Flatness (Note 4)	$R_{FLAT(ON)}$	V+ = 5V, V- = -5V, I_{NO} = 1mA, V_{COM} = -3V, 0V, 3V	MAX4051A, MAX4052A, MAX4053A	T_A = +25°C			10	Ω
				C, E, M			15	
NO Off Leakage Current (Note 5)	$I_{NO(OFF)}$	V+ = 5.5V, V- = -5.5V, V_{NO} = 4.5V, V_{COM} = -4.5V	MAX4051, MAX4052, MAX4053	T_A = +25°C	-1	0.002	1	nA
				C, E	-10		10	
				M	-100		100	
		V+ = 5.5V, V- = -5.5V, V_{NO} = -4.5V, V_{COM} = 4.5V	MAX4051A, MAX4052A, MAX4053A	T_A = +25°C	-0.1	0.002	0.1	
				C, E	-5		5	
				M	-100		100	

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
COM Off Leakage Current (Note 5)	$I_{COM(OFF)}$	V+ = 5.5V, V- = -5.5V, V_{NO} = 4.5V, V_{COM} = -4.5V	MAX4051A	T_A = +25°C	-0.1	0.002	0.1	nA
				C, E	-5		5	
				M	-100		100	
			MAX4051	T_A = +25°C	-1	0.002	1	
				C, E	-10		10	
				M	-100		100	
			MAX4052A, MAX4053A	T_A = +25°C	-0.1	0.002	0.1	
				C, E	-2.5		2.5	
				M	-100		100	
			MAX4052, MAX4053	T_A = +25°C	-1	0.002	1	
				C, E	-5		5	
				M	-50		50	
		V+ = 5.5V, V- = -5.5V, V_{NO} = -4.5V, V_{COM} = 4.5V	MAX4051A	T_A = +25°C	-0.1	0.002	0.1	
				C, E	-5		5	
				M	-100		100	
			MAX4051	T_A = +25°C	-1	0.002	1	
				C, E	-10		10	
				M	-100		100	
			MAX4052A, MAX4053A	T_A = +25°C	-0.1	0.002	0.1	
				C, E	-2.5		2.5	
				M	-50		50	
			MAX4052, MAX4053	T_A = +25°C	-1	0.002	1	
				C, E	-5		5	
				M	-50		50	
COM On Leakage Current (Note 5)	$I_{COM(ON)}$	V+ = 5.5V, V- = -5.5V, $V_{COM} = V_{NO}$ = ±4.5V	MAX4051A	T_A = +25°C	-0.1	0.002	0.1	nA
				C, E	-5		5	
				M	-100		100	
			MAX4051	T_A = +25°C	-1	0.002	1	
				C, E	-10		10	
				M	-100		100	
			MAX4052A, MAX4053A	T_A = +25°C	-0.1	0.002	0.1	
				C, E	-2.5		2.5	
				M	-50		50	
			MAX4052, MAX4053	T_A = +25°C	-1	0.002	1	
				C, E	-5		5	
				M	-50		50	

Low-Voltage, CMOS Analog Multiplexers/Switches

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
DIGITAL I/O							
ADD, INH Input Logic Threshold High	V_{IH}		C, E, M	2.4			V
ADD, INH Input Logic Threshold Low	V_{IL}		C, E, M			0.8	V
ADD, INH Input Current Logic High or Low	I_{IH}, I_{IL}	V_{ADD}, V_{INH} = V+, 0V	C, E, M	-1	0.03	1	µA
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time (Note 6)	t_{ON}	Figure 3	T_A = +25°C		50	175	ns
			C, E, M			225	
Turn-Off Time (Note 6)	t_{OFF}	Figure 3	T_A = +25°C		40	150	ns
			C, E, M			200	
Transition Time	t_{TRANS}	Figure 2	T_A = +25°C		75	250	ns
Break-Before-Make Delay	t_{OPEN}	Figure 4	T_A = +25°C	2	10		ns
Charge Injection (Note 6)	Q	C_L = 1nF, R_S = 0Ω, V_{NO} = 0V, Figure 5	T_A = +25°C		2	10	pC
NO Off Capacitance	$C_{NO(OFF)}$	V_{NO} = GND, f = 1MHz, Figure 7	T_A = +25°C		2		pF
COM Off Capacitance	$C_{COM(OFF)}$	V_{COM} = GND, f = 1MHz, Figure 7	T_A = +25°C		2		pF
Switch On Capacitance	$C_{(ON)}$	V_{COM} = V_{NO} = GND, f = 1MHz, Figure 7	T_A = +25°C		8		pF
Off Isolation	V_{ISO}	C_L = 15pF, R_L = 50Ω, f = 100kHz, V_{NO} = $1V_{RMS}$, Figure 6	T_A = +25°C		<-90		dB
Channel-to-Channel Crosstalk	V_{CT}	C_L = 15pF, R_L = 50Ω, f = 100kHz, V_{NO} = $1V_{RMS}$, Figure 6	T_A = +25°C		<-90		dB
POWER SUPPLY							
Power-Supply Range	V+, V-		C, E, M	±2.7		±8	V
V+ Supply Current	I+	INH = ADD = 0V or V+	T_A = +25°C	-1	0.1	1	µA
			C, E, M			10	
V- Supply Current	I-	INH = ADD = 0V or V+	T_A = +25°C	-1	0.1	1	µA
			C, E, M	-10			

Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Note 3: ΔR_{ON} = $R_{ON(MAX)}$ - $R_{ON(MIN)}$.

Note 4: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges; i.e., V_{NO} = 3V to 0V and 0V to -3V.

Note 5: Leakage parameters are 100% tested at maximum-rated hot operating temperature, and guaranteed by correlation at T_A = +25°C.

Note 6: Guaranteed by design, not production tested.

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +4.5V to +5.5V, V- = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	V_{COM}, V_{NO}			C, E, M	V-		V+	V
COM–NO On-Resistance	R_{ON}	V+ = 5V, I_{NO} = 1mA, V_{COM} = 3.5V		T_A = +25°C		125	225	Ω
				C, E, M			280	
NO Off Leakage Current (Note 5)	$I_{NO(OFF)}$	V+ = 5.5V, V_{NO} = 4.5V, V_{COM} = 0V		T_A = +25°C	-1	0.002	1	nA
				C, E	-10		10	
				M	-100		100	
		V+ = 5.5V, V_{NO} = 0V, V_{COM} = 4.5V		T_A = +25°C	-1	0.002	1	
				C, E	-10		10	
				M	-100		100	
COM Off Leakage Current (Note 5)	$I_{COM(OFF)}$	V+ = 5.5V, V_{NO} = 4.5V, V_{COM} = 0V	MAX4051/A	T_A = +25°C	-1	0.002	1	nA
				C, E	-10		10	
				M	-100		100	
			MAX4052/A, MAX4053/A	T_A = +25°C	-1	0.002	1	
				C, E	-5		5	
				M	-50		50	
		V+ = 5.5V, V_{NO} = 0V, V_{COM} = 4.5V or 0V	MAX4051/A	T_A = +25°C	-1	0.002	1	
				C, E	-10		10	
				M	-100		100	
			MAX4052/A, MAX4053/A	T_A = +25°C	-1	0.002	1	
				C, E	-5		5	
				M	-50		50	
COM On Leakage Current (Note 5)	$I_{COM(ON)}$	V+ = 5.5V, V_{COM} = V_{NO} = 4.5V	MAX4051/A	T_A = +25°C	-1	0.002	1	nA
				C, E	-10		10	
				M	-100		100	
			MAX4052/A, MAX4053/A	T_A = +25°C	-1	0.002	1	
				C, E	-10		10	
				M	-100		100	
DIGITAL I/O								
ADD, INH Input Logic Threshold High	V_{IH}			C, E, M	2.4			V
ADD, INH Input Logic Threshold Low	V_{IL}			C, E, M			0.8	V
ADD, INH Input Current Logic High or Low	I_{IH}, I_{IL}	V_{ADD}, V_{INH} = V+, 0V		C, E, M	-1	0.03	1	µA
POWER SUPPLY								
V+ Supply Current	I+	INH = ADD = 0V or V+		T_A = +25°C	-1		1	µA
				C, E, M			10	

Low-Voltage, CMOS Analog Multiplexers/Switches

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V+ = +4.5V to +5.5V, V- = 0V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time (Note 6)	t_{ON}	Figure 3	T_A = +25°C		90	200	ns
			C, E, M			275	
Turn-Off Time (Note 6)	t_{OFF}	Figure 3	T_A = +25°C		60	125	ns
			C, E, M			175	
Break-Before-Make Delay	t_{OPEN}	Figure 4	T_A = +25°C		30		ns
Charge Injection (Note 6)	Q	C_L = 1nF, R_S = 0Ω, V_{NO} = 0V, Figure 5	T_A = +25°C		2	10	pC
Off Isolation	V_{ISO}	C_L = 15pF, R_L = 50Ω, f = 100kHz, V_{NO} = $1V_{RMS}$, Figure 6	T_A = +25°C		<-90		dB
Channel-to-Channel Crosstalk	V_{CT}	C_L = 15pF, R_L = 50Ω, f = 100kHz, V_{NO} = $1V_{RMS}$, Figure 6	T_A = +25°C		<-90		dB

Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Note 3: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.

Note 4: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges; i.e., V_{NO} = 3V to 0V and 0V to -3V.

Note 5: Leakage parameters are 100% tested at maximum-rated hot operating temperature, and guaranteed by correlation at T_A = +25°C.

Note 6: Guaranteed by design, not production tested.

ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +3.0V to +3.6V, V- = 0V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	V_{COM}, V_{NO}			C, E, M	V-		V+	V
COM–NO On-Resistance	R_{ON}	I_{NO} = 1mA, V+ = 3V, V_{COM} = 1.5V		T_A = +25°C		250	525	Ω
				C, E, M			700	
NO Off Leakage Current (Note 5)	$I_{NO(OFF)}$	V+ = 3.6V, V_{NO} = 3V, V_{COM} = 0V		T_A = +25°C	-1	0.002	1	nA
				C, E	-10		10	
				M	-100		100	
		V+ = 3.6V, V_{NO} = 0V, V_{COM} = 3V		T_A = +25°C	-1	0.002	1	
				C, E	-10		10	
				M	-100		100	
COM Off Leakage Current (Note 5)	$I_{COM(OFF)}$	V+ = 3.6V, V_{NO} = 3V, V_{COM} = 0V	MAX4051/A	T_A = +25°C	-1	0.002	1	nA
				C, E	-10		10	
				M	-100		100	
			MAX4052/A, MAX4053/A	T_A = +25°C	-1	0.002	1	
				C, E	-5		5	
				M	-50		50	
		V+ = 3.6V, V_{NO} = 0V, V_{COM} = 3V	MAX4051/A	T_A = +25°C	-1	0.002	1	
				C, E	-10		10	
				M	-100		100	
			MAX4052/A, MAX4053/A	T_A = +25°C	-1	0.002	1	
				C, E	-5		5	
				M	-50		50	
COM On Leakage Current (Note 5)	$I_{COM(ON)}$	V+ = 3.6V, V_{COM} = V_{NO} = 3V	MAX4051/A	T_A = +25°C	-1	0.002	1	nA
				C, E	-10		10	
				M	-100		100	
			MAX4052/A, MAX4053/A	T_A = +25°C	-1	0.002	1	
				C, E	-10		10	
				M	-100		100	
DIGITAL I/O								
ADD, INH Input Logic Threshold High	V_{IH}			C, E, M	2.4			V
ADD, INH Input Logic Threshold Low	V_{IL}			C, E, M			0.8	V
ADD, INH Input Current Logic High or Low	I_{IH}, I_{IL}	V_{ADD}, V_{INH} = V+, 0V		C, E, M	-1	0.03	1	µA
POWER SUPPLY								
V+ Supply Current	I+	INH = ADD = 0V or V+		T_A = +25°C	-1		1	µA
				C, E, M			10	

Low-Voltage, CMOS Analog Multiplexers/Switches

ELECTRICAL CHARACTERISTICS—Single +3V Supply (continued)

(V+ = +3.0V to +3.6V, V- = 0V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

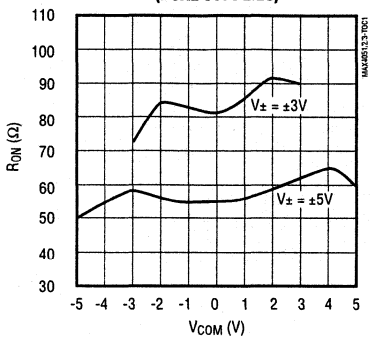
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time (Note 6)	t_{ON}	Figure 3	T_A = +25°C		180	600	ns
			C, E, M			700	
Turn-Off Time (Note 6)	t_{OFF}	Figure 3	T_A = +25°C		100	300	ns
			C, E, M			400	
Break-Before-Make Delay	t_{OPEN}	Figure 4	T_A = +25°C		90		ns
Charge Injection (Note 6)	Q	C_L = 1nF, R_S = 0Ω, V_{NO} = 0V, Figure 5	T_A = +25°C		1	10	pC
Off Isolation	V_{ISO}	C_L = 15pF, R_L = 50Ω, f = 100kHz, V_{NO} = $1V_{RMS}$, Figure 6	T_A = +25°C		<-90		dB
Channel-to-Channel Crosstalk	V_{CT}	C_L = 15pF, R_L = 50Ω, f = 100kHz, V_{NO} = $1V_{RMS}$, Figure 6	T_A = +25°C		<-90		dB

Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.
Note 3: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.
Note 4: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges; i.e., V_{NO} = 3V to 0V and 0V to -3V.
Note 5: Leakage parameters are 100% tested at maximum-rated hot operating temperature, and guaranteed by correlation at T_A = +25°C.
Note 6: Guaranteed by design, not production tested.

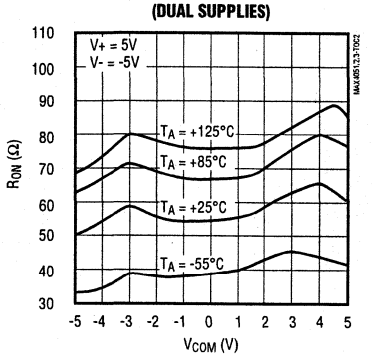
Typical Operating Characteristics

(V+ = +5V, V- = -5V, GND = 0V, T_A = +25°C, unless otherwise noted.)

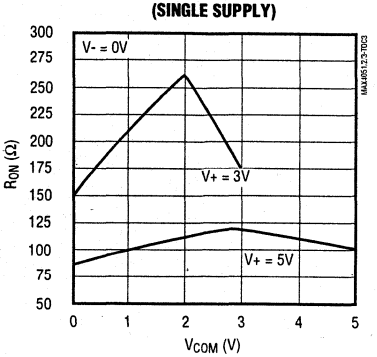
ON-RESISTANCE vs. VCOM (DUAL SUPPLIES)



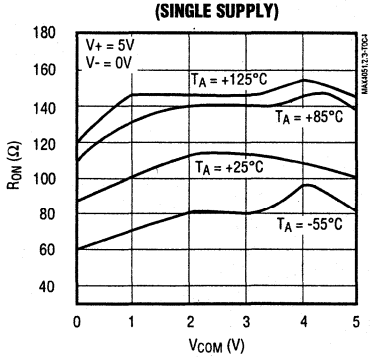
ON-RESISTANCE vs. VCOM AND TEMPERATURE (DUAL SUPPLIES)



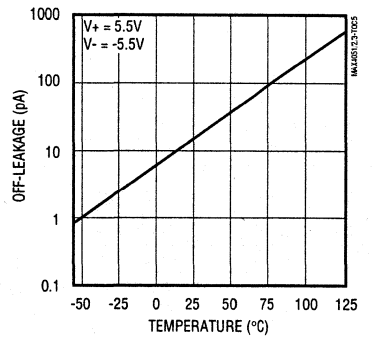
ON-RESISTANCE vs. VCOM (SINGLE SUPPLY)



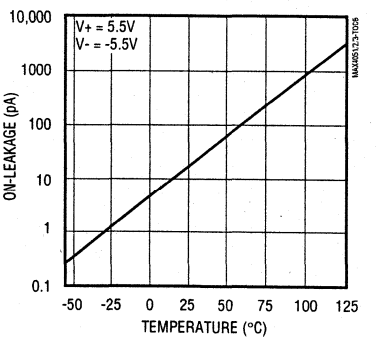
ON-RESISTANCE vs. VCOM AND TEMPERATURE (SINGLE SUPPLY)



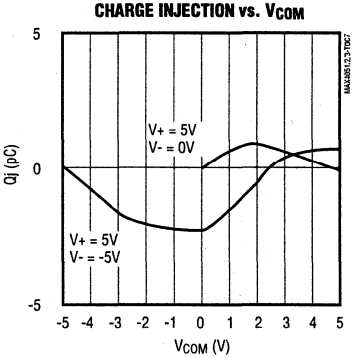
OFF-LEAKAGE vs. TEMPERATURE



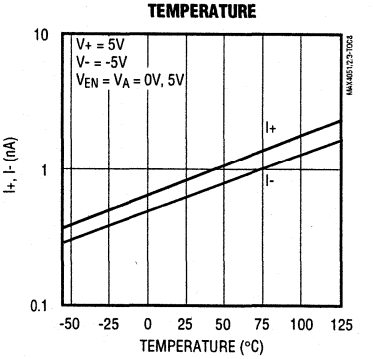
ON-LEAKAGE vs. TEMPERATURE



CHARGE INJECTION vs. VCOM



SUPPLY CURRENT vs. TEMPERATURE

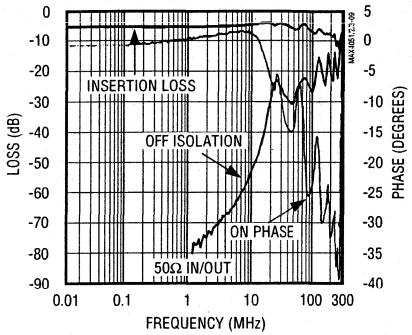


Low-Voltage, CMOS Analog Multiplexers/Switches

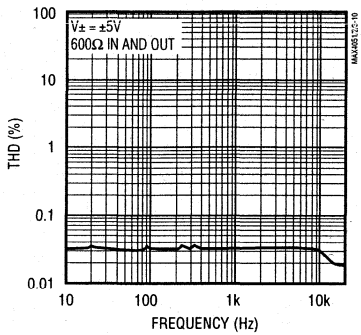
Typical Operating Characteristics (continued)

(V+ = +5V, V- = -5V, GND = 0V, T_A = +25°C, unless otherwise noted.)

FREQUENCY RESPONSE



TOTAL HARMONIC DISTORTION vs. FREQUENCY



Pin Descriptions

PIN			NAME	FUNCTION
MAX4051/ MAX4051A	MAX4052/ MAX4052A	MAX4053/ MAX4053A		
13, 1, 15, 2, 14, 5, 12, 4	—	—	NO0–NO7	Analog Switch Inputs 0–7
3	—	—	COM	Analog Switch Common
—	1, 2, 5, 4	—	NO0B–NO3B	Analog Switch "B" Inputs 0–3
—	3	15	COMB	Analog Switch "B" Common
—	—	1	NOB	Analog Switch "B" Normally Open Input
—	—	2	NCB	Analog Switch "B" Normally Closed Input
—	—	3	NOA	Analog Switch "A" Normally Open Input
—	—	5	NCA	Analog Switch "A" Normally Closed Input
6	6	6	INH	Digital Inhibit Input. Normally connect to GND. Can be driven to logic high to set all switches off.
7	7	7	V-	Negative Analog Supply Voltage Input. Connect to GND for single-supply operation.
8	8	8	GND	Ground. Connect to digital ground. (Analog signals have no ground reference; they are limited to V+ and V-.)
9	9	9	ADDA	Digital Address "A" Input
10	10	10	ADDB	Digital Address "B" Input
11	—	11	ADDC	Digital Address "C" Input
—	12, 15, 14, 11	—	NO0A–NO3A	Analog Switch "A" Inputs 0–3
—	13	4	COMA	Analog Switch "A" Common
—	—	12	NCC	Analog Switch "C" Normally Closed Input
—	—	13	NOC	Analog Switch "C" Normally Open Input
—	—	14	COMC	Analog Switch "C" Common
16	16	16	V+	Positive Analog and Digital Supply Voltage Input

Note: NO, NC, and COM pins are identical and interchangeable. Any may be considered an input or output; signals pass equally well in both directions.

Table 1. Truth Table/Switch Programming

INH	ADDRESS BITS			ON SWITCHES		
	ADDC*	ADDB	ADDA	MAX4051/ MAX4051A	MAX4052/ MAX4052A	MAX4053/ MAX4053A
1	X	X	X	All switches open	All switches open	All switches open
0	0	0	0	COM–NO0	COMB–NO0B, COMC–NO0C	COMA–NCA, COMB–NCB, COMC–NCC
0	0	0	1	COM–NO1	COMB–NO1B, COMC–NO1C	COMA–NOA, COMB–NCB, COMC–NCC
0	0	1	0	COM–NO2	COMB–NO2B, COMC–NO2C	COMA–NCA, COMB–NOB, COMC–NCC
0	0	1	1	COM–NO3	COMB–NO3B, COMC–NO3C	COMA–NOA, COMB–NOB, COMC–NCC
0	1	0	0	COM–NO4	COMB–NO0B, COMC–NO0C	COMA–NCA, COMB–NCB, COMC–NOC
0	1	0	1	COM–NO5	COMB–NO1B, COMC–NO1C	COMA–NOA, COMB–NCB, COMC–NOC
0	1	1	0	COM–NO6	COMB–NO2B, COMC–NO2C	COMA–NCA, COMB–NOB, COMC–NOC
0	1	1	1	COM–NO7	COMB–NO3B, COMC–NO3C	COMA–NOA, COMB–NOB, COMC–NOC

X = Don't care * ADDC not present on MAX4052.

Note: NO and COM pins are identical and interchangeable. Either may be considered an input or output; signals pass equally well in either direction.

Applications Information

Power-Supply Considerations

Overview

The MAX4051/MAX4052/MAX4053 and MAX4051A/MAX4052A/MAX4053A construction is typical of most CMOS analog switches. They have three supply pins: V+, V-, and GND. V+ and V- are used to drive the internal CMOS switches and set the limits of the analog voltage on any switch. Reverse ESD-protection diodes are internally connected between each analog signal pin and both V+ and V-. If any analog signal exceeds V+ or V-, one of these diodes will conduct. During normal operation, these (and other) reverse-biased ESD diodes leak, forming the only current drawn from V+ or V-.

Virtually all the analog leakage current comes from the ESD diodes. Although the ESD diodes on a given signal pin are identical, and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or V- and the analog signal. This means their leakages will vary as the signal varies. The *difference* in the two diode leakages to the V+ and V- pins constitutes the analog signal path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of either the same or opposite polarity.

There is no connection between the analog signal paths and GND.

Low-Voltage, CMOS Analog Multiplexers/Switches

V+ and GND power the internal logic and logic-level translators, and set both the input and output logic limits. The logic-level translators convert the logic levels into switched V+ and V- signals to drive the gates of the analog signals. This drive signal is the only connection between the logic supplies (and signals) and the analog supplies. V+ and V- have ESD-protection diodes to GND.

The logic-level thresholds are TTL/CMOS compatible when V+ is +5V. As V+ rises, the threshold increases slightly, so when V+ reaches +12V, the threshold is about 3.1V; above the TTL-guaranteed high-level minimum of 2.8V, but still compatible with CMOS outputs.

Bipolar Supplies

These devices operate with bipolar supplies between ±3.0V and ±8V. The V+ and V- supplies need not be symmetrical, but their sum cannot exceed the absolute maximum rating of +17V.

Single Supply

These devices operate from a single supply between +3V and +16V when V- is connected to GND. All of the bipolar precautions must be observed. At room temperature, they actually "work" with a single supply at near or below +1.7V, although as supply voltage decreases, switch on-resistance and switching times become very high.

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the devices. Always sequence V+ on first, then V-, followed by the logic inputs (NO) and by COM. If power-supply sequencing is not possible, add two small signal diodes (D1, D2) in series with the supply pins for overvoltage protection (Figure 1).

Adding diodes reduces the analog signal range to one diode drop below V+ and one diode drop above V-, but does not affect the devices' low switch resistance and low leakage characteristics. Device operation is unchanged, and the difference between V+ and V- should not exceed 17V. These protection diodes are not recommended when using a single supply if signal levels must extend to ground.

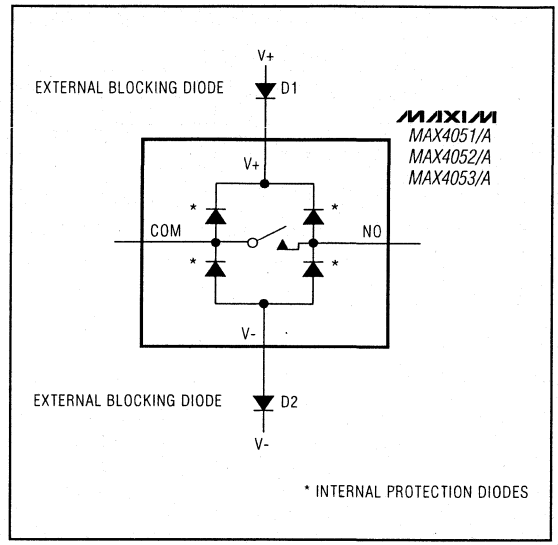
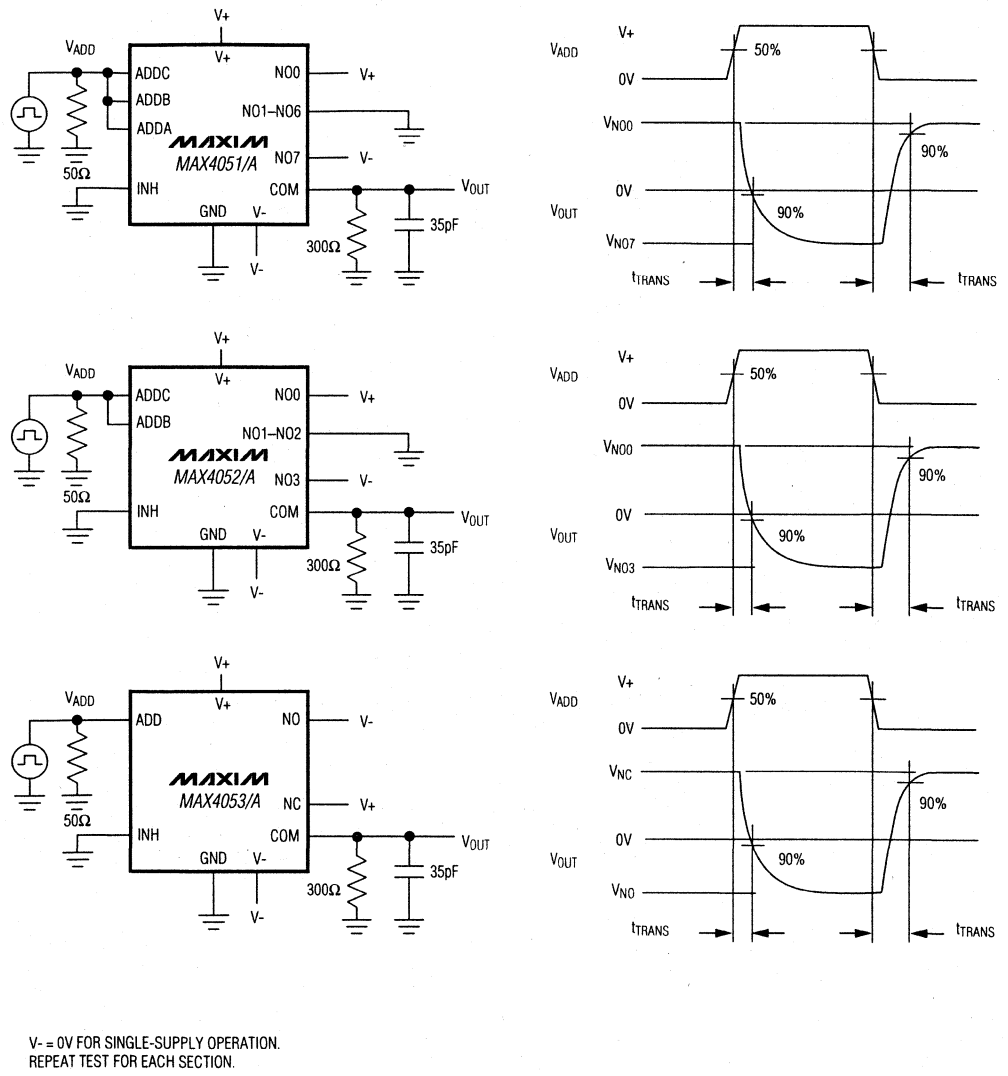


Figure 1. Overvoltage Protection Using External Blocking Diodes

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat up to 50MHz (see *Typical Operating Characteristics*). Above 20MHz, the on response has several minor peaks which are highly layout dependent. The problem is not turning the switch on, but turning it off. The off-state switch acts like a capacitor, and passes higher frequencies with less attenuation. At 10MHz, off isolation is about -45dB in 50Ω systems, becoming worse (approximately 20dB per decade) as frequency increases. Higher circuit impedances also make off isolation worse. Adjacent channel attenuation is about 3dB above that of a bare IC socket, and is entirely due to capacitive coupling.

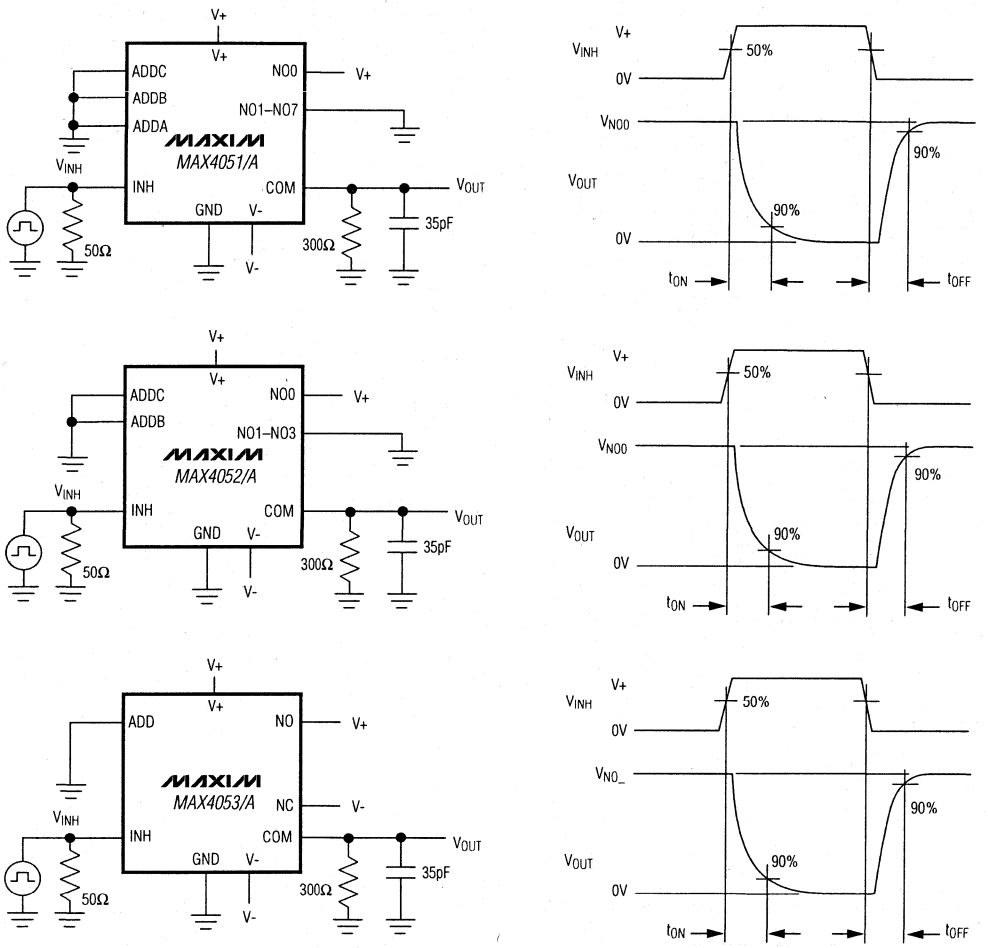
Test Circuits/Timing Diagrams



V- = 0V FOR SINGLE-SUPPLY OPERATION.
REPEAT TEST FOR EACH SECTION.

Figure 2. Address Transition Time

Low-Voltage, CMOS Analog Multiplexers/Switches



V- = 0V FOR SINGLE-SUPPLY OPERATION.
REPEAT TEST FOR EACH SECTION.

Figure 3. Enable Switching Time

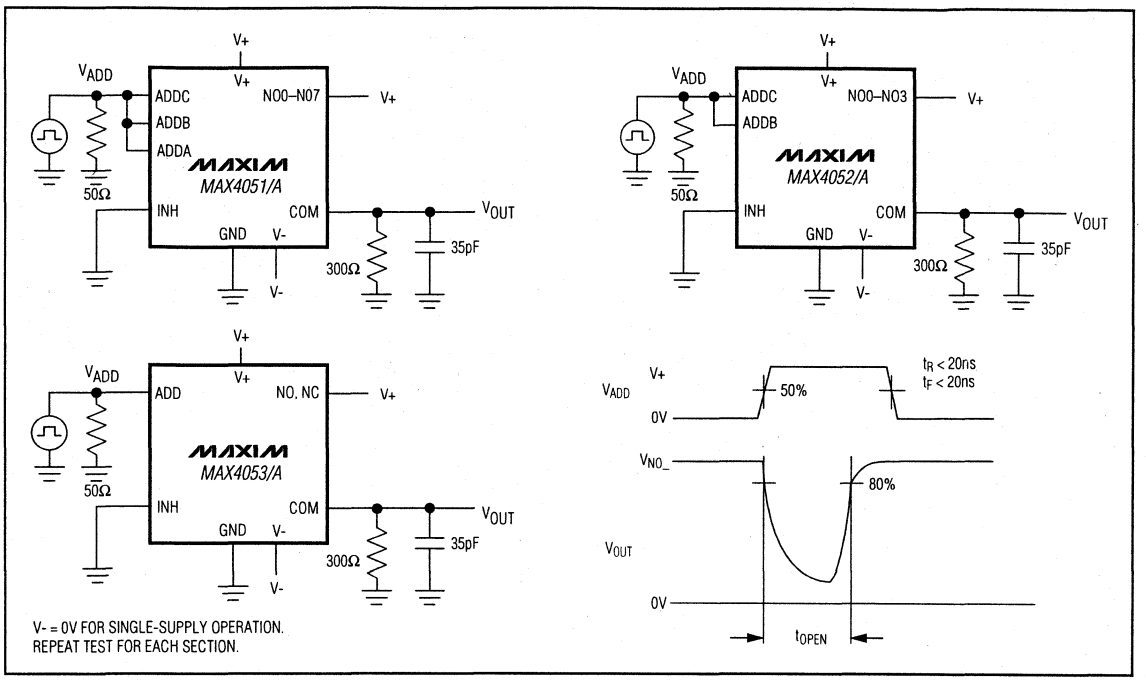


Figure 4. Break-Before-Make Interval

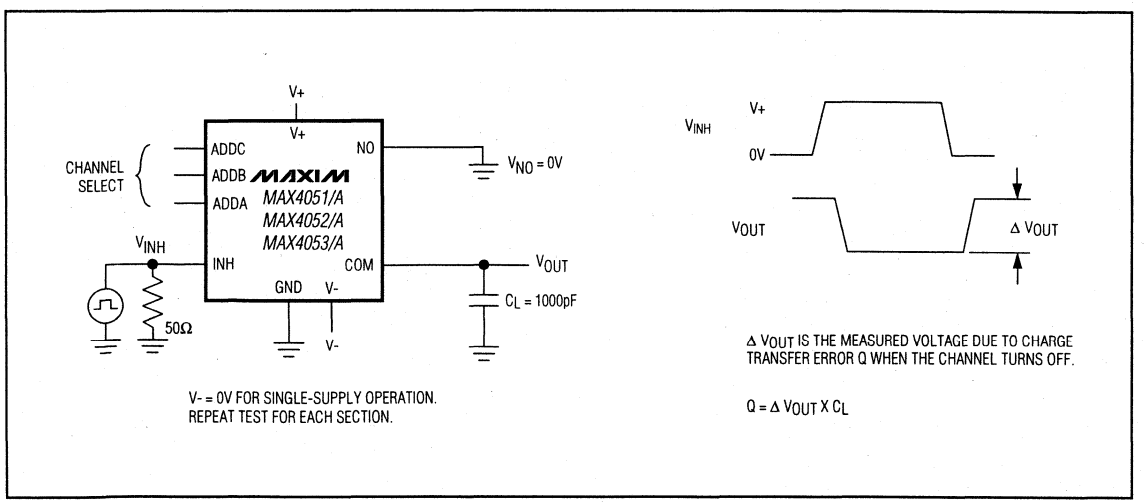


Figure 5. Charge Injection

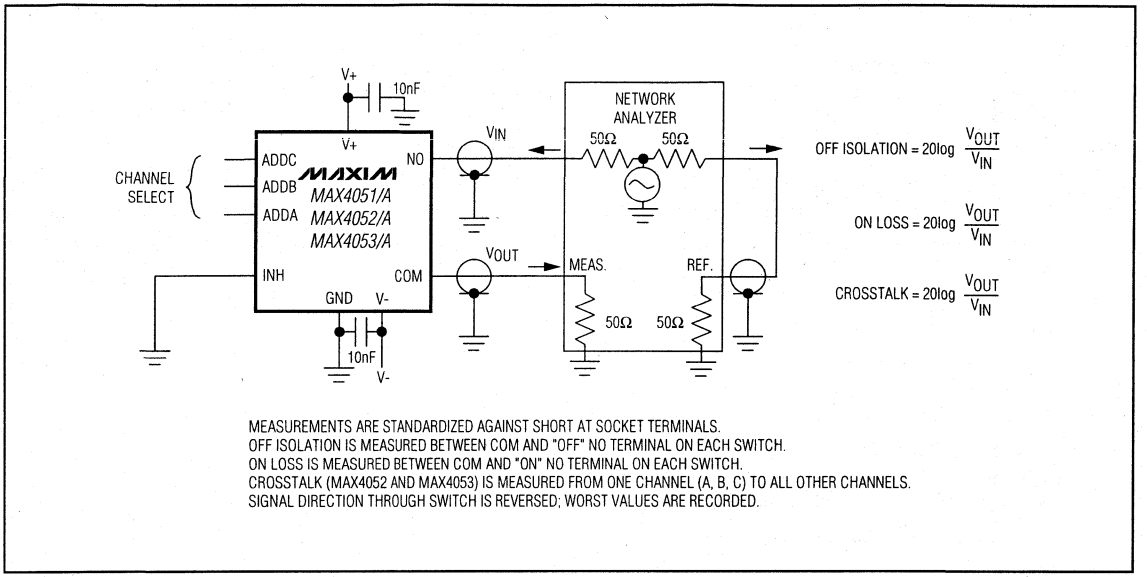


Figure 6. Off Isolation, On Loss, and Crosstalk

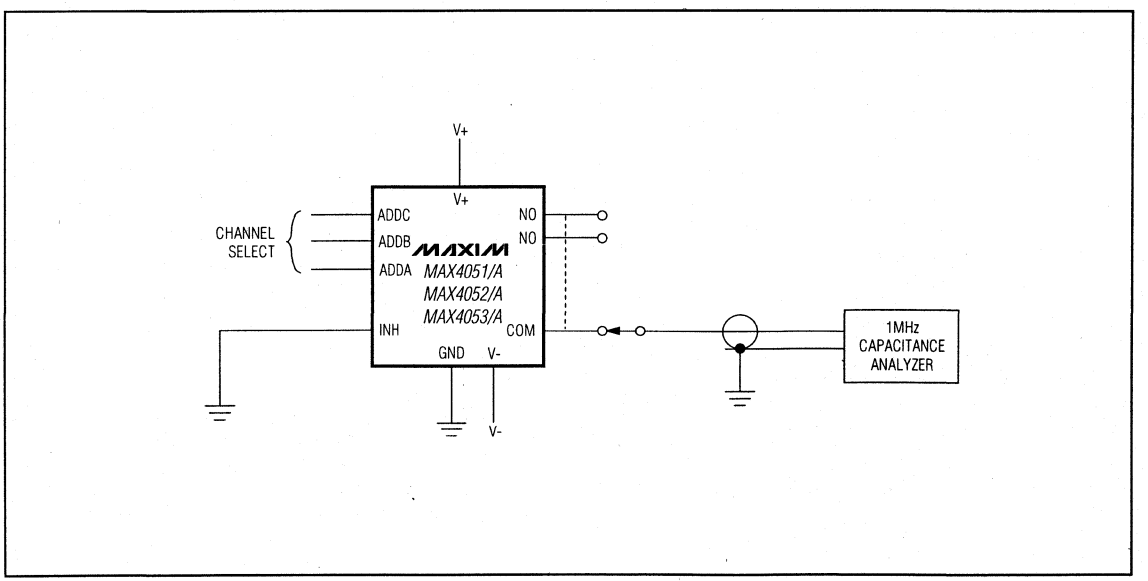


Figure 7. NO/COM Capacitance

Low-Voltage, CMOS Analog Multiplexers/Switches

Ordering Information (continued)

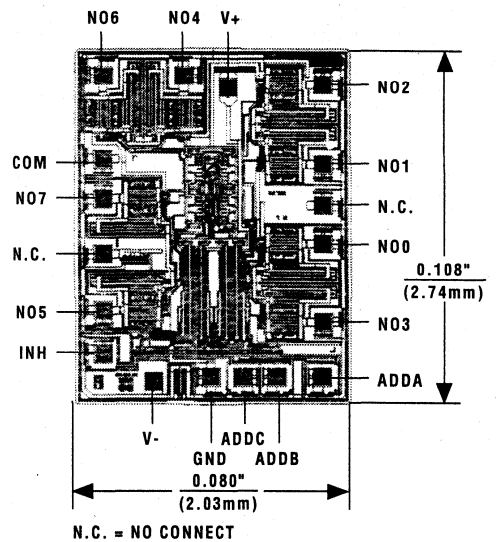
PART	TEMP. RANGE	PIN-PACKAGE
MAX4051AEPE	-40°C to +85°C	16 Plastic DIP
MAX4051AESE	-40°C to +85°C	16 Narrow SO
MAX4051AEEE	-40°C to +85°C	16 QSOP
MAX4051AMJE	-55°C to +125°C	16 CERDIP**
MAX4051CPE	0°C to +70°C	16 Plastic DIP
MAX4051CSE	0°C to +70°C	16 Narrow SO
MAX4051CEE	0°C to +70°C	16 QSOP
MAX4051C/D	0°C to +70°C	Dice*
MAX4051EPE	-40°C to +85°C	16 Plastic DIP
MAX4051ESE	-40°C to +85°C	16 Narrow SO
MAX4051EEE	-40°C to +85°C	16 QSOP
MAX4051MJE	-55°C to +125°C	16 CERDIP**
MAX4052ACPE	0°C to +70°C	16 Plastic DIP
MAX4052ACSE	0°C to +70°C	16 Narrow SO
MAX4052ACEE	0°C to +70°C	16 QSOP
MAX4052AEPE	-40°C to +85°C	16 Plastic DIP
MAX4052AESE	-40°C to +85°C	16 Narrow SO
MAX4052AEEE	-40°C to +85°C	16 QSOP
MAX4052AMJE	-55°C to +125°C	16 CERDIP**
MAX4052CPE	0°C to +70°C	16 Plastic DIP
MAX4052CSE	0°C to +70°C	16 Narrow SO
MAX4052CEE	0°C to +70°C	16 QSOP
MAX4052C/D	0°C to +70°C	Dice*
MAX4052EPE	-40°C to +85°C	16 Plastic DIP
MAX4052ESE	-40°C to +85°C	16 Narrow SO
MAX4052EEE	-40°C to +85°C	16 QSOP
MAX4052MJE	-55°C to +125°C	16 CERDIP**

PART	TEMP. RANGE	PIN-PACKAGE
MAX4053ACPE	0°C to +70°C	16 Plastic DIP
MAX4053ACSE	0°C to +70°C	16 Narrow SO
MAX4053ACEE	0°C to +70°C	16 QSOP
MAX4053AEPE	-40°C to +85°C	16 Plastic DIP
MAX4053AESE	-40°C to +85°C	16 Narrow SO
MAX4053AEEE	-40°C to +85°C	16 QSOP
MAX4053AMJE	-55°C to +125°C	16 CERDIP**
MAX4053CPE	0°C to +70°C	16 Plastic DIP
MAX4053CSE	0°C to +70°C	16 Narrow SO
MAX4053CEE	0°C to +70°C	16 QSOP
MAX4053C/D	0°C to +70°C	Dice*
MAX4053EPE	-40°C to +85°C	16 Plastic DIP
MAX4053ESE	-40°C to +85°C	16 Narrow SO
MAX4053EEE	-40°C to +85°C	16 QSOP
MAX4053MJE	-55°C to +125°C	16 CERDIP**

** Contact factory for dice specifications.*
*** Contact factory for availability.*

Chip Topography

MAX4051/A

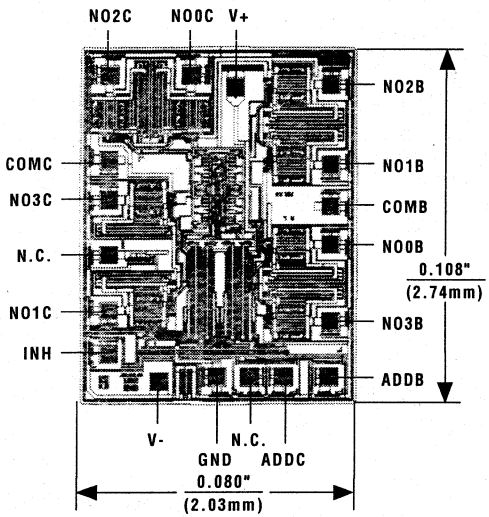


TRANSISTOR COUNT: 161
SUBSTRATE CONNECTED TO V+.

Low-Voltage, CMOS Analog Multiplexers/Switches

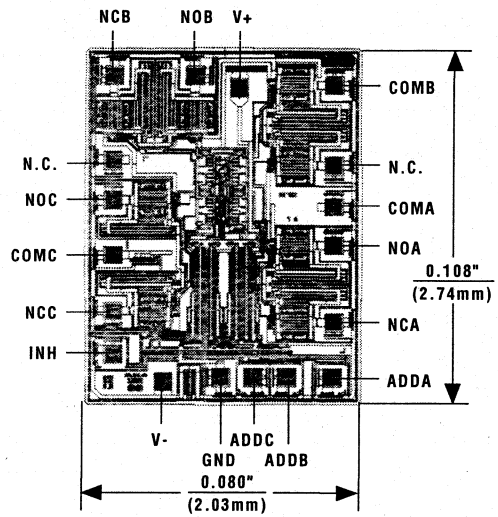
Chip Topographies (continued)

MAX4052/A



TRANSISTOR COUNT: 161
SUBSTRATE CONNECTED TO V+.

MAX4053/A



TRANSISTOR COUNT: 161
SUBSTRATE CONNECTED TO V+.

19-1062; Rev 0; 6/96

MAXIM

Low-Voltage, SPST, CMOS Analog Switches

General Description

The MAX4501/MAX4502 are single-pole/single-throw (SPST), low-voltage, single-supply, CMOS analog switches. The MAX4501 is normally open (NO). The MAX4502 is normally closed (NC).

These CMOS switches can operate continuously with a single supply between +2V and +12V. Each switch can handle rail-to-rail analog signals. The off-leakage current is only 1.0nA at +25°C or 10nA at +85°C.

The digital input has 0.8V and 2.4V logic thresholds, ensuring TTL/CMOS-logic compatibility when using a single +5V supply.

Features

- ♦ **Available in SOT23-5 Package**
- ♦ **+2V to +12V Single-Supply Operation**
- ♦ **Guaranteed On-Resistance: 250Ω at +5V**
- ♦ **Guaranteed Low Off-Leakage Current:**
  1nA at +25°C
  10nA at +85°C
- ♦ **Guaranteed Low On-Leakage Current:**
  2nA at +25°C
  20nA at +85°C
- ♦ **Low Charge Injection: 10pC**
- ♦ **Fast Switching Speed: t_{ON} = 75ns, t_{OFF} = 50ns**
- ♦ **TTL/CMOS-Logic Compatible with +5V Supply**

Applications

Battery-Operated Equipment

Audio and Video Signal Routing

Low-Voltage Data-Acquisition Systems

Communications Circuits

PCMCIA Cards

Cellular Phones

Modems

Ordering Information

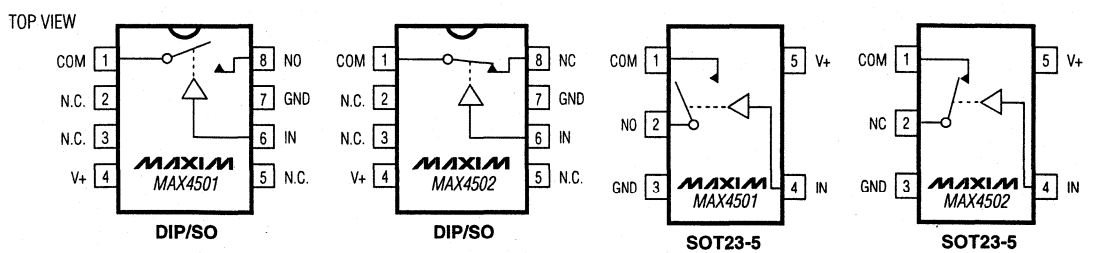
PART	TEMP. RANGE	PIN-PACKAGE
MAX4501CPA	0°C to +70°C	8 Plastic DIP
MAX4501CSA	0°C to +70°C	8 SO
MAX4501CUK	0°C to +70°C	5 SOT23-5
MAX4501C/D	0°C to +70°C	Dice*
MAX4501EPA	-40°C to +85°C	8 Plastic DIP
MAX4501ESA	-40°C to +85°C	8 SO
MAX4501EUK	-40°C to +85°C	5 SOT23-5
MAX4501MJA	-55°C to +125°C	8 CERDIP**

Ordering Information continued at end of data sheet.

** Contact factory for dice specifications.*

*** Contact factory for availability.*

Pin Configurations/Functional Diagrams/Truth Table



INPUT	SWITCH STATE	
	MAX4501	MAX4502
LOW	OFF	ON
HIGH	ON	OFF

MARKING INFORMATION SOTs ONLY
XX XX → LOT SPECIFIC CODE
AA = MAX4501
AB = MAX4502

N.C. = NOT INTERNALLY CONNECTED

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Low-Voltage, SPST, CMOS Analog Switches

ABSOLUTE MAXIMUM RATINGS

(Voltages Referenced to GND)
V+ .....-0.3V, +13V
Voltage into Any Terminal (Note 1).....-0.3V to (V+ + 0.3V)
or ±10mA (whichever occurs first)
Continuous Current into Any Terminal.....±10mA
Peak Current, NO_ or COM_
(pulsed at 1ms,10% duty cycle).....±20mA
ESD per Method 3015.7 .....>2000V
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C).....471mW
SOT23-5 (derate 7.1mW/°C above +70°C).....571mW
CERDIP (derate 8.00mW/°C above +70°C).....640mW
Operating Temperature Ranges
MAX4501C_ _/MAX4502C_ _ .....0°C to +70°C
MAX4501E_ _/MAX4502E_ _ .....-40°C to +85°C
MAX4501MJA/MAX4502MJA .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: Voltages exceeding V+ or GND on any signal terminal are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—+5V Supply

(V+ = +4.5V to +5.5V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	V_{COM}, V_{NO}, V_{NC}				0		V+	V
COM to NO or NC On-Resistance	R_{ON}	V_{COM} = 3.5V, I_{COM} = 1mA	T_A = +25°C			90	250	Ω
			T_A = T_{MIN} to T_{MAX}				350	
NO or NC Off-Leakage Current (Note 3)	$I_{NO(OFF)}$, $I_{NC(OFF)}$	V+ = 5.5V, V_{COM} = 1V, V_{NO} or V_{NC} = 4.5V	T_A = +25°C		-1	0.01	1	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-10		10	
				M	-100		100	
COM Off-Leakage Current (Note 3)	$I_{COM(OFF)}$	V+ = 5.5V, V_{COM} = 1V, V_{NO} or V_{NC} = 4.5V	T_A = +25°C		-1	0.01	1	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-10		10	
				M	-100		100	
COM On-Leakage Current (Note 3)	$I_{COM(ON)}$	V+ = 5.5V, V_{COM} = 1V, V_{NO} or V_{NC} = 4.5V	T_A = +25°C		-2	0.01	2	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-20		20	
				M	-200		200	
DIGITAL I/O								
Input Logic High	V_{IH}				2.4		V+	V
Input Logic Low	V_{IL}				0		0.8	V
Input Current Logic High or Low	I_{IH}, I_{IL}	V_{IN} = V+, 0V			-1	0.03	1	µA
SWITCH DYNAMIC CHARACTERISTICS								
Turn-On Time	t_{ON}	V_{NO} = V_{NC} = 1.5V, V_{IN} = 3V, R_L = 1kΩ Figure 1	T_A = +25°C			16	75	ns
			T_A = T_{MIN} to T_{MAX}				150	
Turn-Off Time	t_{OFF}	V_{NO} = V_{NC} = 1.5V, V_{IN} = 3V, R_L = 1kΩ Figure 1	T_A = +25°C			10	50	ns
			T_A = T_{MIN} to T_{MAX}				150	

ELECTRICAL CHARACTERISTICS—+5V Supply (continued)

(V+ = +4.5V to +5.5V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SWITCH DYNAMIC CHARACTERISTICS (continued)							
Charge Injection (Note 4)	Q	C_L = 1nF, V_{NO} = 0V, R_S = 0Ω, T_A = +25°C, Figure 2			1	10	pC
Off Isolation	V_{ISO}	R_L = 50Ω, C_L = 15pF, V_{NO} = $1V_{RMS}$, f = 100kHz, T_A = +25°C, Figure 3			< -100		dB
NO or NC Off Capacitance	$C_{NO(OFF)}$, $C_{NC(OFF)}$	f = 1MHz, Figure 4			3		pF
COM Off Capacitance	$C_{COM(OFF)}$	f = 1MHz, Figure 4			3		pF
COM On Capacitance	$C_{COM(ON)}$	f = 1MHz, Figure 4			8		pF
POWER SUPPLY							
V+ Supply Current	I+	V_{IN} = 0V or V+	T_A = +25°C	-1		1	µA
			T_A = T_{MIN} to T_{MAX}	-10		10	

ELECTRICAL CHARACTERISTICS—+12V Supply

(V+ = +11.4V to +12.6V, V_{INH} = 5.0V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	V_{COM}, V_{NO}, V_{NC}				0		V+	V
COM to NO or NC On-Resistance	R_{ON}	V_{COM} = 10V, I_{COM} = 1mA	T_A = +25°C			40	160	Ω
			T_A = T_{MIN} to T_{MAX}				200	
NO or NC Off-Leakage Current (Note 3)	$I_{NO(OFF)}$, $I_{NC(OFF)}$	V_{COM} = 10V, V_{NO} or V_{NC} = 1V	T_A = +25°C		-5		5	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-50		50	
				M	-500		500	
COM Off-Leakage Current (Note 3)	$I_{COM(OFF)}$	V_{COM} = 10V, V_{NO} or V_{NC} = 1V	T_A = +25°C		-5		5	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-50		50	
				M	-500		500	
COM On-Leakage Current (Note 3)	$I_{COM(ON)}$	V_{COM} = 10V	T_A = +25°C		-10		10	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-100		100	
				M	-1000		1000	
DIGITAL I/O								
Input Logic High	V_{INH}				5.0		V+	V
Input Logic Low	V_{INL}				0		0.8	V
Input Current Logic High or Low	I_{INH}, I_{INL}	V_{IN} = V+, 0V			-1	0.03	1	µA
POWER SUPPLY								
V+ Supply Current	I+	IN = 0V or V+	T_A = +25°C		-1		1	µA
			T_A = T_{MIN} to T_{MAX}		-10		10	

ELECTRICAL CHARACTERISTICS—+3V Supply

(V+ = +3.0V to +3.6V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	V_{COM}, V_{NO}, V_{NC}			0		V+	V
COM to NO or NC On-Resistance	R_{ON}	V_{COM} = 1.5V, I_{NO} = 0.1mA	T_A = +25°C		175	600	Ω
			$T_A = T_{MIN}$ to T_{MAX}			800	
DIGITAL I/O							
Input Logic High	V_{INH}			2.4		V+	V
Input Logic Low	V_{INL}			0		0.8	V
Input Current Logic High or Low	I_{INH}, I_{INL}	V_{IN} = V+, 0V		-1.00	0.03	1.00	µA
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On-Time (Note 4)	t_{ON}	$V_{NO} = V_{NC}$ = 1.5V, V_{IN} = 3V, R_L = 1kΩ Figure 1	T_A = +25°C		45	300	ns
			$T_A = T_{MIN}$ to T_{MAX}			500	
Turn-Off-Time (Note 4)	t_{OFF}	$V_{NO} = V_{NC}$ = 1.5V, V_{IN} = 3V, R_L = 1kΩ Figure 1	T_A = +25°C		10	125	ns
			$T_A = T_{MIN}$ to T_{MAX}			175	
Charge Injection (Note 4)	Q	C_L = 1nF, T_A = +25°C, Figure 2			0.5	10	pC
POWER SUPPLY							
V+ Supply Current	I+	IN = 0V or V+	T_A = +25°C	-1		1	µA
			$T_A = T_{MIN}$ to T_{MAX}	-10		10	

Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Note 3: Leakage parameters are 100% tested at maximum-rated hot operating temperature, and are guaranteed by correlation at +25°C.

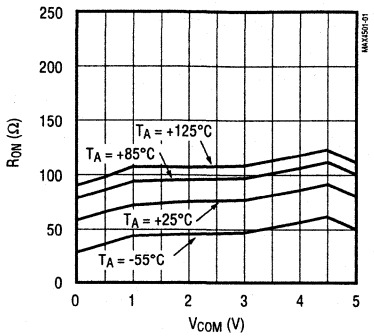
Note 4: Guaranteed, not production tested.

Note 5: SOT packaged parts are 100% tested at +25°C. Limits at maximum and minimum rated temperature are guaranteed by design and correlation limits at +25°C.

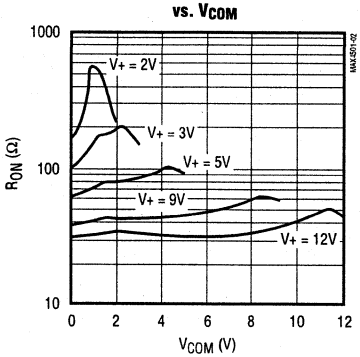
Typical Operating Characteristics

(V+ = 5V, GND = 0V, T_A = +25°C, unless otherwise noted.)

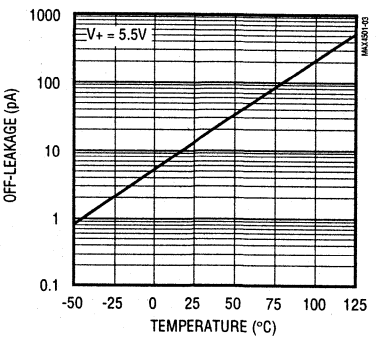
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE



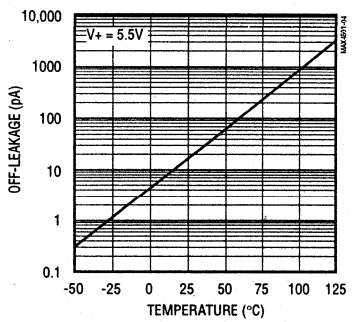
ON-RESISTANCE vs. V_{COM}



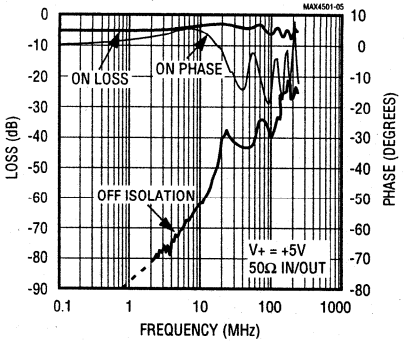
OFF-LEAKAGE vs. TEMPERATURE



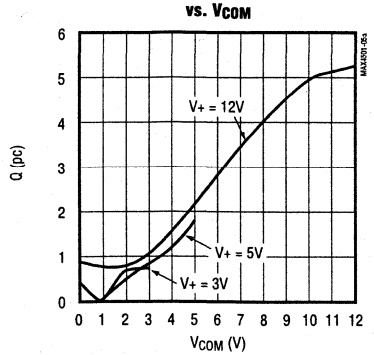
OFF-LEAKAGE vs. TEMPERATURE



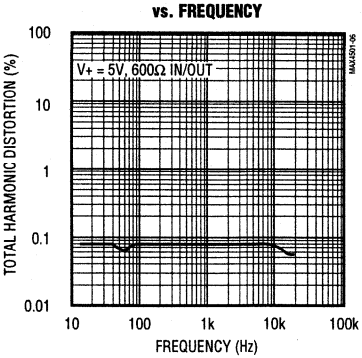
FREQUENCY RESPONSE



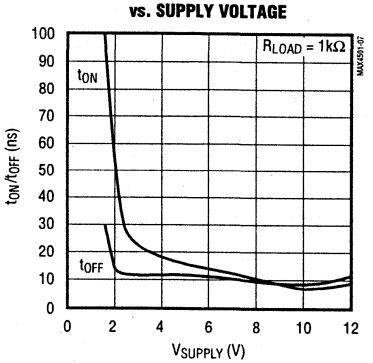
CHARGE INJECTION vs. V_{COM}



TOTAL HARMONIC DISTORTION vs. FREQUENCY



SWITCHING TIME vs. SUPPLY VOLTAGE



Low-Voltage, SPST, CMOS Analog Switches

Pin Description

PIN				NAME	FUNCTION
MAX4501		MAX4502			
DIP/SO	SOT23-5	DIP/SO	SOT23-5		
1	1	1	1	COM	Analog Switch Common Terminal
2, 3, 5	—	2, 3, 5	—	N.C.	No Connect (not internally connected)
4	5	4	5	V+	Positive Supply-Voltage Input (analog and digital)
6	4	6	4	IN	Digital Control Input
7	3	7	3	GND	Ground
8	2	—	—	NO	Analog Switch (normally open)
—	—	8	2	NC	Analog Switch (normally closed)

Note: NO, NC, and COM pins are identical and interchangeable. Any may be considered as an input or an output; signals pass equally well in both directions.

Applications Information

Power-Supply Considerations

The MAX4501/MAX4502 are constructed like most CMOS analog switches, except they have only two supply pins: V+ and GND. V+ and GND drive the internal CMOS switches and set the analog voltage limits of the switch. Reverse ESD-protection diodes are internally connected between each analog-signal pin and both V+ and GND. One of these diodes conducts if any analog signal exceeds V+ or GND. During normal operation, these and other reverse-biased ESD diodes leak, forming the only current drawn from V+ or GND.

Virtually all the analog leakage current comes from the ESD diodes. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or GND and the analog signal. This means their leakages will vary as the signal varies. The *difference* in the two diode leakages to the V+ and GND pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity.

There is no connection between the analog-signal paths and V+ or GND.

V+ and GND also power the internal logic and logic-level translators, and set both the input and output logic limits. The logic-level translators convert the logic levels to switched V+ and GND signals to drive the analog signal gates. This drive signal is the only connection between the logic supplies (and signals) and the analog supplies. COM, NO, and NC pins have ESD-protection diodes to V+ and GND.

The logic-level thresholds are CMOS/TTL-compatible when V+ is +5V. As V+ is raised, the threshold increases slightly. When V+ reaches +12V, the logic-level threshold is about 3V—above the TTL guaranteed high-level minimum of 2.8V, but still compatible with CMOS outputs.

Do not connect the MAX4501/MAX4502's V+ to +3V and then connect the logic-level pins to TTL logic-level signals. TTL levels can exceed +3V and violate the absolute maximum ratings, damaging the part and/or external circuits.

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat up to 250MHz (see *Typical Operating Characteristics*). Above 20MHz, the on response has several minor peaks which are highly layout dependent. The problem is not in turning the switch on; it's in turning it off. The off-state switch acts like a capacitor and passes higher frequencies with less attenuation. At 10MHz, off isolation is about -60dB in 50Ω systems, decreasing approximately 20dB per decade as frequency increases. Higher circuit impedances also cause off isolation to decrease. Adjacent channel attenuation is about 3dB above that of a bare IC socket, and is due entirely to capacitive coupling.

Test Circuits/Timing Diagrams

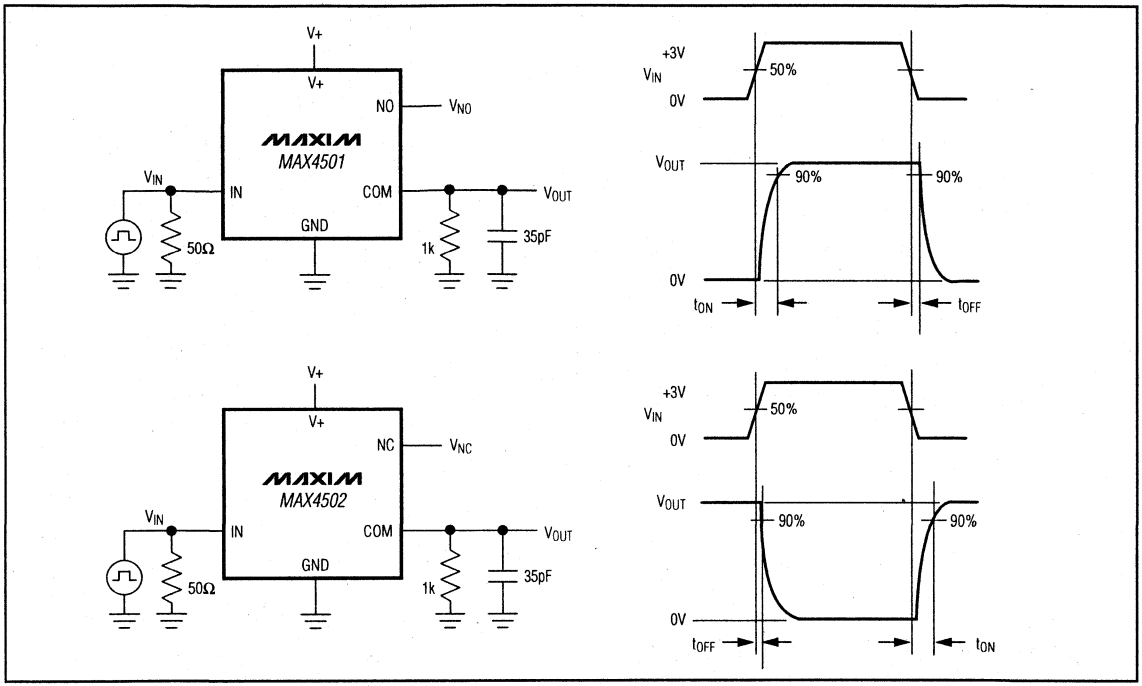


Figure 1. Switching Times

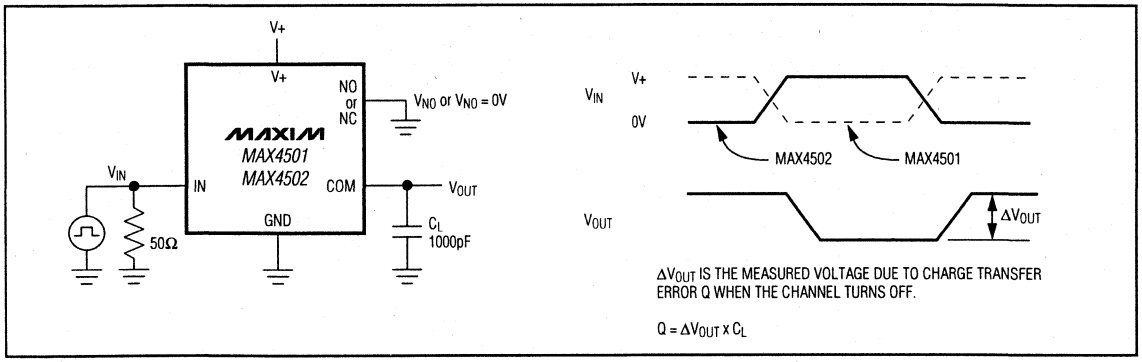


Figure 2. Charge Injection

Low-Voltage, SPST, CMOS Analog Switches

Test Circuits/Timing Diagrams (continued)

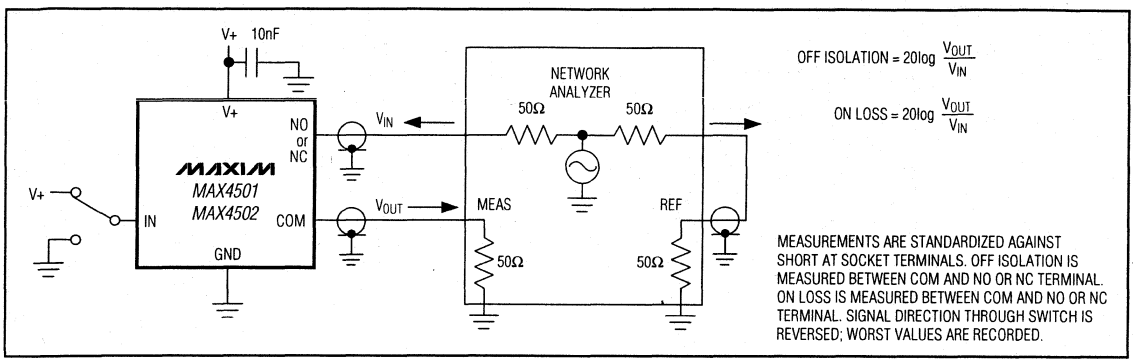


Figure 3. Off Isolation and On Loss

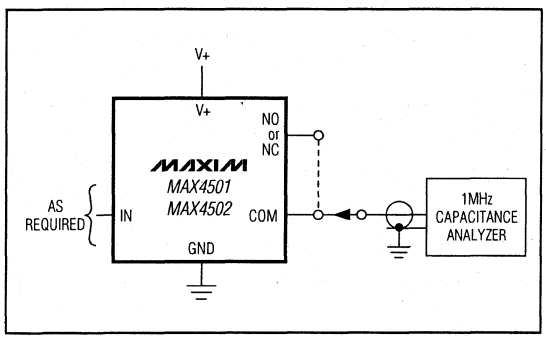
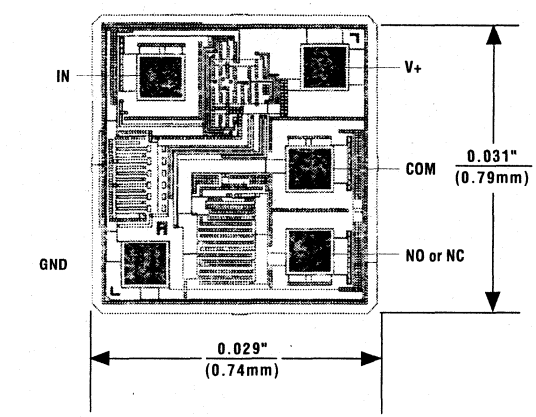


Figure 4. NO, NC, and COM Capacitance

Chip Topography



TRANSISTOR COUNT: 17

SUBSTRATE CONNECTED TO V+

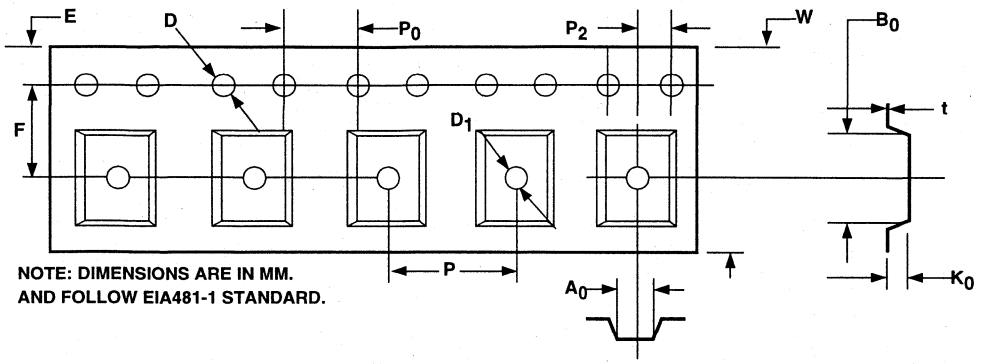
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX4502CPA	0°C to +70°C	8 Plastic DIP
MAX4502CSA	0°C to +70°C	8 SO
MAX4502CUK	0°C to +70°C	5 SOT23-5
MAX4502C/D	0°C to +70°C	Dice*
MAX4502EPA	-40°C to +85°C	8 Plastic DIP
MAX4502ESA	-40°C to +85°C	8 SO
MAX4502EUK	-40°C to +85°C	5 SOT23-5
MAX4502MJA	-55°C to +125°C	8 CERDIP**

** Contact factory for dice specifications.*

*** Contact factory for availability.*

Tape-and-Reel Information



NOTE: DIMENSIONS ARE IN MM.
AND FOLLOW EIA481-1 STANDARD.

A_0	3.200	±0.102
B_0	3.099	±0.102
D	1.499	+0.102 +0.000
D_1	0.991	+0.254 +0.000

E	1.753	±0.102
F	3.505	±0.051
K_0	1.397	±0.102
P	3.988	±0.102

P_0	3.988	±0.102
$P_0$10	40.005	±0.203
P_2	2.007	±0.051
t	0.254	±0.127
W	8.001	+0.305 -0.102

5 SOT23-5

19-1064; Rev 0; 6/96

MAXIM

Low-Voltage, Dual-Supply, SPST, CMOS Analog Switches

General Description

The MAX4503/MAX4504 are low-voltage, dual-supply, single-pole/single-throw (SPST), CMOS analog switches. The MAX4503 is normally open (NO). The MAX4504 is normally closed (NC).

These CMOS switches can operate continuously with dual supplies between ±1.V and ±6V. Each switch can handle rail-to-rail analog signals. The off-leakage current is only 1nA at +25°C or 10nA at +85°C.

The digital input is CMOS-logic compatible when using ±5V supplies. A unique logic input architecture allows this even though the parts have no ground pin.

For single-supply operation, use the MAX4501/MAX4502, which are pin-for-pin equivalents.

Features

- ♦ **Available in SOT23-5 Package**
- ♦ **Dual-Supply Operation from ±1V to ±6V**
- ♦ **Guaranteed On-Resistance:**
  250Ω with ±5V Supplies
- ♦ **Guaranteed Low Off-Leakage Currents:**
  1nA at +25°C
  10nA at +85°C
- ♦ **Guaranteed Low On-Leakage Currents:**
  2nA at +25°C
  20nA at +85°C
- ♦ **Guaranteed Low Charge Injection: 10pC Max**
- ♦ **Fast Switching Speed: t_{ON} = 150ns, t_{OFF} = 100ns**
- ♦ **CMOS-Logic Compatible Input**

Applications

Battery-Operated Equipment

Audio and Video Signal Routing

Low-Voltage Data-Acquisition Systems

Communications Circuits

Cellular Phones

PCMCIA Cards

Modems

Ordering Information

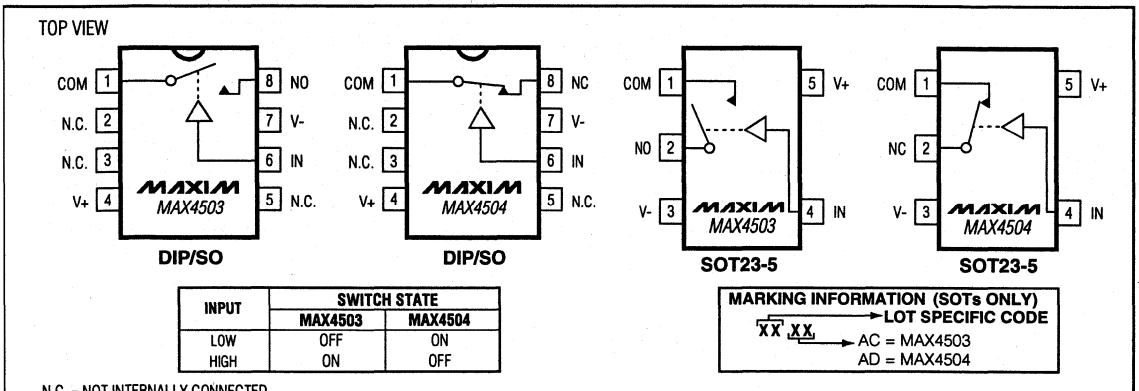
PART	TEMP. RANGE	PIN-PACKAGE
MAX4503CPA	0°C to +70°C	8 Plastic DIP
MAX4503CSA	0°C to +70°C	8 SO
MAX4503CUK	0°C to +70°C	5 SOT23-5
MAX4503C/D	0°C to +70°C	Dice*
MAX4503EPA	-40°C to +85°C	8 Plastic DIP
MAX4503ESA	-40°C to +85°C	8 SO
MAX4503EUK	-40°C to +85°C	5 SOT23-5
MAX4503MJA	-55°C to +125°C	8 CERDIP**

Ordering Information continued at end of data sheet.

** Contact factory for dice specifications.*

*** Contact factory for availability.*

Pin Configurations



INPUT	SWITCH STATE	
	MAX4503	MAX4504
LOW	OFF	ON
HIGH	ON	OFF

MARKING INFORMATION (SOTs ONLY)
XX XX → LOT SPECIFIC CODE
AC = MAX4503
AD = MAX4504

N.C. = NOT INTERNALLY CONNECTED

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Low-Voltage, Dual-Supply, SPST, CMOS Analog Switches

ABSOLUTE MAXIMUM RATINGS

(Voltages Referenced to V-)
V+ .....-0.3V, +13V
Voltage into Any Terminal (Note 1) .....-0.3V to (V+ + 0.3V) or ±10mA (whichever occurs first)
Continuous Current into Any Terminal .....±10mA
Peak Current, NO_ or COM_ (pulsed at 1ms,10% duty cycle) .....±20mA
Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) ...727mW
8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
5-Pin SOT23-5 (derate 7.1mW/°C above +70°C) 571mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C) 640mW
Operating Temperature Ranges
MAX4503C_ _/MAX4504C_ _ .....0°C to +70°C
MAX4503E_ _/MAX4504E_ _ .....-40°C to +85°C
MAX4503MJA/MAX4504MJA .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: Voltages on any signal terminal exceeding V+ or V- are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—±5V Supply

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, V_{INH} =3.5V, V_{INL} = 1.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	V_{COM}, V_{NO}, V_{NC}				V-		V+	V
COM to NO or NC On-Resistance	R_{ON}	$V_{COM_}$ = 3.5V, I_{COM} = 1mA	T_A = +25°C			60	250	Ω
			T_A = T_{MIN} to T_{MAX}				350	
NO or NC Off Leakage Current (Note 3)	$I_{NO(OFF)}$, $I_{NC(OFF)}$	V+ = 5.5V, V- = -5.5V, $V_{COM_}$ = ±4.5V, V_{NO} or V_{NC} = ∓4.5V	T_A = +25°C		-1	0.01	1	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-10		10	
				M	-100		100	
COM Off Leakage Current (Note 3)	$I_{COM(OFF)}$	V+ = 5.5V, V- = -5.5V, $V_{COM_}$ = ±4.5V, V_{NO} or V_{NC} = ∓4.5V	T_A = +25°C		-1	0.01	1	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-10		10	
				M	-100		100	
COM On Leakage Current (Note 3)	$I_{COM(ON)}$	V+ = 5.5V, V- = -5.5V, V_{COM} = ±4.5V, V_{NO} or V_{NC} = ±4.5V	T_A = +25°C		-2	0.01	2	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-20		20	
				M	-200		200	
DIGITAL I/O								
IN Input Logic High	V_{IH}				(V+) - 1.5		V+	V
IN Input Logic Low	V_{IL}				V-		(V+) - 3.5	V
IN Input Current Logic High or Low	I_{IH}, I_{IL}	V_{IN} = V+, 0V			-1	0.03	1	µA

ELECTRICAL CHARACTERISTICS—±5V Supply (continued)

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, V_{INH} = 3.5V, V_{INL} = 1.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	V_{IN} = 3V, R_L = 1kΩ, V_{NO} or V_{NC} = 3V, Figure 1	T_A = +25°C		30	150	ns
			T_A = T_{MIN} to T_{MAX}			240	
Turn-Off Time	t_{OFF}	V_{IN} = 3V, R_L = 1kΩ, V_{NO} or V_{NC} = 3V, Figure 1	T_A = +25°C		20	100	ns
			T_A = T_{MIN} to T_{MAX}			150	
Charge Injection (Note 4)	Q	C_L = 1nF, $V_{NO_}$ = 0V, R_S = 0Ω, T_A = +25°C, Figure 2			1	10	pC
Off Isolation	V_{ISO}	R_L = 50Ω, C_L = 15pF, V_{NO} = $1V_{RMS}$, f = 100kHz, T_A = +25°C, Figure 3			<-90		dB
NO or NC Off Capacitance	$C_{NO(OFF)}$	f = 1MHz, T_A = +25°C, Figure 4			3		pF
COM Off Capacitance	$C_{OFF(COM)}$	f = 1MHz, T_A = +25°C, Figure 4			3		pF
COM On Capacitance	$C_{ON(COM)}$	f = 1MHz, T_A = +25°C, Figure 4			9		pF
POWER SUPPLY							
V+, V- Supply Current	I+, I-	V_{IN} = 0V or V+	T_A = +25°C	-125	40	125	µA
			T_A = T_{MIN} to T_{MAX}	-200		200	

Low-Voltage, Dual-Supply, SPST, CMOS Analog Switches

ELECTRICAL CHARACTERISTICS—±3V Supply

(V+ = +2.7V to +3.3V, V- = -2.7V to -3.3V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

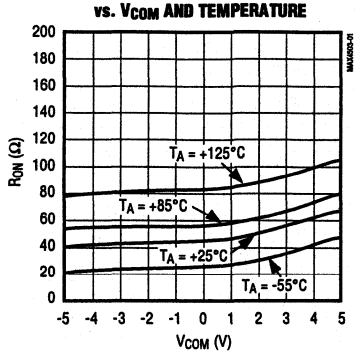
PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	V_{COM}, V_{NO}, V_{NC}				0		V+	V
COM to NO or NC On-Resistance	R_{ON}	$V_{COM_}$ = 1.5V, I_{COM} = 0.1mA	T_A = +25°C			100	400	Ω
			T_A = T_{MIN} to T_{MAX}				500	
NO or NC Off Leakage Current (Notes 3, 4)	$I_{NO(OFF)}$, $I_{NC(OFF)}$	$V_{COM_}$ = ±1.5V, V_{NO} or V_{NC} = ∓1.5V, V+ = 3.3V, V- = -3.3V	T_A = +25°C		-1		1	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-10		10	
				M	-100		100	
COM Off Leakage Current (Notes 3, 4)	$I_{COM(OFF)}$	$V_{COM_}$ = ±1.5V, V_{NO} or V_{NC} = ∓1.5V, V+ = 3.3V, V- = -3.3V	T_A = +25°C		-1		1	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-10		10	
				M	-100		100	
COM On Leakage Current (Notes 3, 4)	$I_{COM(ON)}$	V_{NO} or V_{NC} = ±1.5V, $V_{COM_}$ = ±1.5V, V+ = 3.3V, V- = -3.3V	T_A = +25°C		-2		2	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-20		20	
				M	-200		200	
DIGITAL I/O								
IN Input Logic High	V_{INH}				2.4		V+	V
IN Input Logic Low	V_{INL}				V-		(V+) - 2.3	V
IN Input Current Logic High or Low	I_{IH}, I_{IL}				-1	0.03	1	µA
POWER SUPPLY								
V+, V- Supply Current	I+, I-	IN = 0V or V+	T_A = +25°C		-100	25	100	µA
			T_A = T_{MIN} to T_{MAX}		-175		175	

Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.
Note 4: Guaranteed, not production tested.
Note 3: Leakage parameters are 100% tested at maximum rated hot operating temperature, and guaranteed by correlation at +25°C.
Note 5: SOT packaged parts are 100% tested at +25°C. Limits at maximum and minimum rated temperature are guaranteed by design and correlation limits at +25°C.

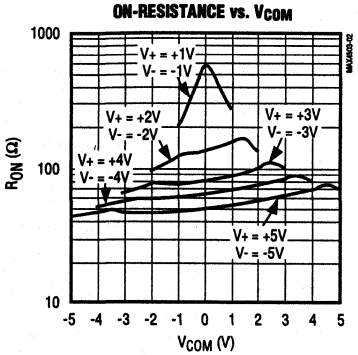
Typical Operating Characteristics

(V+ = +5V, V- = -5V, T_A = +25°C, unless otherwise noted.)

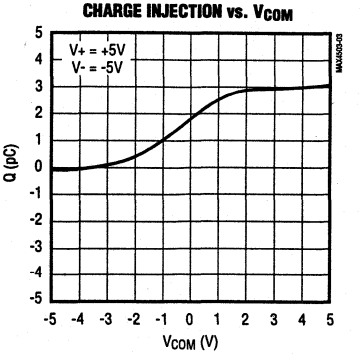
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE



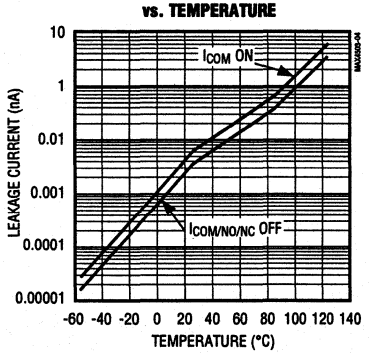
ON-RESISTANCE vs. V_{COM}



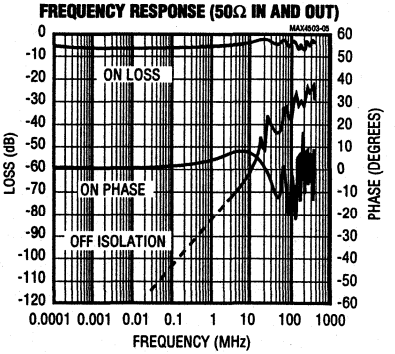
CHARGE INJECTION vs. V_{COM}



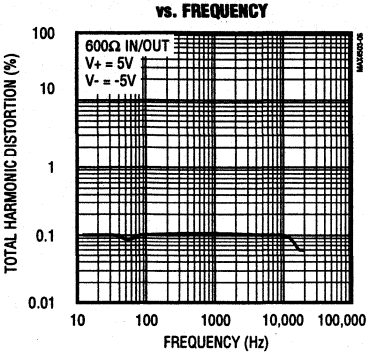
LEAKAGE CURRENT vs. TEMPERATURE



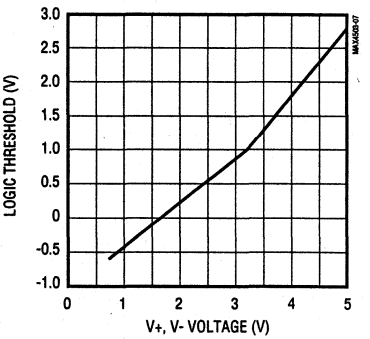
FREQUENCY RESPONSE (50Ω IN AND OUT)



TOTAL HARMONIC DISTORTION vs. FREQUENCY



LOGIC THRESHOLD vs. V+ AND V-



Low-Voltage, Dual-Supply, SPST, CMOS Analog Switches

Pin Description

PIN				NAME	FUNCTION
MAX4503		MAX4504			
DIP/SO	SOT23-5	DIP/SO	SOT23-5		
1	1	1	1	COM	Analog Switch Common Terminal
2, 3, 5	–	2, 3, 5	–	N.C.	No Connect (not internally connected)
4	5	4	5	V+	Positive (analog and digital) Supply Voltage Input
6	4	6	4	IN	Digital Control Input
7	3	7	3	V-	Negative (analog) Supply Voltage Input
8	2	–	–	NO	Analog Switch Normally Open Terminal
–	–	8	2	NC	Analog Switch Normally Closed Terminal

Note: NO, NC, and COM pins are identical and interchangeable. Either may be considered as an input or output; signals pass equally well in both directions.

Applications Information

Power-Supply Considerations

The MAX4503/MAX4504's construction is typical of most CMOS analog switches, except they have only two supply pins: V+ and V-. These voltages set the analog voltage limits of the switch. Reverse ESD-protection diodes are internally connected between IN and each analog signal pin and both V+ and V-. If any analog signal exceeds V+ or V-, one of these diodes will conduct. During normal operation, these (and other) reverse-biased ESD diodes leak, forming the only current drawn from V-. Additional current flows through V+ from the logic-level translator.

Virtually all the analog leakage current is provided through the ESD diodes. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or V- and the analog signal. This means their leakages will vary as the signal varies. The *difference* in the two diode leakages to the V+ and V- pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of either the same or opposite polarity.

There is no connection between the analog signal paths and V+ or V-.

V+ and V- also power the internal logic and logic-level translators. Since there is no ground pin, the logic input has a low-current pull-up to V+ and the logic limit is set by an internal comparator referenced to V+. The logic-level translators convert the logic levels to switched V+ and V- signals, to drive the gates of the analog signals. This drive signal is the only connection between the logic supplies (and signals) and the analog supplies. COM, NO, and NC pins have ESD-protection diodes to V+ and V-.

The logic is CMOS compatible when V+ is +5V. CMOS compatibility is maintained with all V+ values, assuming that the CMOS logic is operated from the same V+ supply. Since the MAX4503/MAX4504 have no ground pins, the logic levels are internally referenced to V+.

Do not connect the MAX4503/MAX4504 V+ to +3V and connect the logic-level pins to TTL-logic-level signals. TTL levels can exceed +3V and violate the absolute maximum ratings, damaging the part and/or external circuits.

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat up to 50MHz. (see *Typical Operating Characteristics*). Above 20MHz the on-response has several minor peaks which are highly layout dependent. The problem is not in turning the switch on, but in turning it off. The off-state switch acts like a capacitor, and passes higher frequencies with less attenuation. At 10MHz, off isolation is about -65dB in 50Ω systems, becoming worse (approximately 20dB per decade) as frequency increases. Higher circuit impedances also make off isolation worse.

Test Circuits/Timing Diagrams

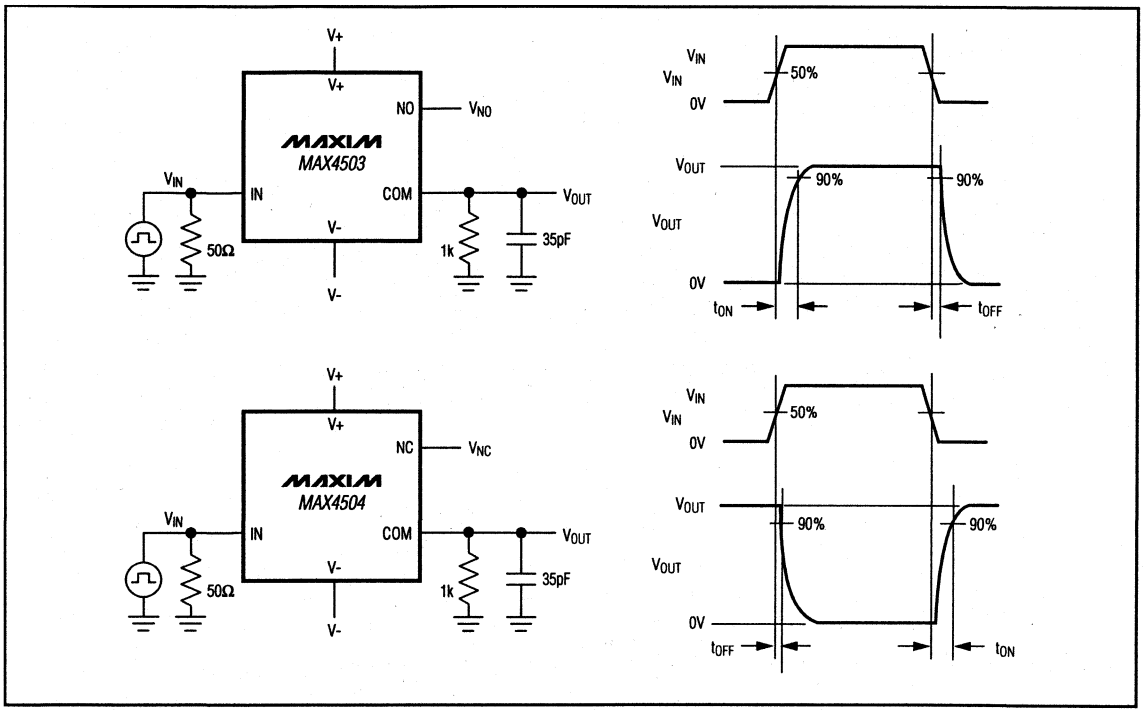


Figure 1. Switching Times

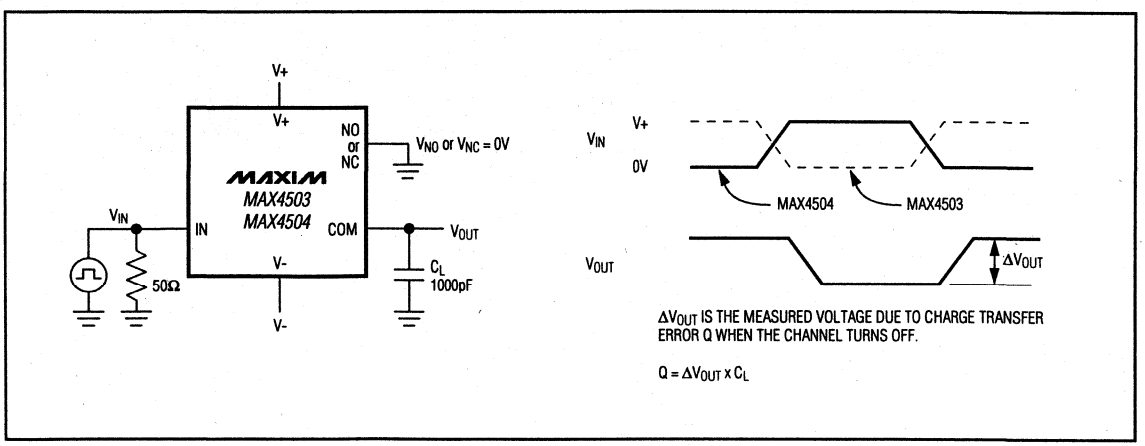


Figure 2. Charge Injection

Low-Voltage, Dual-Supply, SPST, CMOS Analog Switches

Test Circuits/Timing Diagrams (continued)

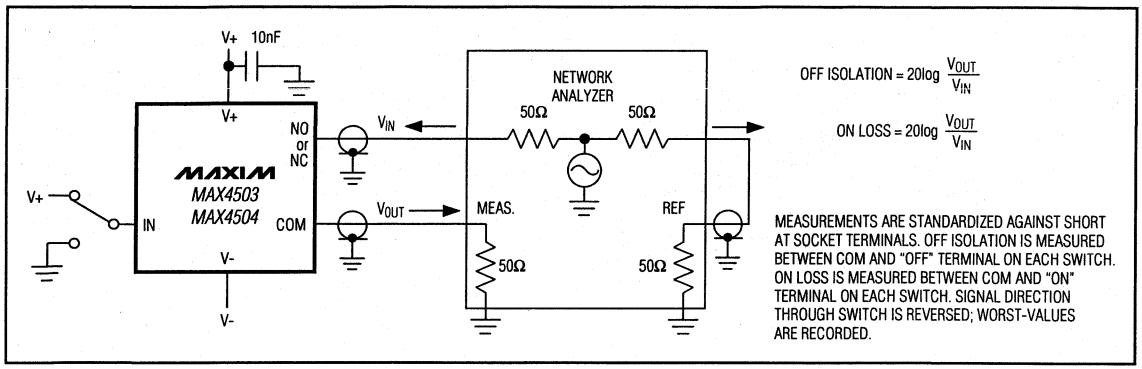


Figure 3. Off Isolation and On Loss

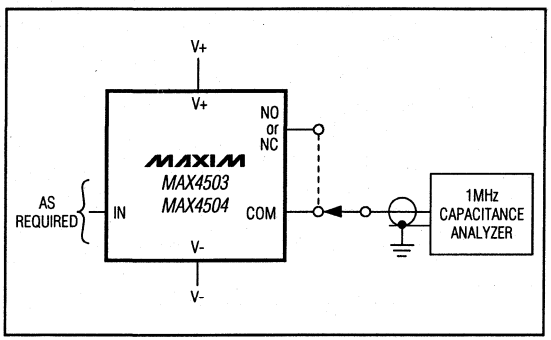


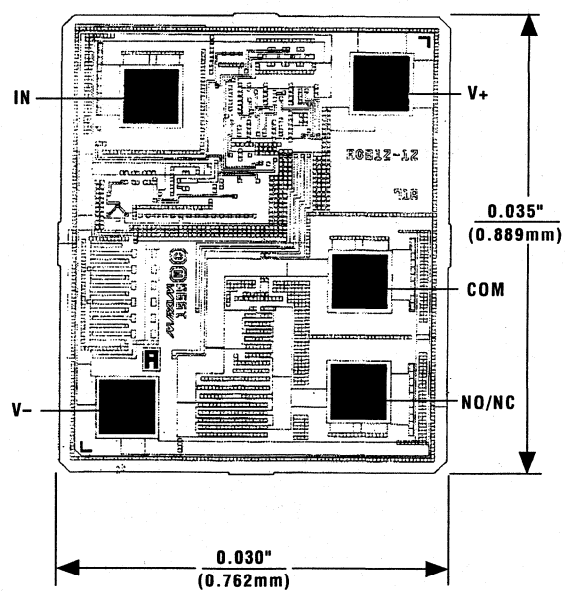
Figure 4. NO, NC, and COM Capacitance

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX4504CPA	0°C to +70°C	8 Plastic DIP
MAX4504CSA	0°C to +70°C	8 SO
MAX4504CUK	0°C to +70°C	5 SOT23-5
MAX4504C/D	0°C to +70°C	Dice*
MAX4504EPA	-40°C to +85°C	8 Plastic DIP
MAX4504ESA	-40°C to +85°C	8 SO
MAX4504EUK	-40°C to +85°C	5 SOT23-5
MAX4504MJA	-55°C to +125°C	8 CERDIP**

** Contact factory for dice specifications.*
*** Contact factory for availability.*

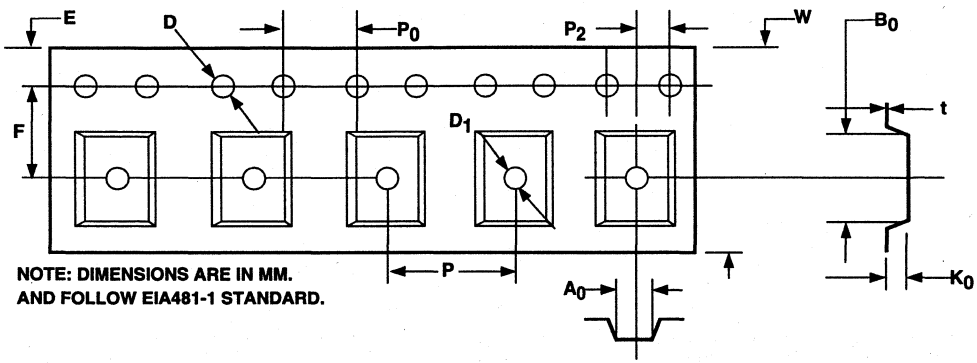
Chip Topography



TRANSISTOR COUNT: 36

SUBSTRATE IS INTERNALLY CONNECTED TO V+

Tape-and-Reel Information



NOTE: DIMENSIONS ARE IN MM.
AND FOLLOW EIA481-1 STANDARD.

A_0	3.200	±0.102
B_0	3.099	±0.102
D	1.499	+0.102 +0.000
D_1	0.991	+0.254 +0.000

E	1.753	±0.102
F	3.505	±0.051
K_0	1.397	±0.102
P	3.988	±0.102

P_0	3.988	±0.102
$P_0$10	40.005	±0.203
P_2	2.007	±0.051
t	0.254	±0.127
W	8.001	+0.305 -0.102

5 SOT23-5

19-1069; Rev 0; 6/96

MAXIM

Low-Voltage, Low-On-Resistance, SPST, CMOS Analog Switches

General Description

The MAX4514/MAX4515 are single-pole/single-throw (SPST), CMOS, low-voltage, single-supply analog switches with very low switch on-resistance. The MAX4514 is normally open (NO). The MAX4515 is normally closed (NC).

These CMOS switches can operate continuously with a single supply between +2V and +12V. Each switch can handle rail-to-rail analog signals. The off-leakage current maximum is only 1nA at +25°C or 20nA at +85°C.

All digital inputs have 0.8V to 2.4V logic thresholds, ensuring TTL/CMOS-logic compatibility when using a +5V supply.

For pin-compatible parts for use with dual supplies, see the MAX4516/MAX4517.

Applications

Battery-Operated Equipment

Audio and Video Signal Routing

Low-Voltage Data-Acquisition Systems

Communications Circuits

PCMCIA Cards

Cellular Phones

Modems

Features

- ♦ **Available in SOT23-5 Package**
- ♦ **+2V to +12V Single-Supply Operation**
- ♦ **Guaranteed On-Resistance:**
  20Ω with +5V Supply
  10Ω with +12V Supply
- ♦ **Guaranteed Low Off-Leakage Currents:**
  1nA at +25°C
  20nA at +85°C
- ♦ **Guaranteed Low On-Leakage Currents:**
  2nA at +25°C
  40nA at +85°C
- ♦ **Low Charge Injection: 10pC**
- ♦ **Fast Switching Speed: t_{ON} = 150ns, t_{OFF} = 100ns**
- ♦ **Break-Before-Make Operation: $t_{ON} > t_{OFF}$ at +5V**
- ♦ **TTL/CMOS-Logic Compatible with +5V Supply**

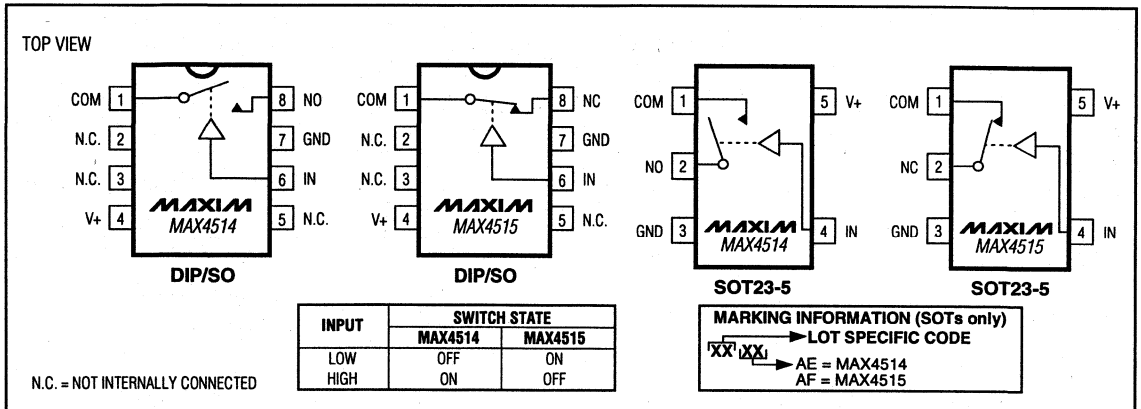
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4514CPA	0°C to +70°C	8 Plastic DIP
MAX4514CSA	0°C to +70°C	8 SO
MAX4514CUK	0°C to +70°C	5 SOT23-5
MAX4514C/D	0°C to +70°C	Dice*

Ordering Information continued at end of data sheet.

** Contact factory for dice specifications.*

Pin Configurations



INPUT	SWITCH STATE	
	MAX4514	MAX4515
LOW	OFF	ON
HIGH	ON	OFF

N.C. = NOT INTERNALLY CONNECTED

MARKING INFORMATION (SOTs only)
XXXX → LOT SPECIFIC CODE
AE = MAX4514
AF = MAX4515

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Low-Voltage, Low-On-Resistance, SPST, CMOS Analog Switches

ABSOLUTE MAXIMUM RATINGS

(Voltages Referenced to GND)
V+ .....-0.3V, +13V
Voltage into Any Terminal (Note 1).....-0.3V to (V+ + 0.3V)
or ±20mA (whichever occurs first)
Continuous Current into Any Terminal.....±20mA
Peak Current, NO_ or COM_
(pulsed at 1ms, 10% duty cycle).....±30mA
ESD per Method 3015.7 .....>2000V
Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
8-Pin SO (derate 5.88mW/°C above +70°C).....471mW
5-Pin SOT23-5 (derate 7.1mW/°C above +70°C) 571mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C).....640mW
Operating Temperature Ranges
MAX4514C_ _/MAX4515C_ _ .....0°C to +70°C
MAX4514E_ _/MAX4515E_ _.....-40°C to +85°C
MAX4514MJA/MAX4515MJA .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec).....+300°C

Note 1: Voltages exceeding V+ or GND on any signal terminal are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—+5V Supply

(V+ = +4.5V to +5.5V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	V_{COM}, V_{NO}, V_{NC}				0		V+	V
COM to NO or NC On-Resistance	R_{ON}	V+ = 5V, V_{COM} = 3.5V, I_{COM} = 1mA	T_A = +25°C			10	20	Ω
			T_A = T_{MIN} to T_{MAX}				25	
COM to NO or NC On-Resistance Flatness	ΔR_{ON}	V_{COM} = 1V, 2V, 3V; I_{COM} = 1mA	T_A = +25°C			1	3	Ω
			T_A = T_{MIN} to T_{MAX}				5	
NO or NC Off-Leakage Current (Note 3)	$I_{NO(OFF)}$ $I_{NC(OFF)}$	V+ = 5.5V, V_{COM} = 1V, V_{NO} or V_{NC} = 4.5V	T_A = +25°C		-1	0.01	1	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-20		20	
				M	-100		100	
COM Off-Leakage Current (Note 3)	$I_{COM(OFF)}$	V+ = 5.5V, V_{COM} = 1V, V_{NO} or V_{NC} = 4.5V	T_A = +25°C		-1	0.01	1	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-20		20	
				M	-100		100	
COM On-Leakage Current (Note 3)	$I_{COM(ON)}$	V+ = 5.5V, V_{COM} = 4.5V, V_{NO} or V_{NC} = 4.5V	T_A = +25°C		-2	0.01	2	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-40		40	
				M	-200		200	
DIGITAL I/O								
Input Logic High	V_{IH}				2.4		V+	V
Input Logic Low	V_{IL}				0		0.8	V
Input Current Logic High or Low	I_{IH}, I_{IL}	V_{IN} = V+, 0V			-1	0.03	1	µA
SWITCH DYNAMIC CHARACTERISTICS								
Turn-On Time	t_{ON}	Figure 2	T_A = +25°C			30	150	ns
			T_A = T_{MIN} to T_{MAX}				240	
Turn-Off Time	t_{OFF}	Figure 2	T_A = +25°C			20	100	ns
			T_A = T_{MIN} to T_{MAX}				150	

ELECTRICAL CHARACTERISTICS—+5V Supply (continued)

(V+ = +4.5V to +5.5V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SWITCH DYNAMIC CHARACTERISTICS							
Charge Injection (Note 4)	Q	C_L = 1nF, V_{NO} = 0V, R_S = 0Ω, T_A = +25°C, Figure 1			2	10	pC
Off Isolation	V_{ISO}	R_L = 50Ω, C_L = 15pF, V_{NO} = $1V_{RMS}$, f = 100kHz, T_A = +25°C, Figure 3			≤-90		dB
NO or NC Off Capacitance	$C_{NO(OFF)}$, $C_{NC(OFF)}$	f = 1MHz, T_A = +25°C, Figure 4			14		pF
COM Off Capacitance	$C_{COM(OFF)}$	f = 1MHz, T_A = +25°C, Figure 4			14		pF
COM On Capacitance	$C_{COM(ON)}$	f = 1MHz, T_A = +25°C, Figure 4			30		pF
POWER SUPPLY							
V+ Supply Current	I+	V_{IN} = 0V or V+	T_A = +25°C	-1		1	µA
			T_A = T_{MIN} to T_{MAX}	-10		10	

ELECTRICAL CHARACTERISTICS—+12V Supply

(V+ = +11.4V to +12.6V, V_{INH} = 5V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	V_{COM}, V_{NO}, V_{NC}				0		V+	V
COM to NO or NC On-Resistance	R_{ON}	V_{COM} = 10V, I_{COM} = 1mA	T_A = +25°C			5	10	Ω
			T_A = T_{MIN} to T_{MAX}				15	
NO, NC Off-Leakage Current (Note 3)	$I_{(NO)OFF}$ $I_{(NC)OFF}$	V_{COM} = 10V, V_{NO} = +1V	T_A = +25°C		-2		2	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-50		50	
				M	-200		200	
COM Off-Leakage Current (Note 3)	$I_{COM(OFF)}$	V_{COM} = 10V, V_{NO} or V_{NC} = 1V	T_A = +25°C		-2		2	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-50		50	
				M	-200		200	
COM On-Leakage Current (Note 3)	$I_{COM(ON)}$	V_{COM} = 10V	T_A = +25°C		-4		4	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-100		100	
				M	-400		400	
DIGITAL I/O								
Input Logic High	V_{INH}				5		V+	V
Input Logic Low	V_{INL}				0		0.8	V
Input Current Logic High or Low	I_{INH}, I_{INL}	V_{IN} = V+, 0V			-1	0.03	1	µA
POWER SUPPLY								
V+ Supply Current	I+	IN = 0V or V+	T_A = +25°C		-2		2	µA
			T_A = T_{MIN} to T_{MAX}		-20		20	

Low-Voltage, Low-On-Resistance, SPST, CMOS Analog Switches

ELECTRICAL CHARACTERISTICS—+3V Supply

(V+ = +3V to +3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

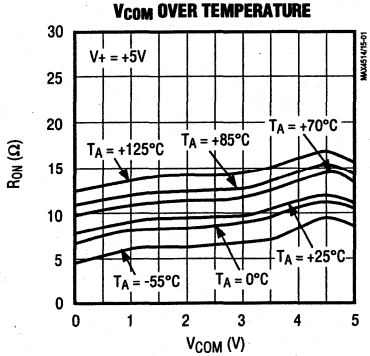
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	V_{COM}, V_{NO}, V_{NC}			0		V+	V
COM to NO or NC On-Resistance	R_{ON}	V_{COM} = 1.5V, I_{NO} = 1mA, V+ = 3V	T_A = +25°C		20	50	Ω
			T_A = T_{MIN} to T_{MAX}			75	
DIGITAL I/O							
Input Logic High	V_{INH}			2.4		V+	V
Input Logic Low	V_{INL}			0		0.80	V
Input Current Logic High or Low	I_{INH}, I_{INL}	V_{IN} = V+, 0V		-1	0.03	1	µA
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time (Note 4)	t_{ON}	Figure 2	T_A = +25°C		45	150	ns
			T_A = T_{MIN} to T_{MAX}			240	
Turn-Off Time (Note 4)	t_{OFF}	Figure 2	T_A = +25°C		30	100	ns
			T_A = T_{MIN} to T_{MAX}			150	
Charge Injection (Note 4)	Q	C_L = 1nF, Figure 1	T_A = +25°C		4	10	pC
POWER SUPPLY							
V+ Supply Current	I+	IN = 0V or V+	T_A = +25°C	-1		1	µA
			T_A = T_{MIN} to T_{MAX}	-10		10	

Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.
Note 3: Leakage parameters are 100% tested at maximum-rated hot operating temperature, and are guaranteed by correlation at +25°C.
Note 4: Guaranteed, not production tested.
Note 5: SOT packaged parts are 100% tested at +25°C. Limits at maximum and minimum rated temperature are guaranteed by design and correlation limits at +25°C.

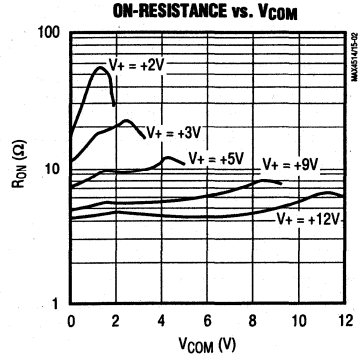
Typical Operating Characteristics

(V+ = +5V, GND = 0V, T_A = +25°C, unless otherwise noted.)

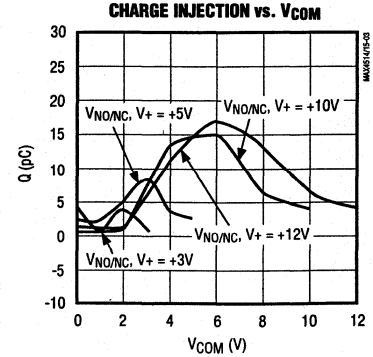
ON-RESISTANCE vs. V_{COM} OVER TEMPERATURE



ON-RESISTANCE vs. V_{COM}



CHARGE INJECTION vs. V_{COM}

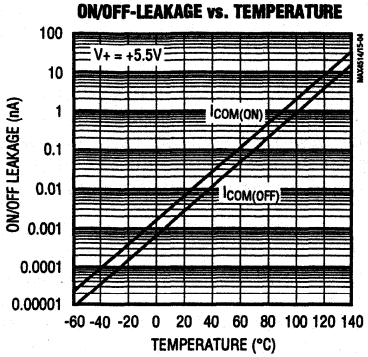


Low-Voltage, Low-On-Resistance, SPST, CMOS Analog Switches

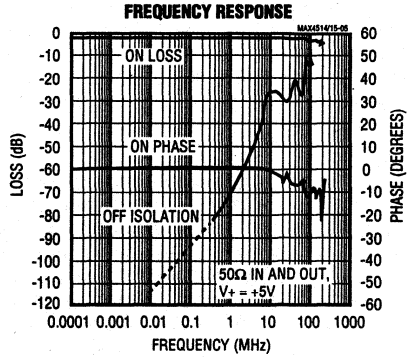
Typical Operating Characteristics (continued)

(V+ = +5V, GND = 0V, T_A = +25°C, unless otherwise noted.)

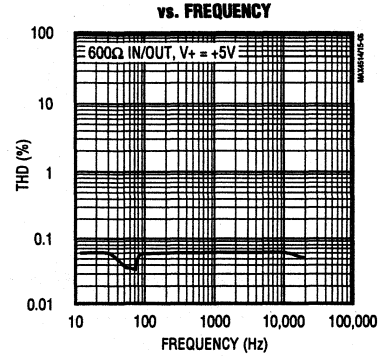
ON/OFF-LEAKAGE vs. TEMPERATURE



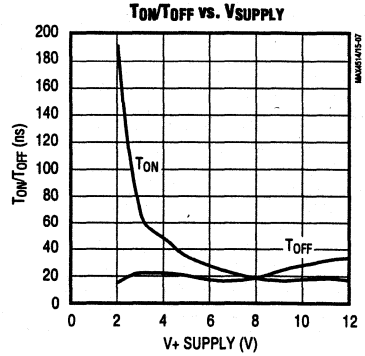
FREQUENCY RESPONSE



TOTAL HARMONIC DISTORTION vs. FREQUENCY



T_{ON}/T_{OFF} vs. V_{SUPPLY}



Pin Description

PIN				NAME	FUNCTION
MAX4514		MAX4515			
DIP/SO	SOT23-5	DIP/SO	SOT23-5		
1	1	1	1	COM	Analog Switch Common Terminal
2, 3, 5	—	2, 3, 5	—	N.C.	No Connect (not internally connected)
4	5	4	5	V+	Positive Supply-Voltage Input (analog and digital)
6	4	6	4	IN	Digital Control Input
7	3	7	3	GND	Ground
8	2	—	—	NO	Analog Switch (normally open)
—	—	8	2	NC	Analog Switch (normally closed)

Note: NO, NC, and COM pins are identical and interchangeable. Any may be considered as an input or an output; signals pass equally well in both directions.

Low-Voltage, Low-On-Resistance, SPST, CMOS Analog Switches

Applications Information

Power-Supply Considerations

The MAX4514/MAX4515 construction is typical of most CMOS analog switches, except that they have only two supply pins: V+ and GND. V+ and GND drive the internal CMOS switches and set their analog voltage limits. Reverse ESD-protection diodes are internally connected between each analog-signal pin and both V+ and GND. One of these diodes conducts if any analog signal exceeds V+ or GND.

Virtually all the analog leakage current comes from the ESD diodes to V+ or GND. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or GND and the analog signal. This means their leakages will vary as the signal varies. The *difference* in the two diode leakages to the V+ and GND pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity.

There is no connection between the analog-signal paths and V+ or GND.

V+ and GND also power the internal logic and logic-level translators. The logic-level translators convert the logic levels to switched V+ and GND signals to drive the analog signal gates.

Logic-Level Thresholds

The logic-level thresholds are CMOS/TTL compatible when V+ is +5V. As V+ is raised, the level threshold increases slightly. When V+ reaches +12V, the level threshold is about 3.0V—above the TTL guaranteed high-level minimum of 2.8V, but still compatible with CMOS outputs.

Do not connect the MAX4514/MAX4515's V+ to +3V and then connect the logic-level pins to logic-level signals that operate from +5V supply. Output levels can exceed +3V and violate the absolute maximum ratings, damaging the part and/or external circuits.

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat up to 250MHz (see *Typical Operating Characteristics*). Above 20MHz, the on response has several minor peaks that are highly layout dependent. The problem is not in turning the switch on; it's in turning it off. The off-state switch acts like a capacitor and passes higher frequencies with less attenuation. At 10MHz, off isolation is about -45dB in 50Ω systems, decreasing (approximately 20dB per decade) as frequency increases. Higher circuit impedances also make off isolation decrease. Off isolation is about 3dB above that of a bare IC socket, and is due entirely to capacitive coupling.

Test Circuits/Timing Diagrams

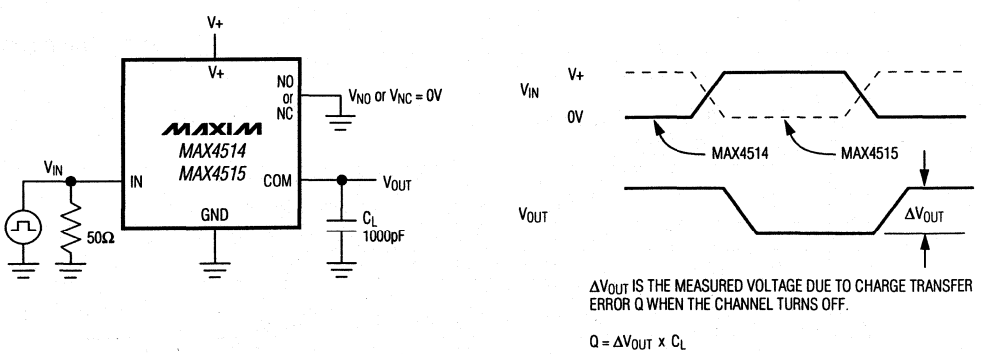


Figure 1. Charge Injection

Test Circuits/Timing Diagrams (continued)

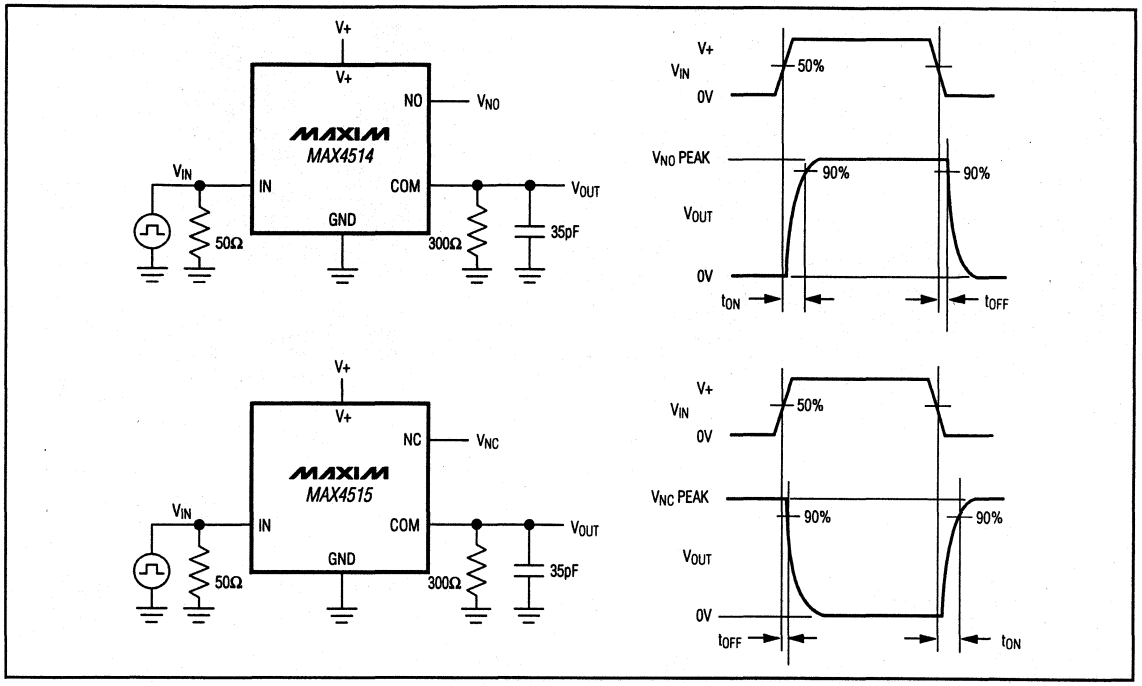


Figure 2. Switching Times

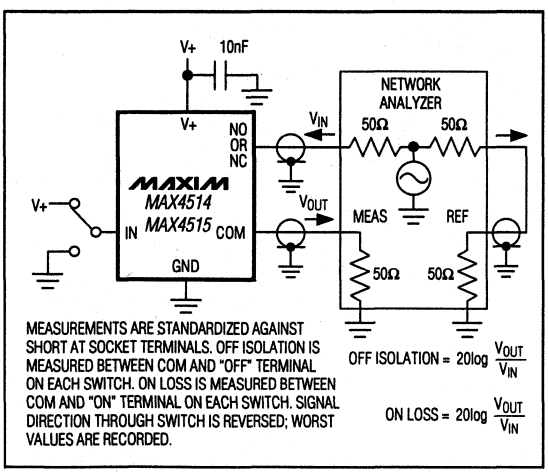


Figure 3. Off Isolation and On Loss

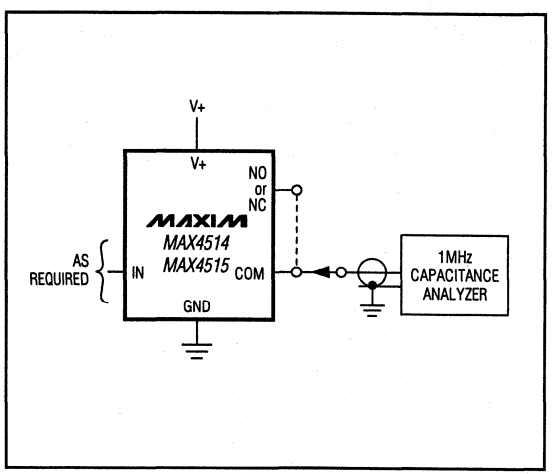


Figure 4. NO, NC, and COM Capacitance

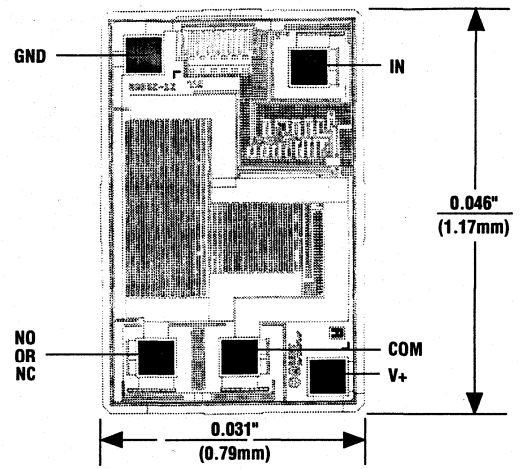
Low-Voltage, Low-On-Resistance, SPST, CMOS Analog Switches

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX4514EPA	-40°C to +85°C	8 Plastic DIP
MAX4514ESA	-40°C to +85°C	8 SO
MAX4514EUK	-40°C to +85°C	5 SOT23-5
MAX4514MJA	-55°C to +125°C	8 CERDIP**
MAX4515CPA	0°C to +70°C	8 Plastic DIP
MAX4515CSA	0°C to +70°C	8 SO
MAX4515CUK	0°C to +70°C	5 SOT23-5
MAX4515C/D	0°C to +70°C	Dice*
MAX4515EPA	-40°C to +85°C	8 Plastic DIP
MAX4515ESA	-40°C to +85°C	8 SO
MAX4515EUK	-40°C to +85°C	5 SOT23-5
MAX4515MJA	-55°C to +125°C	8 CERDIP**

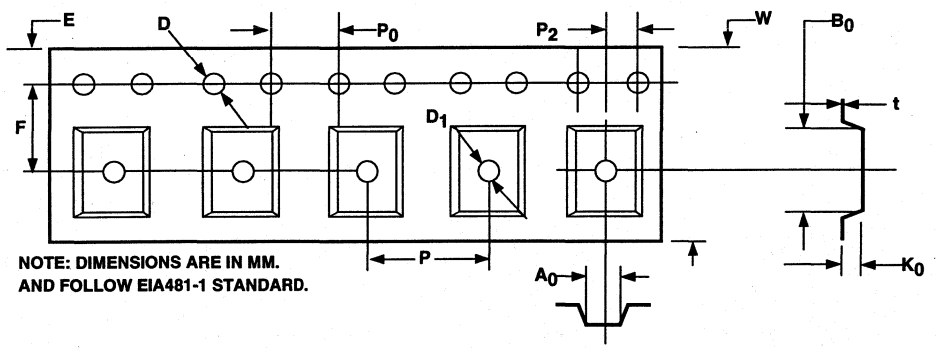
*Contact factory for dice specifications.
**Contact factory for availability.

Chip Topography



TRANSISTOR COUNT: 19
SUBSTRATE IS INTERNALLY CONNECTED TO V+

Tape-and-Reel Information



NOTE: DIMENSIONS ARE IN MM.
AND FOLLOW EIA481-1 STANDARD.

A_0	3.200	±0.102
B_0	3.099	±0.102
D	1.499	+0.102 +0.000
D_1	0.991	+0.254 +0.000

E	1.753	±0.102
F	3.505	±0.051
K_0	1.397	±0.102
P	3.988	±0.102

P_0	3.988	±0.102
$P_0$10	40.005	±0.203
P_2	2.007	±0.051
t	0.254	±0.127
W	8.001	+0.305 -0.102

5-SOT23-5

19-1068; Rev 0; 6/96

MAXIM

Dual-Supply, Low-On-Resistance, SPST, CMOS Analog Switches

General Description

The MAX4516/MAX4517 are single-pole/single-throw (SPST), CMOS, low-voltage, dual-supply analog switches with very low switch on-resistance. The MAX4516 is normally open (NO). The MAX4517 is normally closed (NC).

These CMOS switches can operate continuously with dual supplies between ±1V and ±6V. Each switch can handle rail-to-rail analog signals. The off-leakage current maximum is only 1nA at +25°C or 20nA at +85°C.

The digital input is referenced to the positive power supply and is CMOS compatible.

For pin-compatible parts for use with a single supply, refer to the MAX4514/MAX415.

Applications

Battery-Operated Equipment
Audio and Video Signal Routing
Low-Voltage Data-Acquisition Systems
Communications Circuits
PCMCIA Cards
Cellular Phones
Modems

Features

- ♦ **Available in SOT23-5 Package**
- ♦ **±1V to ±6V Dual-Supply Operation**
- ♦ **Guaranteed On-Resistance: 20Ω with ±5V Supplies**
- ♦ **Guaranteed Low Off-Leakage Currents:**
  1nA at +25°C
  20nA at +85°C
- ♦ **Guaranteed Low On-Leakage Currents:**
  2nA at +25°C
  40nA at +85°C
- ♦ **Low Charge Injection: 20pC Max**
- ♦ **Fast Switching Speed: t_{ON} = 100ns, t_{OFF} = 75ns**
- ♦ **$t_{ON} > t_{OFF}$ at ±5V**
- ♦ **CMOS Logic Compatible with ±5V Supplies**

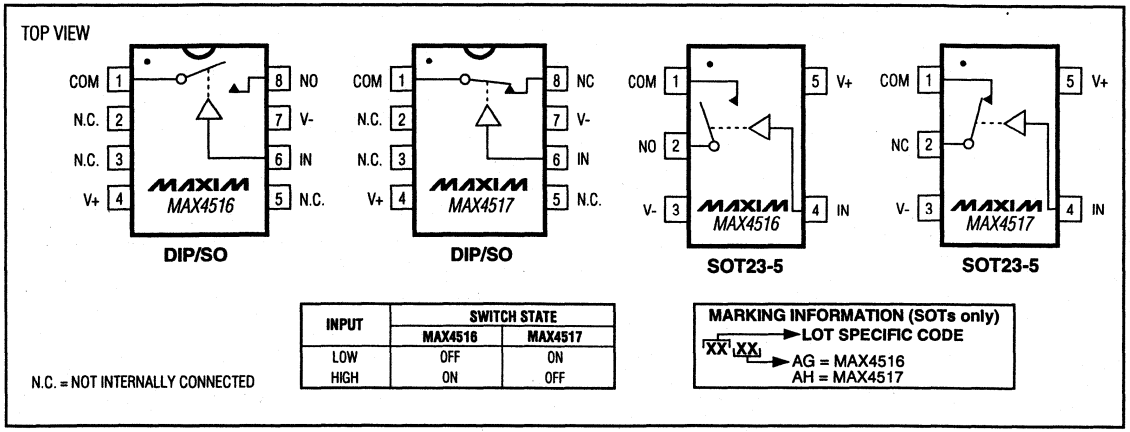
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4516CPA	0°C to +70°C	8 Plastic DIP
MAX4516CSA	0°C to +70°C	8 SO
MAX4516CUK	0°C to +70°C	5 SOT23-5
MAX4516C/D	0°C to +70°C	Dice*

Ordering Information continued at end of data sheet.

**Contact factory for dice specifications.*

Pin Configurations



INPUT	SWITCH STATE	
	MAX4516	MAX4517
LOW	OFF	ON
HIGH	ON	OFF

N.C. = NOT INTERNALLY CONNECTED

MARKING INFORMATION (SOTs only)
XX XX → LOT SPECIFIC CODE
AG = MAX4516
AH = MAX4517

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Dual-Supply, Low-On-Resistance, SPST, CMOS Analog Switches

ABSOLUTE MAXIMUM RATINGS

(Voltages Referenced to V-)
V+ .....-0.3V, +13V
Voltage into Any Terminal (Note 1)
or ±20mA (whichever occurs first) .....-0.3V to (V+ + 0.3V)
Continuous Current into Any Terminal .....±20mA
Peak Current, NO, NC, or COM_
(pulsed at 1ms, 10% duty cycle) .....±30mA
ESD per Method 3015.7 .....>2000V
Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) ...727mW
8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
5-Pin SOT23-5 (derate 7.1mW/°C above +70°C) 571mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C).....640mW
Operating Temperature Ranges
MAX4516C_ _/MAX4517_ _ .....0°C to +70°C
MAX4516E_ _/MAX4517E_ _ .....-40°C to +85°C
MAX4516MJA/MAX4517MJA .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: Voltages exceeding V+ or V- on any signal terminal are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—±5V Supply

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, V_{INH} = 3.5V, V_{INL} = 1.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	V_{COM}, V_{NO}, V_{NC}				V-		V+	V
COM to NO or NC On-Resistance	R_{ON}	V+ = 5V, V- = -5V, V_{NO} or V_{NC} = 3V, I_{COM} = 1mA	T_A = +25°C			10	20	Ω
			T_A = T_{MIN} to T_{MAX}				25	
COM to NO or NC On-Resistance Flatness	$R_{FLAT(ON)}$	V+ = 5V, V- = -5V; V_{NO} or V_{NC} = 3V, 0V, -3V; I_{COM} = 1mA	T_A = +25°C			2	4	Ω
			T_A = T_{MIN} to T_{MAX}				6	
NO or NC Off-Leakage Current (Note 3)	$I_{NO(OFF)}$ $I_{NC(OFF)}$	V+ = 5.5V, V- = 5.5V, V_{COM} = ±4.5V, V_{NO} or V_{NC} = ∓4.5V	T_A = +25°C		-1	0.01	1	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-20		20	
				M	-100		100	
COM Off-Leakage Current (Note 3)	$I_{COM(OFF)}$	V+ = 5.5V, V- = -5.5V, V_{COM} = ±4.5V, V_{NO} or V_{NC} = ∓4.5V	T_A = +25°C		-1	0.01	1	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-20		20	
				M	-100		100	
COM On-Leakage Current (Note 3)	$I_{COM(ON)}$	V+ = 5.5V, V- = -5.5V, V_{COM} = ±4.5V, V_{NO} or V_{NC} = ±4.5V	T_A = +25°C		-2	0.01	2	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-40		40	
				M	-200		200	
DIGITAL I/O								
Input Logic High	V_{IH}				V+ - 1.5V		V+	V
Input Logic Low	V_{IL}				V-		V+ - 3.5V	V
Input Current Logic High or Low	I_{IH}, I_{IL}	V_{IN} = V+, 0V			-0.5	0.03	0.5	µA

ELECTRICAL CHARACTERISTICS—±5V Supply (continued)

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, V_{INH} = 3.5V, V_{INL} = 1.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	Figure 1	T_A = +25°C		40	100	ns
			T_A = T_{MIN} to T_{MAX}			150	
Turn-Off Time	t_{OFF}	Figure 1	T_A = +25°C		30	75	ns
			T_A = T_{MIN} to T_{MAX}			125	
Charge Injection (Note 4)	Q	C_L = 1nF, V_{NO} = 0V, R_S = 0Ω, T_A = +25°C, Figure 2			10	20	pC
Off Isolation	V_{ISO}	R_L = 50Ω, C_L = 15pF, V_{NO} = 1V_{RMS}, f = 100kHz, T_A = +25°C, Figure 3			-86		dB
NO or NC Off Capacitance	$C_{NO(OFF)}$, $C_{NO(ON)}$	f = 1MHz, T_A = +25°C, Figure 4			9		pF
COM Off Capacitance	$C_{COM(OFF)}$	f = 1MHz, T_A = +25°C, Figure 4			9		pF
COM On Capacitance	$C_{COM(ON)}$	f = 1MHz, T_A = +25°C, Figure 4			22		pF
POWER SUPPLY							
Power-Supply Range				±1		±6	V
V+ Supply Current	I+	V_{IN} = 0V or V+	T_A = +25°C		40	125	µA
			T_A = T_{MIN} to T_{MAX}			200	
V- Supply Current	I-	V_{IN} = 0V or V+	T_A = +25°C	-125	-30		µA
			T_A = T_{MIN} to T_{MAX}	200			

Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Note 3: Leakage parameters are 100% tested at maximum-rated hot operating temperature, and are guaranteed by correlation at +25°C.

Note 4: Guaranteed, not production tested.

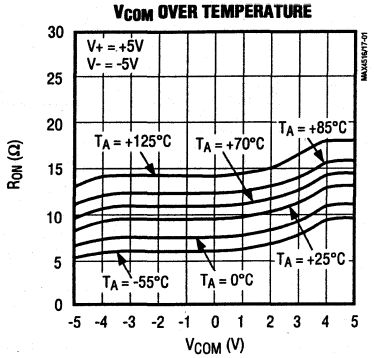
Note 5: SOT packaged parts are 100% tested at +25°C. Limits at maximum and minimum rated temperature are guaranteed by design and correlation limits at +25°C.

Dual-Supply, Low-On-Resistance, SPST, CMOS Analog Switches

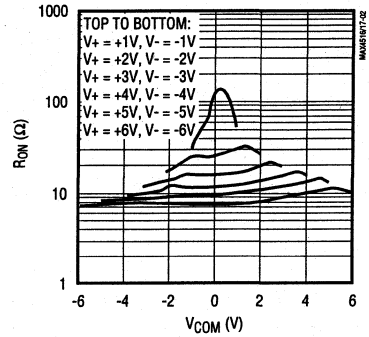
Typical Operating Characteristics

(V+ = +5V, V- = -5V, T_A = +25°C, unless otherwise noted.)

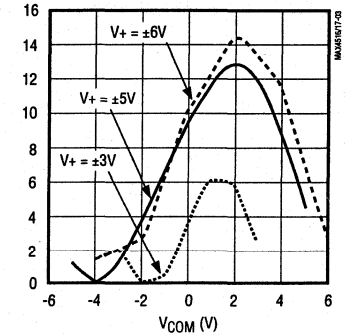
ON-RESISTANCE vs. V_{COM} OVER TEMPERATURE



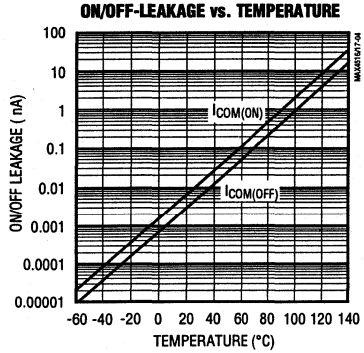
ON-RESISTANCE vs. V_{COM}



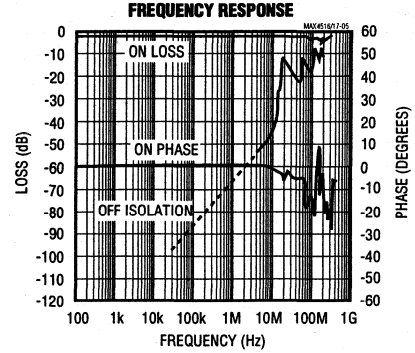
CHARGE INJECTION vs. V_{COM}



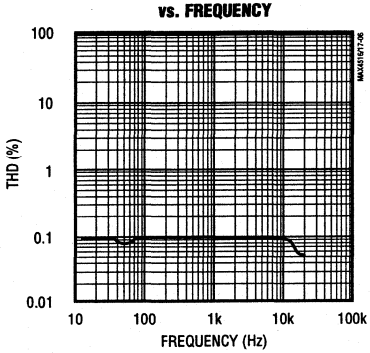
ON/OFF-LEAKAGE vs. TEMPERATURE



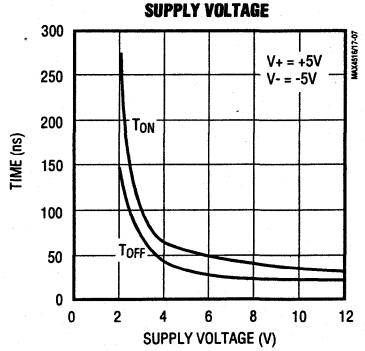
FREQUENCY RESPONSE



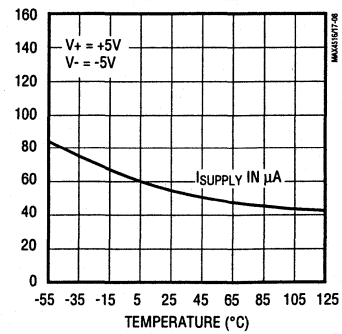
TOTAL HARMONIC DISTORTION vs. FREQUENCY



T_{ON}/T_{OFF} vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



Dual-Supply, Low-On-Resistance, SPST, CMOS Analog Switches

Pin Description

PIN				NAME	FUNCTION
MAX4516		MAX4517			
DIP/SO	SOT23-5	DIP/SO	SOT23-5		
1	1	1	1	COM	Analog Switch Common Terminal
2, 3, 5	—	2, 3, 5	—	N.C.	No Connect (not internally connected)
4	5	4	5	V+	Positive Supply-Voltage Input (analog and digital)
6	4	6	4	IN	Digital Control Input
7	3	7	3	V-	Negative Supply-Voltage Input (analog and digital)
8	2	—	—	NO	Analog Switch (normally open)
—	—	8	2	NC	Analog Switch (normally closed)

Note: NO, NC, and COM pins are identical and interchangeable. Any may be considered as an input or an output; signals pass equally well in both directions.

Applications Information

Power-Supply Considerations

The MAX4516/MAX4517 operate with power-supply voltages from ±1V to ±6V, but are tested and guaranteed only with ±5V supplies. Similarly, they will operate with a single +2V to +12V supply, but logic-level inputs can shift with higher voltages. The pin-compatible MAX4514/MAX4515 are recommended for use with a single supply.

The MAX4516/MAX4517 construction is typical of most CMOS analog switches, except that they have only two supply pins: V+ and V-. V+ and V- drive the internal CMOS switches and set their analog voltage limits. Reverse ESD-protection diodes are internally connected between each analog-signal pin and both V+ and V-. One of these diodes conducts if any analog signal exceeds V+ or V-.

Virtually all the analog leakage current comes from the ESD diodes to V+ or V-. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or V- and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V+ and V- pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity.

There is no connection between the analog-signal paths and V+ or V-.

V+ and V- also power the internal logic and logic-level translators. The logic-level translators convert the logic levels to switched V+ and V- signals to drive the analog signal gates.

Logic-Level Thresholds

The logic-level thresholds are CMOS-compatible but **not TTL-compatible**. Since these parts have no ground pin, the logic-level threshold is referenced to V+. The threshold limits are V+ = -1.5V and V+ = -3.5V for V+ levels between +6V and +3V. When V+ = +2V, the logic threshold is approximately 0.6V.

Do not connect the MAX4516/MAX4517's V+ to +3V and then connect the logic-level pins to logic-level signals that operate from a +5V supply. TTL levels can exceed +3V and violate the absolute maximum ratings, damaging the part and/or external circuits.

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat up to 250MHz (see *Typical Operating Characteristics*). Above 20MHz, the on response has several minor peaks that are highly layout dependent. The problem is not in turning the switch on; it's in turning it off. The off-state switch acts like a capacitor and passes higher frequencies with less attenuation. At 10MHz, off isolation is about -48dB in 50Ω systems, decreasing (approximately 20dB per decade) as frequency increases. Higher circuit impedances also cause off isolation to decrease. Off isolation is about 3dB above that of a bare IC socket, and is due entirely to capacitive coupling.

Dual-Supply, Low-On-Resistance, SPST, CMOS Analog Switches

Test Circuits/Timing Diagrams

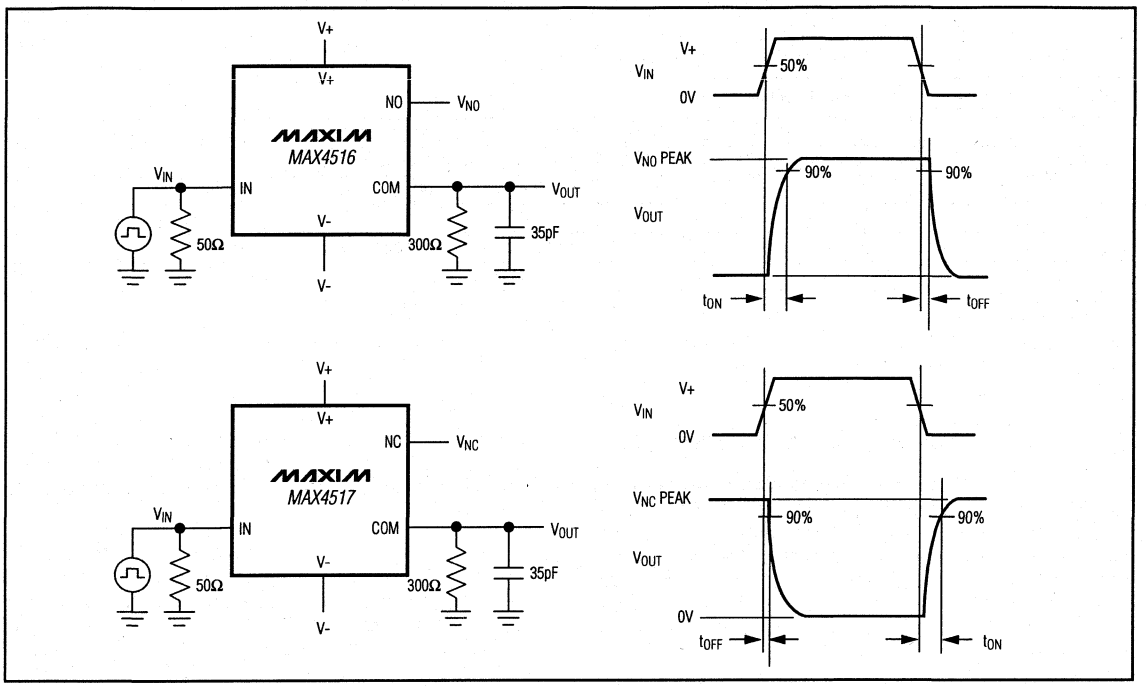


Figure 1. Switching Times

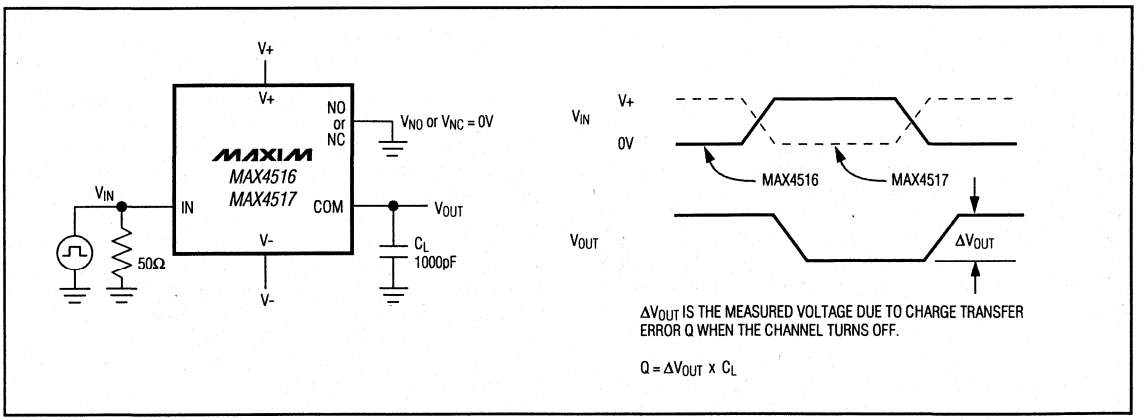


Figure 2. Charge Injection

Dual-Supply, Low-On-Resistance, SPST, CMOS Analog Switches

Test Circuits/Timing Diagrams (continued)

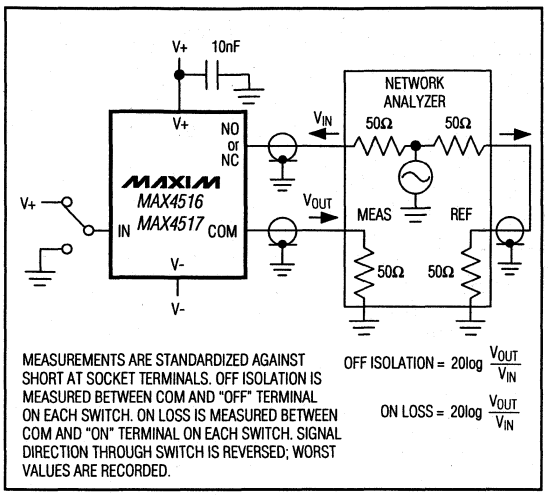


Figure 3. Off Isolation, On Loss, and Crosstalk

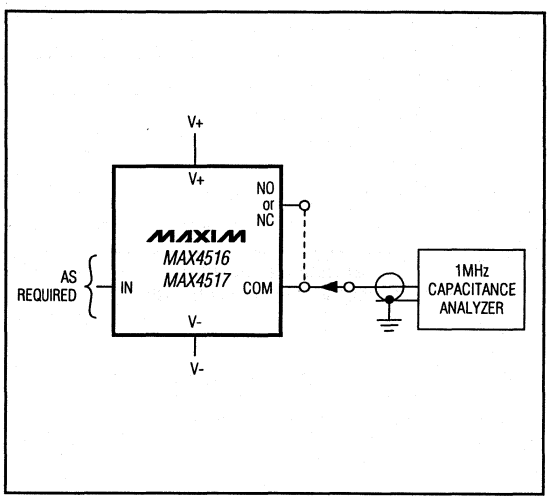


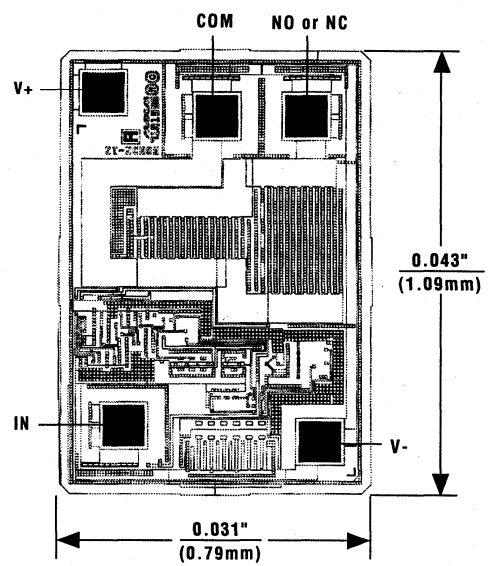
Figure 4. NO, NC, and COM Capacitance

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX4516EPA	-40°C to +85°C	8 Plastic DIP
MAX4516ESA	-40°C to +85°C	8 SO
MAX4516EUK	-40°C to +85°C	5 SOT23-5
MAX4516MJA	-55°C to +125°C	8 CERDIP**
MAX4517CPA	0°C to +70°C	8 Plastic DIP
MAX4517CSA	0°C to +70°C	8 SO
MAX4517CUK	0°C to +70°C	5 SOT23-5
MAX4517C/D	0°C to +70°C	Dice*
MAX4517EPA	-40°C to +85°C	8 Plastic DIP
MAX4517ESA	-40°C to +85°C	8 SO
MAX4517EUK	-40°C to +85°C	5 SOT23-5
MAX4517MJA	-55°C to +125°C	8 CERDIP**

**Contact factory for dice specifications.*
***Contact factory for availability.*

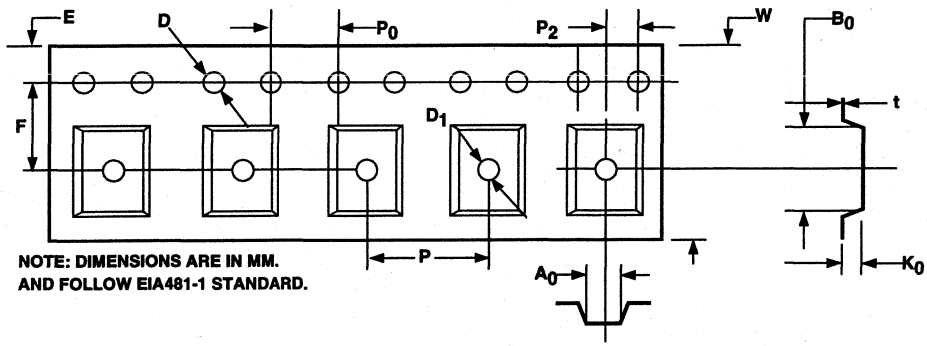
Chip Topography



TRANSISTOR COUNT: 36
SUBSTRATE IS INTERNALLY CONNECTED TO V+

Dual-Supply, Low-On-Resistance, SPST, CMOS Analog Switches

Tape-and-Reel Information



NOTE: DIMENSIONS ARE IN MM.
AND FOLLOW EIA481-1 STANDARD.

A_0	3.200	±0.102
B_0	3.099	±0.102
D	1.499	+0.102 +0.000
D_1	0.991	+0.254 +0.000

E	1.753	±0.102
F	3.505	±0.051
K_0	1.397	±0.102
P	3.988	±0.102

P_0	3.988	±0.102
$P_0$10	40.005	±0.203
P_2	2.007	±0.051
t	0.254	±0.127
W	8.001	+0.305 -0.102

5 SOT23-5

19-1070; Rev. 0; 5/96

MAXIM

Precision, 4-Channel/Dual 2-Channel, Low-Voltage, CMOS Analog Multiplexers

General Description

The MAX4518/MAX4519 precision, monolithic, CMOS analog multiplexers (muxes) offer low on-resistance (less than 100Ω), which is matched to within 4Ω between channels and remains flat over the specified analog signal range (10Ω max). They also offer low leakage over temperature (NO-off leakage current less than 2nA at +85°C) and fast switching speeds (transition time less than 250ns). The MAX4518 is a 4-channel device, and the MAX4519 is a dual 2-channel device.

The MAX4518/MAX4519 are fabricated with Maxim's low-voltage silicon-gate process. Design improvements yield extremely low charge injection (less than 5pC) and guarantee electrostatic discharge protection greater than 2000V.

These muxes operate with a single +2.7V to +15V supply or with bipolar ±2.7V to ±8V supplies, while retaining CMOS-logic input compatibility and fast switching. CMOS inputs provide reduced input loading.

Applications

Sample-and-Hold Circuits
Automatic Test Equipment
Heads-Up Displays
Guidance and Control Systems
Military Radios
Communications Systems
Battery-Operated Systems
PBX, PABX
Audio Signal Routing
Low-Voltage Data-Acquisition Systems

Features

- ♦ **Guaranteed On-Resistance Match Between Channels (<4Ω)**
- ♦ **Low On-Resistance (<100Ω)**
- ♦ **Guaranteed Flat On-Resistance over Signal Range (<10Ω)**
- ♦ **Guaranteed Low Charge Injection (<5pC)**
- ♦ **NO-Off Leakage Current <2nA at +85°C**
- ♦ **COM-Off Leakage Current <5nA at +85°C**
- ♦ **Electrostatic Discharge Protection >2000V**
- ♦ **Single-Supply Operation (+2.7V to +15V) Bipolar-Supply Operation (±2.7V to ±8V)**
- ♦ **Low Power Consumption (<300µW)**
- ♦ **Rail-to-Rail Signal Handling**
- ♦ **TTL/CMOS-Logic Compatible**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4518CPD	0°C to +70°C	14 Plastic DIP
MAX4518CSD	0°C to +70°C	14 SO
MAX4518CEE	0°C to +70°C	16 QSOP
MAX4518C/D	0°C to +70°C	Dice*
MAX4518EPD	0°C to +70°C	14 Plastic DIP
MAX4518ESD	-40°C to +85°C	14 SO
MAX4518EEE	-40°C to +85°C	16 QSOP
MAX4518MJD	-55°C to +125°C	14 CERDIP**

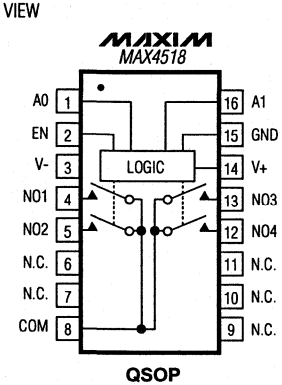
Ordering Information continued at end of data sheet.

** Contact factory for dice specifications.*

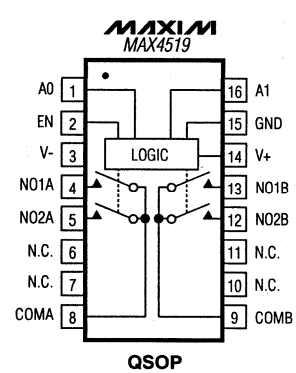
*** Contact factory for package availability.*

Pin Configurations

TOP VIEW



QSOP



QSOP

N.C. = NOT INTERNALLY CONNECTED

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Precision, 4-Channel/Dual 2-Channel, Low-Voltage, CMOS Analog Multiplexers

ABSOLUTE MAXIMUM RATINGS

(Voltage Referenced to GND)
V+ .....-0.3V to +17V
V- .....+0.3V to -17V
V+ to V- .....-0.3V to +17V
Voltage into NO_, NC_ (Note 1) .....(V- - 0.3V) to (V+ + 0.3V) or 30mA (whichever occurs first)
Voltage into EN, A0, A1 (Note 1) .....(V- - 0.3V) to (V- + 17V)
Current into Any Terminal 30mA
Peak Current, Any Terminal
(pulsed at 1ms, 10% duty cycle max) 40mA

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 10.0mW/°C above +70°C) 800mW
Narrow SO (derate 8.0mW/°C above +70°C) 640mW
QSOP (derate 9.52mW/°C above +70°C) 762mW
CERDIP (derate 9.09mW/°C above +70°C) 727mW
Operating Temperature Ranges
MAX4518C_ _ /MAX4519C_ _ .....0°C to +70°C
MAX4518E_ _ /MAX4519E_ _ .....-40°C to +85°C
MAX4518MJD/MAX4519MJD .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: Signals on any terminal exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current ratings.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, GND = 0V, $V_{AH} = V_{ENH}$ = 2.4V, $V_{AL} = V_{ENL}$ = 0.8V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS				MIN	TYP (Note 2)	MAX	UNITS
SWITCH									
Analog Signal Range	V_{COM}, V_{NO}	(Note 3)				V-		V+	V
Channel On-Resistance	R_{ON}	I_{NO} = 1mA, V_{COM} = ±3V		T_A = +25°C			60	100	Ω
				$T_A = T_{MIN}$ to T_{MAX}				125	
On-Resistance Matching Between Channels (Note 4)	ΔR_{ON}	I_{NO} = 1mA, V_{COM} = ±3.5V, V+ = 5V, V- = -5V		T_A = +25°C				4	Ω
				$T_A = T_{MIN}$ to T_{MAX}				6	
On-Resistance Flatness (Note 5)	$R_{FLAT(ON)}$	I_{NO} = 1mA; V_{COM} = ±3V, 0V; V+ = 5V; V- = -5V		T_A = +25°C				10	Ω
				$T_A = T_{MIN}$ to T_{MAX}				13	
NO-Off Leakage Current (Note 6)	$I_{NO(OFF)}$	V_{NO} = ±4.5V, V_{COM} = ∓4.5V, V+ = 5.5V, V- = -5.5V		T_A = +25°C		-0.1		0.1	nA
				$T_A = T_{MIN}$ to T_{MAX}	C, E	-2		2	
					M	-20		20	
COM-Off Leakage Current (Note 6)	$I_{COM(OFF)}$	V_{COM} = ±4.5V, V_{NO} = ∓4.5V, V+ = 5.5V, V- = -5.5V	MAX4518	T_A = +25°C		-0.2		0.2	nA
				$T_A = T_{MIN}$ to T_{MAX}	C, E	-5		5	
					M	-40		40	
			MAX4519	T_A = +25°C		-0.1		0.1	
				$T_A = T_{MIN}$ to T_{MAX}	C, E	-3		3	
					M	-20		20	
COM-On Leakage Current (Note 6)	$I_{COM(ON)}$	V_{COM} = ±4.5V, V_{NO} = ±4.5V,	MAX4518	T_A = +25°C		-0.4		0.4	nA
				$T_A = T_{MIN}$ to T_{MAX}	C, E	-10		10	
					M	-100		100	
			MAX4519	T_A = +25°C		-0.2		0.2	
				$T_A = T_{MIN}$ to T_{MAX}	C, E	-5		5	
					M	-50		50	

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, GND = 0V, $V_{AH} = V_{ENH}$ = 2.4V, $V_{AL} = V_{ENL}$ = 0.8V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
DIGITAL LOGIC INPUT								
Logic High Input Voltage	V_{AH}, V_{ENH}		$T_A = T_{MIN}$ to T_{MAX}		2.4		V+	V
Logic Low Input Voltage	V_{AL}, V_{ENL}		$T_A = T_{MIN}$ to T_{MAX}		0		0.8	V
Input Current with Input Voltage High	I_{AH}, I_{ENH}	$V_A = V_{EN}$ = 2.4V			-0.1		0.1	µA
Input Current with Input Voltage Low	I_{AL}, I_{ENL}	$V_A = V_{EN}$ = 0.8V			-0.1		0.1	µA
SUPPLY								
Power-Supply Range	V+, V-				±2.7		±8	V
Positive Supply Current	I+	$V_{EN} = V_A$ = 0V/V+, V+ = 5.5V, V- = -5.5V	T_A = +25°C		-1		1	µA
			$T_A = T_{MIN}$ to T_{MAX}		-10		10	
Negative Supply Current	I-	$V_{EN} = V_A$ = 0V/V+, V+ = 5.5V, V- = -5.5V	T_A = +25°C		-1		1	µA
			$T_A = T_{MIN}$ to T_{MAX}		-10		10	
Ground Current	I_{GND}	$V_{EN} = V_A$ = 0V/V+, V+ = 5.5V, V- = -5.5V	T_A = +25°C		-1		1	µA
			$T_A = T_{MIN}$ to T_{MAX}		-10		10	
DYNAMIC								
Transition Time	t_{TRANS}	Figure 2	T_A = +25°C				150	ns
			$T_A = T_{MIN}$ to T_{MAX}				250	
Break-Before-Make Interval	t_{OPEN}	Figure 4	T_A = +25°C		0	40		ns
Enable Turn-On Time	$t_{ON(EN)}$	Figure 3	T_A = +25°C			60	150	ns
			$T_A = T_{MIN}$ to T_{MAX}				250	
Enable Turn-Off Time	$t_{OFF(EN)}$	Figure 3	T_A = +25°C			40	150	ns
			$T_A = T_{MIN}$ to T_{MAX}				200	
Charge Injection (Note 3)	Q	Figure 5, C_L = 1.0nF, V_S = 0V, R_S = 0Ω	T_A = +25°C			0	5	pC
Off Isolation (Note 7)	V_{ISO}	Figure 6, V_{EN} = 0V, R_L = 1kΩ, f = 100kHz	T_A = +25°C			-75		dB
Crosstalk Between Channels	V_{CT}	Figure 6, V_{EN} = 2.4V, f = 100kHz, V_{GEN} = 1Vp-p, R_L = 1kΩ	T_A = +25°C			-92		dB
Logic Input Capacitance	C_{IN}	f = 1MHz	T_A = +25°C			8		pF
NO-Off Capacitance	$C_{NO(OFF)}$	f = 1MHz, $V_{EN} = V_D$ = 0V	T_A = +25°C			5		pF
COM-Off Capacitance	$C_{COM(OFF)}$	f = 1MHz, $V_{EN} = V_D$ = 0V	T_A = +25°C	MAX4518		16		pF
				MAX4519		10		
COM-On Capacitance	$C_{COM(ON)}$	f = 1MHz, $V_{EN} = V_D$ = 0V	T_A = +25°C	MAX4518		27		pF
				MAX4519		17		

Precision, 4-Channel/Dual 2-Channel, Low-Voltage, CMOS Analog Multiplexers

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +4.5V to +5.5V, V- = 0V, GND = 0V, V_{AH} = V_{ENH} = 2.4V, V_{AL} = V_{ENL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS				MIN	TYP (Note 2)	MAX	UNITS
SWITCH									
Analog Signal Range	V_{COM}, V_{NO}	(Note 3)				V-		V+	V
On-Resistance	R_{ON}	I_{NO} = 1mA, V_{COM} = 3.5V, V+ = 4.5V		T_A = +25°C			150	225	Ω
				T_A = T_{MIN} to T_{MAX}				280	
On-Resistance Matching Between Channels (Note 4)	ΔR_{ON}	I_{NO} = 1mA, V_{COM} = 3V, V+ = 4.5V		T_A = +25°C				10	Ω
				T_A = T_{MIN} to T_{MAX}				12	
On-Resistance Flatness	R_{FLAT}	I_{NO} = 1mA; V_{COM} = 3V, 2V, 1V; V+ = 5V		T_A = +25°C			10	16	Ω
				T_A = T_{MIN} to T_{MAX}			15	20	
NO-Off Leakage Current (Note 8)	$I_{NO(OFF)}$	V_{NO} = 4.5V, V_{COM} = 0V, V+ = 5.5V		T_A = +25°C		-0.1		0.1	nA
				T_A = T_{MIN} to T_{MAX}	C, E	-1.0		1.0	
					M	-10		10	
COM-Off Leakage Current (Note 8)	$I_{COM(OFF)}$	V_{COM} = 4.5V, V_{NO} = 0V, V+ = 5.5V	MAX4518	T_A = +25°C		-0.2		0.2	nA
				T_A = T_{MIN} to T_{MAX}	C, E	-2.5		2.5	
					M	-20		20	
			MAX4519	T_A = +25°C		-0.2		0.2	
				T_A = T_{MIN} to T_{MAX}	C, E	-1.5		1.5	
					M	-10		10	
COM-On Leakage Current (Note 8)	$I_{COM(ON)}$	V_{COM} = 4.5V, V_{NO} = 4.5V, V+ = 5.5V	MAX4518	T_A = +25°C		-0.4		0.4	nA
				T_A = T_{MIN} to T_{MAX}	C, E	-5		5	
					M	-40		40	
			MAX4519	T_A = +25°C		-0.2		0.2	
				T_A = T_{MIN} to T_{MAX}	C, E	-2.5		2.5	
					M	-20		20	
DIGITAL LOGIC INPUT									
Logic High Input Voltage	V_{AH}, V_{ENH}			T_A = T_{MIN} to T_{MAX}		2.4		V+	V
Logic Low Input Voltage	V_{AL}, V_{ENL}			T_A = T_{MIN} to T_{MAX}		0		0.8	V
Input Current with Input Voltage High	I_{AH}, I_{ENH}	V_A = V_{EN} = 2.4V				-0.1		0.1	µA
Input Current with Input Voltage Low	I_{AL}, I_{ENL}	V_A = V_{EN} = 0.8V				-0.1		0.1	µA
SUPPLY									
Power-Supply Range	V+					2.7		15	V
Positive Supply Current	I+	V_{EN} = V_A = 0V, V+; V+ = 5.5V; V- = 0V				-10		10	µA
Negative Supply Current	I-	V_{EN} = V_A = 0V, V+; V+ = 5.5V; V- = 0V				-10		10	µA
I_{GND} Supply Current	I_{GND}	V_{EN} = V+, 0V; V_A = 0V; V+ = 5.5V; V- = 0V		T_A = +25°C		-1.0		1.0	µA
				T_A = T_{MIN} to T_{MAX}		-10		10	

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V+ = +4.5V to +5.5V, V- = 0V, GND = 0V, V_{AH} = V_{ENH} = 2.4V, V_{AL} = V_{ENL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
DYNAMIC							
Transition Time	t_{TRANS}	V_{NO} = 3V			90	245	ns
Break-Before-Make Interval	t_{OPEN}		T_A = +25°C	10	40		ns
Enable Turn-On Time	$t_{ON(EN)}$		T_A = +25°C		90	200	ns
			T_A = T_{MIN} to T_{MAX}			275	
Enable Turn-Off Time	$t_{OFF(EN)}$		T_A = +25°C		50	125	ns
			T_A = T_{MIN} to T_{MAX}			200	
Charge Injection (Note 3)	Q	C_L = 1.0nF, V_S = 0V, R_S = 0Ω	T_A = +25°C		0	5	pC

ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +2.7V to +3.3V, V- = 0V, GND = 0V, V_{AH} = V_{ENH} = 2.4V, V_{AL} = V_{ENL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SWITCH							
Analog Signal Range	V_{ANALOG}	(Note 3)		V-		V+	V
On-Resistance	R_{ON}	I_{NO} = 0.1mA, V_{COM} = 1.5V, V+ = 3V	T_A = +25°C		230	375	Ω
			T_A = T_{MIN} to T_{MAX}			425	
DYNAMIC							
Transition Time (Note 3)	t_{TRANS}	Figure 1, V_{IN} = 2.4V, V_{INL} = 0V, V_{NO1} = 1.5V	T_A = +25°C		230	575	ns
Enable Turn-On Time (Note 3)	$t_{ON(EN)}$	Figure 3, V_{INH} = 2.4V, V_{INL} = 0V, V_{NO1} = 1.5V	T_A = +25°C		200	500	ns
Enable Turn-Off Time (Note 3)	$t_{OFF(EN)}$	Figure 3, V_{INH} = 2.4V, V_{INL} = 0V, V_{NO1} = 1.5V	T_A = +25°C		75	400	ns
Charge Injection (Note 3)	Q	Figure 5, C_L = 1.0nF, V_S = 0V, R_S = 0Ω	T_A = +25°C		0	5	pC

Note 2: The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.

Note 3: Guaranteed by design.

Note 4: ΔR_{ON} = R_{ON}(max) - R_{ON}(min).

Note 5: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges; i.e., V_{NO} = 3V to 0V and 0V to -3V.

Note 6: Leakage parameters are 100% tested at maximum rated hot operating temperature, and guaranteed by correlation at +25°C.

Note 7: Worst-case isolation is on channel 4 because of its proximity to the COM pin. Off isolation = 20log V_{COM}/V_{NO}, V_{COM} = output, V_{NO} = input to off switch.

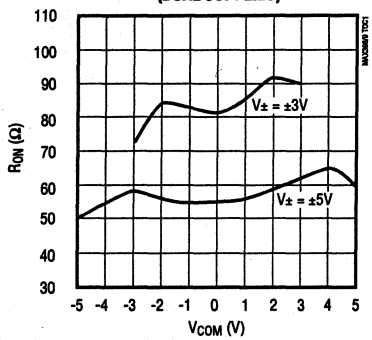
Note 8: Leakage testing at single supply is guaranteed by correlation testing with dual supplies.

Precision, 4-Channel/Dual 2-Channel, Low-Voltage, CMOS Analog Multiplexers

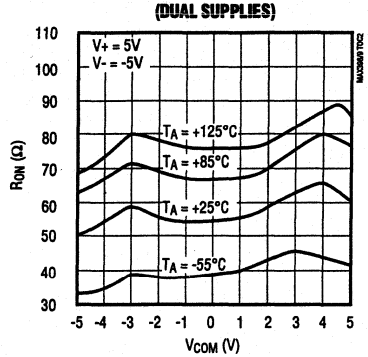
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

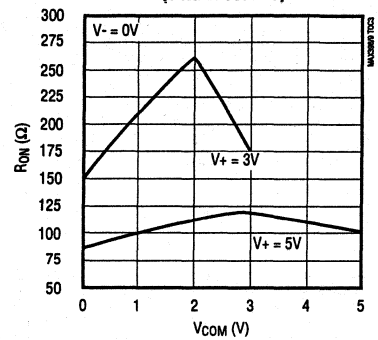
ON-RESISTANCE vs. V_{COM} (DUAL SUPPLIES)



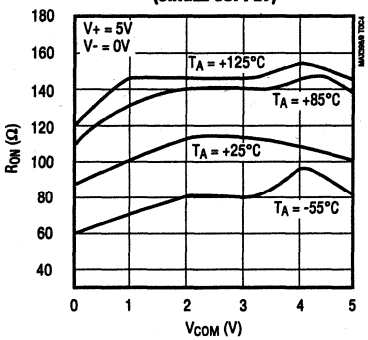
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (DUAL SUPPLIES)



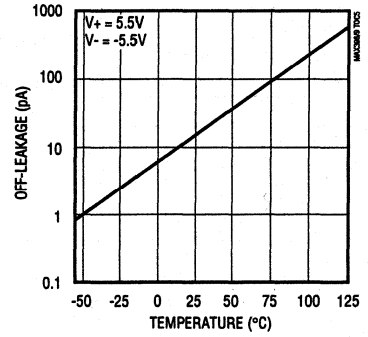
ON-RESISTANCE vs. V_{COM} (SINGLE SUPPLY)



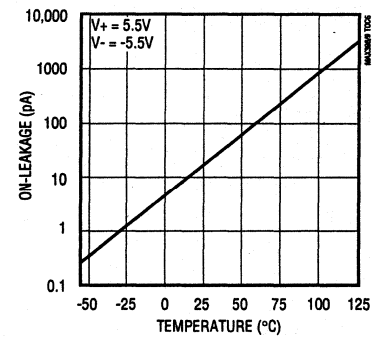
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (SINGLE SUPPLY)



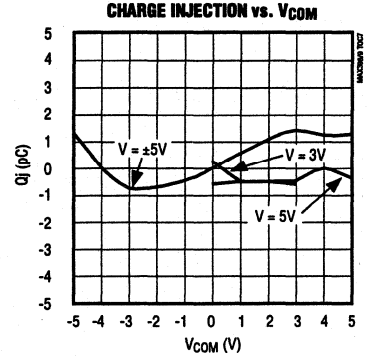
OFF-LEAKAGE vs. TEMPERATURE



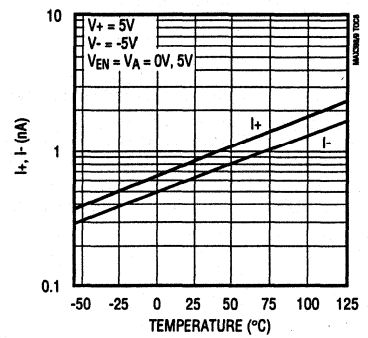
ON-LEAKAGE vs. TEMPERATURE



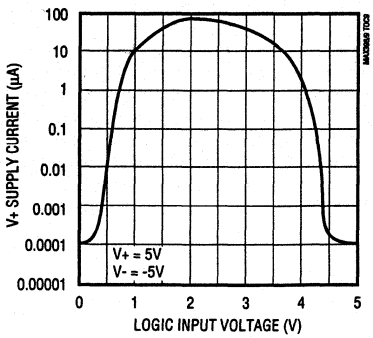
CHARGE INJECTION vs. V_{COM}



SUPPLY CURRENT vs. TEMPERATURE



V+ SUPPLY CURRENT vs. LOGIC INPUT VOLTAGE



Precision, 4-Channel/Dual 2-Channel, Low-Voltage, CMOS Analog Multiplexers

Pin Description

PIN				NAME	FUNCTION
MAX4518		MAX4519			
DIP/SO	QSOP	DIP/SO	QSOP		
1	1	1	1	A0	Address 0 Logic Input
2	2	2	2	EN	Enable Logic Input
3	3	3	3	V-	Negative Supply Voltage Input. Connect to GND for single-supply operation.
4	4	—	—	NO1	Analog Signal Normally Open number 1
5	5	—	—	NO2	Analog Signal Normally Open number 2
—	—	4	4	NO1A	Analog Signal Normally Open number 1 -A switch
—	—	5	5	NO2A	Analog Signal Normally Open number 2 -A switch
—	—	6	8	COMA	Analog Signal Common -A switch
6	8	—	—	COM	Analog Signal Common
7, 8, 9	6, 7, 9, 10, 11	7, 8	6, 7, 10, 11	N.C.	Not internally connected
—	—	9	9	COMB	Analog Signal Common -B switch
—	—	10	12	NO2B	Analog Signal Normally Open number 2 -B switch
—	—	11	13	NO1B	Analog Signal Normally Open number 1 -B switch
10	12	—	—	NO4	Analog Signal Normally Open number 4
11	13	—	—	NO3	Analog Signal Normally Open number 3
12	14	12	14	V+	Positive Supply Voltage Input
13	15	13	15	GND	Logic Ground Input
14	16	14	16	A1	Address 1 Logic Input

Precision, 4-Channel/Dual 2-Channel, Low-Voltage, CMOS Analog Multiplexers

Applications Information

Operation with Supply Voltages Other than ±5V

Using supply voltages less than ±5V reduces the analog signal range. The MAX4518/MAX4519 muxes operate with ±2.7V to ±8V bipolar supplies or with a +2.7V to +15V single supply. Connect V- to GND when operating with a single supply. Both device types can also operate with unbalanced supplies, such as +10V and -5V. The *Typical Operating Characteristics* graphs show typical on-resistance with ±3V, ±5V, +3V and +5V supplies. (Switching times increase by a factor of two or more for operation at 5V.)

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the devices. Always sequence V+ on first, then V-, followed by the logic inputs, NO, or COM. If power-supply sequencing is not possible, add two small signal diodes (D1, D2) in series with supply pins for overvoltage protection (Figure 1). Adding diodes reduces the analog signal range to one diode drop below V+ and one diode drop above V-, but does not affect the devices' low switch resistance and low leakage characteristics. Device operation is unchanged, and the difference between V+ and V- should not exceed 17V. These protection diodes are not recommended when using a single supply.

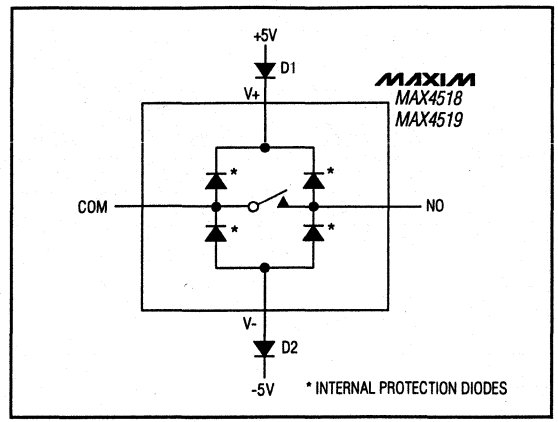


Figure 1. Overvoltage Protection Using External Blocking Diodes

Test Circuits/Timing Diagrams

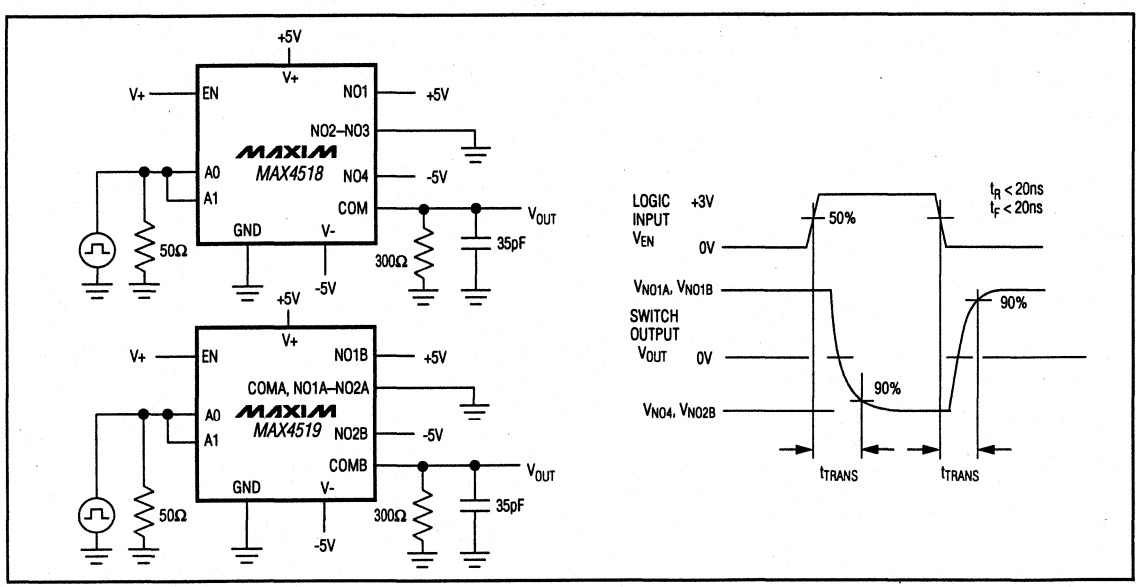


Figure 2. Transition Time

Test Circuits/Timing Diagrams (continued)

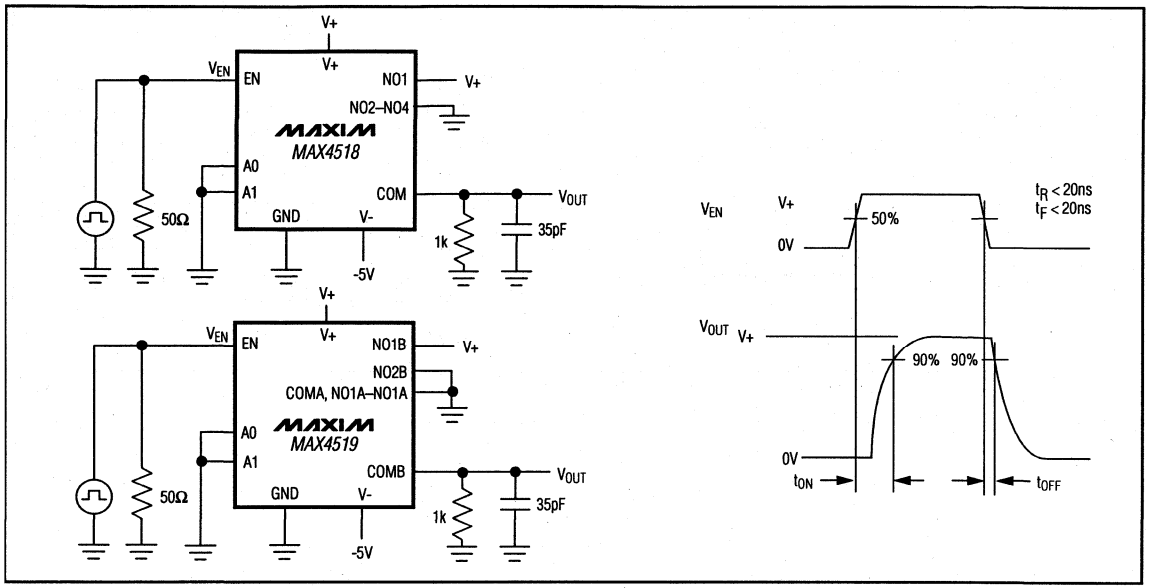


Figure 3. Enable Switching Time

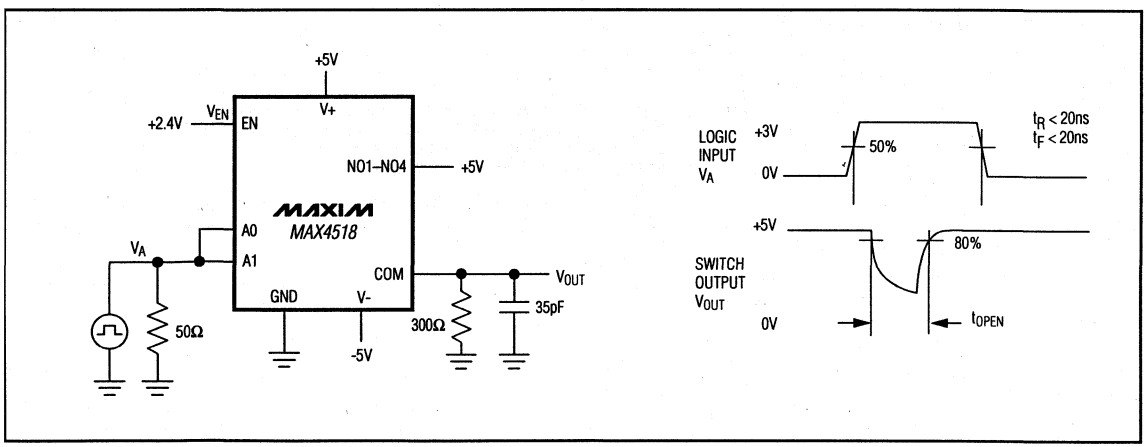


Figure 4. Break-Before-Make Interval

Precision, 4-Channel/Dual 2-Channel, Low-Voltage, CMOS Analog Multiplexers

Test Circuits/Timing Diagrams (continued)

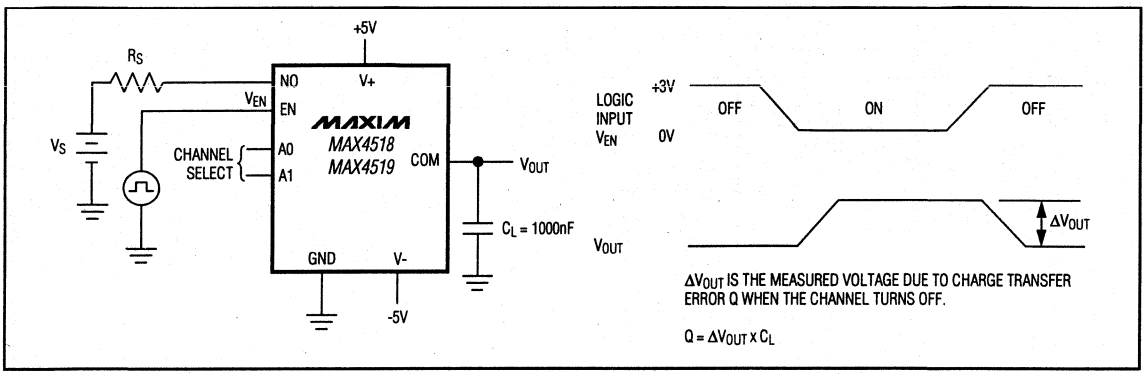


Figure 5. Charge Injection

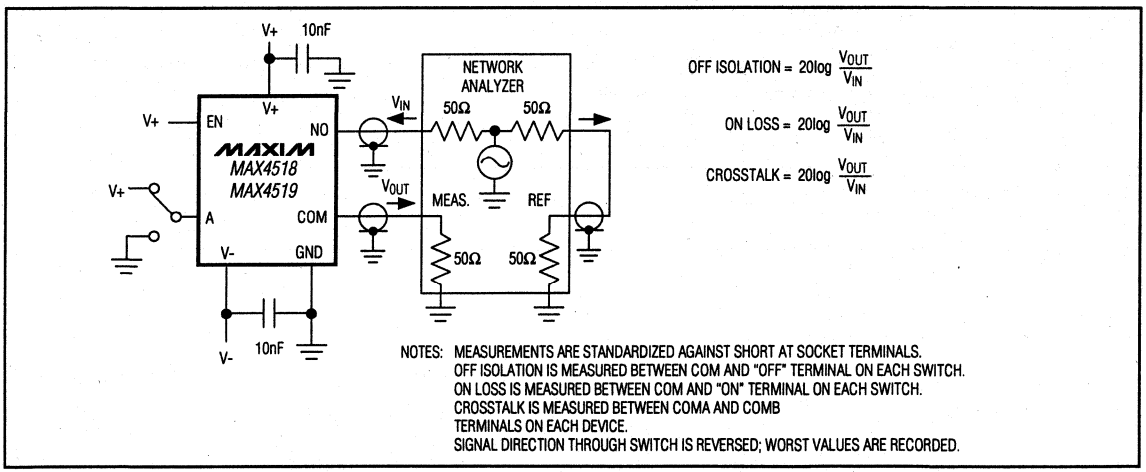


Figure 6. Off Isolation, On Loss, Crosstalk

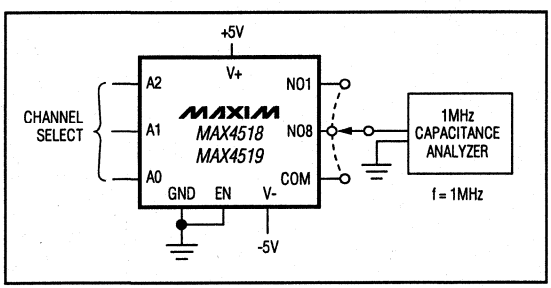
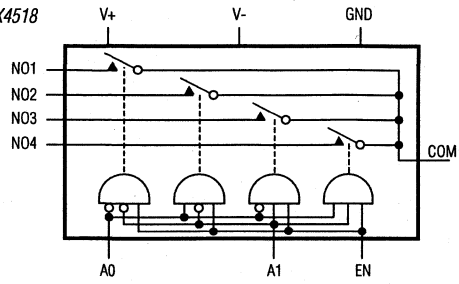


Figure 7. NO/COM Capacitance

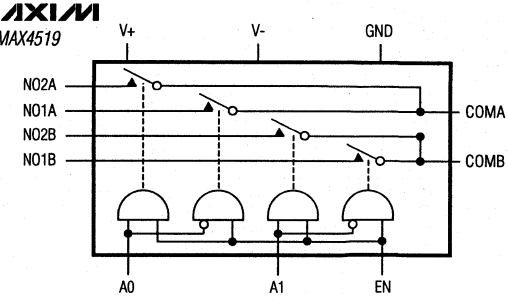
Precision, 4-Channel/Dual 2-Channel, Low-Voltage, CMOS Analog Multiplexers

Functional Diagrams/Truth Tables

MAXIM
MAX4518



MAXIM
MAX4519



MAX4518			
A1	A0	EN	ON SWITCH
X	X	0	NONE
0	0	1	NO1
0	1	1	NO2
1	0	1	NO3
1	1	1	NO4

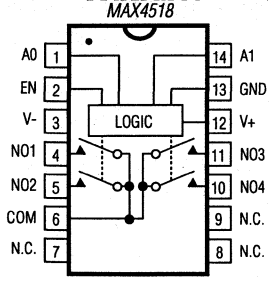
MAX4519			
A1	A0	EN	ON SWITCH
X	X	0	NONE
0	0	1	NO1A, NO1B
0	1	1	NO2A, NO1B
1	0	1	NO1A, NO2B
1	1	1	NO2A, NO2B

LOGIC "0" $V_{AL} \leq +0.8$ V, LOGIC "1" $V_{AH} \geq +2.4$ V

Pin Configurations (continued)

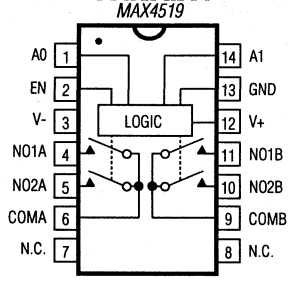
TOP VIEW

MAXIM
MAX4518



DIP/SO

MAXIM
MAX4519



DIP/SO

N.C. = NOT INTERNALLY CONNECTED

Precision, 4-Channel/Dual 2-Channel, Low-Voltage, CMOS Analog Multiplexers

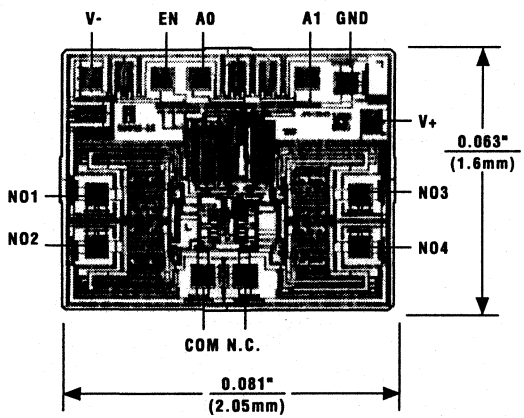
_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX4519CPD	0°C to +70°C	14 Plastic DIP
MAX4519CSD	0°C to +70°C	14 SO
MAX4519CEE	0°C to +70°C	16 QSOP
MAX4519C/D	0°C to +70°C	Dice*
MAX4519EPD	0°C to +70°C	14 Plastic DIP
MAX4519ESD	-40°C to +85°C	14 SO
MAX4519EEE	-40°C to +85°C	16 QSOP
MAX4519MJD	-55°C to +125°C	14 CERDIP**

** Contact factory for dice specifications.*
*** Contact factory for package availability.*

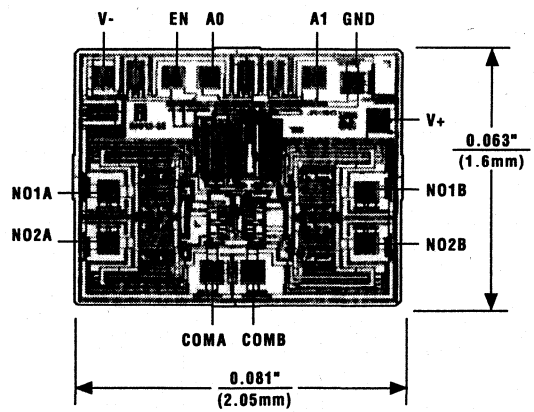
Chip Topographies

MAX4518



TRANSISTOR COUNT: 86
SUBSTRATE CONNECTED TO V+

MAX4519



TRANSISTOR COUNT: 86
SUBSTRATE CONNECTED TO V+

19-1136; Rev 0; 9/96

MAXIM

Quad, Low-Voltage, SPST Analog Switches

General Description

The MAX4521/MAX4522/MAX4523 are quad, low-voltage, single-pole/single-throw (SPST) analog switches. On-resistance (100Ω max) is matched between switches to 4Ω max, and is flat (12Ω max) over the specified signal range. Each switch can handle rail-to-rail analog signals. The off-leakage current is only 1nA at +25°C and 10nA at +85°C.

The MAX4521 has four normally closed (NC) switches, and the MAX4522 has four normally open (NO) switches. The MAX4523 has two NC switches and two NO switches.

These CMOS switches can operate with dual power supplies ranging from ±2V to ±6V or a single supply between +2V and +12V. They are fully specified for single +2.7V operation.

All digital inputs have +0.8V and +2.4V logic thresholds, ensuring TTL/CMOS-logic compatibility when using ±5V or a single +5V supply.

Applications

Battery-Operated Equipment
Data Acquisition
Test Equipment
Avionics
Audio Signal Routing
Networking

Features

- **+2V to +12V Single Supply**
  ±2V to ±6V Dual Supplies
- **100Ω Signal Paths with ±5V Supplies**
- **Low Power Consumption, <1µW**
- **4 Separately Controlled SPST Switches**
- **Rail-to-Rail Signal Handling**
- **Pin Compatible with Industry-Standard DG211/DG212/DG213**
- **>2kV ESD Protection per Method 3015.7**
- **TTL/CMOS-Compatible Inputs with ±5V or Single +5V Supply**

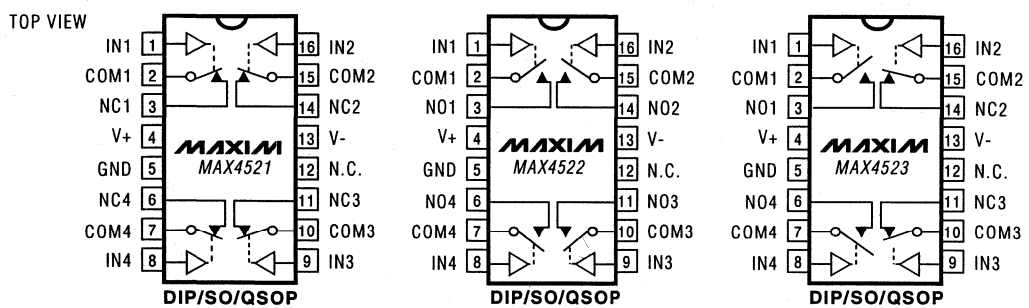
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4521CPE	0°C to +70°C	16 Plastic DIP
MAX4521CSE	0°C to +70°C	16 Narrow SO
MAX4521CEE	0°C to +70°C	16 QSOP
MAX4521C/D	0°C to +70°C	Dice*

Ordering Information continued at end of data sheet.

**Contact factory for dice specifications.*

Pin Configurations/Functional Diagrams/Truth Tables



MAX4521	
LOGIC	SWITCH
0	ON
1	OFF

N.C. = NOT CONNECTED

MAX4522	
LOGIC	SWITCH
0	OFF
1	ON

SWITCHES SHOWN FOR LOGIC "0" INPUT

MAX4523		
LOGIC	SWITCHES 1, 4	SWITCHES 2, 3
0	OFF	ON
1	ON	OFF

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Quad, Low-Voltage, SPST Analog Switches

ABSOLUTE MAXIMUM RATINGS

(Voltages Referenced to GND)
V+ .....-0.3V to +13.0V
V- .....-13.0V to +0.3V
V+ to V- .....-0.3V to +13.0V
All Other Pins (Note 1) .....(V- - 0.3V) to (V+ + 0.3V)
Continuous Current into Any Terminal .....±10mA
Peak Current, into Any Terminal
(pulsed at 1ms,10% duty cycle) .....±20mA
ESD per Method 3015.7 .....>2000V

Continuous Power Dissipation (T_A = +70°C) (Note 2)
Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
Narrow SO (derate 8.70mW/°C above +70°C) 696mW
QSOP (derate 9.52mW/°C above +70°C) 762mW
CERDIP (derate 10.00mW/°C above +70°C) 800mW
Operating Temperature Ranges
MAX452_C_E .....0°C to +70°C
MAX452_E_E .....-40°C to +85°C
MAX452_MJE .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10 sec) .....+300°C

Note 1: Signals on NC_, NO_, COM_, or IN_ exceeding V+ or V- are clamped by internal diodes. Limit forward-diode current to maximum current rating.
Note 2: All leads are soldered or welded to PC boards.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 3)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{COM_}$, $V_{NO_}$, $V_{NC_}$	(Note 4)	C, E, M	V-		V+	V
COM_ to NO_, COM_ to NC_ On-Resistance	R_{ON}	V+ = 5V, V- = -5V, $V_{COM_}$ = ±3V, $I_{COM_}$ = 1mA	+25°C		65	100	Ω
			C, E, M			125	
COM_ to NO_, COM_ to NC_ On-Resistance Match Between Channels (Note 5)	ΔR_{ON}	V+ = 5V, V- = -5V, $V_{COM_}$ = ±3V, $I_{COM_}$ = 1mA	+25°C		1	4	Ω
			C, E, M			6	
COM_ to NO_, COM_ to NC_ On-Resistance Flatness (Note 6)	$R_{FLAT(ON)}$	V+ = 5V, V- = -5V, $V_{COM_}$ = ±3V, $I_{COM_}$ = 1mA	+25°C		7	12	Ω
			C, E, M			15	
NO_, NC_ Off-Leakage Current (Note 7)	$I_{NO_(OFF)}$, $I_{NC_(OFF)}$	V+ = 5.5V, V- = -5.5V, $V_{COM_}$ = ∓4.5V, $V_{N_}$ = ±4.5V	+25°C	-1	0.01	1	nA
			C, E	-10		10	
			M	-100		100	
COM_ Off-Leakage Current (Note 7)	$I_{COM_(OFF)}$	V+ = 5.5V, V- = -5.5V, $V_{COM_}$ = ±4.5V, $V_{N_}$ = ∓ 4.5V	+25°C	-1	0.01	1	nA
			C, E	-10		10	
			M	-100		100	
COM_ On-Leakage Current (Note 7)	$I_{COM_(ON)}$	V+ = 5.5V, V- = -5.5V, $V_{COM_}$ = ±4.5V	+25°C	-2	0.01	2	nA
			C, E	-20		20	
			M	-200		200	

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 3)	MAX	UNITS
LOGIC INPUT							
IN_ Input Logic Threshold High	V_{IN_H}		C, E, M		1.6	2.4	V
IN_ Input Logic Threshold Low	V_{IN_L}		C, E, M	0.8	1.6		V
IN_ Input Current Logic High or Low	$I_{INH_}$, $I_{INL_}$	$V_{IN_}$ = 0.8V or 2.4V	C, E, M	-1	0.03	1	µA
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	$V_{COM_}$ = ±3V, V+ = 4.5V, V- = -4.5V, Figure 1	+25°C		45	80	ns
			C, E, M			100	
Turn-Off Time	t_{OFF}	$V_{COM_}$ = ±3V, V+ = 4.5V, V- = -4.5V, Figure 1	+25°C		15	30	ns
			C, E, M			40	
Break-Before-Make Time Delay (MAX4523 Only)	t_{BBM}	$V_{COM_}$ = ±3V, V+ = 5.5V, V- = -5.5V, Figure 2	+25°C	5	20		ns
Charge Injection (Note 4)	Q	C_L = 1nF, $V_{NO_}$ = 0V, R_S = 0Ω, Figure 3	+25°C		1	5	pC
NO_, NC_ Off-Capacitance	$C_{N_(OFF)}$	$V_{NO_}$ = GND, f = 1MHz, Figure 6	+25°C		2		pF
COM_ Off-Capacitance	$C_{COM_(OFF)}$	$V_{COM_}$ = GND, f = 1MHz, Figure 6	+25°C		2		pF
COM_ On-Capacitance	$C_{COM_(ON)}$	$V_{COM_}$ = $V_{NO_}$ = GND, f = 1MHz, Figure 7	+25°C		5		pF
Off-Isolation (Note 8)	V_{ISO}	R_L = 50Ω, C_L = 15pF, $V_{N_}$ = $1V_{RMS}$, f = 100kHz, Figure 4	+25°C		< -90		dB
Channel-to-Channel Crosstalk (Note 9)	V_{CT}	R_L = 50, C_L = 15pF, $V_{N_}$ = $1V_{RMS}$, f = 100kHz, Figure 5	+25°C		< -90		dB
POWER SUPPLY							
Power-Supply Range	V+, V-		C, E, M	-6		6	V
V+ Supply Current	I+	V+ = 5.5V, all $V_{IN_}$ = 0V or V+	+25°C	-1	0.05	1	µA
			C, E, M	-1		1	
V- Supply Current	I-	V- = -5.5V	+25°C	-1	0.05	1	µA
			C, E, M	-1		1	

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +4.5V to +5.5V, V- = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 3)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{COM_}$, $V_{NO_}$, $V_{NC_}$	(Note 4)	C, E, M	0		V+	V
COM_ to NO_, COM_ to NC_ On-Resistance	R_{ON}	V+ = 4.5V, $V_{COM_}$ = 3.5V, $I_{COM_}$ = 1mA	+25°C		125	200	Ω
			C, E, M			250	
COM_ to NO_, COM_ to NC_ On-Resistance Match Between Channels (Note 5)	ΔR_{ON}	V+ = 5V, $V_{COM_}$ = 3.5V, $I_{COM_}$ = 1mA	+25°C		2	8	Ω
			C, E, M			10	
NO_, NC_ Off-Leakage Current (Notes 7, 10)	$I_{NO_(OFF)}$, $I_{NC_(OFF)}$	V+ = 5.5V; $V_{COM_}$ = 1V, 4.5V; $V_{N_}$ = 4.5V, 1V	+25°C	-1	0.01	1	nA
			C, E	-10		10	
			M	-100		100	
COM_ Off-Leakage Current (Notes 7, 10)	$I_{COM_(OFF)}$	V+ = 5.5V; $V_{COM_}$ = 1V, 4.5V; $V_{N_}$ = 4.5V, 1V	+25°C	-1	0.01	1	nA
			C, E	-10		10	
			M	-100		100	
COM_ On-Leakage Current (Notes 7, 10)	$I_{COM_(ON)}$	V+ = 5.5V; $V_{COM_}$ = 4.5V, 1V	+25°C	-2	0.01	2	nA
			C, E,	-20		20	
			M	-200		200	
LOGIC INPUT							
IN_ Input Logic Threshold High	V_{IN_H}		C, E		1.6	2.4	V
IN_ Input Logic Threshold Low	V_{IN_L}		C, E	0.8	1.6		V
IN_ Input Current Logic High or Low	$I_{INH_}$, $I_{INL_}$	$V_{IN_}$ = 0.8V or 2.4V	C, E	-1	0.03	1	µA
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	$V_{COM_}$ = 3V, V+ = 4.5V, Figure 1	+25°C		60	100	ns
			C, E, M			150	
Turn-Off Time	t_{OFF}	$V_{COM_}$ = 3V, V+ = 4.5V, Figure 1	+25°C		20	50	ns
			C, E, M			75	
Break-Before-Make Time Delay (MAX4523 Only)	t_{BBM}	$V_{COM_}$ = 3V, V+ = 5.5V, Figure 2	+25°C	10	30		ns
Charge Injection (Note 4)	Q	C_L = 1nF, $V_{NO_}$ = 0V, R_S = 0Ω, Figure 3	+25°C		1	5	pC
POWER SUPPLY							
V+ Supply Current	I+	V+ = 5.5V, all $V_{IN_}$ = 0V or V+	+25°C	-1	0.05	1	µA
			C, E, M	-1		1	
V- Supply Current	I-	V- = 0V	+25°C	-1	0.05	1	µA
			C, E, M	-1		1	

ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +2.7V to +3.6V, V- = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 3)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{COM_}$, $V_{NO_}$, $V_{NC_}$	(Note 4)	C, E, M	0		V+	V
COM_ to NO_, COM_ to NC_ On-Resistance	R_{ON}	V+ = 2.7V, $V_{COM_}$ = 1.0V, $I_{COM_}$ = 0.1mA	+25°C		260	500	Ω
			C, E, M			600	
LOGIC INPUT							
IN_ Input Logic Threshold High	V_{IN_H}		C, E		1.6	2.4	V
IN_ Input Logic Threshold Low	V_{IN_L}		C, E	0.8	1.6		V
IN_ Input Current Logic High or Low	$I_{INH_}$, $I_{INL_}$	$V_{IN_}$ = 0.8V or 2.4V	C, E	-1	0.03	1	µA
SWITCH DYNAMIC CHARACTERISTICS (Note 4)							
Turn-On Time	t_{ON}	$V_{COM_}$ = 1.5V, V+ = 2.7V, Figure 1	+25°C		120	250	ns
			C, E, M			300	
Turn-Off Time	t_{OFF}	$V_{COM_}$ = 1.5V, V+ = 2.7V, Figure 1	+25°C		40	80	ns
			C, E, M			100	
Break-Before-Make Time Delay (MAX4523 Only)	t_{BBM}	$V_{COM_}$ = 1.5V, V+ = 3.6V, Figure 2	+25°C	15	50		ns
Charge Injection	Q	C_L = 1nF, $V_{NO_}$ = 0V, R_S = 0Ω, Figure 3	+25°C		0.5	5	pC
POWER SUPPLY							
V+ Supply Current	I+	V+ = 3.6V, all $V_{IN_}$ = 0V or V+	+25°C	-1	0.05	1	µA
			C, E, M	-1		1	
V- Supply Current	I-	V- = 0V	+25°C	-1	0.05	1	µA
			C, E, M	-1		1	

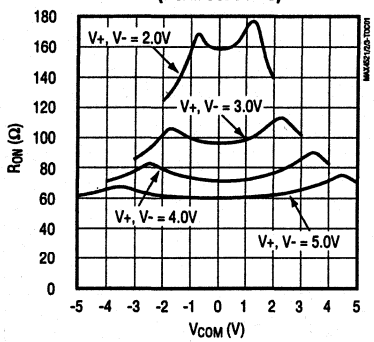
Note 3: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.
Note 4: Guaranteed by design.
Note 5: $\Delta R_{ON} = \Delta R_{ON(MAX)} - \Delta R_{ON(MIN)}$.
Note 6: Resistance flatness is defined as the difference between the maximum and minimum on-resistance values, as measured over the specified analog signal range.
Note 7: Leakage parameters are 100% tested at maximum rated temperature, and guaranteed by correlation at T_A = +25°C.
Note 8: Off-isolation = 20log10 [$V_{COM_}$ / ($V_{NC_}$ or $V_{NO_}$)], $V_{COM_}$ = output, $V_{NC_}$ or $V_{NO_}$ = input to off switch.
Note 9: Between any two switches.
Note 10: Leakage testing for single-supply operation is guaranteed by testing with dual supplies.

Quad, Low-Voltage, SPST Analog Switches

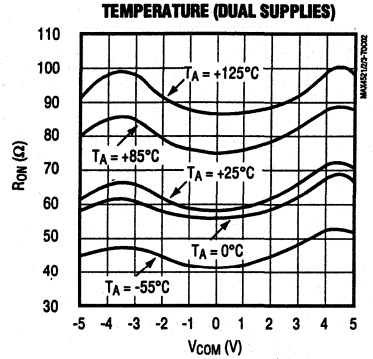
Typical Operating Characteristics

(V+ = +5V, V- = -5V, GND = 0V, T_A = +25°C, unless otherwise noted.)

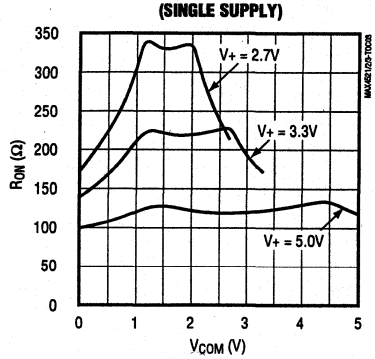
ON-RESISTANCE vs. VCOM (DUAL SUPPLIES)



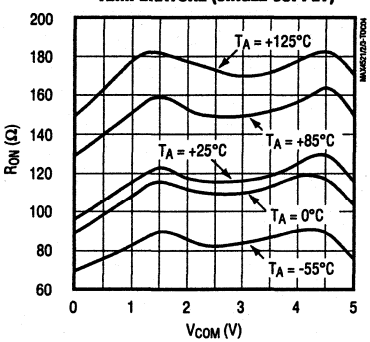
ON-RESISTANCE vs. VCOM AND TEMPERATURE (DUAL SUPPLIES)



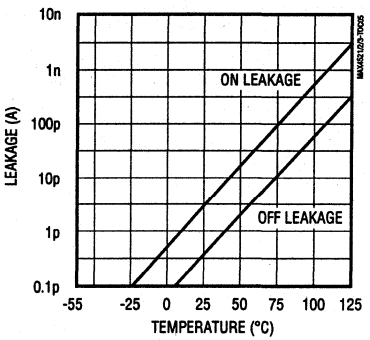
ON-RESISTANCE vs. VCOM (SINGLE SUPPLY)



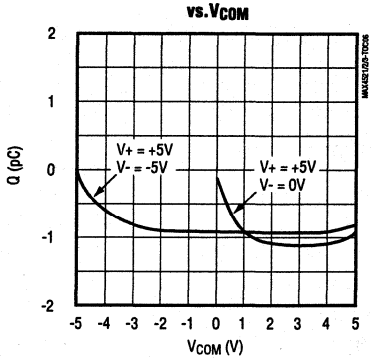
ON-RESISTANCE vs. VCOM AND TEMPERATURE (SINGLE SUPPLY)



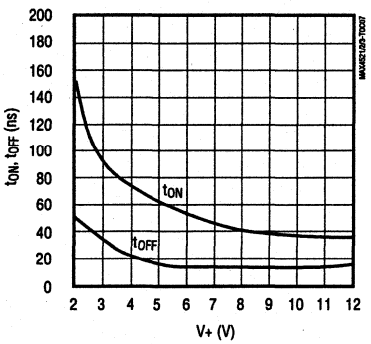
ON- AND OFF-LEAKAGE CURRENT vs. TEMPERATURE



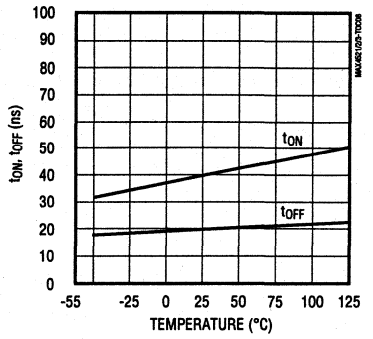
CHARGE INJECTION vs. VCOM



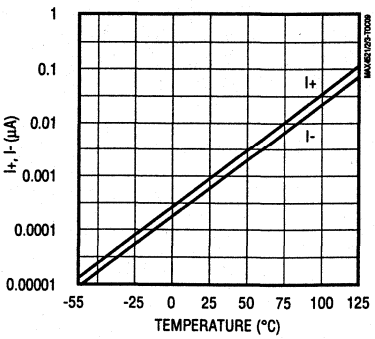
TURN-ON/OFF TIME vs. SUPPLY VOLTAGE



TURN-ON/OFF TIME vs. TEMPERATURE

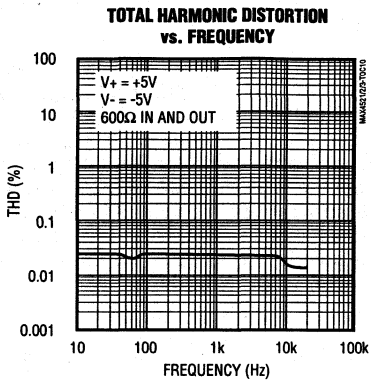


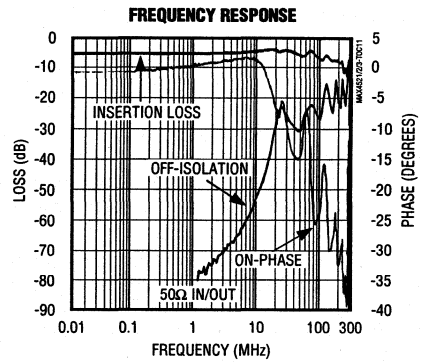
POWER-SUPPLY CURRENT vs. TEMPERATURE



Typical Operating Characteristics (continued)

(V+ = +5V, V- = -5V, GND = 0V, T_A = +25°C, unless otherwise noted.)





Pin Description

PIN			NAME	FUNCTION
MAX4521	MAX4522	MAX4523		
1, 16, 9, 8	1, 16, 9, 8	1, 16, 9, 8	IN1–IN4	Logic-Control Digital Inputs
2, 15, 10, 7	2, 15, 10, 7	2, 15, 10, 7	COM1–COM4	Analog Switch Common* Terminals
3, 14, 11, 6	—	—	NC1–NC4	Analog Switch Normally Closed Terminals
—	3, 14, 11, 6	—	NO1–NO4	Analog Switch Normally Open Terminals
—	—	3, 6	NO1, NO4	Analog Switch Normally Open Terminals
—	—	14, 11	NC2, NC3	Analog Switch Normally Closed Terminals
4	4	4	V-	Negative Analog Supply-Voltage Input. Connect to GND for single-supply operation.
5	5	5	GND	Ground. Connect to digital ground. (Analog signals have no ground reference; they are limited to V+ and V-.)
12	12	12	N.C.	No Connect. Not internally connected.
13	13	13	V+	Positive Analog and Digital Supply Voltage Input. Internally connected to substrate.

**NO_ (or NC_) and COM_ pins are identical and interchangeable. Either may be considered as an input or output; signals pass equally well in either direction.*

Quad, Low-Voltage, SPST Analog Switches

Applications Information

Power-Supply Considerations

Overview

The MAX4521/MAX4522/MAX4523 construction is typical of most CMOS analog switches. They have three supply pins: V+, V-, and GND. V+ and V- are used to drive the internal CMOS switches, and they set the limits of the analog voltage on any switch. Reverse ESD-protection diodes are internally connected between each analog-signal pin and both V+ and V-. If any analog signal exceeds V+ or V-, one of these diodes conducts. During normal operation these reverse-biased ESD diodes leak, forming the only current drawn from V+ or V-.

Virtually all the analog leakage current is through the ESD diodes. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or V- and the analog signal. This means their leakages vary as the signal varies. The *difference* in the two diode leakages from the signal path to the V+ and V- pins constitutes the analog-signal-path leakage current. All analog leakage current flows to the supply terminals, not to the other switch terminal. This explains how both sides of a given switch can show leakage currents of the same or opposite polarity.

There is no connection between the analog-signal paths and GND. The analog-signal paths consist of an N-channel and P-channel MOSFET with their sources and drains paralleled, and their gates driven out of phase to V+ and V- by the logic-level translators.

V+ and GND power the internal logic and logic-level translators, and set the input logic thresholds. The logic-level translators convert the logic levels to switched V+ and V- signals, to drive the gates of the analog switches. This drive signal is the only connection between the logic supplies and the analog supplies. V+ and V- have ESD-protection diodes to GND. The logic-level inputs and output have ESD protection to V+ and to GND.

Increasing V- has no effect on the logic-level thresholds, but it does increase the drive to the P-channel switches, reducing their on-resistance. V- also sets the negative limit of the analog-signal voltage.

The logic-level thresholds are CMOS/TTL compatible when V+ = +5V. The threshold increases slightly as V+ is raised, and when V+ reaches +12V, the level threshold is about 3.1V. This is above the TTL output high-level minimum of 2.8V, but still compatible with CMOS outputs.

Bipolar Supplies

The MAX4521/MAX4522/MAX4523 operate with bipolar supplies between ±2V and ±6V. The V+ and V- supplies need not be symmetrical, but their sum cannot exceed the absolute maximum rating of 13.0V. **Do not connect the MAX4521/MAX4522/MAX4523 V+ to +3V, and then connect the logic-level-input pins to TTL logic-level signals. TTL logic-level outputs in excess of the absolute maximum ratings can damage the part and/or external circuits.**

Caution: The absolute maximum V+ to V- differential voltage is 13.0V. Typical ±6V or 12V supplies with ±10% tolerances can be as high as 13.2V. This voltage can damage the MAX4521/MAX4522/MAX4523. Even ±5% tolerance supplies may have overshoot or noise spikes that exceed 13.0V.

Single Supply

The MAX4521/MAX4522/MAX4523 operate from a single supply between +2V and +12V when V- is connected to GND. All of the bipolar precautions must be observed.

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat up to 50MHz (see *Typical Operating Characteristics*). Above 20MHz, the on-response has several minor peaks that are highly layout dependent. The problem with high-frequency operation is not turning the switch on, but turning it off. The off-state switch acts like a capacitor and passes higher frequencies with less attenuation. At 10MHz, off-isolation is about -52dB in 50Ω systems, becoming worse (approximately 20dB per decade) as frequency increases. Higher circuit impedances also make off-isolation worse. Adjacent channel attenuation is about 3dB above that of a bare IC socket, and is due entirely to capacitive coupling.

Test Circuits/Timing Diagrams

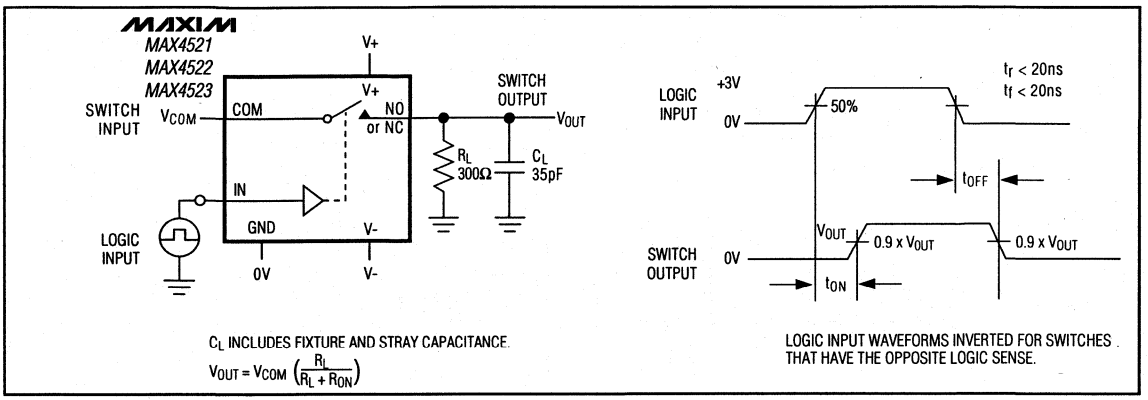


Figure 1. Switching Time

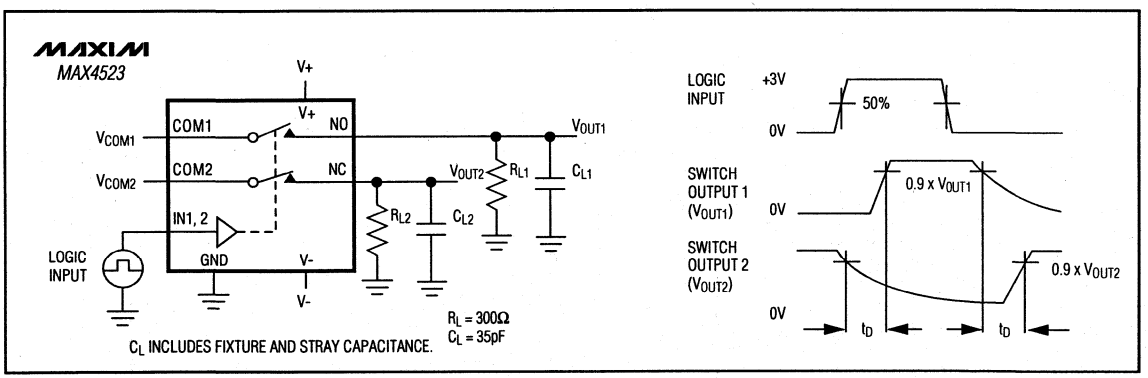


Figure 2. Break-Before-Make Interval (MAX4523 only)

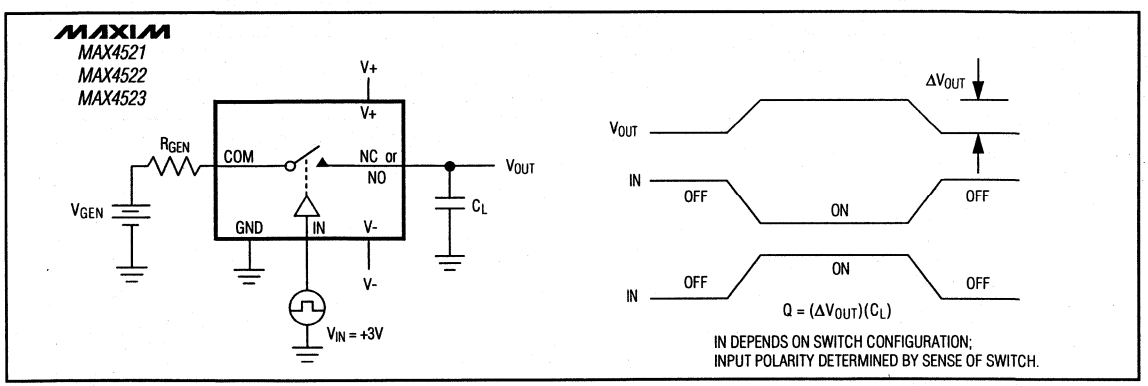


Figure 3. Charge Injection

Test Circuits/Timing Diagrams (continued)

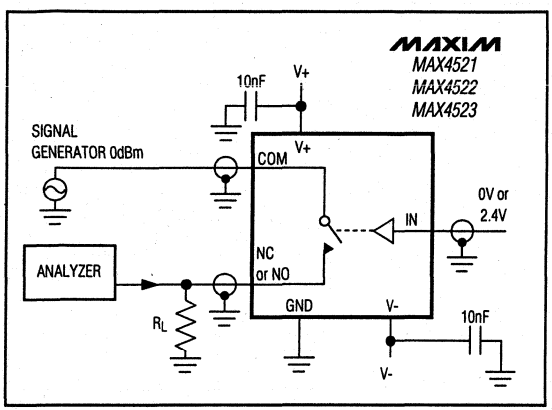


Figure 4. Off Isolation

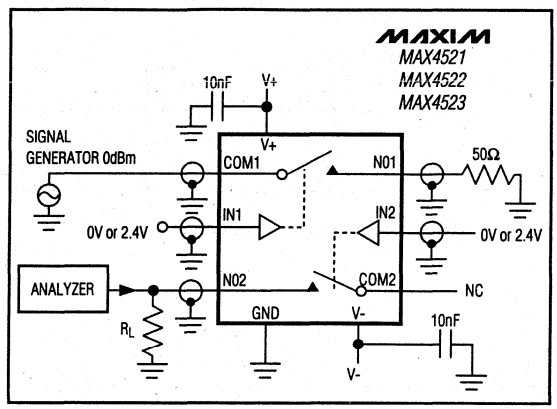


Figure 5. Crosstalk

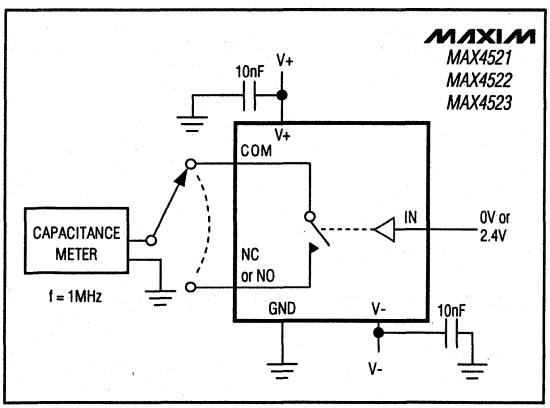


Figure 6. Channel-Off Capacitance

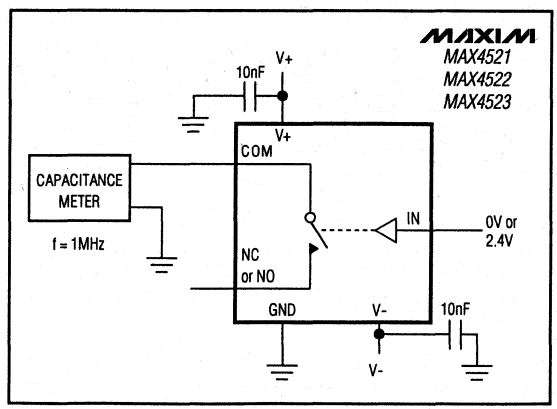


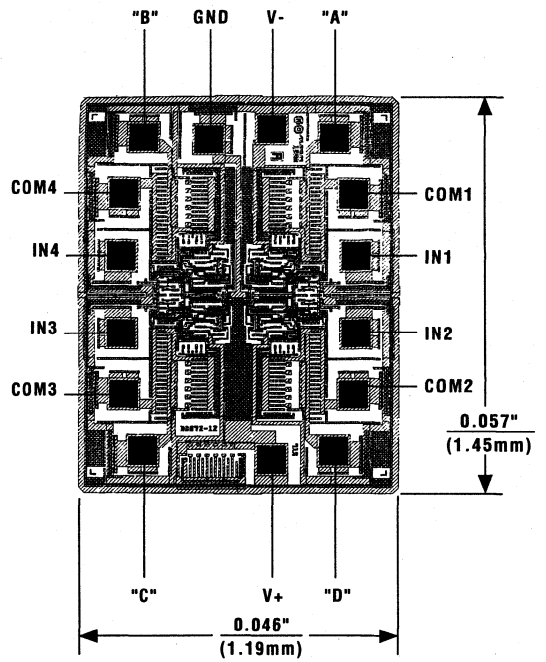
Figure 7. Channel-On Capacitance

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX4521EPE	-40°C to +85°C	16 Plastic DIP
MAX4521ESE	-40°C to +85°C	16 Narrow SO
MAX4521EEE	-40°C to +85°C	16 QSOP
MAX4521MJE	-55°C to +125°C	16 CERDIP**
MAX4522CPE	0°C to +70°C	16 Plastic DIP
MAX4522CSE	0°C to +70°C	16 Narrow SO
MAX4522CEE	0°C to +70°C	16 QSOP
MAX4522C/D	0°C to +70°C	Dice*
MAX4522EPE	-40°C to +85°C	16 Plastic DIP
MAX4522ESE	-40°C to +85°C	16 Narrow SO
MAX4522EEE	-40°C to +85°C	16 QSOP
MAX4522MJE	-55°C to +125°C	16 CERDIP**
MAX4523CPE	0°C to +70°C	16 Plastic DIP
MAX4523CSE	0°C to +70°C	16 Narrow SO
MAX4523CEE	0°C to +70°C	16 QSOP
MAX4523C/D	0°C to +70°C	Dice*
MAX4523EPE	-40°C to +85°C	16 Plastic DIP
MAX4523ESE	-40°C to +85°C	16 Narrow SO
MAX4523EEE	-40°C to +85°C	16 QSOP
MAX4523MJE	-55°C to +125°C	16 CERDIP**

*Contact factory for dice specifications.
**Contact factory for availability.

Chip Topography



MAX4521		MAX4522		MAX4523	
PIN	NAME	PIN	NAME	PIN	NAME
A	NC1	A	NO1	A	NO1
B	NC4	B	NO4	B	NO4
C	NC3	C	NO3	C	NC3
D	NC2	D	NO2	D	NC2

TRANSISTOR COUNT: 97
SUBSTRATE CONNECTED TO V+

ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
10/96

MAXIM

Phase-Reversal Analog Switches

General Description

The MAX4526/MAX4527 are CMOS analog ICs configured as phase-reversal switches. The MAX4526 is optimized for high-speed applications such as chopper amplifiers, while the MAX4527 is optimized for low-power applications.

The MAX4526/MAX4527 operate from a single supply of +4.5V to +36V or dual supplies of ±4.5V to ±18V. On-resistance (175Ω max) is matched between switches to 8Ω max. Each switch can handle rail-to-rail analog signals. The off-leakage current is only 1nA at +25°C and 20nA at +85°C.

All digital inputs have +0.8V and +2.4V logic thresholds, ensuring both TTL- and CMOS-logic compatibility.

Features

- ♦ **Low Charge Injection: <10pC**
- ♦ **Low Charge-Injection Match: <2pC**
- ♦ **±4.5V to ±18V Dual Supplies**
- ♦ **175Ω Signal Paths with ±15V Supplies**
- ♦ **Rail-to-Rail Signal Handling**
- ♦ **t_{ON} and t_{OFF} = 150ns and 120ns (@ ±15V)**
- ♦ **Low Power Consumption: 200µA (MAX4527)**
- ♦ **>2kV ESD Protection per Method 3015.7**
- ♦ **TTL/CMOS-Compatible Inputs**
- ♦ **Small Packages: 8-Pin µMAX/SO/DIP**

Ordering Information

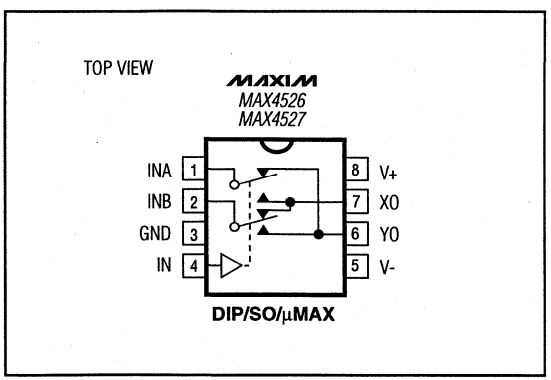
PART	TEMP. RANGE	PIN-PACKAGE
MAX4526CPA	0°C to +70°C	8 Plastic DIP
MAX4526CSA	0°C to +70°C	8 SO
MAX4526CUA	0°C to +70°C	8 µMAX
MAX4526C/D	0°C to +70°C	Dice*
MAX4526EPA	-40°C to +85°C	8 Plastic DIP
MAX4526ESA	-40°C to +85°C	8 SO
MAX4526EUA	-40°C to +85°C	8 µMAX
MAX4527CPA	0°C to +70°C	8 Plastic DIP
MAX4527CSA	0°C to +70°C	8 SO
MAX4527CUA	0°C to +70°C	8 µMAX
MAX4527C/D	0°C to +70°C	Dice*
MAX4527EPA	-40°C to +85°C	8 Plastic DIP
MAX4527ESA	-40°C to +85°C	8 SO
MAX4527EUA	-40°C to +85°C	8 µMAX

**Contact factory for availability.*

Applications

Chopper-Stabilized Amplifiers
Data Acquisition
Test Equipment
Audio Signal Routing

Pin Configuration/ Functional Diagram



DIP/SO/µMAX

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

10/96

MAXIM

Low-Voltage, CMOS Analog Multiplexers/Switches

General Description

The MAX4530/MAX4531/MAX4532 are low-voltage CMOS analog ICs configured as an 8-channel multiplexer (MAX4530), two 4-channel multiplexers (MAX4531), and three single-pole/double-throw switches (MAX4532). These devices are pin compatible with the industry-standard 74HC4351/74HC4352/74HC4353. They have two complementary switch-enable inputs and address latching.

The MAX4530/MAX4531/MAX4532 operate from a single supply of +2V to +12V or dual supplies of ±2V to ±6V. On-resistance (150Ω max) is matched between switches to 8Ω max. Each switch can handle rail-to-rail analog signals. The off-leakage current is only 1nA at +25°C and 10nA at +85°C.

All digital inputs have +0.8V and +2.4V logic thresholds, ensuring both TTL- and CMOS-logic compatibility when using ±5V or a single +5V supply.

Applications

Battery-Operated Equipment
Data Acquisition
Test Equipment
Avionics
Networking
ATE Equipment
Audio Signal Routing

Features

- **Pin Compatible with 74HC4351/74HC4352/74HC4353**
- **±2.0V to ±6V Dual Supplies +2.0V to +12V Single Supply**
- **75Ω Signal Paths with ±5V Supplies 150Ω Signal Paths with +5V Supply**
- **Rail-to-Rail Signal Handling**
- **t_{ON} and t_{OFF} = 150ns and 120ns (@ ±4.5V)**
- **Low Power Consumption: <1µW**
- **>2kV ESD Protection per Method 3015.7**
- **TTL/CMOS-Compatible Inputs**
- **Small Packages: 20-Pin SO, DIP, SSOP**

Ordering Information

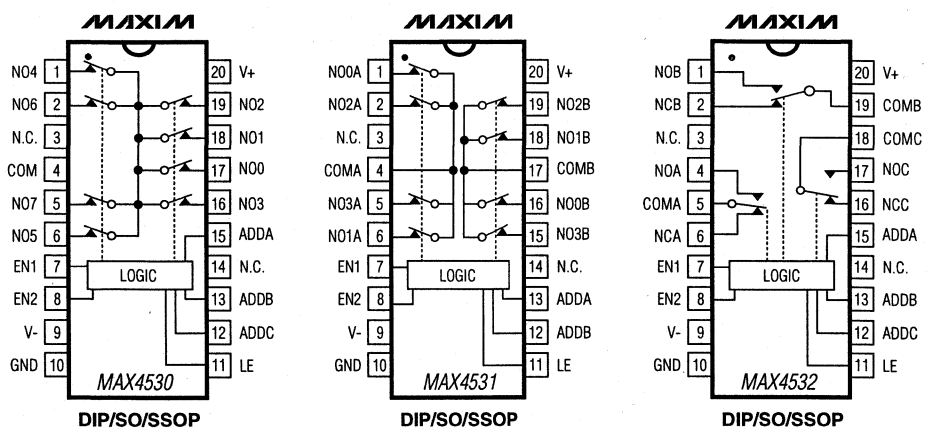
PART	TEMP. RANGE	PIN-PACKAGE
MAX4530CPP	0°C to +70°C	20 Plastic DIP
MAX4530CWP	0°C to +70°C	20 SO
MAX4530CAP	0°C to +70°C	20 SSOP
MAX4530C/D	0°C to +70°C	Dice*

Ordering Information continued on next page.

**Contact factory for availability.*

Pin Configurations

TOP VIEW



N.C. = NOT CONNECTED

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Low-Voltage, CMOS Analog Multiplexers/Switches

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX4530EPP	-40°C to +85°C	20 Plastic DIP
MAX4530EWP	-40°C to +85°C	20 SO
MAX4530EAP	-40°C to +85°C	20 SSOP
MAX4531CPP	0°C to +70°C	20 Plastic DIP
MAX4531CWP	0°C to +70°C	20 SO
MAX4531CAP	0°C to +70°C	20 SSOP
MAX4531C/D	0°C to +70°C	Dice*
MAX4531EPP	-40°C to +85°C	20 Plastic DIP
MAX4531EWP	-40°C to +85°C	20 SO
MAX4531EAP	-40°C to +85°C	20 SSOP
MAX4532CPP	0°C to +70°C	20 Plastic DIP
MAX4532CWP	0°C to +70°C	20 SO
MAX4532CAP	0°C to +70°C	20 SSOP
MAX4532C/D	0°C to +70°C	Dice*
MAX4532EPP	-40°C to +85°C	20 Plastic DIP
MAX4532EWP	-40°C to +85°C	20 SO
MAX4532EAP	-40°C to +85°C	20 SSOP

Contact factory for availability.

ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
10/96

MAXIM

Quad, Low-Voltage, SPST Analog Switches

General Description

The MAX4536/MAX4537/MAX4538 are quad, low-voltage, single-pole/single-throw (SPST) analog switches that are pin compatible with the industry-standard 74HC4316. The MAX4536 has four normally open (NO) switches, and the MAX4537 has four normally closed (NC) switches. The MAX4538 has two NO switches and two NC switches.

These devices operate from a single supply of +2V to +12V or dual supplies of ±2V to ±6V. On-resistance (100Ω max) is matched between switches to 4Ω max and is flat (10Ω max) over the specified signal range. Each switch can handle rail-to-rail analog signals. The off-leakage current is only 1nA at +25°C and 10nA at +85°C.

All digital inputs have +0.8V and +2.4V logic thresholds, ensuring both TTL- and CMOS-logic compatibility when using ±5V or a single +5V supply.

Applications

Battery-Operated Equipment
Data Acquisition
Test Equipment
Avionics
ATE Equipment
Audio Signal Routing
Networking

Features

- ♦ **Pin Compatible with 74HC4316**
- ♦ **±2.7V to ±6V Dual Supplies**
  +2V to +12V Single Supply
- ♦ **4 Separately Controlled SPST Switches with Single Enable**
- ♦ **100Ω Signal Paths with ±5V Supplies**
  200Ω Signal Paths with +4.5V Supply
- ♦ **Rail-to-Rail Signal Handling**
- ♦ **t_{ON} and t_{OFF} = 100ns and 80ns (@ ±4.5V)**
- ♦ **Low Power Consumption: <1µW**
- ♦ **>2kV ESD Protection per Method 3015.7**
- ♦ **TTL/CMOS-Compatible Inputs**
- ♦ **Small Packages: Narrow SO, DIP, QSOP**

Ordering Information

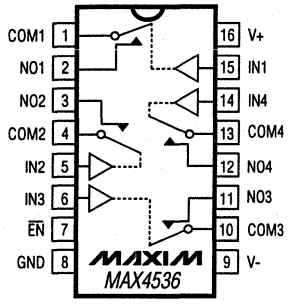
PART	TEMP. RANGE	PIN-PACKAGE
MAX4536CPE	0°C to +70°C	16 Plastic DIP
MAX4536CSE	0°C to +70°C	16 Narrow SO
MAX4536CEE	0°C to +70°C	16 QSOP
MAX4536C/D	0°C to +70°C	Dice*
MAX4536EPE	-40°C to +85°C	16 Plastic DIP
MAX4536ESE	-40°C to +85°C	16 Narrow SO
MAX4536EEE	-40°C to +85°C	16 QSOP
MAX4537CPE	0°C to +70°C	16 Plastic DIP
MAX4537CSE	0°C to +70°C	16 Narrow SO
MAX4537CEE	0°C to +70°C	16 QSOP
MAX4537C/D	0°C to +70°C	Dice*
MAX4537EPE	-40°C to +85°C	16 Plastic DIP
MAX4537ESE	-40°C to +85°C	16 Narrow SO
MAX4537EEE	-40°C to +85°C	16 QSOP
MAX4538CPE	0°C to +70°C	16 Plastic DIP
MAX4538CSE	0°C to +70°C	16 Narrow SO
MAX4538CEE	0°C to +70°C	16 QSOP
MAX4538C/D	0°C to +70°C	Dice*
MAX4538EPE	-40°C to +85°C	16 Plastic DIP
MAX4538ESE	-40°C to +85°C	16 Narrow SO
MAX4538EEE	-40°C to +85°C	16 QSOP

**Contact factory for availability.*

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

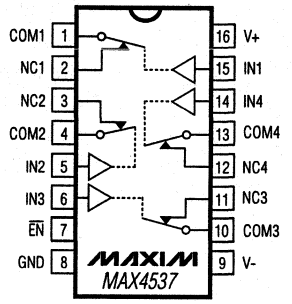
Quad, Low-Voltage, SPST Analog Switches

Pin Configurations/Functional Diagrams/Truth Tables



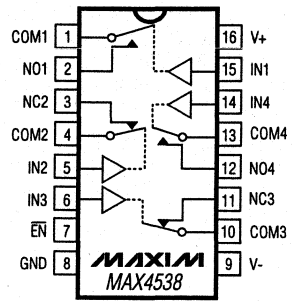
DIP/SO/QSOP

MAX4536		
$\overline{EN}$	IN_	SWITCH_
0	0	OFF
0	1	ON
1	X	OFF



DIP/SO/QSOP

MAX4537		
$\overline{EN}$	IN_	SWITCH_
0	0	ON
0	1	OFF
1	X	OFF



DIP/SO/QSOP

MAX4538			
$\overline{EN}$	IN_	SWITCHES 1, 4	SWITCHES 2, 3
0	0	OFF	ON
0	1	ON	OFF
1	X	OFF	OFF

SWITCHES SHOWN FOR LOGIC "0" INPUT

MAXIM

Interface Products

Interface Products, Product Tables and Trees 2-3

MAX202E	±15kV ESD-Protected, 5V RS-232 Transceiver	2-9
MAX203E	±15kV ESD-Protected, Complete, 5V, Dual RS-232 Transceiver	2-9
MAX205E	±15kV ESD-Protected, 5-Driver/5-Receiver, +5V, RS-232 Transceiver with Shutdown	2-9
MAX206E	±15kV ESD-Protected, 4-Driver/3-Receiver, +5V, RS-232 Transceiver with Shutdown	2-9
MAX207E	±15kV ESD-Protected, 5-Driver/3-Receiver, +5V, RS-232 Transceiver	2-9
MAX208E	±15kV ESD-Protected, 4-Driver/4-Receiver, +5V, RS-232 Transceiver	2-9
MAX211E	±15kV ESD-Protected, 5V RS-232 Transceiver	2-9
MAX213E	±15kV ESD-Protected, 5V RS-232 Transceiver	2-9
MAX232E	±15kV ESD-Protected, 5V RS-232 Transceiver	2-9
MAX241E	±15kV ESD-Protected, 5V RS-232 Transceiver	2-9
MAX481E	2.5Mbps, ±15kV ESD-Protected, Low-Power RS-485/RS-422 Transceiver	2-31
MAX483E	250kbps, ±15kV ESD-Protected, Low-Power RS-485/RS-422 Transceiver with Shutdown	2-31
MAX485E	2.5Mbps, ±15kV ESD-Protected, Low-Power RS-485/RS-422 Transceiver	2-31
MAX487E	250kbps, ±15kV ESD-Protected, Low-Power RS-485/RS-422 Transceiver with 1/4-Unit Load	2-31
MAX488E	250kbps, ±15kV ESD-Protected, Low-Power, Full-Duplex RS-485/RS-422 Transceiver	2-31
MAX489E	250kbps, ±15kV ESD-Protected, Low-Power, Full-Duplex RS-485/RS-422 Transceiver	2-31
MAX490E	2.5Mbps, ±15kV ESD-Protected, Low-Power RS-485/RS-422 Transceiver	2-31
MAX491E	2.5Mbps, ±15kV ESD-Protected, Low-Power RS-485/RS-422 Transceiver	2-31
MAX1406	±15kV ESD-Protected, EMC-Compliant, 230kbps, 3-Tx/3-Rx RS-232 IC	2-47
MAX1480A/B	Complete, Isolated RS-485/RS-422 Data Interface IC	2-55
MAX1487E	2.5Mbps, ±15kV ESD-Protected, Low-Power, RS-485/RS-422 Transceiver	2-31
MAX1488E	±15kV ESD-Protected, Quad, Low-Power RS-232 Line Driver	2-75
MAX1489E	±15kV ESD-Protected, Quad, Low-Power RS-232 Line Receiver	2-81
MAX1490A/B	Complete, Isolated, Full-Duplex RS-485/RS-422 Data Interface IC	2-55
MAX3080	Fail-Safe, 115kbps, Slew-Rate-Limited, Full-Duplex RS-485/RS-422 Transceiver	2-87
MAX3081	Fail-Safe, 115kbps, Slew-Rate-Limited, Full-Duplex RS-485/RS-422 Transceiver	2-87
MAX3082	Fail-Safe, 115kbps, Slew-Rate-Limited, Half-Duplex RS-485/RS-422 Transceiver	2-87
MAX3083	Fail-Safe, 500kbps, Slew-Rate-Limited, Full-Duplex RS-485/RS-422 Transceiver	2-87
MAX3084	Fail-Safe, 500kbps, Slew-Rate-Limited, Full-Duplex RS-485/RS-422 Transceiver	2-87
MAX3085	Fail-Safe, 500kbps, Slew-Rate-Limited, Half-Duplex RS-485/RS-422 Transceiver	2-87
MAX3086	Fail-Safe, 10Mbps, Full-Duplex RS-485/RS-422 Transceiver	2-87
MAX3087	Fail-Safe, 10Mbps, Full-Duplex RS-485/RS-422 Transceiver	2-87
MAX3088	Fail-Safe, 10Mbps, Half-Duplex RS-485/RS-422 Transceiver	2-87
MAX3089	Fail-Safe, 115kbps/500kbps/10Mbps, Half or Full-Duplex RS-485/RS-422 Transceiver	2-87
MAX3185	±15kV ESD-Protected, EMC-Compliant, 230kbps, RS-232 Serial Port for Motherboards/Desktop PCs	2-107
MAX3186	±15kV ESD-Protected, EMC-Compliant, 230kbps, RS-232 Serial Port for Modems	2-115
MAX3221	True 3V to 5.5V, RS-232 Transceiver with AutoShutdown Draws 1µA	2-123
MAX3222	300µA, 2-Driver/2-Receiver, True RS-232 Transceiver Using Four 0.1µF Capacitors	2-137

Interface Products (continued)

MAX3223	1µA, 3V to 5.5V, True RS-232 Transceiver with AutoShutdown	2-123
MAX3232	300µA, 2-Driver/2-Receiver, True RS-232 Transceiver Using Four 0.1µF Capacitors	2-137
MAX3237	500µA, 5-Driver/3-Receiver, True RS-232 Transceiver with 1Mbps Data Rate, Using Four 0.1µF Capacitors	2-137
MAX3238	Low-Power, 250kbps, True RS-232 Transceiver with AutoShutdown Plus	2-153
MAX3241	300µA, 3-Driver/5-Receiver, True RS-232 Transceiver Using Four 0.1µF Capacitors	2-137
MAX3243	1µA, 3V to 5.5V, True RS-232 Transceiver with AutoShutdown	2-123
MAX3480A/B	Complete, Isolated, 3.3V RS-485/RS-422 Data Interface IC	2-165

Line Drivers/Receivers

see next page for RS-485/RS-422

AppleTalk™

MAX216 (1 single-ended driver/2-single-ended receivers, 1 differential driver/1 differential receiver)

RS-232

+3V Powered

MegaBaud™ Mode

★ MAX3237 (1Mbps data rate in MegaBaud mode, 5Tx, 3Rx)

4 DRVRs, 5 RCVRs

MAX560 (2 receivers active in shutdown)
MAX561 (shutdown)

Complete PC Serial Ports

☆ MAX212 (true RS-232, 3mA I_{CC} max)
MAX3241 (true RS-232, 0.1µF caps, 1mA I_{CC} max)
MAX562 (2.7V to 5.25V operation)

2 DRVRs, 2 RCVRs

MAX218 (1.8V to 4.25V V_{CC} in, true RS-232 out)
MAX3222 (true RS-232, 0.1µF caps, 2 receivers active in shutdown)
MAX3232 (true RS-232, 0.1µF caps)
MAX563 (120kbps data rate, 2 receivers active in shutdown)

1µA Supply Current

MAX3212 (3Tx, 5Rx, 2.7V to 3.6V operation)
MAX3218 (2Tx, 2Rx, 1.8V to 4.25V operation)
★ MAX3221 (1Tx, 1Rx, 3.0V to 5.5V operation, 0.1µF caps)
MAX3223 (2Tx, 2Rx, 3.0V to 5.5V operation, 0.1µF caps)
★ MAX3238 (5Tx, 3Rx, 3.0V to 5.5V operation, 0.1µF caps)
MAX3243 (3Tx, 5Rx, 3.0V to 5.5V operation, 0.1µF caps)

+5V, 4 Ext. Caps

2 DRVRs, 2 RCVRs

MAX202 (0.1µF caps, low cost)
MAX220 (ultra-low power)
MAX222 (I_Q = 10µA in shutdown)
MAX232 (industry standard)
MAX232A (116kbits/sec data rate, 0.1µF caps)
MAX242 (receivers active in shutdown)
MAX243 (simplified cabling)

Complete PC Serial Ports

MAX211 (pin compatible with MAX241, 0.1µF caps)
MAX213 (2 receivers active in shutdown, 0.1µF caps)
MAX214 (programmable DTE/DCE port)
MAX223 (2 receivers active in shutdown)
MAX241 (industry standard)

High DRVR/RCVR Count

MAX200 (5 drivers, 0 receivers, 0.1µF caps)
MAX204 (4 drivers, 0 receivers, 0.1µF caps)
MAX206 (4 drivers, 3 receivers, 0.1µF caps)
MAX207 (5 drivers, 3 receivers, 0.1µF caps)
MAX208 (4 drivers, 4 receivers, 0.1µF caps)
MAX230 (5 drivers, 0 receivers)
MAX234 (4 drivers, 0 receivers)
MAX236 (4 drivers, 3 receivers)
MAX237 (5 drivers, 3 receivers)
MAX238 (4 drivers, 4 receivers)
MAX240 (5 drivers, 5 receivers)
MAX244 (8 drivers, 10 receivers)
MAX248 (8 drivers, 8 receivers)
MAX249 (8 drivers, 10 receivers)

+5V, Internal Caps

2 DRVRs, 2 RCVRs

MAX203 (available in SO)
MAX233
MAX233A (116kbits/sec)

High DRVR/RCVR Count

MAX205 (5 drivers, 5 receivers)
MAX225 (5 drivers, 5 receivers, SO package)
MAX235 (5 drivers, 5 receivers)
MAX245 (8 drivers, 10 receivers)
MAX246 (8 drivers, 10 receivers)
MAX247 (8 drivers, 9 receivers)

±15kV ESD Protection

+5V, ±12V

★ MAX1406 (3Tx/3Rx, ±15kV ESD per human body model & IEC 1000-4-2)
MAX1488E (4Tx, ±15kV ESD per human body model & IEC 1000-4-2)
MAX1489E (4Rx, ±15kV ESD per human body model & IEC 1000-4-2)
★ MAX3185 (3Tx/5Rx, ±15kV ESD per human body model & IEC 1000-4-2)
★ MAX3186 (5Tx/3Rx, ±15kV ESD per human body model & IEC 1000-4-2)

+5V

MAX202E (2Tx/2Rx, ±15kV ESD per human body model & IEC 1000-4-2)
MAX203E (2Tx/2Rx, ±15kV ESD per human body model & IEC 1000-4-2, no external caps)
★ MAX205E (5Tx/5Rx, ±15kV ESD per human body model & IEC 1000-4-2, no external caps)
★ MAX206E (4Tx/3Rx, ±15kV ESD per human body model & IEC 1000-4-2)
★ MAX207E (5Tx/3Rx, ±15kV ESD per human body model & IEC 1000-4-2)
★ MAX208E (4Tx/4Rx, ±15kV ESD per human body model & IEC 1000-4-2)
MAX211E (4Tx/5Rx, ±15kV ESD per human body model & IEC 1000-4-2)
MAX213E (4Tx/5Rx, ±15kV ESD per human body model & IEC 1000-4-2)
MAX232E (2Tx/2Rx, ±15kV ESD per human body model & IEC 1000-4-2)
MAX241E (4Tx/5Rx, ±15kV ESD per human body model & IEC 1000-4-2)

Isolation Products

2-Chip Set

MAX250
MAX251

Complete Module

MAX252A (UL recognized)
MAX252B (500V isolation)

+5V/+12V or Battery Power, 2 Ext. Caps

2 DRVRs, 2 RCVRs

MAX201 (0.1µF caps)
MAX231

Complete PC Serial Ports

MAX209 (3 drivers, 5 receivers, 0.1µF caps)
MAX239 (3 drivers, 5 receivers)

★ New product
☆ Evaluation kit available
AppleTalk is a trademark of Apple Computer, Inc.

Line Drivers/Receivers

see previous page for RS-232/AppleTalk™

RS-485/RS-422

+5V Powered

Fail-Safe Operation

- ★ MAX3080 (full-duplex, 115kbps)
- ★ MAX3081 (full-duplex, 115kbps)
- ★ MAX3082 (half-duplex, 115kbps)
- ★ MAX3083 (full-duplex, 0.5Mbps)
- ★ MAX3084 (full-duplex, 0.5Mbps)
- ★ MAX3085 (half-duplex, 0.5Mbps)
- ★ MAX3086 (full-duplex, 10Mbps)
- ★ MAX3087 (full-duplex, 10Mbps)
- ★ MAX3088 (half-duplex, 10Mbps)
- ★ MAX3089 (full/half-duplex selectability, selectable data rate)

±15kV, ESD Protection

- MAX1487E (MAX485E plus 1/4-unit load)
- MAX481E (1µA shutdown, half duplex)
- MAX483E (250kbps, reduces EMI by 100x)
- MAX485E (industry standard with ±15kV ESD)
- MAX487E (MAX483E plus 1/4-unit load)
- MAX488E (250kbps, reduces EMI by 100x)
- MAX489E (MAX488E plus driver/receiver enable)
- MAX490E (2.5Mbps)
- MAX491E (MAX490E plus driver/receiver enable)

1 DRVR, 1 RCVR Full Duplex

- MAX1482 (250kbps, 256 transceivers on the bus)
- MAX488 (250kbps, reduces EMI by 100x)
- MAX489 (MAX488 plus driver/receiver enables)
- MAX490 (direct LTC490 replacement)
- MAX491 (direct LTC491 replacement)

1 DRVR, 1 RCVR Half Duplex

- MAX1483 (250kbps, 256 transceivers on the bus)
- MAX1487 (2.5Mbps, 128 transceivers on the bus)
- MAX481 (MAX485 plus 1µA shutdown)
- MAX483 (250kbps, reduces EMI by 100x)
- MAX485 (direct LTC485 replacement)
- MAX487 (MAX483 plus 1/4-unit load)

Isolation Products

- MAX1480A (complete 2.5Mbps isolated RS-485 in one package)
- MAX1480B (complete 250kbps isolated RS-485 in one package)
- ★ MAX1490A (complete 2.5Mbps isolated RS-485 in one package)
- ★ MAX1490B (complete 250kbps isolated RS-485 in one package)
- MAX253 (isolated power for MAX48x family)

★ New product

+3V Powered

1 DRVR, 1 RCVR Full Duplex

- MAX3488 (250kbps, reduces EMI by 100x)
- MAX3490 (10Mbps, 8-pin package)
- MAX3491 (10Mbps, driver/receiver enables)

1 DRVR, 1 RCVR Half Duplex

- MAX3483 (250kbps, reduces EMI by 100x)
- MAX3485 (10Mbps guaranteed data rate)
- MAX3486 (2.5Mbps guaranteed data rate)

Isolation Products

- ★ MAX3480A (Complete 2.5Mbps, isolated RS-485 in one package)
- ★ MAX3480B (Complete 250kbps, isolated RS-485 in one package)

Part Number	Power Supply (V)	No. of RS-232 Tx/Rx	Supply Current (mA)	No. of Ext. Caps	Nominal Cap. Value (µF)	Shutdown & Three-State	Receivers Active in Shutdown	True RS-232	Data Rate (kbps)	Features
+3V RS-232 PRODUCTS										
MAX212	+3 to +3.6	3/5	1.5	2	0.33/0.68	Yes	✔	Yes	250	5 receivers active in shutdown, I_{CC} = 1.5mA, chip inductor
MAX218	+1.8 to +4.25	2/2	1.9	2	0.33/0.68	Yes	✔	Yes	250	True RS-232 performance from 1.8V to 4.25V input
MAX3212	+2.7 to +3.6	3/5	1µA	2	0.33/0.68	Yes	4	Yes	230	AutoShutdown™ reduces supply current to 1µA
MAX3218	+1.8 to +4.25	2/2	1µA	2	0.33/0.68	Yes	4	Yes	230	AutoShutdown™ reduces supply current to 1µA
MAX3221	+3 to +5.5	1/1	1µA	4	0.1	Yes	✔	Yes	230	AutoShutdown™ reduces supply current to 1µA
MAX3222	+3 to +5.5	2/2	300µA	4	0.1	Yes	4	Yes	230	2 receivers active in shutdown, 0.5mA I_{CC}, true RS-232
MAX3223	+3 to +5.5	2/2	1µA	4	0.1	Yes	4	Yes	230	AutoShutdown™ reduces supply current to 1µA
MAX3232	+3 to +5.5	2/2	300µA	4	0.1	No		Yes	230	Industry-standard MAX232 pinout, true RS-232
MAX3237	+3 to +5.5	5/3	500µA	4	0.1	Yes	✔	Yes	1Mbps	World's fastest RS-232 transceiver at 1Mbps
MAX3238	+3 to +5.5	3/3	1µA	4	0.1	Yes	5	Yes	250	AutoShutdown Plus™ reduces supply current to 1µA
MAX3241	+3 to +5.5	3/5	300µA	4	0.1	Yes	5	Yes	230	Mouse driveability, 2 spare receivers active in shutdown, true RS-232
MAX3243	+3 to +5.5	3/5	1µA	4	0.1	Yes	5	Yes	230	AutoShutdown™ reduces supply current to 1µA
MAX560	+3 to +3.6	4/5	5	4	1	Yes	✔	No	120	+3V, MAX561 with receivers active in shutdown
MAX561	+3 to +3.6	4/5	5	4	1	Yes		No	120	+3V, complete IBM PC serial port
MAX562	+2.7 to +5.25	3/5	20	5	0.33/0.68	Yes	✔	No	250	+2.7V to +5.25V operation, 230kbps guaranteed data rate
MAX563	+3 to +3.6	2/2	4	4	0.1	Yes	✔	No	200	2 receivers active in shutdown
+5V RS-232 PRODUCTS										
MAX214	+5	3/5	9	4	1	Yes		Yes	120	Programmable DTE/DCE port
MAX220	+5	2/2	500µA	4	4.7/10	No		Yes	22	Ultra-low power, industry-standard pinout
MAX222	+5	2/2	4	4	0.1	Yes		Yes	200	+5V IBM PC serial port with receivers active in shutdown
MAX223(MAX213)	+5	4/5	7	4	1(0.1)	Yes	✔	Yes	120	MAX241 + receivers active in shutdown
MAX225	+5	5/5	11	0	–	Yes		Yes	120	Available in 28-pin SO package
MAX230(MAX200)	+5	5/0	7	4	1(0.1)	Yes		Yes	120	5 drivers with shutdown
MAX231(MAX201)	+5 and +7.5 to +13.2	2/2	400µA	2	1(0.1)	No		Yes	120	Standard +5/+12V or battery supplies; same functions as MAX232
MAX232(MAX202)	+5	2/2	5	4	1(0.1)	No		Yes	120(64)	Industry standard
MAX232A	+5	2/2	4	4	0.1	No		Yes	200	High slew rate, small caps, guaranteed 120kbps data rate
MAX233(MAX203)	+5	2/2	5	0	–	No		Yes	120	No external caps, MAX203 available in SOIC
MAX233A	+5	2/2	4	0	–	No		Yes	200	No external caps, high slew rate
MAX234(MAX204)	+5	4/0	7	4	1(0.1)	No		Yes	120	Replaces 1488
MAX235(MAX205)	+5	5/5	7	0	–	Yes		Yes	120	No external caps
MAX236(MAX206)	+5	4/3	7	4	1(0.1)	Yes		Yes	120	Shutdown, three-state
MAX237(MAX207)	+5	5/3	7	4	1(0.1)	No		Yes	120	Complements IBM PC serial port
MAX238(MAX208)	+5	4/4	7	4	1(0.1)	No		Yes	120	Replaces 1488 and 1489
MAX239(MAX209)	+5 and +7.5 to +13.2	3/5	7	2	1(0.1)	No		Yes	120	Standard +5/+12V or battery supplies; single package solution for IBM PC serial port
MAX240	+5	5/5	7	4	1	Yes		Yes	120	DIP or flatpack package
MAX241(MAX211)	+5	4/5	7	4	1(0.1)	Yes		Yes	120	Complete IBM PC serial port, industry standard
MAX242	+5	2/2	4	4	0.1	Yes	✔	Yes	200	Separate shutdown and enable
MAX243	+5	2/2	4	4	0.1	No		Yes	200	Open-line detection simplifies cabling
MAX244	+5	8/10	11	4	1	No		Yes	120	High slew rate
MAX245	+5	8/10	11	0	–	Yes	✔	Yes	120	High slew rate, int. caps, two shutdown modes
MAX246	+5	8/10	11	0	–	Yes	✔	Yes	120	High slew rate, int. caps, three shutdown modes
MAX247	+5	8/9	11	0	–	Yes	✔	Yes	120	High slew rate, int. caps, nine operating modes
MAX248	+5	8/8	11	4	1	Yes	✔	Yes	120	High slew rate, selective half-chip enables
MAX249	+5	6/10	11	4	1	Yes	✔	Yes	120	Available in quad flatpack package

AutoShutdown is a trademark of Maxim Integrated Products.
AutoShutdown Plus is a trademark of Maxim Integrated Products.

Part Number	Power Supply (V)	No. of RS-232 Tx/Rx	Supply Current (mA)	No. of Ext. Caps	Nominal Cap. Value (µF)	Shutdown & Three-State	Receivers Active in Shutdown	True RS-232	Data Rate (kbps)	Features
RS-232 ISOLATION PRODUCTS										
MAX250	+5	2/2	100µA	–	–	Yes		Yes	120	Isolated RS-232 chip set
MAX251	+5	2/2	100µA	–	–	Yes		Yes	120	Isolated RS-232 chip set
MAX252A	+5	2/2	130	0	–	Yes		Yes	20	UL recognized, 1500V isolation
MAX252B	+5	2/2	130	0	–	Yes		Yes	20	Economical 500V isolation

Part Number	Data Rate (Mbps)	No. of RS-485 Drivers/ Receivers	Supply Current (µA)	Shutdown Supply Current (µA)	Duplex	No. of Rx/Tx On Bus	Features
+5V RS-485/RS-422 PRODUCTS							
MAX1482	0.25	1/1	20	0.1	Full	256	250kbps, 256 transceivers on bus
MAX1483	0.25	1/1	20	0.1	Half	256	250kbps, 256 transceivers on bus
MAX1487	2.5	1/1	250	300	Half	128	2.5Mbps, 128 transceivers on bus
MAX481	2.5	1/1	500	1	Half	32	MAX485 + 1µA shutdown mode
MAX483	0.25	1/1	350	1	Half	32	Slew-rate limiting reduces EMI and reflections
MAX485	2.5	1/1	500	300	Half	32	Direct LTC485 replacement
MAX487	0.25	1/1	250	1	Half	128	MAX483 plus 1/4-unit load
MAX488	0.25	1/1	350	–	Full	32	Slew-rate limiting reduces EMI and reflections
MAX489	0.25	1/1	350	1	Full	32	MAX488 plus driver/receiver enable
MAX490	2.5	1/1	500	–	Full	32	Direct LTC490 replacement
MAX491	2.5	1/1	500	300	Full	32	Direct LTC491 replacement
+3V (+3.0V to +3.6V) RS-485/RS-422 PRODUCTS							
MAX3483	0.25	1/1	1mA	1	Half	32	Slew-rate limiting reduces EMI and reflections
MAX3485	10	1/1	1mA	1	Half	32	Guaranteed 10Mbps data rate
MAX3486	2.5	1/1	1mA	1	Half	32	Guaranteed 2.5Mbps data rate
MAX3488	0.25	1/1	1mA	–	Full	32	Slew-rate limiting reduces EMI and reflections
MAX3490	10	1/1	1mA	–	Full	32	Guaranteed 10Mbps data rate
MAX3491	10	1/1	1mA	1	Full	32	MAX3490 plus driver/receiver enable

Part Number	Data Rate (Mbps)	No. of RS-485 Drivers/ Receivers	ESD Voltage (kV)	Supply Current (µA)	Shutdown Supply Current (µA)	Duplex	No. of Rx/Tx On Bus	Features
HIGH ESD RS-485 PRODUCTS								
MAX1487E	2.5	1/1	±15	250	300	Half	128	2.5Mbps, 128 transceivers on bus
MAX481E	2.5	1/1	±15	500	1	Half	32	MAX485 + 1µA shutdown mode
MAX483E	0.25	1/1	±15	350	1	Half	32	Slew-rate limiting reduces EMI and reflections
MAX485E	2.5	1/1	±15	500	300	Half	32	Direct LTC485 replacement
MAX487E	0.25	1/1	±15	250	1	Half	128	MAX483 plus 1/4-unit load
MAX488E	0.25	1/1	±15	350	–	Full	32	Slew-rate limiting reduces EMI and reflections
MAX489E	0.25	1/1	±15	350	1	Full	32	MAX488 plus driver/receiver enable
MAX490E	2.5	1/1	±15	500	–	Full	32	Direct LTC490 replacement
MAX491E	2.5	1/1	±15	500	300	Full	32	Direct LTC491 replacement

Part Number	Half/Full Duplex	Data Rate (Mbps)	Slew-Rate Limited	Low-Power Shutdown	Receiver/ Driver Enable	Quiescent Current (µA)	No. of Transceivers on Bus	Pin Count	Industry-Standard Pinout
FAIL-SAFE PRODUCTS									
MAX3080	Full	0.115	Yes	Yes	Yes	375	256	14	75180
MAX3081	Full	0.115	Yes	No	No	375	256	8	75179
MAX3082	Half	0.115	Yes	Yes	Yes	375	256	8	75176
MAX3083	Full	0.5	Yes	Yes	Yes	375	256	14	75180
MAX3084	Full	0.5	Yes	No	No	375	256	8	75179
MAX3085	Half	0.5	Yes	Yes	Yes	375	256	8	75176
MAX3086	Full	10	No	Yes	Yes	375	256	14	75180
MAX3087	Full	10	No	No	No	375	256	8	75179
MAX3088	Half	10	No	Yes	Yes	375	256	8	75176
MAX3089	Selectable	Selectable	Selectable	Yes	Yes	375	256	14	75180*

Part Number	Power Supply (V)	Data Rate (Mbps)	No. of RS-485 Drivers/ Receivers	Supply Current (mA)	Isolated Power (mW)	Isolation Voltage (V)	Shutdown Supply Current (µA)	Full Duplex	Features
RS-485 ISOLATION PRODUCTS									
MAX1480A	+5	2.5	1/1	55	–	1500	0.2	No	Complete isolated RS-485 in one package
MAX1480B	+5	0.25	1/1	28	–	1500	0.2	No	Complete isolated RS-485 in one package
MAX1490A	+5	2.5	1/1	100	–	1500	0.2	Yes	Complete isolated RS-485 in one package
MAX1490B	+5	0.25	1/1	65	–	1500	0.2	Yes	Complete isolated RS-485 in one package
MAX253	+5	–	–	5	750	–	1	–	Isolated power driver for RS-485
MAX3480A	+3.3	2.5	1/1	180	–	1500	0.2	No	Complete isolated RS-485 in one package
MAX3480B	+3.3	0.25	1/1	120	–	1500	0.2	No	Complete isolated RS-485 in one package

Part Number	Power Supply (V)	No. of Single-Ended Drivers/Receivers	No. of Differential Drivers/Receivers	Shutdown	Single-Ended Data Rate (kbps)	Differential Data Rate (Mbps)	Description
APPLETALK™ TRANSCEIVER							
MAX216	±5	1/2	1/1	Yes	120	1	Complete AppleTalk™ interface

Part Number	Power Supply (V)	No. of RS-232 Drivers/ Receivers	ESD Voltage (kV)	Ext. Caps (µF)	Shutdown & Three-State	Rx Active in Shutdown	Data Rate (kbps)	Features
HIGH ESD RS-232 PRODUCTS								
MAX1406	+5, ±12	3/3	±15	None			230	Ideal for telecom, printers, modems
MAX1488E	+5, ±12	4/0	±15	None			120	±15kV ESD per human body model and ±15kV per IEC 1000-4-2
MAX1489E	+5	0/4	±15	None			120	±15kV ESD per human body model and ±15kV per IEC 1000-4-2
MAX202E	+5	2/2	±15	4 x 0.1			120	±15kV ESD per human body model and ±15kV per IEC 1000-4-2
MAX203E	+5	2/2	±15	None			120	±15kV ESD per human body model and ±15kV per IEC 1000-4-2
MAX205E	+5	5/5	±15	None	Yes		120	±15kV ESD per human body model and ±15kV per IEC 1000-4-2
MAX206E	+5	4/3	±15	4 x 0.1	Yes		120	±15kV ESD per human body model and ±15kV per IEC 1000-4-2
MAX207E	+5	5/3	±15	4 x 0.1			120	±15kV ESD per human body model and ±15kV per IEC 1000-4-2
MAX208E	+5	4/4	±15	4 x 0.1			120	±15kV ESD per human body model and ±15kV per IEC 1000-4-2
MAX211E	+5	4/5	±15	4 x 0.1	Yes		120	±15kV ESD per human body model and ±15kV per IEC 1000-4-2
MAX213E	+5	4/5	±15	4 x 0.1	Yes	✔	120	±15kV ESD per human body model and ±15kV per IEC 1000-4-2
MAX232E	+5	2/2	±15	4 x 1.0			120	±15kV ESD per human body model and ±15kV per IEC 1000-4-2
MAX241E	+5	4/5	±15	4 x 1.0	Yes		120	±15kV ESD per human body model and ±15kV per IEC 1000-4-2
MAX3185	+5, ±12	3/5	±15	None			230	Ideal for desktop PCs and motherboards
MAX3186	+5, ±12	5/3	±15	None			230	Ideal for modems

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19-0175; Rev 3; 5/96

MAXIM

±15kV ESD-Protected, +5V RS-232 Transceivers

General Description

The MAX202E–MAX213E, MAX232E/MAX241E line drivers/receivers are designed for RS-232 and V.28 communications in harsh environments. Each transmitter output and receiver input is protected against ±15kV electrostatic discharge (ESD) shocks, without latchup. The various combinations of features are outlined in the *Selection Guide.* The drivers and receivers for all ten devices meet all EIA/TIA-232E and CCITT V.28 specifications at data rates up to 120kbps, when loaded in accordance with the EIA/TIA-232E specification.

The MAX211E/MAX213E/MAX241E are available in 28-pin SO packages, as well as a 28-pin SSOP that uses 60% less board space. The MAX202E/MAX232E come in 16-pin narrow SO, wide SO, and DIP packages. The MAX203E comes in a 20-pin DIP/SO package, and needs no external charge-pump capacitors. The MAX205E comes in a 24-pin wide DIP package, and also eliminates external charge-pump capacitors. The MAX206E/MAX207E/MAX208E come in 24-pin SO, SSOP, and narrow DIP packages. The MAX232E/MAX241E operate with four 1µF capacitors, while the MAX202E/MAX206E/MAX207E/MAX208E/MAX211E/MAX213E operate with four 0.1µF capacitors, further reducing cost and board space.

Applications

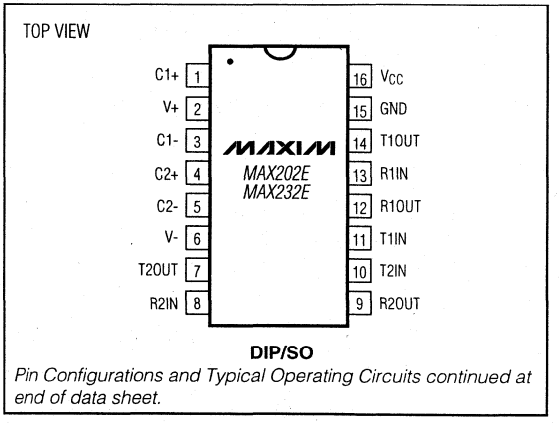
Notebook, Subnotebook, and Palmtop Computers
Battery-Powered Equipment
Hand-Held Equipment

Ordering Information appears at end of data sheet.

Features

- **ESD Protection for RS-232 I/O Pins:**
  ±15kV—Human Body Model
  ±8kV—IEC1000-4-2, Contact Discharge
  ±15kV—IEC1000-4-2, Air-Gap Discharge
- **Latchup Free (unlike bipolar equivalents)**
- **Guaranteed 120kbps Data Rate—LapLink™ Compatible**
- **Guaranteed 3V/µs Min Slew Rate**
- **Operate from a Single +5V Power Supply**

Pin Configurations



DIP/SO

Pin Configurations and Typical Operating Circuits continued at end of data sheet.

Selection Guide

PART	No. of RS-232 DRIVERS	No. of RS-232 RECEIVERS	RECEIVERS ACTIVE IN SHUTDOWN	No. of EXTERNAL CAPACITORS	LOW-POWER SHUTDOWN	TTL THREE-STATE
MAX202E	2	2	0	4 (0.1µF)	No	No
MAX203E	2	2	0	None	No	No
MAX205E	5	5	0	None	Yes	Yes
MAX206E	4	3	0	4 (0.1µF)	Yes	Yes
MAX207E	5	3	0	4 (0.1µF)	No	No
MAX208E	4	4	0	4 (0.1µF)	No	No
MAX211E	4	5	0	4 (0.1µF)	Yes	Yes
MAX213E	4	5	2	4 (0.1µF)	Yes	Yes
MAX232E	2	2	0	4 (1µF)	No	No
MAX241E	4	5	0	4 (1µF)	Yes	Yes

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ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... -0.3V to +6V
V+ ..... (V_{CC} - 0.3V) to +14V
V- ..... -14V to +0.3V
Input Voltages
T_IN ..... -0.3V to (V+ + 0.3V)
R_IN ..... ±30V
Output Voltages
T_OUT ..... (V- - 0.3V) to (V+ + 0.3V)
R_OUT ..... -0.3V to (V_{CC} + 0.3V)
Short-Circuit Duration, T_OUT ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
16-Pin Narrow SO (derate 8.70mW/°C above +70°C) 696mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) 762mW
20-Pin Plastic DIP (derate 11.11mW/°C above +70°C)...889mW
20-Pin SO (derate 10.00mW/°C above +70°C).....800mW
24-Pin Narrow Plastic DIP
(derate 13.33mW/°C above +70°C) 1.07W
24-Pin Wide Plastic DIP
(derate 14.29mW/°C above +70°C).....1.14W
24-Pin SO (derate 11.76mW/°C above +70°C).....941mW
24-Pin SSOP (derate 8.00mW/°C above +70°C) 640mW
28-Pin SO (derate 12.50mW/°C above +70°C).....1W
28-Pin SSOP (derate 9.52mW/°C above +70°C) 762mW
Operating Temperature Ranges
MAX2_ _EC_ _ .....0°C to +70°C
MAX2_ _EE_ _ .....-40°C to +85°C
Storage Temperature Range .....-65°C to +165°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V ±10% for MAX202E/206E/208E/211E/213E/232E/241E; V_{CC} = +5V ±5% for MAX203E/205E/207E; C1–C4 = 0.1µF for MAX202E/206E/207E/208E/211E/213E; C1–C4 = 1µF for MAX232E/241E; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS							
V_{CC} Supply Current	I_{CC}	No load, T_A = +25°C	MAX202E/203E		8	15	mA
			MAX205E–208E		11	20	
			MAX211E/213E		14	20	
			MAX232E		5	10	
			MAX241E		7	15	
Shutdown Supply Current		T_A = +25°C, Figure 1	MAX205E/206E		1	10	µA
			MAX211E/241E		1	10	
			MAX213E		15	50	
LOGIC							
Input Pull-Up Current		T_IN = 0V (MAX205E–208E/211E/213E/241E)			15	200	µA
Input Leakage Current		T_IN = 0V to V_{CC} (MAX202E/203E/232E)				±10	µA
Input Threshold Low	V_{IL}	T_IN; EN, $\overline{SHDN}$ (MAX213E) or $\overline{EN}$, SHDN (MAX205E–208E/211E/241E)				0.8	V
Input Threshold High	V_{IH}	T_IN		2.0			V
		EN, $\overline{SHDN}$ (MAX213E) or $\overline{EN}$, SHDN (MAX205E–208E/211E/241E)		2.4			
Output Voltage Low	V_{OL}	R_OUT; I_{OUT} = 3.2mA (MAX202E/203E/232E) or I_{OUT} = 1.6mA (MAX205E/208E/211E/213E/241E)				0.4	V
Output Voltage High	V_{OH}	R_OUT; I_{OUT} = -1.0mA		3.5	V_{CC} - 0.4		V
Output Leakage Current		$\overline{EN}$ = V_{CC}, EN = 0V, 0V ≤ R_{OUT} ≤ V_{CC}, MAX205E–208E/211E/213E/241E outputs disabled			±0.05	±10	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V ±10% for MAX202E/206E/208E/211E/213E/232E/241E; V_{CC} = +5V ±5% for MAX203E/205E/207E; C1–C4 = 0.1µF for MAX202E/206E/207E/208E/211E/213E; C1–C4 = 1µF for MAX232E/241E; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

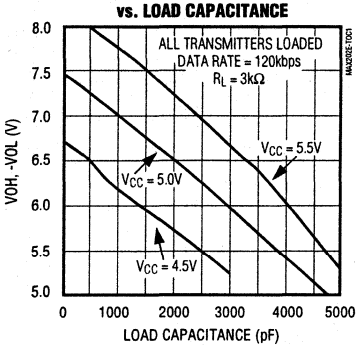
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
EIA/TIA-232E RECEIVER INPUTS							
Input Voltage Range				-30		30	V
Input Threshold Low		T_A = +25°C, V_{CC} = 5V	All parts, normal operation	0.8	1.2		V
			MAX213E, $\overline{SHDN}$ = 0V, EN = V_{CC}	0.6	1.5		
Input Threshold High		T_A = +25°C, V_{CC} = 5V	All parts, normal operation		1.7	2.4	V
			MAX213E (R4, R5), $\overline{SHDN}$ = 0V, EN = V_{CC}		1.5	2.4	
Input Hysteresis		V_{CC} = 5V, no hysteresis in shutdown		0.2	0.5	1.0	V
Input Resistance		T_A = +25°C, V_{CC} = 5V		3	5	7	kΩ
EIA/TIA-232E TRANSMITTER OUTPUTS							
Output Voltage Swing		All drivers loaded with 3kΩ to ground (Note 1)		±5	±9		V
Output Resistance		V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V		300			Ω
Output Short-Circuit Current					±10	±60	mA
TIMING CHARACTERISTICS							
Maximum Data Rate		R_L = 3kΩ to 7kΩ, C_L = 50pF to 1000pF, one transmitter switching		120			kbps
Receiver Propagation Delay	t_{PLHR}, t_{PHLR}	C_L = 150pF	All parts, normal operation		0.5	10	µs
			MAX213E (R4, R5), $\overline{SHDN}$ = 0V, EN = V_{CC}		4	40	
Receiver Output Enable Time		MAX205E/206E/211E/213E/241E normal operation, Figure 2			600		ns
Receiver Output Disable Time		MAX205E/206E/211E/213E/241E normal operation, Figure 2			200		ns
Transmitter Propagation Delay	t_{PLHT}, t_{PHLT}	R_L = 3kΩ, C_L = 2500pF, all transmitters loaded			2		µs
Transition-Region Slew Rate		T_A = +25°C, V_{CC} = 5V, R_L = 3kΩ to 7kΩ, C_L = 50pF to 1000pF, measured from -3V to +3V or +3V to -3V, Figure 3		3	6	30	V/µs
ESD PERFORMANCE: TRANSMITTER OUTPUTS, RECEIVER INPUTS							
ESD-Protection Voltage		Human Body Model			±15		kV
		IEC1000-4-2, Contact Discharge			±8		
		IEC1000-4-2, Air-Gap Discharge			±15		

Note 1: MAX211EE_ _ tested with V_{CC} = +5V ±5%.

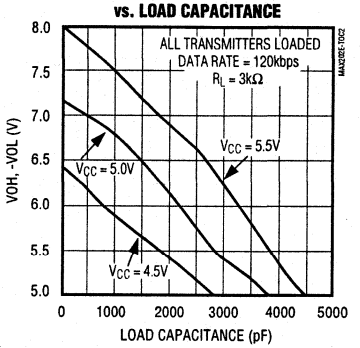
Typical Operating Characteristics

(Typical Operating Circuits, V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

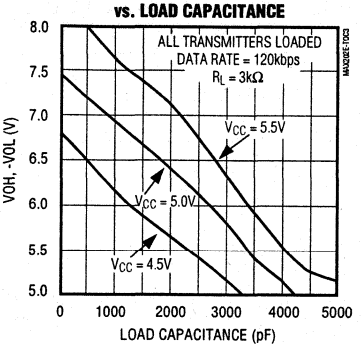
MAX232E
TRANSMITTER OUTPUT VOLTAGE
vs. LOAD CAPACITANCE



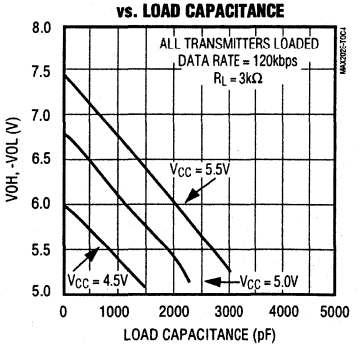
MAX202E/MAX203E
TRANSMITTER OUTPUT VOLTAGE
vs. LOAD CAPACITANCE



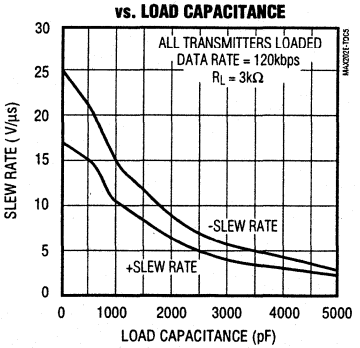
MAX241E
TRANSMITTER OUTPUT VOLTAGE
vs. LOAD CAPACITANCE



MAX211E/MAX213E
TRANSMITTER OUTPUT VOLTAGE
vs. LOAD CAPACITANCE



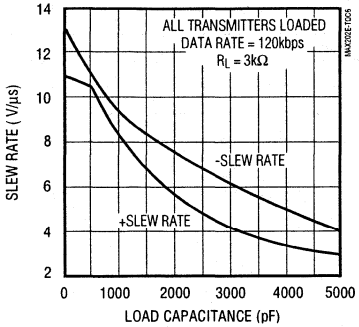
MAX211E/MAX213E/MAX241E
TRANSMITTER SLEW RATE
vs. LOAD CAPACITANCE



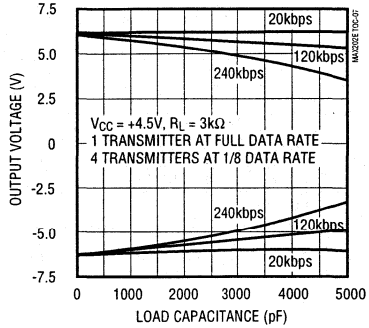
Typical Operating Characteristics (continued)

(Typical Operating Circuits, V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

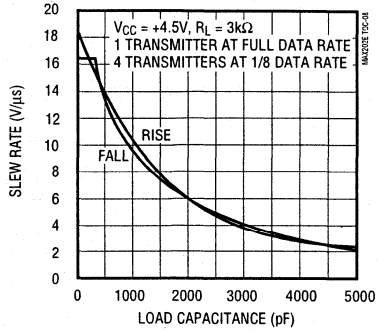
MAX202E/MAX203E/MAX232E TRANSMITTER SLEW RATE vs. LOAD CAPACITANCE



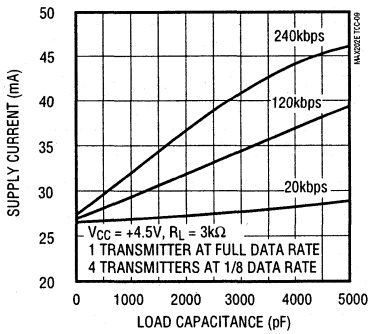
MAX205E–MAX208E TRANSMITTER OUTPUT VOLTAGE vs. LOAD CAPACITANCE



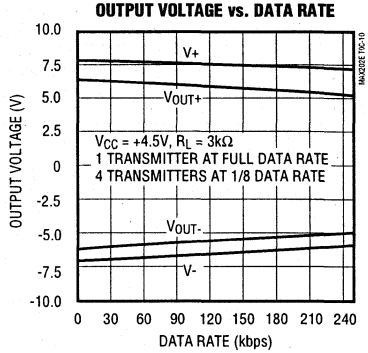
MAX205E–MAX208E TRANSMITTER SLEW RATE vs. LOAD CAPACITANCE



MAX205E–MAX208E SUPPLY CURRENT vs. LOAD CAPACITANCE



MAX205E–MAX208E OUTPUT VOLTAGE vs. DATA RATE



Pin Descriptions

MAX202E/MAX232E

PIN		NAME	FUNCTION
DIP/SO	LCC		
1, 3	2, 4	C1+, C1-	Terminals for positive charge-pump capacitor
2	3	V+	+2V_{CC} voltage generated by the charge pump
4, 5	5, 7	C2+, C2-	Terminals for negative charge-pump capacitor
6	8	V-	-2V_{CC} voltage generated by the charge pump
7, 14	9, 18	T_OUT	RS-232 Driver Outputs
8, 13	10, 17	R_IN	RS-232 Receiver Outputs
9, 12	12, 15	R_OUT	RS-232 Receiver Outputs
10, 11	13, 14	T_IN	RS-232 Driver Inputs
15	19	GND	Ground
16	20	V_{CC}	+4.5V to +5.5V Supply-Voltage Input
—	1, 6, 11, 16	N.C.	No Connect—not internally connected.

MAX203E

PIN		NAME	FUNCTION
DIP	SO		
1, 2	1, 2	T_IN	RS-232 Driver Inputs
3, 20	3, 20	R_OUT	RS-232 Receiver Outputs
4,19	4, 19	R_IN	RS-232 Receiver Inputs
5,18	5, 18	T_OUT	RS-232 Transmitter Outputs
6, 9	6, 9	GND	Ground
7	7	V_{CC}	+4.5V to +5.5V Supply-Voltage Input
8	13	C1+	Make no connection to this pin.
10, 16	11, 16	C2-	Connect pins together.
12, 17	10, 17	V-	-2V_{CC} voltage generated by the charge pump. Connect pins together.
13	14	C1-	Make no connection to this pin.
14	8	V+	+2V_{CC} voltage generated by the charge pump
11, 15	12, 15	C2+	Connect pins together.

MAX205E

PIN	NAME	FUNCTION
1–4, 19	T_OUT	RS-232 Driver Outputs
5, 10, 13, 18, 24	R_IN	RS-232 Receiver Inputs
6, 9, 14, 17, 23	R_OUT	TTL/CMOS Receiver Outputs. All receivers are inactive in shutdown.
7, 8, 15, 16, 22	T_IN	TTL/CMOS Driver Inputs. Internal pull-ups to V_{CC}.
11	GND	Ground
12	V_{CC}	+4.75V to +5.25V Supply Voltage
20	$\overline{EN}$	Receiver Enable—active low
21	SHDN	Shutdown Control—active high

Pin Descriptions (continued)

MAX206E

PIN	NAME	FUNCTION
1, 2, 3, 24	T_OUT	RS-232 Driver Outputs
4, 16, 23	R_IN	RS-232 Receiver Inputs
5, 17, 22	R_OUT	TTL/CMOS Receiver Outputs. All receivers are inactive in shutdown.
6, 7, 18, 19	T_IN	TTL/CMOS Driver Inputs. Internal pull-ups to V_{CC}.
8	GND	Ground
9	V_{CC}	+4.5V to +5.5V Supply Voltage
10, 12	C1+, C1-	Terminals for positive charge-pump capacitor
11	V+	+2V_{CC} generated by the charge pump
13, 14	C2+, C2-	Terminals for negative charge-pump capacitor
15	V-	-2V_{CC} generated by the charge pump
20	$\overline{EN}$	Receiver Enable—active low
21	SHDN	Shutdown Control—active high

MAX207E

PIN	NAME	FUNCTION
1, 2, 3, 20, 24	T_OUT	RS-232 Driver Outputs
4, 16, 23	R_IN	RS-232 Receiver Inputs
5, 17, 22	R_OUT	TTL/CMOS Receiver Outputs. All receivers are inactive in shutdown.
6, 7, 18, 19, 21	T_IN	TTL/CMOS Driver Inputs. Internal pull-ups to V_{CC}.
8	GND	Ground
9	V_{CC}	+4.75V to +5.25V Supply Voltage
10, 12	C1+, C1-	Terminals for positive charge-pump capacitor
11	V+	+2V_{CC} generated by the charge pump
13, 14	C2+, C2-	Terminals for negative charge-pump capacitor
15	V-	-2V_{CC} generated by the charge pump

MAX208E

PIN	NAME	FUNCTION
1, 2, 20, 24	T_OUT	RS-232 Driver Outputs
3, 7, 16, 23	R_IN	RS-232 Receiver Inputs
4, 6, 17, 22	R_OUT	TTL/CMOS Receiver Outputs. All receivers are inactive in shutdown.
5, 18, 19, 21	T_IN	TTL/CMOS Driver Inputs. Internal pull-ups to V_{CC}.
8	GND	Ground
9	V_{CC}	+4.5V to +5.5V Supply Voltage
10, 12	C1+, C1-	Terminals for positive charge-pump capacitor
11	V+	+2V_{CC} generated by the charge pump
13, 14	C2+, C2-	Terminals for negative charge-pump capacitor
15	V-	-2V_{CC} generated by the charge pump

Pin Descriptions (continued)

MAX211E/MAX213E/MAX241E

PIN	NAME	FUNCTION
1, 2, 3, 28	T_OUT	RS-232 Driver Outputs
4, 9, 18, 23, 27	R_IN	RS-232 Receiver Inputs
5, 8, 19, 22, 26	R_OUT	TTL/CMOS Receiver Outputs. For the MAX213E, receivers R4 and R5 are active in shutdown mode when EN = 1. For the MAX211E and MAX241E, all receivers are inactive in shutdown.
6, 7, 20, 21	T_IN	TTL/CMOS Driver Inputs. Only the MAX211E, MAX213E, and MAX241E have internal pull-ups to V_{CC}.
10	GND	Ground
11	V_{CC}	+4.5V to +5.5V Supply Voltage
12, 14	C1+, C1-	Terminals for positive charge-pump capacitor
13	V+	$+2V_{CC}$ voltage generated by the charge pump
15, 16	C2+, C2-	Terminals for negative charge-pump capacitor
17	V-	$-2V_{CC}$ voltage generated by the charge pump
24	$\overline{EN}$	Receiver Enable—active low (MAX211E, MAX241E)
	EN	Receiver Enable—active high (MAX213E)
25	SHDN	Shutdown Control—active high (MAX211E, MAX241E)
	$\overline{SHDN}$	Shutdown Control—active low (MAX213E)

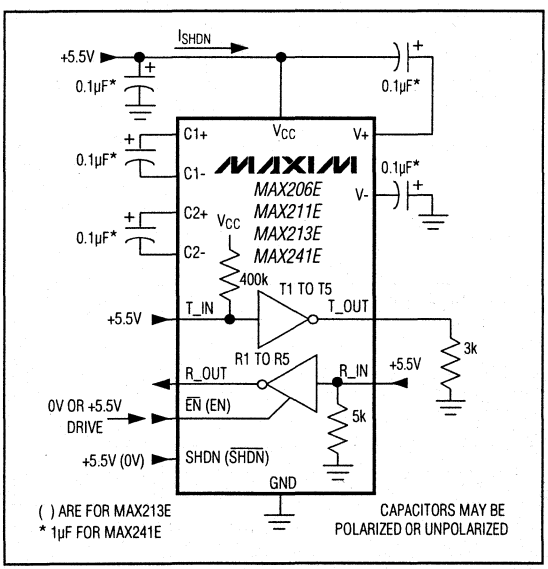


Figure 1. Shutdown-Current Test Circuit (MAX206E, MAX211E/MAX213E/MAX241E)

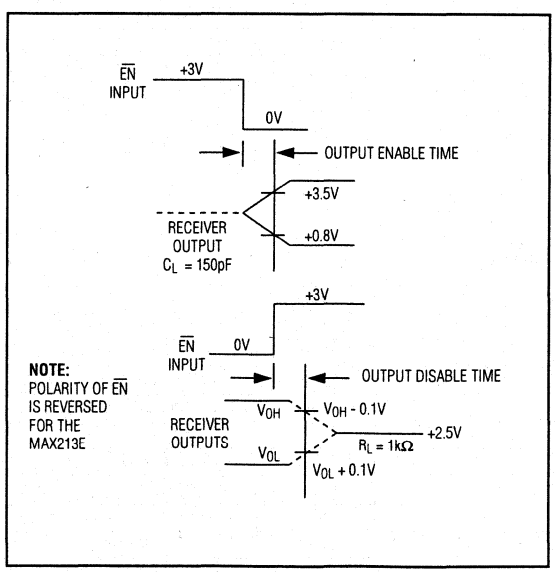


Figure 2. Receiver Output Enable and Disable Timing (MAX205E/MAX206E/MAX211E/MAX213E/MAX241E)

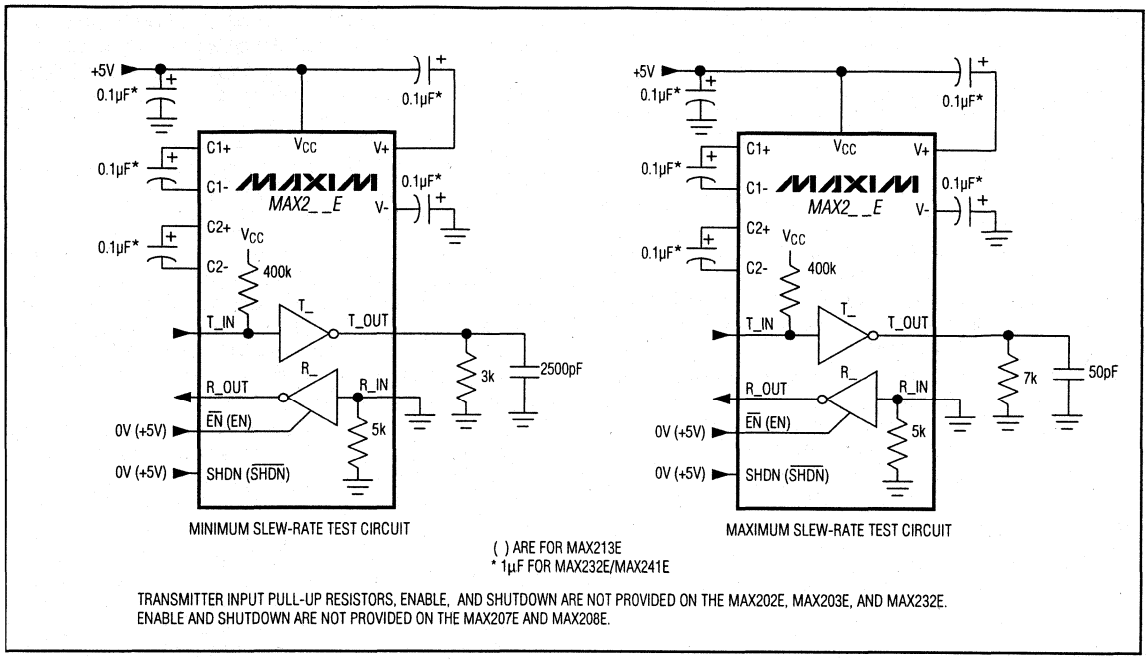


Figure 3. Transition Slew-Rate Circuit

Detailed Description

The MAX202E–MAX213E, MAX232E/MAX241E consist of three sections: charge-pump voltage converters, drivers (transmitters), and receivers. These E versions provide extra protection against ESD. They survive ±15kV discharges to the RS-232 inputs and outputs, tested using the Human Body Model. When tested according to IEC1000-4-2, they survive ±8kV contact-discharges and ±15kV air-gap discharges. The rugged E versions are intended for use in harsh environments or applications where the RS-232 connection is frequently changed (such as notebook computers). The standard (non-"E") MAX202, MAX203, MAX205–MAX208, MAX211, MAX213, MAX232, and MAX241 are recommended for applications where cost is critical.

+5V to ±10V Dual Charge-Pump Voltage Converter

The +5V to ±10V conversion is performed by dual charge-pump voltage converters (Figure 4). The first charge-pump converter uses capacitor C1 to double the +5V into +10V, storing the +10V on the output filter capacitor, C3. The second uses C2 to invert the +10V into -10V, storing the -10V on the V- output filter capacitor, C4.

In shutdown mode, V+ is internally connected to V_{CC} by a 1kΩ pull-down resistor, and V- is internally connected to ground by a 1kΩ pull-up resistor.

RS-232 Drivers

With V_{CC} = 5V, the typical driver output voltage swing is ±8V when loaded with a nominal 5kΩ RS-232 receiver. The output swing is guaranteed to meet EIA/TIA-232E and V.28 specifications that call for ±5V minimum output levels under worst-case conditions. These include a 3kΩ load, minimum V_{CC}, and maximum operating temperature. The open-circuit output voltage swings from (V+ - 0.6V) to V-.

Input thresholds are CMOS/TTL compatible. The unused drivers' inputs on the MAX205E–MAX208E, MAX211E, MAX213E, and MAX241E can be left unconnected because 400kΩ pull-up resistors to V_{CC} are included on-chip. Since all drivers invert, the pull-up resistors force the unused drivers' outputs low. The MAX202E, MAX203E, and MAX232E do not have pull-up resistors on the transmitter inputs.

When in low-power shutdown mode, the MAX205E/MAX206E/MAX211E/MAX213E/MAX241E driver outputs are turned off and draw only leakage currents—even if they are back-driven with voltages between 0V and 12V. Below -0.5V in shutdown, the transmitter output is diode-clamped to ground with a 1kΩ series impedance.

RS-232 Receivers

The receivers convert the RS-232 signals to CMOS-logic output levels. The guaranteed 0.8V and 2.4V receiver input thresholds are significantly tighter than the ±3V thresholds required by the EIA/TIA-232E specification. This allows the receiver inputs to respond to TTL/CMOS-logic levels, as well as RS-232 levels.

The guaranteed 0.8V input low threshold ensures that receivers shorted to ground have a logic 1 output. The 5kΩ input resistance to ground ensures that a receiver with its input left open will also have a logic 1 output.

Receiver inputs have approximately 0.5V hysteresis. This provides clean output transitions, even with slow rise/fall-time signals with moderate amounts of noise and ringing.

In shutdown, the MAX213E's R4 and R5 receivers have no hysteresis.

Shutdown and Enable Control (MAX205E/MAX206E/MAX211E/MAX213E/MAX241E)

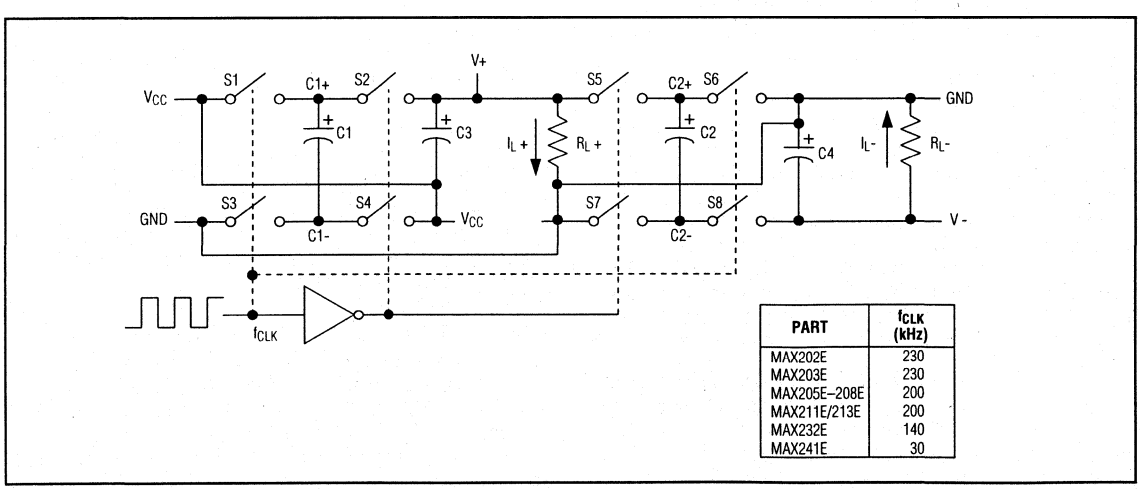
In shutdown mode, the charge pumps are turned off, V+ is pulled down to V_{CC}, V- is pulled to ground, and the transmitter outputs are disabled. This reduces supply current typically to 1µA (15µA for the MAX213E). The time required to exit shutdown is under 1ms, as shown in Figure 5.

Receivers

All MAX213E receivers, except R4 and R5, are put into a high-impedance state in shutdown mode (see Tables 1a and 1b). The MAX213E's R4 and R5 receivers still function in shutdown mode. These two awake-in-shutdown receivers can monitor external activity while maintaining minimal power consumption.

The enable control is used to put the receiver outputs into a high-impedance state, to allow wire-OR connection of two EIA/TIA-232E ports (or ports of different types) at the UART. It has no effect on the RS-232 drivers or the charge pumps.

Note: The enable control pin is active low for the MAX211E/MAX241E ($\overline{EN}$), but is active high for the MAX213E (EN). The shutdown control pin is active high for the MAX205E/MAX206E/MAX211E/MAX241E (SHDN), but is active low for the MAX213E ($\overline{SHDN}$).



PART	f_{CLK} (kHz)
MAX202E	230
MAX203E	230
MAX205E–208E	200
MAX211E/213E	200
MAX232E	140
MAX241E	30

Figure 4. Charge-Pump Diagram

The MAX213E's receiver propagation delay is typically 0.5µs in normal operation. In shutdown mode, propagation delay increases to 4µs for both rising and falling transitions. The MAX213E's receiver inputs have approximately 0.5V hysteresis, except in shutdown, when receivers R4 and R5 have no hysteresis.

When entering shutdown with receivers active, R4 and R5 are not valid until 80µs after $\overline{SHDN}$ is driven low. When coming out of shutdown, all receiver outputs are invalid until the charge pumps reach nominal voltage levels (less than 2ms when using 0.1µF capacitors).

±15kV ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver outputs and receiver inputs have extra protection against static electricity. Maxim's engineers developed state-of-the-art structures to protect these pins against ESD of ±15kV without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, Maxim's E versions keep working without latchup, whereas competing RS-232 products can latch and must be powered down to remove latchup.

ESD protection can be tested in various ways; the transmitter outputs and receiver inputs of this product family are characterized for protection to the following limits:

1) ±15kV using the Human Body Model
2) ±8kV using the contact-discharge method specified in IEC1000-4-2
3) ±15kV using IEC1000-4-2's air-gap method.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test set-up, test methodology, and test results.

Human Body Model

Figure 6a shows the Human Body Model, and Figure 6b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

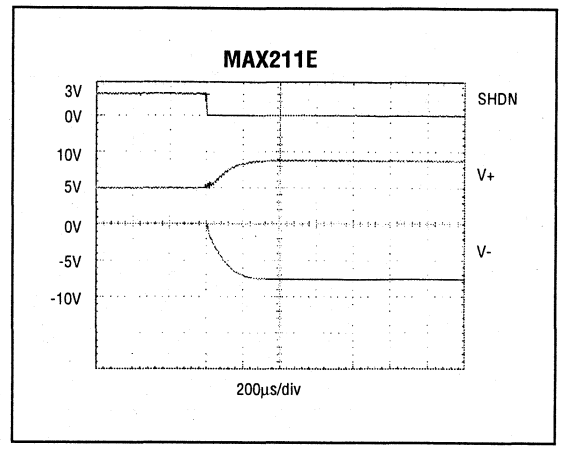


Figure 5. MAX211E V+ and V- when Exiting Shutdown (0.1µF capacitors)

Table 1a. MAX205E/MAX206E/MAX211E/MAX241E Control Pin Configurations

SHDN	$\overline{EN}$	OPERATION STATUS	Tx	Rx
0	0	Normal Operation	All Active	All Active
0	1	Normal Operation	All Active	All High-Z
1	X	Shutdown	All High-Z	All High-Z

X = Don't Care

Table 1b. MAX213E Control Pin Configurations

$\overline{SHDN}$	EN	OPERATION STATUS	Tx 1–4	Rx	
				1–3	4, 5
0	0	Shutdown	All High-Z	High-Z	High-Z
0	1	Shutdown	All High-Z	High-Z	Active*
1	0	Normal Operation	All Active	High-Z	High-Z
1	1	Normal Operation	All Active	Active	Active

**Active = active with reduced performance*

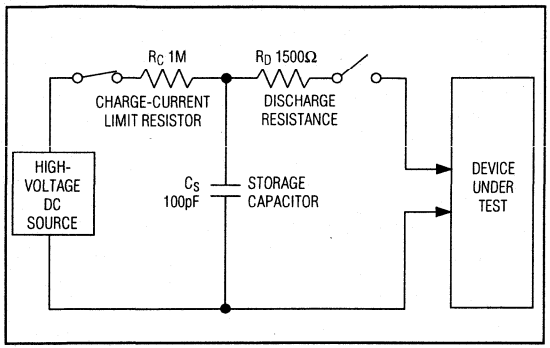


Figure 6a. Human Body ESD Test Model

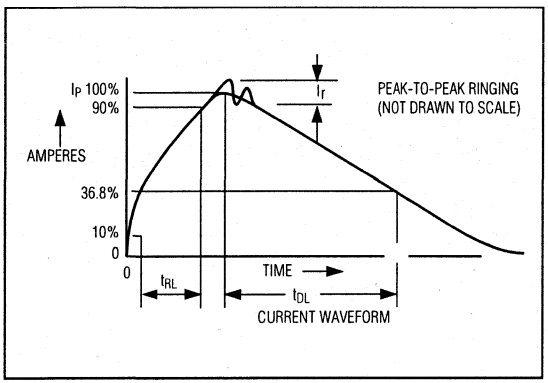


Figure 6b. Human Body Model Current Waveform

IEC1000-4-2

The IEC1000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits. The MAX202E/MAX203E–MAX213E, MAX232E/MAX241E help you design equipment that meets level 4 (the highest level) of IEC1000-4-2, without the need for additional ESD-protection components.

The major difference between tests done using the Human Body Model and IEC1000-4-2 is higher peak current in IEC1000-4-2, because series resistance is lower in the IEC1000-4-2 model. Hence, the ESD withstand voltage measured to IEC1000-4-2 is generally lower than that measured using the Human Body Model. Figure 7b shows the current waveform for the 8kV IEC1000-4-2 level-four ESD contact-discharge test.

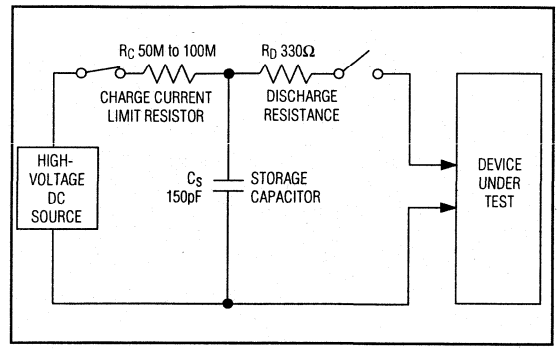


Figure 7a. IEC1000-4-2 ESD Test Model

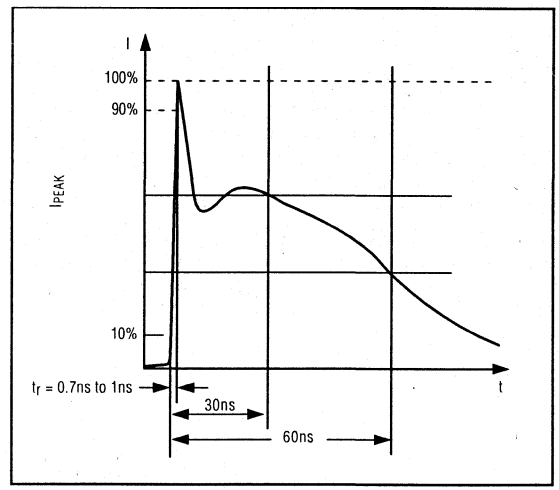


Figure 7b. IEC1000-4-2 ESD Generator Current Waveform

The air-gap test involves approaching the device with a charged probe. The contact-discharge method connects the probe to the device before the probe is energized.

Machine Model

The Machine Model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. Its objective is to emulate the stress caused by contact that occurs with handling and assembly during manufacturing. Of course, all pins require this protection during manufacturing, not just RS-232 inputs and outputs. Therefore, after PC board assembly, the Machine Model is less relevant to I/O ports.

Applications Information

Capacitor Selection

The capacitor type used for C1–C4 is not critical for proper operation. The MAX202E, MAX206–MAX208E, MAX211E, and MAX213E require 0.1µF capacitors, and the MAX232E and MAX241E require 1µF capacitors, although in all cases capacitors up to 10µF can be used without harm. Ceramic, aluminum-electrolytic, or tantalum capacitors are suggested for the 1µF capacitors, and ceramic dielectrics are suggested for the 0.1µF capacitors. When using the minimum recommended capacitor values, make sure the capacitance value does not degrade excessively as the operating temperature varies. If in doubt, use capacitors with a larger (e.g., 2x) nominal value. The capacitors' effective series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V-.

Use larger capacitors (up to 10µF) to reduce the output impedance at V+ and V-. This can be useful when "stealing" power from V+ or from V-. The MAX203E and MAX205E have internal charge-pump capacitors.

Bypass V_{CC} to ground with at least 0.1µF. In applications sensitive to power-supply noise generated by the charge pumps, decouple V_{CC} to ground with a capacitor the same size as (or larger than) the charge-pump capacitors (C1–C4).

V+ and V- as Power Supplies

A small amount of power can be drawn from V+ and V-, although this will reduce both driver output swing and noise margins. Increasing the value of the charge-pump capacitors (up to 10µF) helps maintain performance when power is drawn from V+ or V-.

Driving Multiple Receivers

Each transmitter is designed to drive a single receiver. Transmitters can be paralleled to drive multiple receivers.

Driver Outputs when Exiting Shutdown

The driver outputs display no ringing or undesirable transients as they come out of shutdown.

High Data Rates

These transceivers maintain the RS-232 ±5.0V minimum driver output voltages at data rates of over 120kbps. For data rates above 120kbps, refer to the Transmitter Output Voltage vs. Load Capacitance graphs in the *Typical Operating Characteristics*. Communication at these high rates is easier if the capacitive loads on the transmitters are small; i.e., short cables are best.

Table 2. Summary of EIA/TIA-232E, V.28 Specifications

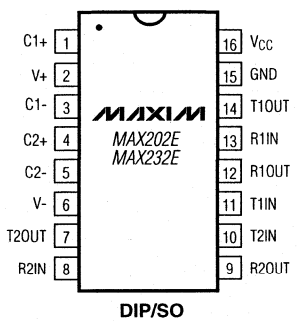
PARAMETER		CONDITIONS	EIA/TIA-232E, V.28 SPECIFICATIONS
Driver Output Voltage	0 Level	3kΩ to 7kΩ load	+5V to +15V
	1 Level	3kΩ to 7kΩ load	-5V to -15V
Driver Output Level, Max		No load	±25V
Data Rate		3kΩ ≤ R_L ≤ 7kΩ, C_L ≤ 2500pF	Up to 20kbps
Receiver Input Voltage	0 Level		+3V to +15V
	1 Level		-3V to -15V
Receiver Input Level			±25V
Instantaneous Slew Rate, Max		3kΩ ≤ R_L ≤ 7kΩ, C_L ≤ 2500pF	30V/µs
Driver Output Short-Circuit Current, Max			100mA
Transition Rate on Driver Output		V.28	1ms or 3% of the period
		EIA/TIA-232E	4% of the period
Driver Output Resistance		-2V < V_{OUT} < +2V	300Ω

Table 3. DB9 Cable Connections Commonly Used for EIA/TIAE-232E and V.24 Asynchronous Interfaces

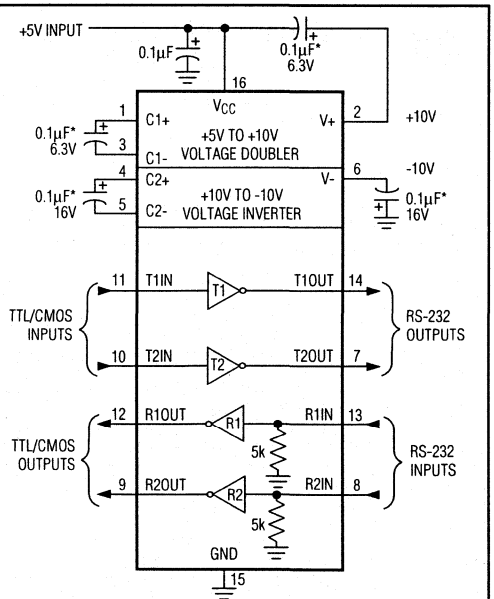
PIN	CONNECTION	
1	Received Line Signal Detector (sometimes called Carrier Detect, DCD)	Handshake from DCE
2	Receive Data (RD)	Data from DCE
3	Transmit Data (TD)	Data from DTE
4	Data Terminal Ready	Handshake from DTE
5	Signal Ground	Reference point for signals
6	Data Set Ready (DSR)	Handshake from DCE
7	Request to Send (RTS)	Handshake from DTE
8	Clear to Send (CTS)	Handshake from DCE
9	Ring Indicator	Handshake from DCE

Pin Configurations and Typical Operating Circuits (continued)

TOP VIEW



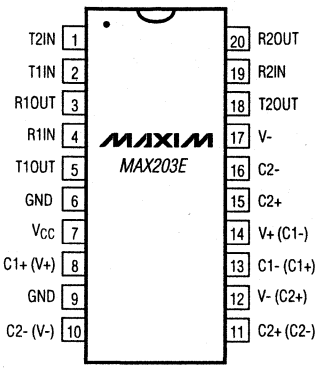
DIP/SO



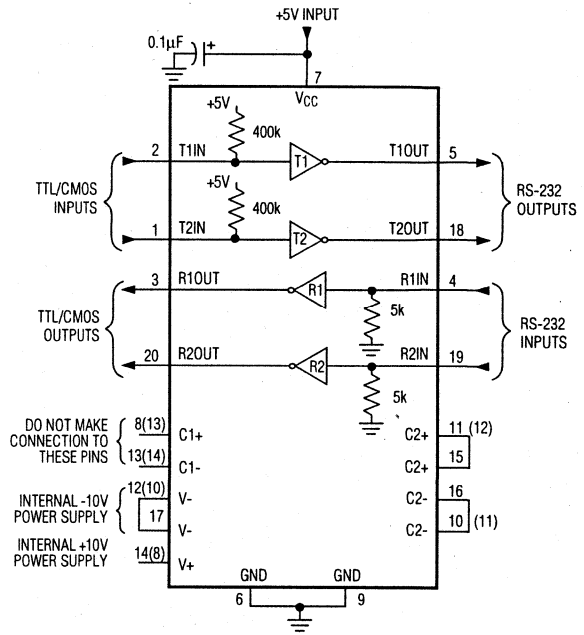
PIN NUMBERS ON TYPICAL OPERATING CIRCUIT REFER TO DIP/SO PACKAGE, NOT LCC.
* 1.0µF CAPACITORS, MAX232E ONLY.

Pin Configurations and Typical Operating Circuits (continued)

TOP VIEW



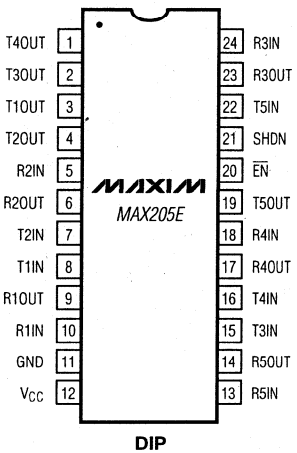
DIP/SO



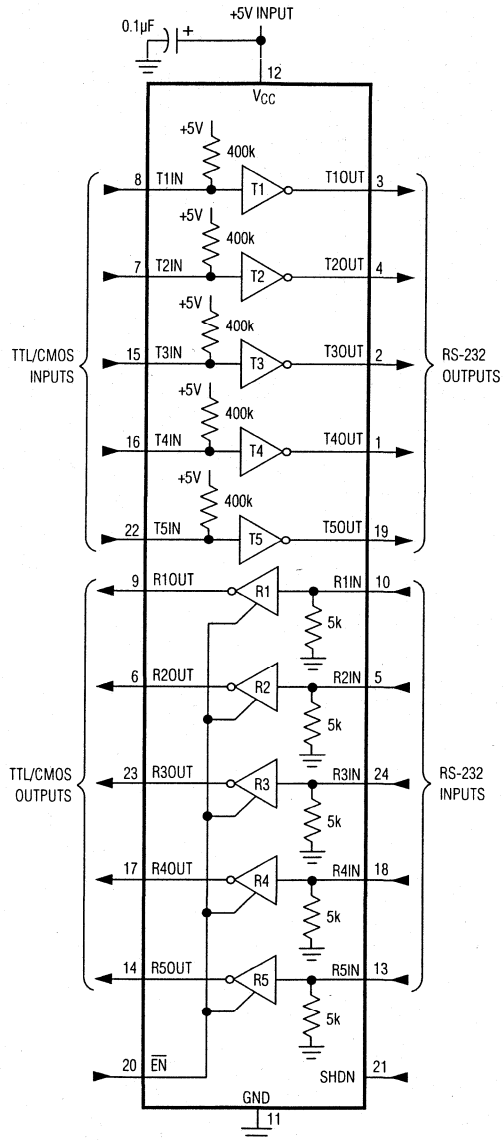
PIN NUMBERS IN ( ) ARE FOR SO PACKAGE.

Pin Configurations and Typical Operating Circuits (continued)

TOP VIEW

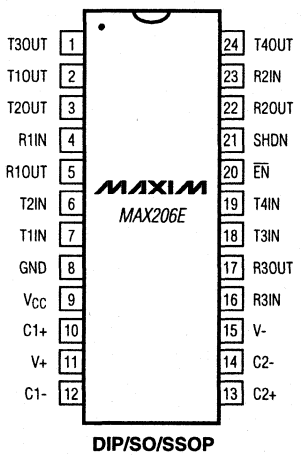


DIP

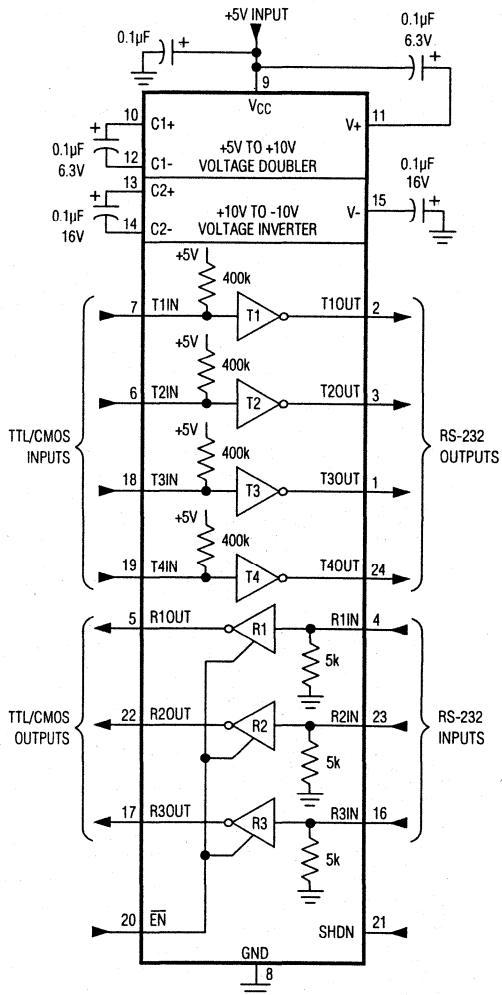


Pin Configurations and Typical Operating Circuits (continued)

TOP VIEW

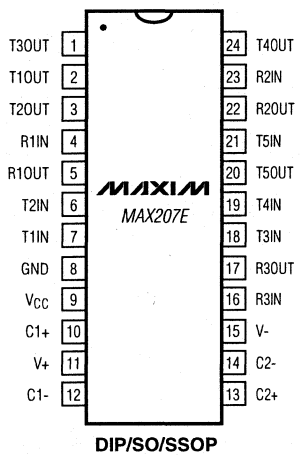


DIP/SO/SSOP

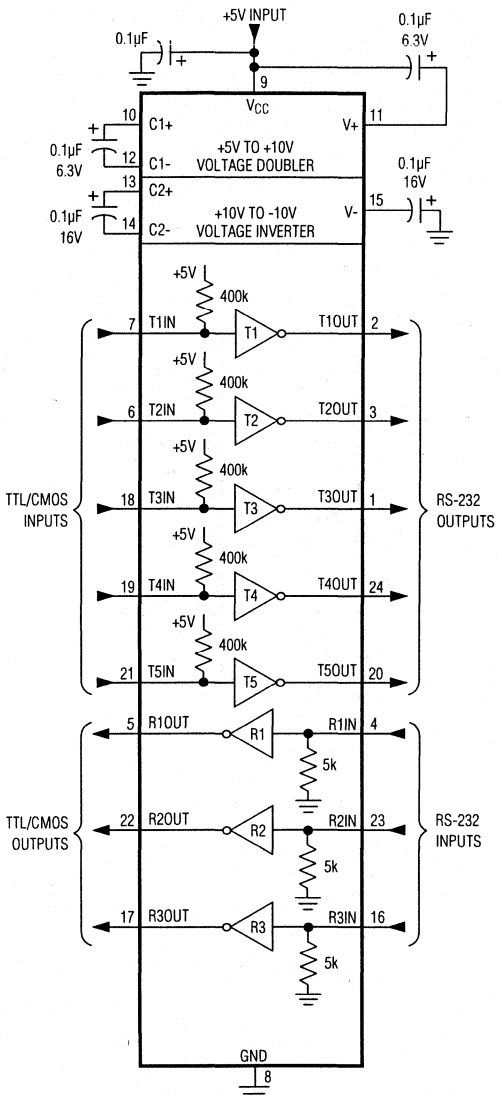


Pin Configurations and Typical Operating Circuits (continued)

TOP VIEW

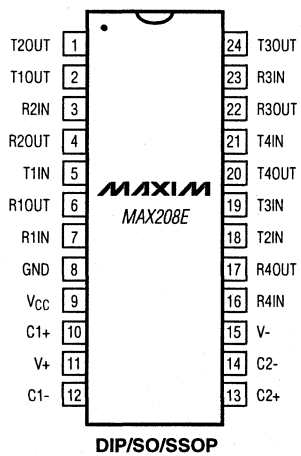


DIP/SO/SSOP

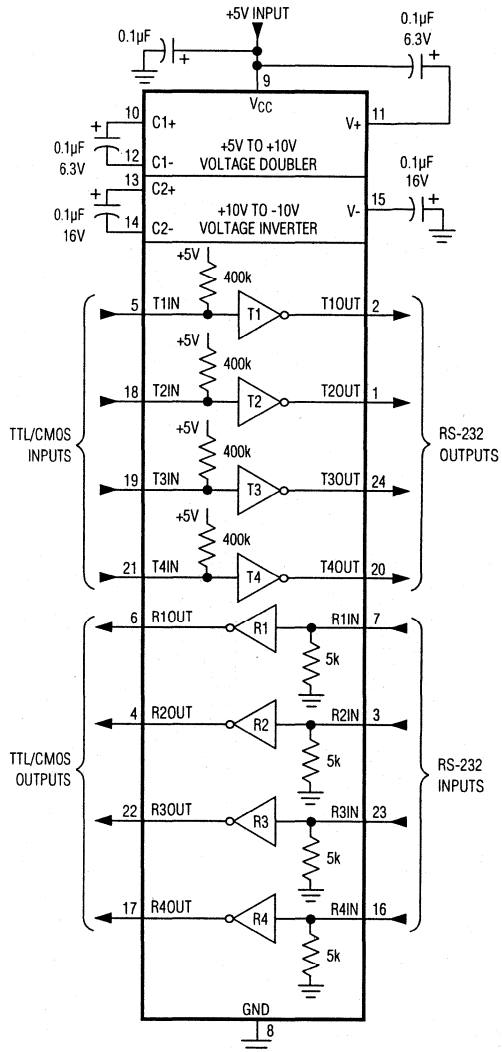


Pin Configurations and Typical Operating Circuits (continued)

TOP VIEW

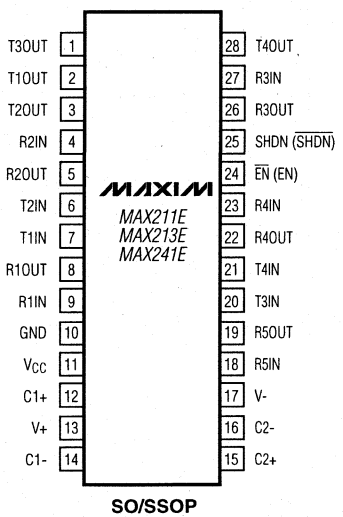


DIP/SO/SSOP

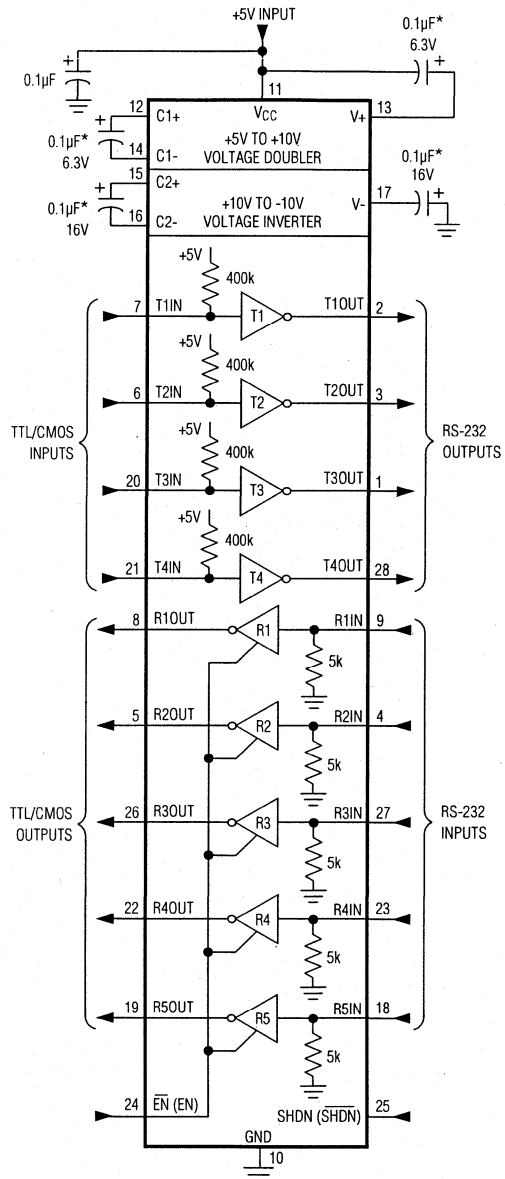


Pin Configurations and Typical Operating Circuits (continued)

TOP VIEW



SO/SSOP



( ) ARE FOR MAX213E ONLY
* 1.0µF CAPACITORS, MAX241E ONLY

Ordering Information

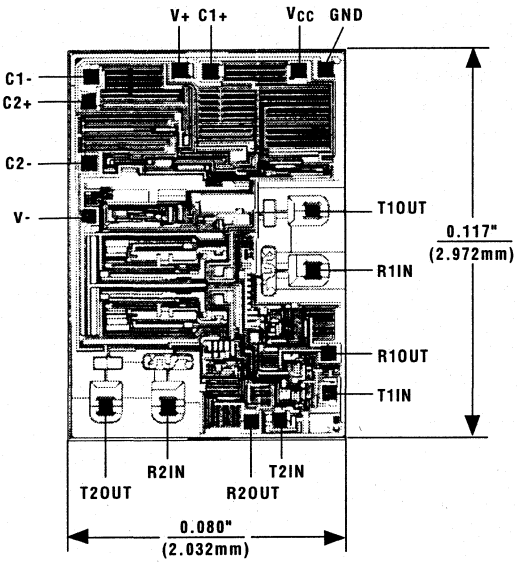
PART	TEMP. RANGE	PIN-PACKAGE
MAX202ECPE	0°C to +70°C	16 Plastic DIP
MAX202ECSE	0°C to +70°C	16 Narrow SO
MAX202ECWE	0°C to +70°C	16 Wide SO
MAX202EC/D	0°C to +70°C	Dice*
MAX202EEPE	-40°C to +85°C	16 Plastic DIP
MAX202EESE	-40°C to +85°C	16 Narrow SO
MAX202EEWE	-40°C to +85°C	16 Wide SO
MAX203ECPP	0°C to +70°C	20 Plastic DIP
MAX203ECWP	0°C to +70°C	20 SO
MAX203EEPP	-40°C to +85°C	20 Plastic DIP
MAX203EEWP	-40°C to +85°C	20 SO
MAX205ECPG	0°C to +70°C	24 Wide Plastic DIP
MAX205EEPG	-40°C to +85°C	24 Wide Plastic DIP
MAX206ECNG	0°C to +70°C	24 Narrow Plastic DIP
MAX206ECWG	0°C to +70°C	24 SO
MAX206ECAG	0°C to +70°C	24 SSOP
MAX206EENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX206EEWG	-40°C to +85°C	24 SO
MAX206EEAG	-40°C to +85°C	24 SSOP
MAX207ECNG	0°C to +70°C	24 Narrow Plastic DIP
MAX207ECWG	0°C to +70°C	24 SO
MAX207ECAG	0°C to +70°C	24 SSOP
MAX207EENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX207EEWG	-40°C to +85°C	24 SO
MAX207EEAG	-40°C to +85°C	24 SSOP

PART	TEMP. RANGE	PIN-PACKAGE
MAX208ECNG	0°C to +70°C	24 Narrow Plastic DIP
MAX208ECWG	0°C to +70°C	24 SO
MAX208ECAG	0°C to +70°C	24 SSOP
MAX208EENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX208EEWG	-40°C to +85°C	24 SO
MAX208EEAG	-40°C to +85°C	24 SSOP
MAX211ECWI	0°C to +70°C	28 SO
MAX211ECAI	0°C to +70°C	28 SSOP
MAX211EEWI	-40°C to +85°C	28 SO
MAX211EEAI	-40°C to +85°C	28 SSOP
MAX213ECWI	0°C to +70°C	28 SO
MAX213ECAI	0°C to +70°C	28 SSOP
MAX213EEWI	-40°C to +85°C	28 SO
MAX213EEAI	-40°C to +85°C	28 SSOP
MAX232ECPE	0°C to +70°C	16 Plastic DIP
MAX232ECSE	0°C to +70°C	16 Narrow SO
MAX232ECWE	0°C to +70°C	16 Wide SO
MAX232EC/D	0°C to +70°C	Dice*
MAX232EEPE	-40°C to +85°C	16 Plastic DIP
MAX232EESE	-40°C to +85°C	16 Narrow SO
MAX232EEWE	-40°C to +85°C	16 Wide SO
MAX241ECWI	0°C to +70°C	28 SO
MAX241ECAI	0°C to +70°C	28 SSOP
MAX241EEWI	-40°C to +85°C	28 SO
MAX241EEAI	-40°C to +85°C	28 SSOP

*Dice are specified at T_A = +25°C.

Chip Topographies

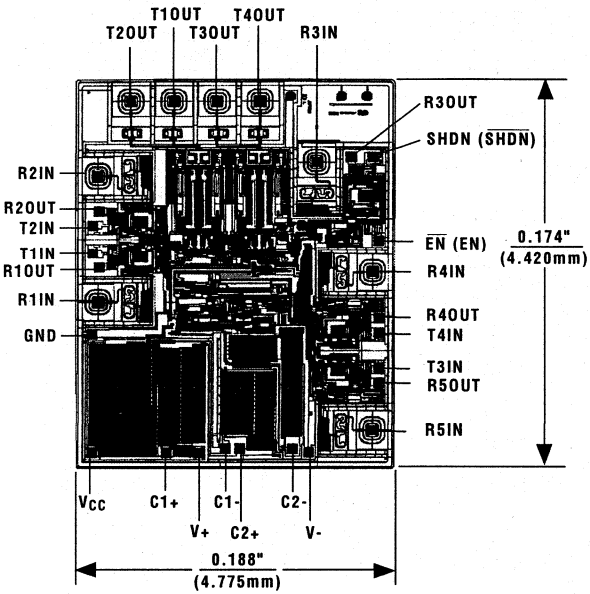
MAX202E/MAX232E



TRANSISTOR COUNT: 123

SUBSTRATE CONNECTED TO GND

MAX211E/MAX213E/MAX241E



( ) ARE FOR MAX213E ONLY

TRANSISTOR COUNT: 542

SUBSTRATE CONNECTED TO GND

Chip Information

MAX205E/MAX206E/MAX207E/MAX208E

TRANSISTOR COUNT: 328

SUBSTRATE CONNECTED TO GND

19-0410; Rev 3; 7/96

MAXIM

±15kV ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceivers

General Description

The MAX481E, MAX483E, MAX485E, MAX487E–MAX491E, and MAX1487E are low-power transceivers for RS-485 and RS-422 communications in harsh environments. Each driver output and receiver input is protected against ±15kV electrostatic discharge (ESD) shocks, without latchup. These parts contain one driver and one receiver. The MAX483E, MAX487E, MAX488E, and MAX489E feature reduced slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, thus allowing error-free data transmission up to 250kbps. The driver slew rates of the MAX481E, MAX485E, MAX490E, MAX491E, and MAX1487E are not limited, allowing them to transmit up to 2.5Mbps.

These transceivers draw as little as 120µA supply current when unloaded or when fully loaded with disabled drivers (see *Selection Table*). Additionally, the MAX481E, MAX483E, and MAX487E have a low-current shutdown mode in which they consume only 0.5µA. All parts operate from a single +5V supply.

Drivers are short-circuit current limited, and are protected against excessive power dissipation by thermal shutdown circuitry that places their outputs into a high-impedance state. The receiver input has a fail-safe feature that guarantees a logic-high output if the input is open circuit.

The MAX487E and MAX1487E feature quarter-unit-load receiver input impedance, allowing up to 128 transceivers on the bus. The MAX488E–MAX491E are designed for full-duplex communications, while the MAX481E, MAX483E, MAX485E, MAX487E, and MAX1487E are designed for half-duplex applications. For applications that are not ESD sensitive see the pin- and function-compatible MAX481, MAX483, MAX485, MAX487–MAX491, and MAX1487.

Applications

Low-Power RS-485 Transceivers
Low-Power RS-422 Transceivers
Level Translators
Transceivers for EMI-Sensitive Applications
Industrial-Control Local Area Networks

Features

- **ESD Protection: ±15kV—Human Body Model**
- **Slew-Rate Limited for Error-Free Data Transmission (MAX483E/487E/488E/489E)**
- **Low Quiescent Current:**
  120µA (MAX483E/487E/488E/489E)
  230µA (MAX1487E)
  300µA (MAX481E/485E/490E/491E)
- **-7V to +12V Common-Mode Input Voltage Range**
- **Three-State Outputs**
- **30ns Propagation Delays, 5ns Skew (MAX481E/485E/490E/491E/1487E)**
- **Full-Duplex and Half-Duplex Versions Available**
- **Allows up to 128 Transceivers on the Bus (MAX487E/MAX1487E)**
- **Current Limiting and Thermal Shutdown for Driver Overload Protection**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX481ECPA	0°C to +70°C	8 Plastic DIP
MAX481ECSA	0°C to +70°C	8 SO
MAX481EEPA	-40°C to +85°C	8 Plastic DIP
MAX481EESA	-40°C to +85°C	8 SO

Ordering Information continued on last page.

Selection Table

PART NUMBER	HALF/FULL DUPLEX	DATA RATE (Mbps)	SLEW-RATE LIMITED	LOW-POWER SHUTDOWN	RECEIVER/ DRIVER ENABLE	QUIESCENT CURRENT (µA)	NUMBER OF TRANSMITTERS ON BUS	PIN COUNT
MAX481E	Half	2.5	No	Yes	Yes	300	32	8
MAX483E	Half	0.25	Yes	Yes	Yes	120	32	8
MAX485E	Half	2.5	No	No	Yes	300	32	8
MAX487E	Half	0.25	Yes	Yes	Yes	120	128	8
MAX488E	Full	0.25	Yes	No	No	120	32	8
MAX489E	Full	0.25	Yes	No	Yes	120	32	14
MAX490E	Full	2.5	No	No	No	300	32	8
MAX491E	Full	2.5	No	No	Yes	300	32	14
MAX1487E	Half	2.5	No	No	Yes	230	128	8

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

±15kV ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceivers

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) 12V
Control Input Voltage ($\overline{RE}$, DE) ..... -0.5V to (V_{CC} + 0.5V)
Driver Input Voltage (DI) ..... -0.5V to (V_{CC} + 0.5V)
Driver Output Voltage (Y, Z; A, B) ..... -8V to +12.5V
Receiver Input Voltage (A, B) ..... -8V to +12.5V
Receiver Output Voltage (RO) ..... -0.5V to (V_{CC} + 0.5V)
Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C) ..800mW
8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
14-Pin SO (derate 8.33mW/°C above +70°C) 667mW
Operating Temperature Ranges
MAX4_ _C_ _/MAX1487EC_ A ..... 0°C to +70°C
MAX4_ _E_ _/MAX1487EE_ A ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Differential Driver Output (no load)	V_{OD1}					5	V
Differential Driver Output (with load)	V_{OD2}	R = 50Ω (RS-422)		2			V
		R = 27Ω (RS-485), Figure 8		1.5		5	
Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	ΔV_{OD}	R = 27Ω or 50Ω, Figure 8				0.2	V
Driver Common-Mode Output Voltage	V_{OC}	R = 27Ω or 50Ω, Figure 8				3	V
Change in Magnitude of Driver Common-Mode Output Voltage for Complementary Output States	ΔV_{OD}	R = 27Ω or 50Ω, Figure 8				0.2	V
Input High Voltage	V_{IH}	DE, DI, $\overline{RE}$		2.0			V
Input Low Voltage	V_{IL}	DE, DI, $\overline{RE}$				0.8	V
Input Current	I_{IN1}	DE, DI, $\overline{RE}$				±2	µA
Input Current (A, B)	I_{IN2}	DE = 0V; V_{CC} = 0V or 5.25V, all devices except MAX487E/MAX1487E	V_{IN} = 12V			1.0	mA
			V_{IN} = -7V			-0.8	
		MAX487E/MAX1487E, DE = 0V, V_{CC} = 0V or 5.25V	V_{IN} = 12V			0.25	mA
			V_{IN} = -7V			-0.2	
Receiver Differential Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ 12V		-0.2		0.2	V
Receiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0V			70		mV
Receiver Output High Voltage	V_{OH}	I_O = -4mA, V_{ID} = 200mV		3.5			V
Receiver Output Low Voltage	V_{OL}	I_O = 4mA, V_{ID} = -200mV				0.4	V
Three-State (high impedance) Output Current at Receiver	I_{OZR}	0.4V ≤ V_O ≤ 2.4V				±1	µA
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ 12V, all devices except MAX487E/MAX1487E		12			kΩ
		-7V ≤ V_{CM} ≤ 12V, MAX487E/MAX1487E		48			kΩ

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
No-Load Supply Current (Note 3)	I_{CC}	MAX488E/MAX489E, DE, DI, $\overline{RE}$ = 0V or V_{CC}				120	250	µA
		MAX490E/MAX491E, DE, DI, $\overline{RE}$ = 0V or V_{CC}				300	500	
		MAX481E/MAX485E, $\overline{RE}$ = 0V or V_{CC}	DE = V_{CC}			500	900	
			DE = 0V			300	500	
		MAX1487E, $\overline{RE}$ = 0V or V_{CC}	DE = V_{CC}			300	500	
			DE = 0V			230	400	
		MAX483E/MAX487E, $\overline{RE}$ = 0V or V_{CC}	DE = V_{CC}	MAX483E		350	650	
				MAX487E		250	400	
			DE = 0V			120	250	
Supply Current in Shutdown	I_{SHDN}	MAX481E/483E/487E, DE = 0V, $\overline{RE}$ = V_{CC}				0.5	10	µA
Driver Short-Circuit Current, V_O = High	I_{OSD1}	-7V ≤ V_O ≤12V (Note 4)			35		250	mA
Driver Short-Circuit Current, V_O = Low	I_{OSD2}	-7V ≤ V_O ≤12V (Note 4)			35		250	mA
Receiver Short-Circuit Current	I_{OSR}	0V ≤ V_O ≤ V_{CC}			7		95	mA
ESD Protection		A, B, Y and Z pins, tested using Human Body Model				±15		kV

SWITCHING CHARACTERISTICS—MAX481E/MAX485E, MAX490E/MAX491E, MAX1487E

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Driver Input to Output	t_{PLH}	Figures 10 and 12, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		10	40	60	ns
	t_{PHL}			10	40	60	
Driver Output Skew to Output	t_{SKEW}	Figures 10 and 12, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF			5	10	ns
Driver Rise or Fall Time	t_R, t_F	Figures 10 and 12, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	MAX481E, MAX485E, MAX1487E	3	20	40	ns
			MAX490EC/E, MAX491EC/E	5	20	25	
Driver Enable to Output High	t_{ZH}	Figures 11 and 13, C_L = 100pF, S2 closed			45	70	ns
Driver Enable to Output Low	t_{ZL}	Figures 11 and 13, C_L = 100pF, S1 closed			45	70	ns
Driver Disable Time from Low	t_{LZ}	Figures 11 and 13, C_L = 15pF, S1 closed			45	70	ns
Driver Disable Time from High	t_{HZ}	Figures 11 and 13, C_L = 15pF, S2 closed			45	70	ns
Receiver Input to Output	t_{PLH}, t_{PHL}	Figures 10 and 14, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	MAX481E, MAX485E, MAX1487E	20	60	200	ns
			MAX490EC/E, MAX491EC/E	20	60	150	
| t_{PLH} - t_{PHL} | Differential Receiver Skew	t_{SKD}	Figures 10 and 14, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF			5		ns
Receiver Enable to Output Low	t_{ZL}	Figures 9 and 15, C_{RL} = 15pF, S1 closed			20	50	ns
Receiver Enable to Output High	t_{ZH}	Figures 9 and 15, C_{RL} = 15pF, S2 closed			20	50	ns
Receiver Disable Time from Low	t_{LZ}	Figures 9 and 15, C_{RL} = 15pF, S1 closed			20	50	ns
Receiver Disable Time from High	t_{HZ}	Figures 9 and 15, C_{RL} = 15pF, S2 closed			20	50	ns
Maximum Data Rate	f_{MAX}			2.5			Mbps
Time to Shutdown	t_{SHDN}	MAX481E (Note 5)		50	200	600	ns

SWITCHING CHARACTERISTICS—MAX481E/MAX485E, MAX490E/MAX491E, MAX1487E (continued)

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Enable from Shutdown to Output High (MAX481E)	$t_{ZH(SHDN)}$	Figures 11 and 13, C_L = 100pF, S2 closed		45	100	ns
Driver Enable from Shutdown to Output Low (MAX481E)	$t_{ZL(SHDN)}$	Figures 11 and 13, C_L = 100pF, S1 closed		45	100	ns
Receiver Enable from Shutdown to Output High (MAX481E)	$t_{ZH(SHDN)}$	Figures 9 and 15, C_L = 15pF, S2 closed, A - B = 2V		225	1000	ns
Receiver Enable from Shutdown to Output Low (MAX481E)	$t_{ZL(SHDN)}$	Figures 9 and 15, C_L = 15pF, S1 closed, B - A = 2V		225	1000	ns

SWITCHING CHARACTERISTICS—MAX483E, MAX487E/MAX488E/MAX489E

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Input to Output	t_{PLH}	Figures 10 and 12, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	250	800	2000	ns
	t_{PHL}		250	800	2000	
Driver Output Skew to Output	t_{SKEW}	Figures 10 and 12, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		20	800	ns
Driver Rise or Fall Time	t_R, t_F	Figures 10 and 12, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	250		2000	ns
Driver Enable to Output High	t_{ZH}	Figures 11 and 13, C_L = 100pF, S2 closed	250		2000	ns
Driver Enable to Output Low	t_{ZL}	Figures 11 and 13, C_L = 100pF, S1 closed	250		2000	ns
Driver Disable Time from Low	t_{LZ}	Figures 11 and 13, C_L = 15pF, S1 closed	300		3000	ns
Driver Disable Time from High	t_{HZ}	Figures 11 and 13, C_L = 15pF, S2 closed	300		3000	ns
Receiver Input to Output	t_{PLH}	Figures 10 and 14, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	250		2000	ns
	t_{PHL}		250		2000	
| t_{PLH} - t_{PHL} | Differential Receiver Skew	t_{SKD}	Figures 10 and 14, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		100		ns
Receiver Enable to Output Low	t_{ZL}	Figures 9 and 15, C_{RL} = 15pF, S1 closed		25	50	ns
Receiver Enable to Output High	t_{ZH}	Figures 9 and 15, C_{RL} = 15pF, S2 closed		25	50	ns
Receiver Disable Time from Low	t_{LZ}	Figures 9 and 15, C_{RL} = 15pF, S1 closed		25	50	ns
Receiver Disable Time from High	t_{HZ}	Figures 9 and 15, C_{RL} = 15pF, S2 closed		25	50	ns
Maximum Data Rate	f_{MAX}	t_{PLH}, t_{PHL} < 50% of data period	250			kbps
Time to Shutdown	t_{SHDN}	MAX483E/MAX487E (Note 5)	50	200	600	ns
Driver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	MAX483E/MAX487E, Figures 11 and 13, C_L = 100pF, S2 closed			2000	ns
Driver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	MAX483E/MAX487E, Figures 11 and 13, C_L = 100pF, S1 closed			2000	ns
Receiver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	MAX483E/MAX487E, Figures 9 and 15, C_L = 15pF, S2 closed			2500	ns
Receiver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	MAX483E/MAX487E, Figures 9 and 15, C_L = 15pF, S1 closed			2500	ns

NOTES FOR ELECTRICAL/SWITCHING CHARACTERISTICS

Note 1: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 2: All typical specifications are given for V_{CC} = 5V and T_A = +25°C.

Note 3: Supply current specification is valid for loaded transmitters when DE = 0V.

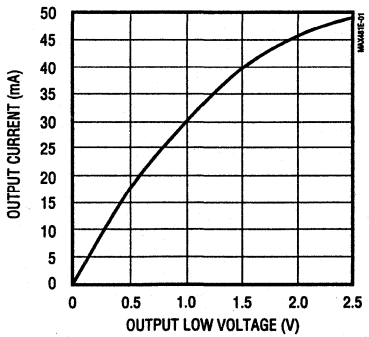
Note 4: Applies to peak current. See *Typical Operating Characteristics.*

Note 5: The MAX481E/MAX483E/MAX487E are put into shutdown by bringing $\overline{RE}$ high and DE low. If the inputs are in this state for less than 50ns, the parts are guaranteed not to enter shutdown. If the inputs are in this state for at least 600ns, the parts are guaranteed to have entered shutdown. See *Low-Power Shutdown Mode* section.

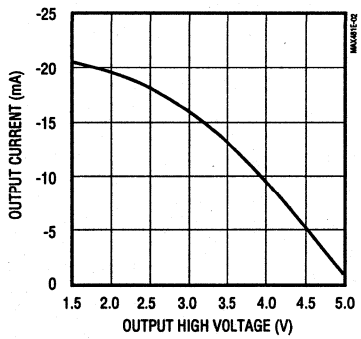
Typical Operating Characteristics

(V_{CC} = 5V, T_A = +25°C, unless otherwise noted.)

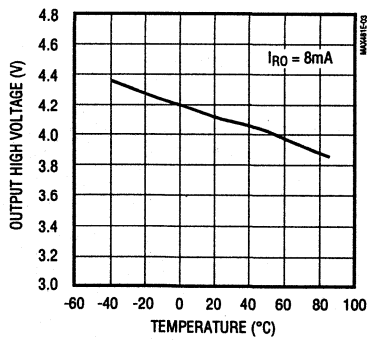
OUTPUT CURRENT vs. RECEIVER OUTPUT LOW VOLTAGE



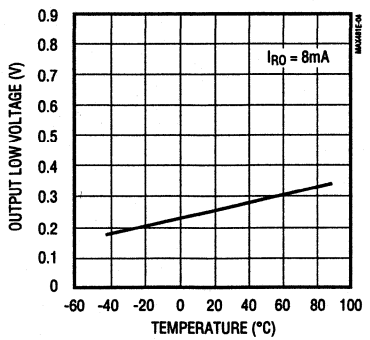
OUTPUT CURRENT vs. RECEIVER OUTPUT HIGH VOLTAGE



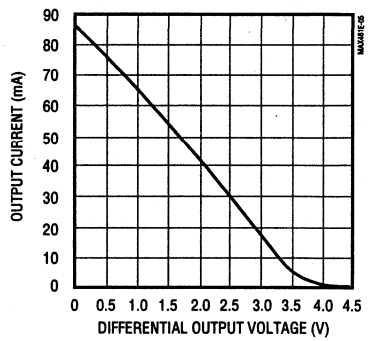
RECEIVER OUTPUT HIGH VOLTAGE vs. TEMPERATURE



RECEIVER OUTPUT LOW VOLTAGE vs. TEMPERATURE



DRIVER OUTPUT CURRENT vs. DIFFERENTIAL OUTPUT VOLTAGE

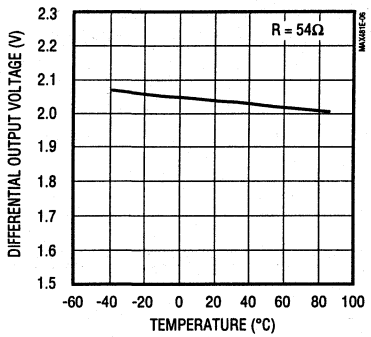


±15kV ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceivers

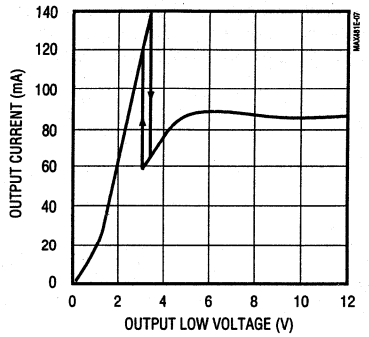
Typical Operating Characteristics (continued)

(V_{CC} = 5V, T_A = +25°C, unless otherwise noted.)

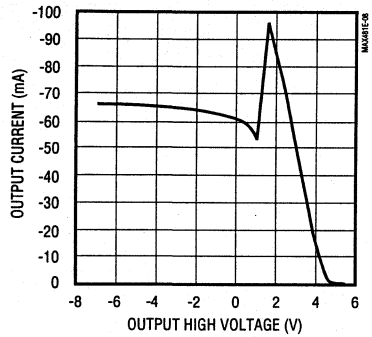
DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs. TEMPERATURE



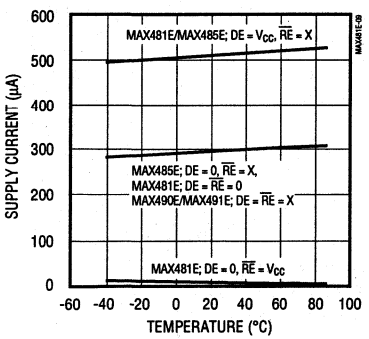
OUTPUT CURRENT vs. DRIVER OUTPUT LOW VOLTAGE



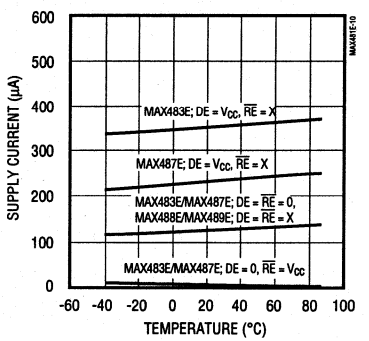
OUTPUT CURRENT vs. DRIVER OUTPUT HIGH VOLTAGE



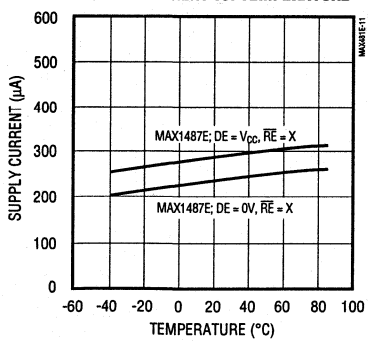
MAX481E/MAX485E/MAX490E/MAX491E SUPPLY CURRENT vs. TEMPERATURE



MAX483E/MAX487E–MAX489E SUPPLY CURRENT vs. TEMPERATURE



MAX1487E SUPPLY CURRENT vs. TEMPERATURE



Pin Description

PIN			NAME	FUNCTION
MAX481E/MAX483E MAX485E/MAX487E MAX1487E	MAX488E MAX490E	MAX489E MAX491E		
1	2	2	RO	Receiver Output: If A > B by 200mV, RO will be high; If A < B by 200mV, RO will be low.
2	—	3	$\overline{RE}$	Receiver Output Enable. RO is enabled when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high.
3	—	4	DE	Driver Output Enable. The driver outputs, Y and Z, are enabled by bringing DE high. They are high impedance when DE is low. If the driver outputs are enabled, the parts function as line drivers. While they are high impedance, they function as line receivers if $\overline{RE}$ is low.
4	3	5	DI	Driver Input. A low on DI forces output Y low and output Z high. Similarly, a high on DI forces output Y high and output Z low.
5	4	6, 7	GND	Ground
—	5	9	Y	Noninverting Driver Output
—	6	10	Z	Inverting Driver Output
6	—	—	A	Noninverting Receiver Input and Noninverting Driver Output
—	8	12	A	Noninverting Receiver Input
7	—	—	B	Inverting Receiver Input and Inverting Driver Output
—	7	11	B	Inverting Receiver Input
8	1	14	V_{CC}	Positive Supply: $4.75V \le V_{CC} \le 5.25V$
—	—	1, 8, 13	N.C.	No Connect—not internally connected

±15kV ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceivers

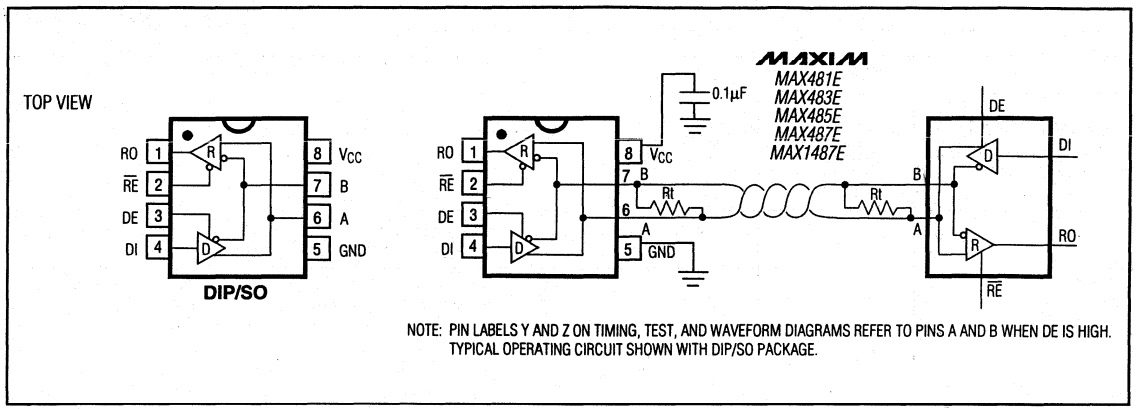


Figure 1. MAX481E/MAX483E/MAX485E/MAX487E/MAX1487E Pin Configuration and Typical Operating Circuit

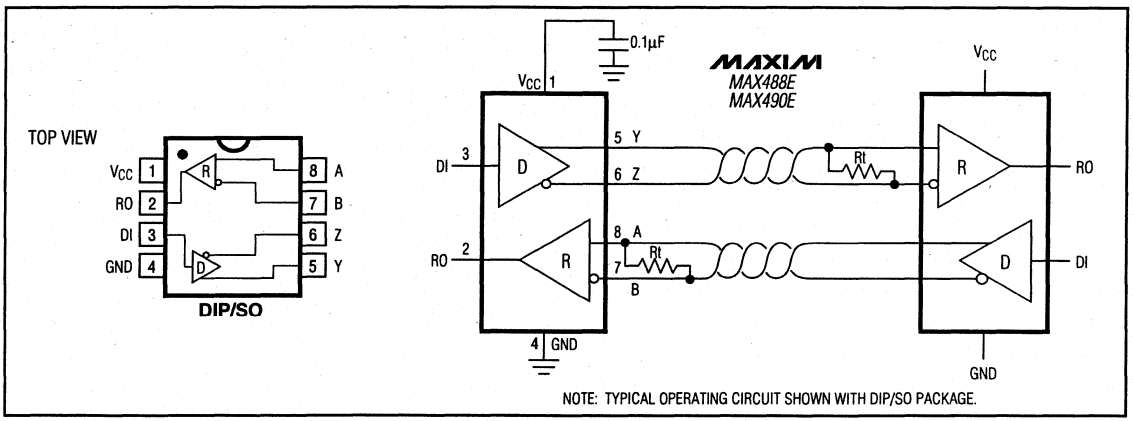


Figure 2. MAX488E/MAX490E Pin Configuration and Typical Operating Circuit

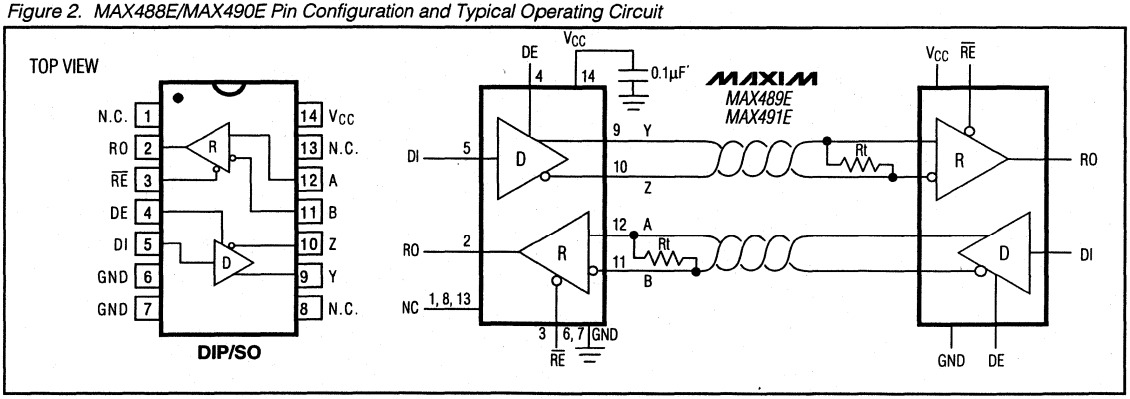


Figure 3. MAX489E/MAX491E Pin Configuration and Typical Operating Circuit

Function Tables (MAX481E/MAX483E/MAX485E/MAX487E/MAX1487E)

Table 1. Transmitting

INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	Z	Y
X	1	1	0	1
X	1	0	1	0
0	0	X	High-Z	High-Z
1	0	X	High-Z*	High-Z*

X = Don't care
High-Z = High impedance
* Shutdown mode for MAX481E/MAX483E/MAX487E

Table 2. Receiving

INPUTS			OUTPUT
$\overline{RE}$	DE	A-B	RO
0	0	≥ +0.2V	1
0	0	≤ -0.2V	0
0	0	Inputs open	1
1	0	X	High-Z*

X = Don't care
High-Z = High impedance
* Shutdown mode for MAX481E/MAX483E/MAX487E

Applications Information

The MAX481E/MAX483E/MAX485E/MAX487E–MAX491E and MAX1487E are low-power transceivers for RS-485 and RS-422 communications. These "E" versions of the MAX481, MAX483, MAX485, MAX487–MAX491, and MAX1487 provide extra protection against ESD. The rugged MAX481E, MAX483E, MAX485E, MAX497E–MAX491E, and MAX1487E are intended for harsh environments where high-speed communication is important. These devices eliminate the need for transient suppressor diodes and the associated high capacitance loading. The standard (non-"E") MAX481, MAX483, MAX485, MAX487–MAX491, and MAX1487 are recommended for applications where cost is critical.

The MAX481E, MAX485E, MAX490E, MAX491E, and MAX1487E can transmit and receive at data rates up to 2.5Mbps, while the MAX483E, MAX487E, MAX488E, and MAX489E are specified for data rates up to 250kbps. The MAX488E–MAX491E are full-duplex transceivers, while the MAX481E, MAX483E, MAX487E, and MAX1487E are half-duplex. In addition, driver-enable (DE) and receiver-enable (RE) pins are included on the MAX481E, MAX483E, MAX485E, MAX487E, MAX489E, MAX491E, and MAX1487E. When disabled, the driver and receiver outputs are high impedance.

±15kV ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver outputs and receiver inputs have extra protection against static electricity. Maxim's engineers developed state-of-the-art structures to protect these pins against ESD of ±15kV without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, Maxim's MAX481E, MAX483E, MAX485E, MAX487E–MAX491E, and MAX1487E keep working without latchup.

ESD protection can be tested in various ways; the transmitter outputs and receiver inputs of this product family are characterized for protection to ±15kV using the Human Body Model.

Other ESD test methodologies include IEC10004-2 contact discharge and IEC1000-4-2 air-gap discharge (formerly IEC801-2).

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test set-up, test methodology, and test results.

Human Body Model

Figure 4 shows the Human Body Model, and Figure 5 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

IEC1000-4-2

The IEC1000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits (Figure 6).

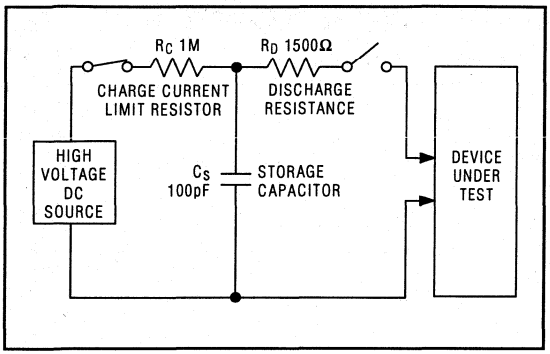


Figure 4. Human Body ESD Test Model

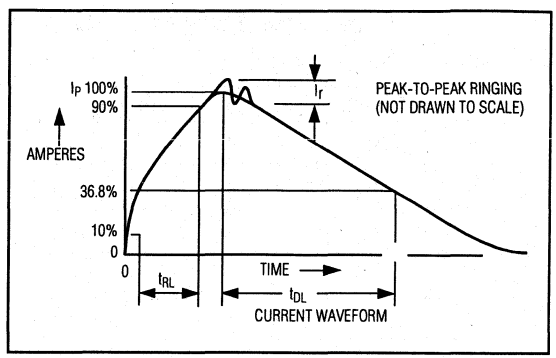


Figure 5. Human Body Model Current Waveform

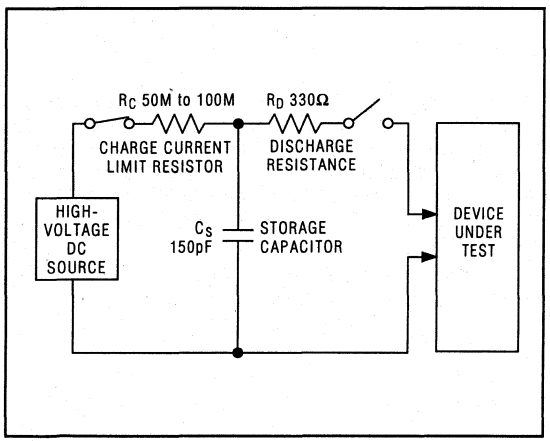


Figure 6. IEC1000-4-2 ESD Test Model

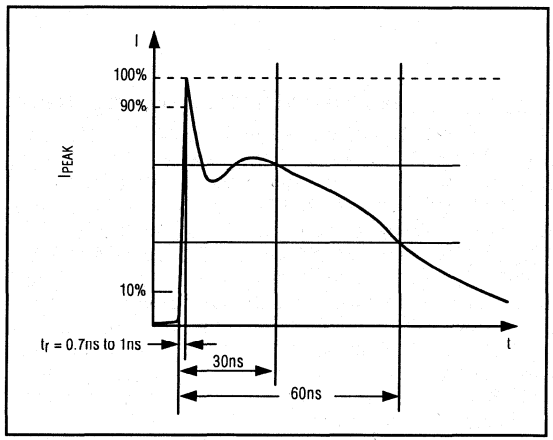


Figure 7. IEC1000-4-2 ESD Generator Current Waveform

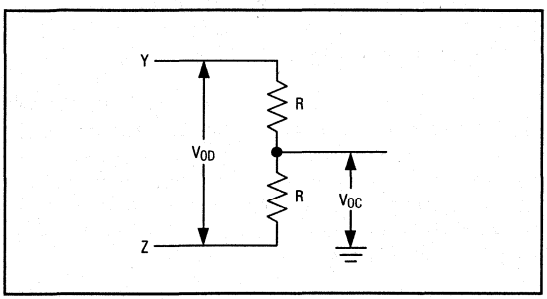


Figure 8. Driver DC Test Load

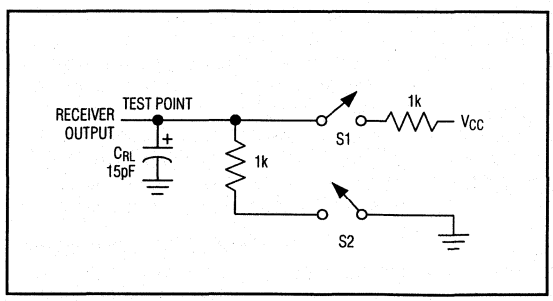


Figure 9. Receiver Timing Test Load

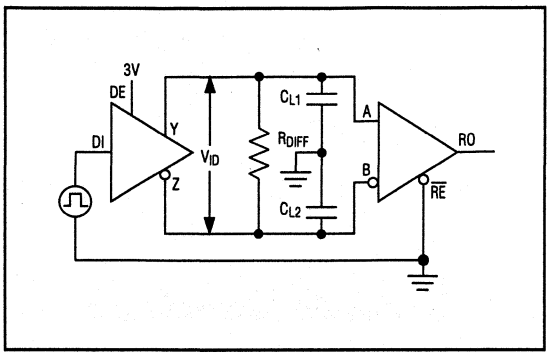


Figure 10. Driver/Receiver Timing Test Circuit

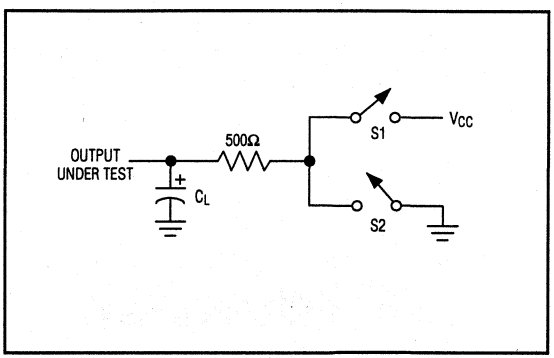


Figure 11. Driver Timing Test Load

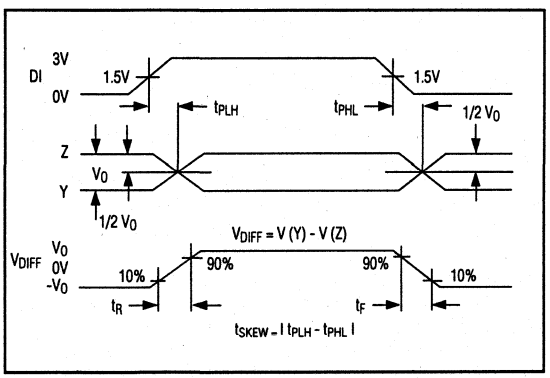


Figure 12. Driver Propagation Delays

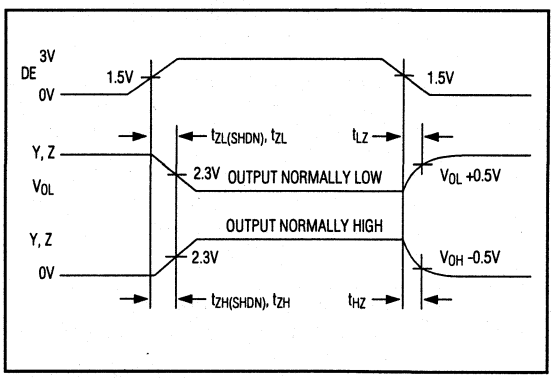


Figure 13. Driver Enable and Disable Times (except MAX488E and MAX490E)

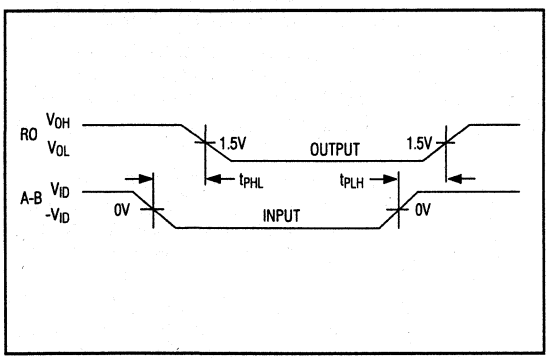


Figure 14. Receiver Propagation Delays

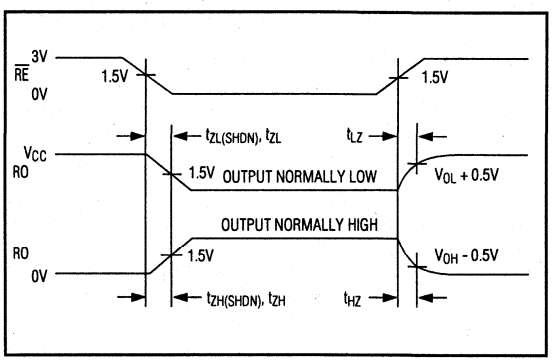


Figure 15. Receiver Enable and Disable Times (except MAX488E and MAX490E)

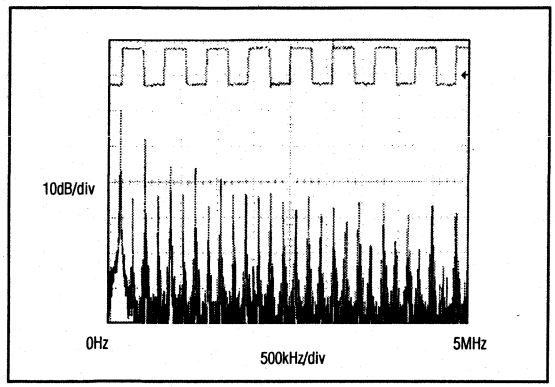


Figure 16. Driver Output Waveform and FFT Plot of MAX485E/MAX490E/MAX491E/MAX1487E Transmitting a 150kHz Signal

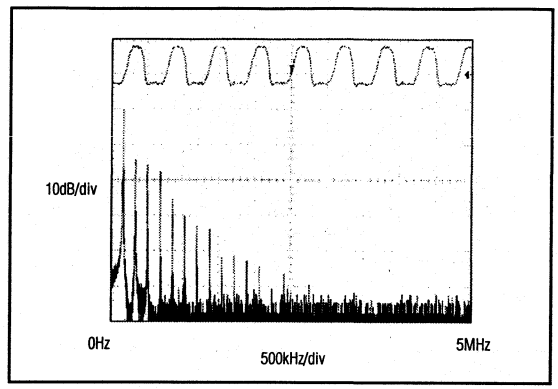


Figure 17. Driver Output Waveform and FFT Plot of MAX483E/MAX487E–MAX489E Transmitting a 150kHz Signal

The major difference between tests done using the Human Body Model and IEC1000-4-2 is higher peak current in IEC1000-4-2, because series resistance is lower in the IEC1000-4-2 model. Hence, the ESD withstand voltage measured to IEC1000-4-2 is generally lower than that measured using the Human Body Model. Figure 7 shows the current waveform for the 8kV IEC1000-4-2 ESD contact-discharge test.

The air-gap test involves approaching the device with a charged probe. The contact-discharge method connects the probe to the device before the probe is energized.

Machine Model

The Machine Model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. Its objective is to emulate the stress caused by contact that occurs with handling and assembly during manufacturing. Of course, all pins require this protection during manufacturing—not just inputs and outputs. Therefore, after PC board assembly, the Machine Model is less relevant to I/O ports.

MAX487E/MAX1487E: 128 Transceivers on the Bus

The 48kΩ, 1/4-unit-load receiver input impedance of the MAX487E and MAX1487E allows up to 128 transceivers on a bus, compared to the 1-unit load (12kΩ input impedance) of standard RS-485 drivers (32 transceivers maximum). Any combination of MAX487E/MAX1487E and other RS-485 transceivers with a total of 32 unit loads or less can be put on the bus. The MAX481E, MAX483E, MAX485E, and MAX488E–MAX491E have standard 12kΩ receiver input impedance.

MAX483E/MAX487E/MAX488E/MAX489E: Reduced EMI and Reflections

The MAX483E and MAX487E–MAX489E are slew-rate limited, minimizing EMI and reducing reflections caused by improperly terminated cables. Figure 16 shows the driver output waveform and its Fourier analysis of a 150kHz signal transmitted by a MAX481E, MAX485E, MAX490E, MAX491E, or MAX1487E. High-frequency harmonics with large amplitudes are evident. Figure 17 shows the same information displayed for a MAX483E, MAX487E, MAX488E, or MAX489E transmitting under the same conditions. Figure 17's high-frequency harmonics have much lower amplitudes, and the potential for EMI is significantly reduced.

Low-Power Shutdown Mode (MAX481E/MAX483E/MAX487E)

A low-power shutdown mode is initiated by bringing both $\overline{RE}$ high and DE low. The devices will not shut down unless both the driver and receiver are disabled. In shutdown, the devices typically draw only 0.5µA of supply current.

$\overline{RE}$ and DE may be driven simultaneously; the parts are guaranteed not to enter shutdown if $\overline{RE}$ is high and DE is low for less than 50ns. If the inputs are in this state for at least 600ns, the parts are guaranteed to enter shutdown.

For the MAX481E, MAX483E, and MAX487E, the t_{ZH} and t_{ZL} enable times assume the part was not in the low-power shutdown state (the MAX485E, MAX488E–MAX491E, and MAX1487E can not be shut down). The $t_{ZH(SHDN)}$ and $t_{ZL(SHDN)}$ enable times assume the parts were shut down (see *Electrical Characteristics*).

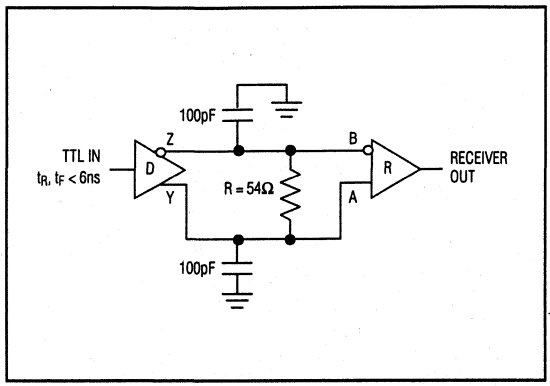


Figure 18. Receiver Propagation Delay Test Circuit

It takes the drivers and receivers longer to become enabled from the low-power shutdown state ($t_{ZH(SHDN)}$, $t_{ZL(SHDN)}$) than from the operating mode (t_{ZH}, t_{ZL}). (The parts are in operating mode if the $\overline{RE}$, DE inputs equal a logical 0,1 or 1,1 or 0, 0.)

Driver Output Protection

Excessive output current and power dissipation caused by faults or by bus contention are prevented by two mechanisms. A foldback current limit on the output stage provides immediate protection against short circuits over the whole common-mode voltage range (see *Typical Operating Characteristics*). In addition, a thermal shutdown circuit forces the driver outputs into a high-impedance state if the die temperature rises excessively.

Propagation Delay

Many digital encoding schemes depend on the difference between the driver and receiver propagation delay times. Typical propagation delays are shown in Figures 19–22 using Figure 18's test circuit.

The difference in receiver delay times, t_{PLH} - t_{PHL}, is typically under 13ns for the MAX481E, MAX485E, MAX490E, MAX491E, and MAX1487E, and is typically less than 100ns for the MAX483E and MAX487E–MAX489E.

The driver skew times are typically 5ns (10ns max) for the MAX481E, MAX485E, MAX490E, MAX491E, and MAX1487E, and are typically 100ns (800ns max) for the MAX483E and MAX487E–MAX489E.

Typical Applications

The MAX481E, MAX483E, MAX485E, MAX487E–MAX491E, and MAX1487E transceivers are designed for bidirectional data communications on multipoint bus transmission lines. Figures 25 and 26 show typical network application circuits. These parts can also be used as line repeaters, with cable lengths longer than 4000 feet.

To minimize reflections, the line should be terminated at both ends in its characteristic impedance, and stub lengths off the main line should be kept as short as possible. The slew-rate-limited MAX483E and MAX487E–MAX489E are more tolerant of imperfect termination. Bypass the V_{CC} pin with 0.1µF.

Isolated RS-485

For isolated RS-485 applications, see the MAX253 and MAX1480 data sheets.

Line Length vs. Data Rate

The RS-485/RS-422 standard covers line lengths up to 4000 feet. Figures 23 and 24 show the system differential voltage for the parts driving 4000 feet of 26AWG twisted-pair wire at 110kHz into 100Ω loads.

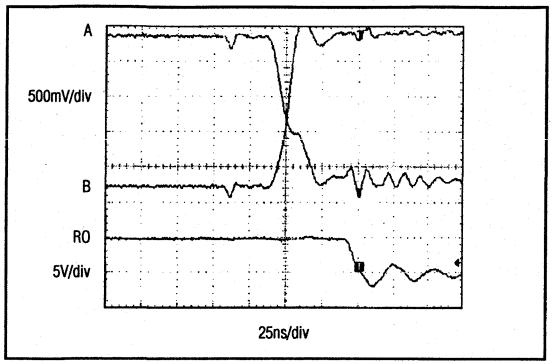


Figure 19. MAX481E/MAX485E/MAX490E/MAX1487E Receiver t_{PHL}

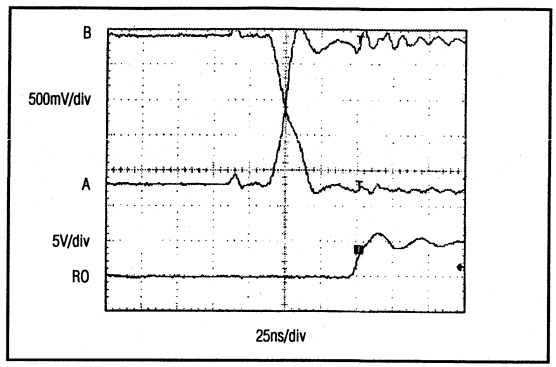


Figure 20. MAX481E/MAX485E/MAX490E/MAX491E/ MAX1487E Receiver t_{PLH}

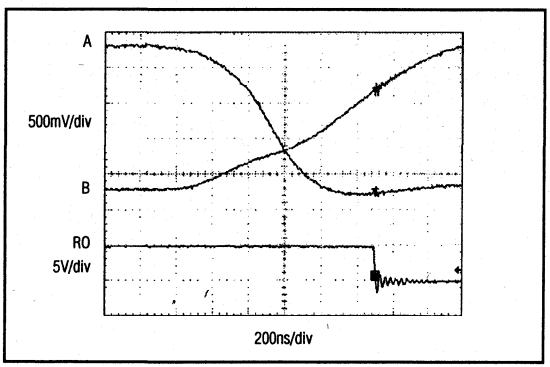


Figure 21. MAX483E/MAX487E–MAX489E Receiver t_{PHL}

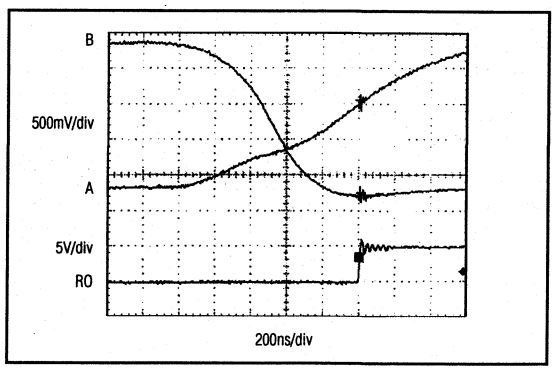


Figure 22. MAX483E/MAX487E–MAX489E Receiver t_{PLH}

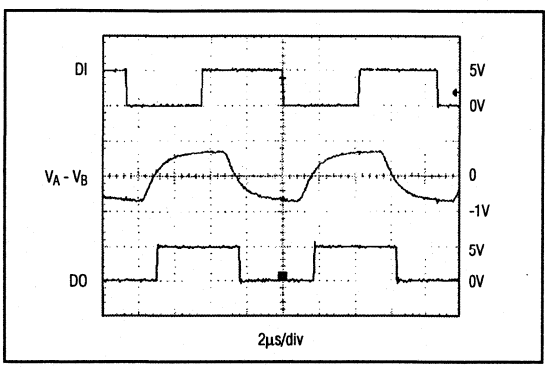


Figure 23. MAX481E/MAX485E/MAX490E/MAX491E/ MAX1487E System Differential Voltage at 110kHz Driving 4000ft of Cable

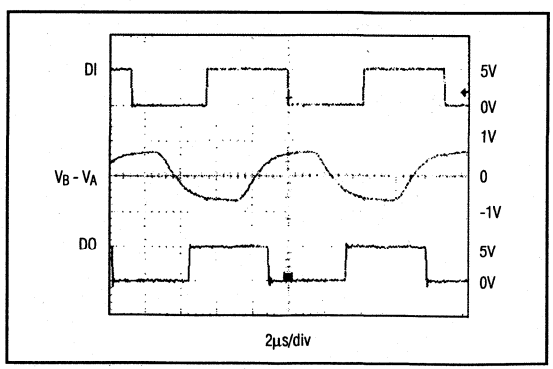


Figure 24. MAX483E/MAX1487E–MAX489E System Differential Voltage at 110kHz Driving 4000ft of Cable

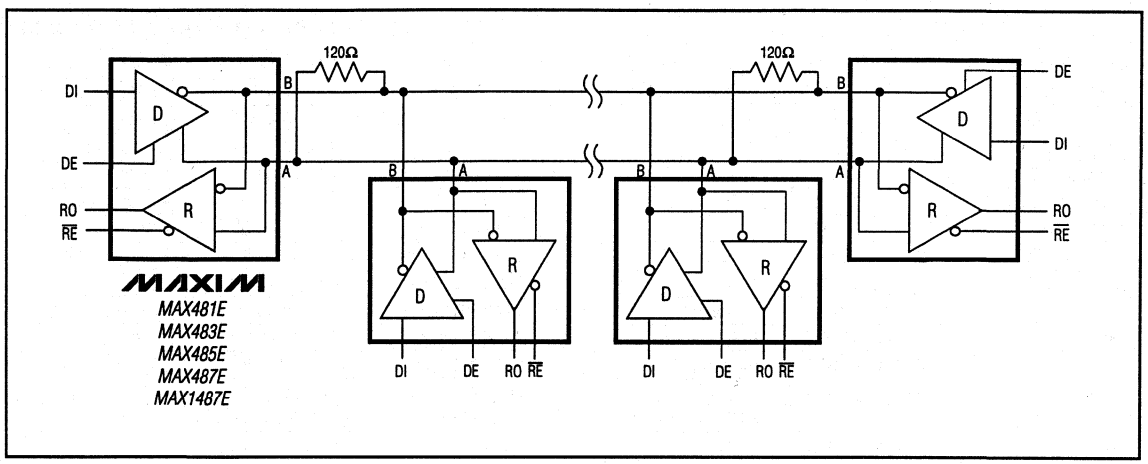


Figure 25. MAX481E/MAX483E/MAX485E/MAX487E/MAX1487E Typical Half-Duplex RS-485 Network

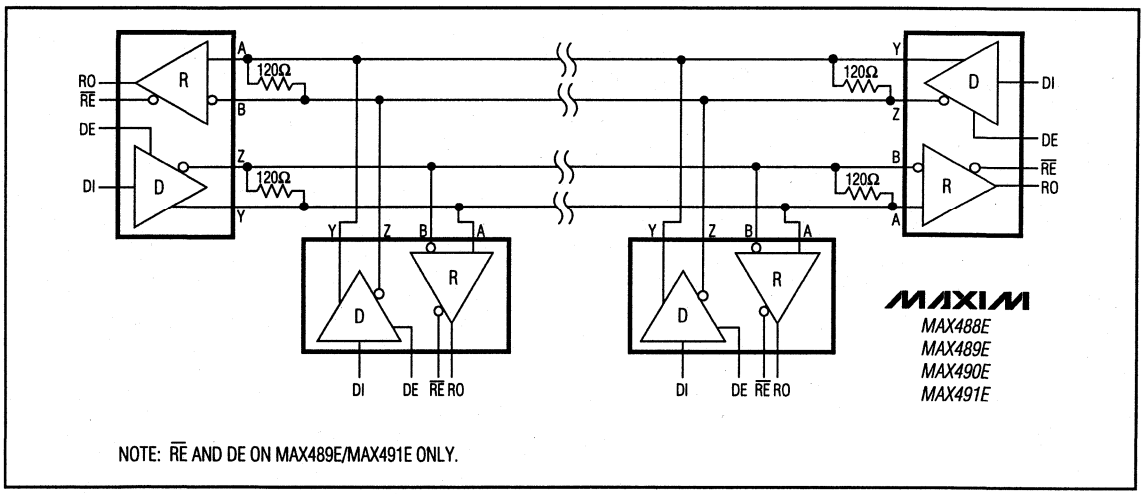


Figure 26. MAX488E–MAX491E Full-Duplex RS-485 Network

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX483ECPA	0°C to +70°C	8 Plastic DIP
MAX483ECSA	0°C to +70°C	8 SO
MAX483EEPA	-40°C to +85°C	8 Plastic DIP
MAX483EESA	-40°C to +85°C	8 SO
MAX485ECPA	0°C to +70°C	8 Plastic DIP
MAX485ECSA	0°C to +70°C	8 SO
MAX485EEPA	-40°C to +85°C	8 Plastic DIP
MAX485EESA	-40°C to +85°C	8 SO
MAX487ECPA	0°C to +70°C	8 Plastic DIP
MAX487ECSA	0°C to +70°C	8 SO
MAX487EEPA	-40°C to +85°C	8 Plastic DIP
MAX487EESA	-40°C to +85°C	8 SO
MAX488ECPA	0°C to +70°C	8 Plastic DIP
MAX488ECSA	0°C to +70°C	8 SO
MAX488EEPA	-40°C to +85°C	8 Plastic DIP
MAX488EESA	-40°C to +85°C	8 SO

PART	TEMP. RANGE	PIN-PACKAGE
MAX489ECPD	0°C to +70°C	14 Plastic DIP
MAX489ECSD	0°C to +70°C	14 SO
MAX489EEPD	-40°C to +85°C	14 Plastic DIP
MAX489EESD	-40°C to +85°C	14 SO
MAX490ECPA	0°C to +70°C	8 Plastic DIP
MAX490ECSA	0°C to +70°C	8 SO
MAX490EEPA	-40°C to +85°C	8 Plastic DIP
MAX490EESA	-40°C to +85°C	8 SO
MAX491ECPD	0°C to +70°C	14 Plastic DIP
MAX491ECSD	0°C to +70°C	14 SO
MAX491EEPD	-40°C to +85°C	14 Plastic DIP
MAX491EESD	-40°C to +85°C	14 SO
MAX1487ECPA	0°C to +70°C	8 Plastic DIP
MAX1487ECSA	0°C to +70°C	8 SO
MAX1487EEPA	-40°C to +85°C	8 Plastic DIP
MAX1487EESA	-40°C to +85°C	8 SO

Chip Information

TRANSISTOR COUNT: 295

19-1120; Rev 0; 9/96

MAXIM

±15kV ESD-Protected, EMC-Compliant, 230kbps, 3-Tx/3-Rx RS-232 IC

General Description

The MAX1406 is an RS-232 IC designed to meet the stringent electrostatic discharge (ESD) requirements of the European community. All transmitter outputs and receiver inputs are protected to ±15kV using IEC1000-4-2 Air-Gap Discharge, ±8kV using IEC 1000-4-2 Contact Discharge, and ±15kV using the Human Body Model.

The MAX1406 has three RS-232 transmitters and three RS-232 receivers, and is optimized for operation in printer, modem, and telecom applications. It is guaranteed to run at data rates up to 230kbps, providing compatibility with popular software for communicating with personal computers. Power-supply current is less than 500µA for I_{DD} and I_{SS}, and less than 1mA for I_{CC}.

The MAX1406 is pin and functionally compatible with the industry-standard MC145406, so existing designs can instantly become Electromagnetic Compatibility (EMC) compliant. The MAX1406 is available in DIP and SO packages, and in a tiny SSOP that reduces board space.

Applications

Telecommunications

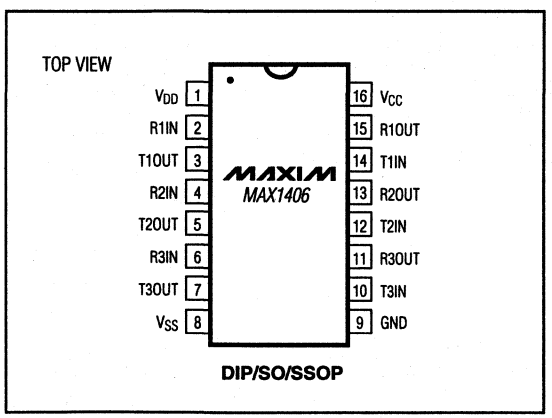
Modems

Printers

Instruments

Equipment Meeting IEC1000-4-2

Pin Configuration



Features

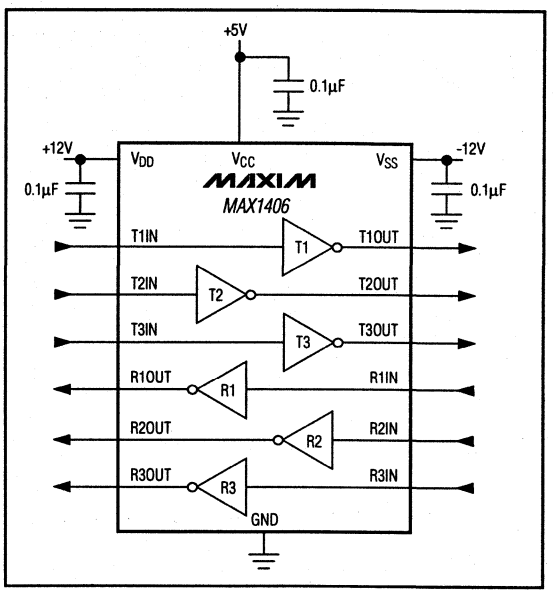
- ♦ **Enhanced ESD Protection:**
  - **±15kV Human Body Model**
  - **±8kV IEC1000-4-2, Contact Discharge**
  - **±15kV IEC1000-4-2, Air-Gap Discharge**
- ♦ **Latchup Free During an ESD Event**
- ♦ **16-Pin SSOP or SO Packages**
- ♦ **Guaranteed 230kbps Data Rate**
- ♦ **Flow-Through Pinout**
- ♦ **Pin Compatible with MC145406**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1406CPE	0°C to +70°C	16 Plastic DIP
MAX1406CWE	0°C to +70°C	16 Wide SO
MAX1406CAE	0°C to +70°C	16 SSOP
MAX1406C/D	0°C to +70°C	Dice*
MAX1406EPE	-40°C to +85°C	16 Plastic DIP
MAX1406EWE	-40°C to +85°C	16 Wide SO
MAX1406EAE	-40°C to +85°C	16 SSOP

*Dice are specified at T_A = +25°C, DC parameters only.

Functional Diagram



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±15kV ESD-Protected, EMC-Compliant, 230kbps, 3-Tx/3-Rx RS-232 IC

ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... -0.3V to +7V
V_{DD} ..... -0.3V to +14V
V_{SS} ..... +0.3V to -14V
Input Voltages
  T_{IN} ..... -0.3V to +6V
  R_{IN} ..... ±30V
Output Voltages
  T_{OUT} ..... ±15V
  R_{OUT} ..... -0.3V to (V_{CC} + 0.3V)
Short-Circuit Duration
  T_{OUT} (one at a time) ..... Continuous
  R_{OUT} (one at a time) ..... Continuous

Continuous Power Dissipation (T_A = +70°C)
  DIP (derate 10.53mW/°C above +70°C) 842mW
  Wide SO (derate 20.00mW/°C above +70°C) 1.6W
  SSOP (derate 8.00mW/°C above +70°C) 640mW
Operating Temperature Ranges
  MAX1406C_E ..... 0°C to +70°C
  MAX1406E_E ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.5V to +5.5V, V_{DD} = +10.8V to +13.2V, V_{SS} = -10.8V to -13.2V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Operating Voltage Range	V_{CC}		4.5		5.5	V
	V_{DD}		10.8		13.2	
	V_{SS}		-13.2		-10.8	
Supply Current	I_{CC}	No load		230	1000	µA
	I_{DD}			185	500	
	I_{SS}			185	500	
LOGIC						
Input Logic Threshold Low	V_{ILT}	T_IN			0.8	V
Input Logic Threshold High	V_{IHT}	T_IN	2.0			V
Input Leakage Current				0.01	1	µA
Output Voltage Low	V_{OLR}	R_{OUT}; I_{SINK} = 3.2mA			0.4	V
Output Voltage High	V_{OHR}	R_{OUT}; I_{SOURCE} = 1mA	V_{CC} - 0.6			V
TRANSMITTER OUTPUTS						
Output Voltage Swing		V_{DD} = 7.0V, V_{SS} = -7.0V, R_L = 3kΩ	±5.0			V
		V_{DD} = 12V, V_{SS} = -12V, R_L = 3kΩ	±9.5			
Transmitter Output Resistance		V_{CC} = V_{DD} = V_{SS} = 0V, V_{T_OUT} = ±2V	300			Ω
RS-232 Output Short-Circuit Current				±35	±60	mA
RECEIVER INPUTS						
Receiver Input Voltage Operating Range			-25		+25	V
RS-232 Input Threshold Low			0.75			V
RS-232 Input Threshold High					2.4	V
RS-232 Input Hysteresis				0.65		V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +4.5V to +5.5V, V_{DD} = +10.8V to +13.2V, V_{SS} = -10.8V to -13.2V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RECEIVER INPUTS (continued)						
RS-232 Input Resistance			3	5	7	kΩ
Receiver Output Short-Circuit Current				±10		mA
ESD CHARACTERISTICS						
ESD Protection		Human Body Model		±15		kV
		IEC1000-4-2 (Contact Discharge)		±8		
		IEC1000-4-2 (Air-Gap Discharge)		±15		

TIMING CHARACTERISTICS

(T_A = +25°C, unless otherwise noted.)

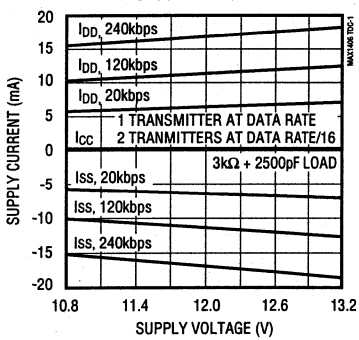
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Transmitter Output Propagation Delay, Low to High	t_{PLHT}	V_{DD} = 12V, V_{SS} = -12V, R_L = 3kΩ, C_L = 1000pF				4	µs
Transmitter Output Propagation Delay, High to Low	t_{PLHT}	V_{DD} = 12V, V_{SS} = -12V R_L = 3kΩ, C_L = 1000pF				4	µs
Transmitter Propagation Delay Skew, $\lvert t_{PLHT} - t_{PHLT} \rvert$	t_{SKT}	V_{DD} = 12V, V_{SS} = -12V R_L = 3kΩ, C_L = 1000pF				0.4	µs
Transition Output Slew Rate	SR	V_{DD} = 12V, V_{SS} = -12V, R_L = 3kΩ to 7kΩ, measured from +3V to -3V or -3V to +3V	C_L = 150pF to 2500pF	4	12	30	V/µs
			C_L = 50pF to 1000pF	8	12	30	
Receiver Output Propagation Delay, Low to High	t_{PLHR}	V_{CC} = 5V, C_L = 50pF				4.0	µs
Receiver Output Propagation Delay, High to Low	t_{PHLR}	V_{CC} = 5V, C_L = 50pF				4.0	µs
Receiver Propagation Delay Skew, $\lvert t_{PLHR} - t_{PHLR} \rvert$	t_{SKR}	V_{CC} = 5V, C_L = 50pF				0.4	µs
Guaranteed Data Rate	DR	V_{CC} = 5V, V_{DD} = 12V, V_{SS} = -12V, R_L = 3kΩ to 7kΩ	C_L = 150pF to 2500pF	120			kbps
			C_L = 50pF to 1000pF	230			

±15kV ESD-Protected, EMC-Compliant, 230kbps, 3-Tx/3-Rx RS-232 IC

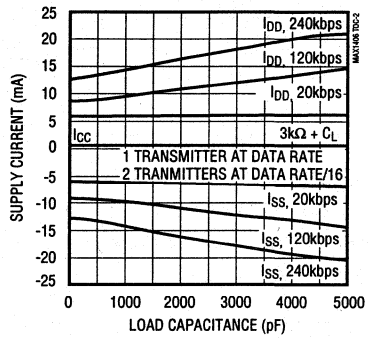
Typical Operating Characteristics

(VCC = +5.0V, VDD = +12.0V, VSS = -12.0V, TA = +25°C, unless otherwise noted.)

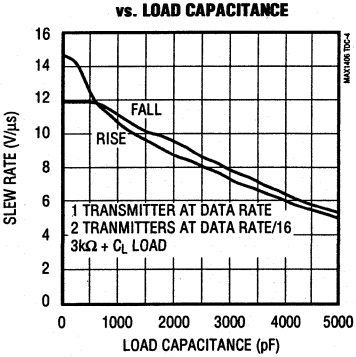
SUPPLY CURRENT vs. SUPPLY VOLTAGE



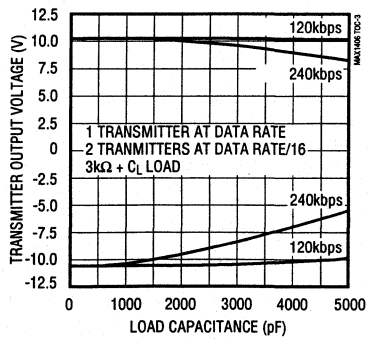
SUPPLY CURRENT vs. LOAD CAPACITANCE



SLEW RATE vs. LOAD CAPACITANCE



TRANSMITTER OUTPUT VOLTAGE vs. LOAD CAPACITANCE



Pin Description

PIN	NAME	FUNCTION
1	V_{DD}	Supply-Voltage Input, +10.8V to +13.2V
3, 5, 7	T1OUT, T2OUT,T3OUT	Transmitter Outputs, swing between V_{DD} and V_{SS}
2, 4, 6	R1IN, R2IN, R3IN	Receiver Inputs
8	V_{SS}	Supply-Voltage Input, -10.8V to -13.2V
9	GND	Ground. Connect to system ground.
10, 12, 14	T3IN, T2IN, T1IN	Transmitter Inputs. Tie unused inputs to GND or V_{CC}.
11, 13, 15	R3OUT, R2OUT, R1OUT	Receiver Outputs, swing between GND and V_{CC}
16	V_{CC}	Supply-Voltage Input, +4.5V to +5.5V

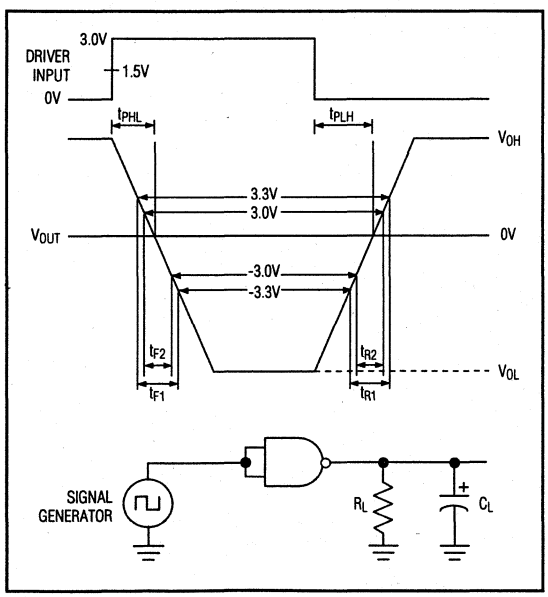


Figure 1. Slew-Rate Test Circuit and Timing Diagram

Detailed Description

RS-232 Transmitters

The transmitters are inverting level translators that convert CMOS-logic input levels to an EIA/TIA-232 voltage between ±5V and ±13.2V, into a load between 3kΩ and 7kΩ. The MAX1406 guarantees a 230kbps data rate with a worst-case load of 3kΩ and 1000pF, providing compatibility with PC-to-PC communication software.

When the power is off, the MAX1406 outputs are permitted to be driven up to ±15V. The transmitter inputs do not have internal pull-up resistors. Connect unused inputs to GND or V_{CC}.

RS-232 Receivers

The receiver inputs invert and convert the RS-232 signals to CMOS-logic output levels. The MAX1406 has hysteresis of 650mV. The receiver output swings between GND and V_{CC}.

±15kV ESD Protection

As with all Maxim devices, electrostatic discharge (ESD) protection structures are incorporated on all pins to protect against ESD encountered during handling and assembly. The MAX1406 driver outputs and receiver inputs have extra protection against static electricity found in normal operation. Maxim's engineers developed state-of-the-art structures to protect these pins against ±15kV ESD without damage. After an ESD event, the MAX1406 continues working without latchup.

ESD protection can be tested in several ways. The transmitter outputs and the receiver inputs are characterized for protection to the following:

1) ±15kV using the Human Body Model

2) ±8kV using the Contact-Discharge method specified in IEC1000-4-2 (formerly IEC801-2)

3) ±15kV using the Air-Gap Discharge method specified in IEC1000-4-2 (formerly IEC801-2)

ESD Test Conditions

ESD performance depends on a number of conditions. Contact Maxim for a reliability report that documents test setup, methodology, and results.

±15kV ESD-Protected, EMC-Compliant, 230kbps, 3-Tx/3-Rx RS-232 IC

Human Body Model

Figure 2a shows the Human Body Model, and Figure 2b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

IEC1000-4-2

The IEC1000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits. The MAX1406 helps you design equipment that meets Level 4 (the highest level) of IEC1000-4-2, without additional ESD-protection components.

The main difference between tests done using the Human Body Model and IEC1000-4-2 is higher peak current in IEC1000-4-2 (Figure 3). Because series resistance is lower in the IEC1000-4-2 ESD test model, the ESD withstand voltage measured to this standard is generally lower than that measured using the Human Body Model. Figure 3b shows the current waveform for the ±8kV IEC1000-4-2 Level 4 ESD Contact-Discharge test.

The Air-Gap test involves approaching the device with a charge probe. The Contact-Discharge method connects the probe to the device before the probe is energized.

Machine Model

The Machine Model for ESD testing uses a 200pF storage capacitor and zero-discharge resistance. It mimics the stress caused by handling during manufacturing and assembly. Of course, all pins (not just RS-232 inputs and outputs) require this protection during manufacturing. Therefore, the Machine Model is less relevant to the I/O ports than are the Human Body Model and IEC1000-4-2.

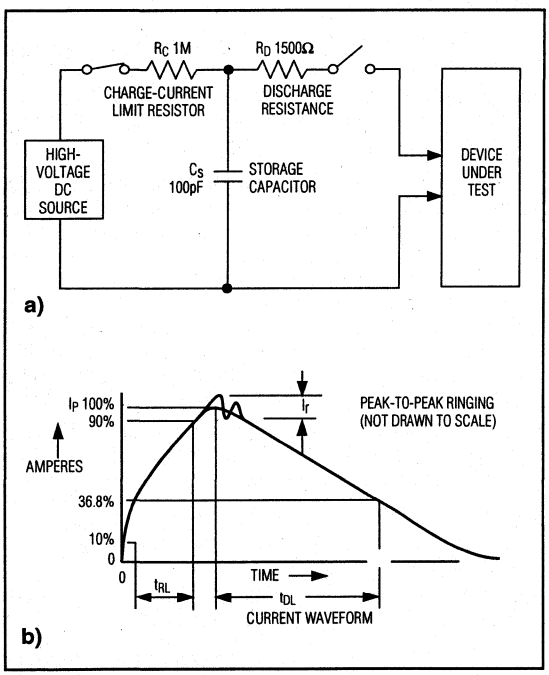


Figure 2. Human Body ESD Test Model and ESD-Generator Current Waveform

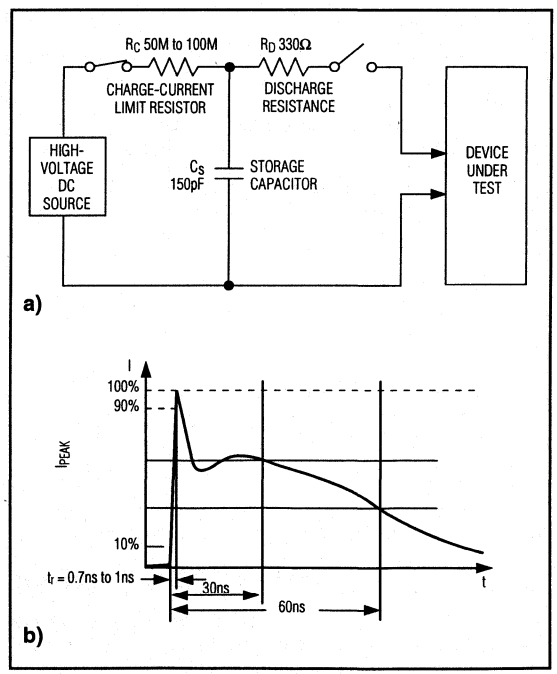


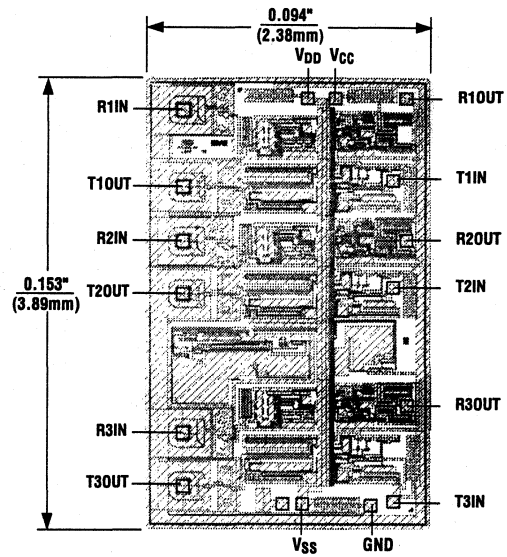
Figure 3. IEC1000-4-2 Test Model and ESD-Generator Current Waveform

Applications Information

Because the MAX1406 is not sensitive to power-supply sequencing, no external protection diodes are required. Any of the three supplies can power up first. However, use proper layout techniques to ensure other devices on your board are not damaged in case of an ESD event.

- Minimize the ground-lead return path to the power supply, because currents as high as 60A can pass into the ground.
- Use a separate return path to the power supply.
- Make trace widths greater than 40 mils.
- Bypass V_{CC}, V_{DD}, and V_{SS} with 0.1µF capacitors as close to the MAX1406 as possible to ensure maximum ESD protection.
- Tie any unused transmitter inputs to GND or V_{CC} to minimize power consumption.

Chip Topography



TRANSISTOR COUNT: 161

SUBSTRATE CONNECTED TO GND

19-0259; Rev 1; 1/96

MAXIM

Complete, Isolated, RS-485/RS-422 Data Interface

General Description

The MAX1480A/MAX1480B/MAX1490A/MAX1490B are complete, electrically isolated, RS-485/RS-422 data-communications interface solutions. Transceivers, optocouplers, and a transformer provide a complete interface in a standard DIP package. A single +5V supply on the logic side powers both sides of the interface.

The MAX1480B/MAX1490B feature reduced-slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free data transmission at data rates up to 250kbps. The MAX1480A/MAX1490A driver slew rate is not limited, allowing transmission rates up to 2.5Mbps. The MAX1480A/B are designed for half-duplex communication, while the MAX1490A/B feature full-duplex communication.

Drivers are short-circuit current limited and protected against excessive power dissipation by thermal shutdown circuitry that places the driver outputs into a high-impedance state. The receiver input has a fail-safe feature that guarantees a known output ($\overline{RO}$ low for the MAX1480A/B, RO high for the MAX1490A/B) if the input is open circuit.

The MAX1480A/MAX1480B/MAX1490A/MAX1490B typically withstand 1600V_{RMS} (1 minute) or 2000V_{RMS} (1 second). Their isolated outputs meet all RS-485/RS-422 specifications. The MAX1480A/B are available in a 28-pin DIP package, and the MAX1490A/B are available in a 24-pin DIP package.

Selection Table

PART	HALF/FULL DUPLEX	DATA RATE (Mbps)	SLEW-RATE LIMITED	DRIVER ENABLE
MAX1480A	Half	2.5	No	Yes
MAX1480B	Half	0.25	Yes	Yes
MAX1490A	Full	2.5	No	No
MAX1490B	Full	0.25	Yes	No

Applications

Isolated RS-485/RS-422 Data Interface
Transceivers for EMI-Sensitive Applications
Industrial-Control Local Area Networks
Automatic Test Equipment
HVAC/Building Control Networks

Features

- **Isolated Data Interface, Typically to 1600V_{RMS} (1 minute)**
- **Slew-Rate Limited for Errorless Data Transmission (MAX1480B/MAX1490B)**
- **High-Speed, Isolated, 2.5Mbps RS-485/RS-422 Interface (MAX1480A/MAX1490A)**
- **Full-Duplex Data Communication (MAX1490A/B)**
- **-7V to +12V Common-Mode Input Voltage Range with Respect to Isolated Ground**
- **Single +5V Supply**
- **Current Limiting and Thermal Shutdown for Driver Overload Protection**
- **Standard 0.6" DIP Package:**
  28-Pin DIP (MAX1480A/B)
  24-Pin DIP (MAX1490A/B)

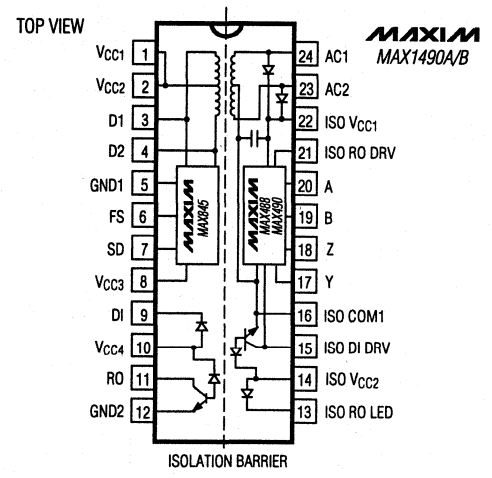
Ordering Information

PART†	TEMP. RANGE	PIN-PACKAGE
MAX1480ACPI	0°C to +70°C	28 Wide Plastic DIP
MAX1480AEPI	-40°C to +85°C	28 Wide Plastic DIP

Ordering Information continued at end of data sheet.

† *Data rate for "A" parts is up to 2500kbps. Data rate for "B" parts is up to 250kbps.*

Pin Configurations



DIP

Pin Configurations continued at end of data sheet.

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Complete, Isolated, RS-485/RS-422 Data Interface

ABSOLUTE MAXIMUM RATINGS

With Respect to GND_
- Supply Voltage ($V_{CC_}$) ..... -0.3V to +6V
- Control Input Voltage (SD, FS) ..... -0.3V to ($V_{CC_}$ + 0.3V)
- Receiver Output Voltage ($\overline{RO}$, RO) ..... -0.3V to ($V_{CC_}$ + 0.3V)
- Output Switch Voltage (D1, D2) ..... +12V

With Respect to ISO COM_
- Control Input Voltage (ISO DE_) .... -0.3V to (ISO $V_{CC_}$ + 0.3V)
- Driver Input Voltage (ISO DI_) ..... -0.3V to (ISO $V_{CC_}$ + 0.3V)
- Receiver Output Voltage (ISO RO_) .-0.3V to (ISO $V_{CC_}$ + 0.3V)
- Driver Output Voltage (A, B, Y, Z) ..... -8V to +12.5V
- Receiver Input Voltage (A, B) ..... -8V to +12.5V

LED Forward Current (DI, DE, ISO RO LED) 50mA

Continuous Power Dissipation (T_A = +70°C)
- 24-Pin Plastic DIP (derate 8.7mW°C above +70°C) 696mW
- 28-Pin Plastic DIP (derate 9.09mW/°C above +70°C) .. 727mW

Operating Temperature Ranges
- MAX1480_CPI/MAX1490_CPI ..... 0°C to +70°C
- MAX1480_EPI/MAX1490_EPI ..... -40°C to +85°C

Storage Temperature Range ..... -65°C to +160°C

Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{CC_}$ = 5V ±10%, FS = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at $V_{CC_}$ = 5V and T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V_S	FS = 0V		4.5	5.0	5.5	V
		FS = $V_{CC_}$ or open		4.75	5.0	5.25	
Switch Frequency	F_{SWL}	FS = 0V	MAX1480A/B		200		kHz
			MAX1490A/B		535		
	F_{SWH}	FS = $V_{CC_}$ or open	MAX1480A/B		350		
			MAX1490A/B		725		
Operating Supply Current	I_{CC}	MAX1480A, DE´ = $V_{CC_}$ or open	R_L = ∞		55	90	mA
			R_L = 54Ω		120		
		MAX1480B, DE´ = $V_{CC_}$ or open	R_L = ∞		28	45	
			R_L = 54Ω		86		
		MAX1490A	R_L = ∞		100	150	
			R_L = 54Ω		170		
		MAX1490B	R_L = ∞		65	125	
			R_L = 54Ω		135		
Shutdown Supply Current (Note 3)	I_{SHDN}	SD = $V_{CC_}$			0.2		µA
Shutdown Input Threshold	V_{SDH}	High		2.4			V
	V_{SDL}	Low				0.8	
Shutdown Input Leakage Current					10		pA
FS Input Threshold	V_{FSH}	High		2.4			V
	V_{FSL}	Low				0.8	
FS Input Pull-Up Current		FS low				50	µA
FS Input Leakage Current		FS high			10		pA
Input High Voltage	V_{IH}	DE´, DI´		$V_{CC_}$ - 0.4			V
Input Low Voltage	V_{IL}	DE´, DI´				0.4	V
Isolation Resistance	R_{ISO}	T_A = +25°C, V_{ISO} = 50VDC		100	10,000		MΩ
Isolation Capacitance	C_{ISO}	T_A = +25°C, V_{ISO} = 50VDC			10		pF

ELECTRICAL CHARACTERISTICS (continued)

($V_{CC_}$ = 5V ±10%, FS = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at $V_{CC_}$ = 5V and T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Differential Driver Output (no load)	V_{OD1}					8	V
Differential Driver Output (with load)	V_{OD2}	R = 50Ω (RS-422)		2			V
		R = 27Ω (RS-485), Figure 4		1.5		5	
Change in Magnitude of Driver Output Voltage for Complementary Output States	ΔV_{OD}	R = 27Ω or 50Ω, Figure 4	Differential			0.3	V
			Common Mode			0.3	
Driver Common-Mode Output	V_{OC}	R = 27Ω or 50Ω, Figure 4				4	V
Input Current (A, B)	ISO I_{IN}	DE´ = 0V, $V_{CC_}$ = 0V or 5.5V	V_{IN} = 12V			1.0	mA
			V_{IN} = -7V			0.8	
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ 12V		12			kΩ
Receiver Differential Threshold	V_{TH}	-7V ≤ V_{CM} ≤ 12V		-0.2		0.2	V
Receiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0V			70		mV
$\overline{\text{Receiver Output}}$/Receiver Output Low Voltage	V_{OL}	Using resistor values listed in Tables 1 and 2				0.4	V
$\overline{\text{Receiver Output}}$/Receiver Output High Current	I_{OH}	V_{OUT} = 5.5V				250	µA
Driver Short-Circuit Current	ISO I_{OSD}	-7V ≤ V_O ≤ 12V (Note 4)			100		mA

SWITCHING CHARACTERISTICS—MAX1480A/MAX1490A

($V_{CC_}$ = 5V ±10%, FS = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at $V_{CC_}$ = 5V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Input to Output Propagation Delay	t_{PLH}	Figures 5 and 7, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		100	275	ns
	t_{PHL}			100	275	
Driver Output Skew	t_{SKEW}	Figures 5 and 7, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		25	90	ns
Driver Rise or Fall Time	t_R, t_F	Figures 5 and 7, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		15	40	ns
Driver Enable to Output High (MAX1480A only)	t_{ZH}	Figures 6 and 8, C_L = 100pF, S2 closed		0.5	1.5	µs
Driver Enable to Output Low (MAX1480A only)	t_{ZL}	Figures 6 and 8, C_L = 100pF, S1 closed		0.5	1.5	µs
Driver Disable Time from Low (MAX1480A only)	t_{LZ}	Figures 6 and 8, C_L = 15pF, S1 closed		0.5	1.5	µs
Driver Disable Time from High (MAX1480A only)	t_{HZ}	Figures 6 and 8, C_L = 15pF, S2 closed		0.5	1.5	µs
Receiver Input to Output Propagation Delay	t_{PLH}	Figures 5 and 10, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		100	225	ns
	t_{PHL}			100	225	
$\lvert t_{PLH} - t_{PHL} \rvert$ Differential Receiver Skew	t_{SKD}	Figures 5 and 10, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		20		ns
Maximum Data Rate	f_{MAX}	t_{PLH}, t_{PHL} < 50% of data period	2.5			Mbps
Time to Shutdown	t_{SHDN}			100		µs
Shutdown to Driver Output High	$t_{ZH(SHDN)}$	Figures 6 and 9, C_L = 100pF, S2 closed		3	10	µs
Shutdown to Driver Output Low	$t_{ZL(SHDN)}$	Figures 6 and 9, C_L = 100pF, S1 closed		3	10	µs

Complete, Isolated, RS-485/RS-422 Data Interface

SWITCHING CHARACTERISTICS—MAX1480B/MAX1490B

($V_{CC_}$ = 5V ±10%, FS = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at $V_{CC_}$ = 5V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Input to Output Propagation Delay	t_{PLH}	Figures 5 and 7, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		1.0	2.0	µs
	t_{PHL}	Figures 5 and 7, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		1.0	2.0	
Driver Output Skew	t_{SKEW}	Figures 5 and 7, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		100	800	ns
Driver Rise or Fall Time	t_R, t_F	Figures 5 and 7, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		1.0	2.0	µs
Driver Enable to Output High (MAX1480B only)	t_{ZH}	Figures 6 and 8, C_L = 100pF, S2 closed		35	100	µs
Driver Enable to Output Low (MAX1480B only)	t_{ZL}	Figures 6 and 8, C_L = 100pF, S1 closed		35	100	µs
Driver Disable Time from Low (MAX1480B only)	t_{LZ}	Figures 6 and 8, C_L = 15pF, S1 closed		13	50	µs
Driver Disable Time from High (MAX1480B only)	t_{HZ}	Figures 6 and 8, C_L = 15pF, S2 closed		13	50	µs
Receiver Input to Output Propagation Delay	t_{PLH}	Figures 5 and 10, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		0.8	2.0	µs
	t_{PHL}			0.8	2.0	
$\lvert t_{PLH} - t_{PHL} \rvert$ Differential Receiver Skew	t_{SKD}	Figures 5 and 10, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		200		ns
Maximum Data Rate	f_{MAX}	t_{PLH}, t_{PHL} < 50% of data period	0.25			Mbps
Time to Shutdown	t_{SHDN}			100		µs
Shutdown to Driver Output High	$t_{ZH(SHDN)}$	Figures 6 and 9, C_L = 100pF, S2 closed		35	100	µs
Shutdown to Driver Output Low	$t_{ZL(SHDN)}$	Figures 6 and 9, C_L = 100pF, S1 closed		35	100	µs

Note 1: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to logic-side ground (GND_), unless otherwise specified.

Note 2: For $\overline{DE}$ and $\overline{DI}$ pin descriptions, see *Detailed Block Diagram and Typical Application Circuit* (Figure 1 for MAX1480A/MAX1480B, Figure 2 for MAX1490A/MAX1490B).

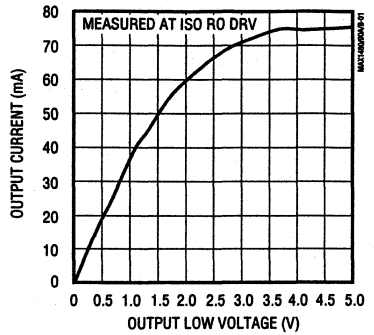
Note 3: Shutdown supply current is the current at V_{CC1} and V_{CC2} when shutdown is enabled.

Note 4: Applies to peak current (see *Typical Operating Characteristics*). Although the MAX1480A/B and MAX1490A/B provide electrical isolation between logic ground and signal paths, they do not provide isolation between external shields and the signal paths (see *Isolated Common Connection* section).

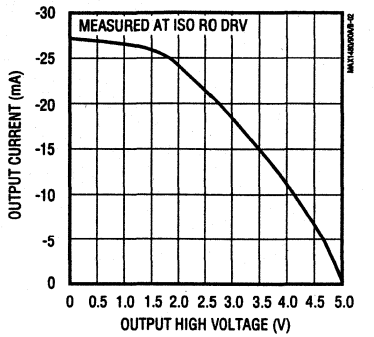
Typical Operating Characteristics

($V_{CC_}$ = 5V, T_A = +25°C, unless otherwise noted.)

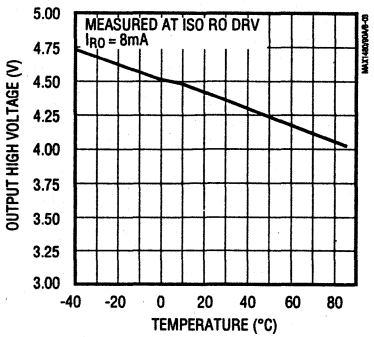
OUTPUT CURRENT vs. RECEIVER OUTPUT LOW VOLTAGE



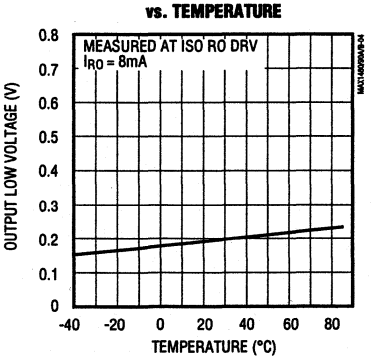
OUTPUT CURRENT vs. RECEIVER OUTPUT HIGH VOLTAGE



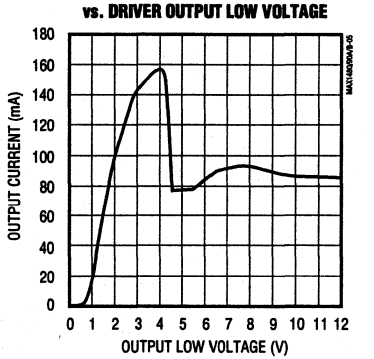
RECEIVER OUTPUT HIGH VOLTAGE vs. TEMPERATURE



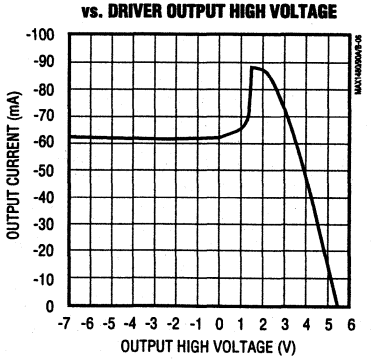
RECEIVER OUTPUT LOW VOLTAGE vs. TEMPERATURE



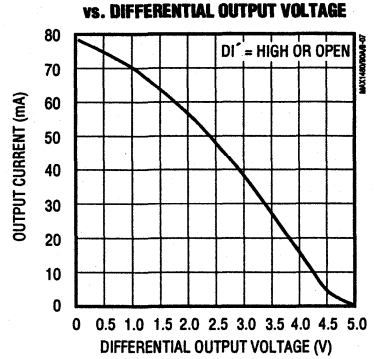
OUTPUT CURRENT vs. DRIVER OUTPUT LOW VOLTAGE



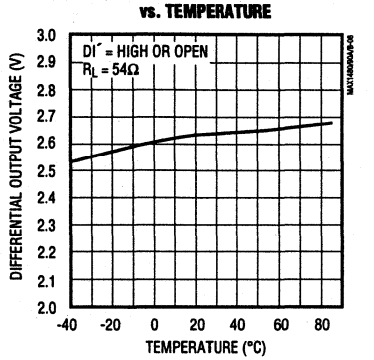
OUTPUT CURRENT vs. DRIVER OUTPUT HIGH VOLTAGE



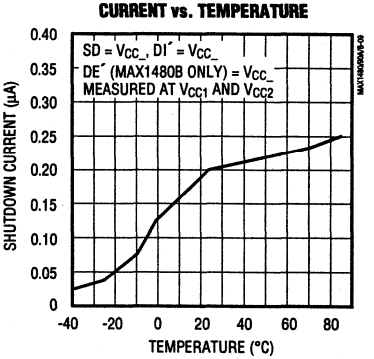
DRIVER OUTPUT CURRENT vs. DIFFERENTIAL OUTPUT VOLTAGE



DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs. TEMPERATURE



MAX1480B/MAX1490B SHUTDOWN CURRENT vs. TEMPERATURE

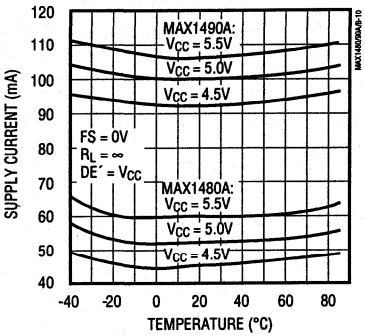


Complete, Isolated, RS-485/RS-422 Data Interface

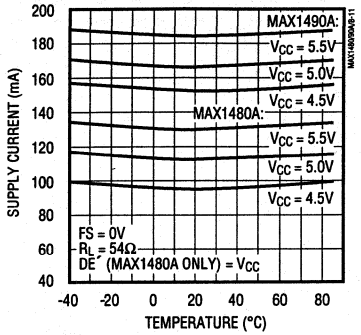
Typical Operating Characteristics (continued)

($V_{CC_}$ = 5V, T_A = +25°C, unless otherwise noted.)

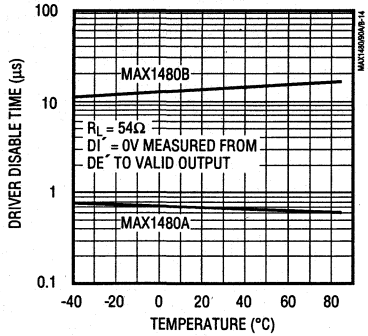
MAX1480A/MAX1490A UNLOADED SUPPLY CURRENT vs. TEMPERATURE



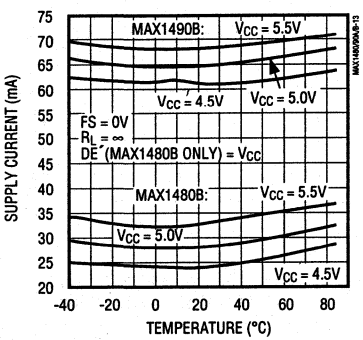
MAX1480A/MAX1490A LOADED SUPPLY CURRENT vs. TEMPERATURE



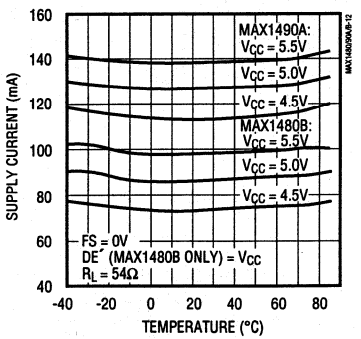
DRIVER DISABLE TIME vs. TEMPERATURE



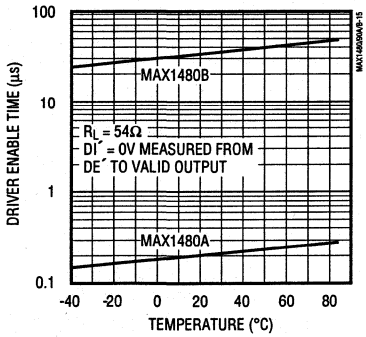
MAX1480B/MAX1490B UNLOADED SUPPLY CURRENT vs. TEMPERATURE



MAX1480B/MAX1490B LOADED SUPPLY CURRENT vs. TEMPERATURE



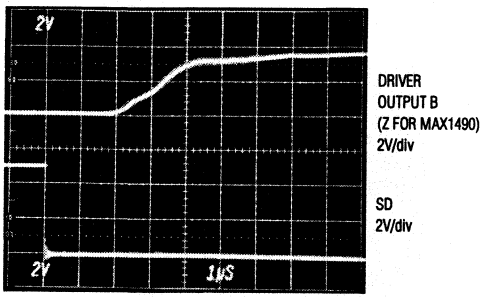
DRIVER ENABLE TIME vs. TEMPERATURE



Typical Operating Characteristics (continued)

($V_{CC_}$ = 5V, T_A = +25°C, unless otherwise noted.)

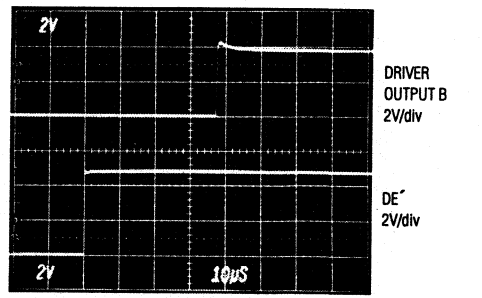
MAX1480A/MAX1490A
POWER-UP DELAY TO DRIVER OUTPUTS VALID



1µs/div

$V_{CC_}$ = 5.0V, DI´= 0V
SD = 5V TO 0V AT 1kHz

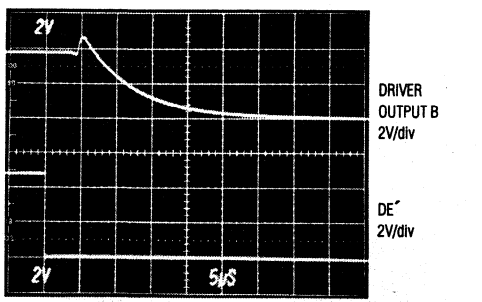
MAX1480B
DRIVER ENABLE TIME



10µs/div

$V_{CC_}$ = 5.0V, DI´= 0V
DE´ TOGGLED 0V TO 5V AT 5kHz

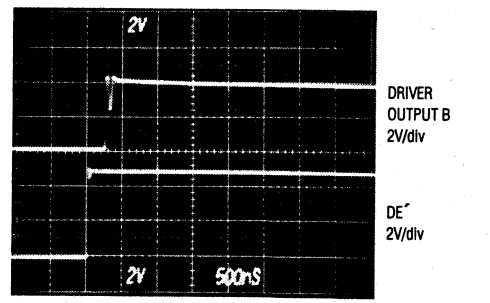
MAX1480B
DRIVER DISABLE TIME



5µs/div

$V_{CC_}$ = 5.0V, DI´= 0V
DE´ TOGGLED 0V TO 5V AT 5kHz

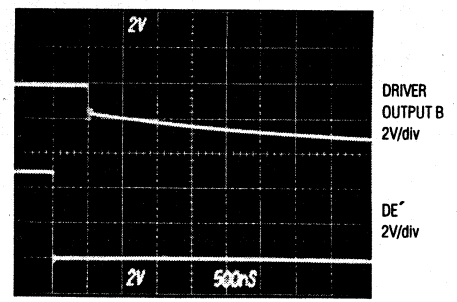
MAX1480A
DRIVER ENABLE TIME



500ns/div

$V_{CC_}$ = 5.0V, DI´= 0V
DE´ TOGGLED 0V TO 5V AT 5kHz

MAX1480A
DRIVER DISABLE TIME



500ns/div

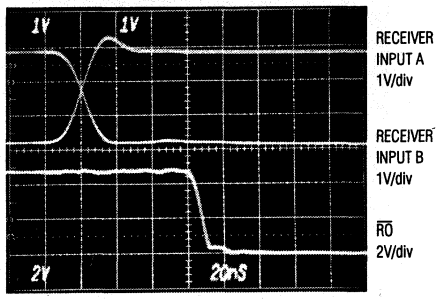
$V_{CC_}$ = 5.0V, DI´= 0V
DE´ TOGGLED 0V TO 5V AT 5kHz

Complete, Isolated, RS-485/RS-422 Data Interface

Typical Operating Characteristics (continued)

($V_{CC_}$ = 5V, T_A = +25°C, unless otherwise noted.)

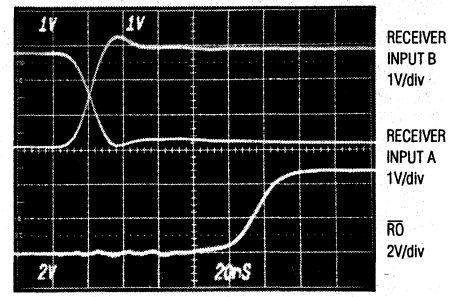
MAX1480A/MAX1490A
RECEIVER t_{PHL}



20ns/div

$V_{CC_}$ = 5.0V, DE = $V_{CC_}$
DI = 0V TO 5V AT 1.25MHz

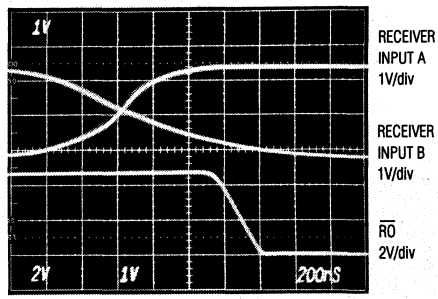
MAX1480A/MAX1490A
RECEIVER t_{PLH}



20ns/div

$V_{CC_}$ = 5.0V, DE = $V_{CC_}$
DI = 0V TO 5V AT 1.25MHz

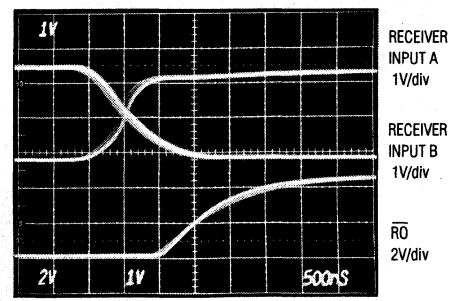
MAX1480B/MAX1490B
RECEIVER t_{PHL}



200ns/div

$V_{CC_}$ = 5.0V, DE = $V_{CC_}$
DI = 0V TO 5V AT 125kHz

MAX1480B/MAX1490B
RECEIVER t_{PLH}



500ns/div

$V_{CC_}$ = 5.0V, DE = $V_{CC_}$
DI = 0V TO 5V AT 125kHz

Pin Descriptions

PIN		NAME	FUNCTION
MAX1480A/B	MAX1490A/B		
PINS ON THE NON-ISOLATED SIDE			
1, 2, 8, 10	1, 2, 8, 10	V_{CC1}–V_{CC4}	Logic-Side (non-isolated side) +5V Supply Voltages
3, 4	3, 4	D1, D2	Internal Connections. Leave these pins unconnected.
5	5	GND1	Logic-Side Ground. Connect to GND2 (pin 12).
6	6	FS	Frequency Switch Input. If FS = $V_{CC_}$ or is open, switch frequency is high; if FS = 0V, switch frequency is low.
7	7	SD	Shutdown Input. Ground for normal operation. When high, the power oscillator is disabled.
9	9	DI	Driver Input. With DE´ high (MAX1480A/B only), a low on DI´ forces output A low and output B high. Similarly, a high on DI´ forces output A high and output B low. Drives internal LED cathode through a resistor (Table 1 of Figure 1 for MAX1480, Table 2 of Figure 2 for MAX1490).
11	—	DE	Driver-Enable Input. The driver outputs, A and B, are enabled by bringing DE´ high. The driver outputs are high impedance when DE´ is low. If the driver outputs are enabled, the device functions as a line driver. While the driver outputs are high impedance, the device functions as a line receiver. Drives internal LED cathode through a resistor (Table 1 of Figure 1).
—	11	RO	Receiver Output. If A > B by 200mV, RO will be high; if A < B by 200mV, RO will be low. Open collector; must have pull-up to V_{CC} (Table 2 of Figure 2).
12	12	GND2	Logic-Side Ground. Connect to GND1 (pin 5).
13	—	$\overline{RO}$	Receiver Output. If A > B by 200mV, $\overline{RO}$ will be low; if A < B by 200mV, $\overline{RO}$ will be high. Open collector; must have pull-up to $V_{CC_}$ (Table 1 of Figure 1).
14	—	V_{CC5}	Logic-Side (non-isolated side) +5V Supply Voltage
PINS ON THE ISOLATED RS-485/RS-422 SIDE			
15	13	ISO RO LED	Isolated Receiver Output LED. Internal LED anode in MAX1480 and LED cathode in MAX1490. Connect to ISO RO DRV through a resistor (Table 1 of Figure 1 for MAX1480; Table 2 of Figure 2 for MAX1490).
16	—	ISO COM2	Isolated Common. Connect to ISO COM1 (pin 20).
17	—	ISO DE DRV	Isolated Driver-Enable Drive. The driver outputs, A and B, are enabled by bringing DE´ high. The driver outputs are high impedance when DE´ is low. If the driver outputs are enabled, the device functions as a line driver. While the driver outputs are high impedance, the device functions as a line receiver. Open-collector output; must have pull-up to ISO VCC_ and be tied to ISO DE IN for normal operation (Table 1 of Figure 1).
18	14	ISO V_{CC2}	Isolated Supply Voltage. Connect to ISO V_{CC1} (pin 26 for MAX1480, or pin 22 for MAX1490).
19	15	ISO DI DRV	Isolated Driver-Input Drive. With DE´ high (MAX1480 only), a low on DI´ forces output A low and output B high. Similarly, a high on DI´ forces output A high and output B low. Connect to ISO DI IN (on the MAX1480 only) for normal operation. Open-collector output; connect a pull-up resistor to ISO $V_{CC_}$ (Table 1 of Figure 1 for MAX1480; Table 2 of Figure 2 for MAX1490).
20	16	ISO COM1	Isolated Common. For MAX1480, connect to ISO COM2 (pin 16) (Figures 1 and 2).

Complete, Isolated, RS-485/RS-422 Data Interface

Pin Descriptions (continued)

PIN		NAME	FUNCTION
MAX1480A/B	MAX1490A/B		
PINS ON THE ISOLATED RS-485/RS-422 SIDE (continued)			
—	17	Y	Noninverting Driver Output
—	18	Z	Inverting Driver Output
—	19	B	Inverting Receiver Input
—	20	A	Noninverting Receiver Input
21	—	ISO DE IN	Isolated Driver-Enable Input. Connect to ISO DI DRV for normal operation.
22	—	ISO DI IN	Isolated Driver Input. Connect to ISO DI DRV for normal operation.
23	—	A	Noninverting Driver Output and Noninverting Receiver Input
24	21	ISO RO DRV	Isolated Receiver-Output Drive. Connect to ISO RO LED through a resistor (Table 1 of Figure 1 for MAX1480, Table 2 of Figure 2 for MAX1490).
25	—	B	Inverting Driver Output and Inverting Receiver Input
26	22	ISO V_{CC1}	Isolated Supply Voltage Source
27, 28	23, 24	AC2, AC1	Internal Connections. Leave these pins unconnected.

Note: For DE′ and DI′ pin descriptions, see *Detailed Block Diagram and Typical Application Circuit* (Figure 1 for MAX1480A/B, Figure 2 for MAX1490A/B).

Detailed Description

The MAX1480A/MAX1480B/MAX1490A/MAX1490B are complete, electrically isolated, RS-485/RS-422 data-communications interface solutions. Transceivers, optocouplers, a power driver, and a transformer in one standard 28-pin DIP package (24-pin for the MAX1490A/B) provide a complete interface. Signals and power are internally transported across the isolation barrier (Figures 1, 2). Power is transferred from the logic side (non-isolated side) to the isolated side of the barrier through a center-tapped transformer. Signals cross the barrier through high-speed optocouplers. A single +5V supply on the logic side powers both sides of the interface. The MAX1480A/B offer half-duplex communications while the MAX1490A/B feature full-duplex communication. The functional input/output relationships are shown in Tables 3–6.

The MAX1480B/MAX1490B feature reduced-slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free transmission at data rates up to 250kbps. The MAX1480A/MAX1490A driver slew rate is not limited, allowing transmission rates up to 2.5Mbps.

The MAX1480B/MAX1490B shutdown feature reduces supply current to as low as 0.2µA by using the SD pin (see *Low-Power Shutdown Mode* section).

Use the FS pin to select between high and low switching frequencies for the isolated power driver. The driver switches at the lower frequency (200kHz for the MAX1480A/B, 535kHz for the MAX1490A/B) when FS is low, and at the higher frequency (350kHz for the MAX1480A/B, 725kHz for the MAX1490A/B) when FS is high. At the lower switching frequency, the devices' operating voltage ranges increase from 5V ±5% to 5V ±10%.

The FS pin has a weak internal pull-up that switches the device to the high-frequency mode when FS is left unconnected. With FS high or open, no-load supply current is reduced by approximately 4mA, and by up to 8mA when fully loaded.

Drivers are short-circuit current limited and are protected against excessive power dissipation by thermal shutdown circuitry that puts the driver outputs into a high-impedance state. The receiver input has a fail-safe feature that guarantees a logic-high RO (logic-low $\overline{RO}$) output if the input is open circuit.

On the MAX1480A/B, the driver outputs are enabled by bringing DE′ high. Driver-enable times are typically 0.5µs for the MAX1480A and 35µs for the MAX1480B. Allow time for the devices to be enabled before sending data (see the Driver Enable Time vs. Temperature graph in the *Typical Operating Characteristics*). When enabled, driver outputs function as line drivers. Driver outputs are high impedance when DE′ is low. While outputs are high impedance, they function as line receivers.

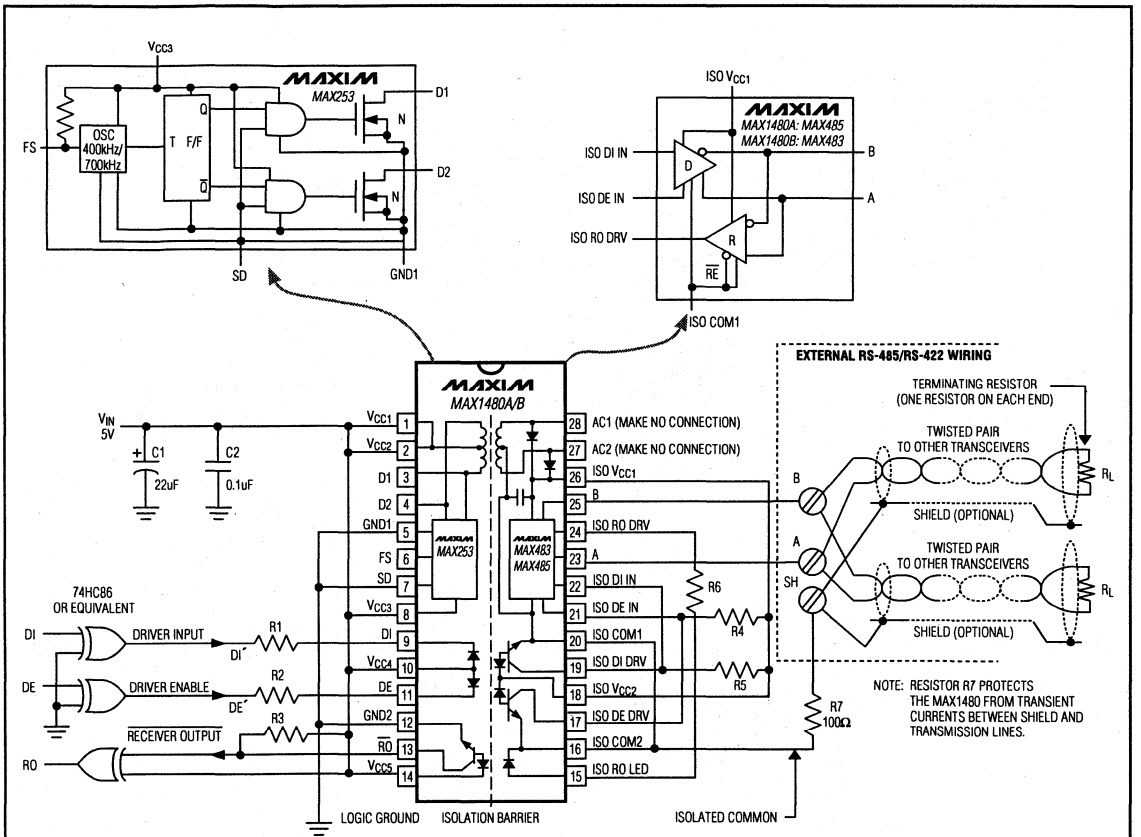


Table 1. Pull-Up and LED Drive Resistors

PART	R1 (Ω)	R2 (Ω)	R3 (Ω)	R4 (Ω)	R5 (Ω)	R6 (Ω)
MAX1480A	200	200	1000	4300	1000	200
MAX1480B	200	510	3000	2200	3000	200

Figure 1. MAX1480A/MAX1480B Detailed Block Diagram and Typical Application Circuit

The MAX1480A/MAX1480B/MAX1490A/MAX1490B typically withstand 1600V_{RMS} (1 minute) or 2000V_{RMS} (1 second). The logic inputs can be driven from TTL/CMOS-logic with a series resistor, and the received data output can directly drive TTL or CMOS-logic families with only resistive pull-up.

Low-Power Shutdown Mode

The SD pin shuts down the oscillator on the internal power driver. With the primary side in shutdown, no power is transferred across the isolation barrier. The DI and DE optocouplers, however, still consume current if the drive signals on the non-isolated side are low. Therefore, leave DI´ and DE´ high or floating when in shutdown mode.

Complete, Isolated, RS-485/RS-422 Data Interface

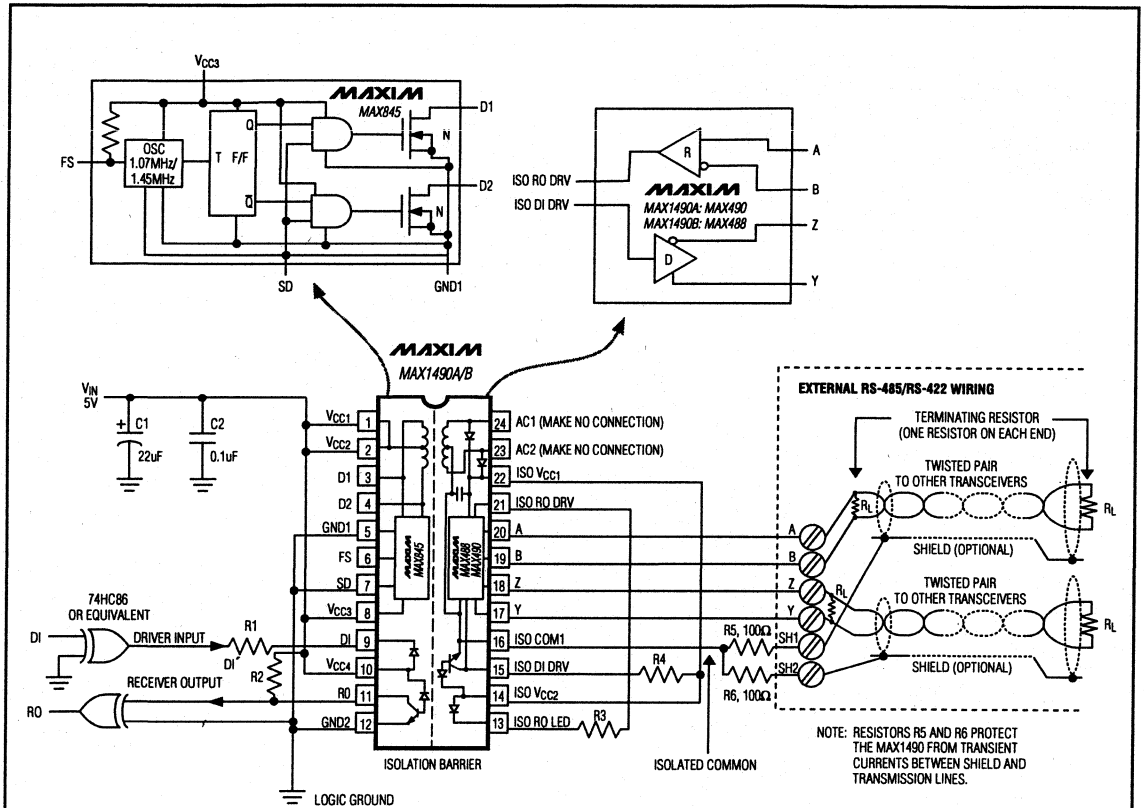


Table 2. Pull-Up and LED Drive Resistors

PART	R1 (Ω)	R2 (Ω)	R3 (Ω)	R4 (Ω)
MAX1490A	200	1000	330	1000
MAX1490B	200	3000	330	3000

Figure 2. MAX1490A/MAX1490B Detailed Block Diagram and Typical Application Circuit

Under these conditions, the MAX1480B/MAX1490B supply current is reduced to as low as 0.2µA.

The high-speed optocouplers on the MAX1480A/MAX1490A consume an additional 10mA through V_{CC5} (V_{CC4} for the MAX1490A). Therefore, to completely shut down these devices, use an external P-channel MOSFET as shown in Figure 3. In normal operation, SD is low, turning the MOSFET on and thereby providing power to all the $V_{CC_}$ pins. When SD is pulled high, the power oscillator is disabled and the switch is turned off, disconnecting power from the DI and DE optocouplers. In normal operating mode, the switch carries only the optocoupler currents, so an on-resistance of several ohms will not significantly degrade efficiency.

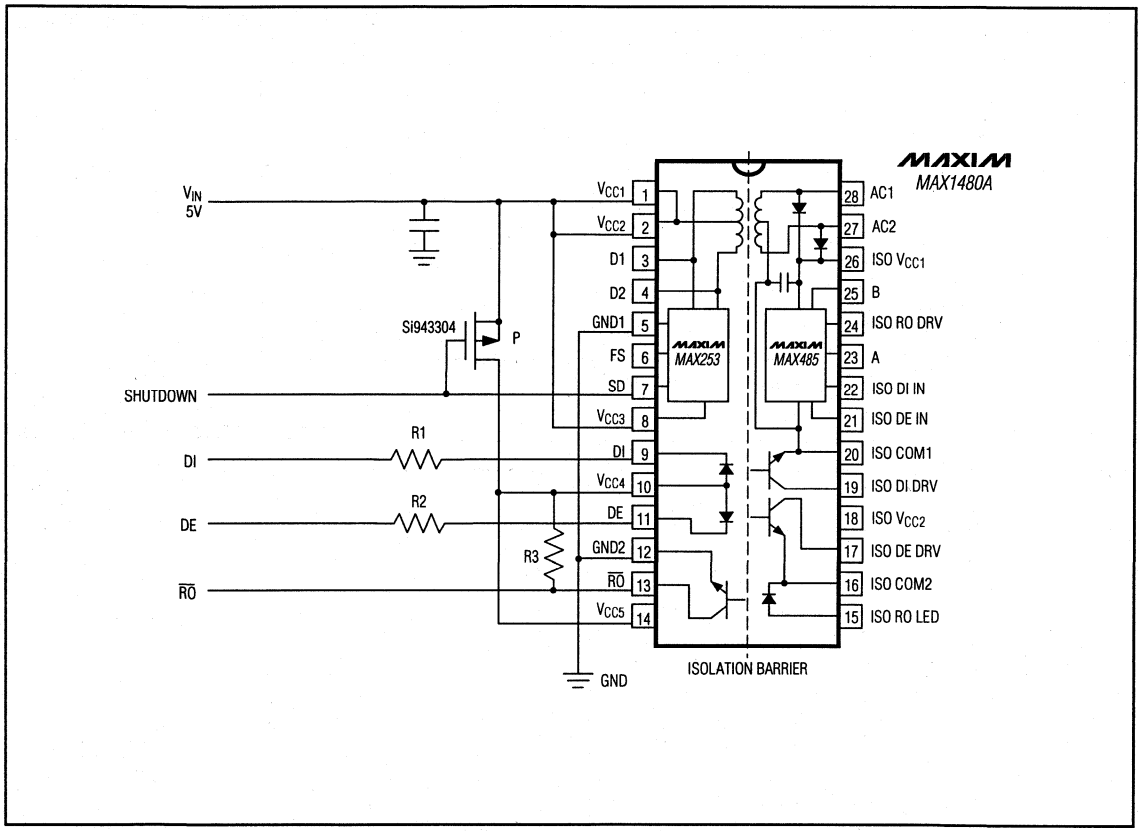


Figure 3. MAX1480A Low-Power Shutdown Mode

Test Circuits

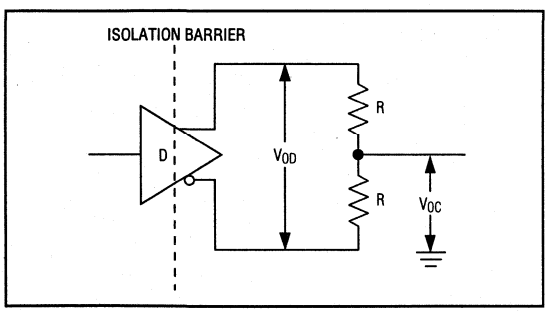


Figure 4. Driver DC Test Load

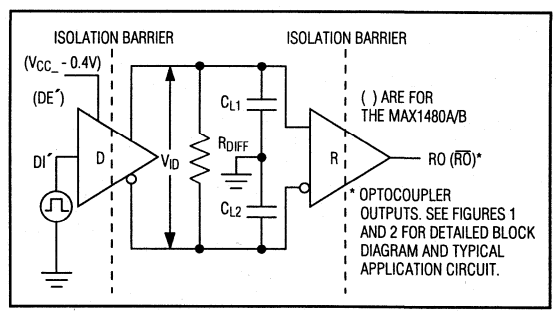


Figure 5. Driver/Receiver Timing Test Circuit

Complete, Isolated, RS-485/RS-422 Data Interface

Test Circuits (continued)

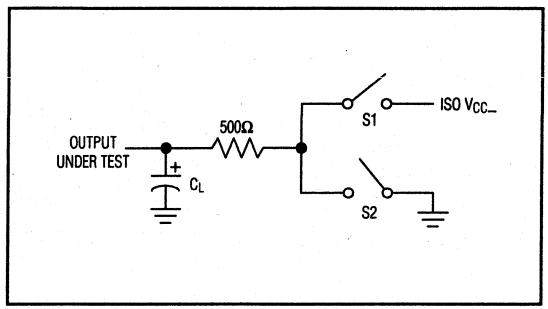


Figure 6. Driver Timing Test Load

Switching Waveforms

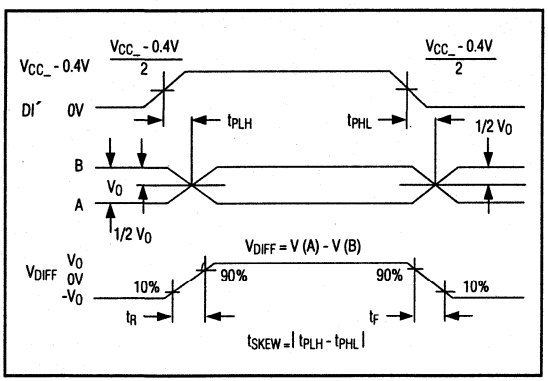


Figure 7. Driver Propagation Delays and Transition Times

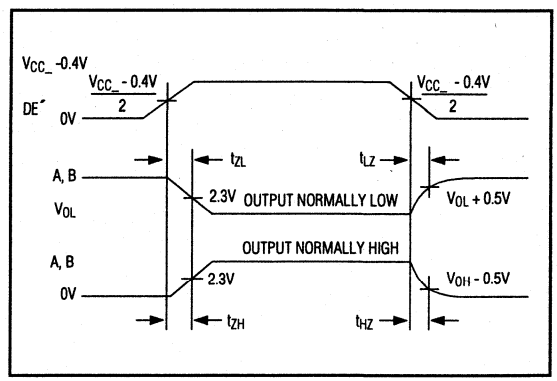


Figure 8. Driver Enable and Disable Times

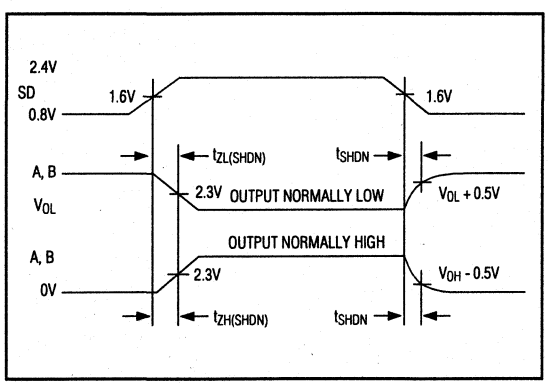


Figure 9. Times to/from Shutdown

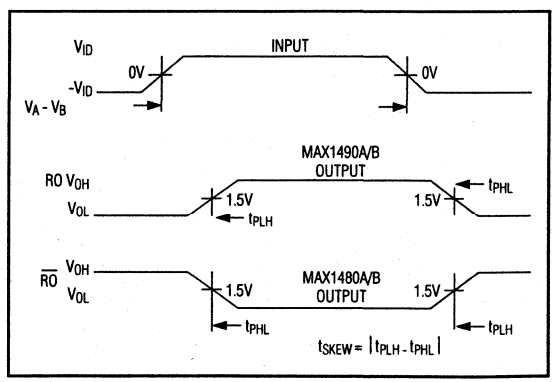


Figure 10. Receiver Propagation Delays

MAX1480B/MAX1490B: Reduced EMI and Reflections

The MAX1480B/MAX1490B are slew-rate-limited, minimizing EMI and reducing reflections caused by improperly terminated cables. Figure 11 shows both the driver output waveform of a MAX1480A/MAX1490A transmitting a 150kHz signal and the Fourier analysis of that waveform. High-frequency harmonics with large amplitudes are evident. Figure 12 shows the same information for the slew-rate-limited MAX1480B/MAX1490B transmitting the same signal. The high-frequency harmonics have much lower amplitudes, and therefore the potential for EMI is significantly reduced.

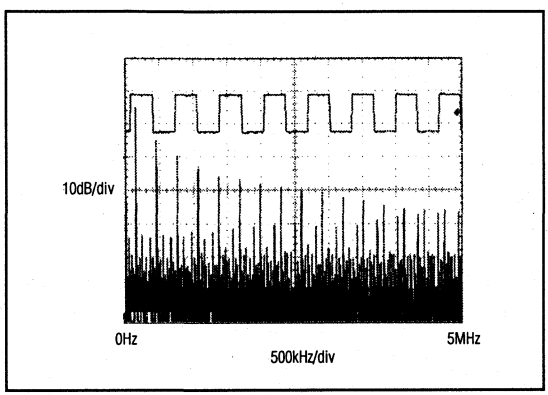


Figure 11. Driver Output Waveform and FFT Plot of MAX1480A/MAX1490A Transmitting a 150kHz Signal

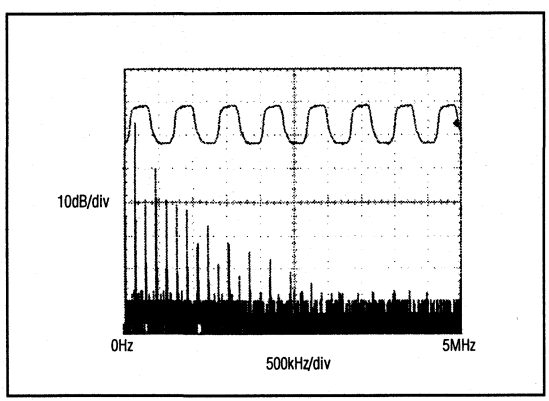


Figure 12. Driver Output Waveform and FFT Plot of MAX1480B/MAX1490B Transmitting a 150kHz Signal

Function Tables

Half-Duplex Devices (MAX1480A/MAX1480B)

Table 3. Transmitting

INPUTS*		OUTPUTS	
DE´	DI´	B	A
1	1	0	1
1	0	1	0
0	X	High-Z	High-Z

X = Don't care
High-Z = High impedance

Table 4. Receiving

INPUTS*		OUTPUT ($\overline{RO}$)
DE´	V_A - V_B	
0	≥ +0.2V	0
0	≤ -0.2V	1
0	Open	0

Full-Duplex Devices (MAX1490A/MAX1490B)

Table 5. Transmitting

INPUT (DI´)*	OUTPUTS	
	Z	Y
1	0	1
0	1	0

Table 6. Receiving

INPUT* (V_A - V_B)	OUTPUT (RO)
≥ +0.2V	1
≤ -0.2V	0
Open	1

* For DE´ and DI´ pin descriptions, see *Detailed Block Diagram and Typical Application Circuit* (Figure 1 for MAX1480A/B, Figure 2 for MAX1490A/B).

Complete, Isolated, RS-485/RS-422 Data Interface

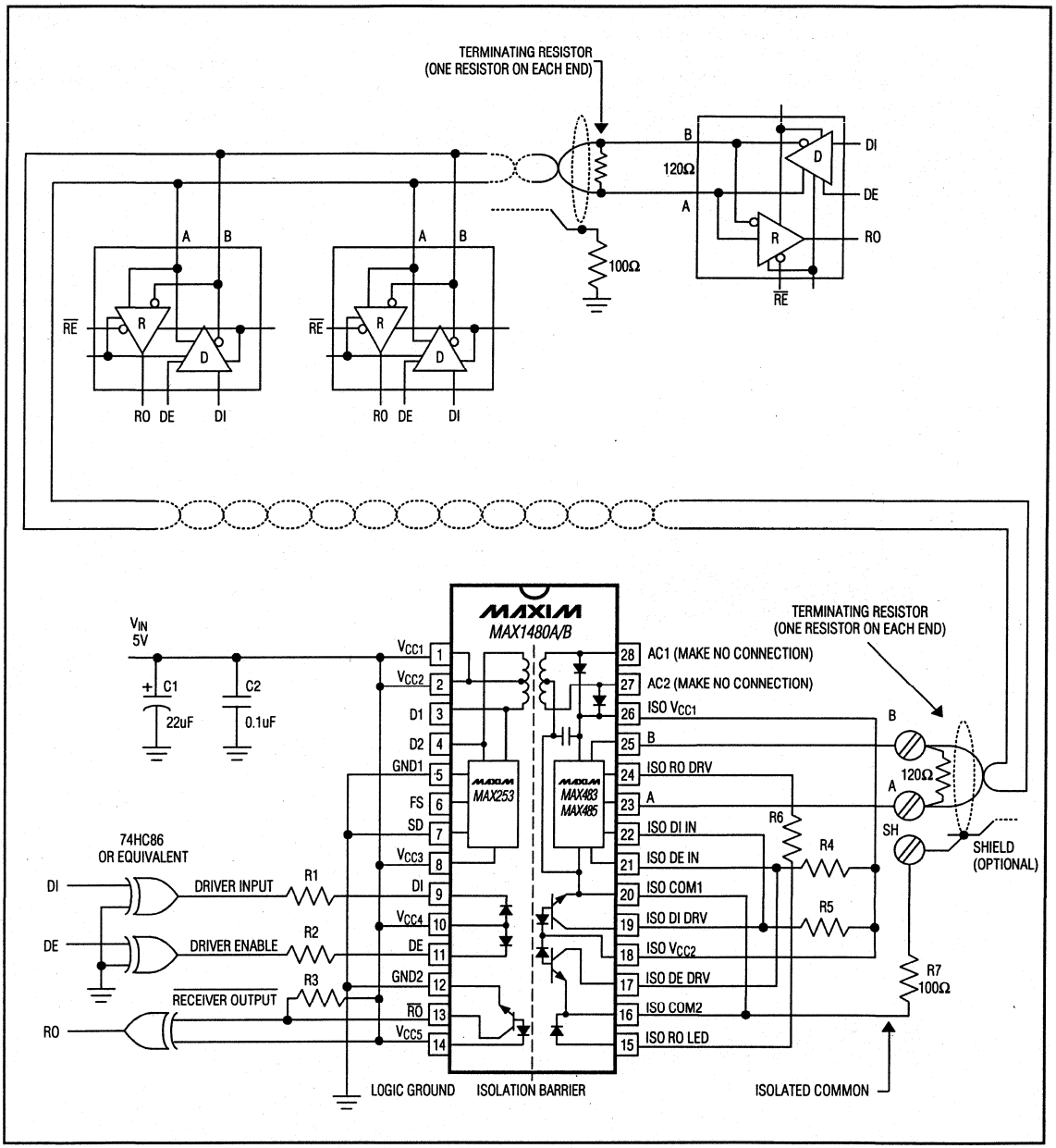


Figure 13. Typical Half-Duplex RS-485/RS-422 Network

Driver Output Protection

There are two mechanisms to prevent excessive output current and power dissipation caused by faults or by bus contention. A foldback current limit on the output stage provides immediate protection against short circuits over the entire common-mode range (see *Typical Operating Characteristics*). In addition, a thermal shutdown circuit forces the driver outputs into a high-impedance state if the die temperature rises excessively.

Propagation Delay Skew

Typical propagation delays are shown in the *Typical Operating Characteristics* using the test circuit of Figure 5. Propagation delay skew is simply the difference between the low-to-high and high-to-low propagation delay. Small driver/receiver skew times help reduce EMI and reflections by maintaining balanced differential signals.

The receiver skew time, $|t_{PLH} - t_{PHL}|$, is typically under 100ns for the MAX1480A/MAX1490A and under 1µs for the MAX1480B/MAX1490B.

The driver skew time is typically 25ns for the MAX1480A/MAX1490A and 100ns for the MAX1480B/MAX1490B.

Applications Information

DI and DE are intended to be driven through a series current-limiting resistor. Directly grounding these pins destroys the device.

The MAX1480A/MAX1480B are designed for bidirectional data communications on multipoint bus-transmission lines. The MAX1490A/MAX1490B are designed for full-duplex bidirectional communications that are primarily point-to-point. Figures 13 and 14 show half-duplex and full-duplex typical network application circuits, respectively. To minimize reflections, terminate the line at both ends with its characteristic impedance, and keep stub lengths off the main line as short as possible. The slew-rate-limited MAX1480B/MAX1490B are more tolerant of imperfect termination and stubs off the main line.

Layout Considerations

The MAX1480A/MAX1480B/MAX1490A/MAX1490B pinouts enable optimal PC board layout by minimizing interconnect lengths and crossovers.

- For maximum isolation, the "isolation barrier" should not be breached except by the MAX1480A/MAX1480B/MAX1490A/MAX1490B. Connections

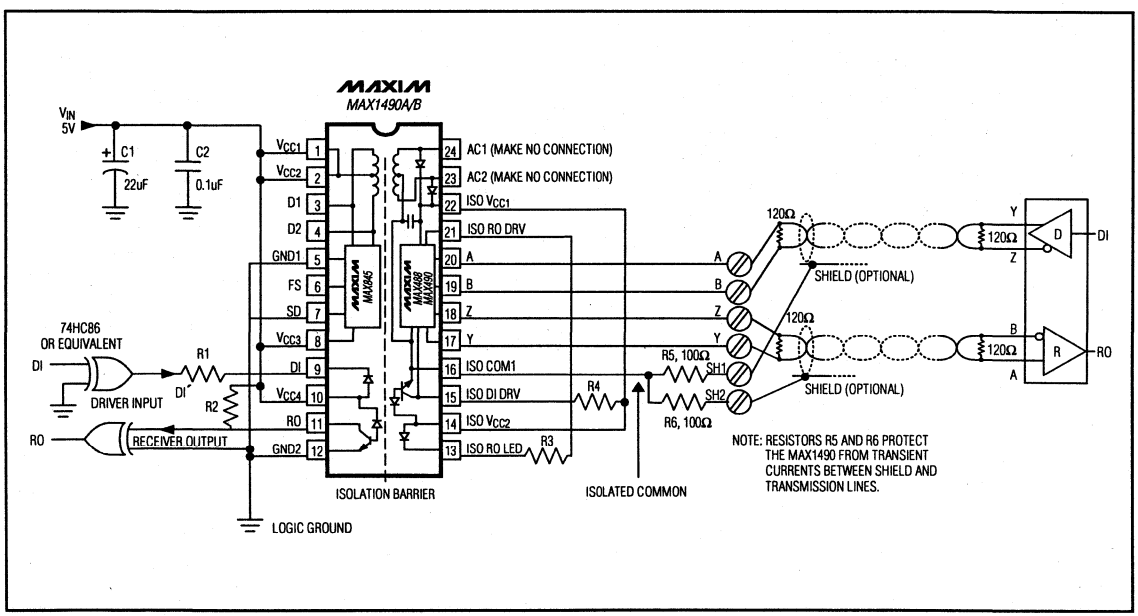


Figure 14. Typical Full-Duplex RS-485/RS-422 Network

Complete, Isolated, RS-485/RS-422 Data Interface

and components from one side should not be located near those of the other side.

- A shield trace connected to the ground on each side of the barrier can help intercept capacitive currents that might otherwise couple into the signal path. In a double-sided or multilayer board, these shield traces should be present on all conductor layers.
- Try to maximize the width of the isolation barrier wherever possible; a clear space of at least 0.25 inches between ground and isolated common is suggested.

Pull-Up and LED Drive Resistors

The MAX1480A/MAX1480B/MAX1490A/MAX1490B are specified and characterized using the resistor values shown in Table 1 of Figure 1 and Table 2 of Figure 2. Altering the recommended values can degrade performance.

The DI and DE (MAX1480A/B only) inputs are the cathodes of LEDs whose anodes are connected to the supply. These points are best driven by a CMOS-logic gate with a series resistor to limit the current. The resistor values shown in Tables 1 and 2 are recommended when the 74HC86 gate or equivalent is used. These values may need to be adjusted if a driving gate with dissimilar series resistance is used.

All pull-up resistors are based on optocoupler specifications in order to optimize the devices' data-transfer rates.

Isolated Common Connection

The isolated common may be completely floating with respect to the logic ground and the effective network ground. The receiver input resistors will cause the isolated common voltage to go to the mean voltage of the receiver inputs. If using shielded cable, tie the isolated common to the shield through a 100Ω resistor. In the case of the MAX1490, each shield should have its own 100Ω resistor (Figures 1, 2, 13, and 14).

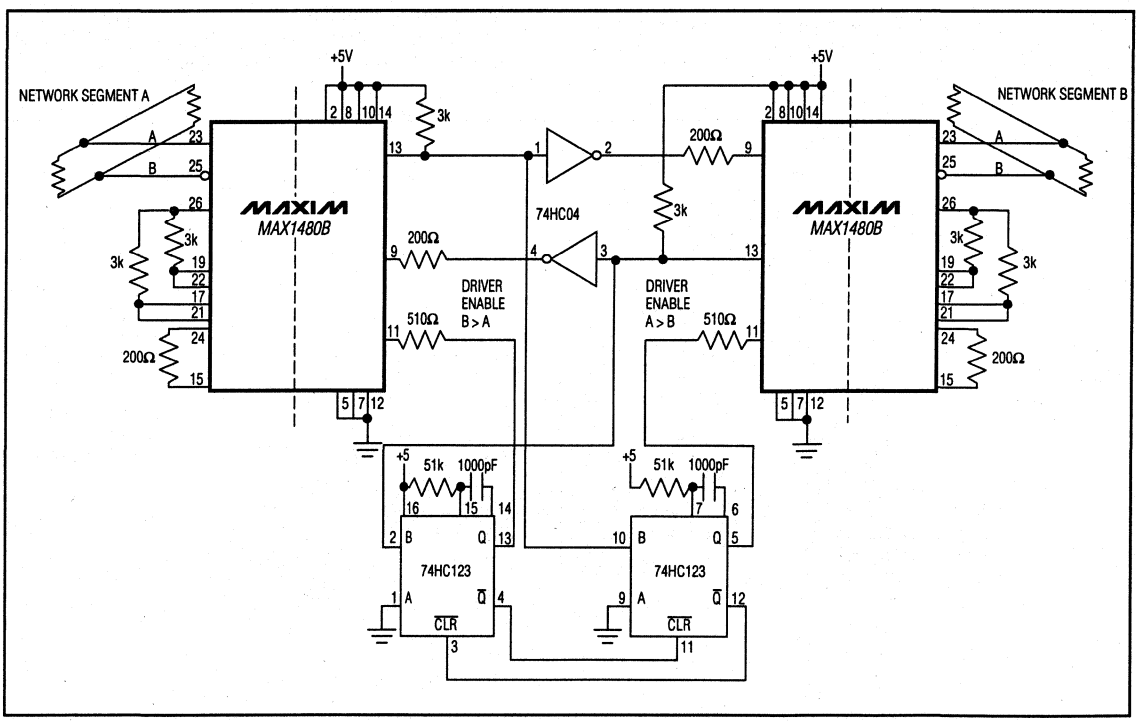


Figure 15. Doubly Isolated RS-485 Repeater

Doubly Isolated RS-485 Repeater

The RS-422/RS-485 standard is specified for cable lengths up to 4000 feet. When approaching or exceeding the specified maximum cable length, a ground-potential difference of several tens of volts can easily develop. This difference can be either DC, AC, at power-line frequency, or any imaginable noise or impulse waveform. It is typically very low impedance so that if a connection between the two grounds is attempted, very large currents may flow. These currents are by their nature unstable and unpredictable. In addition, they may cause noise to be injected into sensitive instrumentation and, in severe cases, might actually cause physical damage to such equipment.

Figure 15 shows a half-duplex (two-wire), bidirectional, party-line repeater system that prevents interference and/or damage from ground-potential differences. Two MAX1480A/MAX1480B isolated RS-485 transceivers are used to isolate each of the network segments from the electrical environment of the repeater. The MAX1480A/MAX1480B also regenerate bus signals that may have been degraded by line attenuation or dispersion.

In the idle state, both transmitters are disabled, while all receivers in the system are enabled. If any device on the system has information for any other device, it starts sending its data onto the bus. Each data transmission on the bus retriggers the one-shot, keeping the sending transmitter enabled until there are no more transmissions. All receivers receive all data; if this is undesirable, the protocol must allow for an address field so receivers can ignore data not directed to them.

Each node must refrain from transmitting when data already exists on the bus, and must resend data that is corrupted by the collisions that inevitably occur with a party-line system. With the repeater of Figure 15, there might be transmitters up to 8000 feet apart. That represents more than 8µs (assuming 1ns/foot of delay) in which two nodes could be transmitting simultaneously.

The circuit in Figure 15 can be used either directly as shown, with the slew-rate-limited MAX1480B, for data transfer rates up to 250kbps, or with the MAX1480A for data rates up to 2.5Mbps (see Table 1 for pull-up and LED resistor values when using the MAX1480A). If dual-port isolation is not needed, one of the MAX1480 devices can be replaced by a MAX485 for 2.5Mbps applications, or by a MAX483 for 250kbps applications.

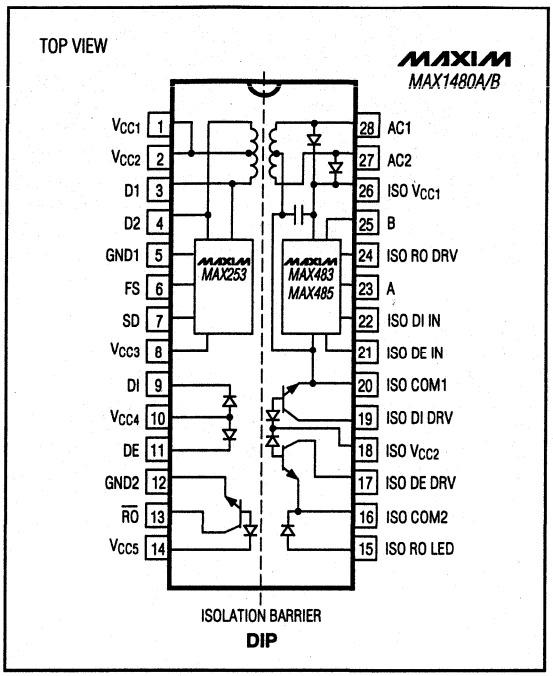
Complete, Isolated, RS-485/RS-422 Data Interface

_Ordering Information (continued)

PART†	TEMP. RANGE	PIN-PACKAGE
MAX1480BCPI	0°C to +70°C	28 Wide Plastic DIP
MAX1480BEPI	-40°C to +85°C	28 Wide Plastic DIP
MAX1490ACPG	0°C to +70°C	24 Wide Plastic DIP
MAX1490AEPG	-40°C to +85°C	24 Wide Plastic DIP
MAX1490BCPG	0°C to +70°C	24 Wide Plastic DIP
MAX1490BEPG	-40°C to +85°C	24 Wide Plastic DIP

† *Data rate for "A" parts is up to 2500kbps. Data rate for "B" parts is up to 250kbps.*

____Pin Configurations (continued)



19-2403; Rev 0; 8/95

MAXIM

±15kV ESD-Protected, Quad, Low-Power RS-232 Line Driver

General Description

The MAX1488E quad, low-power line driver is designed for EIA/TIA-232, EIA/TIA-562, and CCITT V.28 communications in harsh environments. Each transmitter output is protected against ±15kV electrostatic discharge (ESD) shocks. The inputs are TTL and CMOS compatible with minimal loading. The outputs feature internally controlled slew-rate limiting and current limiting. This device has a guaranteed 120kbps data rate. Power-supply current is less than 180µA over a ±4.5V to ±13.2V supply voltage range.

The MAX1488E is pin compatible with the MC1488, MC14C88, SN75188, SN75C188, DS1488, and DS14C88. It is available in 14-pin plastic DIP and SO packages.

Features

- **ESD Protection:**
  ±15kV—Human Body Model
  ±6kV—IEC801-2, Contact Discharge
  ±15kV—IEC801-2, Air-Gap Discharge
- **Latchup Free, Even During an ESD Event**
- **Low 85µA Supply Current from I_{EE} or I_{CC}**
- **Guaranteed 120kbps Data Rate**
- **No External Capacitors Required for Slew-Rate Limiting**
- **Pin Compatible with MC1488, MC14C88, SN75188, SN75C188, DS1488, and DS14C88**

Applications

PC Motherboards

Modems

Interface Data Terminal Equipment (DTE) with Data Circuit-Terminating Equipment (DCE)

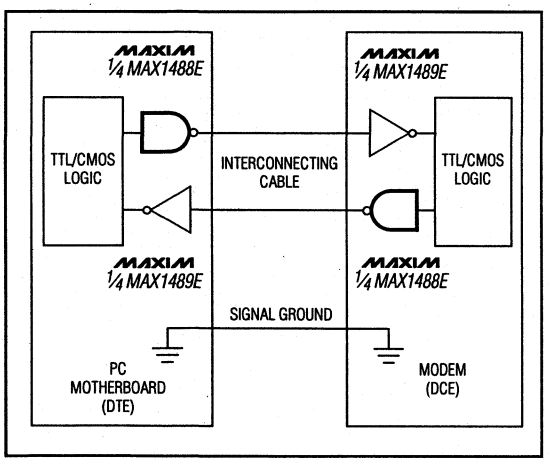
Equipment Meeting IEC1000-4-2 (formerly IEC801-2) or ±15kV ESD Protection

Ordering Information

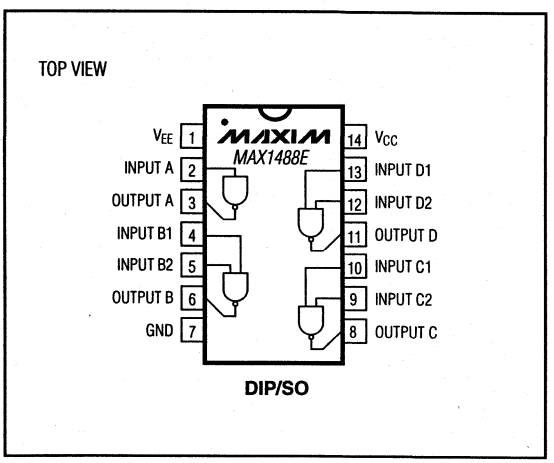
PART	TEMP. RANGE	PIN-PACKAGE
MAX1488ECPD	0°C to +70°C	14 Plastic DIP
MAX1488ECSD	0°C to +70°C	14 SO
MAX1488EC/D	0°C to +70°C	Dice*
MAX1488EEPD	-40°C to +85°C	14 Plastic DIP
MAX1488EESD	-40°C to +85°C	14 SO

** Dice are specified at T_A = +25°C.*

Typical Operating Circuit



Pin Configuration



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

±15kV ESD-Protected, Quad, Low-Power RS-232 Line Driver

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (V_{CC}) ..... +14V
Negative Supply Voltage (V_{EE}) ..... -14V
Input Voltage (V_{IN}) ..... -0.3V to +15V
Driver Output Voltage ..... ±15V
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 10.00mW/°C above +70°C) 800mW
SO (derate 8.7mW/°C above +70°C) 695mW

Operating Temperature Ranges
MAX1488EC_D ..... 0°C to +70°C
MAX1488EE_D ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.5V to 13.2V, V_{EE} = -4.5V to -13.2V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Output Voltage High	V_{OH}	V_{CC} = -V_{EE} = 5.0V, R_L = 3kΩ	3.7	4.0		V
		V_{CC} = -V_{EE} = 6.5V, R_L = 3kΩ	5	5.4		
		V_{CC} = -V_{EE} = 12.0V, R_L = 3kΩ	10	10.5		
		V_{CC} = -V_{EE} = 13.2V, R_L = open			13.2	
Output Voltage Low	V_{OL}	V_{CC} = -V_{EE} = 5.0V, R_L = 3kΩ		-4.5	-3.7	V
		V_{CC} = -V_{EE} = 6.5V, R_L = 3kΩ		-5.8	-5	
		V_{CC} = -V_{EE} = 12.0V, R_L = 3kΩ		-10.8	-10	
		V_{CC} = -V_{EE} = 13.2V, R_L = open	-13.2			
Operating Voltage Range	V_{CC}		4.5		13.2	V
	V_{EE}		-13.2		-4.5	
Positive Supply Current	I_{CC}	No load		85	180	µA
Negative Supply Current	I_{EE}	No load	-180	-85		µA
Output Short-Circuit Current	I_{OS}	Output shorted to ground (Note 1)	±4	±20	±45	mA
Input High Voltage	V_{IH}		2.0			V
Input Low Voltage	V_{IL}				0.8	V
Input Current	I_{IN1}			0	±2	µA
Output Resistance	R_O	V_{CC} = V_{EE} = 0V $\lvert V_O \rvert \le$ 2.0V		300		Ω
TIMING CHARACTERISTICS (see Figure 1)						
Output Propagation Delay, Low to High	t_{PLH}	V_{CC} = 4.5V, V_{EE} = -4.5V, C_L = 50pF		2.4	3.5	µs
		V_{CC} = 9.0V, V_{EE} = -9.0V, C_L = 50pF		2.8	3.9	
		V_{CC} = 12.0V, V_{EE} = -12.0V, C_L = 50pF		3.1	4.2	
Output Propagation Delay, High to Low	t_{PHL}	V_{CC} = 4.5V, V_{EE} = -4.5V, C_L = 50pF		2.1	4.5	µs
		V_{CC} = 9.0V, V_{EE} = -9.0V, C_L = 50pF		2.4	5.1	
		V_{CC} = 12.0V, V_{EE} = -12.0V, C_L = 50pF		2.6	5.4	
Propagation Delay Skew, $\lvert t_{PLH} - t_{PHL} \rvert$	t_{SK}	V_{CC} = 4.5V, V_{EE} = -4.5V, C_L = 50pF		0.25		µs
		V_{CC} = 9.0V, V_{EE} = -9.0V, C_L = 50pF		0.42		
		V_{CC} = 12.0V, V_{EE} = -12.0V, C_L = 50pF		0.42		
ESD CHARACTERISTICS						
ESD Protection		Human Body Model		±15		kV
		IEC-1000-4-2 (Contact Discharge)		±6		
		IEC-1000-4-2 (Air-Gap Discharge)		±15		

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4.5V to 13.2V, V_{EE} = -4.5V to -13.2V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

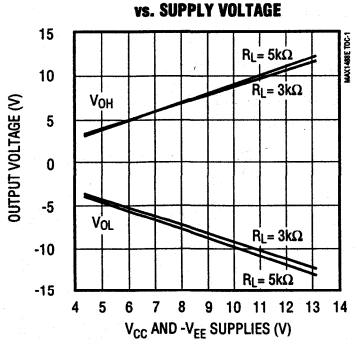
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Rise Time	t_{R1}	C_L = 1500pF, R_L = 5kΩ, $V_{OUTPUT_}$ from -3.3V to 3.3V		850		ns
	t_{R2}	C_L = 1500pF, R_L = 5kΩ, $V_{OUTPUT_}$ from -3.0V to 3.0V		740		
Output Fall Time	t_{F1}	C_L = 1500pF, R_L = 5kΩ, $V_{OUTPUT_}$ from -3.3V to 3.3V		860		ns
	t_{F2}	C_L = 1500pF, R_L = 5kΩ, $V_{OUTPUT_}$ from -3.0V to 3.0V		765		
Output Slew Rate	SR	C_L = 15pF to 2500pF, R_L = 3kΩ to 7kΩ, V_{CC} = 12V, V_{EE} = -12V, T_A = +25°C, $V_{OUTPUT_}$ from -3.0V to 3.0V	4		30	V/µs
Guaranteed Data Rate		C_L = 15pF to 2500pF, R_L = 3kΩ to 7kΩ, V_{CC} = 12V, V_{EE} = -12V, T_A = +25°C	120			kbps

Note 1: The I_{OS} value is for one output at a time. If more than one output is shorted simultaneously, damage may occur.

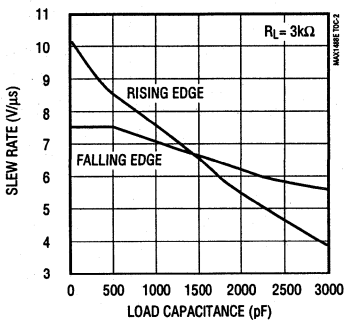
Typical Operating Characteristics

(V_{CC} = 12V, V_{EE} = -12V, T_A = +25°C, unless otherwise noted.)

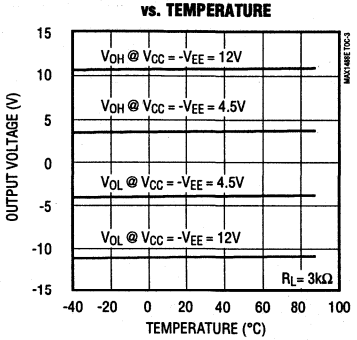
OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



SLEW RATE vs. LOAD CAPACITANCE



OUTPUT VOLTAGE vs. TEMPERATURE



±15kV ESD-Protected, Quad, Low-Power RS-232 Line Driver

Pin Description

PIN	NAME	FUNCTION
1	V_{EE}	-4.5V to -13.2V Supply Voltage Input
2, 4, 5, 9, 10, 12, 13	INPUT_	Driver Inputs
3, 6, 8, 11	OUTPUT_	Driver Outputs
7	GND	Ground
14	V_{CC}	+4.5V to +13.2V Supply Voltage Input

Detailed Description

The MAX1488E provides ±15kV of ESD protection when operating or when powered down. After an ESD event, the MAX1488E will not latch up. Internal slew-rate-limiting circuitry eliminates the need for external capacitors. The MAX1488E has a guaranteed 120kbps data rate.

Outputs

Tables 1 and 2 describe the output states. The output voltage level is affected by both the load current and supply voltage, and is stable over temperature. Refer to the *Typical Operating Characteristics* to see how the output voltage varies with supply voltage, load capacitance, and temperature.

Table 1. Driver A Functions

INPUT A	OUTPUTA
H	L
L	H

Table 2. Driver B–D Functions

INPUT_1	INPUT_2	OUTPUT_
H	H	L
L	X	H
X	L	H

Inputs

The driver inputs determine the driver output states (Tables 1 and 2). Driver inputs B, C, and D have two inputs. **Connect unused inputs to ground or V_{CC}.**

±15kV ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The MAX1488E driver outputs have extra protection against static electricity found in normal operation. Maxim's engineers developed state-of-the-art structures to protect these pins against ESD of ±15kV, without damage. After an ESD event, the MAX1488E keeps working without latchup.

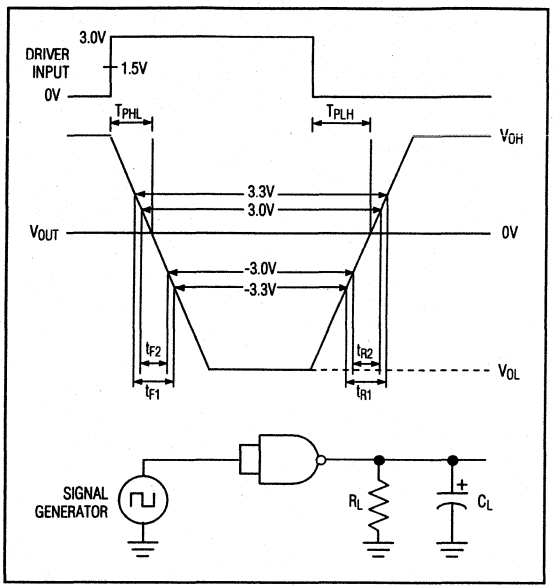


Figure 1. Slew-Rate Test Circuit and Timing Diagram

ESD protection can be tested in various ways; the transmitter outputs are characterized for protection to the following:

1) ±15kV using the Human Body Model
2) ±6kV using the Contact-Discharge Method specified in IEC1000-4-2 (formerly IEC801-2)
3) ±15kV using the Air-Gap Method specified in IEC1000-4-2 (formerly IEC801-2).

ESD Test Conditions

ESD performance depends on a number of conditions. Contact Maxim for a reliability report that documents test setup, methodology, and results.

Human Body Model

Figure 2a shows the Human Body Model, and Figure 2b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

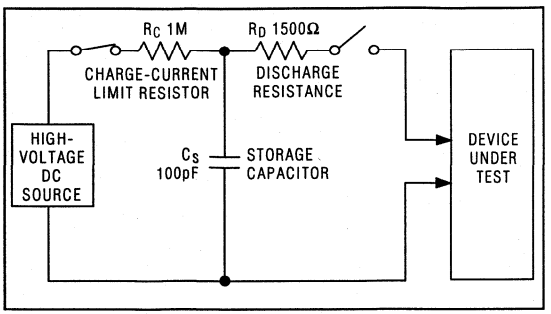


Figure 2a. Human Body ESD Test Model

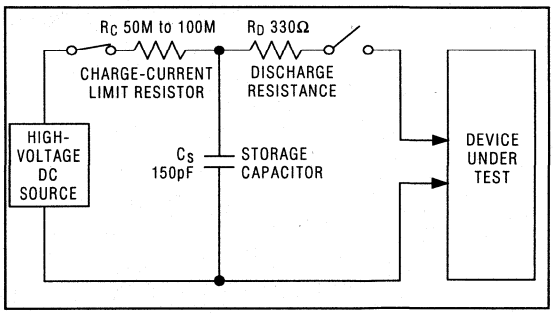


Figure 3a. IEC1000-4-2 ESD Test Model

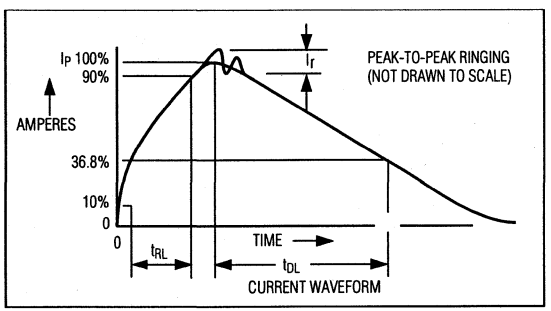


Figure 2b. Human Body Model Current Waveform

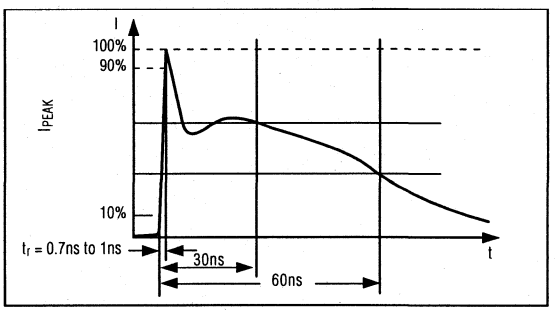


Figure 3b. IEC1000-4-2 ESD Generator Current Waveform

IEC1000-4-2

The IEC1000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits. The MAX1488E helps you design equipment that meets Level 4 (the highest level) of IEC1000-4-2, without additional ESD-protection components.

The major difference between tests done using the Human Body Model and IEC1000-4-2 is higher peak current in IEC1000-4-2. Because series resistance is lower in the IEC1000-4-2 ESD test model (Figure 3a), the ESD withstand voltage measured to this standard is generally lower than that measured using the Human Body Model. Figure 3b shows the current waveform for the ±6kV IEC1000-4-2 Level 4 ESD Contact-Discharge test.

The Air-Gap test involves approaching the device with a charged probe. The Contact-Discharge method connects the probe to the device before the probe is energized.

Machine Model

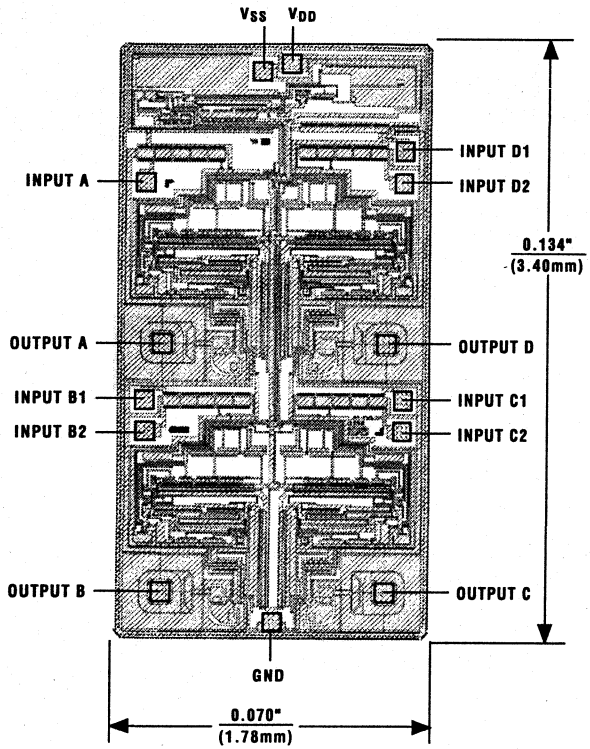
The Machine Model for ESD testing uses a 200pF storage capacitor and zero-discharge resistance. Its objective is to mimic the stress caused by contact that occurs with handling and assembly during manufacturing. Of course, all pins (not just RS-232 inputs and outputs) require this protection during manufacturing. Therefore, the Machine Model is less relevant to the I/O ports than the Human Body Model and IEC1000-4-2.

Applications Information

Use proper layout to ensure other devices on your board are not damaged in an ESD strike. Currents as high as 60A can instantaneously pass into the ground, so it is important to minimize the ground-lead return path to the power supply. A separate return path to the power supply is recommended. Trace widths should be greater than 40 mils. V_{CC} and V_{EE} must be bypassed with 0.1µF capacitors as close to the part as possible to ensure maximum ESD protection.

±15kV ESD-Protected, Quad, Low-Power RS-232 Line Driver

Chip Topography



TRANSISTOR COUNT: 95
SUBSTRATE CONNECTED TO GND

19-0426; Rev 0; 8/95

MAXIM

±15kV ESD-Protected, Quad, Low-Power RS-232 Line Receiver

General Description

The MAX1489E quad, low-power line receiver is designed for EIA/TIA-232, EIA/TIA-562, and CCITT V.28 communications in harsh environments. Each receiver input is protected against ±15kV electrostatic discharge (ESD) shocks. These inputs have a ±25V range and feature hysteresis and time-domain filtering. The outputs are TTL and CMOS compatible. The MAX1489E has a 120kbps guaranteed data rate. Supply current is typically 350µA.

The MAX1489E is pin compatible with the MC1489, MC14C89, SN75189, SN75C189, DS1489, and DS14C89. It is available in 14-pin plastic DIP and SO packages.

Applications

PC Motherboards

Modems

Interfacing Data Terminal Equipment (DTE) with Data Circuit-Terminating Equipment (DCE)

Equipment Meeting IEC1000-4-2 (formerly IEC801-2) or ±15kV ESD Protection

Features

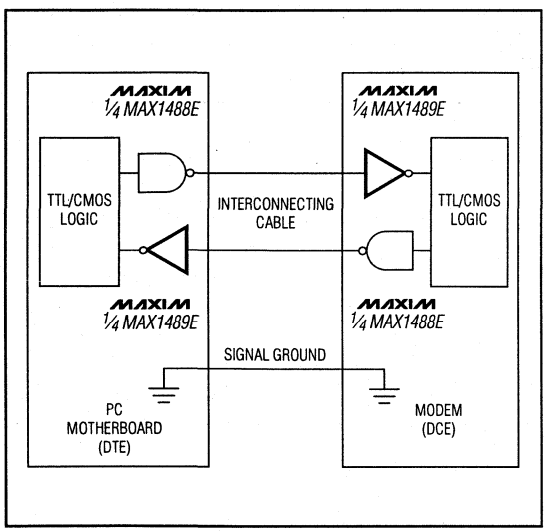
- **Enhanced ESD Protection:**
  ±15kV—Human Body Model
  ±8kV—IEC1000-4-2, Contact Discharge
  ±15kV—IEC1000-4-2, Air-Gap Discharge
- **Latchup Free During an ESD Event**
- **Low 350µA Supply Current**
- **Input Hysteresis and Time-Domain Filtering Eliminate the Need for External Filtering**
- **Stable Input Thresholds**
- **Pin Compatible with MC1489, MC14C89, SN75189, SN75C189, DS1489, and DS14C89**

Ordering Information

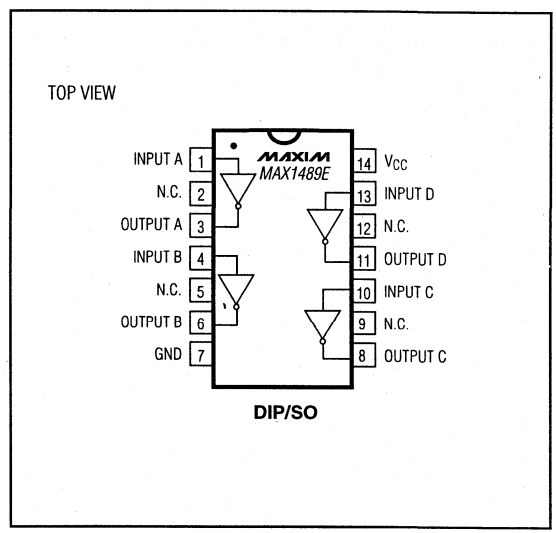
PART	TEMP. RANGE	PIN-PACKAGE
MAX1489ECPD	0°C to +70°C	14 Plastic DIP
MAX1489ECSD	0°C to +70°C	14 SO
MAX1489EC/D	0°C to +70°C	Dice*
MAX1489EEPD	-40°C to +85°C	14 Plastic DIP
MAX1489EESD	-40°C to +85°C	14 SO

** Dice are specified at T_A = +25°C.*

Typical Operating Circuit



Pin Configuration



DIP/SO

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

±15kV ESD-Protected, Quad, Low-Power RS-232 Line Receiver

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) ..... +7V
Input Voltage (V_{IN}) ..... ±30V
Output Short-Circuit Current
(Shorted to GND or V_{CC}) (Note 1) ..... Self Limiting
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 10.00mW/°C above +70°C) 800mW
SO (derate 8.7mW/°C above +70°C) 695mW

Operating Temperature Ranges
MAX1489EC_D ..... 0°C to +70°C
MAX1489EE_D ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = 5V, T_A = +25°C.)

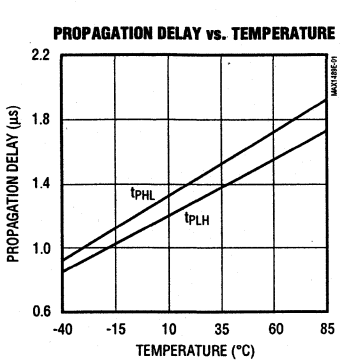
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS							
Output Voltage High	V_{OH}	$V_{IN} \le 0.4V$	I_{OUT} = -3.2mA	3.5	4.99		V
			I_{OUT} = -20µA	2.5	4.41		
Output Voltage Low	V_{OL}	$V_{IN} \ge 2.4V$, I_{OUT} = 3.2mA			0.17	0.4	V
Output Short-Circuit Current (Note 1)	I_{OS}	Shorted to GND		-35			mA
		Shorted to V_{CC}				60	
Supply Current	I_{CC}				260	600	µA
Input Voltage Range	V_{IN}			-25		25	V
Input Voltage High	V_{IH}			1.60	2.17	2.60	V
Input Voltage Low	V_{IL}			0.75	1.06	1.30	V
Input Hysteresis	V_{HYST}				1.11		V
Input Resistance	R_{IN}			3.0	5.0	7.0	kΩ
TIMING CHARACTERISTICS							
Output Propagation Delay, Low to High	t_{PLH}	Figure 1		1.38		4.0	µs
Output Propagation Delay, High to Low	t_{PHL}	Figure 1		1.45		4.0	µs
Output Propagation Delay Skew, $\lvert t_{PLH} - t_{PHL} \rvert$	t_{SKEW}	Figure 1			70		ns
Output Transition Time	t_{TR}	V_{OUT} = 10% to 90%			35	120	ns
Input Noise Rejection	t_N	Pulse amplitude = 5V (Note 2)			1.0		µs
Guaranteed Data Rate	DR			120	240		kbps
ESD CHARACTERISTICS							
ESD Protection		Human Body Model			±15		kV
		IEC1000-4-2 (Contact Discharge)			±8		
		IEC1000-4-2 (Air-Gap Discharge)			±15		

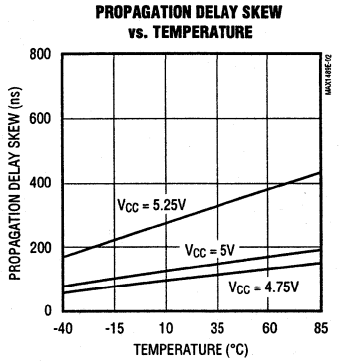
Note 1: Only one output may be shorted at a time.
Note 2: See Noise Pulse Rejection graph in *Typical Operating Characteristics* section.

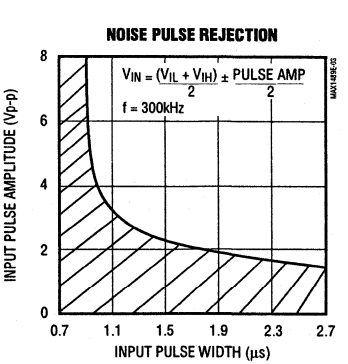
±15kV ESD-Protected, Quad, Low-Power RS-232 Line Receiver

Typical Operating Characteristics

(V_{CC} = 5V, T_A = +25°C, unless otherwise noted.)







Pin Description

PIN	NAME	FUNCTION
1, 4, 10, 13	INPUT_	Receiver Inputs
2, 5, 9, 12	N.C.	No Connect—not internally connected
3, 6, 8, 11	OUTPUT_	Receiver Outputs
7	GND	Ground
14	V_{CC}	Supply Voltage

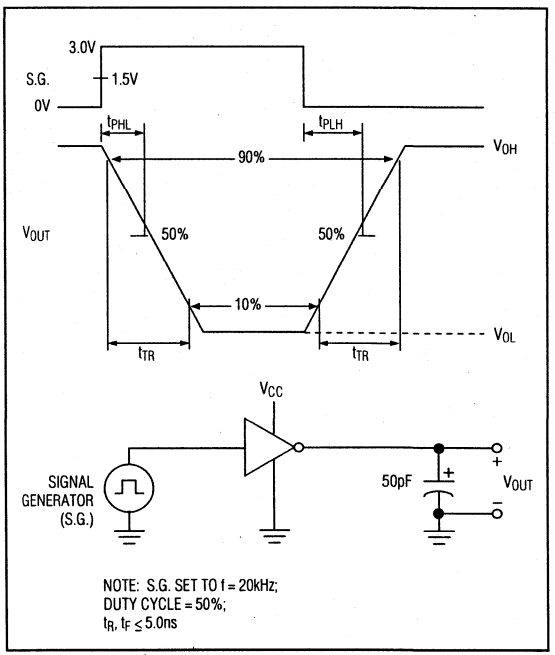


Figure 1. Timing Diagram

±15kV ESD-Protected, Quad, Low-Power RS-232 Line Receiver

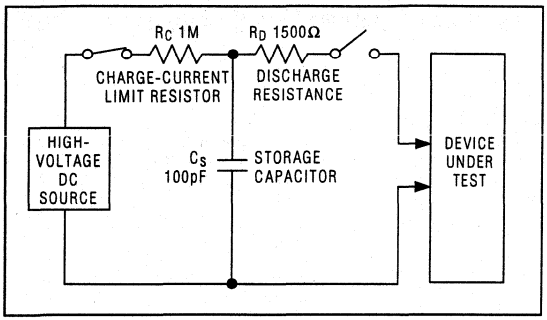


Figure 2a. Human Body ESD Test Model

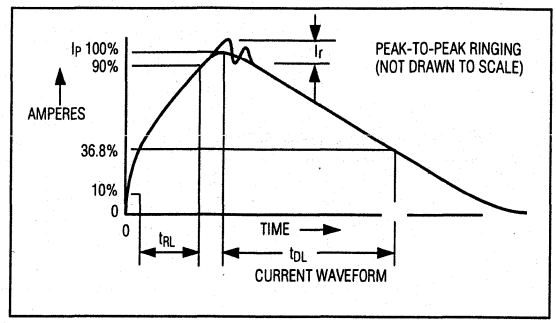


Figure 2b. Human Body Model Current Waveform

Detailed Description

±15kV ESD Protection

As with all Maxim devices, ESD protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The MAX1489E receiver inputs have extra protection against static electricity found in normal operation. Maxim's engineers developed state-of-the-art structures to protect these pins against ESD of ±15kV without damage. After an ESD event, the MAX1489E keeps working without latchup.

ESD protection can be tested in various ways; the receiver inputs are characterized for protection to the following:

1) ±15kV using the Human Body Model
2) ±8kV using the Contact Discharge method specified in IEC1000-4-2 (formerly IEC801-2)
3) ±15kV using the Air-Gap Discharge method specified in IEC1000-4-2 (formerly IEC801-2).

ESD Test Conditions

Contact Maxim for a reliability report that documents test setup, methodology, and results.

Human Body Model

Figure 2a shows the Human Body Model, and Figure 2b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

IEC1000-4-2

The IEC100-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits. The MAX1489E helps you design equipment that meets Level 4 (the highest level) of IEC1000-4-2, without additional ESD protection components.

The major difference between tests done using the Human Body Model and IEC1000-4-2 is higher peak current in IEC1000-4-2. Because series resistance is lower in the IEC1000-4-2 ESD test model (Figure 3a), the ESD withstand voltage measured to this standard is generally lower than that measured using the Human Body Model. Figure 3b shows the current waveform for the ±8kV IEC1000-4-2 Level 4 ESD Contact Discharge test.

The Air-Gap test involves approaching the device with a charged probe. The Contact Discharge method connects the probe to the device before the probe is energized.

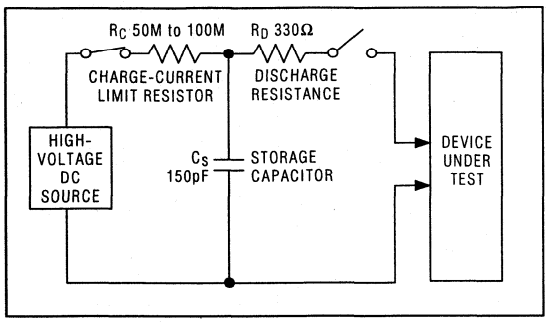


Figure 3a. IEC1000-4-2 ESD Test Model

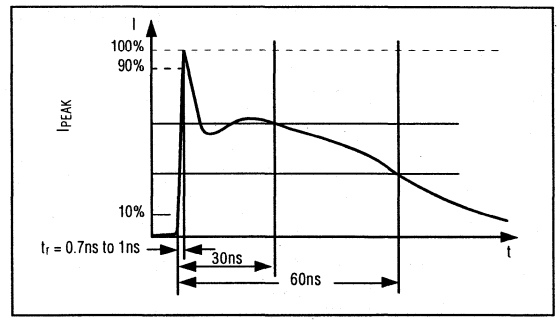


Figure 3b. IEC1000-4-2 ESD Generator Current Waveform

Machine Model

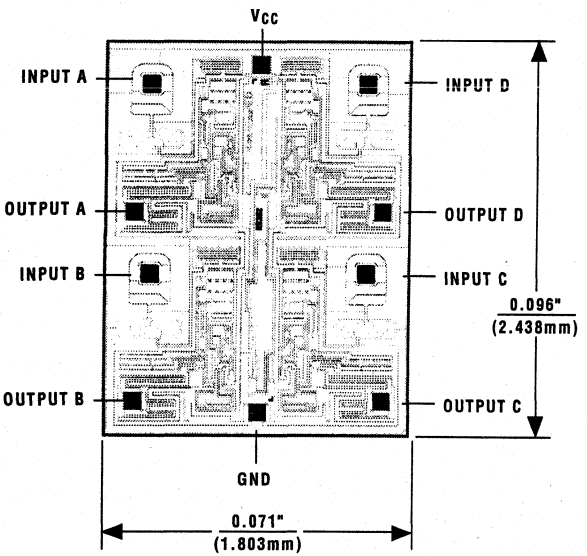
The Machine Model for ESD testing uses a 200pF storage capacitor and zero-discharge resistance. Its objective is to mimic the stress caused by contact that occurs with handling and assembly during manufacturing. Of course, all pins (not just RS-232 inputs and outputs) require this protection during manufacturing. Therefore, the Machine Model is less relevant to the I/O ports than the Human Body Model and IEC1000-4-2.

Applications Information

Use proper layout to ensure other devices on your board are not damaged in an ESD strike. Currents as high as 60A can instantaneously pass through the ground pin, so it is important to minimize the ground-lead return path to the power supply. A separate return path to the power supply is recommended. Trace widths should be greater than 40 mils. V_{CC} must be bypassed with 0.1µF capacitors as close to the part as possible to ensure maximum ESD protection.

±15kV ESD-Protected, Quad, Low-Power RS-232 Line Receiver

Chip Topography



TRANSISTOR COUNT: 144
SUBSTRATE CONNECTED TO GND

19-1138; Rev 0; 9/96

MAXIM

Fail-Safe, High-Speed (10Mbps), Slew-Rate-Limited RS-485/RS-422 Transceivers

General Description

The MAX3080–MAX3089 high-speed transceivers for RS-485/RS-422 communication contain one driver and one receiver. These devices feature fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted. This means that the receiver output will be a logic high if all transmitters on a terminated bus are disabled (high impedance). The MAX3080/MAX3081/MAX3082 feature reduced slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free data transmission up to 115kbps. The MAX3083/MAX3084/MAX3085 offer higher driver output slew-rate limits, allowing transmit speeds up to 500kbps. The MAX3086/MAX3087/MAX3088's driver slew rates are not limited, making transmit speeds up to 10Mbps possible. The MAX3089's slew rate is selectable between 115kbps, 500kbps, and 10Mbps by driving a selector pin with a single three-state driver.

These transceivers typically draw 375µA of supply current when unloaded, or when fully loaded with the drivers disabled.

All devices have a 1/8-unit-load receiver input impedance that allows up to 256 transceivers on the bus. The MAX3082/MAX3085/MAX3088 are intended for half-duplex communications, while the MAX3080/MAX3081/MAX3083/MAX3084/MAX3086/MAX3087 are intended for full-duplex communications. The MAX3089 is selectable between half-duplex and full-duplex operation. It also features independently programmable receiver and transmitter output phase via separate pins.

Features

- ♦ **True Fail-Safe Receiver While Maintaining EIA/TIA-485 Compatibility**
- ♦ **Enhanced Slew-Rate Limiting Facilitates Error-Free Data Transmission (MAX3080–MAX3085/MAX3089)**
- ♦ **1nA Low-Current Shutdown Mode (except MAX3081/MAX3084/MAX3087)**
- ♦ **Pin-Selectable Full/Half-Duplex Operation (MAX3089)**
- ♦ **Phase Controls to Correct for Twisted-Pair Reversal (MAX3089)**
- ♦ **Allow Up to 256 Transceivers on the Bus**

Applications

RS-422/RS-485 Communications
Level Translators
Transceivers for EMI-Sensitive Applications
Industrial-Control Local Area Networks

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3080CPD	0°C to +70°C	14 Plastic DIP
MAX3080CSD	0°C to +70°C	14 SO
MAX3080EPD	-40°C to +85°C	14 Plastic DIP
MAX3080ESD	-40°C to +85°C	14 SO

Ordering Information continued on last page.

Selection Table

Part	Half/Full Duplex	Data Rate (Mbps)	Slew Rate Limited	Low-Power Shutdown	Receiver/ Driver Enable	Quiescent Current (µA)	Transceivers On Bus	Pin Count	Industry-Standard Pinout
MAX3080	Full	0.115	Yes	Yes	Yes	375	256	14	75180
MAX3081	Full	0.115	Yes	No	No	375	256	8	75179
MAX3082	Half	0.115	Yes	Yes	Yes	375	256	8	75176
MAX3083	Full	0.5	Yes	Yes	Yes	375	256	14	75180
MAX3084	Full	0.5	Yes	No	No	375	256	8	75179
MAX3085	Half	0.5	Yes	Yes	Yes	375	256	8	75176
MAX3086	Full	10	No	Yes	Yes	375	256	14	75180
MAX3087	Full	10	No	No	No	375	256	8	75179
MAX3088	Half	10	No	Yes	Yes	375	256	8	75176
MAX3089	Selectable	Selectable	Selectable	Yes	Yes	375	256	14	75180*

**Pin compatible with 75180, with additional features implemented using pins 1, 6, 8, and 13.*

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Fail-Safe, High-Speed (10Mbps), Slew-Rate-Limited RS-485/RS-422 Transceivers

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) ..... +7V
Control Input Voltage ($\overline{RE}$, DE) ..... -0.3V to (V_{CC} + 0.3V)
Special Input Voltage
(H/$\overline{F}$, SRL, TXP, RXP) ..... -0.3V to (V_{CC} + 0.3V)
Driver Input Voltage (DI) ..... -0.3V to (V_{CC} + 0.3V)
Driver Output Voltage (A, B, Y, Z) ..... ±13V
Receiver Input Voltage (A, B) ..... ±13V
Receiver Input Voltage, Full Duplex (A, B) ..... ±25V
Receiver Output Voltage (RO) ..... -0.3V to (V_{CC} + 0.3V)

Continuous Power Dissipation
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) ... 727mW
8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
14-Pin Plastic DIP (derate 10.0mW/°C above +70°C) 800mW
14-Pin SO (derate 8.33mW/°C above +70°C) 667mW
Operating Temperature Ranges
MAX308_C_ _ ..... 0°C to +70°C
MAX308_E_ _ ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DRIVER							
Differential Driver Output (no load)	V_{OD1}	Figure 5				5	V
Differential Driver Output	V_{OD2}	Figure 5, R = 50Ω (RS-422)		2.0			V
		Figure 5, R = 27Ω (RS-485)		1.5			
Change in Magnitude of Differential Output Voltage (Note 2)	ΔV_{OD}	Figure 5, R = 50Ω or R = 27Ω				0.2	V
Driver Common-Mode Output Voltage	V_{OC}	Figure 5, R = 50Ω or R = 27Ω				3	V
Change In Magnitude of Common-Mode Voltage (Note 2)	ΔV_{OC}	Figure 5, R = 50Ω or R = 27Ω				0.2	V
Input High Voltage	V_{IH1}	DE, DI, $\overline{RE}$, H/$\overline{F}$, TXP, RXP		2.0			V
Input Low Voltage	V_{IL1}	DE, DI, $\overline{RE}$, H/$\overline{F}$, TXP, RXP				0.8	V
DI Input Hysteresis	V_{HYS}	MAX3080–MAX3085, and MAX3089 with SRL = V_{CC} or unconnected			100		mV
SRL Input Current	I_{IN1}	DE, DI, $\overline{RE}$				±2	µA
	I_{IN2}	H/$\overline{F}$, TXP, RXP, internal pull-down		10		40	
Input High Voltage	V_{IH2}	SRL		V_{CC} - 0.8			V
Input Middle Voltage	V_{IM2}	SRL (Note 3)		0.4V_{CC}		0.6V_{CC}	V
Input Low Voltage	V_{IL2}	SRL				0.8	V
SRL Input Current	I_{IN3}	SRL = V_{CC}				75	µA
		SRL = GND (Note 3)		-75			
Input Current (A and B) Full Duplex	I_{IN4}	DE = GND, V_{CC} = GND or 5.25V	V_{IN} = 12V			125	µA
			V_{IN} = -7V			-75	
Output Leakage (Y and Z) Full Duplex	I_O	DE = GND, V_{CC} = GND or 5.25V	V_{IN} = 12V			125	µA
			V_{IN} = -7V	-100			
Driver Short-Circuit Output Current (Note 4)	V_{OD1}	-7V ≤ V_{OUT} ≤ V_{CC}		-250			mA
		0V ≤ V_{OUT} ≤ 12V				250	
		0V ≤ V_{OUT} ≤ V_{CC}		±25			

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
RECEIVER							
Receiver Differential Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ 12V		-200	-125	-50	mV
Receiver Input Hysteresis	ΔV_{TH}				25		mV
Receiver Output High Voltage	V_{OH}	I_O = -4mA, V_{ID} = -50mV		V_{CC} -1.5			V
Receiver Output Low Voltage	V_{OL}	I_O = 4mA, V_{ID} = -200mV				0.4	V
Three-State Output Current at Receiver	I_{OZR}	0.4V ≤ V_O ≤ 2.4V				±1	µA
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ 12V		96			kΩ
Receiver Output Short-Circuit Current	I_{OSR}	0V ≤ V_{RO} ≤ V_{CC}		±7		±95	mA
SUPPLY CURRENT							
Supply Current	I_{CC}	No load, $\overline{RE}$ = DI = GND or V_{CC}, SRL = V_{CC}	DE = V_{CC}		430	900	µA
			DE = GND		375	600	
		No load, $\overline{RE}$ = DI = GND or V_{CC}, SRL = GND	DE = V_{CC}		475	1000	µA
			DE = GND		420	800	
Supply Current in Shutdown Mode	I_{SHDN}	DE = GND, $V_{\overline{RE}}$ = V_{CC}			0.001	10	µA

Note 1: All currents into the device are positive; all currents out of the device are negative. All voltages are referred to device ground unless otherwise noted.

Note 2: ΔV_{OD} and ΔV_{OC} are the changes in V_{OD} and V_{OC}, respectively, when the DI input changes state.

Note 3: The SRL pin is internally biased to V_{CC} / 2 by a 100kΩ/100kΩ resistor divider. It is guaranteed to be V_{CC} / 2 if left unconnected.

Note 4: Maximum current level applies to peak current just prior to foldback-current limiting; minimum current level applies during current limiting.

Fail-Safe, High-Speed (10Mbps), Slew-Rate-Limited RS-485/RS-422 Transceivers

SWITCHING CHARACTERISTICS—MAX3080–MAX3082, and MAX3089 with SRL = Unconnected

(V_{CC} = +5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Input to Output	t_{DPLH}	Figures 7 and 9, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	500	2.03	260	ns
	t_{DPHL}		500	2.03	260	
Driver Output Skew | t_{DPLH} - t_{DPHL} |	t_{DSKEW}	Figures 7 and 9, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		-3	±200	ns
Driver Rise or Fall Time	t_{DR}, t_{DF}	Figures 7 and 9, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	667	1320	2500	ns
Maximum Data Rate	f_{MAX}		115			kbps
Driver Enable to Output High	t_{DZH}	Figures 8 and 10, C_L = 100pF, S2 closed			3500	ns
Driver Enable to Output Low	t_{DZL}	Figures 8 and 10, C_L = 100pF, S1 closed			3500	ns
Driver Disable Time from Low	t_{DLZ}	Figures 8 and 10, C_L = 15pF, S1 closed			100	ns
Driver Disable Time from High	t_{DHZ}	Figures 8 and 10, C_L = 15pF, S2 closed			100	ns
Receiver Input to Output	t_{RPLH}, t_{RPHL}	Figures 11 and 13; | V_{ID} | ≥ 2.0V; rise and fall time of V_{ID} ≤ 15ns		127	200	ns
| t_{RPLH} - t_{RPHL} | Differential Receiver Skew	t_{RSKD}	Figures 11 and 13; | V_{ID} | ≥ 2.0V; rise and fall time of V_{ID} ≤ 15ns		3	±30	ns
Receiver Enable to Output Low	t_{RZL}	Figures 6 and 12, C_L = 100pF, S1 closed		20	50	ns
Receiver Enable to Output High	t_{RZH}	Figures 6 and 12, C_L = 100pF, S2 closed		20	50	ns
Receiver Disable Time from Low	t_{RLZ}	Figures 6 and 12, C_L = 100pF, S1 closed		20	50	ns
Receiver Disable Time from High	t_{RHZ}	Figures 6 and 12, C_L = 100pF, S2 closed		20	50	ns
Time to Shutdown	t_{SHDN}	(Note 5)	50	200	600	ns
Driver Enable from Shutdown to Output High	$t_{DZH(SHDN)}$	Figures 8 and 10, C_L = 15pF, S2 closed			6000	ns
Driver Enable from Shutdown to Output Low	$t_{DZL(SHDN)}$	Figures 8 and 10, C_L = 15pF, S1 closed			6000	ns
Receiver Enable from Shutdown to Output High	$t_{RZH(SHDN)}$	Figures 6 and 12, C_L = 100pF, S2 closed			3500	ns
Receiver Enable from Shutdown to Output Low	$t_{RZL(SHDN)}$	Figures 6 and 12, C_L = 100pF, S1 closed			3500	ns

SWITCHING CHARACTERISTICS—MAX3083–MAX3085, and MAX3089 with SRL = VCC

(V_{CC} = +5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V and T_A = +25°C.)

	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Input to Output	t_{DPLH}	Figures 7 and 9, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	250	720	1000	ns
	t_{DPHL}		250	720	1000	
Driver Output Skew | t_{DPLH} - t_{DPHL} |	t_{DSKEW}	Figures 7 and 9, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		-3	±100	ns
Driver Rise or Fall Time	t_{DR}, t_{DF}	Figures 7 and 9, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	200	530	750	ns
Maximum Data Rate	f_{MAX}		500			kbps
Driver Enable to Output High	t_{DZH}	Figures 8 and 10, C_L = 100pF, S2 closed			2500	ns
Driver Enable to Output Low	t_{DZL}	Figures 8 and 10, C_L = 100pF, S1 closed			2500	ns
Driver Disable Time from Low	t_{DLZ}	Figures 8 and 10, C_L = 15pF, S1 closed			100	ns
Driver Disable Time from High	t_{DHZ}	Figures 8 and 10, C_L = 15pF, S2 closed			100	ns
Receiver Input to Output	t_{RPLH}, t_{RPHL}	Figures 11 and 13; | V_{ID} | ≥ 2.0V; rise and fall time of V_{ID} ≤ 15ns		127	200	ns
| t_{RPLH} - t_{RPHL} | Differential Receiver Skew	t_{RSKD}	Figures 11 and 13; | V_{ID} | ≥ 2.0V; rise and fall time of V_{ID} ≤ 15ns		3	±30	ns
Receiver Enable to Output Low	t_{RZL}	Figures 6 and 12, C_L = 100pF, S1 closed		20	50	ns
Receiver Enable to Output High	t_{RZH}	Figures 6 and 12, C_L = 100pF, S2 closed		20	50	ns
Receiver Disable Time from Low	t_{RLZ}	Figures 6 and 12, C_L = 100pF, S1 closed		20	50	ns
Receiver Disable Time from High	t_{RHZ}	Figures 6 and 12, C_L = 100pF, S2 closed		20	50	ns
Time to Shutdown	t_{SHDN}	(Note 5)	50	200	600	ns
Driver Enable from Shutdown to Output High	$t_{DZH(SHDN)}$	Figures 8 and 10, C_L = 15pF, S2 closed			4500	ns
Driver Enable from Shutdown to Output Low	$t_{DZL(SHDN)}$	Figures 8 and 10, C_L = 15pF, S1 closed			4500	ns
Receiver Enable from Shutdown to Output High	$t_{RZH(SHDN)}$	Figures 6 and 12, C_L = 100pF, S2 closed			3500	ns
Receiver Enable from Shutdown to Output Low	$t_{RZL(SHDN)}$	Figures 6 and 12, C_L = 100pF, S1 closed			3500	ns

Fail-Safe, High-Speed (10Mbps), Slew-Rate-Limited RS-485/RS-422 Transceivers

SWITCHING CHARACTERISTICS—MAX3086–MAX3088, and MAX3089 with SRL = GND

(V_{CC} = +5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Input to Output	t_{DPLH}	Figures 7 and 9, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		34	60	ns
	t_{DPHL}			34	60	
Driver Output Skew | t_{DPLH} - t_{DPHL} |	t_{DSKEW}	Figures 7 and 9, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		-2.5	±10	ns
Driver Rise or Fall Time	t_{DR}, t_{DF}	Figures 7 and 9, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		14	25	ns
Maximum Data Rate	f_{MAX}		10			Mbps
Driver Enable to Output High	t_{DZH}	Figures 8 and 10, C_L = 100pF, S2 closed			150	ns
Driver Enable to Output Low	t_{DZL}	Figures 8 and 10, C_L = 100pF, S1 closed			150	ns
Driver Disable Time from Low	t_{DLZ}	Figures 8 and 10, C_L = 15pF, S1 closed			100	ns
Driver Disable Time from High	t_{DHZ}	Figures 8 and 10, C_L = 15pF, S2 closed			100	ns
Receiver Input to Output	t_{RPLH}, t_{RPHL}	Figures 11 and 13; | V_{ID} | ≥ 2.0V; rise and fall time of V_{ID} ≤ 15ns		106	150	ns
| t_{RPLH} - t_{RPHL} | Differential Receiver Skew	t_{RSKD}	Figures 11 and 13; | V_{ID} | ≥ 2.0V; rise and fall time of V_{ID} ≤ 15ns		0	±10	ns
Receiver Enable to Output Low	t_{RZL}	Figures 6 and 12, C_L = 100pF, S1 closed		20	50	ns
Receiver Enable to Output High	t_{RZH}	Figures 6 and 12, C_L = 100pF, S2 closed		20	50	ns
Receiver Disable Time from Low	t_{RLZ}	Figures 6 and 12, C_L = 100pF, S1 closed		20	50	ns
Receiver Disable Time from High	t_{RHZ}	Figures 6 and 12, C_L = 100pF, S2 closed		20	50	ns
Time to Shutdown	t_{SHDN}	(Note 5)	50	200	600	ns
Driver Enable from Shutdown to Output High	$t_{DZH(SHDN)}$	Figures 8 and 10, C_L = 15pF, S2 closed			250	ns
Driver Enable from Shutdown to Output Low	$t_{DZL(SHDN)}$	Figures 8 and 10, C_L = 15pF, S1 closed			250	ns
Receiver Enable from Shutdown to Output High	$t_{RZH(SHDN)}$	Figures 6 and 12, C_L = 100pF, S2 closed			3500	ns
Receiver Enable from Shutdown to Output Low	$t_{RZL(SHDN)}$	Figures 6 and 12, C_L = 100pF, S1 closed			3500	ns

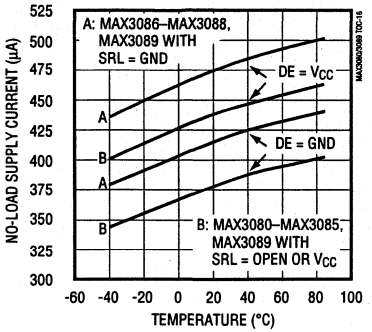
Note 5: The device is put into shutdown by bringing $\overline{RE}$ high and DE low. If the enable inputs are in this state for less than 50ns, the device is guaranteed not to enter shutdown. If the enable inputs are in this state for at least 600ns, the device is guaranteed to have entered shutdown.

Fail-Safe, High-Speed (10Mbps), Slew-Rate-Limited RS-485/RS-422 Transceivers

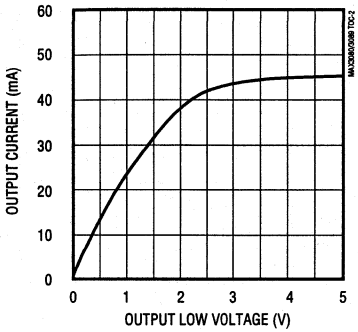
Typical Operating Characteristics

(V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

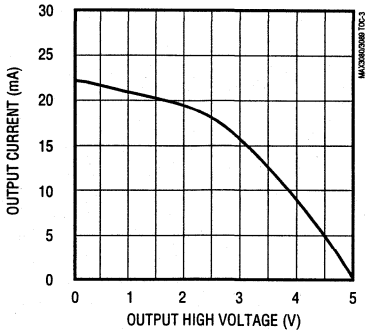
NO-LOAD SUPPLY CURRENT vs. TEMPERATURE



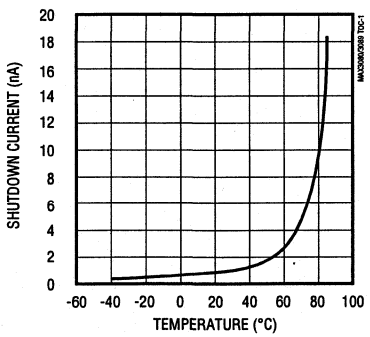
OUTPUT CURRENT vs. RECEIVER OUTPUT LOW VOLTAGE



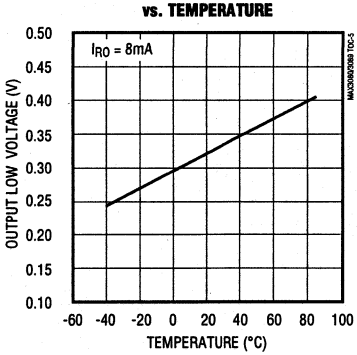
OUTPUT CURRENT vs. RECEIVER OUTPUT HIGH VOLTAGE



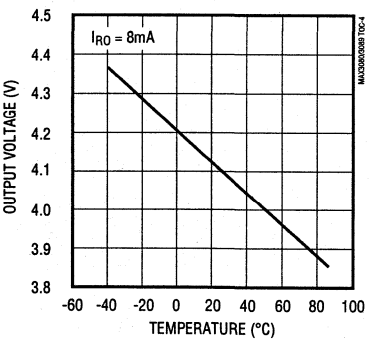
SHUTDOWN CURRENT vs. TEMPERATURE



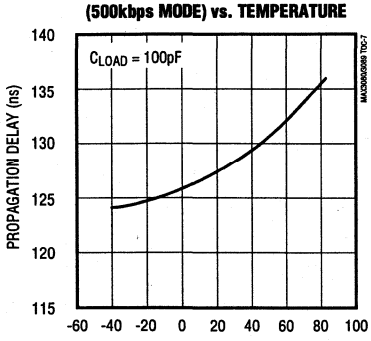
RECEIVER OUTPUT LOW VOLTAGE vs. TEMPERATURE



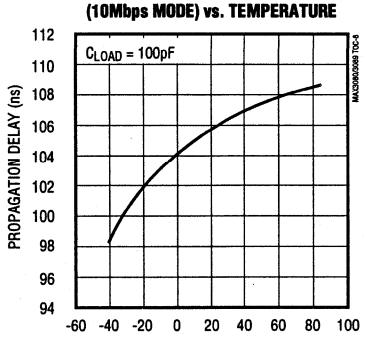
RECEIVER OUTPUT HIGH VOLTAGE vs. TEMPERATURE



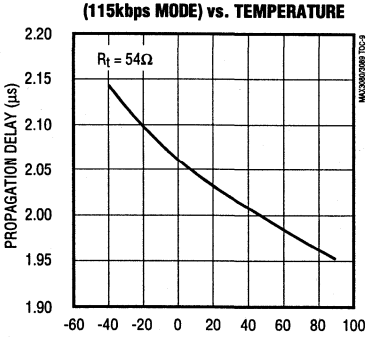
RECEIVER PROPAGATION DELAY (500kbps MODE) vs. TEMPERATURE



RECEIVER PROPAGATION DELAY (10Mbps MODE) vs. TEMPERATURE



DRIVER PROPAGATION DELAY (115kbps MODE) vs. TEMPERATURE

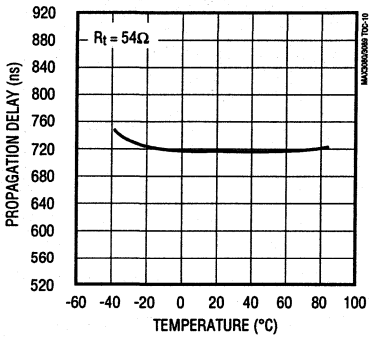


Fail-Safe, High-Speed (10Mbps), Slew-Rate-Limited RS-485/RS-422 Transceivers

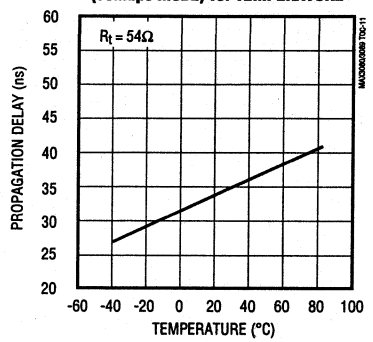
Typical Operating Characteristics (continued)

(V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

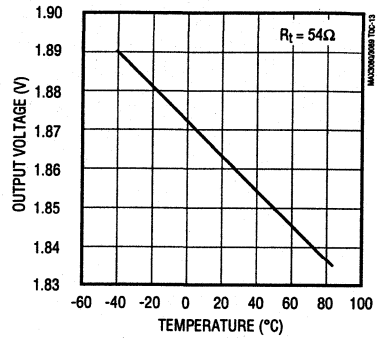
DRIVER PROPAGATION DELAY (500kbps MODE) vs. TEMPERATURE



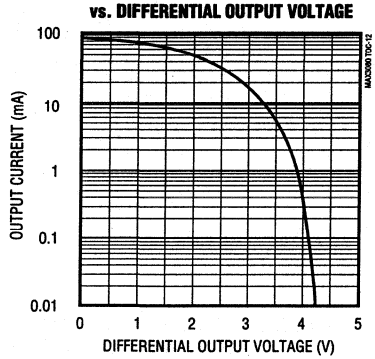
DRIVER PROPAGATION DELAY (10Mbps MODE) vs. TEMPERATURE



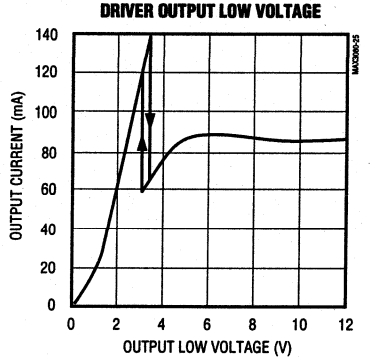
DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs. TEMPERATURE



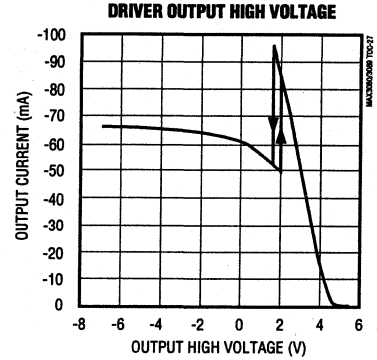
DRIVER OUTPUT CURRENT vs. DIFFERENTIAL OUTPUT VOLTAGE



OUTPUT CURRENT vs. DRIVER OUTPUT LOW VOLTAGE



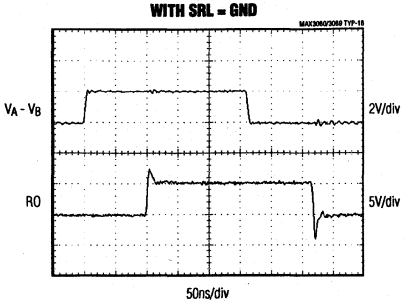
OUTPUT CURRENT vs. DRIVER OUTPUT HIGH VOLTAGE



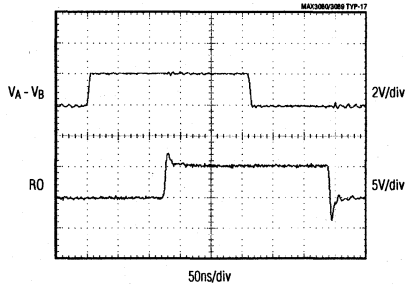
Typical Operating Characteristics (continued)

(V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

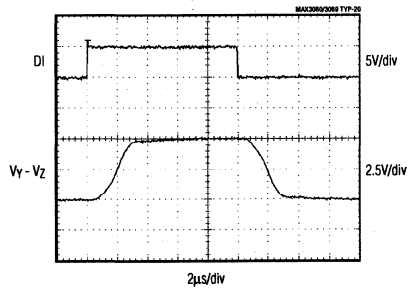
RECEIVER PROPAGATION DELAY
MAX3086–MAX3088, AND MAX3089
WITH SRL = GND



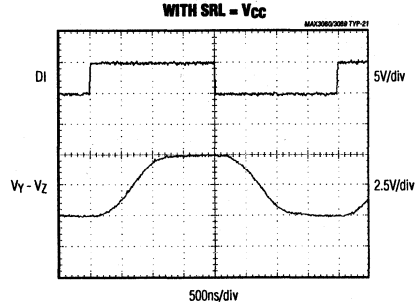
RECEIVER PROPAGATION DELAY
MAX3080–MAX3085, AND MAX3089
WITH SRL = OPEN OR V_{CC}



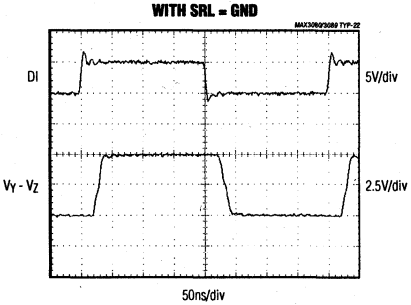
DRIVER PROPAGATION DELAY
MAX3080/MAX3081/MAX3082, AND MAX3089
WITH SRL = OPEN



DRIVER PROPAGATION DELAY
MAX3083/MAX3084/MAX3085, AND MAX3089
WITH SRL = V_{CC}



DRIVER PROPAGATION DELAY
MAX3086/MAX3087/MAX3088, AND MAX3089
WITH SRL = GND



Fail-Safe, High-Speed (10Mbps), Slew-Rate-Limited RS-485/RS-422 Transceivers

Pin Description

PIN					NAME	FUNCTION
MAX3080 MAX3083 MAX3086	MAX3081 MAX3084 MAX3087	MAX3082 MAX3085 MAX3088	MAX3089			
FULL-DUPLEX DEVICES		HALF-DUPLEX DEVICES	FULL-DUPLEX MODE	HALF-DUPLEX MODE		
—	—	—	1	1	H/$\overline{F}$	Half/Full-Duplex Selector Pin. Connect H/$\overline{F}$ to V_{CC} for half-duplex mode; connect to GND or leave unconnected for full-duplex mode.
2	2	1	2	2	RO	Receiver Output. When $\overline{RE}$ is low and if A - B ≥ -50mV, RO will be high; if A - B ≤ -200mV, RO will be low.
3	—	2	3	3	$\overline{RE}$	Receiver Output Enable. Drive $\overline{RE}$ low to enable RO; RO is high impedance when $\overline{RE}$ is high. Drive $\overline{RE}$ high and DE low to enter low-power shutdown mode.
4	—	3	4	4	DE	Driver Output Enable. Drive DE high to enable driver outputs. These outputs are high impedance when DE is low. Drive $\overline{RE}$ high and DE low to enter low-power shutdown mode.
5	3	4	5	5	DI	Driver Input. With DE high, a low on DI forces noninverting output low and inverting output high. Similarly, a high on DI forces non-inverting output high and inverting output low.
—	—	—	6	6	SRL	Slew-Rate-Limit Selector Pin. Connect SRL to GND for 10Mbps communication rate; connect to V_{CC} for 500kbps communication rate. Leave unconnected for 115kbps communication rate.
6, 7	4	5	7	7	GND	Ground
—	—	—	8	8	TXP	Transmitter Phase. Connect TXP to GND, or leave floating for normal transmitter phase/polarity. Connect to V_{CC} to invert the transmitter phase/polarity.
9	5	—	9	—	Y	Noninverting Driver Output
—	—	—	—	9	Y	Noninverting Receiver Input and Noninverting Driver Output*
10	6	—	10	—	Z	Inverting Driver Output
—	—	—	—	10	Z	Inverting Receiver Input and Inverting Driver Output*
11	7	—	11	—	B	Inverting Receiver Input
—	—	—	—	11	B	Receiver Input Resistors*
—	—	7	—	—	B	Inverting Receiver Input and Inverting Driver Output

Fail-Safe, High-Speed (10Mbps), Slew-Rate-Limited RS-485/RS-422 Transceivers

Pin Description (continued)

PIN					NAME	FUNCTION
MAX3080 MAX3083 MAX3086	MAX3081 MAX3084 MAX3087	MAX3082 MAX3085 MAX3088	MAX3089			
FULL-DUPLEX DEVICES		HALF-DUPLEX DEVICES	FULL-DUPLEX MODE	HALF-DUPLEX MODE		
12	8	—	12	—	A	Noninverting Receiver Input
—	—	—	—	12	A	Receiver Input Resistors*
—	—	6	—	—	A	Noninverting Receiver Input and Noninverting Driver Output
—	—	—	13	13	RXP	Receiver Phase. Connect RXP to GND, or leave unconnected for normal transmitter phase/polarity. Connect to V_{CC} to invert the receiver phase/polarity.
14	1	8	14	14	V_{CC}	Positive Supply; 4.75V ≤ V_{CC} ≤ 5.25V
1, 8, 13	—	—	—	—	N.C.	Not Connected. Not internally connected.

**(MAX3089 only.) In half-duplex mode, the driver outputs serve as receiver inputs. The full-duplex receiver inputs (A and B) will still have a 1/8-unit load, but are not connected to the receiver.*

Function Tables

MAX3080/MAX3083/MAX3086

TRANSMITTING				
INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	Z	Y
X	1	1	0	1
X	1	0	1	0
0	0	X	High-Z	High-Z
1	0	X	Shutdown	

RECEIVING			
INPUTS			OUTPUT
$\overline{RE}$	DE	A-B	RO
0	X	≥ -0.05V	1
0	X	≤ -0.2V	0
0	X	Open/shorted	1
1	1	X	High-Z
1	0	X	Shutdown

X = Don't care
Shutdown mode, driver and receiver outputs high impedance

MAX3081/MAX3084/MAX3087

TRANSMITTING		
INPUT	OUTPUTS	
DI	Z	Y
1	0	1
0	1	0

RECEIVING	
INPUTS	OUTPUT
A-B	RO
≥ -0.05V	1
≤ -0.2V	0
Open/shorted	1

Fail-Safe, High-Speed (10Mbps), Slew-Rate-Limited RS-485/RS-422 Transceivers

Function Tables (continued)

MAX3082/MAX3085/MAX3088

TRANSMITTING				
INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	B/Z	A/Y
X	1	1	0	1
X	1	0	1	0
0	0	X	High-Z	High-Z
1	0	X	Shutdown	

RECEIVING			
INPUTS			OUTPUT
$\overline{RE}$	DE	A-B	RO
0	X	≥ -0.05V	1
0	X	≤ -0.2V	0
0	X	Open/shorted	1
1	1	X	High-Z
1	0	X	Shutdown

MAX3089

TRANSMITTING					
INPUTS				OUTPUTS	
TXP	$\overline{RE}$	DE	DI	Z	Y
0	X	1	1	0	1
0	X	1	0	1	0
1	X	1	1	1	0
1	X	1	0	0	1
X	0	0	X	High-Z	High-Z
X	1	0	X	Shutdown	

RECEIVING						
INPUTS						OUTPUT
H/$\overline{F}$	RXP	$\overline{RE}$	DE	A-B	Y-Z	RO
0	0	0	X	≥ -0.05V	X	1
0	0	0	X	≤ -0.2V	X	0
0	1	0	X	≥ -0.05V	X	0
0	1	0	X	≤ -0.2V	X	1
1	0	0	X	X	≥ -0.05V	1
1	0	0	X	X	≤ -0.2V	0
1	1	0	X	X	≥ -0.05V	0
1	1	0	X	X	≤ -0.2V	1
0	0	0	X	Open/ shorted	X	1
1	0	0	X	X	Open/ shorted	1
0	1	0	X	Open/ shorted	X	0
1	1	0	X	X	Open/ shorted	0
X	X	1	1	X	X	High-Z
X	X	1	0	X	X	Shutdown

X = Don't care
Shutdown mode, driver and receiver outputs high impedance

Fail-Safe, High-Speed (10Mbps), Slew-Rate-Limited RS-485/RS-422 Transceivers

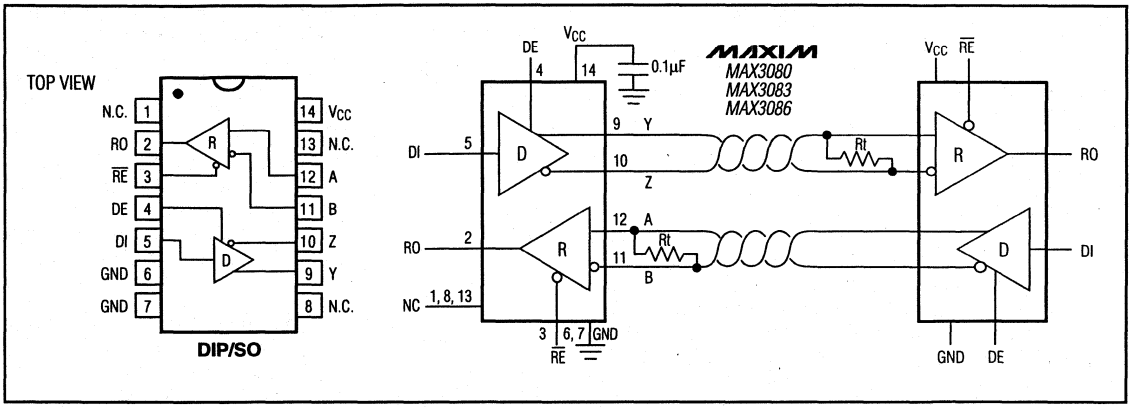


Figure 1. MAX3080/MAX3083/MAX3086 Pin Configuration and Typical Full-Duplex Operating Circuit

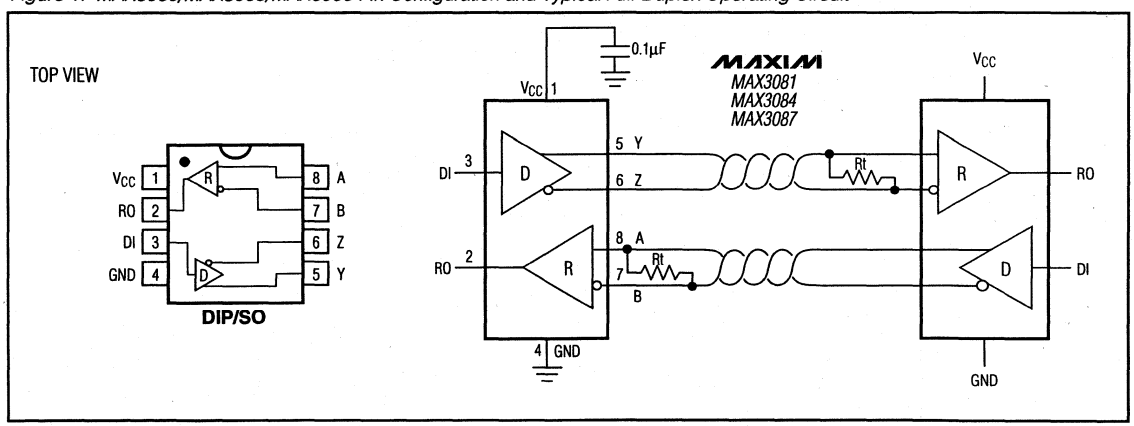


Figure 2. MAX3081/MAX3084/MAX3087 Pin Configuration and Typical Full-Duplex Operating Circuit

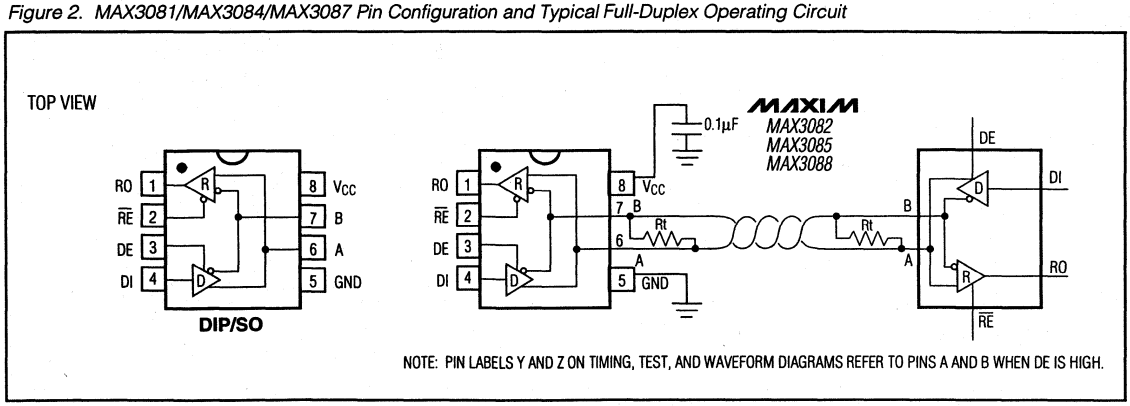


Figure 3. MAX3082/MAX3085/MAX3088 Pin Configuration and Typical Half-Duplex Operating Circuit

Fail-Safe, High-Speed (10Mbps), Slew-Rate-Limited RS-485/RS-422 Transceivers

Detailed Description

The MAX3080–MAX3089 high-speed transceivers for RS-485/RS-422 communication contain one driver and one receiver. These devices feature fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted, or when they are connected to a terminated transmission line with all drivers disabled (see *Fail-Safe* section). The MAX3080/MAX3081/MAX3082 feature reduced slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free data transmission up to 115kbps (see *Reduced EMI and Reflections* section). The MAX3083/MAX3084/MAX3085 offer higher driver output slew-rate limits, allowing transmit speeds up to 500kbps. The MAX3086/MAX3087/MAX3088's driver slew rates are not limited, making transmit speeds up to 10Mbps possible. The MAX3089's slew rate is selectable between 115kbps, 500kbps, and 10Mbps by driving a selector pin with a three-state driver.

The MAX3082/MAX3085/MAX3088 are half-duplex transceivers, while the MAX3080/MAX3081/MAX3083/MAX3084/MAX3086/MAX3087 are full-duplex transceivers. The MAX3089 is selectable between half- and full-duplex communication by driving a selector pin high or low, respectively.

All of these parts operate from a single +5V supply. Drivers are output short-circuit current limited. Thermal shutdown circuitry protects drivers against excessive power dissipation. When activated, the thermal shutdown circuitry places the driver outputs into a high-impedance state.

Receiver Input Filtering

The receivers of the MAX3080–MAX3085, and the MAX3089 when operating in 115kbps or 500kbps mode, incorporate input filtering in addition to input hysteresis. This filtering enhances noise immunity with differential signals that have very slow rise and fall times. Receiver propagation delay increases by 20% due to this filtering.

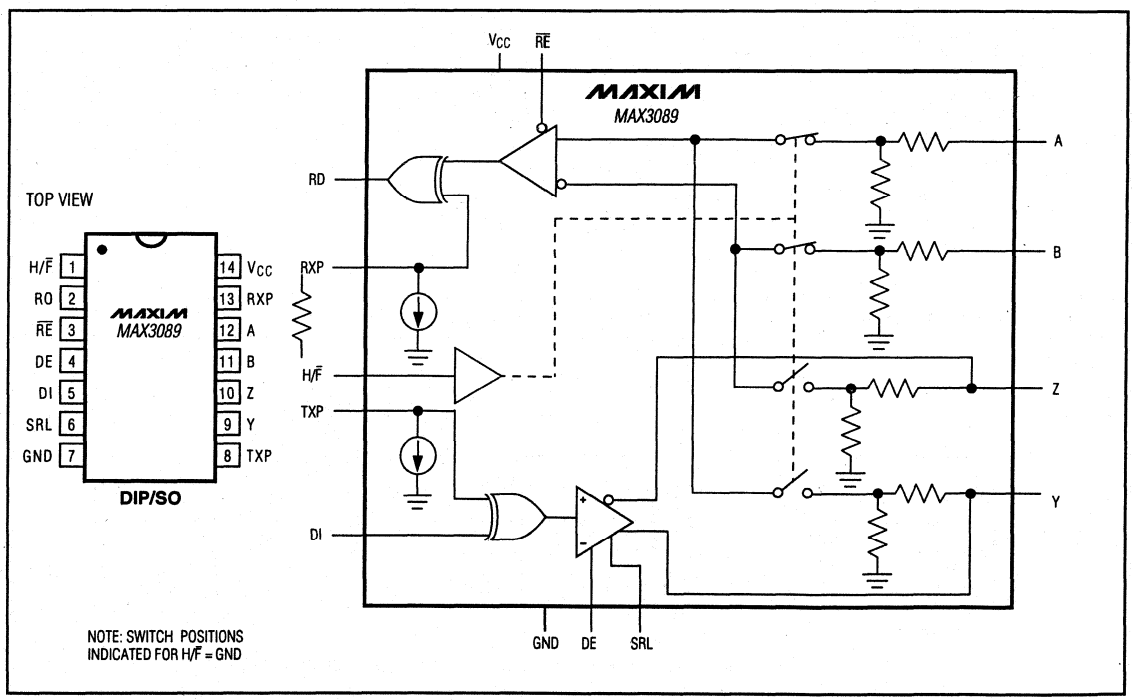


Figure 4. MAX3080/MAX3089 Pin Configuration and Functional Diagram

Fail-Safe, High-Speed (10Mbps), Slew-Rate-Limited RS-485/RS-422 Transceivers

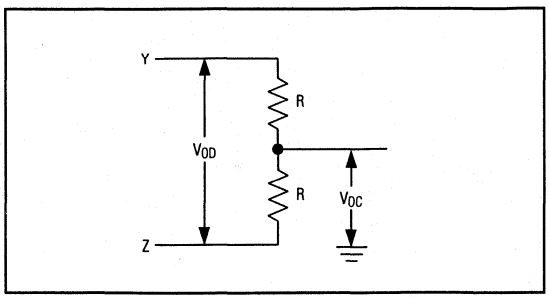


Figure 5. Driver DC Test Load

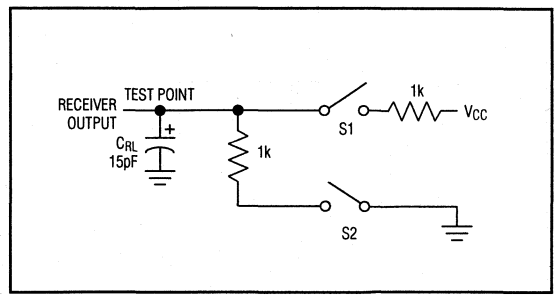


Figure 6. Receiver Enable/Disable Timing Test Load

Fail-Safe

The MAX3080 family **guarantees** a logic-high receiver output when the receiver inputs are shorted or open, or when they are connected to a terminated transmission line with all drivers disabled. This is done by setting the receiver threshold between -50mV and -200mV. If the differential receiver input voltage (A-B) is greater than or equal to -50mV, RO is logic high. If A-B is less than or equal to -200mV, RO is logic low. In the case of a terminated bus with all transmitters disabled, the receiver's differential input voltage is pulled to 0V by the termination. With the receiver thresholds of the MAX3080 family, this results in a logic high with a 50mV minimum noise margin. Unlike previous fail-safe devices, the -50mV to -200mV threshold complies with the ±200mV EIA/TIA-485 standard.

MAX3089 Programming

The MAX3089 has several programmable operating modes. Transmitter rise and fall times are programmable between 2500ns, 750ns, and 25ns, resulting in maximum data rates of 115kbps, 500kbps, and 10Mbps, respectively. To select the desired data rate, drive SRL to one of three possible states by using a three-state driver, by connecting it to VCC or GND, or by leaving it unconnected. For 115kbps operation, set the three-state device in high-impedance mode or leave SRL unconnected. For 500kbps operation, drive SRL high or connect it to VCC. For 10Mbps operation, drive SRL low or connect it to GND. SRL can be changed during operation without interrupting data communications.

Occasionally, twisted-pair lines are connected backward from normal orientation. The MAX3089 has two pins that invert the phase of the driver and the receiver to correct for this problem. For normal operation, drive TXP and RXP low, connect them to ground, or leave them unconnected (internal pull-down). To invert the driver phase, drive TXP high or connect it to VCC. To invert the receiver phase, drive RXP high or connect it to VCC. Note that the receiver threshold is positive when RXP is high.

The MAX3089 can operate in full- or half-duplex mode. Drive the H/$\overline{F}$ pin low, leave it unconnected (internal pull-down), or connect it to GND for full-duplex operation, and drive it high for half-duplex operation. In full-duplex mode, the pin configuration of the driver and receiver is the same as that of a MAX3080 (Figure 4). In half-duplex mode, the receiver inputs are switched to the driver outputs, connecting outputs Y and Z to inputs A and B, respectively. In half-duplex mode, the internal full-duplex receiver input resistors are still connected to pins 11 and 12.

Applications Information

256 Transceivers on the Bus

The standard RS-485 receiver input impedance is 12kΩ (one-unit load), and the standard driver can drive up to 32 unit loads. The MAX3080 family of transceivers have a 1/8-unit-load receiver input impedance (96kΩ), allowing up to 256 transceivers to be connected in parallel on one communication line. Any combination of these devices and/or other RS-485 transceivers with a total of 32 unit loads or less can be connected to the line.

Reduced EMI and Reflections

The MAX3080–MAX3085, and MAX3089 with SRL = VCC or unconnected, are slew-rate limited, minimizing EMI and reducing reflections caused by improperly terminated cables. Figure 14 shows the driver output waveform and its Fourier analysis of a 20kHz signal transmitted by a MAX3086/MAX3087/MAX3088, and MAX3089 with SRL = GND. High-frequency harmonic

Fail-Safe, High-Speed (10Mbps), Slew-Rate-Limited RS-485/RS-422 Transceivers

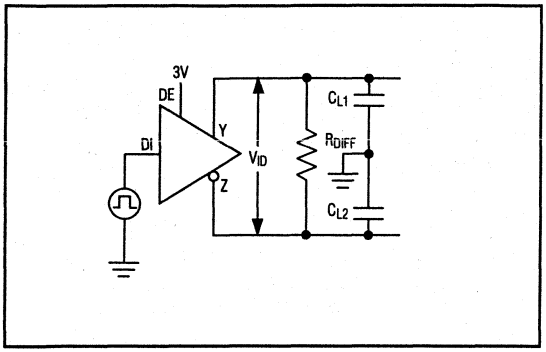


Figure 7. Driver Timing Test Circuit

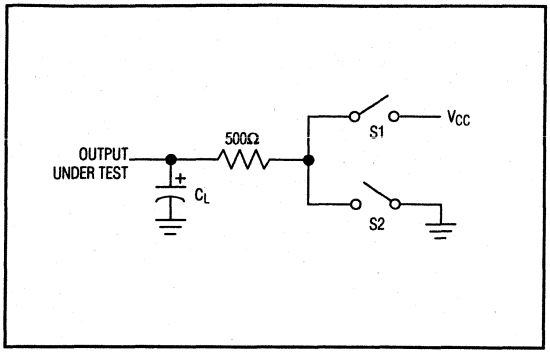


Figure 8. Driver Enable/Disable Timing Test Load

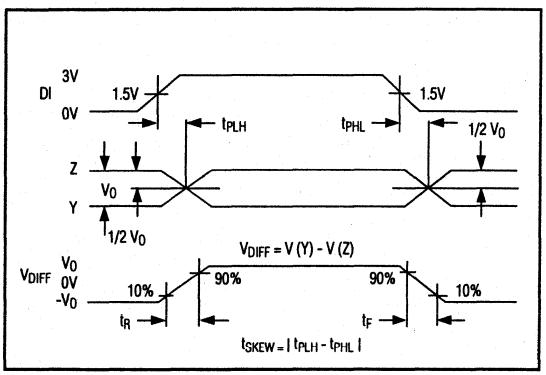


Figure 9. Driver Propagation Delays

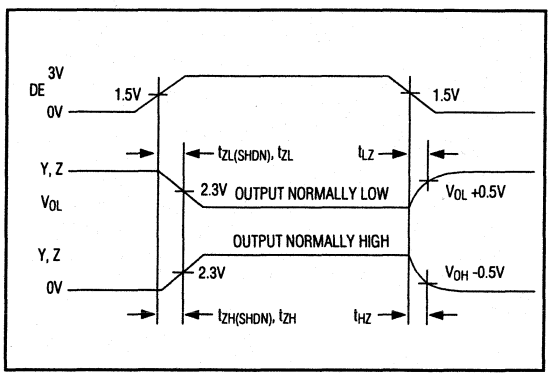


Figure 10. Driver Enable and Disable Times (except MAX3081/MAX3084/MAX3087)

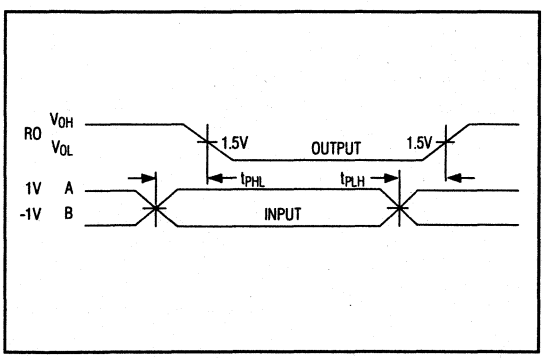


Figure 11. Receiver Propagation Delays

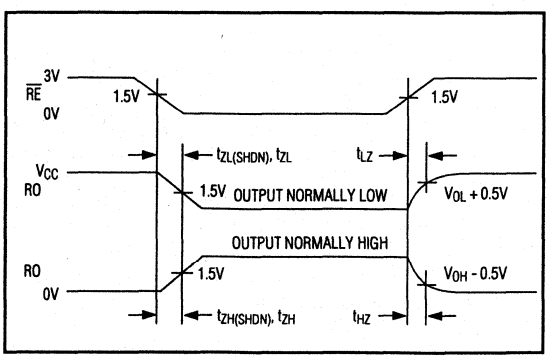


Figure 12. Receiver Enable and Disable Times (except MAX3081/MAX3084/MAX3087)

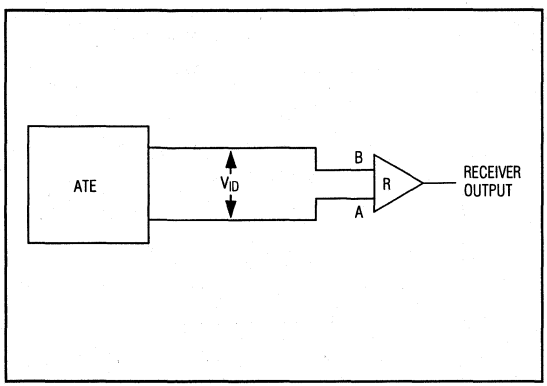


Figure 13. Receiver Propagation Delay Test Circuit

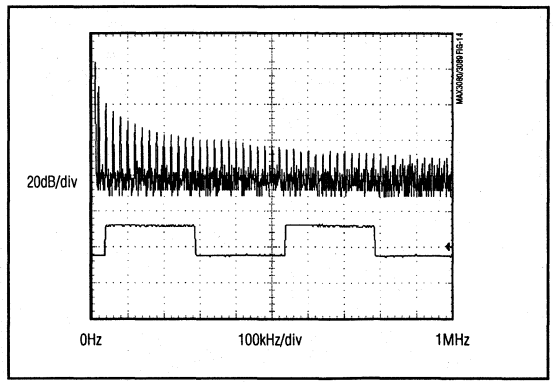


Figure 14. Driver Output Waveform and FFT Plot of MAX3086/MAX3087/MAX3088, and MAX3089 with SRL = GND, Transmitting a 20kHz Signal

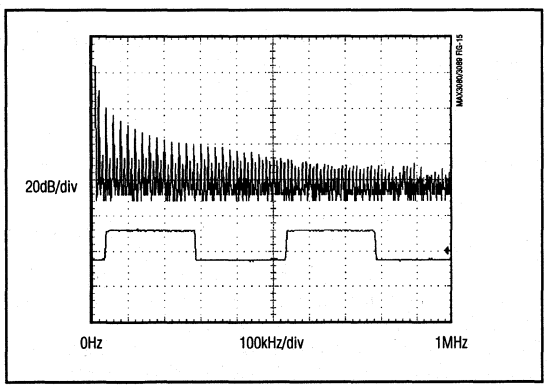


Figure 15. Driver Output Waveform and FFT Plot of MAX3083/MAX3084/MAX3085, and MAX3089 with SRL = VCC, Transmitting a 20kHz Signal

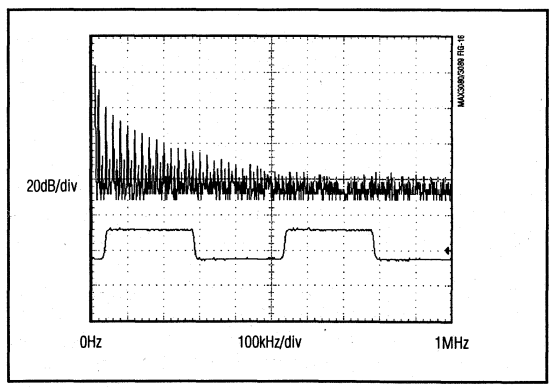


Figure 16. Driver Output Waveform and FFT Plot of MAX3080/MAX3081/MAX3082, and MAX3089 with SRL = Unconnected, Transmitting a 20kHz Signal

components with large amplitudes are evident. Figure 15 shows the same signal displayed for a MAX3083/MAX3084/MAX3085, and MAX3089 with SRL = VCC), transmitting under the same conditions. Figure 15's high-frequency harmonic components are much lower in amplitude, compared with Figure 14's, and the potential for EMI is significantly reduced. Figure 16 shows the same signal displayed for a MAX3080/MAX3081/MAX3082, and MAX3089 with SRL = unconnected, transmitting under the same conditions. Figure 16's high-frequency harmonic components are even lower.

In general, a transmitter's rise time relates directly to the length of an unterminated stub, which can be driven with only minor waveform reflections. The following equation expresses this relationship conservatively:

$$\text{Length} = t_{RISE} / (10 \times 1.5\text{ns/ft})$$

where t_{RISE} is the transmitter's rise time.

For example, the MAX3080's rise time is typically 1320ns, which results in excellent waveforms with a stub length up to 90 feet. A system can work well with longer unterminated stubs, even with severe reflections, if the waveform settles out before the UART samples them.

Fail-Safe, High-Speed (10Mbps), Slew-Rate-Limited RS-485/RS-422 Transceivers

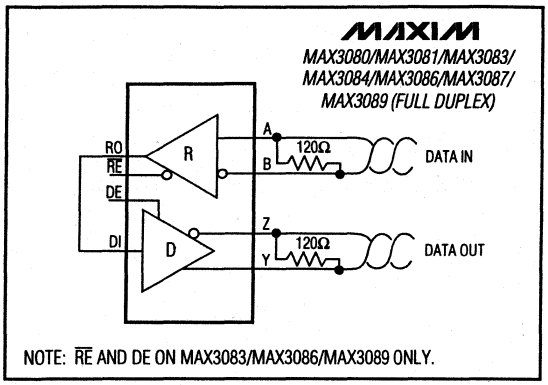


Figure 17. Line Repeater for MAX3080/MAX3081/ MAX3083/MAX3084/MAX3086/MAX3087, and MAX3089 in Full-Duplex Mode

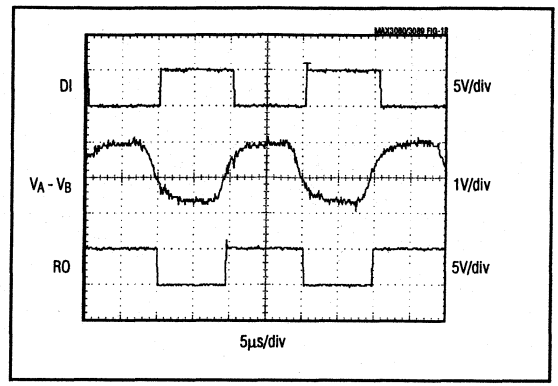


Figure 18. MAX3080/MAX3081/MAX3082, and MAX3089 with SRL = Unconnected, System Differential Voltage at 50kHz Driving 4000 feet of Cable

Low-Power Shutdown Mode (except MAX3082/MAX3085/MAX3088)

Low-power shutdown mode is initiated by bringing both $\overline{RE}$ high and DE low. In shutdown, the devices typically draw only 1nA of supply current.

$\overline{RE}$ and DE may be driven simultaneously; the parts are guaranteed not to enter shutdown if $\overline{RE}$ is high and DE is low for less than 50ns. If the inputs are in this state for at least 600ns, the parts are guaranteed to enter shutdown.

Enable times t_{ZH} and t_{ZL} in the *Switching Characteristics* tables assume the part was not in a low-power shutdown state. Enable times $t_{ZH(SHDN)}$ and $t_{ZL(SHDN)}$ assume the parts were shut down. It takes drivers and receivers longer to become enabled from low-power shutdown mode ($t_{ZH(SHDN)}$, $t_{ZH(SHDN)}$) than from driver/receiver-disable mode (t_{ZH}, t_{ZL}).

Driver Output Protection

Two mechanisms prevent excessive output current and power dissipation caused by faults or by bus contention. The first, a foldback current limit on the output stage, provides immediate protection against short circuits over the whole common-mode voltage range (see *Typical Operating Characteristics*). The second, a thermal shutdown circuit, forces the driver outputs into a high-impedance state if the die temperature becomes excessive.

Line Length vs. Data Rate

The RS-485/RS-422 standard covers line lengths up to 4000 feet. For line lengths greater than 4000 feet, use the repeater application shown in Figure 17.

Figures 18, 19, and 20 show the system differential voltage for the parts driving 4000 feet of 26AWG twisted-pair wire at 110kHz into 120Ω loads.

Typical Applications

The MAX3082/MAX3085/MAX3088/MAX3089 transceivers are designed for bidirectional data communications on multipoint bus transmission lines. Figures 21 and 22 show typical network applications circuits. These parts can also be used as line repeaters, with cable lengths longer than 4000 feet, as shown in Figure 17.

To minimize reflections, the line should be terminated at both ends in its characteristic impedance, and stub lengths off the main line should be kept as short as possible. The slew-rate-limited MAX3082/MAX3085, and the two modes of the MAX3089, are more tolerant of imperfect termination.

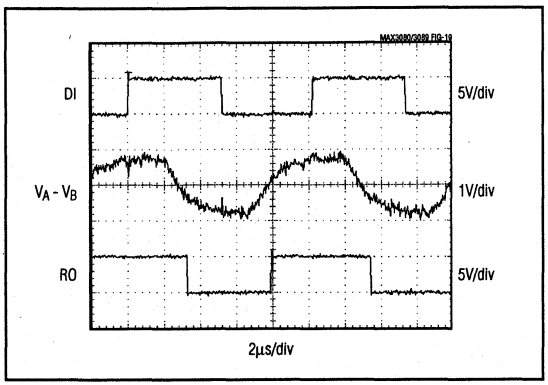


Figure 19. MAX3083/MAX3084/MAX3085, and MAX3089 with SRL = V_{CC}, System Differential Voltage at 50kHz Driving 4000 feet of Cable

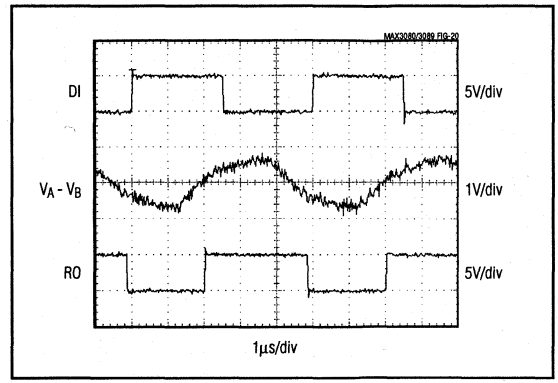


Figure 20. MAX3086/MAX3087/MAX3088, and MAX3089 with SRL = GND, System Differential Voltage at 200kHz Driving 4000 feet of Cable

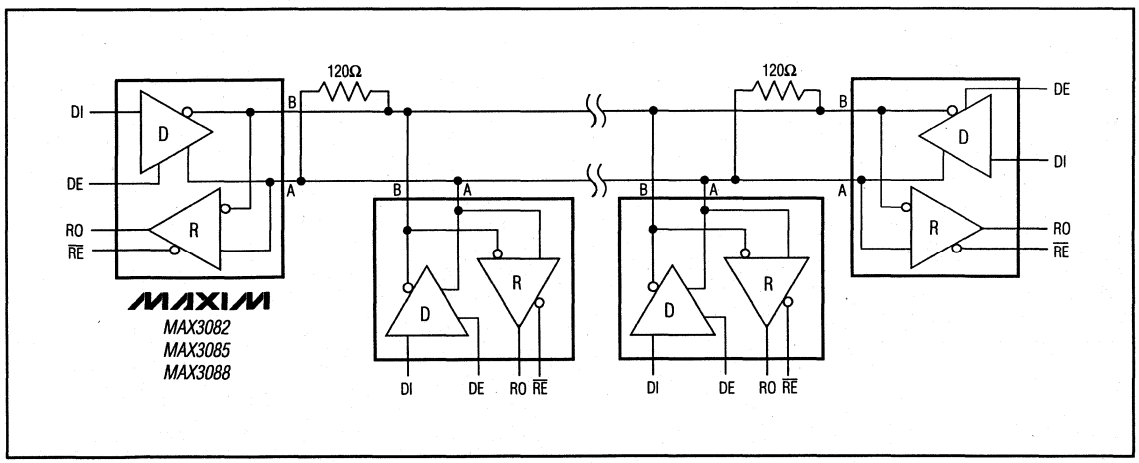


Figure 21. Typical Half-Duplex RS-485 Network

Fail-Safe, High-Speed (10Mbps), Slew-Rate-Limited RS-485/RS-422 Transceivers

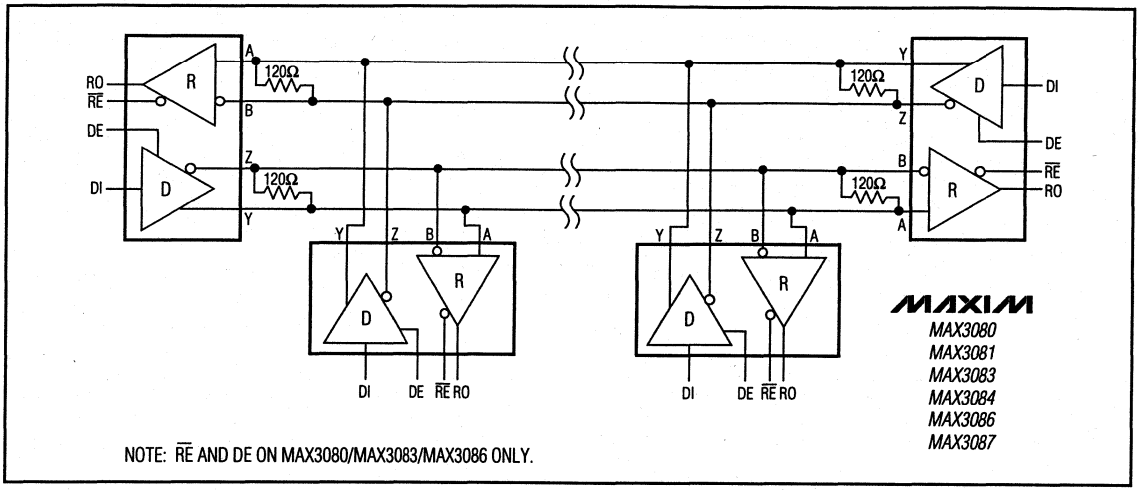


Figure 22. Typical Full-Duplex RS-485 Network

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX3081CPA	0°C to +70°C	8 Plastic DIP
MAX3081CSA	0°C to +70°C	8 SO
MAX3081EPA	-40°C to +85°C	8 Plastic DIP
MAX3081ESA	-40°C to +85°C	8 SO
MAX3082CPA	0°C to +70°C	8 Plastic DIP
MAX3082CSA	0°C to +70°C	8 SO
MAX3082EPA	-40°C to +85°C	8 Plastic DIP
MAX3082ESA	-40°C to +85°C	8 SO
MAX3083CPD	0°C to +70°C	14 Plastic DIP
MAX3083CSD	0°C to +70°C	14 SO
MAX3083EPD	-40°C to +85°C	14 Plastic DIP
MAX3083ESD	-40°C to +85°C	14 SO
MAX3084CPA	0°C to +70°C	8 Plastic DIP
MAX3084CSA	0°C to +70°C	8 SO
MAX3084EPA	-40°C to +85°C	8 Plastic DIP
MAX3084ESA	-40°C to +85°C	8 SO
MAX3085CPA	0°C to +70°C	8 Plastic DIP
MAX3085CSA	0°C to +70°C	8 SO
MAX3085EPA	-40°C to +85°C	8 Plastic DIP
MAX3085ESA	-40°C to +85°C	8 SO

PART	TEMP. RANGE	PIN-PACKAGE
MAX3086CPD	0°C to +70°C	14 Plastic DIP
MAX3086CSD	0°C to +70°C	14 SO
MAX3086EPD	-40°C to +85°C	14 Plastic DIP
MAX3086ESD	-40°C to +85°C	14 SO
MAX3087CPA	0°C to +70°C	8 Plastic DIP
MAX3087CSA	0°C to +70°C	8 SO
MAX3087EPA	-40°C to +85°C	8 Plastic DIP
MAX3087ESA	-40°C to +85°C	8 SO
MAX3088CPA	0°C to +70°C	8 Plastic DIP
MAX3088CSA	0°C to +70°C	8 SO
MAX3088EPA	-40°C to +85°C	8 Plastic DIP
MAX3088ESA	-40°C to +85°C	8 SO
MAX3089CPD	0°C to +70°C	14 Plastic DIP
MAX3089CSD	0°C to +70°C	14 SO
MAX3089EPD	-40°C to +85°C	14 Plastic DIP
MAX3089ESD	-40°C to +85°C	14 SO

19-1076; Rev 0; 9/96

MAXIM

±15kV ESD-Protected, EMC-Compliant, 230kbps RS-232 Serial Port for Motherboards/Desktop PCs

General Description

The MAX3185 is a complete DTE RS-232 serial port designed to meet the stringent ESD requirements of the European community. All transmitter outputs and receiver inputs are protected to ±15kV using IEC 1000-4-2 Air-Gap Discharge, ±8kV using IEC 1000-4-2 Contact Discharge, and ±15kV using the Human Body Model.

The MAX3185 has three RS-232 transmitters, five RS-232 receivers, and no charge pump, optimizing it for operation in desktop PC and motherboard applications. It is guaranteed to run at data rates up to 230kbps, providing compatibility with popular software for communicating with personal computers. Power-supply current is less than 300µA for I_{DD} and I_{SS}, and less than 1mA for I_{CC}.

The MAX3185 is pin and functionally compatible with the industry-standard 75185, so existing designs can instantly become EMC compliant. The MAX3185 is available in an SO package and in the tiny SSOP that further reduces board space.

Applications

Desktop PC

Motherboards

Instruments

Equipment Meeting IEC1000-4-2

Features

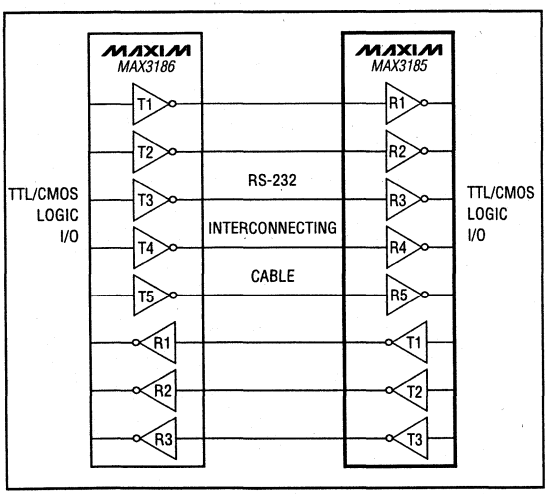
- **Enhanced ESD Protection:**
  ±15kV—Human Body Model
  ±8kV—IEC1000-4-2, Contact Discharge
  ±15kV—IEC1000-4-2, Air-Gap Discharge
- **Latchup Free During an ESD Event**
- **20-Pin SSOP and SO Packages**
- **Guaranteed 230kbps Data Rate**
- **Flow-Through Pinout**
- **Pin Compatible with SN75C185**
- **Complete DTE Serial Port**

Ordering Information

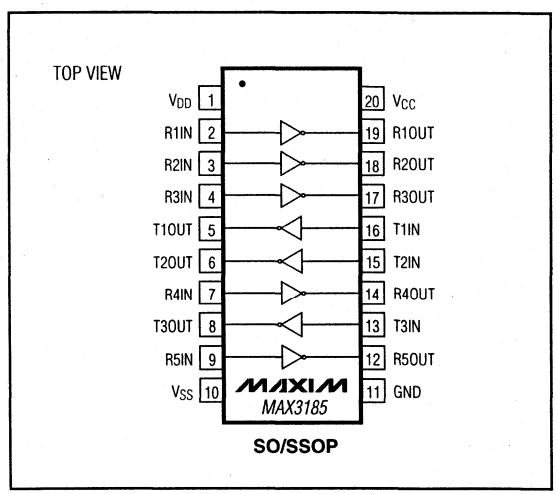
PART	TEMP. RANGE	PIN-PACKAGE
MAX3185CWP	0°C to +70°C	20 SO
MAX3185CAP	0°C to +70°C	20 SSOP
MAX3185EWP	-40°C to +85°C	20 SO
MAX3185EAP	-40°C to +85°C	20 SSOP

2

Typical Operating Circuit



Pin Configuration



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

±15kV ESD-Protected, EMC-Compliant, 230kbps RS-232 Serial Port for Motherboards/Desktop PCs

ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... -0.3V to +7V
V_{DD} ..... -0.3V to +14V
V_{SS} ..... +0.3V to -14V
Input Voltages
  T_{IN} ..... -0.3V to +6V
  R_{IN} ..... ±30V
Output Voltages
  T_{OUT} ..... ±15V
  R_{OUT} ..... -0.3V to (V_{CC} + 0.3V)
Short-Circuit Duration
  T_{OUT} (one at a time) ..... Continuous
  R_{OUT} (one at a time) ..... Continuous

Continuous Power Dissipation (T_A = +70°C)
  Wide SO (derate 10.00mW/°C above +70°C) 800mW
  SSOP (derate 8.00mW/°C above +70°C) 640mW
Operating Temperature Ranges
  MAX3185C_ P ..... 0°C to +70°C
  MAX3185E_ P ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.5V to +5.5V, V_{DD} = +10.8V to +13.2V, V_{SS} = -10.8V to -13.2V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Operating Voltage Range	V_{CC}		4.5		5.5	V
	V_{DD}		10.8		13.2	
	V_{SS}		-13.2		-10.8	
Supply Current	I_{CC}	No load		380	1500	µA
	I_{DD}	No load		185	500	
	I_{SS}	No load		185	500	
LOGIC						
Input Logic Threshold Low	V_{ILT}	T_{IN}			0.8	V
Input Logic Threshold High	V_{IHT}	T_{IN}	2.0			V
Input Leakage Current				0.01	1	µA
Output Voltage Low	V_{OLR}	R_{OUT}; I_{SINK} = 3.2mA			0.4	V
Output Voltage High	V_{OHR}	R_{OUT}; I_{SOURCE} = 1mA	V_{CC} - 0.6			V
TRANSMITTER OUTPUTS						
Output Voltage Swing		V_{DD} = 7.0V, V_{SS} = -7.0V, R_L = 3kΩ	±5.0			V
		V_{DD} = 12V, V_{SS} = -12V, R_L = 3kΩ	±9.5			
Transmitter Output Resistance		V_{CC} = V_{DD} = V_{SS} = 0V, V_{T_OUT} = ±2V	300			Ω
RS-232 Output Short-Circuit Current				±35	±60	mA
RECEIVER INPUTS						
Receiver Input Voltage Operating Range			-25		25	V
RS-232 Input Threshold Low			0.75			V
RS-232 Input Threshold High					2.4	V
RS-232 Input Hysteresis				0.65		V
RS-232 Input Resistance			3	5	7	kΩ
Receiver Output Short-Circuit Current				±10		mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +4.5V to +5.5V, V_{DD} = +10.8V to +13.2V, V_{SS} = -10.8V to -13.2V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

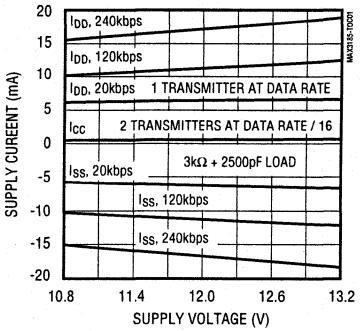
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ESD CHARACTERISTICS							
ESD Protection		Human Body Model			±15		kV
		IEC1000-4-2 (Contact Discharge)			±8		
		IEC1000-4-2 (Air-Gap Discharge)			±15		
TIMING CHARACTERISTICS							
Transmitter Output Propagation Delay, Low to High	t_{PLHT}	V_{DD} = 12V, V_{SS} = -12V, R_L = 3kΩ, C_L = 1000pF, T_A = +25°C				4	µs
Transmitter Output Propagation Delay, High to Low	t_{PHLT}	V_{DD} = 12V, V_{SS} = -12V, R_L = 3kΩ, C_L = 1000pF, T_A = +25°C				4	µs
Transmitter Propagation Delay Skew, $\lvert t_{PLHT} - t_{PHLT} \rvert$	t_{SKT}	V_{DD} = 12V, V_{SS} = -12V, R_L = 3kΩ, C_L = 1000pF, T_A = +25°C				0.4	µs
Transition Output Slew Rate	SR	V_{DD} = 12V, V_{SS} = -12V, R_L = 3kΩ to 7kΩ, measured from +3V to -3V or -3V to +3V, Figure 3, T_A = +25°C	C_L = 150pF to 2500pF	4		30	V/µs
			C_L = 50pF to 1000pF	8		30	
Receiver Output Propagation Delay, Low to High	t_{PLHR}	V_{CC} = 5V, C_L = 50pF, T_A = +25°C				4.0	µs
Receiver Output Propagation Delay, High to Low	t_{PHLR}	V_{CC} = 5V, C_L = 50pF, T_A = +25°C				4.0	µs
Receiver Propagation Delay Skew, $\lvert t_{PLHR} - t_{PHLR} \rvert$	t_{SKR}	V_{CC} = 5V, C_L = 50pF, T_A = +25°C				0.4	µs
Guaranteed Data Rate	DR	V_{CC} = 5V, V_{DD} = 12V, V_{SS} = -12V, R_L = 3kΩ to 7kΩ, T_A = +25°C	C_L = 50pF to 2500pF	120			kbps
			C_L = 50pF to 1000pF	230			
Mouse Driveability		T3OUT = -5mA, T1OUT = T2OUT = +5mA		±7.5			V

±15kV ESD-Protected, EMC-Compliant, 230kbps RS-232 Serial Port for Motherboards/Desktop PCs

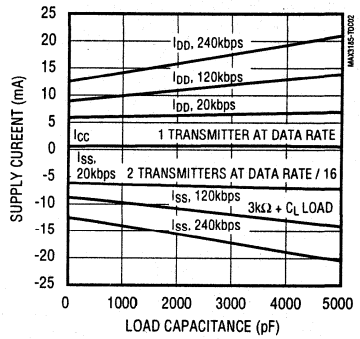
Typical Operating Characteristics

(V_{CC} = +5.0V, V_{DD} = +12.0V, V_{SS} = -12.0V, T_A = +25°C, unless otherwise noted.)

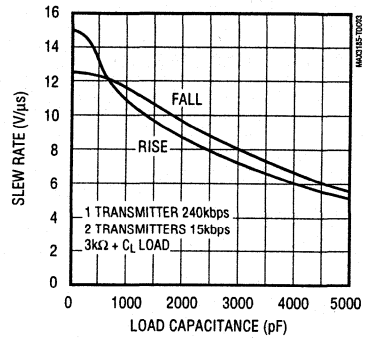
SUPPLY CURRENT vs. SUPPLY VOLTAGE



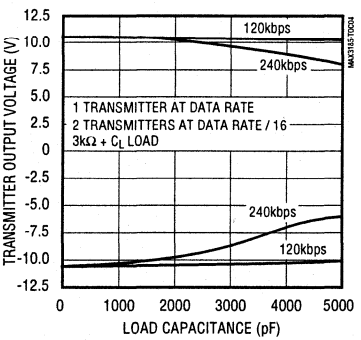
SUPPLY CURRENT vs. LOAD CAPACITANCE



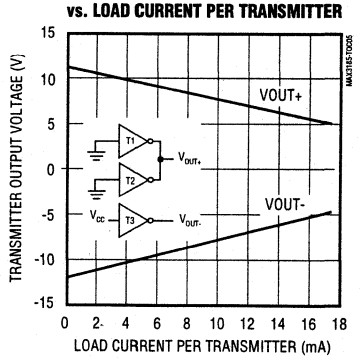
SLEW RATE vs. LOAD CAPACITANCE



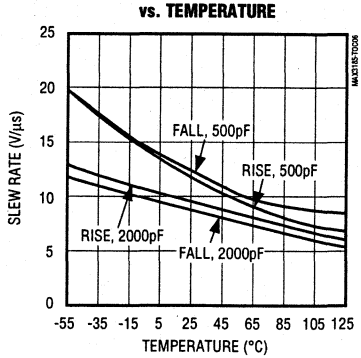
TRANSMITTER OUTPUT VOLTAGE vs. LOAD CAPACITANCE



MAX3185 TRANSMITTER OUTPUT VOLTAGE vs. LOAD CURRENT PER TRANSMITTER



SLEW RATE vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1	V_{DD}	Supply-Voltage Input, +10.8V to +13.2V
12, 14, 17, 18, 19	R5OUT–R1OUT	Receiver Outputs, swing between GND and V_{CC}
16, 15, 13	T3IN, T2IN, T1IN	Transmitter Inputs
10	V_{SS}	Supply-Voltage Input, -10.8V to -13.2V
11	GND	Ground. Connect system to ground.
2, 3, 4, 7, 9	R1IN–R5IN	Receiver Inputs
5, 6, 8	T1OUT, T2OUT, T3OUT	Transmitter Outputs, swing between V_{DD} and V_{SS}
20	V_{CC}	Supply-Voltage Input, +4.5V to +5.5V

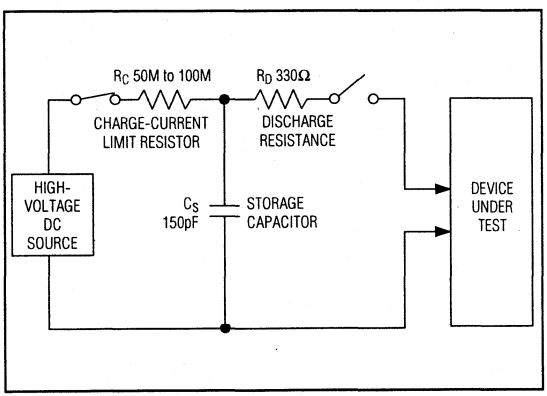


Figure 1a. IEC1000-4-2 ESD Test Model

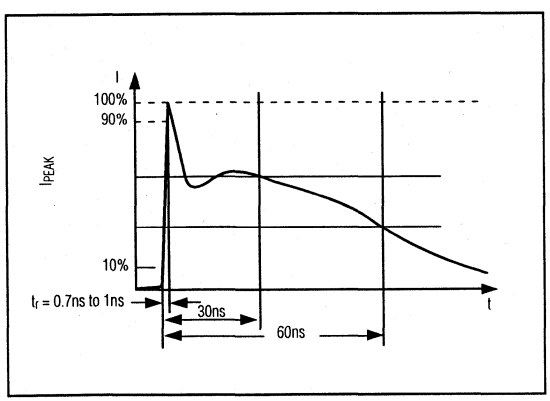


Figure 1b. IEC1000-4-2 ESD-Generator Current Waveform

Detailed Description

±15kV ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The MAX3185 driver outputs and receiver inputs have extra protection against static electricity found in normal operation. Maxim's engineers developed state-of-the-art structures to protect these pins against ESD of ±15kV, without damage. After an ESD event, the MAX3185 continues working without latchup.

ESD protection can be tested in several ways. The transmitter outputs and the receiver inputs are characterized for protection to the following:

1) ±15kV using the Human Body Model
2) ±8kV using the Contact-Discharge Method specified in IEC1000-4-2 (formerly IEC801-2)
3) ±15kV using the Air-Gap Method specified in IEC1000-4-2 (formerly IEC801-2)

ESD Test Conditions

ESD performance depends on a number of conditions. Contact Maxim for a reliability report that documents test setup, methodology, and results.

±15kV ESD-Protected, EMC-Compliant, 230kbps RS-232 Serial Port for Motherboards/Desktop PCs

Human Body Model

Figure 2a shows the Human Body Model, and Figure 2b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

IEC1000-4-2

The IEC1000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits. The MAX3185 helps you design equipment that meets Level 4 (the highest level) of IEC1000-4-2, without additional ESD-protection components.

The main difference between tests done using the Human Body Model and IEC1000-4-2 is higher peak current in IEC1000-4-2. Because series resistance is lower in the IEC1000-4-2 ESD test model (Figure 1a), the ESD withstand voltage measured to this standard is generally lower than that measured using the Human Body Model. Figure 1b shows the current waveform for the ±8kV IEC1000-4-2 Level 4 ESD Contact-Discharge test.

The Air-Gap test involves approaching the device with a charge probe. The Contact-Discharge method connects the probe to the device before the probe is energized.

Machine Model

The Machine Model for ESD testing uses a 200pF storage capacitor and zero-discharge resistance. It mimics the stress caused by handling during manufacturing and assembly. Of course, all pins (not just RS-232 inputs and outputs) require this protection during manufacturing. Therefore, the Machine Model is less relevant to the I/O ports than are the Human Body Model and IEC1000-4-2.

Applications Information

Use proper layout to ensure other devices on your board are not damaged in an ESD strike. Currents as high as 60A can instantaneously pass into ground, so be sure to minimize the ground-lead return path to the power supply. A separate return path to the power supply is recommend. Trace widths should be greater than 40 mils. Bypass V_{CC}, V_{DD}, and V_{SS} with 0.1µF capacitors as close to the part as possible to ensure maximum ESD protection.

Tie any unused transmitter inputs to GND or V_{CC}. No external protection diodes are needed because the MAX3185 is not sensitive to power-supply sequencing.

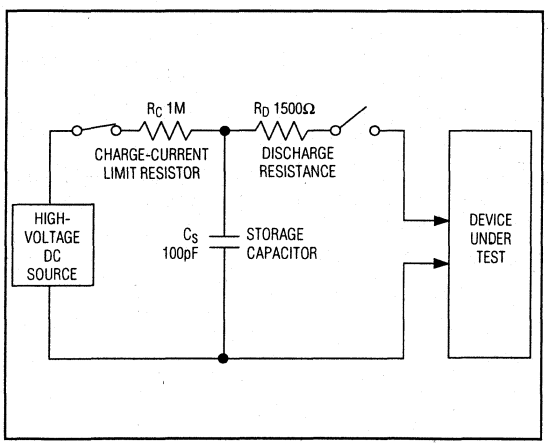


Figure 2a. Human Body ESD Test Model

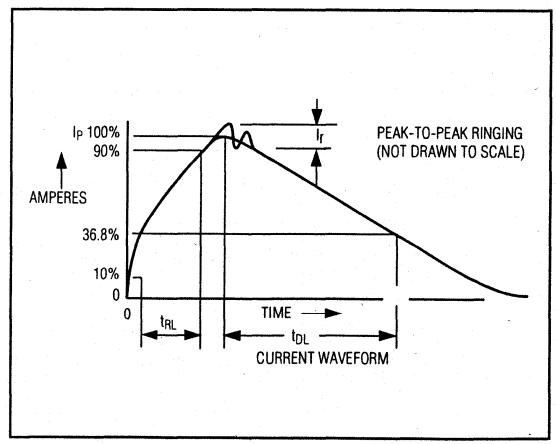


Figure 2b. Human Body Model Current Waveform

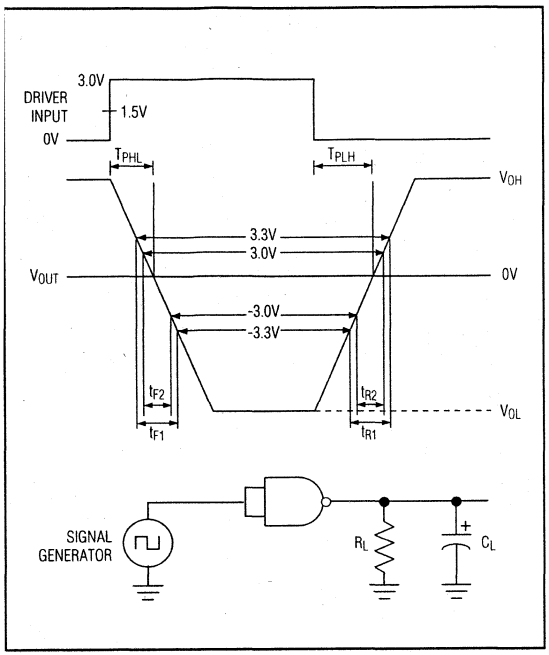


Figure 3. Slew-Rate Test Circuit and Timing Diagram

Chip Information

TRANSISTOR COUNT: 217

19-1077; Rev 0; 9/96

MAXIM

±15kV ESD-Protected, EMC-Compliant, 230kbps RS-232 Serial Port for Modems

General Description

The MAX3186 is a complete DCE RS-232 serial port designed to meet the stringent ESD requirements of the European community. All transmitter outputs and receiver inputs are protected to ±15kV using IEC 1000-4-2 Air-Gap Discharge, ±8kV using IEC 1000-4-2 Contact Discharge, and ±15kV using the Human Body Model.

The MAX3186 has five RS-232 transmitters, three RS-232 receivers, and no charge pump, optimizing it for operation in modem applications. It is guaranteed to run at data rates up to 230kbps, providing compatibility with popular software for communicating with personal computers. Power-supply current is less than 300µA for I_{DD} and I_{SS}, and less than 1mA for I_{CC}.

The MAX3186 is available in an SO package and in the tiny SSOP that further reduces board space.

Applications

Modems

ISDN Modems

Instruments

Equipment Meeting IEC1000-4-2

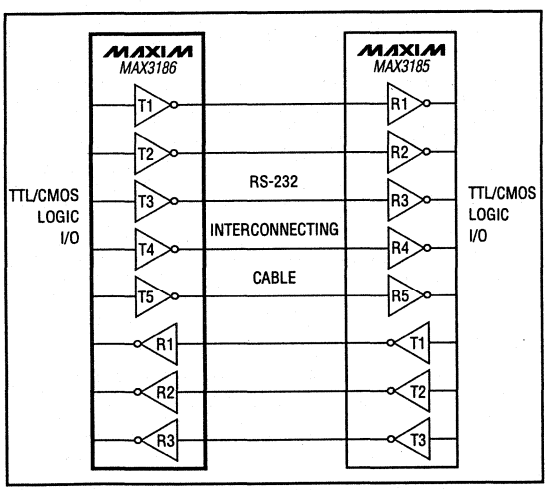
Features

- **Enhanced ESD Protection:**
  - **±15kV—Human Body Model**
  - **±8kV—IEC1000-4-2, Contact Discharge**
  - **±15kV—IEC1000-4-2, Air-Gap Discharge**
- **Latchup Free During an ESD Event**
- **20-Pin SSOP or SO Packages**
- **Guaranteed 230kbps Data Rate**
- **Flow-Through Pinout**
- **Complete DCE Serial Port**

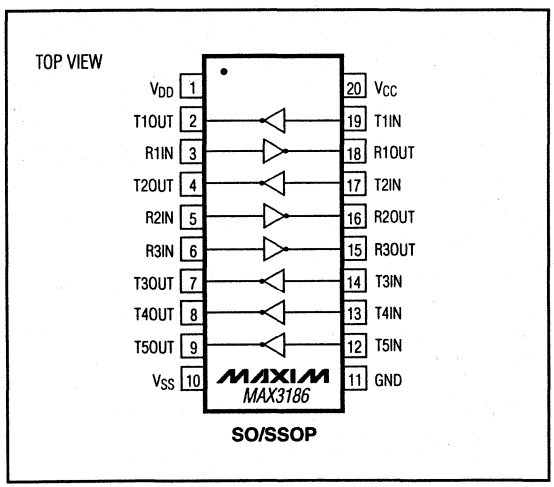
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3186CWP	0°C to +70°C	20 SO
MAX3186CAP	0°C to +70°C	20 SSOP
MAX3186EWP	-40°C to +85°C	20 SO
MAX3186EAP	-40°C to +85°C	20 SSOP

Typical Operating Circuit



Pin Configuration



SO/SSOP

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

±15kV ESD-Protected, EMC-Compliant, 230kbps RS-232 Serial Port for Modems

ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... -0.3V to +7V
V_{DD} ..... -0.3V to +14V
V_{SS} ..... +0.3V to -14V
Input Voltages
T_{IN} ..... -0.3V to +6V
R_{IN} ..... ±30V
Output Voltages
T_{OUT} ..... ±15V
R_{OUT} ..... -0.3V to (V_{CC} + 0.3V)
Short-Circuit Duration
T_{OUT} (one at a time) ..... Continuous
R_{OUT} (one at a time) ..... Continuous

Continuous Power Dissipation (T_A = +70°C)
Wide SO (derate 10.00mW/°C above +70°C) 800mW
SSOP (derate 8.00mW/°C above +70°C) 640mW
Operating Temperature Ranges
MAX3186C_P ..... 0°C to +70°C
MAX3186E_P ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.5V to +5.5V, V_{DD} = +10.8V to +13.2V, V_{SS} = -10.8V to -13.2V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Operating Voltage Range	V_{CC}		4.5		5.5	V
	V_{DD}		10.8		13.2	
	V_{SS}		-13.2		-10.8	
Supply Current	I_{CC}	No load		230	1000	µA
	I_{DD}	No load		280	750	
	I_{SS}	No load		280	750	
LOGIC						
Input Logic Threshold Low	V_{ILT}	T_{IN}			0.8	V
Input Logic Threshold High	V_{IHT}	T_{IN}	2.0			V
Input Leakage Current				0.01	1	µA
Output Voltage Low	V_{OLR}	R_{OUT}; I_{SINK} = 3.2mA			0.4	V
Output Voltage High	V_{OHR}	R_{OUT}; I_{SOURCE} = 1mA	V_{CC} - 0.6			V
TRANSMITTER OUTPUTS						
Output Voltage Swing		V_{DD} = 7.0V, V_{SS} = -7.0V, R_L = 3kΩ	±5.0			V
		V_{DD} = 12V, V_{SS} = -12V, R_L = 3kΩ	±9.5			
Transmitter Output Resistance		V_{CC} = V_{DD} = V_{SS} = 0V, V_{T_OUT} = ±2V	300			Ω
RS-232 Output Short-Circuit Current				±35	±60	mA
RECEIVER INPUTS						
Receiver Input Voltage Operating Range			-25		25	V
RS-232 Input Threshold Low			0.75			V
RS-232 Input Threshold High					2.4	V
RS-232 Input Hysteresis				0.65		V
RS-232 Input Resistance			3	5	7	kΩ
Receiver Output Short-Circuit Current				±10		mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +4.5V to +5.5V, V_{DD} = +10.8V to +13.2V, V_{SS} = -10.8V to -13.2V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

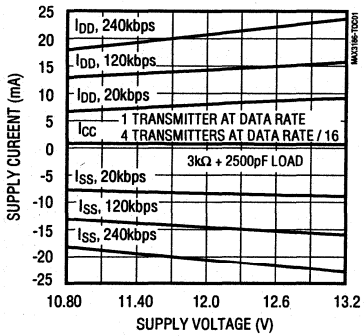
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ESD CHARACTERISTICS							
ESD Protection		Human Body Model			±15		kV
		IEC1000-4-2 (Contact Discharge)			±8		
		IEC1000-4-2 (Air-Gap Discharge)			±15		
TIMING CHARACTERISTICS							
Transmitter Output Propagation Delay, Low to High	t_{PLHT}	V_{DD} = 12V, V_{SS} = -12V, R_L = 3kΩ, C_L = 1000pF, T_A = +25°C				4	µs
Transmitter Output Propagation Delay, High to Low	t_{PHLT}	V_{DD} = 12V, V_{SS} = -12V, R_L = 3kΩ, C_L = 1000pF, T_A = +25°C				4	µs
Transmitter Propagation Delay Skew, $\lvert t_{PLHT} - t_{PHLT} \rvert$	t_{SKT}	V_{DD} = 12V, V_{SS} = -12V, R_L = 3kΩ, C_L = 1000pF, T_A = +25°C				0.4	µs
Transition Output Slew Rate	SR	V_{DD} = 12V, V_{SS} = -12V, R_L = 3kΩ to 7kΩ, measured from +3V to -3V or -3V to +3V, Figure 3, T_A = +25°C	C_L = 150pF to 2500pF	4		30	V/µs
			C_L = 50pF to 1000pF	8		30	
Receiver Output Propagation Delay, Low to High	t_{PLHR}	V_{CC} = 5V, C_L = 50pF, T_A = +25°C				4.0	µs
Receiver Output Propagation Delay, High to Low	t_{PHLR}	V_{CC} = 5V, C_L = 50pF, T_A = +25°C				4.0	µs
Receiver Propagation Delay Skew, $\lvert t_{PLHR} - t_{PHLR} \rvert$	t_{SKR}	V_{CC} = 5V, C_L = 50pF, T_A = +25°C				0.4	µs
Guaranteed Data Rate	DR	V_{CC} = 5V, V_{DD} = 12V, V_{SS} = -12V, R_L = 3kΩ to 7kΩ, T_A = +25°C	C_L = 50pF to 2500pF	120			kbps
			C_L = 50pF to 1000pF	230			

±15kV ESD-Protected, EMC-Compliant, 230kbps RS-232 Serial Port for Modems

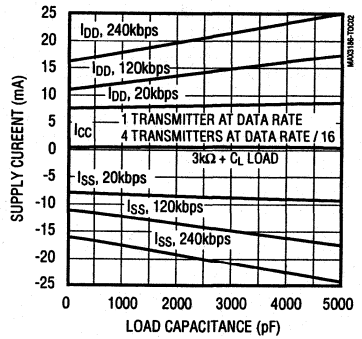
Typical Operating Characteristics

(V_{CC} = +5.0V, V_{DD} = +12.0V, V_{SS} = -12.0V, T_A = +25°C, unless otherwise noted.)

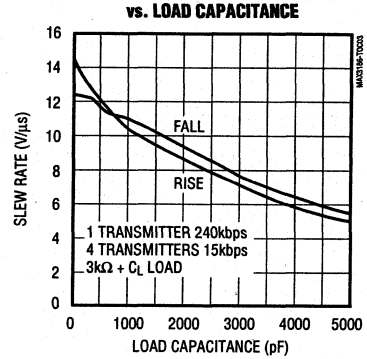
SUPPLY CURRENT vs. SUPPLY VOLTAGE



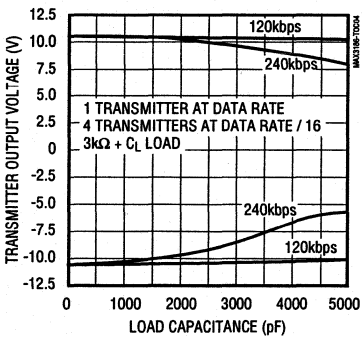
SUPPLY CURRENT vs. LOAD CAPACITANCE



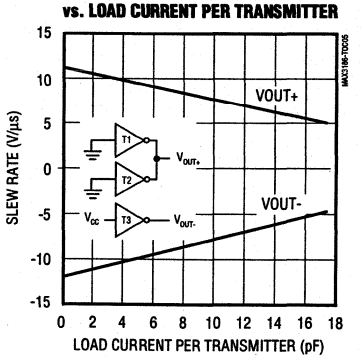
SLEW RATE vs. LOAD CAPACITANCE



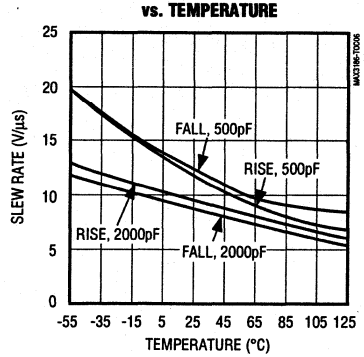
TRANSMITTER OUTPUT VOLTAGE vs. LOAD CAPACITANCE



TRANSMITTER OUTPUT VOLTAGE vs. LOAD CURRENT PER TRANSMITTER



SLEW RATE vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1	V_{DD}	Supply-Voltage Input, +10.8V to +13.2V
2, 4, 7, 8, 9	T1OUT–T5OUT	Transmitter Outputs, swing between V_{DD} and V_{SS}
3, 5, 6	R1IN, R2IN, R3IN	Receiver Inputs
10	V_{SS}	Supply-Voltage Input, -10.8V to -13.2V
11	GND	Ground. Connect to system ground.
12, 13, 14, 17, 19	T5IN–T1IN	Transmitter Inputs
15, 16, 18	R3OUT, R2OUT, R1OUT	Receiver Outputs, swing between GND and V_{CC}
20	V_{CC}	Supply-Voltage Input, +4.5V to +5.5V

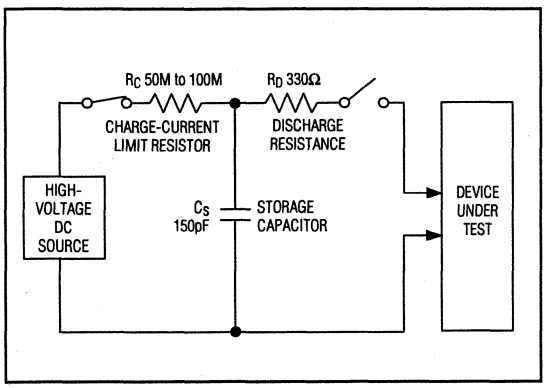


Figure 1a. IEC1000-4-2 ESD Test Model

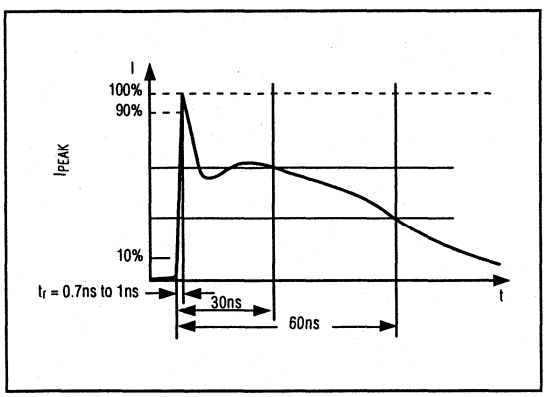


Figure 1b. IEC1000-4-2 ESD Generator Current Waveform

Detailed Description

±15kV ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The MAX3186 driver outputs and receiver inputs have extra protection against static electricity found in normal operation. Maxim's engineers developed state-of-the-art structures to protect these pins against ESD of ±15kV, without damage. After an ESD event, the MAX3186 continues working without latchup.

ESD protection can be tested in several ways. The transmitter outputs and the receiver inputs are characterized for protection to the following:

1) ±15kV using the Human Body Model
2) ±8kV using the Contact-Discharge Method specified in IEC1000-4-2 (formerly IEC801-2)
3) ±15kV using the Air-Gap Method specified in IEC1000-4-2 (formerly IEC801-2)

ESD Test Conditions

ESD performance depends on a number of conditions. Contact Maxim for a reliability report that documents test setup, methodology, and results.

±15kV ESD-Protected, EMC-Compliant, 230kbps RS-232 Serial Port for Modems

Human Body Model

Figure 2a shows the Human Body Model, and Figure 2b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

IEC1000-4-2

The IEC1000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits. The MAX3186 helps you design equipment that meets Level 4 (the highest level) of IEC1000-4-2, without additional ESD-protection components.

The main difference between tests done using the Human Body Model and IEC1000-4-2 is higher peak current in IEC1000-4-2. Because series resistance is lower in the IEC1000-4-2 ESD test model (Figure 1a), the ESD withstand voltage measured to this standard is generally lower than measured using the Human Body Model. Figure 1b shows the current waveform for the ±8kV IEC1000-4-2 Level 4 ESD Contact-Discharge test.

The Air-Gap test involves approaching the device with a charge probe. The Contact-Discharge method connects the probe to the device before the probe is energized.

Machine Model

The Machine Model for ESD testing uses a 200pF storage capacitor and zero-discharge resistance. It mimics the stress caused by handling during manufacturing and assembly. Of course, all pins (not just RS-232 inputs and outputs) require this protection during manufacturing. Therefore, the Machine Model is less relevant to the I/O ports than are the Human Body Model and IEC1000-4-2.

Applications Information

Use proper layout to ensure other devices on your board are not damaged in an ESD strike. Currents as high as 60A can instantaneously pass into the ground, so be sure to minimize the ground-lead return path to the power supply. A separate return path to the power supply is recommend. Trace widths should be greater than 40 mils. Bypass V_{CC}, V_{DD}, and V_{SS} with 0.1µF capacitors as close to the part as possible to ensure maximum ESD protection.

Tie any transmitter inputs to GND or V_{CC}. No external protection diodes are needed because the MAX3186 is not sensitive to power-supply sequencing.

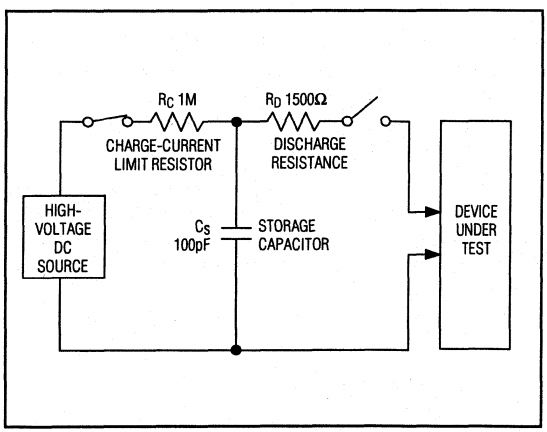


Figure 2a. Human Body ESD Test Model

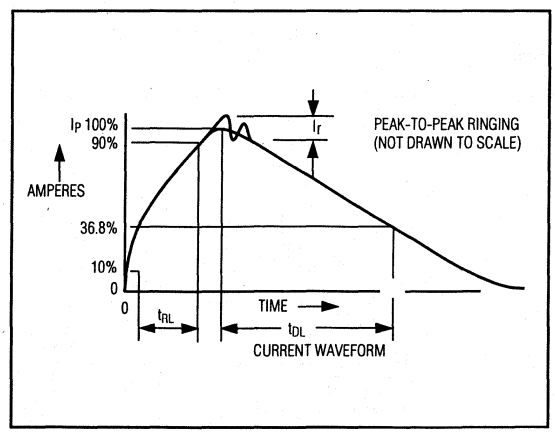


Figure 2b. Human Body Model Current Waveform

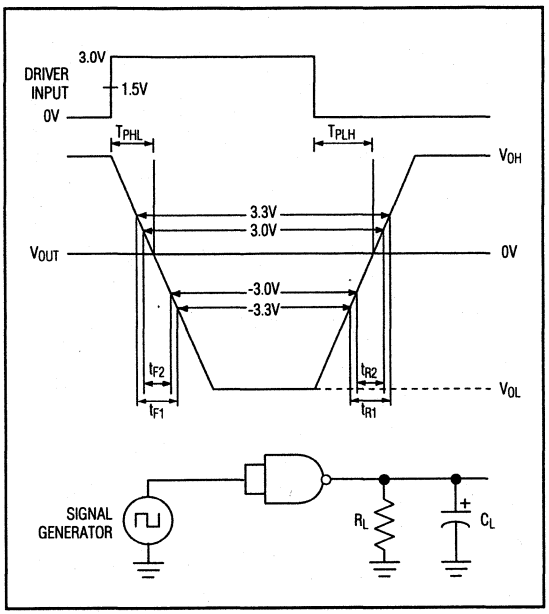
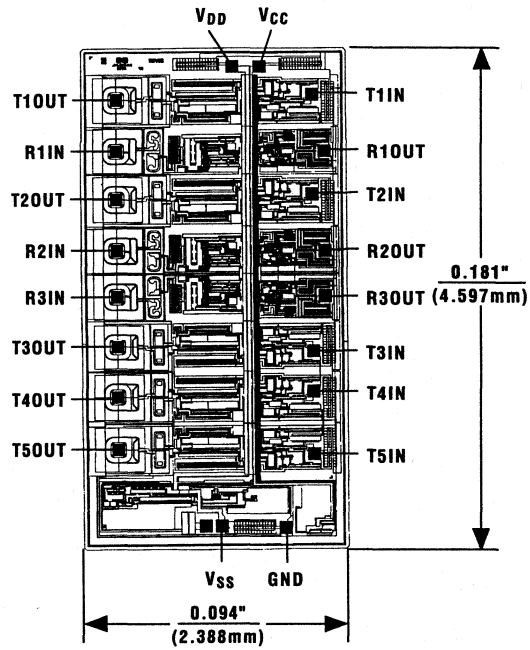


Figure 3. Slew-Rate Test Circuit and Timing Diagram

Chip Topography



TRANSISTOR COUNT: 195
SUBSTRATE CONNECTED TO GND

19-0306; Rev 4; 10/96

MAXIM

1µA Supply Current, True +3V to +5.5V RS-232 Transceivers with AutoShutdown™

General Description

The MAX3221/MAX3223/MAX3243 achieve 1µA supply current with Maxim's revolutionary AutoShutdown™ feature. When the MAX3221/MAX3223/MAX3243 do not sense a valid signal level on their receiver inputs, the on-board power supply and drivers shut down. This occurs if the RS-232 cable is disconnected or if the transmitters of the connected peripheral are turned off. The system turns on again when a valid level is applied to any RS-232 receiver input. As a result, the system saves power without changes to the existing BIOS or operating system.

The MAX3221/MAX3223/MAX3243 transceivers are 3V-powered EIA/TIA-232 and V.28/V.24 communications interfaces intended for notebook computer applications. A proprietary, high-efficiency, dual charge-pump power supply and a low-dropout transmitter combine to deliver true RS-232 performance from a single +3.0V to +5.5V supply. A guaranteed data rate of 120kbps provides compatibility with popular software for communicating with personal computers.

The MAX3221/MAX3223/MAX3243 require only 0.1µF capacitors in 3.3V operation, and can operate from input voltages ranging from +3.0V to +5.5V. They are ideal for 3.3V-only systems, mixed 3.3V and 5.0V systems, or 5.0V-only systems that require true RS-232 performance.

The MAX3221 is a 1-driver/1-receiver 16-pin SSOP version of the 20-pin MAX3223 (2-driver/2-receiver). The MAX3243 3-driver/5-receiver, complete serial port is ideal for notebook or subnotebook computers. The MAX3243 includes one complementary always-active receiver. This receiver can monitor an external device (such as a modem) in shutdown, without forward biasing the protection diodes in a UART that may have V_{CC} completely removed.

Selector Guide

PART	Tx	Rx	V_{CC} RANGE (V)	AutoShutdown
MAX3221	1	1	3.0 to 5.5	Yes
MAX3223	2	2	3.0 to 5.5	Yes
MAX3243	3	5	3.0 to 5.5	Yes

Features

- ♦ **1µA Supply Current Achieved with AutoShutdown**
- ♦ **Small 0.1µF Capacitors**
- ♦ **True RS-232 Operation from V_{CC} = 3.0V to 5.5V**
- ♦ **Meets EIA/TIA-562 Specifications Down to 2.7V**
- ♦ **Guaranteed 120kbps Data Rate**
- ♦ **6V/µs Min Guaranteed Slew Rate**
- ♦ **Smallest Single-Supply RS-232 Transceiver (MAX3221)**
- ♦ **Guaranteed Mouse Driveability (MAX3243)**

Applications

Notebook, Subnotebook, and Palmtop Computers

Battery-Powered Equipment

Hand-Held Equipment

Peripherals

Printers

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3221CAE	0°C to +70°C	16 SSOP
MAX3221EAE	-40°C to +85°C	16 SSOP
MAX3223CPP	0°C to +70°C	20 Plastic DIP
MAX3223CAP	0°C to +70°C	20 SSOP
MAX3223EPP	-40°C to +85°C	20 Plastic DIP
MAX3223EAP	-40°C to +85°C	20 SSOP
MAX3243CWI	0°C to +70°C	28 Wide SO
MAX3243CAI	0°C to +70°C	28 SSOP
MAX3243EWI	-40°C to +85°C	28 Wide SO
MAX3243EAI	-40°C to +85°C	28 SSOP

Pin Configurations appear at end of data sheet.

Typical Operating Circuits appear at end of data sheet.

AutoShutdown is a trademark of Maxim Integrated Products.

** Covered by U.S. Patent numbers 4,636,930; 4,679,134; 4,777,577; 4,797,899; 4,809,152; 4,897,774; 4,999,761; and other patents pending.*

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

1µA Supply Current, True +3V to +5.5V RS-232 Transceivers with AutoShutdown™

ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... -0.3V to +6V
V+ (Note 1) ..... -0.3V to +7V
V- (Note 1) ..... +0.3V to -7V
V+ + |V-| (Note 1) ..... +13V
Input Voltages
T_IN, $\overline{FORCEOFF}$, FORCEON, $\overline{EN}$ (MAX3223) ..... -0.3V to +6V
R_IN ..... ±25V
Output Voltages
T_OUT ..... ±13.2V
R_OUT, $\overline{INVALID}$ ..... -0.3V to (V_{CC} + 0.3V)
Short-Circuit Duration
T_OUT ..... Continuous

Continuous Power Dissipation (T_A = +70°C)
16-Pin SSOP (derate 7.14mW/°C above +70°C) 571mW
20-Pin Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
20-Pin SSOP (derate 8.00mW/°C above +70°C) 640mW
28-Pin Wide SO (derate 12.50mW/°C above +70°C) 1W
28-Pin SSOP (derate 9.52mW/°C above +70°C) 762mW
Operating Temperature Ranges
MAX32_ _C_ _ ..... 0°C to +70°C
MAX32_ _E_ _ ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: V+ and V- can have maximum magnitudes of 7V, but their absolute difference cannot exceed 13V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.0V to 5.5V, C1–C4 = 0.1µF (Note 2), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Supply Current, AutoShutdown	V_{CC} = 3.3V or 5.0V, T_A = +25°C	All R_IN open, FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}		1.0	10	µA
Supply Current, Shutdown		$\overline{FORCEOFF}$ = GND		1.0	10	µA
Supply Current, AutoShutdown Disabled		FORCEON = $\overline{FORCEOFF}$ = V_{CC}, no load		0.3	1.0	mA
LOGIC INPUTS AND RECEIVER OUTPUTS						
Input Logic Threshold Low	T_IN, FORCEON, $\overline{FORCEOFF}$, $\overline{EN}$ (MAX3223)				0.8	V
Input Logic Threshold High	T_IN, EN, FORCEON, $\overline{FORCEOFF}$	V_{CC} = 3.3V	2.0			V
		V_{CC} = 5.0V	2.4			
Input Leakage Current	T_IN, EN, FORCEON, $\overline{FORCEOFF}$			±0.01	±1.0	µA
Output Leakage Current	Receivers disabled			±0.05	±10	µA
Output Voltage Low	I_{OUT} = 1.6mA				0.4	V
Output Voltage High	I_{OUT} = -1.0mA		V_{CC} - 0.6	V_{CC} - 0.1		V
AUTOSHUTDOWN (FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC})						
Receiver Input Thresholds to Transmitters Enabled	Figure 5	Positive threshold			2.7	V
		Negative threshold	-2.7			
Receiver Input Thresholds to Transmitters Disabled	1µA supply current, Figure 5		-0.3		0.3	V
$\overline{INVALID}$ Output Voltage Low	I_{OUT} = 1.6mA				0.4	V
$\overline{INVALID}$ Output Voltage High	I_{OUT} = -1.0mA		V_{CC} - 0.6			V
Receiver Threshold to Transmitters Enabled (t_{WU})	Figure 5			250		µs
Receiver Positive or Negative Threshold to $\overline{INVALID}$ High (t_{INVH})	Figure 5			1		µs
Receiver Positive or Negative Threshold to $\overline{INVALID}$ Low (t_{INVL})	Figure 5			30		µs

1µA Supply Current, True +3V to +5.5V RS-232 Transceivers with AutoShutdown™

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.0V to 5.5V, C1–C4 = 0.1µF (Note 2), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RECEIVER INPUTS						
Input Voltage Range			-25		25	V
Input Threshold Low	T_A = +25°C	V_{CC} = 3.3V	0.6	1.2		V
		V_{CC} = 5.0V	0.8	1.5		
Input Threshold High	T_A = +25°C	V_{CC} = 3.3V		1.5	2.4	V
		V_{CC} = 5.0V		1.8	2.4	
Input Hysteresis				0.3		V
Input Resistance	T_A = +25°C		3	5	7	kΩ
TRANSMITTER OUTPUTS						
Output Voltage Swing	All transmitter outputs loaded with 3kΩ to ground		±5.0	±5.4		V
Output Resistance	V_{CC} = V+ = V- = 0V, transmitter output = ±2V		300	10M		Ω
Output Short-Circuit Current				±35	±60	mA
Output Leakage Current	V_{OUT} = ±12V, V_{CC} = 0V or 3.0V to 5.5V, transmitters disabled				±25	µA
MOUSE DRIVEABILITY (MAX3243)						
Transmitter Output Voltage	T1IN = T2IN = GND, T3IN = V_{CC}, T3OUT loaded with 3kΩ to GND, T1OUT and T2OUT loaded with 2.5mA each		±5			V
TIMING CHARACTERISTICS						
Maximum Data Rate	R_L = 3kΩ, C_L = 1000pF, one transmitter switching		120	235		kbps
Receiver Propagation Delay	Receiver input to receiver output, C_L = 150pF	t_{PHL}		0.3		µs
		t_{PLH}		0.3		
Receiver Output Enable Time	Normal operation			200		ns
Receiver Output Disable Time	Normal operation			200		ns
Transmitter Skew	| t_{PHL} - t_{PLH} |			100	500	ns
Receiver Skew	| t_{PHL} - t_{PLH} |			200	1000	ns
Transition-Region Slew Rate	V_{CC} = 3.3V, R_L = 3kΩ to 7kΩ, T_A = +25°C, measured from +3V to -3V or -3V to +3V	C_L = 200pF to 2500pF	4	8.0	30	V/µs
		C_L = 200pF to 1000pF	6		30	

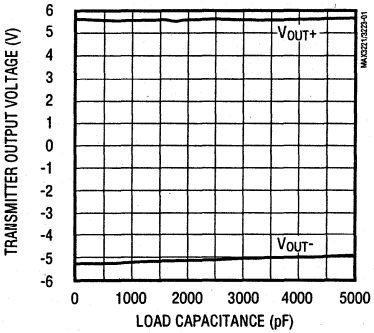
Note 2: C1–C4 = 0.1µF, tested at 3.3V ±10%. C1 = 0.047µF, C2–C4 = 0.33µF, tested at 5.0V ±10%.

1µA Supply Current, True +3V to +5.5V RS-232 Transceivers with AutoShutdown™

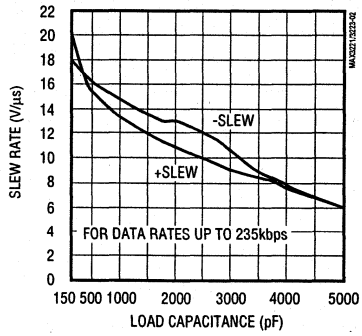
Typical Operating Characteristics

(V_{CC} = 3.3V, 235kbps data rate, 0.1µF capacitors, all transmitters loaded with 3kΩ, T_A = +25°C, unless otherwise noted.)

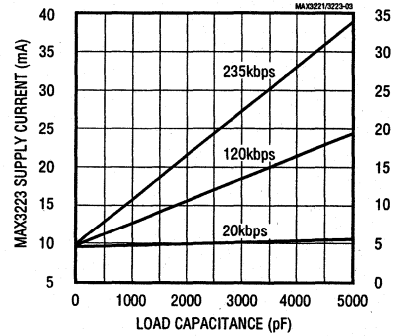
MAX3221/MAX3223
TRANSMITTER OUTPUT VOLTAGE vs. LOAD CAPACITANCE



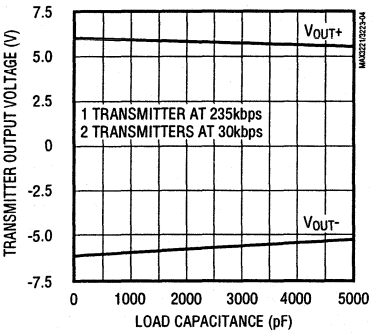
MAX3221/MAX3223
SLEW RATE vs. LOAD CAPACITANCE



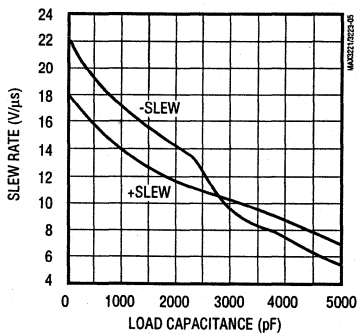
MAX3221/MAX3223
SUPPLY CURRENT vs. LOAD CAPACITANCE WHEN TRANSMITTING DATA



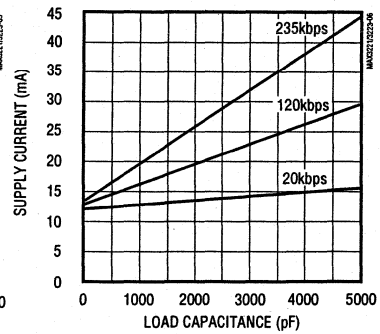
MAX3243
TRANSMITTER OUTPUT VOLTAGE vs. LOAD CAPACITANCE



MAX3243
SLEW RATE vs. LOAD CAPACITANCE



MAX3243
SUPPLY CURRENT vs. LOAD CAPACITANCE WHEN TRANSMITTING DATA



1µA Supply Current, True +3V to +5.5V RS-232 Transceivers with AutoShutdown™

Pin Description

PIN			NAME	FUNCTION
MAX3221	MAX3223	MAX3243		
1	1	—	$\overline{EN}$	Receiver Enable Control. Drive low for normal operation. Drive high to force the receiver outputs into a high-Z state.
5	5	1	C2+	Positive terminal of inverting charge-pump capacitor
6	6	2	C2-	Negative terminal of inverting charge-pump capacitor
7	7	3	V-	-5.5V generated by the charge pump
8	9, 16	4–8	R_IN	RS-232 Receiver Inputs
13	8, 17	9, 10, 11	T_OUT	RS-232 Transmitter Outputs
11	12, 13	12, 13, 14	T_IN	TTL/CMOS Transmitter Inputs
9	10, 15	15–19	R_OUT	TTL/CMOS Receiver Outputs
—	—	20	R2OUTB	Noninverting Receiver Output—active in shutdown
10	11	21	$\overline{INVALID}$	Output of the valid signal detector. Indicates if a valid RS-232 level is present on receiver inputs logic "1".
16	20	22	$\overline{FORCEOFF}$	Drive low to shut down transmitters and on-board power supply. This overrides all automatic circuitry and FORCEON (Table 1).
12	14	23	FORCEON	Drive high to override automatic circuitry keeping transmitters on ($\overline{FORCEOFF}$ must be high) (Table 1).
4	4	24	C1-	Negative terminal of the voltage doubler charge-pump capacitor
14	18	25	GND	Ground
15	19	26	V_{CC}	+3.0V to +5.5V Supply Voltage
3	3	27	V+	+5.5V generated by the charge pump
2	2	28	C1+	Positive terminal of the voltage doubler charge-pump capacitor

Detailed Description

Dual Charge-Pump Voltage Converter

The MAX3221/MAX3223/MAX3243's internal power supply consists of a regulated dual charge pump that provides output voltages of +5.5V (doubling charge pump) and -5.5V (inverting charge pump), regardless of the input voltage (V_{CC}) over the +3.0V to +5.5V range. The charge pumps operate in a discontinuous mode: if the output voltages are less than 5.5V, the charge pumps are enabled; if the output voltages exceed 5.5V, the charge pumps are disabled. Each charge pump requires a flying capacitor (C1, C2) and a reservoir capacitor (C3, C4) to generate the V+ and V- supplies.

RS-232 Transmitters

The transmitters are inverting level translators that convert CMOS-logic levels to 5.0V EIA/TIA-232 levels. They guarantee a 120kbps data rate with worst-case loads of 3kΩ in parallel with 1000pF, providing compatibility with PC-to-PC communication software (such as Laplink™). Typically, the MAX3221/MAX3223/MAX3243 can operate at data rates of 235kbps. Transmitters can be paralleled to drive multiple receivers or mice (MAX3243). Figure 1 shows a complete system connection.

When $\overline{FORCEOFF}$ is driven to ground, or the AutoShutdown circuitry senses invalid voltage levels at all receiver inputs, the transmitters are disabled and the outputs are forced into a high-impedance state.

LapLink is a trademark of Traveling Software.

1µA Supply Current, True +3V to +5.5V RS-232 Transceivers with AutoShutdown™

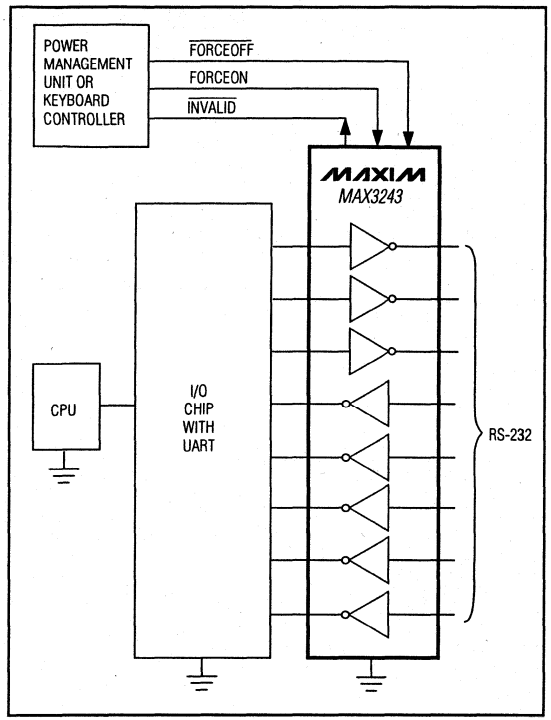


Figure 1. Interface Under Control of PMU

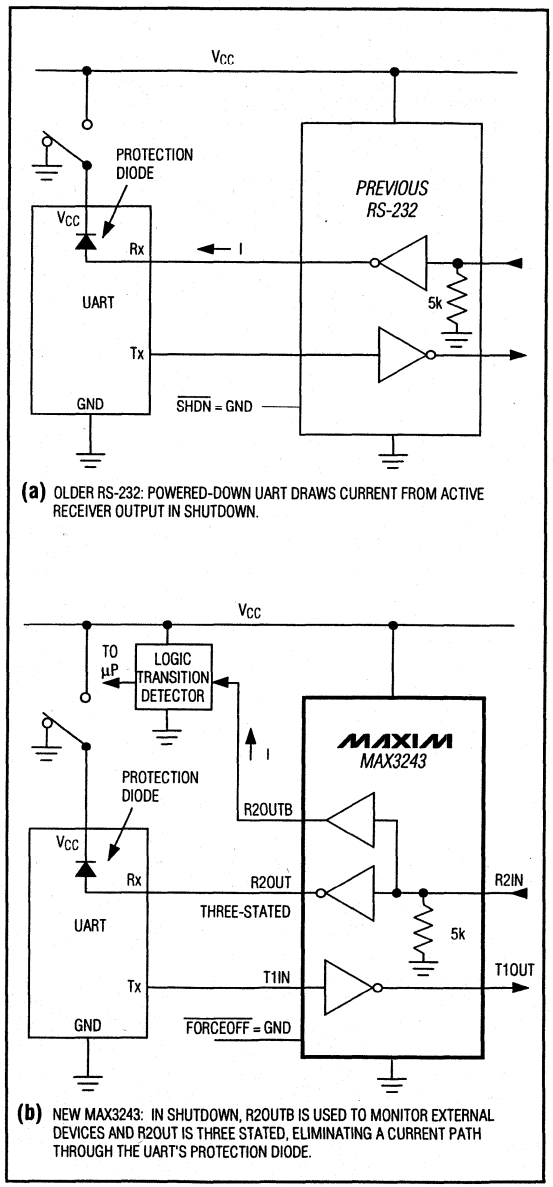


Figure 2. The MAX3243 detects RS-232 activity when the UART and interface are shut down.

RS-232 Receivers

The MAX3221/MAX3223/MAX3243's receivers convert RS-232 signals to CMOS-logic output levels. All receivers have one inverting three-state output. In shutdown ($\overline{FORCEOFF}$ = low) or in AutoShutdown, the MAX3221/MAX3223's receivers are active (Table 1). Driving $\overline{EN}$ high places the receiver(s) in a high-impedance state. The MAX3243's receivers are high impedance when the part is shut down.

The MAX3243 has an always-active complementary output (R2OUTB). R2OUTB is an extra output that monitors receiver activity while the other receivers are high impedance. This allows Ring Indicator to be monitored without forward biasing other devices connected to the receiver outputs. This is ideal for systems where V_{CC} is set to 0V in shutdown to accommodate peripherals, such as UARTs (Figure 2).

1µA Supply Current, True +3V to +5.5V RS-232 Transceivers with AutoShutdown™

Table 1a. MAX3221/MAX3223 $\overline{\text{FORCEOFF}}$ and Enable Control Truth Table

$\overline{\text{FORCEOFF}}$	$\overline{\text{EN}}$	T_OUT	R_OUT
0	0	High-Z	Active
0	1	High-Z	High-Z
1	0	Active*	Active
1	1	Active*	High-Z

Table 1b. MAX3243 $\overline{\text{FORCEOFF}}$ Control Truth Table

$\overline{\text{FORCEOFF}}$	T_OUT	R_OUT	R2OUTB
0	High-Z	High-Z	Active
1	Active*	Active*	Active

***Note:** If the part is in AutoShutdown mode ($\overline{\text{FORCEOFF}}$ = VCC, FORCEON = GND), it is shut down if no valid RS-232 levels are present on all receiver inputs.

AutoShutdown

A 1µA supply current is achieved with Maxim's new AutoShutdown feature, which operates when FORCEON is low and $\overline{\text{FORCEOFF}}$ is high. When the MAX3221/MAX3223/MAX3243 sense no valid signal levels on all receiver inputs for 30µs, the on-board power supply and drivers are shut off, reducing supply current to 1µA. This occurs if the RS-232 cable is disconnected or the connected peripheral transmitters are turned off. The system turns on again when a valid level is applied to any RS-232 receiver input. As a result, the system saves power without changes to the existing BIOS or operating system. When using AutoShutdown, the $\overline{\text{INVALID}}$ output is high when the device is on and low when the device is shut down. Because $\overline{\text{INVALID}}$ indicates the receiver inputs' condition, it can be used in any mode (Figure 3).

Table 2 and Figure 3c summarize the MAX3221/MAX3223/MAX3243 operating modes. FORCEON and $\overline{\text{FORCEOFF}}$ override the automatic circuitry and force the transceiver into its normal operating state or into its low-power standby state. When neither control is asserted, the IC selects between these states automatically based on receiver input levels. Figures 3a, 3b, and 5a depict valid and invalid RS-232 receiver levels.

A mouse or other system with AutoShutdown may need time to wake up. Figure 4 shows a circuit that forces the transmitters on for 100ms, allowing enough time for the

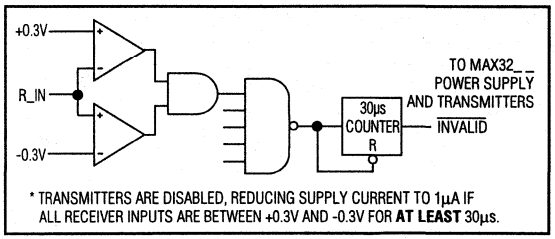


Figure 3a. MAX32_ _ Entering 1µA Supply Mode via AutoShutdown

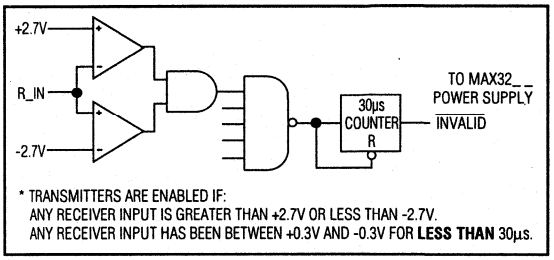


Figure 3b. MAX32_ _ with Transmitters Enabled Using AutoShutdown

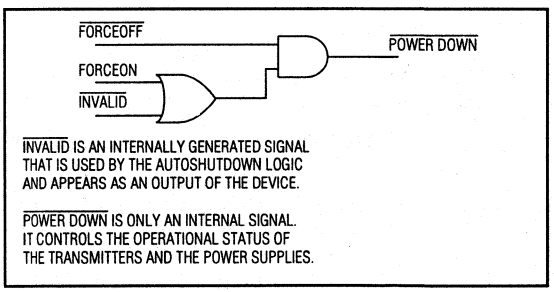


Figure 3c. AutoShutdown Logic

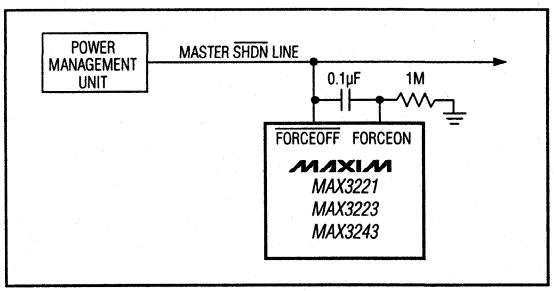


Figure 4. AutoShutdown with Initial Turn-On to Wake Up a Mouse or Another System

1µA Supply Current, True +3V to +5.5V RS-232 Transceivers with AutoShutdown™

Table 2. AutoShutdown Logic

RS-232 SIGNAL PRESENT AT RECEIVER INPUT	FORCEOFF INPUT	FORCEON INPUT	INVALID OUTPUT	TRANSCEIVER STATUS
Yes	H	X	H	Normal Operation
No	H	H	L	Normal Operation (Forced On)
No	H	L	L	Shutdown (AutoShutdown)
Yes	L	X	H	Shutdown (Forced Off)
No	L	X	L	Shutdown (Forced Off)

other system to realize that the MAX3221/MAX3223/MAX3243 is awake. If the other system outputs valid RS-232 signals within that time, the RS-232 ports on both systems remain enabled.

When shut down, the device's charge pumps are turned off, V+ decays to VCC, V- decays to ground, and the transmitter outputs are disabled (high impedance). The time required to exit shutdown is typically 100µs (Figure 5b).

Software-Controlled Shutdown

If direct software control is desired, INVALID can be used to indicate DTR or Ring Indicator signal. Tie FORCEOFF and FORCEON together to bypass Auto-Shutdown so the line acts like a SHDN input.

Applications Information

Capacitor Selection

The capacitor type used for C1–C4 is not critical for proper operation; either polarized or nonpolarized capacitors may be used. The charge pump requires 0.1µF capacitors for 3.3V operation. For other supply voltages, refer to Table 3 for required capacitor values. Do not use values smaller than those listed in Table 3. Increasing the capacitor values (e.g., by a factor of 2) reduces ripple on the transmitter outputs and slightly reduces power consumption. C2, C3, and C4 can be increased without changing C1's value. **However, do not increase C1 without also increasing the values of C2, C3, and C4 to maintain the proper ratios (C1 to the other capacitors).**

When using the minimum required capacitor values, make sure the capacitor value does not degrade excessively with temperature. If in doubt, use capacitors with a larger nominal value. The capacitor's equivalent series resistance (ESR) usually rises at low temperatures and influences the amount of ripple on V+ and V-.

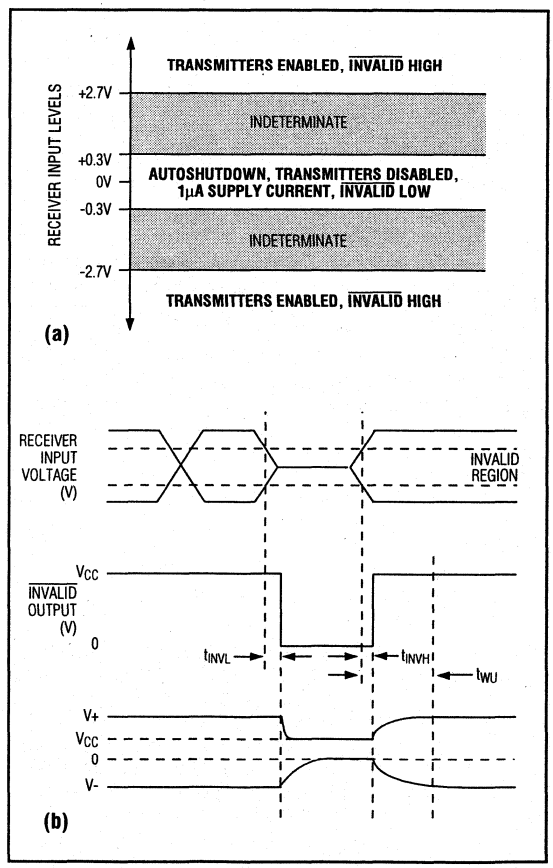


Figure 5. AutoShutdown Trip Levels

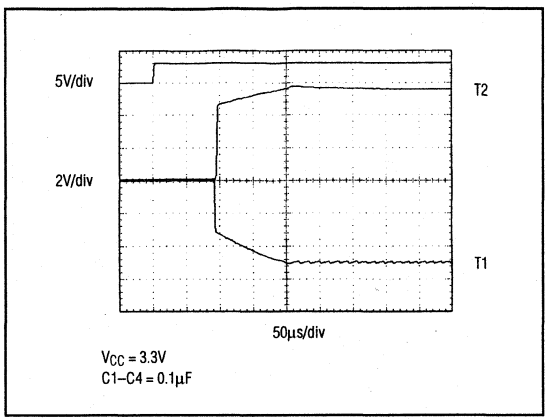


Figure 6. Transmitter Outputs when Exiting Shutdown or Powering Up

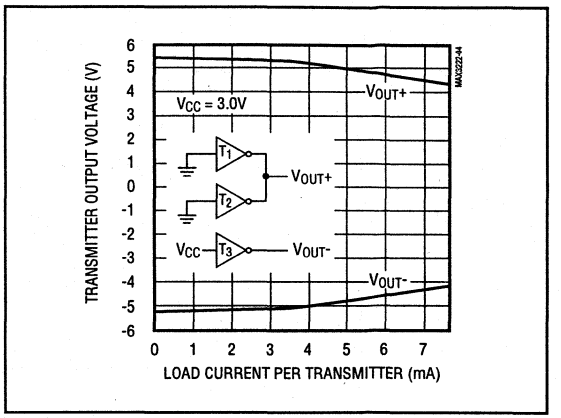


Figure 7a. MAX3243 Transmitter Output Voltage vs. Load Current per Transmitter

Power-Supply Decoupling

In most circumstances a 0.1µF bypass capacitor is adequate. In applications that are sensitive to power-supply noise, decouple VCC to ground with a capacitor of the same value as the charge-pump capacitor C1. Connect bypass capacitors as close to the IC as possible.

Transmitter Outputs when Exiting Shutdown

Figure 6 shows two transmitter outputs when exiting shutdown mode. As they become active, the two transmitter outputs are shown going to opposite RS-232 levels. Each transmitter is loaded with 3kΩ in parallel with 2500pF. The transmitter outputs display no ringing or undesirable transients as they come out of shutdown. Note that the transmitters are enabled only when the magnitude of V- exceeds approximately 3V. Figure 7a shows the MAX3243's transmitter output voltage vs. current per transmitter. Figure 7b is a mouse driver test circuit.

Mouse Driveability (MAX3243)

The MAX3243 has been specifically designed to power serial mice while operating from low-voltage power supplies. It has been tested with samples of ten major mouse models from six manufacturers including the leading three: Logitech (5 models), Mouse Systems, and Microsoft. The MAX3243 successfully drove all serial mice and met their respective current and voltage requirements. Figure 7a shows the transmitter outputs under increasing load current. The MAX3243's switching regulator ensures the transmitters will supply at least ±5V during worst-case conditions. The AutoShutdown feature does not work with a mouse, so $\overline{\text{FORCEOFF}}$ and FORCEON should be connected to VCC.

High Data Rates

The MAX3221/MAX3223/MAX3243 maintain the RS-232 ±5.0V minimum transmitter output voltage even at high data rates. Figure 8 shows a transmitter loopback test circuit. Figure 9 shows a loopback test result at 120kbps, and Figure 10 shows the same test at 240kbps. For Figure 9, all three transmitters were driven simultaneously at 120kbps into RS-232 loads in parallel with 1000pF. For Figure 10, a single transmitter was driven at 235kbps, but all three transmitters were loaded with an RS-232 receiver in parallel with 1000pF.

Interconnection with 3V and 5V Logic

The MAX3221/MAX3223/MAX3243 can directly interface with various 5V logic families, including ACT and HCT CMOS. See Table 4 for more information on possible combinations of interconnections.

1µA Supply Current, True +3V to +5.5V RS-232 Transceivers with AutoShutdown™

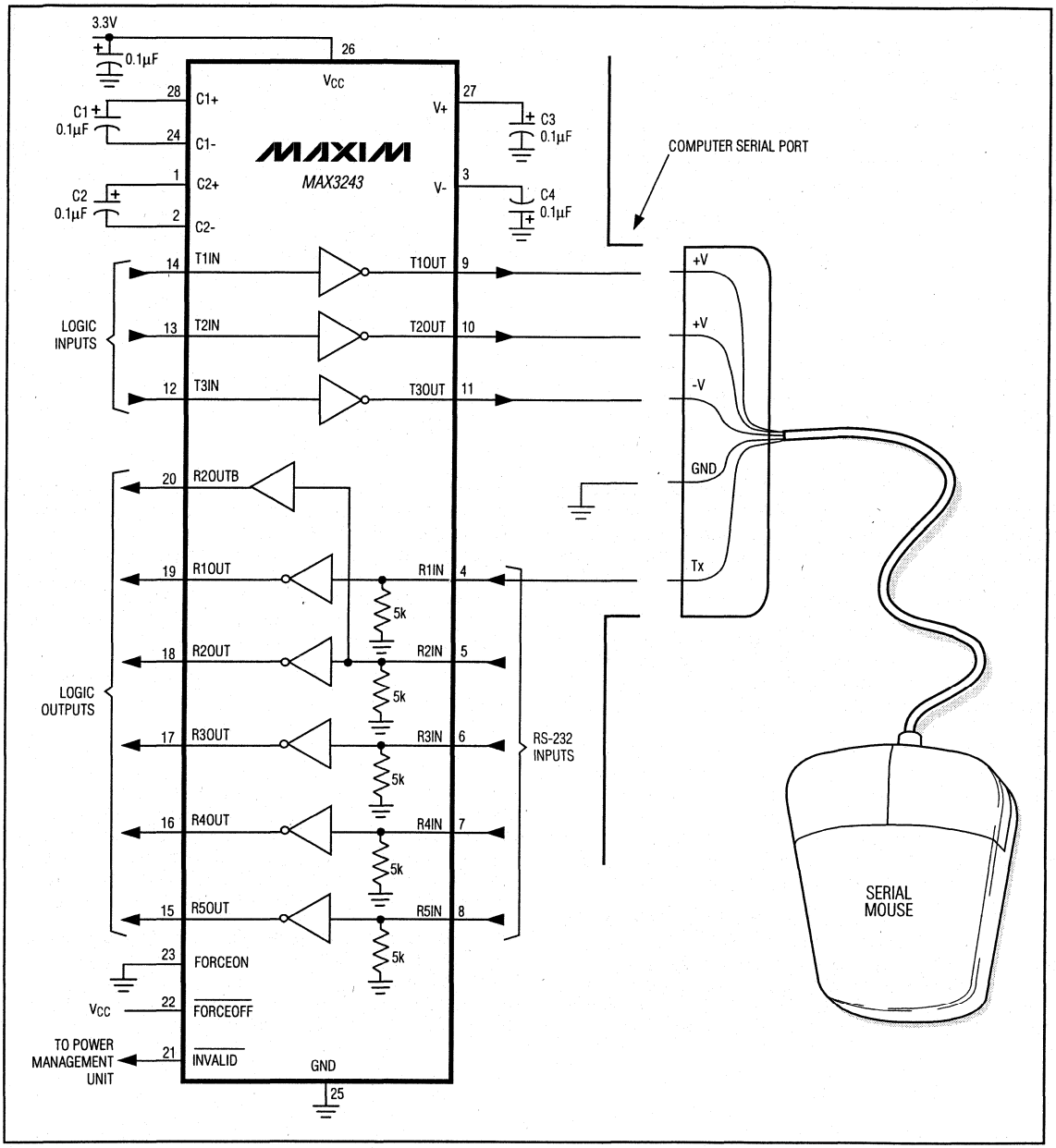


Figure 7b. Mouse Driver Test Circuit

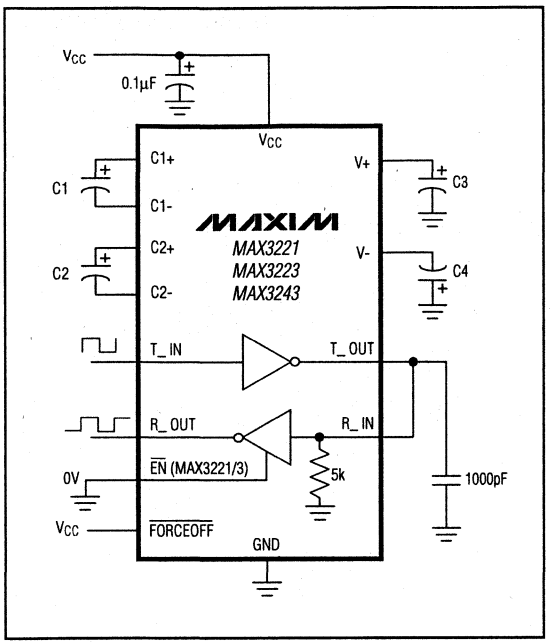


Figure 8. Loopback Test Circuit

Table 3. Required Capacitor Values

VCC (V)	C1 (µF)	C2, C3, C4 (µF)
3.0 to 3.6	0.1	0.1
4.5 to 5.5	0.047	0.33
3.0 to 5.5	0.1	0.47

Table 4. Logic Family Compatibility with Various Supply Voltages

SYSTEM POWER-SUPPLY VOLTAGE (V)	VCC SUPPLY VOLTAGE (V)	COMPATIBILITY
3.3	3.3	Compatible with all CMOS families.
5	5	Compatible with all TTL and CMOS-logic families.
5	3.3	Compatible with ACT and HCT CMOS, and with TTL. Incompatible with AC, HC, or CD4000 CMOS.

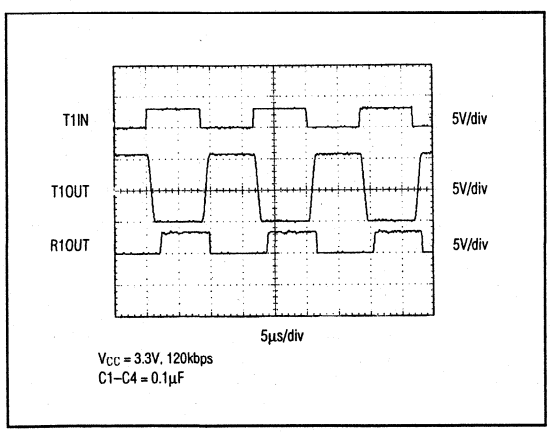


Figure 9. Loopback Test Result at 120kbps

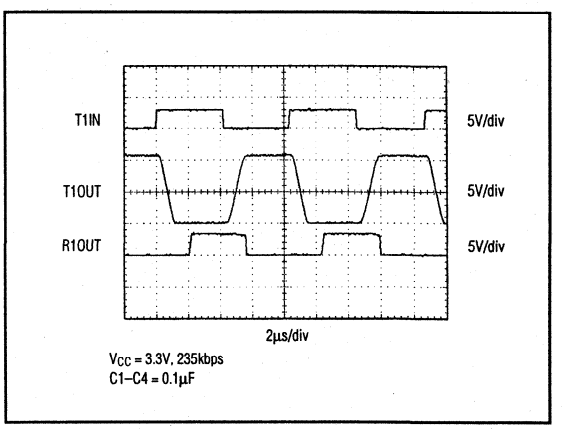
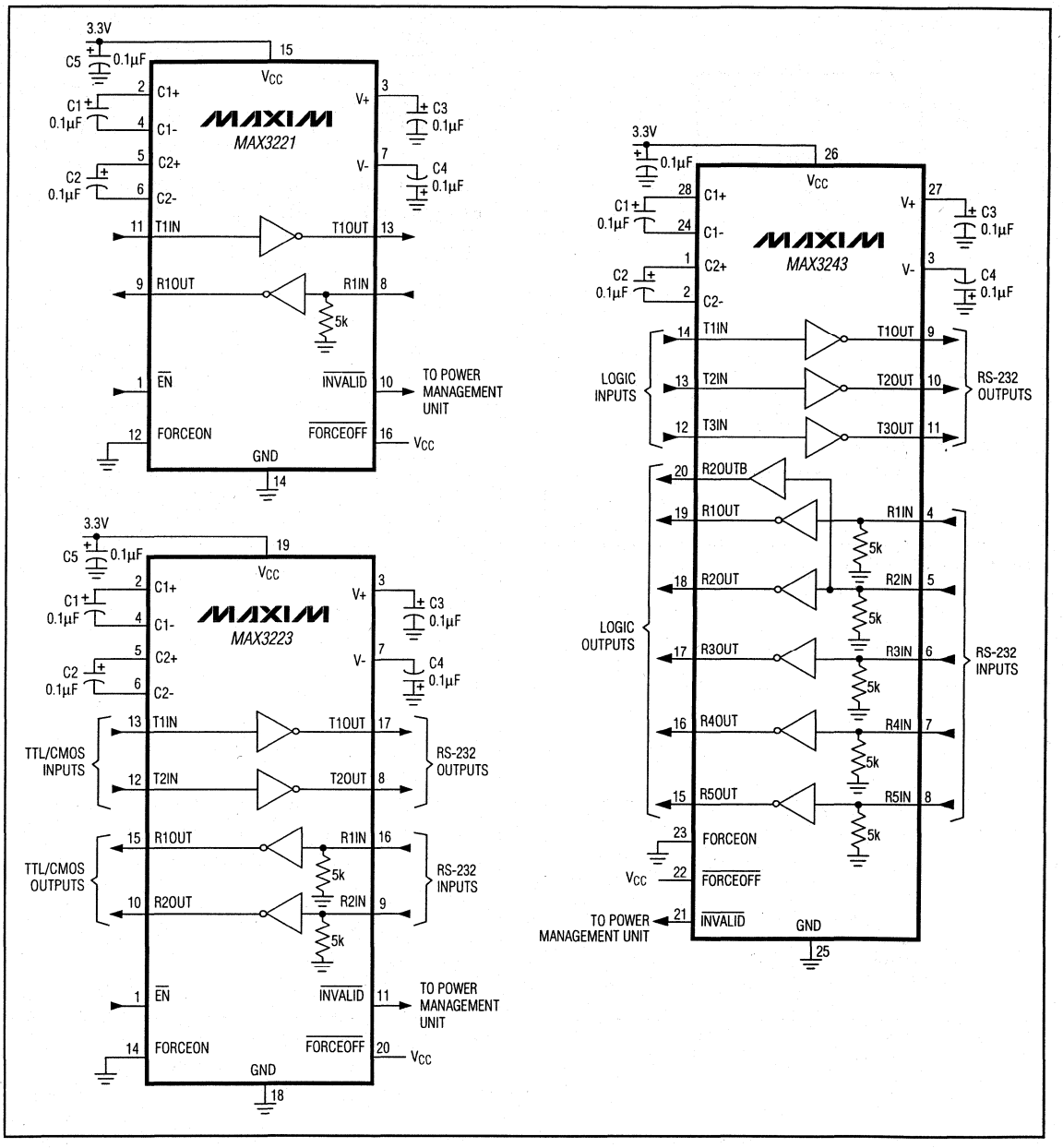


Figure 10. Loopback Test Result at 235kbps

1µA Supply Current, True +3V to +5.5V RS-232 Transceivers with AutoShutdown™

Typical Operating Circuits



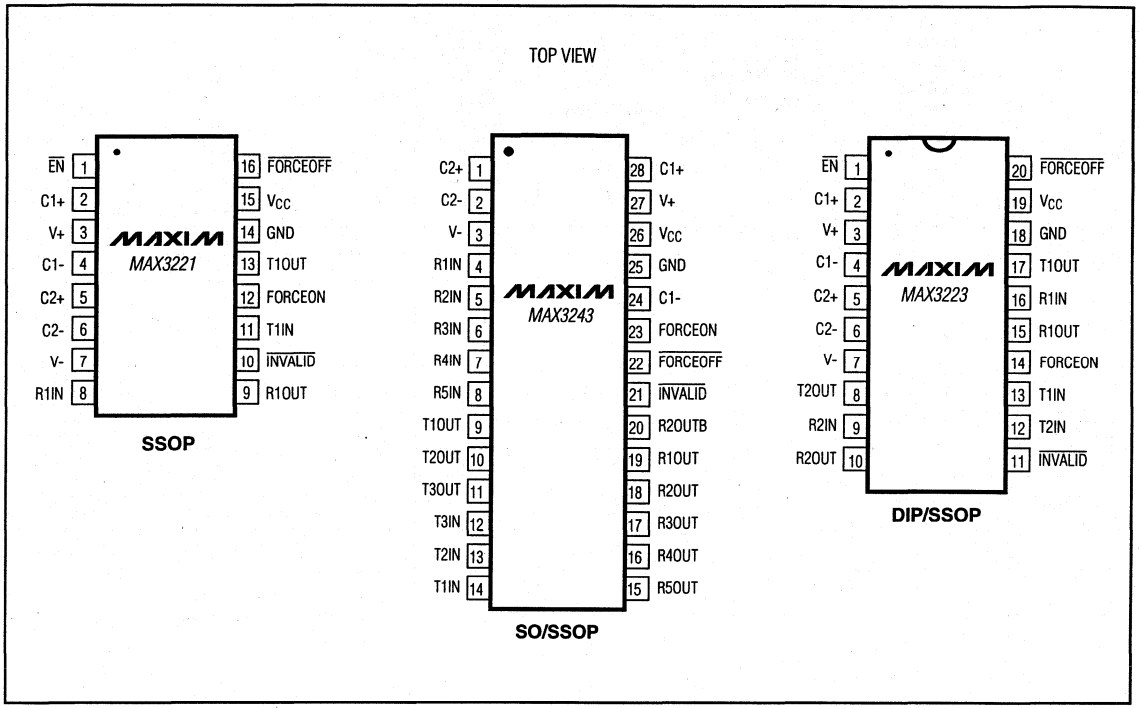
1µA Supply Current, True +3V to +5.5V RS-232 Transceivers with AutoShutdown™

3V-Powered EIA/TIA-232 and EIA/TIA-562 Transceivers from Maxim

PART	POWER-SUPPLY VOLTAGE (V)	No. OF TRANSMITTERS/ RECEIVERS	No. OF RECEIVERS ACTIVE IN SHUTDOWN	GUAR-ANTEED DATA RATE (kbps)	EIA/TIA-232 OR 562	FEATURES
MAX212	3.0 to 3.6	3/5	5	120	232	Drives mice
MAX218	1.8 to 4.25	2/2	2	120	232	Operates directly from batteries without a voltage regulator
MAX562	2.7 to 5.25	3/5	5	230	562	230kbps guaranteed data rate
MAX563	3.0 to 3.6	2/2	2	120	562	0.1µF capacitors
MAX3212	2.7 to 3.6	3/5	5	235	232	AutoShutdown, complementary receiver, drives mice, transient detection
MAX3221	3.0 to 5.5	1/1	1	120	232	0.1µF capacitors, 16-pin SSOP
MAX3222	3.0 to 5.5	2/2	2	120	232	0.1µF capacitors, MAX242 pinout
MAX3223	3.0 to 5.5	2/2	2	120	232	0.1µF capacitors, AutoShutdown
MAX3232	3.0 to 5.5	2/2	N/A	120	232	0.1µF capacitors, MAX232 pinout
MAX3241	3.0 to 5.5	3/5	5	120	232	0.1µF capacitors, 2 complementary receivers, drives mice
MAX3243	3.0 to 5.5	3/5	1	120	232	0.1µF capacitors, AutoShutdown complementary receiver, drives mice

1µA Supply Current, True +3V to +5.5V RS-232 Transceivers with AutoShutdown™

Pin Configurations



Chip Information

MAX3221
TRANSISTOR COUNT: 269

MAX3223
TRANSISTOR COUNT: 339

MAX3243
TRANSISTOR COUNT: 476

19-0273; Rev 4; 6/96

MAXIM

3.0V to 5.5V, Low-Power, up to 1Mbps, True RS-232 Transceivers Using Four 0.1µF External Capacitors

General Description

The MAX3222/MAX3232/MAX3237/MAX3241 transceivers have a proprietary low-dropout transmitter output stage enabling true RS-232 performance from a 3.0V to 5.5V supply with a dual charge pump. The devices require only four small 0.1µF external charge-pump capacitors. The MAX3222, MAX3232, and MAX3241 are guaranteed to run at data rates of 120kbps while maintaining RS-232 output levels. The MAX3237 is guaranteed to run at data rates of 250kbps in the normal operating mode and 1Mbps in the MegaBaud™ operating mode, while maintaining RS-232 output levels.

The MAX3222/MAX3232 have 2 receivers and 2 drivers. The MAX3222 features a 1µA shutdown mode that reduces power consumption and extends battery life in portable systems. Its receivers remain active in shutdown mode, allowing external devices such as modems to be monitored using only 1µA supply current. The MAX3222 and MAX3232 are pin, package, and functionally compatible with the industry-standard MAX242 and MAX232, respectively.

The MAX3241 is a complete serial port (3 drivers/5 receivers) designed for notebook and subnotebook computers. The MAX3237 (5 drivers/3 receivers) is ideal for fast modem applications. Both these devices feature a shutdown mode in which all receivers can remain active while using only 1µA supply current. Receivers R1 (MAX3237/MAX3241) and R2 (MAX3241) have extra outputs in addition to their standard outputs. These extra outputs are always active, allowing external devices such as a modem to be monitored without forward biasing the protection diodes in circuitry that may have V_{CC} completely removed.

The MAX3222, MAX3237, and MAX3241 are available in space-saving SSOP packages.

Applications

Notebook, Subnotebook, and Palmtop Computers

High-Speed Modems

Battery-Powered Equipment

Hand-Held Equipment

Peripherals

Printers

Typical Operating Circuits appear at end of data sheet.

Features

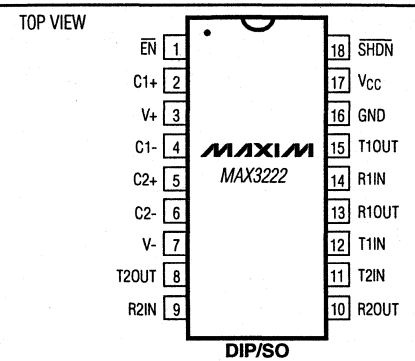
- **Low Supply Current:**
  300µA (MAX3222/MAX3232/MAX3241)
  500µA (MAX3237)
- **Guaranteed Data Rate:**
  120kbps (MAX3222/MAX3232/MAX3241)
  250kbps (MAX3237—Normal Operation)
  1Mbps (MAX3237—MegaBaud Operation)
- **1µA Low-Power Shutdown with Receivers Active (MAX3222/MAX3237/MAX3241)**
- **Flow-Through Pinout (MAX3237)**
- **Meets EIA/TIA-232 Specifications Down to 3.0V**
- **Guaranteed Mouse Driveability (MAX3241)**
- **Pin Compatible with Industry-Standard MAX232 (MAX3232)**
  Pin Compatible with Industry-Standard MAX242 (MAX3222)
- **Guaranteed Slew Rate:**
  6V/µs (MAX3222/MAX3232/MAX3237/MAX3241)
  24V/µs (MAX3237—MegaBaud Operation)

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3222CPN	0°C to +70°C	18 Plastic DIP
MAX3222CWN	0°C to +70°C	18 SO
MAX3222CAP	0°C to +70°C	20 SSOP

Ordering Information continued at end of data sheet.

Pin Configurations



Pin Configurations continued at end of data sheet.

MegaBaud is a trademark of Maxim Integrated Products.

*Covered by U.S. Patent numbers 4,636,930; 4,679,134; 4,777,577; 4,797,899; 4,809,152; 4,897,774; 4,999,761; and other patents pending.

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

3.0V to 5.5V, Low-Power, up to 1Mbps, True RS-232 Transceivers Using Four 0.1µF External Capacitors

ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... -0.3V to +6V
V+ (Note 1) ..... -0.3V to +7V
V- (Note 1) ..... +0.3V to -7V
V+ + V- (Note 1) ..... +13V
Input Voltages
T_IN, $\overline{SHDN}$, $\overline{EN}$ ..... -0.3V to +6V
MBAUD ..... -0.3V to (V_{CC} + 0.3V)
R_IN ..... ±25V
Output Voltages
T_OUT ..... ±13.2V
R_OUT ..... -0.3V to (V_{CC} + 0.3V)
Short-Circuit Duration
T_OUT ..... Continuous

Continuous Power Dissipation (T_A = +70°C)
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) ... 842mW
16-Pin Narrow SO (derate 8.70mW/°C above +70°C) 696mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) 762mW
18-Pin Plastic DIP (derate 11.11mW/°C above +70°C) .. 889mW
18-Pin SO (derate 9.52mW/°C above +70°C) 762mW
20-Pin SSOP (derate 8.00mW/°C above +70°C) 640mW
28-Pin SO (derate 12.50mW/°C above +70°C) 1W
28-Pin SSOP (derate 9.52mW/°C above +70°C) 762mW
Operating Temperature Ranges
MAX32_ _C_ _ ..... 0°C to +70°C
MAX32_ _E_ _ ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: V+ and V- can have a maximum magnitude of 7V, but their absolute difference cannot exceed 13V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +5.5V, C1–C4 = 0.1µF (Note 2), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
V_{CC} Power-Supply Current	No load, V_{CC} = 3.3V or 5.0V, T_A = +25°C	MAX3222/MAX3232/ MAX3241		0.3	1.0	mA
		MAX3237		0.5	2.0	
Shutdown Supply Current	SHDN = GND, T_A = +25°C			1.0	10	µA
LOGIC INPUTS AND RECEIVER OUTPUTS						
Input Logic Threshold Low (Note 3)	T_IN, $\overline{EN}$, $\overline{SHDN}$, MBAUD				0.8	V
Input Logic Threshold High (Note 3)	V_{CC} = 3.3V		2.0			V
	V_{CC} = 5.0V		2.4			
Input Leakage Current	T_IN, $\overline{EN}$, $\overline{SHDN}$, MBAUD			±0.01	±1.0	µA
Output Leakage Current	Receivers disabled			±0.05	±10	µA
Output Voltage Low	I_{OUT} = 1.6mA				0.4	V
Output Voltage High	I_{OUT} = -1.0mA		V_{CC} - 0.6	V_{CC} - 0.1		V
RECEIVER INPUTS						
Input Voltage Range			-25		25	V
Input Threshold Low	V_{CC} = 3.3V		0.6	1.2		V
	V_{CC} = 5.0V		0.8	1.5		
Input Threshold High	V_{CC} = 3.3V			1.5	2.4	V
	V_{CC} = 5.0V			1.8	2.4	
Input Hysteresis				0.3		V
Input Resistance	T_A = +25°C		3	5	7	kΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +5.5V, C1–C4 = 0.1µF (Note 2), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TRANSMITTER OUTPUTS					
Output Voltage Swing	All transmitter outputs loaded with 3kΩ to ground	±5.0	±5.4		V
Output Resistance	V_{CC} = V+ = V- = 0V, T_{OUT} = 2V	300	10M		Ω
Output Short-Circuit Current			±35	±60	mA
Output Leakage Current	V_{OUT} = 12V, V_{CC} = 0V to 5.5V, transmitters disabled			±25	µA
MOUSE DRIVEABILITY (MAX3241)					
Transmitter Output Voltage	T1IN = T2IN = GND, T3IN = V_{CC}, T3OUT loaded with 3kΩ to GND, T1OUT and T2OUT loaded with 2.5mA each	±5.0			V

TIMING CHARACTERISTICS—MAX3222/MAX3232/MAX3241

(V_{CC} = +3.0V to +5.5V, C1–C4 = 0.1µF (Note 2), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Maximum Data Rate	R_L = 3kΩ, C_L = 1000pF, one transmitter switching		120	235		kbps
Receiver Propagation Delay	R_IN to R_OUT, C_L = 150pF	t_{PHL}		0.3		µs
		t_{PLH}		0.3		
Receiver Output Enable Time	Normal operation			200		ns
Receiver Output Disable Time	Normal operation			200		ns
Transmitter Skew	$\lvert t_{PHL} - t_{PLH} \rvert$			300		ns
Receiver Skew	$\lvert t_{PHL} - t_{PLH} \rvert$			300		ns
Transition-Region Slew Rate	V_{CC} = 3.3V, R_L = 3Ω to 7kΩ, +3V to -3V or -3V to +3V, T_A = +25°C	C_L = 150pF to 1000pF	6		30	V/µs
		C_L = 150pF to 2500pF	4		30	

3.0V to 5.5V, Low-Power, up to 1Mbps, True RS-232 Transceivers Using Four 0.1µF External Capacitors

TIMING CHARACTERISTICS—MAX3237

(V_{CC} = +3.0V to +5.5V, C1–C4 = 0.1µF (Note 2), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Maximum Data Rate	R_L = 3kΩ, C_L = 1000pF, one transmitter switching, MBAUD = GND			250			kbps
	V_{CC} = 3.0V to 4.5V, R_L = 3kΩ, C_L = 250pF, one transmitter switching, MBAUD = V_{CC}			1000			
	V_{CC} = 4.5V to 5.5V, R_L = 3kΩ, C_L = 1000pF, one transmitter switching, MBAUD = V_{CC}			1000			
Receiver Propagation Delay	R_IN to R_OUT, C_L = 150pF	t_{PHL}			0.15		µs
		t_{PLH}			0.15		
Receiver Output Enable Time	Normal operation				200		ns
Receiver Output Disable Time	Normal operation				200		ns
Transmitter Skew	$\lvert t_{PHL} - t_{PLH} \rvert$, MBAUD = GND				100		ns
	$\lvert t_{PHL} - t_{PLH} \rvert$, MBAUD = V_{CC}				25		ns
Receiver Skew	$\lvert t_{PHL} - t_{PLH} \rvert$				50		ns
Transition-Region Slew Rate	V_{CC} = 3.3V, R_L = 3Ω to 7kΩ, +3V to -3V or -3V to +3V, T_A = +25°C	C_L = 150pF to 1000pF	MBAUD = GND	6		30	V/µs
			MBAUD = V_{CC}	24		150	
		C_L = 150pF to 2500pF, MBAUD = GND		4		30	

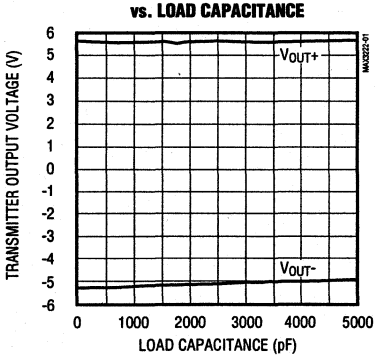
Note 2: MAX3222/MAX3232/MAX3241: C1–C4 = 0.1µF tested at 3.3V ±10%; C1 = 0.047µF, C2–C4 = 0.33µF tested at 5.0V ±10%. MAX3237: C1–C4 = 0.1µF tested at 3.3V ±5%; C1–C4 = 0.22µF tested at 3.3V ±10%; C1 = 0.047µF, C2–C4 = 0.33µF tested at 5.0V ±10%.

Note 3: Transmitter input hysteresis is typically 250mV.

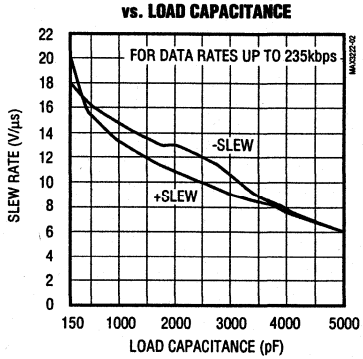
Typical Operating Characteristics

(V_{CC} = +3.3V, 235kbps data rate, 0.1µF capacitors, all transmitters loaded with 3kΩ, T_A = +25°C, unless otherwise noted.)

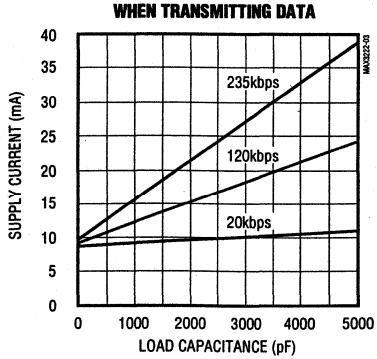
MAX3222/MAX3232
TRANSMITTER OUTPUT VOLTAGE vs. LOAD CAPACITANCE



MAX3222/MAX3232
SLEW RATE vs. LOAD CAPACITANCE



MAX3222/MAX3232
SUPPLY CURRENT vs. LOAD CAPACITANCE WHEN TRANSMITTING DATA

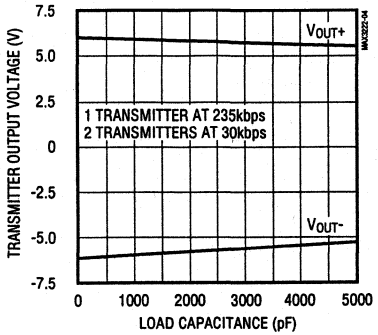


3.0V to 5.5V, Low-Power, up to 1Mbps, True RS-232 Transceivers Using Four 0.1µF External Capacitors

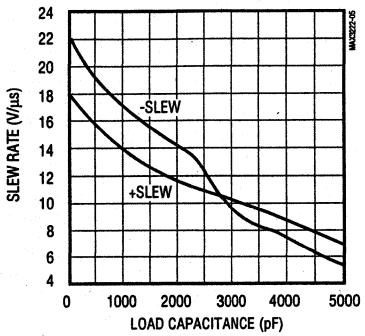
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, 235kbps data rate, 0.1µF capacitors, all transmitters loaded with 3kΩ, T_A = +25°C, unless otherwise noted.)

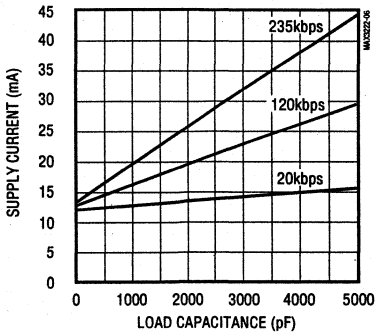
MAX3241
TRANSMITTER OUTPUT VOLTAGE vs. LOAD CAPACITANCE



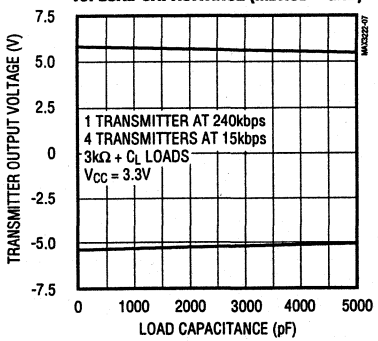
MAX3241
SLEW RATE vs. LOAD CAPACITANCE



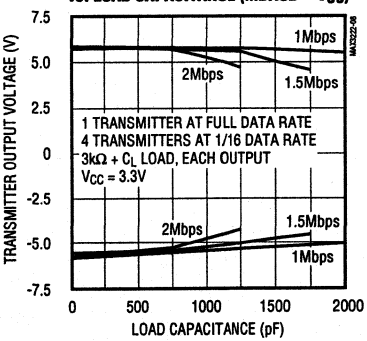
MAX3241
SUPPLY CURRENT vs. LOAD CAPACITANCE WHEN TRANSMITTING DATA



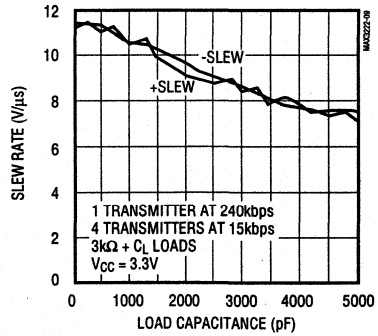
MAX3237
TRANSMITTER OUTPUT VOLTAGE vs. LOAD CAPACITANCE (MBAUD = GND)



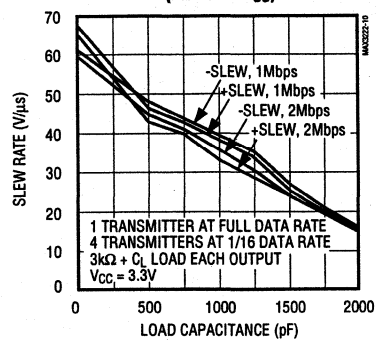
MAX3237
TRANSMITTER OUTPUT VOLTAGE vs. LOAD CAPACITANCE (MBAUD = VCC)



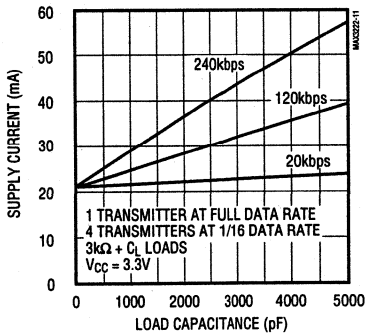
MAX3237
SLEW RATE vs. LOAD CAPACITANCE (MBAUD = GND)



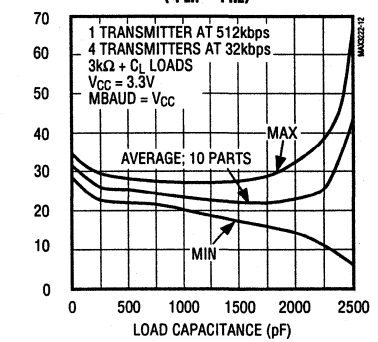
MAX3237
SLEW RATE vs. LOAD CAPACITANCE (MBAUD = VCC)



MAX3237
SUPPLY CURRENT vs. LOAD CAPACITANCE (MBAUD = GND)



MAX3237
SKEW vs. LOAD CAPACITANCE (t_{PLH} - t_{PHL})



3.0V to 5.5V, Low-Power, up to 1Mbps, True RS-232 Transceivers Using Four 0.1µF External Capacitors

Pin Description

PIN					NAME	FUNCTION
MAX3222		MAX3232	MAX3237	MAX3241		
DIP/SO	SSOP					
1	1	—	13	23	$\overline{EN}$	Receiver Enable. Active low.
2	2	1	28	28	C1+	Positive Terminal of Voltage-Doubler Charge-Pump Capacitor
3	3	2	27	27	V+	+5.5V Generated by the Charge Pump
4	4	3	25	24	C1-	Negative Terminal of Voltage-Doubler Charge-Pump Capacitor
5	5	4	1	1	C2+	Positive Terminal of Inverting Charge-Pump Capacitor
6	6	5	3	2	C2-	Negative Terminal of Inverting Charge-Pump Capacitor
7	7	6	4	3	V-	-5.5V Generated by the Charge Pump
8, 15	8, 17	7, 14	5, 6, 7, 10, 12	9, 10, 11	T_OUT	RS-232 Transmitter Outputs
9, 14	9, 16	8, 13	8, 9, 11	4–8	R_IN	RS-232 Receiver Inputs
10, 13	10, 15	9, 12	18, 20, 21	15–19	R_OUT	TTL/CMOS Receiver Outputs
11, 12	12, 13	10, 11	17, 19, 22, 23, 24	12, 13, 14	T_IN	TTL/CMOS Transmitter Inputs
16	18	15	2	25	GND	Ground
17	19	16	26	26	V_{CC}	+3.0V to +5.5V Supply Voltage
18	20	—	14	22	$\overline{SHDN}$	Shutdown Control. Active low.
—	11, 14	—	—	—	N.C.	No Connection
—	—	—	15	—	MBAUD	MegaBaud Control Input. Connect to GND for normal operation; connect to V_{CC} for 1Mbps transmission rates.
—	—	—	16	20, 21	R_OUTB	Noninverting Complementary Receiver Outputs. Always active.

3.0V to 5.5V, Low-Power, up to 1Mbps, True RS-232 Transceivers Using Four 0.1µF External Capacitors

Detailed Description

Dual Charge-Pump Voltage Converter

The MAX3222/MAX3232/MAX3237/MAX3241's internal power supply consists of a regulated dual charge pump that provides output voltages of +5.5V (doubling charge pump) and -5.5V (inverting charge pump), regardless of the input voltage (V_{CC}) over the 3.0V to 5.5V range. The charge pumps operate in a discontinuous mode; if the output voltages are less than 5.5V, the charge pumps are enabled, and if the output voltages exceed 5.5V, the charge pumps are disabled. Each charge pump requires a flying capacitor (C1, C2) and a reservoir capacitor (C3, C4) to generate the V+ and V- supplies.

RS-232 Transmitters

The transmitters are inverting level translators that convert CMOS-logic levels to 5.0V EIA/TIA-232 levels.

The MAX3222/MAX3232/MAX3241 transmitters guarantee a 120kbps data rate with worst-case loads of 3kΩ in parallel with 1000pF, providing compatibility with PC-to-PC communication software (such as LapLink™). Typically, these three devices can operate at data rates of 235kbps. Transmitters can be paralleled to drive multiple receivers or mice.

The MAX3222/MAX3237/MAX3241's output stage is turned off (high impedance) when the device is in shutdown mode. When the power is off, the MAX3222/MAX3232/MAX3237/MAX3241 permit the outputs to be driven up to ±12V.

The transmitter inputs do not have pull-up resistors. Connect unused inputs to GND or V_{CC}.

MAX3237 MegaBaud Operation

In normal operating mode (MBAUD = GND), the MAX3237 transmitters guarantee a 250kbps data rate with worst-case loads of 3kΩ in parallel with 1000pF. This provides compatibility with PC-to-PC communication software, such as Laplink™.

For higher speed serial communications, the MAX3237 features MegaBaud operation. In MegaBaud operating mode (MBAUD = V_{CC}), the MAX3237 transmitters guarantee a 1Mbps data rate with worst-case loads of 3kΩ in parallel with 250pF for 3.0V < V_{CC} < 4.5V. For 5V ±10% operation, the MAX3237 transmitters guarantee a 1Mbps data rate into worst-case loads of 3kΩ in parallel with 1000pF.

LapLink is a trademark of Traveling Software.

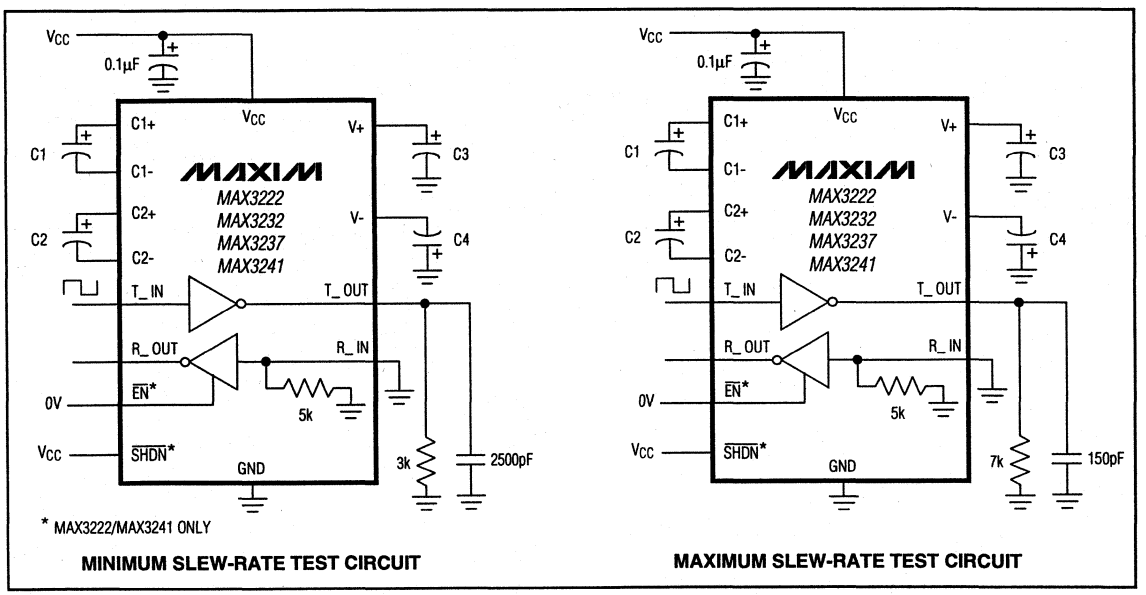


Figure 1. Slew-Rate Test Circuits

3.0V to 5.5V, Low-Power, up to 1Mbps, True RS-232 Transceivers Using Four 0.1µF External Capacitors

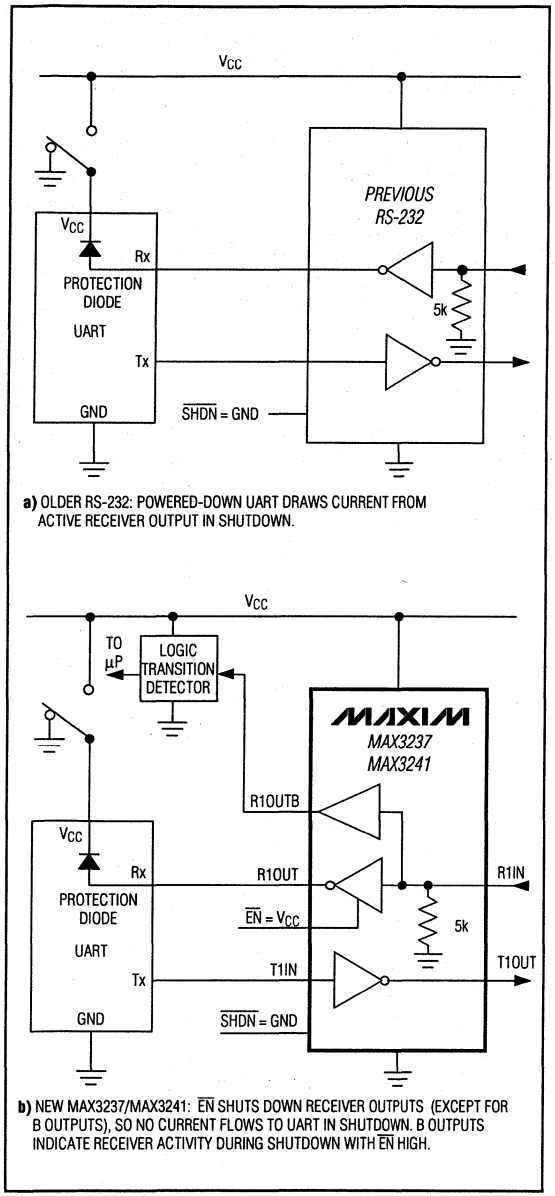


Figure 2. Detection of RS-232 Activity when the UART and Interface are Shut Down; Comparison of MAX3237/MAX3241 (b) with Previous Transceivers (a).

RS-232 Receivers

The receivers convert RS-232 signals to CMOS-logic output levels. The MAX3222/MAX3237/MAX3241 receivers have inverting three-state outputs. In shutdown, the receivers can be active or inactive (Table 1).

The complementary outputs on the MAX3237 (R1OUTB) and the MAX3241 (R1OUTB, R2OUTB) are always active, regardless of the state of $\overline{EN}$ or $\overline{SHDN}$. This allows for Ring Indicator applications without forward biasing other devices connected to the receiver outputs. This is ideal for systems where V_{CC} is set to 0V in shutdown to accommodate peripherals, such as UARTs (Figure 2).

MAX3222/MAX3237/MAX3241 Shutdown Mode

Supply current falls to less than 1µA in shutdown mode ($\overline{SHDN}$ = low). When shut down, the device's charge pumps are turned off, V+ is pulled down to V_{CC}, V- is pulled to ground, and the transmitter outputs are disabled (high impedance). The time required to exit shutdown is typically 100µs, as shown in Figure 3. Connect $\overline{SHDN}$ to V_{CC} if the shutdown mode is not used. $\overline{SHDN}$ has no effect on R_OUT or R_OUTB.

MAX3222/MAX3237/MAX3241 Enable Control

The inverting receiver outputs (R_OUT) are put into a high-impedance state when $\overline{EN}$ is high. The complementary outputs R1OUTB and R2OUTB are always active, regardless of the state of $\overline{EN}$ and $\overline{SHDN}$ (Table 1). $\overline{EN}$ has no effect on T_OUT.

Applications Information

Capacitor Selection

The capacitor type used for C1–C4 is not critical for proper operation; polarized or nonpolarized capacitors can be used. The charge pump requires 0.1µF capacitors for 3.3V operation. For other supply voltages, refer to Table 2 for required capacitor values. Do not use values smaller than those listed in Table 2. Increasing the capacitor values (e.g., by a factor of 2) reduces ripple on the transmitter outputs and slightly reduces power consumption. C2, C3, and C4 can be increased without changing C1's value. However, do not increase C1 without also increasing the values of C2, C3, and C4, to maintain the proper ratios (C1 to the other capacitors).

When using the minimum required capacitor values, make sure the capacitor value does not degrade excessively with temperature. If in doubt, use capacitors with a larger nominal value. The capacitor's equivalent series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V-.

Table 1. MAX3222/MAX3237/MAX3241 Shutdown and Enable Control Truth Table

SHDN	EN	T_OUT	R_OUT	R_OUTB (MAX3237/ MAX3241)
0	0	High-Z	Active	Active
0	1	High-Z	High-Z	Active
1	0	Active	Active	Active
1	1	Active	High-Z	Active

Table 2. Required Minimum Capacitor Values

VCC (V)	C1 (µF)	C2, C3, C4 (µF)
MAX3222/MAX3232/MAX3241		
3.0 to 3.6	0.1	0.1
4.5 to 5.5	0.047	0.33
3.0 to 5.5	0.1	0.47
MAX3237		
3.0 to 3.6	0.22	0.22
3.15 to 3.6	0.1	0.1
4.5 to 5.5	0.047	0.33
3.0 to 5.5	0.22	1.0

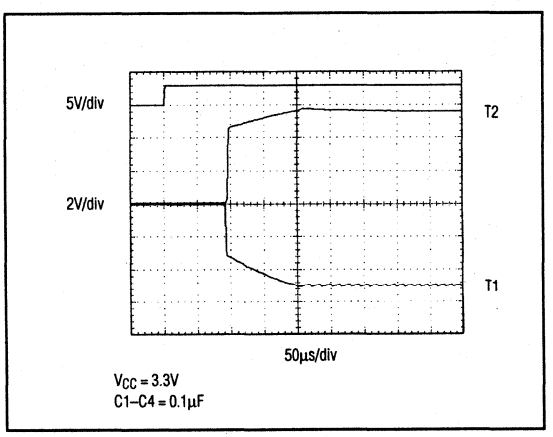


Figure 3. Transmitter Outputs when Exiting Shutdown or Powering Up

Power-Supply Decoupling

In most circumstances, a 0.1µF bypass capacitor is adequate. In applications that are sensitive to power-supply noise, decouple VCC to ground with a capacitor of the same value as charge-pump capacitor C1. Connect bypass capacitors as close to the IC as possible.

Operation Down to 2.7V

Transmitter outputs will meet EIA/TIA-562 levels of ±3.7V with supply voltages as low as 2.7V.

Transmitter Outputs when Exiting Shutdown

Figure 3 shows two transmitter outputs when exiting shutdown mode. As they become active, the two transmitter outputs are shown going to opposite RS-232 levels (one transmitter input is high, the other is low). Each transmitter is loaded with 3kΩ in parallel with 2500pF. The transmitter outputs display no ringing or undesirable transients as they come out of shutdown. Note that the transmitters are enabled only when the magnitude of V- exceeds approximately 3V.

Mouse Driveability

The MAX3241 has been specifically designed to power serial mice while operating from low-voltage power supplies. It has been tested with leading mouse brands from manufacturers such as Microsoft and Logitech. The MAX3241 successfully drove all serial mice tested and met their respective current and voltage requirements. Figure 4a shows the transmitter output voltages under increasing load current at 3.0V. Figure 4b shows a typical mouse connection using the MAX3241.

3.0V to 5.5V, Low-Power, up to 1Mbps, True RS-232 Transceivers Using Four 0.1µF External Capacitors

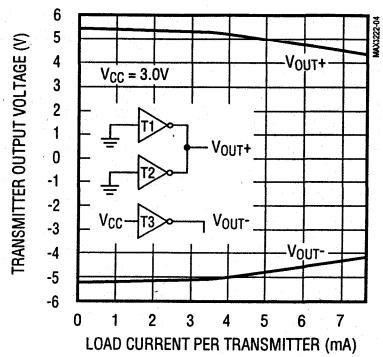


Figure 4a. MAX3241 Transmitter Output Voltage vs. Load Current per Transmitter

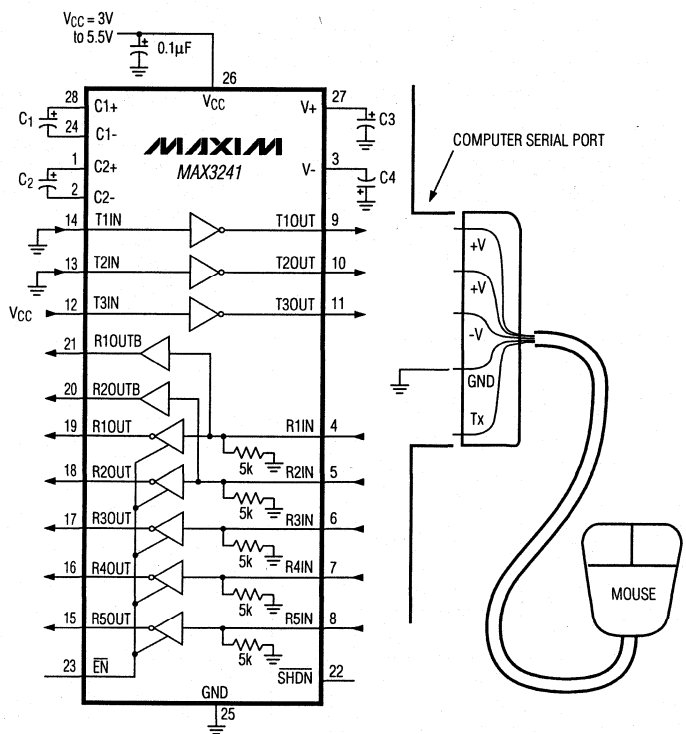


Figure 4b. Mouse Driver Test Circuit

3.0V to 5.5V, Low-Power, up to 1Mbps, True RS-232 Transceivers Using Four 0.1µF External Capacitors

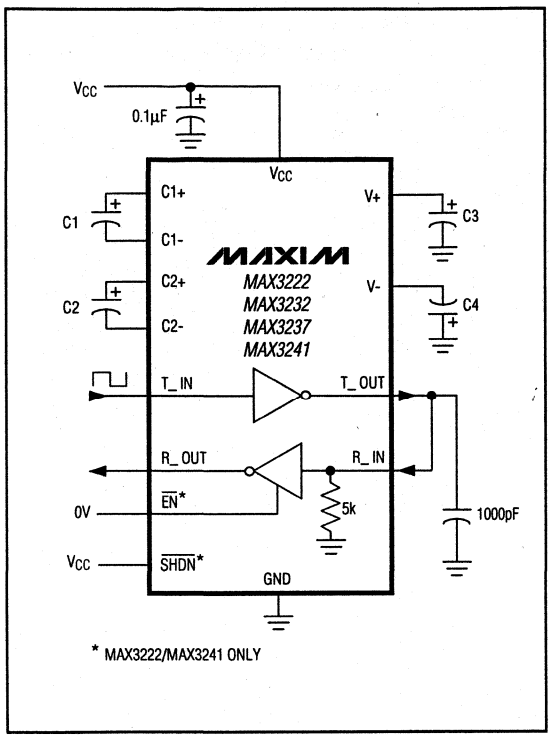


Figure 5. Loopback Test Circuit

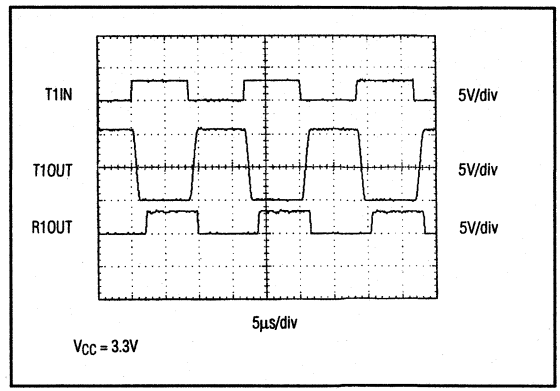


Figure 6. MAX3241 Loopback Test Result at 120kbps

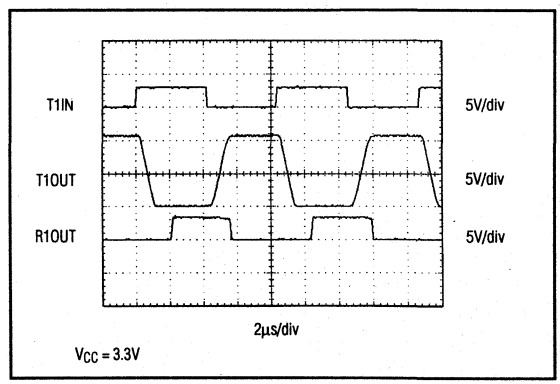


Figure 7. MAX3241 Loopback Test Result at 235kbps

High Data Rates

The MAX3222/MAX3232/MAX3241 maintain the RS-232 ±5.0V minimum transmitter output voltage even at high data rates. Figure 5 shows a transmitter loopback test circuit. Figure 6 shows a loopback test result at 120kbps, and Figure 7 shows the same test at 235kbps. For Figure 6, all transmitters were driven simultaneously at 120kbps into RS-232 loads in parallel with 1000pF. For Figure 7, a single transmitter was driven at 235kbps, and all transmitters were loaded with an RS-232 receiver in parallel with 1000pF.

The MAX3237 maintains the RS-232 ±5.0V minimum transmitter output voltage at data rates up to 1Mbps. Figure 8 shows a loopback test result at 1Mbps with MBAUD = VCC. For Figure 8, all transmitters were loaded with an RS-232 receiver in parallel with 250pF.

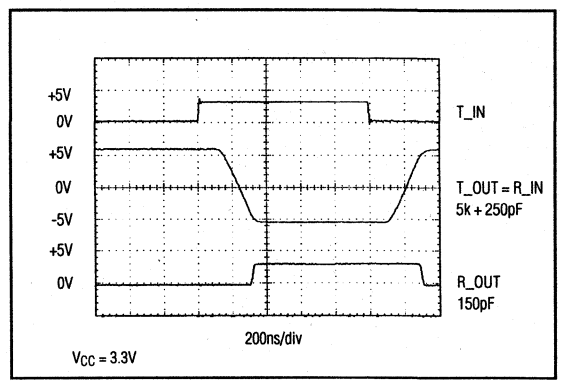


Figure 8. MAX3237 Loopback Test Result at 1000kbps (MBAUD = VCC)

3.0V to 5.5V, Low-Power, up to 1Mbps, True RS-232 Transceivers Using Four 0.1µF External Capacitors

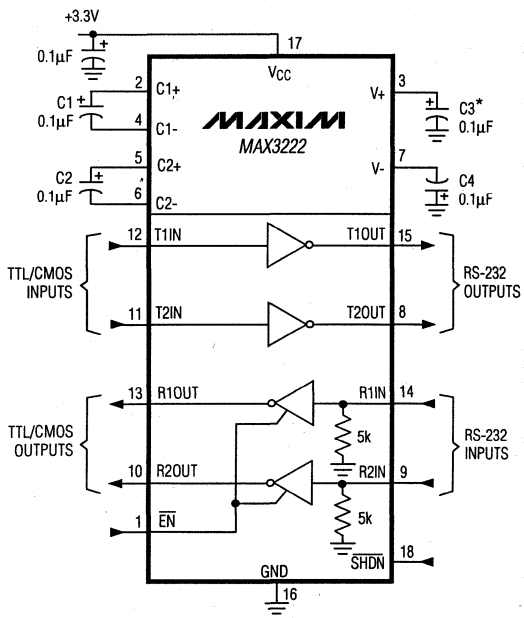
Interconnection with 3V and 5V Logic

The MAX3222/MAX3232/MAX3237/MAX3241 can directly interface with various 5V logic families, including ACT and HCT CMOS. See Table 3 for more information on possible combinations of interconnections.

Table 3. Logic-Family Compatibility with Various Supply Voltages

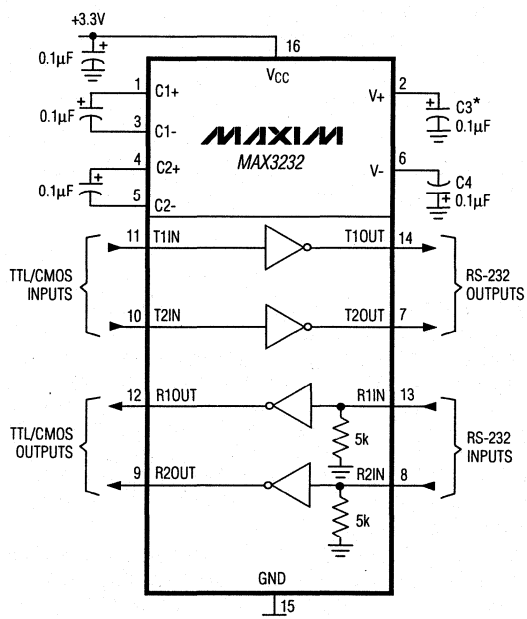
SYSTEM POWER-SUPPLY VOLTAGE (V)	MAX32__ VCC SUPPLY VOLTAGE (V)	COMPATIBILITY
3.3	3.3	Compatible with all CMOS families.
5	5	Compatible with all TTL and CMOS-logic families.
5	3.3	Compatible with ACT and HCT CMOS, and with TTL. Incompatible with AC, HC, and CD4000 CMOS.

Typical Operating Circuits



PIN NUMBERS REFER TO DIP/SO PACKAGES.

* C3 CAN BE RETURNED TO EITHER VCC OR GROUND.

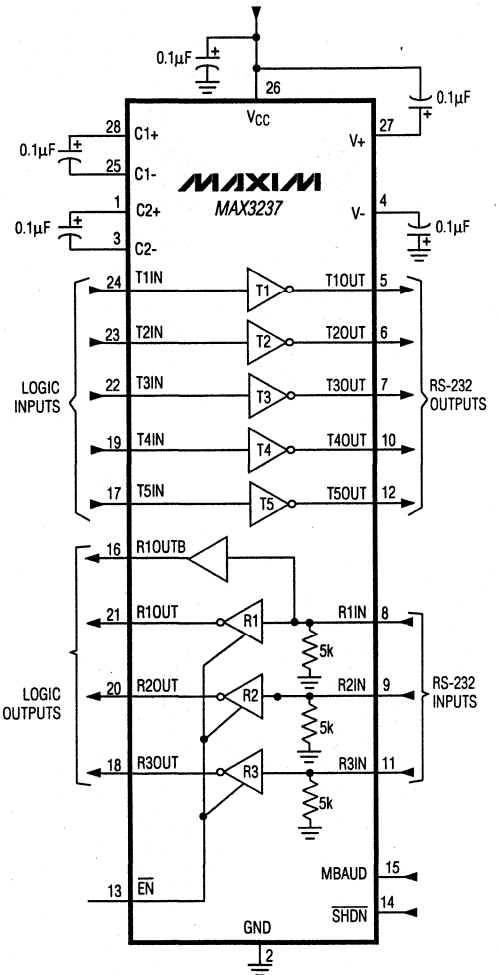


* C3 CAN BE RETURNED TO EITHER VCC OR GROUND.

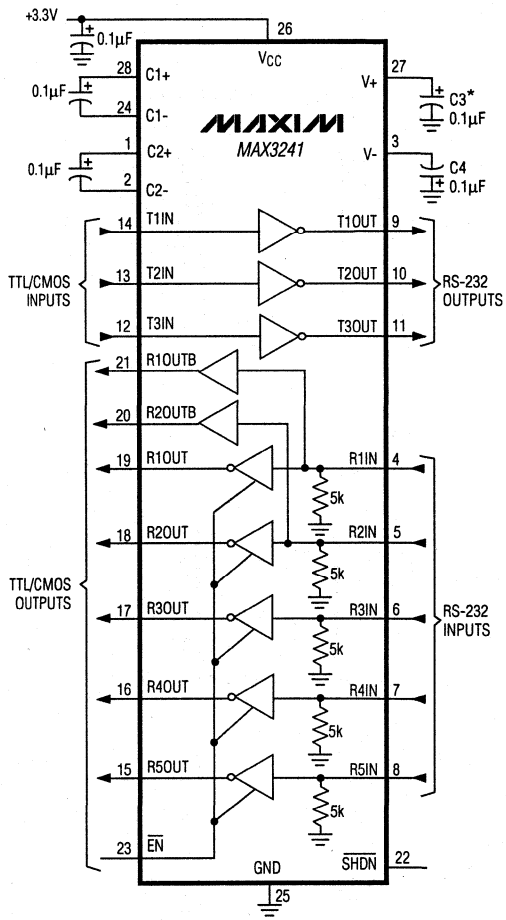
SEE TABLE 2 FOR CAPACITOR SELECTION

3.0V to 5.5V, Low-Power, up to 1Mbps, True RS-232 Transceivers Using Four 0.1µF External Capacitors

Typical Operating Circuits (continued)



* C3 CAN BE RETURNED TO EITHER V_{CC} OR GROUND.

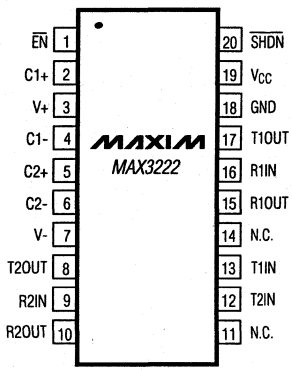


* C3 CAN BE RETURNED TO EITHER V_{CC} OR GROUND.

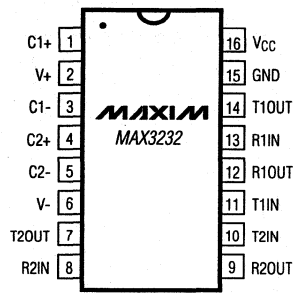
3.0V to 5.5V, Low-Power, up to 1Mbps, True RS-232 Transceivers Using Four 0.1µF External Capacitors

Pin Configurations (continued)

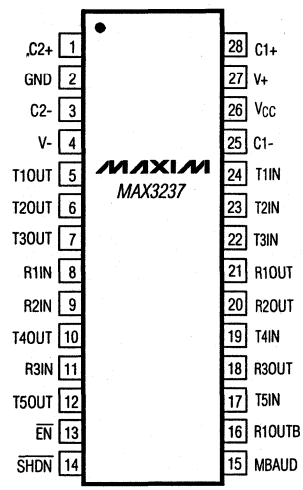
TOP VIEW



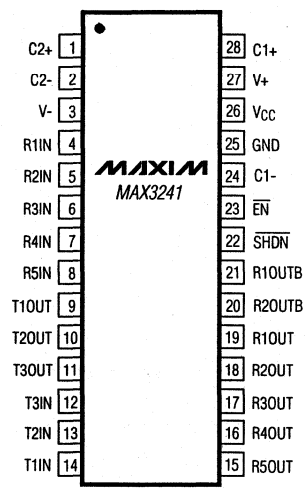
SSOP



DIP/SO



SSOP



SO/SSOP

3.0V to 5.5V, Low-Power, up to 1Mbps, True RS-232 Transceivers Using Four 0.1µF External Capacitors

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX3222C/D	0°C to +70°C	Dice*
MAX3222EPN	-40°C to +85°C	18 Plastic DIP
MAX3222EWN	-40°C to +85°C	18 SO
MAX3222EAP	-40°C to +85°C	20 SSOP
MAX3232CPE	0°C to +70°C	16 Plastic DIP
MAX3232CSE	0°C to +70°C	16 Narrow SO
MAX3232CWE	0°C to +70°C	16 Wide SO
MAX3232EPE	-40°C to +85°C	16 Plastic DIP
MAX3232ESE	-40°C to +85°C	16 Narrow SO
MAX3232EWE	-40°C to +85°C	16 Wide SO
MAX3237CAI	0°C to +70°C	28 SSOP
MAX3237EAI	-40°C to +85°C	28 SSOP
MAX3241CWI	0°C to +70°C	28 SO
MAX3241CAI	0°C to +70°C	28 SSOP
MAX3241EWI	-40°C to +85°C	28 SO
MAX3241EAI	-40°C to +85°C	28 SSOP

** Dice are tested at T_A = +25°C, DC parameters only.*

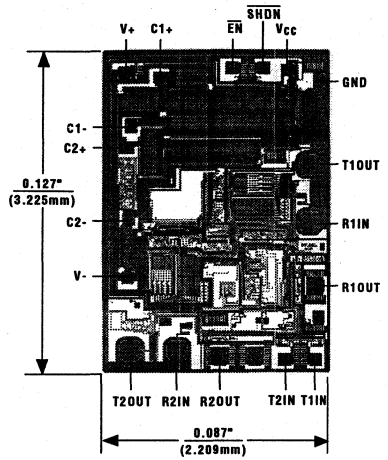
_____3V-Powered EIA/TIA-232 and EIA/TIA-562 Transceivers from Maxim

PART	POWER-SUPPLY VOLTAGE (V)	No. OF TRANSMITTERS/ RECEIVERS	No. OF RECEIVERS ACTIVE IN SHUTDOWN	GUAR-ANTEED DATA RATE (kbps)	EIA/ TIA-232 OR 562	FEATURES
MAX212	3.0 to 3.6	3/5	5	120	232	Drives mice
MAX218	1.8 to 4.25	2/2	2	120	232	Operates directly from batteries without a voltage regulator
MAX562	2.7 to 5.25	3/5	5	230	562	Wide supply range
MAX563	3.0 to 3.6	2/2	2	230	562	0.1µF capacitors
MAX3212	2.7 to 3.6	3/5	5	235	232	AutoShutdown, complementary receiver, drives mice, transient detection
MAX3222	3.0 to 5.5	2/2	2	120	232	0.1µF capacitors
MAX3223	3.0 to 5.5	2/2	2	120	232	0.1µF capacitors, AutoShutdown
MAX3232	3.0 to 5.5	2/2	N/A	120	232	0.1µF capacitors
MAX3237	3.0 to 5.5	5/3	3	250/1000	232	0.1µF capacitors, 1 complementary receiver, MegaBaud operation
MAX3241	3.0 to 5.5	3/5	5	120	232	0.1µF capacitors, 2 complementary receivers, drives mice
MAX3243	3.0 to 5.5	3/5	1	120	232	0.1µF capacitors, AutoShutdown, complementary receiver, drives mice

3.0V to 5.5V, Low-Power, up to 1Mbps, True RS-232 Transceivers Using Four 0.1µF External Capacitors

Chip Topography

MAX3222



TRANSISTOR COUNT: 339
SUBSTRATE CONNECTED TO GND

Chip Information

PART	TRANSISTOR COUNT
MAX3222	339
MAX3232	339
MAX3237	1212
MAX3241	894

19-1144; Rev 0; 9/96

MAXIM

+3.0V to +5.5V, 1µA, up to 250kbps, True RS-232 Transceiver with AutoShutdown Plus™

General Description

The MAX3238 true RS-232 transceiver achieves a 1µA supply current with Maxim's revolutionary AutoShutdown Plus feature. When the device does not sense a valid signal transition on either the receiver or transmitter inputs within 30sec, the on-board power supply and drivers shut down. This occurs if the RS-232 cable is disconnected or if the transmitters of the connected peripheral are inactive. The system turns on again when a valid transition is applied to any RS-232 receiver or transmitter input, saving power without changes to the existing BIOS or operating system.

The MAX3238 5-driver/3-receiver complete serial port is a 3V-powered EIA/TIA-232 and V.28/V.24 communications interface intended for notebook or subnotebook computer applications. A proprietary, high-efficiency, dual charge-pump power supply and a low-dropout transmitter combine to deliver true RS-232 performance from a single +3.0V to +5.5V supply. A guaranteed data rate of 250kbps provides compatibility with popular software for communicating with personal computers. The MAX3238 requires only 0.1µF capacitors in 3.3V operation. It is ideal for 3.3V-only systems, mixed 3.3V and 5.0V systems, or 5V-only systems that require true RS-232 performance.

Receiver R1 has an extra, always-active output (in addition to its standard output), which allows external devices, such as a modem, to be monitored without forward biasing the protection diodes in circuitry that may have V_{CC} completely removed.

The MAX3238 is available in a space-saving SSOP package.

Applications

Notebook, Subnotebook, and Palmtop Computers

High-Speed Modems

Battery-Powered Equipment

Hand-Held Equipment

Peripherals

Printers

Typical Operating Circuit appears at end of data sheet.

AutoShutdown Plus is a trademark of Maxim Integrated Products.
**Patents Pending*

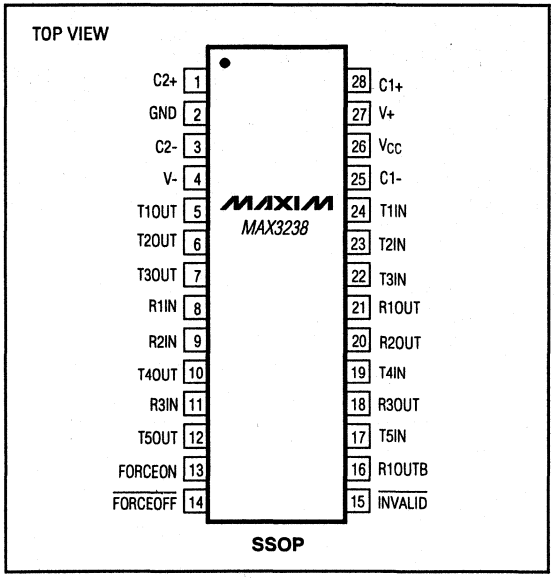
Features

- ♦ **1µA Supply Current Achieved with AutoShutdown Plus**
- ♦ **Guaranteed Data Rate: 250kbps**
- ♦ **1µA Low-Power Shutdown**
- ♦ **Receivers Active in AutoShutdown Plus Mode**
- ♦ **Flow-Through Pinout**
- ♦ **Meets EIA/TIA-232 Specifications Down to 3.0V**
- ♦ **Guaranteed 6V/µs Slew Rate**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3238CAI	0°C to +70°C	28 SSOP
MAX3238EAI	-40°C to +85°C	28 SSOP

Pin Configuration



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

+3.0V to +5.5V, 1µA, up to 250kbps, True RS-232 Transceiver with AutoShutdown Plus™

ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... -0.3V to +6V
V+ (Note 1) ..... -0.3V to +7V
V- (Note 1) ..... +0.3V to -7V
V+ + IV-I (Note 1) ..... +13V
Input Voltages
T_IN, $\overline{FORCEOFF}$, FORCEON ..... -0.3V to +6V
R_IN ..... ±25V
Output Voltages
T_OUT ..... ±13.2V
R_OUT, $\overline{INVALID}$ ..... -0.3V to (V_{CC} + 0.3V)

Short-Circuit Duration
T_OUT (one at a time) ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
SSOP (derate 9.52mW/°C above +70°C) 762mW
Operating Temperature Ranges
MAX3238CAI ..... 0°C to +70°C
MAX3238EAI ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: V+ and V- can have a maximum magnitude of +7V, but their absolute difference can not exceed +13V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +5.5V; C1–C4 = 0.1µF (tested at 3.3V ±5%), C1–C4 = 0.22µF (tested at 3.3V ±10%), C1 = 0.047µF and C2–C4 = 0.33µF (tested at 5.0V ±10%); T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS					
Supply Current, AutoShutdown Plus	V_{CC} = 3.3V or 5.0V, T_A = +25°C, receivers idle, transmitters idle, FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}		1.0	10	µA
Supply Current, Shutdown	$\overline{FORCEOFF}$ = GND, T_A = +25°C		1.0	10	µA
Supply Current, AutoShutdown Plus Disabled	FORCEON = $\overline{FORCEOFF}$ = V_{CC}, no load		0.5	2.0	mA
LOGIC INPUTS AND RECEIVER OUTPUTS					
Input Logic Threshold Low	T_IN, FORCEON, $\overline{FORCEOFF}$			0.8	V
Input Logic Threshold High	V_{CC} = 3.3V	2.0			V
	V_{CC} = 5.0V	2.4			
Input Leakage Current	T_IN, FORCEON, $\overline{FORCEOFF}$		±0.01	±1.0	µA
Output Leakage Current	Receivers disabled		±0.05	±10	µA
Output Voltage Low	I_{OUT} = 1.6mA			0.4	V
Output Voltage High	I_{OUT} = -1.0mA	V_{CC} - 0.6	V_{CC} - 0.1		V
RECEIVER INPUTS					
Input Voltage Range		-25		25	V
Input Threshold Low	V_{CC} = 3.3V	0.6	1.2		V
	V_{CC} = 5.0V	0.8	1.5		
Input Threshold High	V_{CC} = 3.3V		1.5	2.4	V
	V_{CC} = 5.0V		1.8	2.4	
Input Hysteresis			0.3		V
Input Resistance	T_A = +25°C	3	5	7	kΩ

+3.0V to +5.5V, 1µA, up to 250kbps, True RS-232 Transceiver with AutoShutdown Plus™

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +5.5V; C1–C4 = 0.1µF (tested at 3.3V ±5%), C1–C4 = 0.22µF (tested at 3.3V ±10%), C1 = 0.047µF and C2–C4 = 0.33µF (tested at 5.0V ±10%); T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
AutoShutdown (FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC})						
Receiver Input Threshold to $\overline{INVALID}$ Output High	Figure 7a	Positive threshold			2.7	V
		Negative threshold	-2.7			
Receiver Input Threshold to $\overline{INVALID}$ Output Low	Figure 4a		-0.3		0.3	V
$\overline{INVALID}$ Output Voltage Low	I_{OUT} = 1.6mA				0.4	V
$\overline{INVALID}$ Output Voltage High	I_{OUT} = -1.0mA		V_{CC} - 0.6			V
Receiver Positive or Negative Threshold to $\overline{INVALID}$ High (t_{INVH})	V_{CC} = 5V, Figure 4b			0.1		µs
Receiver Positive or Negative Threshold to $\overline{INVALID}$ Low (t_{INVL})	V_{CC} = 5V, Figure 4b			50		µs
Receiver or Transmitter Edge to Transmitters Enabled (t_{WU})	V_{CC} = 5V, Figure 4b (Note 2)			25		µs
Receiver or Transmitter Edge to Shutdown ($t_{AUTOSHDN}$)	Figure 4b (Note 2)		15	30	60	sec
TRANSMITTER OUTPUTS						
Output Voltage Swing	All transmitter outputs loaded with 3kΩ to ground		±5.0	±5.4		V
Output Resistance	V_{CC} = V+ = V- = GND, T_{OUT} = 2V		300	10M		Ω
Output Short-Circuit Current	V_{CC} ≤ 3.6V			±35	±60	mA
	V_{CC} > 3.6V			±40	±100	
Output Leakage Current	V_{OUT} = ±12V, V_{CC} = 0V to 5.5V, transmitters disabled				±25	µA
TIMING CHARACTERISTICS						
Maximum Data Rate	R_L = 3kΩ, C_L = 1000pF, one transmitter switching		250			kbps
Receiver Propagation Delay	R_IN to R_OUT, C_L = 150pF	t_{PHL}		0.15		µs
		t_{PLH}		0.15		
Receiver Output Enable Time	Normal operation			200		ns
Receiver Output Disable Time	Normal operation			200		ns
Transmitter Skew	$\lvert t_{PHL} - t_{PLH} \rvert$			100		ns
Receiver Skew	$\lvert t_{PHL} - t_{PLH} \rvert$			50		ns
Transition-Region Slew Rate	V_{CC} = 3.3V, T_A = +25°C, R_L = 3Ω to 7kΩ, measured from +3V to -3V or -3V to +3V	C_L = 150pF to 1000pF	6		30	V/µs
		C_L = 150pF to 2500pF	4		30	

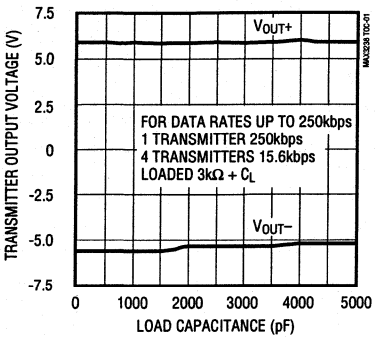
Note 2: A transmitter/receiver edge is defined as a transition through the transmitter/receiver input logic thresholds.

+3.0V to +5.5V, 1µA, up to 250kbps, True RS-232 Transceiver with AutoShutdown Plus™

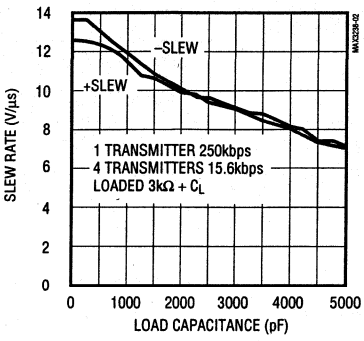
Typical Operating Characteristics

(V_{CC} = +3.3V, 250kbps data rate, 0.1µF capacitors, all transmitters loaded with 3kΩ, T_A = +25°C, unless otherwise noted.)

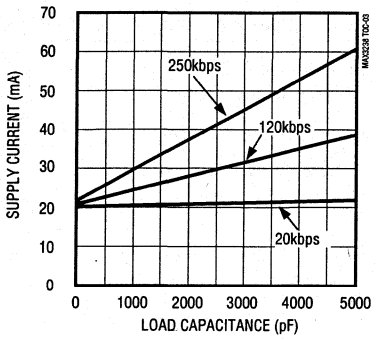
TRANSMITTER OUTPUT VOLTAGE vs. LOAD CAPACITANCE



SLEW RATE vs. LOAD CAPACITANCE



SUPPLY CURRENT vs. LOAD CAPACITANCE WHEN TRANSMITTING DATA



Pin Description

PIN	NAME	FUNCTION
1	C2+	Positive Terminal of Inverting Charge-Pump Capacitor
2	GND	Ground
3	C2-	Negative Terminal of Inverting Charge-Pump Capacitor
4	V-	-5.5V Generated by the Charge Pump
5, 6, 7, 10, 12	T_OUT	RS-232 Transmitter Outputs (T1OUT–T5OUT)
8, 9, 11	R_IN	RS-232 Receiver Inputs (R1IN–R3IN)
13	FORCEON	Force-Off Input. Drive high to override AutoShutdown Plus, keeping transmitters and receivers on ($\overline{\text{FORCEOFF}}$ must be high) (Table 1).
14	$\overline{\text{FORCEOFF}}$	Force-Off Input. Drive low to shut down transmitters, receivers (except R1OUTB), and on-board supply. This overrides AutoShutdown Plus and FORCEON (Table 1).
15	$\overline{\text{INVALID}}$	Output of the Valid Signal Detector. A logic "1" indicates if a valid RS-232 level is present on receiver inputs.
16	R1OUTB	Noninverting Complementary Receiver Output. Always active.
17, 19, 22, 23, 24	T_IN	TTL/CMOS Transmitter Inputs (T5IN–T1IN)
18, 20, 21	R_OUT	TTL/CMOS Receiver Outputs (R3OUT–R1OUT)
25	C1-	Negative Terminal of Voltage-Doubler Charge-Pump Capacitor
26	V_{CC}	+3.0V to +5.5V Supply Voltage
27	V+	+5.5V Generated by the Charge Pump
28	C1+	Positive Terminal of Voltage-Doubler Charge-Pump Capacitor

+3.0V to +5.5V, 1µA, up to 250kbps, True RS-232 Transceiver with AutoShutdown Plus™

Table 1. Output Control Truth Table

FORCEON	$\overline{\text{FORCEOFF}}$	AUTOSHUTDOWN PLUS*	OPERATION STATUS	T_OUT	R_OUT	R1OUTB
X	0	X	Shutdown (Forced Off)	High-Z	High-Z	Active
1	1	X	Normal Operation (Forced On)	Active	Active	Active
0	1	<30sec*	Normal Operation (AutoShutdown Plus)	Active	Active	Active
0	1	>30sec*	Shutdown (AutoShutdown Plus)	High-Z	Active	Active

X = Don't Care
** Time since last receiver or transmitter input transition.*

Detailed Description

Dual Charge-Pump Voltage Converter

The MAX3238's internal power supply consists of a regulated dual charge pump that provides output voltages of +5.5V (doubling charge pump) and -5.5V (inverting charge pump), regardless of the input voltage (V_{CC}) over the 3.0V to 5.5V range. The charge pumps operate in a discontinuous mode: if the output voltages are less than 5.5V, the charge pumps are enabled; if the output voltages exceed 5.5V, the charge pumps are disabled. Each charge pump requires a flying capacitor (C1, C2) and a reservoir capacitor (C3, C4) to generate the V+ and V- supplies.

RS-232 Transmitters

The transmitters are inverting level translators that convert CMOS-logic levels to 5.0V EIA/TIA-232 levels. The MAX3238 transmitters guarantee a 250kbps data rate with worst-case loads of 3kΩ in parallel with 1000pF, providing compatibility with PC-to-PC communication software (such as LapLink™). Transmitters can be paralleled to drive multiple receivers. Figure 1 shows a complete system connection.

When $\overline{\text{FORCEOFF}}$ is driven to ground, the transmitters and receivers are disabled and the outputs go high impedance, except for R1OUTB. When the AutoShutdown Plus circuitry senses that all receiver and transmitter inputs are inactive for more than 30sec, the transmitters are disabled and the outputs go into a high-impedance state, but the receivers remain active. When the power is off, the MAX3238 permits the outputs to be driven up to ±12V.

The transmitter inputs do not have pull-up resistors. Connect unused inputs to GND or V_{CC}.

RS-232 Receivers

The receivers convert RS-232 signals to CMOS-logic output levels. All receivers have inverting three-state outputs and are inactive in shutdown ($\overline{\text{FORCEOFF}}$) (Table 1). The MAX3238 also features an extra, always-active noninverting output, R1OUTB. This extra output monitors receiver activity while the other receivers are high impedance, allowing Ring Indicator to be monitored without forward biasing other devices connected to the receiver outputs. This is ideal for systems where V_{CC} is set to 0V in shutdown to accommodate peripherals, such as UARTs (Figure 2).

LapLink is a trademark of Traveling Software.

+3.0V to +5.5V, 1µA, up to 250kbps, True RS-232 Transceiver with AutoShutdown Plus™

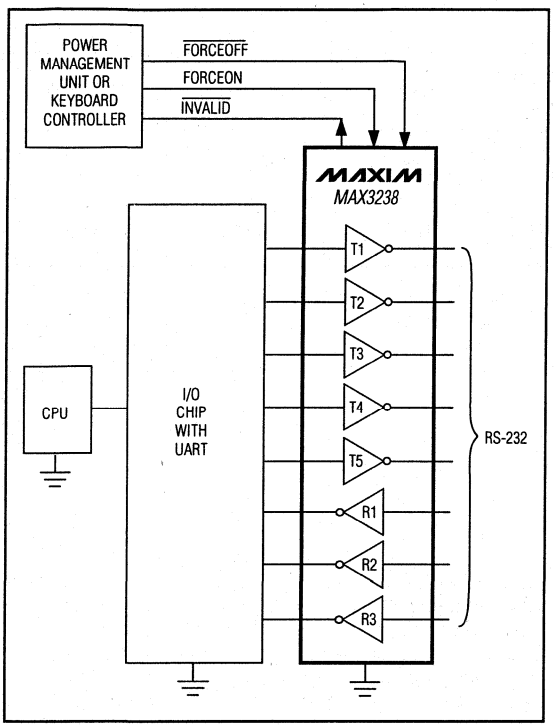


Figure 1. Interface Under Control of PMU

AutoShutdown Plus Mode

1µA supply current is achieved with Maxim's AutoShutdown Plus feature, which operates when FORCEOFF is low and FORCEON is high. When the MAX3238 senses no valid signal transitions on all receiver and transmitter inputs for 30sec, the on-board power supply and drivers are shut off, reducing supply current to 1µA. This occurs if the RS-232 cable is disconnected or if the connected peripheral transmitters are turned off. The system turns on again when a valid transition is applied to any RS-232 receiver or transmitter input. As a result, the system saves power without changes to the existing BIOS or operating system. The INVALID output is high when the receivers are active. Since INVALID indicates the receiver inputs' condition, it can be used in any mode (Figure 3).

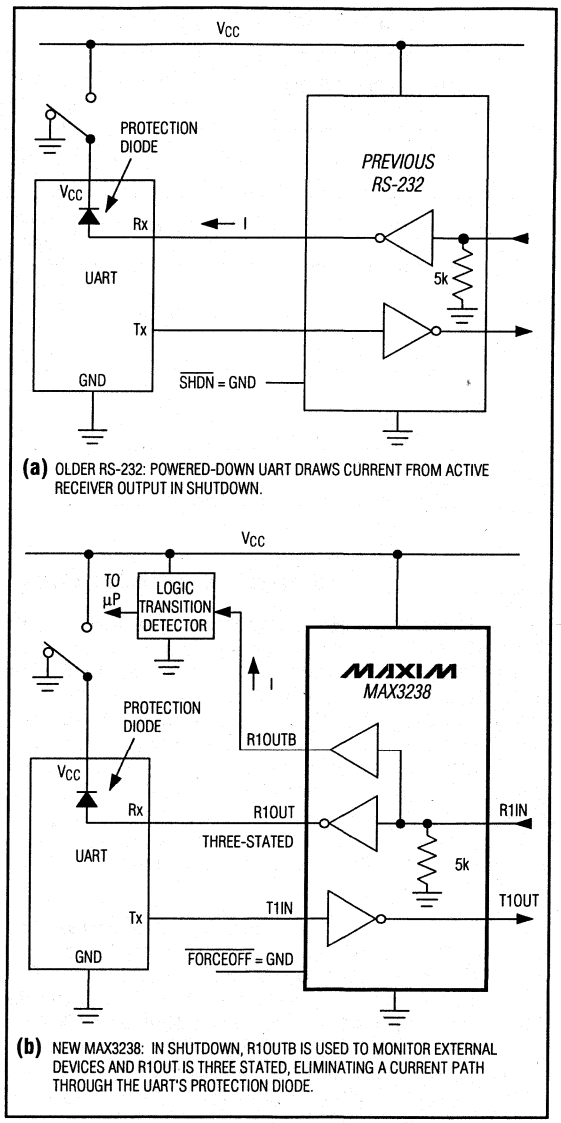


Figure 2. The MAX3238 detects RS-232 activity when the UART and interface are shut down.

Table 2. $\overline{\text{INVALID}}$ Truth Table

RS-232 SIGNAL PRESENT AT ANY RECEIVER INPUT	$\overline{\text{INVALID}}$ OUTPUT
Yes	H
No	L

Tables 1 and 2 and Figure 3 summarize the MAX3238's operating modes. FORCEON and $\overline{\text{FORCEOFF}}$ override the automatic circuitry and force the transceiver into its normal operating state or into its low-power standby state. When neither control is asserted, the IC enters AutoShutdown Plus mode and selects between these states automatically, based on the last receiver or transmitter input edge received.

When shut down, the device's charge pumps turn off, V+ decays to V_{CC}, V- decays to ground, and the transmitter outputs are disabled (high impedance). The time required to exit shutdown is typically 25µs (Figure 4b).

Software-Controlled Shutdown

If direct software control is desired, use $\overline{\text{INVALID}}$ to indicate DTR or Ring Indicator signal. Tie $\overline{\text{FORCEOFF}}$ and FORCEON together to bypass the AutoShutdown feature so the line acts like a $\overline{\text{SHDN}}$ input.

Applications Information

Capacitor Selection

The capacitor type used for C1–C4 is not critical for proper operation; polarized or nonpolarized capacitors can be used. The charge pump requires 0.1µF capacitors for 3.3V operation. For other supply voltages, see Table 3 for required capacitor values. Do not use values smaller than those listed in Table 3. Increasing the capacitor values (e.g., by a factor of 2) reduces ripple on the transmitter outputs and slightly reduces power consumption. C2, C3, and C4 can be increased without changing C1's value. However, **do not increase C1 without also increasing the values of C2, C3, C4, and C_{BYPASS},** to maintain the proper ratios (C1 to the other capacitors).

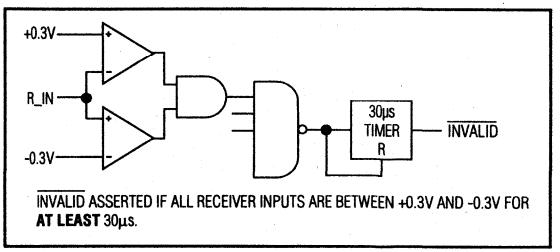


Figure 3a. $\overline{\text{INVALID}}$ Functional Diagram, $\overline{\text{INVALID}}$ Low

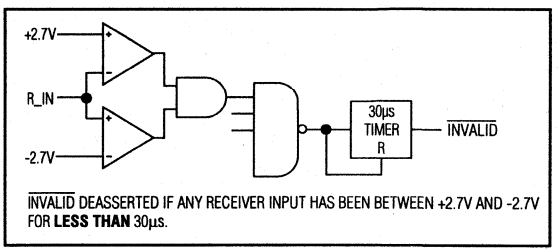


Figure 3b. $\overline{\text{INVALID}}$ Functional Diagram, $\overline{\text{INVALID}}$ High

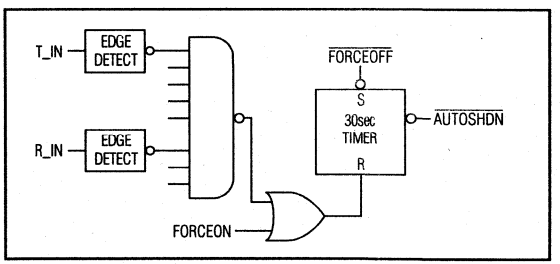


Figure 3c. AutoShutdown Plus Logic

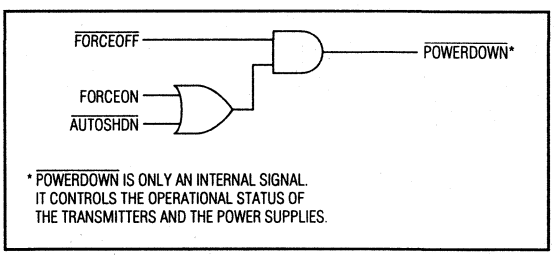


Figure 3d. Power-Down Logic

+3.0V to +5.5V, 1µA, up to 250kbps, True RS-232 Transceiver with AutoShutdown Plus™

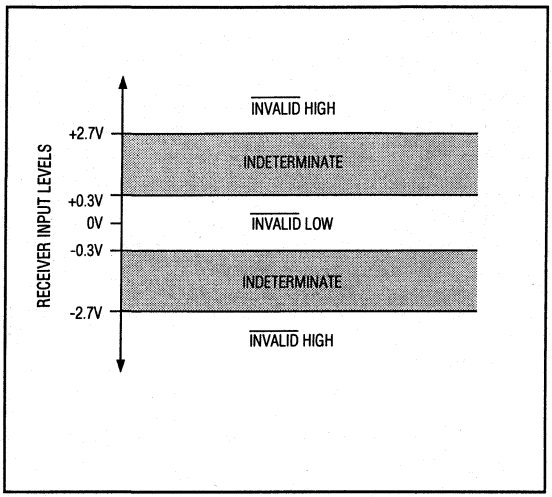


Figure 4a. Receiver Positive/Negative Thresholds for $\overline{INVALID}$

When using the minimum required capacitor values, make sure the capacitor value does not degrade excessively with temperature. If in doubt, use capacitors with a larger nominal value. The capacitor's equivalent series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V-.

Table 3. Required Minimum Capacitance Values

V_{CC} (V)	C1 (µF)	C2, C3, C4, C_{BYPASS} (µF)
3.0 to 3.6	0.22	0.22
3.15 to 3.6	0.1	0.1
4.5 to 5.5	0.047	0.33
3.0 to 5.5	0.22	1

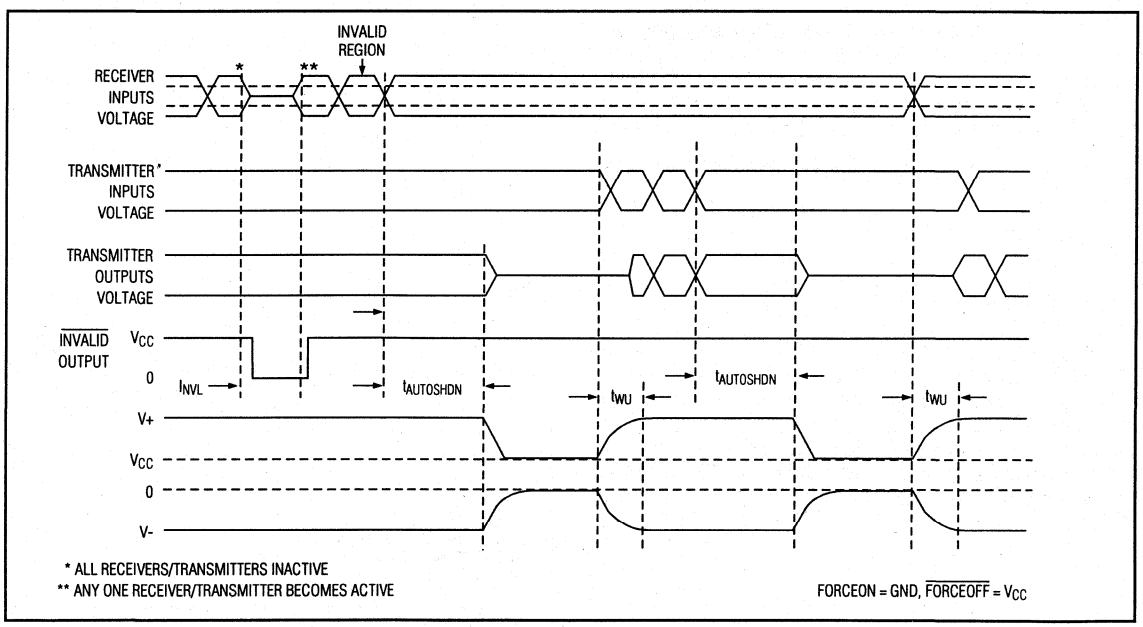


Figure 4b. AutoShutdown Plus and $\overline{INVALID}$ Timing Diagram

+3.0V to +5.5V, 1µA, up to 250kbps, True RS-232 Transceiver with AutoShutdown Plus™

Power-Supply Decoupling

In applications that are sensitive to power-supply noise, decouple V_{CC} to ground with a capacitor of the same value as capacitors C2, C3, and C4. Connect the bypass capacitor as close to the IC as possible.

Transmitter Outputs when Exiting Shutdown

Figure 5 shows two transmitter outputs when exiting shutdown mode. As they become active, the outputs are shown going to opposite RS-232 levels (one transmitter input is high, the other is low). Each transmitter is loaded with 3kΩ in parallel with 2500pF. The transmitter outputs display no ringing or undesirable transients as they come out of shutdown. Note that the transmitters are enabled only when the magnitude of V- exceeds approximately 3V.

High Data Rates

The MAX3238 maintains the RS-232 ±5.0V minimum transmitter output voltage even at high data rates. Figure 6 shows a transmitter loopback test circuit. Figure 7 shows a loopback test result at 120kbps, and Figure 8 shows the same test at 250kbps. For Figure 7, all transmitters were driven simultaneously at 120kbps into RS-232 loads in parallel with 1000pF. For Figure 8, a single transmitter was driven at 250kbps, and all transmitters were loaded with an RS-232 receiver in parallel with 1000pF.

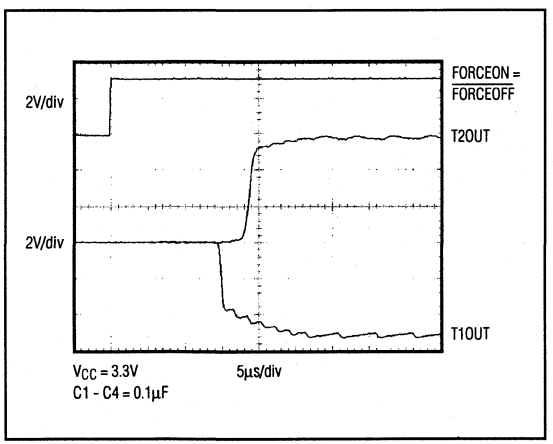


Figure 5. Transmitter Outputs when Exiting Shutdown or Powering Up

Interconnection with 3V and 5V Logic

The MAX3238 can directly interface with various 5V-logic families, including ACT and HCT CMOS. See Table 4 for more information on possible combinations of interconnections.

Table 4. Logic Family Compatibility with Various Supply Voltages

SYSTEM POWER-SUPPLY VOLTAGE (V)	V_{CC} SUPPLY VOLTAGE (V)	COMPATIBILITY
3.3	3.3	Compatible with all CMOS families.
5	5	Compatible with all TTL and CMOS families.
5	3.3	Compatible with ACT and HCT CMOS, and with AC, HC, or CD4000 CMOS.

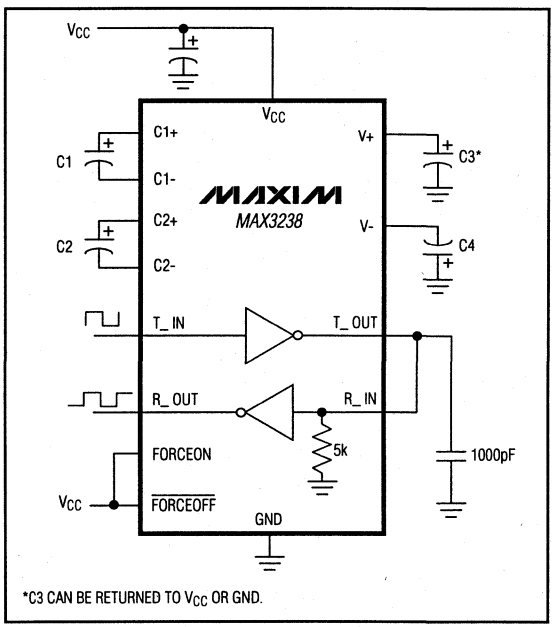


Figure 6. Loopback Test Circuit

+3.0V to +5.5V, 1µA, up to 250kbps, True RS-232 Transceiver with AutoShutdown Plus™

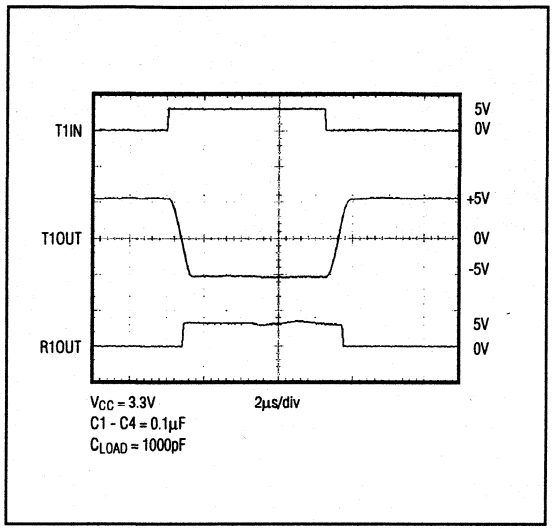


Figure 7. Loopback Test Result at 120kbps

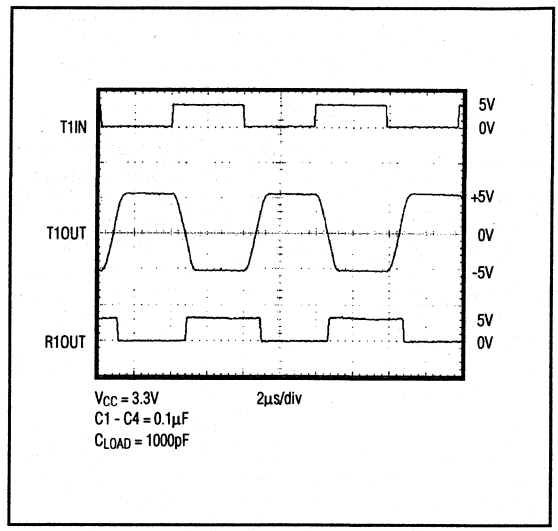


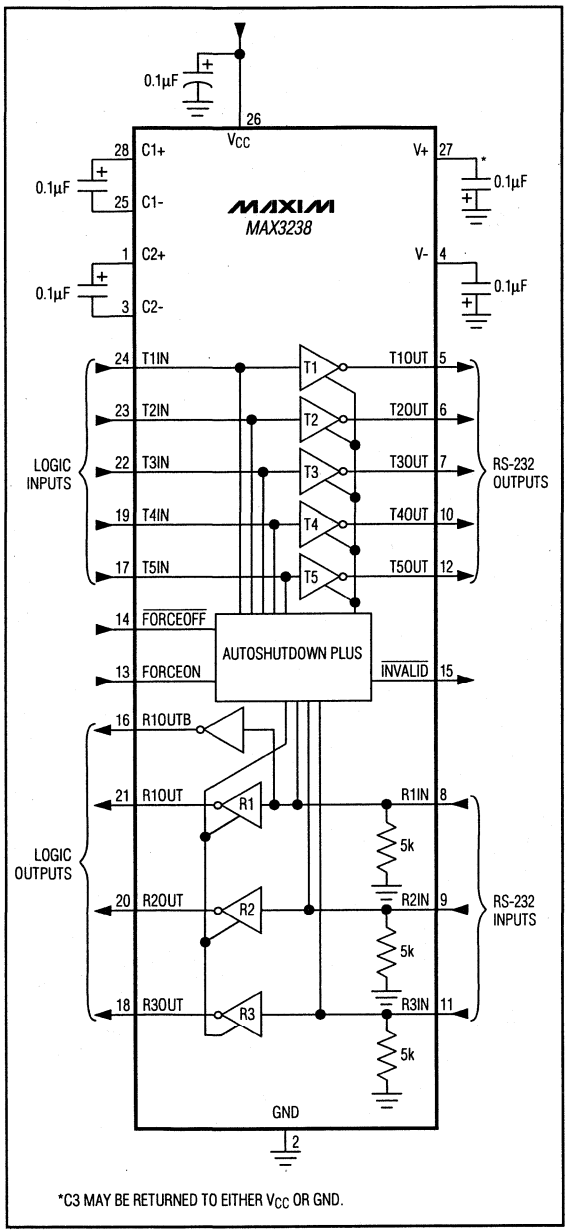
Figure 8. Loopback Test Result at 250kbps

Chip Information

TRANSISTOR COUNT: 1404

+3.0V to +5.5V, 1µA, up to 250kbps, True RS-232 Transceiver with AutoShutdown Plus™

Typical Operating Circuit



*C3 MAY BE RETURNED TO EITHER V_{CC} OR GND.

19-0453; Rev 0; 1/96

MAXIM

Complete, Isolated, 3.3V RS-485/RS-422 Data Interface

General Description

The MAX3480A/MAX3480B are electrically isolated RS-485/RS-422 data-communications interfaces. Transceivers, optocouplers, and a transformer are all included in one low-cost, 28-pin DIP package. A single +3.3V supply on the logic side powers both sides of the interface.

The MAX3480B features reduced-slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free data transmission at data rates up to 250kbps. The MAX3480A's driver slew rate is not limited, allowing transmission rates up to 2.5Mbps.

These devices typically draw 180mA of quiescent supply current. The MAX3480B provides a low-power shutdown mode in which it consumes only 0.2µA.

Drivers are short-circuit current limited and are protected against excessive power dissipation by thermal shutdown circuitry that places the driver outputs into a high-impedance state. The receiver input has a fail-safe feature that guarantees a logic-high output if the input is open circuit.

The MAX3480A/MAX3480B typically withstand 1600V_{RMS} (1 minute) or 2000V_{RMS} (1 second). Their isolated inputs and outputs meet RS-485/RS-422 specifications.

Applications

Isolated RS-485/RS-422 Data Interface
Transceivers for EMI-Sensitive Applications
Industrial-Control Local Area Networks
Automatic Test Equipment
HVAC/Building Control Networks

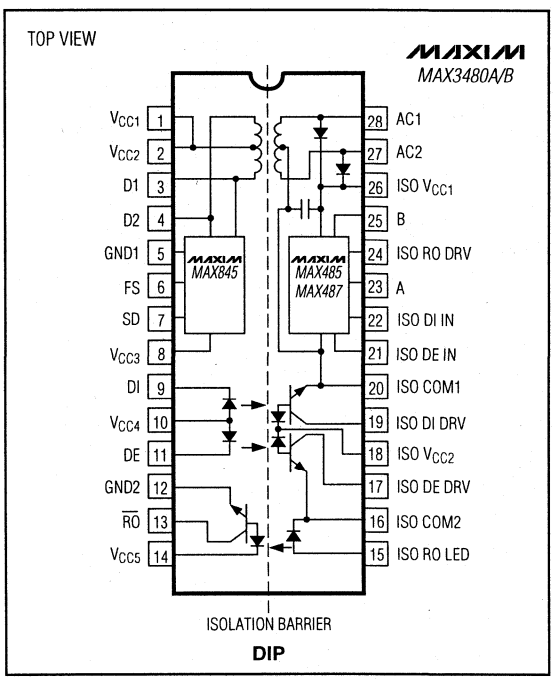
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	DATA RATE (kbps)
MAX3480ACPI	0°C to +70°C	28 Plastic DIP	2500
MAX3480AEPI	-40°C to +85°C	28 Plastic DIP	2500
MAX3480BCPI	0°C to +70°C	28 Plastic DIP	250
MAX3480BEPI	-40°C to +85°C	28 Plastic DIP	250

Features

- ♦ **Isolated Data Interface to 1600V_{RMS} (1 minute)**
- ♦ **Slew-Rate-Limited Data Transmission (MAX3480B)**
- ♦ **High-Speed, Isolated, 2.5Mbps RS-485 Interface (MAX3480A)**
- ♦ **-7V to +12V Common-Mode Input Voltage Range with Respect to Isolated Ground**
- ♦ **Single +3.3V Supply**
- ♦ **Current Limiting and Thermal Shutdown for Driver Overload Protection**
- ♦ **Standard 28-Pin DIP Package**

Pin Configuration



DIP

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Complete, Isolated, 3.3V RS-485/RS-422 Data Interface

ABSOLUTE MAXIMUM RATINGS

With Respect to GND:
- Supply Voltage (V_{CC1}, V_{CC2}, V_{CC4}, V_{CC5}) .....-0.3V to +3.8V
- Supply Voltage (V_{CC3}) .....-0.3V to +7V
- Control Input Voltage (SD, FS) .....-0.3V to (V_{CC} + 0.3V)
- Receiver Output Voltage ($\overline{RO}$).....-0.3V to (V_{CC} + 0.3V)

With Respect to ISO COM:
- Control Input Voltage (ISO DE _) .....-0.3V to (ISO V_{CC} + 0.3V)
- Driver Input Voltage (ISO DI _).....-0.3V to (ISO V_{CC} + 0.3V)
- Receiver Output Voltage (ISO RO _).....-0.3V to (ISO V_{CC} + 0.3V)
- Driver Output Voltage (A, B).....-8V to +12.5V
- Receiver Input Voltage (A, B).....-8V to +12.5V

LED Forward Current (DI, DE, ISO RO LED) 50mA
Continuous Power Dissipation (T_A = +70°C)
- Plastic DIP (derate 9.09mW/°C above +70°C) 727mW

Operating Temperature Ranges
- MAX3480_CPI .....0°C to +70°C
- MAX3480_EPI .....-40°C to +85°C

Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = V_{CC1} = V_{CC2} = V_{CC4} = V_{CC5} = 3.0V to 3.6V, FS = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = V_{CC1} = V_{CC2} = V_{CC4} = V_{CC5} = 3.3V and T_A = +25°C.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V_S			3.0	3.3	3.6	V
Switch Frequency	f_{SWL}	FS = 0V			600		kHz
	f_{SWH}	FS = V_{CC} or open			900		
Operating Supply Current	I_{CC}	MAX3480A, DE´ = V_{CC} or open	R_L = ∞		180	260	mA
			R_L = 54Ω		280		
		MAX3480B, DE´ = V_{CC} or open	R_L = ∞		120	200	
			R_L = 54Ω		240		
Shutdown Supply Current (Note 3)	I_{SHDN}	SD = V_{CC3}			0.2		µA
FS Input Threshold	V_{FSH}	High		2.4			V
	V_{FSL}	Low				0.8	
FS Input Pull-Up Current	I_{FSL}	FS low				50	µA
FS Input Leakage Current	I_{FSM}	FS high			10		pA
Input High Voltage	V_{IH}	DE´, DI´ (Figure 1)		V_{CC} - 0.4			V
Input Low Voltage	V_{IL}	DE´, DI´ (Figure 1)				0.4	V
Isolation Resistance	R_{ISO}	T_A = +25°C, V_{ISO} = 50V_{DC}		100	10,000		MΩ
Isolation Capacitance	C_{ISO}	T_A = +25°C, V_{ISO} = 50V_{DC}			10		pF
Differential Driver Output (no load)	V_{OD1}					8	V
Differential Driver Output (with load)	V_{OD2}	R = 50Ω (RS-422)		2			V
		R = 27Ω (RS-485), Figure 3		1.5		5	
Change in Magnitude of Driver Output Voltage for Complementary Output States	ΔV_{OD}	R = 27Ω or 50Ω, Figure 3	Differential			0.3	V
			Common Mode			0.3	
Driver Common-Mode Output	V_{OC}	R = 27Ω or 50Ω, Figure 4				4	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = V_{CC1} = V_{CC2} = V_{CC4} = V_{CC5} = 3.0V to 3.6V, FS = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = V_{CC1} = V_{CC2} = V_{CC4} = V_{CC5} = 3.3V and T_A = +25°C.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Input Current (A, B)	ISO I_{IN}	DE´ = 0V, V_{CC} = 0V or 3.6V	MAX3480A	V_{IN} = 12V			1.0	mA
				V_{IN} = -7V			-0.8	
			MAX3480B	V_{IN} = 12V			0.25	
				V_{IN} = -7V			-0.2	
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ 12V	MAX3480A		12			kΩ
			MAX3480B			48		
Receiver Differential Threshold	V_{TH}	-7V ≤ V_{CM} ≤ 12V			-0.2		0.2	V
Receiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0V				70		mV
$\overline{\text{Receiver Output}}$/Receiver Output Low Voltage	V_{OL}	DI´ = V_{CC}					0.4	V
$\overline{\text{Receiver Output}}$/Receiver Output High Current	I_{OH}	V_{OUT} = 3.6V, DI´ = 0V					250	µA
Driver Short-Circuit Current	ISO I_{OSD}	-7V ≤ V_O ≤ 12V (Note 4)				100		mA

SWITCHING CHARACTERISTICS—MAX3480A

(V_{CC} = V_{CC1} = V_{CC2} = V_{CC4} = V_{CC5} = 3.0V to 3.6V, FS = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = V_{CC1} = V_{CC2} = V_{CC4} = V_{CC5} = 3.3V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Input to Output Propagation Delay	t_{PLH}	Figures 4, 6; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		100	275	ns
	t_{PHL}			100	275	
Driver Output Skew (Note 5)	t_{SKEW}	Figures 4, 6; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		25	90	ns
Driver Rise or Fall Time	t_R, t_F	Figures 4, 6; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		15	40	ns
Driver Enable to Output High	t_{ZH}	Figures 5, 7; C_L = 100pF, S2 closed		0.2	1.5	µs
Driver Enable to Output Low	t_{ZL}	Figures 5, 7; C_L = 100pF, S1 closed		0.2	1.5	µs
Driver Disable Time from High	t_{HZ}	Figures 5, 7; C_L = 15pF, S2 closed		0.3	1.5	µs
Driver Disable Time from Low	t_{LZ}	Figures 5, 7; C_L = 15pF, S1 closed		0.3	1.5	µs
Receiver Input to Output Propagation Delay	t_{PLH}	Figures 4, 8; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		100	225	ns
	t_{PHL}			100	225	
$\lvert t_{PLH} - t_{PHL} \rvert$ Differential Receiver Skew	t_{SKD}	Figures 4, 8; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		20		ns
Maximum Data Rate	f_{MAX}	t_{PLH}, t_{PHL} < 50% of data period	2.5			Mbps

Complete, Isolated, 3.3V RS-485/RS-422 Data Interface

SWITCHING CHARACTERISTICS—MAX3480B

(V_{CC} = V_{CC1} = V_{CC2} = V_{CC4} = V_{CC5} = 3.0V to 3.6V, FS = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are a V_{CC} = V_{CC1} = V_{CC2} = V_{CC4} = V_{CC5} = 3.3V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Input to Output Propagation Delay	t_{PLH}	Figures 4, 6; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		1.0	2.0	µs
	t_{PHL}			1.0	2.0	
Driver Output Skew	t_{SKEW}	Figures 4, 6; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		100	800	ns
Driver Rise or Fall Time	t_R, t_F	Figures 4, 6; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		1.0	2.0	µs
Driver Enable to Output High	t_{ZH}	Figures 5, 7; C_L = 100pF, S2 closed		50	100	µs
Driver Enable to Output Low	t_{ZL}	Figures 5, 7; C_L = 100pF, S1 closed		50	100	µs
Driver Disable Time from Low	t_{LZ}	Figures 5, 7; C_L = 15pF, S1 closed		13	50	µs
Driver Disable Time from High	t_{HZ}	Figures 5, 7; C_L = 15pF, S2 closed		13	50	µs
Receiver Input to Output Propagation Delay	t_{PLH}	Figures 4, 8; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		0.8	2.0	µs
	t_{PHL}			0.8	2.0	
$\lvert t_{PLH} - t_{PHL} \rvert$ Differential Receiver Skew	t_{SKD}	Figures 4, 8; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		50		ns
Maximum Data Rate	f_{MAX}	t_{PLH}, t_{PHL} < 50% of data period	0.25			Mbps

Note 1: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to logic-side ground (GND1, GND2), unless otherwise specified.

Note 2: For DE´ and DI´ pin descriptions, see *Detailed Block Diagram* and *Typical Application Circuit* (Figure 1 for MAX3480A/MAX3480B).

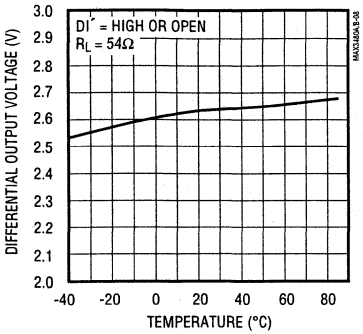
Note 3: Shutdown supply current is the current at V_{CC1} when shutdown is enabled.

Note 4: Applies to peak current. See *Typical Operating Characteristics* and *Applications Information*.

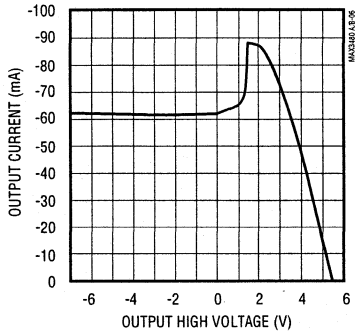
Typical Operating Characteristics

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

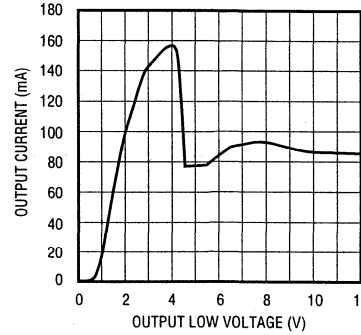
DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs. TEMPERATURE



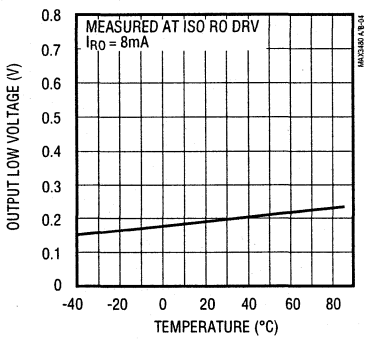
OUTPUT CURRENT vs. DRIVER OUTPUT HIGH VOLTAGE



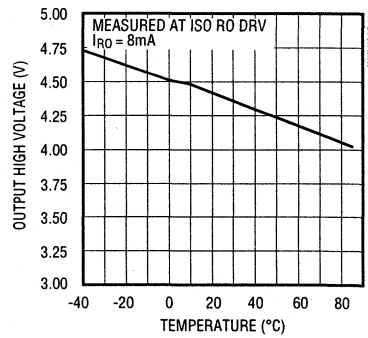
OUTPUT CURRENT vs. DRIVER OUTPUT LOW VOLTAGE



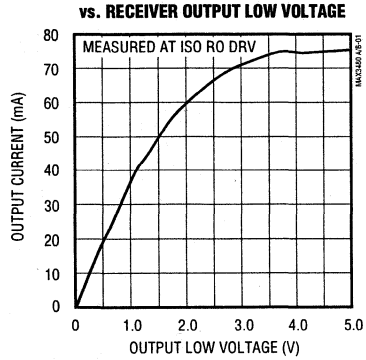
RECEIVER OUTPUT LOW VOLTAGE vs. TEMPERATURE



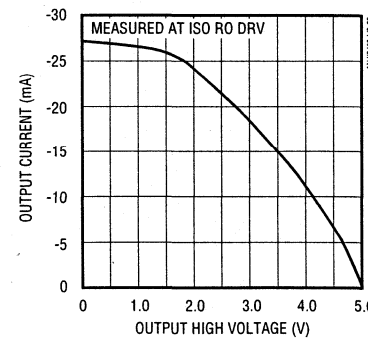
RECEIVER OUTPUT HIGH VOLTAGE vs. TEMPERATURE



OUTPUT CURRENT vs. RECEIVER OUTPUT LOW VOLTAGE



OUTPUT CURRENT vs. RECEIVER OUTPUT HIGH VOLTAGE

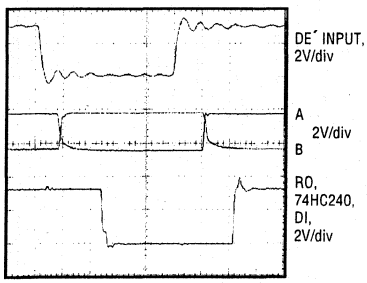


Complete, Isolated, 3.3V RS-485/RS-422 Data Interface

Typical Operating Characteristics (continued)

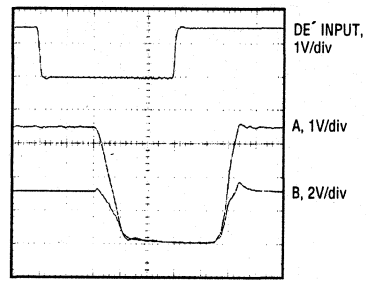
($V_{CC_}$ = 3.3V, T_A = +25°C, unless otherwise noted.)

MAX3480A DRIVER INPUT (AB) AND RECEIVER OUTPUT (RO)



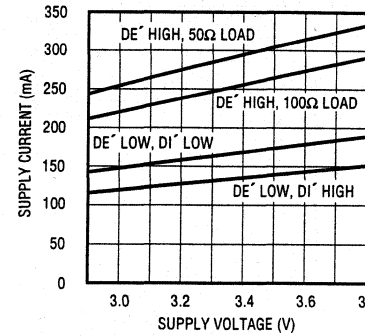
100ns/div
CIRCUIT OF FIGURE 2, TERMINATION: 100Ω

MAX3480A DRIVER ENABLE (AB) AND RECEIVER OUTPUT (RO)

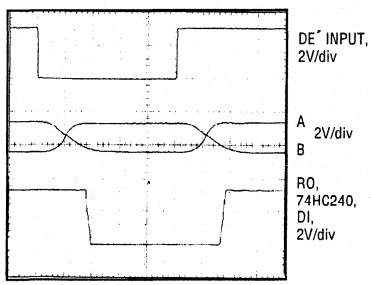


100ns/div
CIRCUIT OF FIGURE 2, TERMINATION: 100Ω

MAX3480A SUPPLY CURRENT vs. SUPPLY VOLTAGE

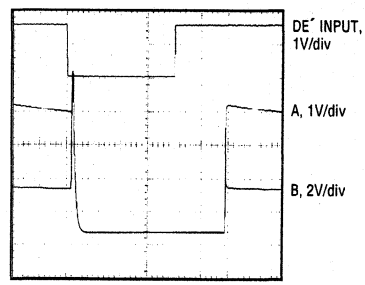


MAX3480B DRIVER INPUT (AB) AND RECEIVER OUTPUT (RO)



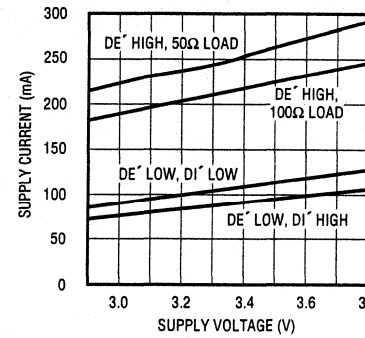
1µs/div
CIRCUIT OF FIGURE 2, TERMINATION: 100Ω

MAX3480B DRIVER ENABLE (AB) AND RECEIVER OUTPUT (RO)

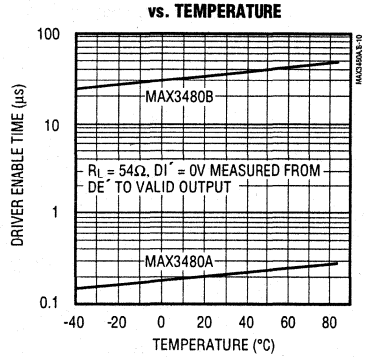


25µs/div
CIRCUIT OF FIGURE 2, TERMINATION: 100Ω

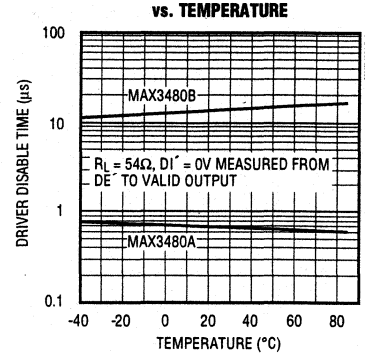
MAX3480B SUPPLY CURRENT vs. SUPPLY VOLTAGE



DRIVER ENABLE TIME vs. TEMPERATURE



DRIVER DISABLE TIME vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
PINS ON THE NON-ISOLATED SIDE		
1	V_{CC1}	Logic-Side (non-isolated side) +3.3V Supply Voltage Input. Connect to pins 2, 10, and 14.
2	V_{CC2}	Logic-Side (non-isolated side) +3.3V Supply Voltage Input. Connect to pins 1, 10, and 14.
3, 4	D1, D2	Boost-Voltage Generator Outputs. See Figures 1 and 2.
5, 12	GND1, GND2	Logic-Side Ground Inputs. Must be connected; not internally connected.
6	FS	Frequency Switch Input. If FS = V_{CC}, switch frequency is high; if FS = 0V, switch frequency is low (normal connection).
7	SD	Power-Supply Shutdown Input. Must be connected to logic ground.
8	V_{CC3}	Boosted V+ Voltage Input. Must be connected as shown in Figures 1 and 2.
9	DI	Driver Input. With DE´ high, a low on DI´ forces output A low and output B high. Similarly, a high on DI´ forces output A high and output B low. Drives internal LED cathode through R1 (Table 1 of Figure 2).
10	V_{CC4}	Logic-Side (non-isolated side) +3.3V Supply Voltage Input. Connect to pins 1, 2, and 14.
11	DE	Driver-Enable Input. The driver outputs, A and B, are enabled by bringing DE´ high. The driver outputs are high impedance when DE´ is low. If the driver outputs are enabled, the device functions as a line driver. While the driver outputs are high impedance, the device functions as a line receiver. Drives internal LED cathode through R2 (Table 1 of Figure 2).
13	$\overline{RO}$	Receiver Output. If A > B by 200mV, $\overline{RO}$ will be low; if A < B by 200mV, $\overline{RO}$ will be high. Open collector; must have pull-up (R3) to V_{CC} (Table 1 of Figure 2).
14	V_{CC5}	Logic-Side (non-isolated side) +3.3V Supply Voltage Input. Connect to pins 1, 2, and 10.

Complete, Isolated, 3.3V RS-485/RS-422 Data Interface

Pin Description (continued)

PIN	NAME	FUNCTION
PINS ON THE ISOLATED RS-485/RS-422 SIDE		
15	ISO RO LED	Isolated Receiver-Output LED Anode (input). If A > B by 200mV, ISO RO LED will be high; if A < B by 200mV, ISO RO LED will be low.
16	ISO COM2	Isolated-Supply Common Input. Connect to ISO COM1.
17	ISO DE DRV	Isolated Driver-Enable Drive Input. The driver outputs, A and B, are enabled by bringing DE´ high. The driver outputs are high impedance when DE´ is low. If the driver outputs are enabled, the device functions as a line driver. While the driver outputs are high impedance, the device functions as a line receiver. Open collector output; must have pull-up (R4) to ISO V_{CC} and be connected to ISO DE IN for normal operation (Table 1 of Figure 2).
18	ISO V_{CC2}	Isolated-Supply Positive Input Voltage. Connect to ISO V_{CC1}.
19	ISO DI DRV	Isolated Driver-Input Drive. With DE´ high, a low on DI´ forces output A low and output B high. Similarly, a high on DI´ forces output A high and output B low. Open-collector output; must have pull-up (R5) to ISO V_{CC} and be connected to ISO DI IN for normal operation (Table 1 of Figure 2).
20	ISO COM1	Isolated-Supply Common Output. Connect to ISO COM2. If RS-485 wires have a shield, connect ISO COM1 to shield via 100Ω resistor.
21	ISO DE IN	Isolated Driver-Enable Input. Connect to ISO DE DRV for normal operation.
22	ISO DI IN	Isolated Driver Input. Connect to ISO DI DRV for normal operation.
23	A	Noninverting Driver Output and Noninverting Receiver Input.
24	ISO RO DRV	Isolated Receiver-Output Drive. Connect to ISO RO LED through R6 (Table 1 of Figure 2).
25	B	Inverting Driver Output and Inverting Receiver Input
26	ISO V_{CC1}	Isolated Supply Positive Output Voltage. Connect to ISO V_{CC2}.
27, 28	AC2, AC1	Internal Connections. Leave these pins unconnected.

Note: For DE´ and DI´ pin descriptions, see *Detailed Block Diagram* and *Typical Application Circuit.*

Complete, Isolated, 3.3V RS-485/RS-422 Data Interface

Detailed Description

The MAX3480A/MAX3480B are electrically isolated, RS-485/RS-422 data-communications interface solutions. Transceivers, optocouplers, a power driver, and a transformer are in one standard 28-pin DIP package. Signals and power are internally transported across the isolation barrier (Figure 1). Power is transferred from the logic side (non-isolated side) to the isolated side of the barrier through a center-tapped transformer. Signals cross the barrier through high-speed optocouplers. A single +3.3V supply on the logic side powers both sides of the interface.

The MAX3480B features reduced-slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free transmission at data rates up to 250kbps. The MAX3480A's driver slew rates are not limited, allowing transmission rates up to 2.5Mbps.

The frequency-select FS is connected to GND_ in normal operation, which selects a switching frequency of approximately 600kHz. Connect to high for a higher 900kHz switching frequency.

Drivers are short-circuit current limited and are protected against excessive power dissipation by thermal

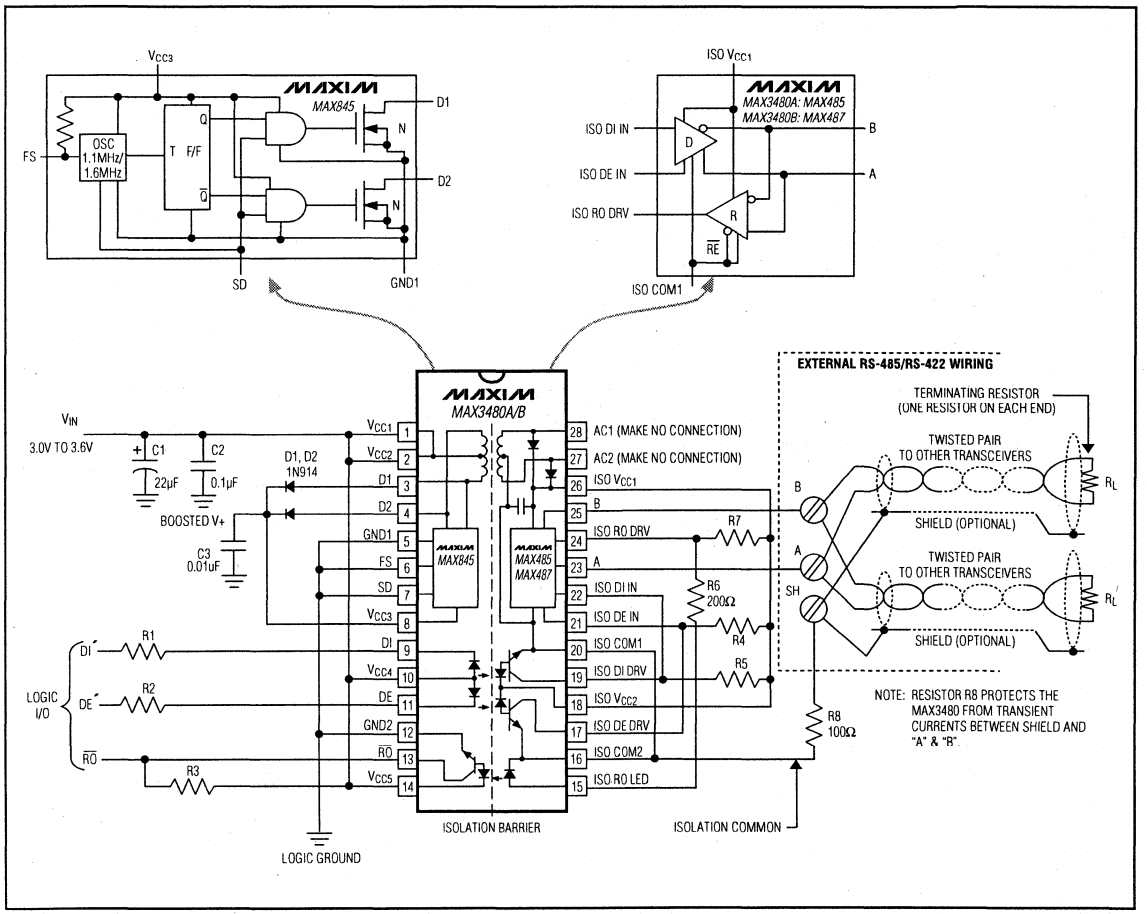


Figure 1. Detailed Block Diagram

Complete, Isolated, 3.3V RS-485/RS-422 Data Interface

shutdown circuitry that puts the driver outputs into a high-impedance state. The receiver input has a fail-safe feature that guarantees a logic-high output if the input is open circuit.

The driver outputs are enabled by bringing DE´ high. Driver-enable times are typically 200ns for the MAX3480A and 50µs for the MAX3480B. Allow time for the devices to be enabled before sending data. When enabled, driver outputs function as line drivers. Driver outputs are high impedance when DE´ is low. While outputs are high impedance, they function as line receivers.

The MAX3480A/MAX3480B typically withstand 1600VRMS (1 minute) or 2000VRMS (1 second). The isolated outputs of these devices meet all RS-485/RS-422 specifications. The logic inputs can be driven from any TTL/CMOS-logic family with a series resistor, and the received data output can directly drive any of the TTL/CMOS-logic families with only a resistive pull-up.

Boost Voltage

The MAX3480 requires external diodes on the primary of the transformer to develop the boost voltage for the power oscillator. In normal operation, whenever one of the oscillator outputs (D1 and D2) goes low, the other

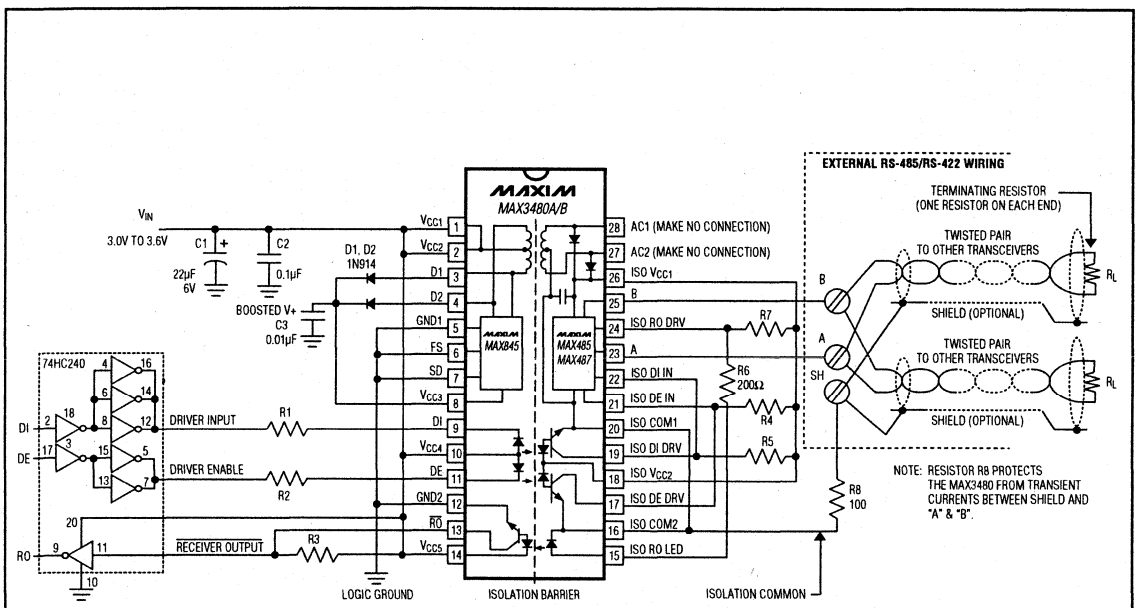


Table 1. Pull-Up and LED Drive Resistors

PART	R1 (Ω)	R2 (Ω)	R3 (Ω)	R4 (Ω)	R5 (Ω)	R6 (Ω)	R7 (Ω)
MAX3480A	150	130	680	3000	1000	200	Open
MAX3480B	130	330	2000	2200	3000	200	470

Figure 2. Typical Application Circuit

Test Circuits

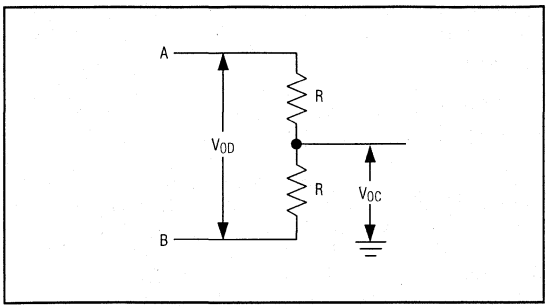


Figure 3. Driver DC Test Load

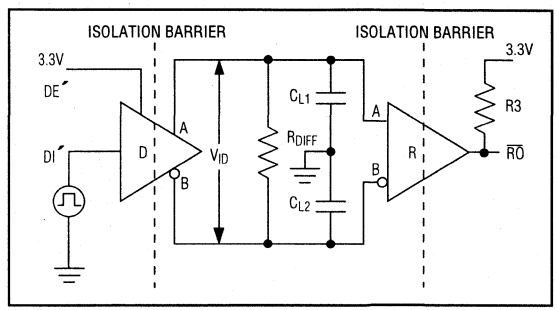


Figure 4. Driver/Receiver Timing Test Circuit

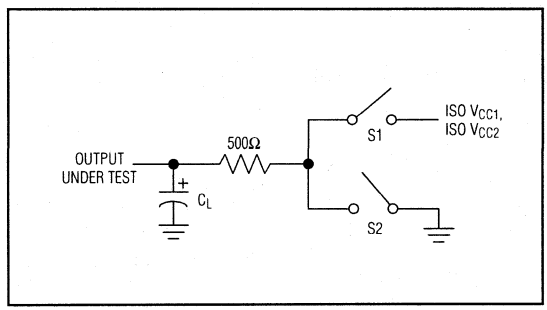


Figure 5. Driver Timing Test Load

Switching Waveforms

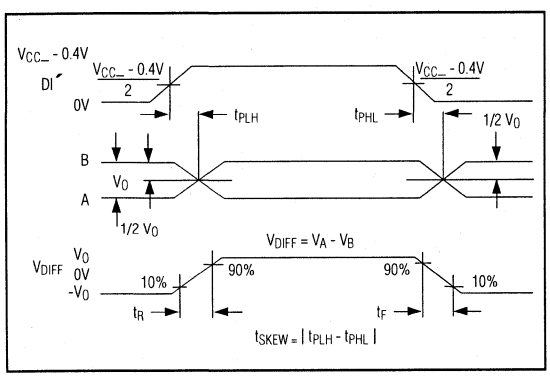


Figure 6. Driver Propagation Delays and Transition Times

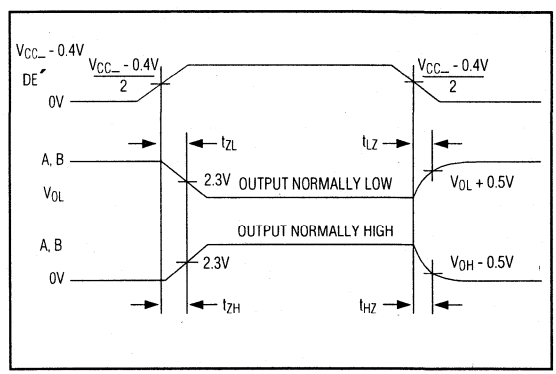


Figure 7. Driver Enable and Disable Times

Complete, Isolated, 3.3V RS-485/RS-422 Data Interface

Switching Waveforms (continued)

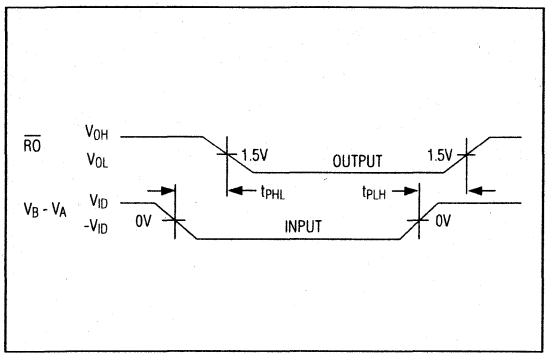


Figure 8. Receiver Propagation Delays

Function Tables

Table 2. Transmitting

INPUTS		OUTPUTS	
DE	DI	B	A
1	1	0	1
1	0	1	0
0	X	High-Z	High-Z

X = Don't care
High-Z = High impedance

Table 3. Receiving

INPUTS		OUTPUT
DE	A-B	$\overline{RO}$
0	≥ +0.2V	0
0	≤ -0.2V	1
0	Inputs open	0

goes to approximately double the supply voltage. Since the circuit is symmetrical, the two outputs can be combined with diodes, filtered, and used to power the oscillator itself.

The diodes on the primary side may be any fast-switching, small-signal diodes, such as the 1N914, 1N4148, or CMPD2838. The nominal value of the primary filter capacitor C3 is 0.01µF.

Driver Output Protection

There are two mechanisms to prevent excessive output current and power dissipation caused by faults or by bus contention. A foldback current limit on the output stage provides immediate protection against short circuits over the whole common-mode voltage range (see *Typical Operating Characteristics*). In addition, a thermal shutdown circuit forces the driver outputs into a high-impedance state if the die temperature rises excessively.

Resistor R8 provides additional protection by current limiting between the shield and the two signal wires. In the event that shielded cable is used and an external voltage or transient is inadvertently applied between the shield and the signal wires, the MAX3480 can be damaged. Although unlikely, this condition can occur during installation.

The MAX3480 provides electrical isolation between logic ground and signal paths; it does not provide isolation from external shields and the signal paths. When in doubt, do not connect the shield. The MAX3480 can be damaged if resistor R8 is shorted out.

Applications Information

The MAX3480A/MAX3480B are designed for bidirectional data communications on multipoint bus-transmission lines. Figure 9 shows a typical network application circuit. To minimize reflections, terminate the line at both ends with its characteristic impedance, and keep stub lengths off the main line as short as possible. The slew-rate-limited MAX3480B is more tolerant of imperfect termination and stubs off the main line.

The MAX3480A/MAX3480B are specified and characterized using the resistor values shown in Table 1 of Figure 2. Altering the recommended values can degrade performance.

The DI and DE inputs are the cathodes of LEDs whose anodes are connected to V_{CC}. These points are best driven by a 3.3V CMOS-logic gate with a series resistor to limit the current. The resistor values shown in Table 1 are recommended when the 74HC240 gate or equivalent is used. These values may need to be adjusted if a driving gate with dissimilar series resistance is used. DI and DE are intended to be driven through a series current-limiting resistor. Directly grounding these pins destroys the device.

Complete, Isolated, 3.3V RS-485/RS-422 Data Interface

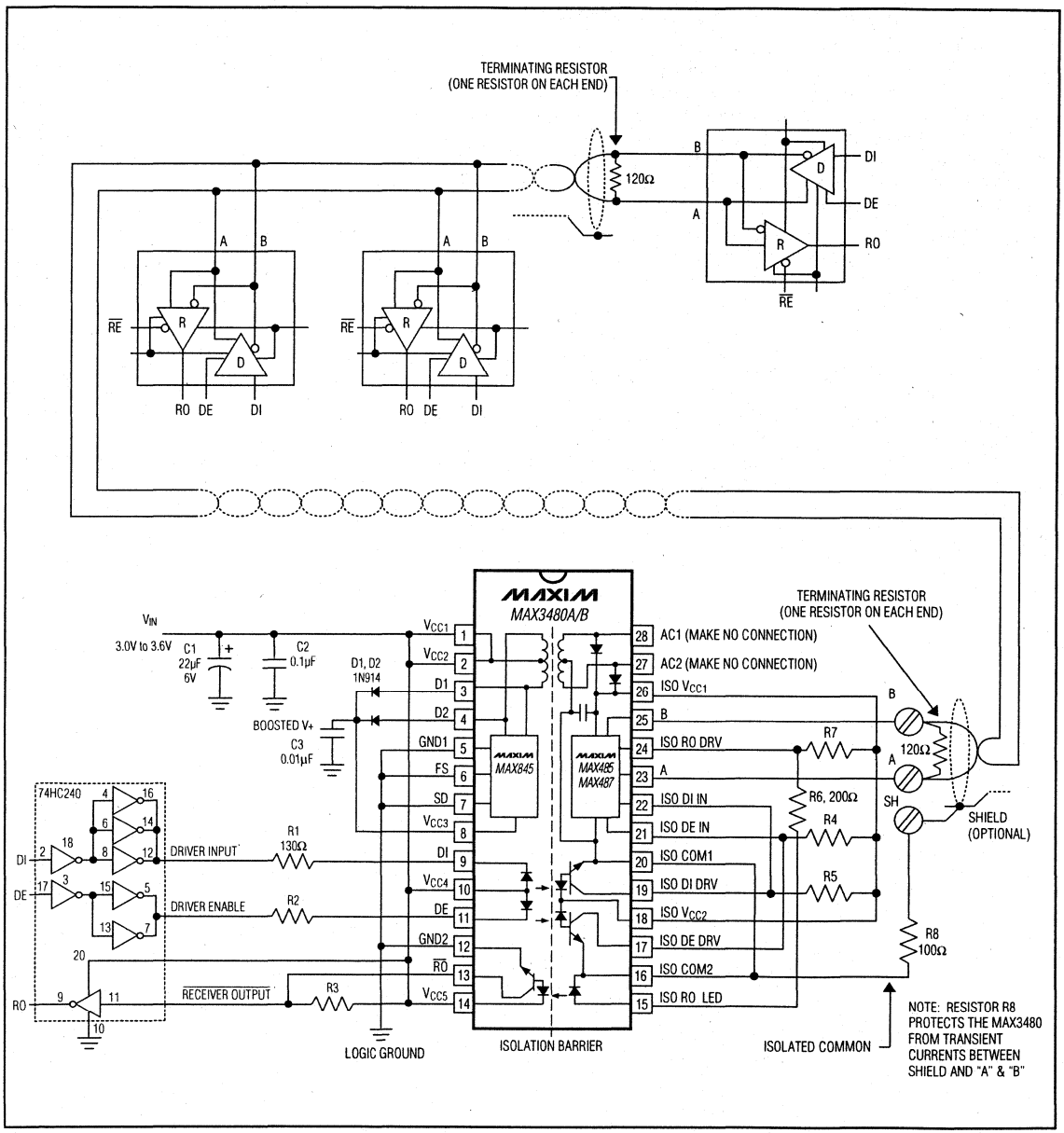


Figure 9. Typical RS-485/RS-422 Network

Table 4. Maxim's Isolated RS-485 Product Family

PART	No. OF Tx/Rx	GUARANTEED DATA RATE (Mbps)	FULL/HALF DUPLEX	SLEW-RATE LIMITED	No. OF Tx/Rx ON BUS	SUPPLY VOLTAGE (V)
MAX1480A	1/1	2.50	Half	No	32	5.0
MAX1480B	1/1	0.25	Half	Yes	32	5.0
MAX1490A	1/1	2.50	Full	No	32	5.0
MAX1490B	1/1	0.25	Full	Yes	32	5.0
MAX3480A	1/1	2.50	Half	No	32	3.3
MAX3480B	1/1	0.25	Half	Yes	128	3.3

MAXIM

Op Amps/Comparators

Op Amps/Comparators, Product Tables and Trees 3-2

MAX951	7µA, Single-Supply Op Amp + Comparator + Reference	3-9
MAX952	7µA, Single-Supply Op Amp + Comparator + Reference	3-9
MAX953	5µA, Single-Supply Op Amp + Comparator	3-9
MAX954	5µA, Single-Supply Op Amp + Comparator	3-9
MAX961	Single-Supply, Operation Down to 2.7V, 4.5ns Comparator	3-21
MAX962	Single-Supply, Operation Down to 2.7V, 4.5ns Comparator	3-21
MAX971	Single, Ultra-Low-Power, Open-Drain-Output Comparator with 1% Accurate Reference	3-31
MAX972	Dual, Ultra-Low-Power, Open-Drain-Output Comparator with 1% Accurate Reference	3-31
MAX973	Dual, Ultra-Low-Power, Open-Drain-Output Comparator with 1% Accurate Reference	3-31
MAX974	Quad, Ultra-Low-Power, Open-Drain-Output Comparator with 1% Accurate Reference	3-31
MAX975	+3V/+5V Dual-Speed Comparator with Auto-Standby	3-45
MAX976	Dual, +3V/+5V-Powered, High-Speed Comparator	3-61*
MAX977	Dual, +3V/+5V Dual-Speed Comparator with Auto-Standby	3-45
MAX978	Quad, +3V/+5V-Powered, High-Speed Comparator	3-61*
MAX981	Single, Ultra-Low-Power, Open-Drain-Output Comparator with 2% Accurate Reference	3-31
MAX982	Dual, Ultra-Low-Power, Open-Drain-Output Comparator with 2% Accurate Reference	3-31
MAX983	Dual, Ultra-Low-Power, Open-Drain-Output Comparator with 2% Accurate Reference	3-31
MAX984	Quad, Ultra-Low-Power, Open-Drain-Output Comparator with 2% Accurate Reference	3-31
MAX4122	Single, 5MHz, Single-Supply Op Amp	3-63
MAX4123	Single, 5MHz, Single-Supply Op Amp with Shutdown	3-63
MAX4124	Single, 10V/µs, Single-Supply Op Amp	3-63
MAX4125	Single, 10V/µs, Single-Supply Op Amp with Shutdown	3-63
MAX4126	Dual, 5MHz, Single-Supply Op Amp	3-63
MAX4127	Dual, 5MHz, Single-Supply Op Amp with Shutdown	3-63
MAX4128	Dual, 10V/µs, Single-Supply Op Amp	3-63
MAX4129	Quad, 5MHz, Single-Supply Op Amp	3-63
MAX4130	Single, 10MHz, Single-Supply Op Amp	3-79
MAX4131	Single, 10MHz, Single-Supply Op Amp with Shutdown	3-79
MAX4132	Dual, 10MHz, Single-Supply Op Amp	3-79
MAX4133	Dual, 10MHz, Single-Supply Op Amp with Shutdown	3-79
MAX4134	Quad, 10MHz, Single-Supply Op Amp	3-79

*Advance Information–first page of data sheet in preparation.

Op Amps

see Section 8 for Video Products/ High-Speed Amplifiers

Precision

Low V_{OS}

Bipolar

MAX400
MAX427
MAX437
MAX471 (current-sense amp)
MAX472 (current-sense amp)
MAX478 (dual, 17µA)
MAX479 (dual, 17µA)
MAX480
MAX492
MAX494
MAX495
MXL1001
MXL1007
MXL1013
MXL1014
MXL1178
MXL1179
OP07
OP27
OP37
OP90

Choppers

MAX420
MAX421
MAX422
MAX423
MAX430 (internal caps)
MAX432 (internal caps)
ICL765x

Low I_{BIAS}

MAX406 (<1pA)
MAX407 (<1pA, dual)
MAX409 (<1pA, 150kHz GBW)
MAX417 (<1pA, dual, 150kHz GBW)
MAX418 (<1pA, quad)
MAX419 (<1pA, quad, 150kHz GBW)
MAX420
MAX421
MAX422
MAX423
MAX430 (internal caps)
MAX432 (internal caps)
ICL761x
ICL762x
ICL763x
ICL764x
ICL765x

Low Noise

MAX400
MAX410 (<2.4nV/√Hz)
MAX412 (dual MAX410)
MAX414 (quad MAX410)
MAX427
MAX437
MXL1001
MXL1007
OP07
OP27
OP37

Low Power

Single Supply

MAX406 (1.2µA, rail-to-rail output)
MAX407 (dual MAX406)
MAX409 (1.2µA, 150kHz GBW, rail-to-rail output)
MAX417 (dual MAX409)
MAX418 (quad MAX406)
MAX419 (quad MAX409)
MAX478 (dual, 17µA)
MAX479 (quad, 17µA)
MAX480
ICL761x
ICL762x
ICL763x
ICL764x
MXL1013
MXL1014
MXL1178
MXL1179

Special

MAX951 (7µA, 20kHz op amp + comparator + reference)
MAX952 (7µA, 125kHz op amp + comparator + reference)
MAX953 (5µA, 20kHz op amp + comparator)
MAX954 (5µA, 125kHz op amp + comparator)

Single Supply & High Speed

★ MAX4122/4123 (5MHz, rail-to-rail I/O)
★ MAX4124/4125 (26MHz, rail-to-rail I/O)
★ MAX4126/4127 (5MHz, rail-to-rail I/O)
★ MAX4128 (26MHz, rail-to-rail I/O)
★ MAX4129 (5MHz, rail-to-rail I/O)
★ MAX4130/4131 (10MHz, rail-to-rail I/O)
★ MAX4132/4133 (10MHz, rail-to-rail I/O)
★ MAX4134 (10MHz, rail-to-rail I/O)
MAX473 (10MHz, 15V/µs)
MAX474 (dual MAX473)
MAX475 (quad MAX473)
MAX492 (dual MAX495)
MAX494 (quad MAX495)
MAX495 (500kHz, rail-to-rail input/output)

High Speed

MAX402 (2MHz, 75µA)
MAX403 (10MHz, 375µA)
MAX410 (28MHz, 2.5mA)
MAX412 (dual, 28MHz, 2.5mA)
MAX414 (quad, 28MHz, 2.5mA)
MAX438 (6MHz, 75µA)
MAX439 (25MHz, 375µA)

★ New product
† Future product

Part Number	V_{OS} (mV max)	I_{BIAS} (nA max)	Unity GBW (MHz)	Input Voltage Range (V_{CC}-_V) to (V_{EE}+_V)	Output Voltage Swing/Load (V_{CC}-_V) to (V_{EE}+_V)/(Ω)	Supply Voltage (V)	Supply Current/ Op Amp (mA max)	Features	Price† 1000-up ($)
MAX400	10 to 15µV	2	0.4	1 to 1	3 to 3/1k	±3 to ±18	4	Ultra-low V_{OS} & drift, non-chopper stabilized	5.16
MAX402	2	5	2	1.2 to 1.2	1.1 to 1.1/20k	±3 to ±5	75µA	High speed, micropower	1.98
MAX403	2	25	10	1.2 to 1.2	1.4 to 1.4/4k	±3 to ±5	375µA	High speed, micropower	2.75
MAX406/407/418	10	10pA	8 to 40kHz	1.1 to 0	0.01 to 0.01/1M	+2.5 to +10	1.2µA	Single/dual/quad, lowest power, single supply, rail-to-rail outputs, unity-gain stable	1.95/2.98/3.98
MAX409/417/419	10	10pA	150kHz (A_V ≥ 10V/V)	1.1 to 0	0.01 to 0.01/1M	+2.5 to +10	1.2µA	Single/dual/quad, lowest power, decompensated (A_V ≥ 10V/V)	1.95/2.98/3.98
MAX410/412/414	1 typ (320µV MAX414)	150	28	1.3 to 1.2	1.3 to 1.2/2k	±2.4 to ±5.25	2.7	Single/dual/quad, high speed, low noise, <2.4nV/√Hz at 1kHz guaranteed, unity-gain stable	1.50/2.45/4.50
MAX420/422	5 to 10µV	0.03 to 0.10	0.125 to 0.5	3.5 to -0.1	0.5 to 0.5/10k 0.4 to 0.4/100k	±2.5 to ±16.5	0.5 to 2	±15V chopper stabilized	3.77/4.21
MAX421/423	5 to 10µV	0.03 to 0.10	0.125 to 0.5	3.5 to -0.1	0.5 to 0.5/10k 0.4 to 0.4/100k	±2.5 to ±16.5	0.5 to 2	±15V chopper stabilized with clamped output and INT/EXT clock option	4.21/5.57
MAX427/437	15µV	35	8/60	2.5 to 2.5	1.2 to 1.2/≥2k	±15	4	High speed, low noise 3.8nV/√Hz precision	1.83
MAX430/432	5µV	0.1	0.125 to 0.5	2.5 to -0.1	0.5 to 0.5/10k	±2.5 to ±16.5	0.5 to 2	±15V chopper stabilized with internal caps	4.80/5.29
MAX438	2	5	6 (A_V ≥ 5V/V)	1.2 to 1.2	1.1 to 1.1/20k	±3 to ±5	75µA	High speed, micropower; 10V/µs slew rate	1.98
MAX439	2	25	25 (A_V ≥ 5V/V)	1.2 to 1.2	1.4 to 1.4/4k	±3 to ±5	375µA	High speed, micropower; 48V/µs slew rate	2.75
MAX471	–	–	–	0 to 3 amps**	1.5 to 0/no load	+3 to +36 (5µA SHDN)	100µA	Precision, high-side current-sense amplifier with internal sense resistor, measures charge and discharge	2.50
MAX472	60µV	–	–	–	1.5 to 0/no load	+3 to +36 (5µA SHDN)	100µA	Precision, high-side current-sense amplifier	2.05
MAX473/474/475	1 to 1.5	150	10	1.7 to -0.1	0.05 to 0.05/no load	+2.7 to +6	3	Single/dual/quad, single or dual supply, wide output swing, 15V/µs min slew rate	1.45/2.25/3.60
MAX478/479	70 to 250µV	6	60kHz	1.1 to -0.3	1.2 to 0.2/2k	+2.2 to +36 ±1.1 to ±18	17µA	Micropower, precision dual 8-pin SO and quad 14-pin narrow SO, 3V, 5V, and ±15V specs	2.58/3.35
MAX480	70µV	3	20kHz	1 to 0	0.8 to 0.1mV/2k, 10k	+1.6 to +36 ±0.8 to ±18	15µA	Low V_{OS} & drift, micropower, single supply, input/output extend to negative rail	3.68
MAX492/494/495	500µV	60	500kHz	0 to 0	0.15 to 0.15/1k	+2.7 to +6	150µA	Dual/quad/single, precision, rail-to-rail input and output	2.25/3.60/1.45
MAX4122/4123	0.6 to 1.2	120	5	-0.25 to -0.25	0.24 to 0.125/250	+2.7 to +6.5	0.825	Single, rail-to-rail input/output, unity-gain stable, MAX4123 has shutdown	0.85/0.98
MAX4124/4125	0.6 to 1.2	120	26 (A_V ≥ 10V/V)	-0.25 to -0.25	0.24 to 0.125/250	+2.7 to +6.5	0.825	Single, rail-to-rail input/output, decompensated MAX4125 has shutdown	0.85/0.98
MAX4126/4127	0.75 to 1.5	120	5	-0.25 to -0.25	0.28 to 0.18/250	+2.7 to +6.5	0.825	Dual, rail-to-rail input/output, unity-gain stable, MAX4127 has shutdown	1.40/1.67
MAX4128	0.75 to 1.5	120	26 (A_V ≥ 10V/V)	-0.25 to -0.25	0.28 to 0.18/250	+2.7 to +6.5	0.825	Dual, rail-to-rail input/output, decompensated	1.40
MAX4129	1.5	120	5	-0.25 to -0.25	0.28 to 0.18/250	+2.7 to +6.5	0.825	Quad, rail-to-rail input/output, unity-gain stable	2.40
MAX4130/4131	0.6 to 1.2	120	10	-0.25 to -0.25	0.24 to 0.125/250	+2.7 to +6.5	1.15	Single, rail-to-rail input/output, unity-gain stable, MAX4131 has shutdown	0.85/0.98
MAX4132/4133	0.6	150	10	-0.25 to -0.25	15mV to 10mV/100k	+2.7 to +6.5	1.15	Dual, rail-to-rail input/output, unity-gain stable, MAX4133 has shutdown	1.40/1.67
MAX4134	0.6	150	10	-0.25 to -0.25	15mV to 10mV/100k	+2.7 to +6.5	1.15	Quad, rail-to-rail input/output, unity-gain stable	2.40
ICL7611	2 to 15	0.05	0.044 to 1.4	0.8 to 1	0.1 to 0.1/100k	±1 to ±8	0.02 to 2.5	Programmable quiescent current	1.35
ICL7612	5 to 15	0.05	0.044 to 1.4	-0.3 to -0.1	0.1 to 0.1/100k	±1 to ±8	0.02 to 2.5	Programmable quiescent current, rail-to-rail input/output	1.29
ICL7614	2 to 15	0.05	0.48*	0.8 to 1	0.1 to 0.1/100k	±1 to ±8	0.25	External compensation	0.95
ICL7616	2 to 15	0.05	0.044 to 1.4	2 to -0.1	0.1 to 0.1/100k	±1 to ±8	0.02 to 2.5	Programmable quiescent current, extended CMVR	1.62

* External 39pF compensation capacitor added.
** Sense resistor current range
† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future product—contact factory for pricing and availability. Specifications are preliminary.

Op Amps (continued)

Part Number	V_{OS} (mV max)	I_{BIAS} (nA max)	Unity GBW (MHz)	Input Voltage Range (V_{CC}-_V) to (V_{EE}+_V)	Output Voltage Swing/Load (V_{CC}-_V) to (V_{EE}+_V)/(Ω)	Supply Voltage (V)	Supply Current/ Op Amp (mA max)	Features	Price† 1000-up ($)
ICL7621/7622	5 to 15	0.05	0.48	0.8 to 1	0.1 to 0.1/100k	±1 to ±8	0.25	Dual, low I_{BIAS} & I_{OS}	1.06/1.48
ICL7631/7632	5 to 20	0.05	0.044 to 1.4	0.8 to 1	0.1 to 0.1/100k	±1 to ±8	0.022 to 2.5	Triple op amp, programmable quiescent current ICL7632 is externally compensated	2.27/2.12
ICL7641/7642	5 to 25	0.05	0.044 to 1.4	1.3 to 1.3, 0.6 to 1	0.5 to 0.5/10k 0.1 to 0.1/1M	±1 to ±8	0.015 to 2.5	Quad, low power, CMOS	1.41/1.56
ICL7650	5 to 10µV	0.01 to 0.02	2	3 to -0.2	0.05 to 0.05/100k	±5	2	Industry standard, chopper stabilized	2.16
ICL7652	5 to 10µV	0.03	0.45	1 to 0.2	0.05 to 0.05/100k	±5	2	Low noise, industry standard, chopper stabilized	3.24
LH0101	3 to 10	300 to 1k	5	-1 to 2	2.5 to 2.5/100	±5 to ±15	35	5A peak power	18.98
MXL1001	15 to 60µV	2 to 4	0.8	1 to 1	1.5 to 1.5/1k	±3 to ±18	2	Precision LT1001 second source	1.73
MXL1007	25 to 60µV	35 to 55	8	2.5 to 2.5	2.5 to 2.5/600	±15	4 to 4.7	Low noise, precision LT1007 second source	1.85
MXL1013/1014	150 to 800µV	20 to 30	0.6	1.2 to -0.3	1 to 5mV/600	+4 to +36 ±2 to ±18	0.50 to 0.55	Dual/quad, precision LT1013/1014 second source	1.57/3.06
MXL1178/1179	70 to 600µV	5 to 6	60kHz	1.1 to -0.3	1.2 to 0.2mV/2k	+2.2 to +36 ±1.1 to ±18	17 to 21µA	Dual/quad, precision, micropower LT1178/1179 second source	2.50/3.35
OP07	25 to 150µV	2 to 12	0.6	1 to 1	3 to 3/1k	±3 to ±18	4	Industry standard, precision	1.58
OP27	25 to 100µV	40 to 80	8	2.7 to 2.7	3.5 to 3.5/600	±3 to ±18	4.6 to 5.6	Industry standard, low noise	2.06
OP37	25 to 100µV	40 to 80	63 ($A_V \geq 5$)	2.7 to 2.7	3.5 to 3.5/600	±3 to ±18	4.6 to 5.6	Industry standard, low noise	2.06
OP90	150 to 450µV	15 to 25	0.020	1 to 0	0.8 to 0.1mV/2k, 10k	±0.8 to ±18 ±1.6 to ±36	15 to 20µA	Industry standard, micropower	1.60

Op Amp + Comparator + Reference ICs

Part Number	Op Amp Compensation	Op Amp GBW (kHz)	Comparator Propagation Delay (µs)	Reference (1.2V ±1%)	Supply Voltage (V min)	Supply Current (µA max)	Features	Price† 1000-up ($)
MAX951	Unity-gain stable	20	4	Yes	2.7	10	Single-supply, rail-to-rail outputs, 8-pin package, low-cost op amp drives capacitive loads	1.60
MAX952	Decompensated ($A_V \geq 10V/V$)	125	4	Yes	2.7	10	MAX951 with decompensated op amp for $A_V \geq 10V/V$	1.60
MAX953	Unity-gain stable	20	4	—	2.4	8	MAX951 without the reference	1.30
MAX954	Decompensated ($A_V \geq 10V/V$)	125	4	—	2.4	8	MAX953 with decompensated op amp for $A_V \geq 10V/V$	1.30

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Comparators

Special

MAX516
(quad, programmable input threshold voltage)

MAX910
(8ns, programmable input threshold voltage)

MAX911
(4ns, programmable input threshold voltage)

High-Speed Comparators

TTL Output Single/Dual Supply

<10ns

MAX900
(quad, 8ns, single/dual supply)

MAX901
(quad, 8ns, single/dual supply)

MAX902
(dual, 8ns, single/dual supply)

MAX903
(8ns, single/dual supply)

MAX910
(8ns, programmable input threshold)

MAX912
(dual, 10ns, single/dual supply)

MAX913
(10ns, single/dual supply)

MAX915
(6ns, master/slave, clocked)

MAX916
(dual MAX915)

★MAX961
(single, 4.5ns, single supply)

★MAX962
(dual, 4.5ns, single supply)

† MAX963
(dual, 4.5ns, single supply)

† MAX964
(quad, 4.5ns, single supply)

<50ns

MAX907
(dual, 40ns, single supply)

MAX908
(quad, 40ns, single supply)

MAX909
(40ns, single/dual supply)

† MAX976
(300µA, 28ns)

† MAX978
(300µA, 28ns)

MAX9686
(6ns, industry standard)

MAX9698
(6ns, industry standard)

MXL1016

MXL1116

3V, High Speed

MAX941
(350µA, 80ns, rail-to-rail inputs)

MAX942
(dual MAX941)

MAX944
(quad MAX941)

† MAX976
(300µA, 28ns)

† MAX978
(300µA, 28ns)

ECL Output

MAX905
(master/slave, clocked)

MAX906
(dual, master/slave, clocked)

MAX911
(4ns, programmable input threshold voltage)

MAX9685
(industry standard)

MAX9687
(industry standard, dual)

MAX9690 (8-pin SO)

Micropower

MAX921/971
(3.2µA comparator + 1% reference)

MAX922/972
(dual, 3.2µA max supply current)

MAX923/973
(dual, 4.5µA comparator + 1% reference)

MAX924/974
(quad, 6.5µA comparator + 1% reference)

MAX931/981
(3.2µA comparator + 2% reference)

MAX932/982
(dual, 4.5µA comparator + 2% reference)

MAX933/983
(dual, 4.5µA comparator + 2% reference, window comparator)

MAX934/984
(quad, 6.5µA comparator + 2% reference)

Special

MAX951
(7µA, 20kHz op amp + comparator + reference)

MAX952
(7µA, 125kHz op amp + comparator + reference)

MAX953
(5µA, 20kHz op amp + comparator)

MAX954
(5µA, 125kHz op amp + comparator)

★MAX975
(dual-speed comparator)

★MAX977
(dual-speed comparator)

★ New product
† Future product

Comparators (High-Speed & Micropower)

Part Number	Comps. per Pkg.	Input Offset Voltage (mV)	Input Voltage Range (V_{CC}-_V) to (V_{EE}+_V)	Logic	Latched Outputs	Complementary Outputs	Supply Voltage (V)	Supply Current per Comp. (mA max)	t_{PD} (ns)	Features	Price† 1000-up ($)
HIGH SPEED											
MAX516	4	4.9*	0 to 0	TTL/CMOS	No	No	+4.75 to +16.5	10.01 (total pkg.)	800	Quad comparator + quad 8-bit DAC for independent threshold setting, single-supply capability, rail-to-rail input voltage ranges	3.00
MAX900	4	0.5	2.25 to -0.1	TTL	Yes	No	+5 to +10, ±5	4 (I_{CC})	8	Single +5V capability, low power, CMVR extends to neg. rail, separate analog & digital supplies, internal pull-up resistors	7.01
MAX901	4	0.5	2.25 to -0.1	TTL	No	No	+5 to +10, ±5	4 (I_{CC})	8	MAX900 without output latch	5.98
MAX902	2	1	2.25 to -0.1	TTL	Yes	No	+5 to +10, ±5	4 (I_{CC})	8	Dual MAX900	4.01
MAX903	1	1	2.25 to -0.1	TTL	Yes	No	+5 to +10, ±5	4 (I_{CC})	8	Single MAX900	3.15
MAX905	1	0.5	2.2 to -0.1	ECL	Yes	Yes	-5 or ±5	24 (I_{EE})	1.8	Edge-triggered master/slave architecture eliminates oscillations and resolves 3mV input voltages, also operates with -5.2V or +5V, -5.2V ECL supplies	3.54
MAX906	2	0.5	2.2 to -0.1	ECL	Yes	Yes	-5 or ±5	24 (I_{EE})	1.8	Dual MAX905, also operates with -5.2V or +5V, -5.2V ECL supplies	5.23
MAX907	2	0.5	1.5 to -0.2	TTL	No	No	+4.5 to +5.5	1	30	High speed, ultra-low power, single +5V, 8-pin DIP/SO, built-in hysteresis	1.70
MAX908	4	0.5	1.5 to -0.2	TTL	No	No	+4.5 to +5.5	1	30	High speed, ultra-low power, single +5V, 14-pin DIP/SO, built-in hysteresis	2.95
MAX909	1	0.5	1.5 to -0.2	TTL	Yes	Yes	+4.5 to +5.5, ±5	1.8	30	High speed, low power, single or dual supply, input range includes ground, complementary outputs	1.50
MAX910	1	1	2 to 2	TTL	Yes	No	±5 or +5, -5.2	30 (I_{CC})	8	TTL-compatible, 8-bit digitally programmable input voltage threshold, on-board reference	5.20
MAX911	1	1	2 to 2	ECL	Yes	Yes	±5 or +5, -5.2	30 (I_{EE})	4	MAX910 with differential ECL outputs	5.20
MAX912	2	0.8	1.5 to -0.2	TTL	Yes	Yes	+5 or ±5	10	10	Dual MAX913	3.90
MAX913	1	0.8	1.5 to -0.2	TTL	Yes	Yes	+5 or ±5	10	10	Lowest power 10ns comparator with complementary outputs single/dual supply, CMVR extends below ground to V+ -1.5V	2.55
MAX915	1	0.5	2.2 to -0.1	TTL	Yes	Yes	+5 or ±5	18 (I_{CC})	6	No oscillations, master/slave, clocked	2.55
MAX916	2	0.5	2.2 to -0.1	TTL	Yes	Yes	+5 or ±5	18 (I_{CC})	6	Dual MAX915	3.90
MAX941	1	1	-0.2 to -0.2	TTL/CMOS	Yes	No	+2.7 to +6	600µA	75	Low power, 3V or 5V single supply, rail-to-rail inputs (5µA SHDN)	1.40
MAX942	2	1	-0.2 to -0.2	TTL/CMOS	No	No	+2.7 to +6	600µA	75	Dual MAX941, 8-pin DIP/SO	1.50
MAX944	4	1	-0.2 to -0.2	TTL/CMOS	No	No	+2.7 to +6	600µA	75	Quad MAX941	2.50
MAX961	1	0.5	-0.1 to -0.1	TTL/CMOS	Yes	Yes	+2.7 to +8	11	4.5	High-speed, internal hysteresis, rail-to-rail inputs, shutdown mode	2.50
MAX962	2	0.5	-0.1 to -0.1	TTL/CMOS	No	No	+2.7 to +8	8	4.5	Dual, internal hysteresis, rail-to-rail inputs	4.25
MAX963	2	0.5	-0.1 to -0.1	TTL/CMOS	Yes	Yes	+2.7 to +8	11	4.5	Dual, internal hysteresis, rail-to-rail inputs, shutdown mode	††
MAX964	4	0.5	-0.1 to -0.1	TTL/CMOS	No	No	+2.7 to +8	8	4.5	Quad, internal hysteresis, rail-to-rail inputs, shutdown mode	††
MAX976	2	0.2	1.2 to -0.02	TTL/CMOS	No	No	+2.7 to +5.25	0.300	28	Dual, high-speed, single-supply comparator	††
MAX978	4	0.2	1.2 to -0.02	TTL/CMOS	No	No	+2.7 to +5.25	0.300	28	Quad, high-speed, single-supply comparator	††
MAX9685	1	5	2.5 to 2.7	ECL	Yes	Yes	±5 or +5, -5.2	32 (I_{EE})	1.3	Higher-speed industry standard	3.38
MAX9686	1	5	2 to 2	TTL	Yes	Yes	±5 or +5, -5.2	25 (I_{CC})	6	Higher-speed industry standard	2.31
MAX9687	2	5	2.5 to 2.5	ECL	Yes	Yes	±5 or +5, -5.2	68 (I_{EE})	1.4	Higher-speed industry standard	5.12
MAX9690	1	5	2.5 to 2.5	ECL	No	Yes	±5 or +5, -5.2	32 (I_{EE})	1.3	8-pin DIP/SO package	3.29
MAX9698	2	5	2 to 2	TTL	Yes	Yes	±5 or +5, -5.2	50 (I_{CC})	6	Higher-speed industry standard	3.92
MXL1016	1	0.8	1.5 to 1.25	TTL	Yes	Yes	+5 or ±5	35 (I_{CC})	10	High speed, complementary outputs, LT1016 second source	2.57
MXL1116	1	1	2.5 to 0	TTL	Yes	Yes	+5 or ±5	38 (I_{CC})	12	High speed, single supply, complementary outputs, LT1116 second source	2.57

* Total unadjusted error equals ±1LSB(max).
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†† Future product—contact factory for pricing and availability. Specifications are preliminary.

Comparators (High-Speed & Micropower) (continued)

Part Number	Comps. per Pkg.	Input Offset Voltage (mV)	Input Voltage Range (V_{CC}-_V) to (V_{EE}+_V)	Logic	Latched Outputs	Complementary Outputs	Supply Voltage (V)	Supply Current per Comp. (µA max)	t_{PD} (µs)	Features	Price† 1000-up ($)
MICROPOWER											
MAX921/971	1 + ref	10	1.3 to 0	TTL/CMOS/ Open Drain	No	No	+2.5 to +11, ±1.25 to ±5	3.2 (total pkg.)	12	Micropower comparator + 1% reference & hysteresis, single-supply capability, CMVR extends to GND	1.50/1.50
MAX922/972	2	10	1.3 to 0	TTL/CMOS/ Open Drain	No	No	+2.5 to +11, ±1.25 to ±5	3.2 (total pkg.)	12	Dual, single-supply micropower comparator in 8-pin DIP/SO	1.50/0.98
MAX923/973	2 + ref	10	1.3 to 0	TTL/CMOS/ Open Drain	No	No	+2.5 to +11, ±1.25 to ±5	4.5 (total pkg.)	12	Dual, single-supply comparator with 1% voltage reference in 8-pin DIP/SO	1.95/1.95
MAX924/974	4 + ref	10	1.3 to 0	TTL/CMOS/ Open Drain	No	No	+2.5 to +11, ±1.25 to ±5	6.5 (total pkg.)	12	Quad, micropower comparator with 1% voltage reference	2.25/2.25
MAX931/981	1 + ref	10	1.3 to 0	TTL/CMOS/ Open Drain	No	No	+2.5 to +11, ±1.25 to ±5	3.2 (total pkg.)	12	Low-cost comparator + 2% reference & hysteresis, single-supply, CMVR extends to GND	0.98/0.98
MAX932/982	2 + ref	10	1.3 to 0	TTL/CMOS/ Open Drain	No	No	+2.5 to +11, ±1.25 to ±5	4.5 (total pkg.)	12	Dual, low-cost, single-supply comparator + 2% reference & hysteresis in 8-pin DIP/SO	1.26/1.26
MAX933/983	2 + ref	10	1.3 to 0	TTL/CMOS/ Open Drain	No	No	+2.5 to +11, ±1.25 to ±5	4.5 (total pkg.)	12	Dual, low-cost, single-supply comparator + 2% reference & hysteresis in 8-pin DIP/SO (window comparator input configuration)	1.26/1.26
MAX934/984	4 + ref	10	1.3 to 0	TTL/CMOS/ Open Drain	No	No	+2.5 to +11, ±1.25 to ±5	6.5 (total pkg.)	12	Quad, low-cost comparator + 2%-accurate reference, single/dual supply	1.31/1.31
MAX951–954 (See Op Amp + Comparator + Reference IC section for tables)											—

Comparators (Special)

Part Number	Comps. per Pkg.	Input Offset Voltage (mV)	Input Voltage Range (V_{CC}-_V) to (V_{EE}+_V)	Logic	Latched Outputs	Complementary Outputs	Supply Voltage (V)	Supply Current per Comp. (mA max)	t_{PD} (ns)	Features	Price† 1000-up ($)
SPECIAL											
MAX975	2 (1 high speed 1 low power)	0.2	1.2 to -0.2	TTL/CMOS	No	No	+2.7 to +5.25	0.300 (high speed) 0.003 (low power)	28 (high speed) 480 (low power)	Dual speed, automatically switches from high-speed comparator to low-power comparator	1.95
MAX977	4 (2 high speed 2 low power)	0.2	1.2 to -0.2	TTL/CMOS	No	No	+2.7 to +5.25	0.300 (high speed) 0.003 (low power)	28 (high speed) 480 (low power)	Dual speed, automatically switches from high-speed comparator to low-power comparator	3.50

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

19-0431; Rev 0; 9/95

MAXIM

Ultra-Low-Power, Single-Supply Op Amp + Comparator + Reference

General Description

The MAX951–MAX954 feature combinations of a micropower operational amplifier, comparator, and reference in an 8-pin package. In the MAX951 and MAX952, the comparator's inverting input is connected to an internal 1.2V ±2% bandgap reference. The MAX953 and MAX954 are offered without an internal reference. The MAX951/MAX952 operate from a single +2.7V to +7V supply with a typical supply current of 7µA, while the MAX953/MAX954 operate from +2.4V to +7V with a 5µA typical supply current. Both the op amp and comparator feature a common-mode input voltage range that extends from the negative supply rail to within 1.6V of the positive rail, as well as output stages that swing rail to rail.

The op amps in the MAX951/MAX953 are internally compensated to be unity-gain stable, while the op amps in the MAX952/MAX954 feature 125kHz typical bandwidth, 66V/ms slew rate, and stability for gains of 10V/V or greater. These op amps have a unique output stage that enables them to operate with an ultra-low supply current while maintaining linearity under loaded conditions. In addition, they have been designed to exhibit good DC characteristics over their entire operating temperature range, minimizing input referred errors.

The comparator output stage of these devices continuously sources as much as 40mA. The comparators eliminate power-supply glitches that commonly occur when changing logic states, minimizing parasitic feedback and making the devices easier to use. In addition, they contain ±3mV internal hysteresis to ensure clean output switching, even with slow-moving input signals.

Features

- **Op Amp + Comparator + Reference in an 8-Pin µMAX Package (MAX951/MAX952)**
- **7µA Typical Supply Current (Op Amp + Comparator + Reference)**
- **Comparator and Op-Amp Input Range Includes Ground**
- **Outputs Swing Rail to Rail**
- **+2.4V to +7V Supply Voltage Range**
- **Unity-Gain Stable and 125kHz Decompensated Av ≥ 10V/V Op-Amp Options**
- **Internal 1.2V ±2% Bandgap Reference**
- **Internal Comparator Hysteresis**
- **Op Amp Capable of Driving up to 1000pF Load**

Applications

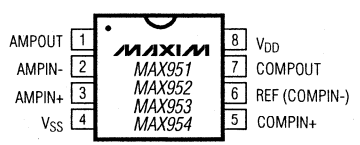
Instruments, Terminals, and Bar-Code Readers
Battery-Powered Systems
Automotive Keyless Entry
Low-Frequency, Local-Area Alarms/Detectors
Photodiode Preamps
Smart Cards
Infrared Receivers for Remote Controls
Smoke Detectors and Safety Sensors

Selection Table

PART	INTERNAL 2% PRECISION REFERENCE	OP-AMP GAIN STABILITY (V/V)	COMPARATOR	SUPPLY CURRENT (µA)
MAX951	Yes	1	Yes	7
MAX952	Yes	10	Yes	7
MAX953	No	1	Yes	5
MAX954	No	10	Yes	5

Pin Configuration

TOP VIEW



DIP/SO/µMAX

( ) ARE FOR MAX953/MAX954

Typical Operating Circuit and Ordering Information appear at end of data sheet.

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Ultra-Low-Power, Single-Supply Op Amp + Comparator + Reference

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{DD} to V_{SS}) 9V
Inputs
  Current (AMPIN_, COMPIN_) 20mA
  Voltage (AMPIN_, COMPIN_) ..... (V_{DD} + 0.3V) to (V_{SS} - 0.3V)
Outputs
  Current (AMPOUT, COMPOUT) 50mA
  Current (REF) 20mA
  Voltage (AMPOUT, COMPOUT, REF) ..... (V_{DD} + 0.3V) to (V_{SS} - 0.3V)
  Short-Circuit Duration (REF, AMPOUT) ..... Continuous
  Short-Circuit Duration (COMPOUT, V_{DD} to $V_{SS} \le 7V$) 1min
Continuous Power Dissipation (T_A = +70°C)
  Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
  SO (derate 5.88mW/°C above +70°C) 471mW
  µMAX (derate 4.10mW/°C above +70°C) 330mW
  CERDIP (derate 8.00mW/°C above +70°C) 640mW
Operating Temperature Ranges
  MAX95_E_A ..... -40°C to +85°C
  MAX95_MJA ..... -55°C to +125°C
Maximum Junction Temperatures
  MAX95_E_A ..... +150°C
  MAX95_MJA ..... +175°C
Storage Temperature Range ..... -65°C to +165°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.8V to 7V for MAX951/MAX952, V_{DD} = 2.4V to 7V for MAX953/MAX954, V_{SS} = 0V, $V_{CM\ COMP}$ = 0V for the MAX953/MAX954, $V_{CM\ OPAMP}$ = 0V, AMPOUT = (V_{DD} + V_{SS}) / 2, COMPOUT = low, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}	MAX951/MAX952	T_A = T_{MIN} to T_{MAX}	2.8		7.0	V
			T_A = -10°C to +85°C	2.7		7.0	
		MAX953/MAX954		2.4		7.0	
Supply Current (Note 1)	I_S	T_A = +25°C, MAX951/MAX952			7	10	µA
		MAX951E/MAX952E				11	
		MAX951M/MAX952M				13	
		T_A = +25°C, MAX953/MAX954			5	8	
		MAX953E/MAX954E				9	
		MAX953M/MAX954M				11	
COMPARATOR							
Input Offset Voltage (Note 2)	V_{OS}	T_A = +25°C			1	3	mV
		MAX95_EPA/ESA				4	
		MAX95_EUA (µMAX)				14	
		MAX95_MJA				6	
Trip Point (Note 3)		T_A = +25°C			4		mV
		MAX95_EUA (µMAX)			17		
		MAX95_EPA/ESA			5		
		MAX95_MJA			7		
Input Leakage Current (Note 4)		T_A = +25°C			0.003	0.050	nA
		MAX95_E			0.003	5	
		MAX95_M				40	
Common-Mode Range	CMVR			V_{SS}		V_{DD} -1.6V	V
Common-Mode Rejection Ratio	CMRR	V_{SS} to (V_{DD} - 1.6V), MAX953/MAX954			0.1	1	mV/V

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 2.8V to 7V for MAX951/MAX952, V_{DD} = 2.4V to 7V for MAX953/MAX954, V_{SS} = 0V, $V_{CM\ COMP}$ = 0V for the MAX953/MAX954, $V_{CM\ OPAMP}$ = 0V, AMPOUT = (V_{DD} + V_{SS}) / 2, COMPOUT = low, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power-Supply Rejection Ratio	PSRR	MAX951/MAX952, V_{DD} = 2.8V to 7V			0.05	1	mV/V
		MAX953/MAX954, V_{DD} = 2.4V to 7V			0.05	1	
Response Time	T_{pd}	C_L = 100pF, T_A = +25°C, V_{DD} - V_{SS} = 5V	V_{OD} = 10mV		22		µs
			V_{OD} = 100mV		4		
Output High Voltage	V_{OH}	I_{SOURCE} = 2mA		V_{DD} - 0.4V			V
Output Low Voltage	V_{OL}	I_{SINK} = 1.8mA				V_{SS} + 0.4V	V
REFERENCE							
Reference Voltage (Note 5)	V_{REF}	MAX95_EPA/ESA		1.176	1.200	1.224	V
		MAX95_EUA (µMAX)		1.130	1.200	1.270	
		MAX95_MJA		1.164	1.200	1.236	
Load Regulation		I_{OUT} = ±20µA, T_A = +25°C			0.1		%
		I_{OUT} = ±6µA, MAX95_E				1.5	
		I_{OUT} = ±3µA, MAX95_M				1.5	
Voltage Noise	e_n	0.1Hz to 10Hz			16		µVp-p
OP AMP							
Input Offset Voltage	V_{OS}	T_A = +25°C			1	3	mV
		MAX95_EPA/ESA				4	
		MAX95_EUA (µMAX)				5	
		MAX95_MJA				5	
Input Bias Current	I_B	T_A = +25°C			0.003	0.050	nA
		MAX95_E			0.003	5	
		MAX95_M			0.003	40	
Large-Signal Gain (no load)	A_{VOL}	AMPOUT = 0.5V to 4.5V, V_{DD} - V_{SS} = 5V	T_A = +25°C	100	1000		V/mV
			MAX95_E	50			
			MAX95_M	10			
Large-Signal Gain (100kΩ load to V_{SS})	A_{VOL}	AMPOUT = 0.5V to 4.5V, V_{DD} - V_{SS} = 5V	T_A = +25°C	40	150		V/mV
			MAX95_E	25			
			MAX95_M	5			
Gain Bandwidth	GBW	A_V = +1V/V, MAX951/MAX953, V_{DD} - V_{SS} = 5V			20		kHz
		A_V = +10V/V, MAX952/MAX954, V_{DD} - V_{SS} = 5V			125		
Slew Rate	SR	A_V = +1V/V, MAX951/MAX953, V_{DD} - V_{SS} = 5V			12.5		V/ms
		A_V = +10V/V, MAX952/MAX954, V_{DD} - V_{SS} = 5V			66		
Common-Mode Input Range	CMVR			V_{SS}		V_{DD} - 1.6	V
Common-Mode Rejection Ratio	CMRR	$V_{CM\ OPAMP}$ = V_{SS} to (V_{DD} - 1.6V)			0.03	1	mV/V
Power-Supply Rejection Ratio	PSRR	V_{DD} = 2.8V to 7V, MAX951/MAX952			0.07	1.0	mV/V
		V_{DD} = 2.4V to 7V, MAX953/MAX954			0.07	1.0	
Input Noise Voltage	en	f_o = 1kHz			80		nV√Hz
		f_o = 0.1Hz to 10Hz			1.2		µVp-p

Ultra-Low-Power, Single-Supply Op Amp + Comparator + Reference

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 2.8V to 7V for MAX951/MAX952, V_{DD} = 2.4V to 7V for MAX953/MAX954, V_{SS} = 0V, $V_{CM\ COMP}$ = 0V for the MAX953/MAX954, $V_{CM\ OPAMP}$ = 0V, AMPOUT = (V_{DD} + V_{SS}) / 2, COMPOUT = low, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH}	R_L = 100kΩ to V_{SS}	V_{DD} - 500mV			V
Output Low Voltage	V_{OL}	R_L = 100kΩ to V_{SS}			V_{SS} + 50mV	V
Output Source Current	I_{SRC}	T_A = +25°C	70	134		µA
		T_A = +25°C, V_{DD} - V_{SS} = 5V	300	820		
		MAX95_E	60			
		MAX95_M	40			
Output Sink Current	I_{SNK}	T_A = +25°C	140			µA
		T_A = +25°C, V_{DD} - V_{SS} = 5V	200	570		
		MAX95_E	50			
		MAX95_M	30			

Note 1: Supply current is tested with COMPIN+ = (REF - 100mV) for MAX951/MAX952, and COMPIN+ = 0V for MAX953/MAX954.

Note 2: Input Offset Voltage is defined as the center of the input-referred hysteresis. $V_{CM\ COMP}$ = REF for MAX951/MAX952, and $V_{CM\ COMP}$ = 0V for MAX953/MAX954.

Note 3: Trip Point is defined as the differential input voltage required to make the comparator output change. The difference between upper and lower trip points is equal to the width of the input-referred hysteresis. $V_{CM\ COMP}$ = REF for MAX951/MAX952, and $V_{CM\ COMP}$ = 0V for MAX953/MAX954.

Note 4: For MAX951/MAX952, input leakage current is measured for COMPIN- at the reference voltage. For MAX953/MAX954, input leakage current is measured for both COMPIN+ and COMPIN- at V_{SS}.

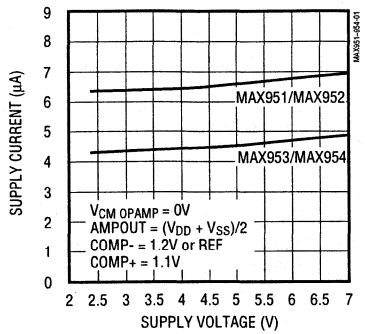
Note 5: Reference voltage is measured with respect to V_{SS}. Contact factory for availability of a 3% accurate reference voltage in the µMAX package.

Ultra-Low-Power, Single-Supply Op Amp + Comparator + Reference

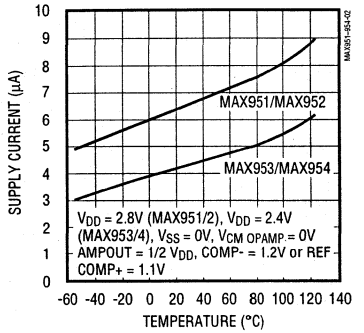
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

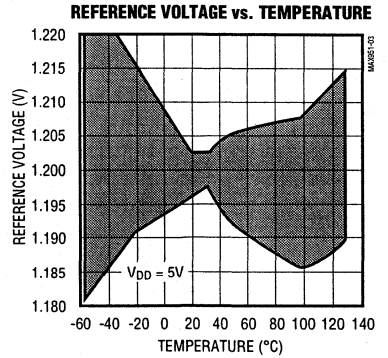
SUPPLY CURRENT vs. SUPPLY VOLTAGE



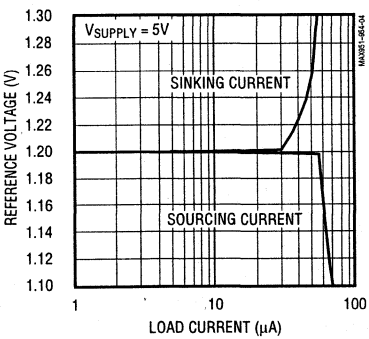
SUPPLY CURRENT vs. TEMPERATURE



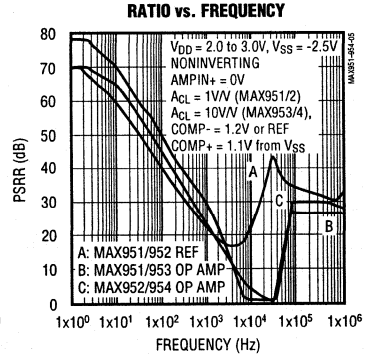
REFERENCE VOLTAGE vs. TEMPERATURE



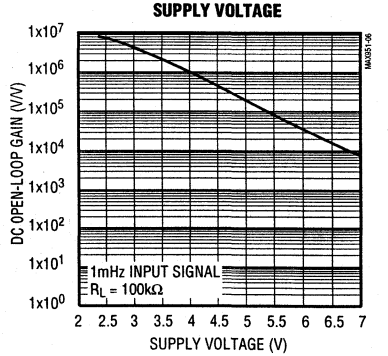
REFERENCE OUTPUT VOLTAGE vs. LOAD CURRENT



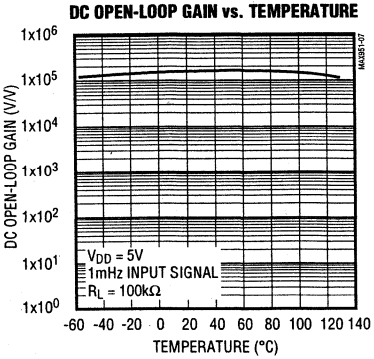
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



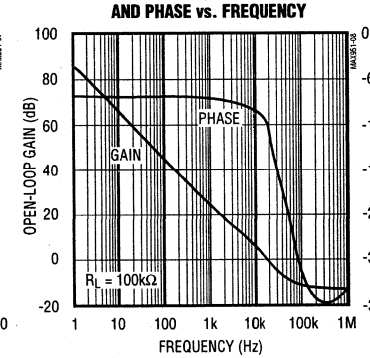
DC OPEN-LOOP GAIN vs. SUPPLY VOLTAGE



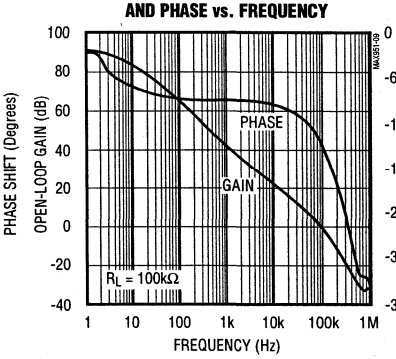
DC OPEN-LOOP GAIN vs. TEMPERATURE



MAX951/MAX953 OPEN-LOOP GAIN AND PHASE vs. FREQUENCY



MAX952/MAX954 OPEN-LOOP GAIN AND PHASE vs. FREQUENCY

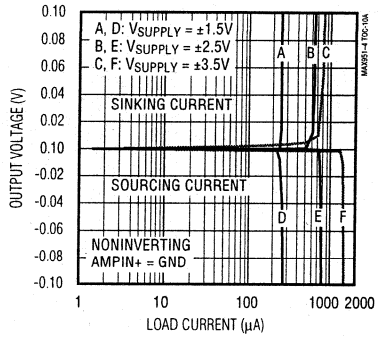


Ultra-Low-Power, Single-Supply Op Amp + Comparator + Reference

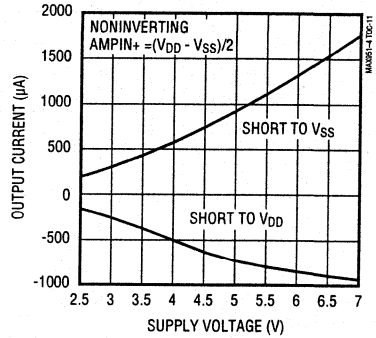
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

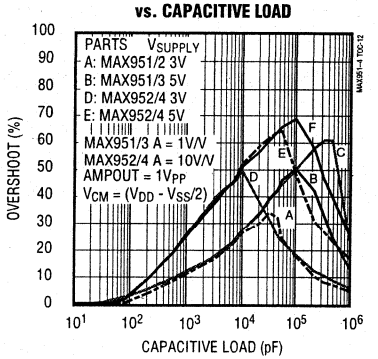
OP-AMP OUTPUT VOLTAGE vs. LOAD CURRENT



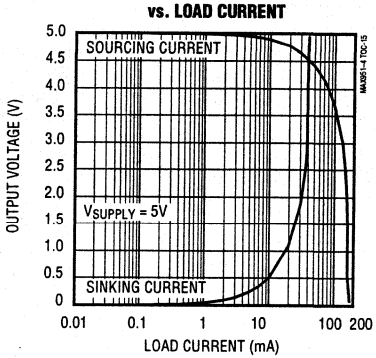
OP-AMP SHORT-CIRCUIT CURRENT vs. SUPPLY VOLTAGE



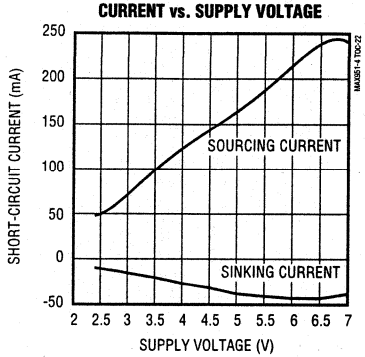
OP AMP PERCENT OVERSHOOT vs. CAPACITIVE LOAD



COMPARATOR OUTPUT VOLTAGE vs. LOAD CURRENT



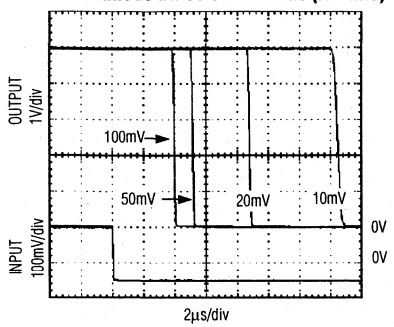
COMPARATOR SHORT-CIRCUIT CURRENT vs. SUPPLY VOLTAGE



Typical Operating Characteristics (continued)

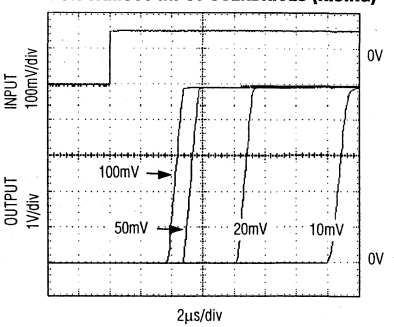
(T_A = +25°C, unless otherwise noted.)

COMPARATOR RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES (FALLING)



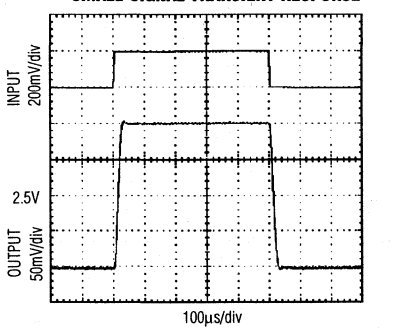
MAX953, LOAD = 100kΩ || 100pF, V_{SUPPLY} = 5V

COMPARATOR RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES (RISING)



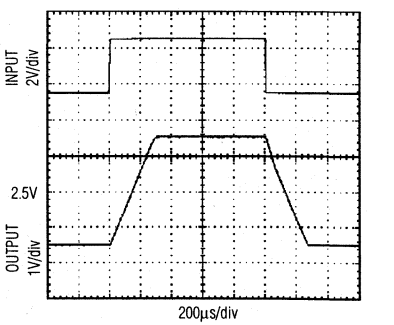
MAX953, LOAD = 100kΩ || 100pF, V_{SUPPLY} = 5V

MAX951/MAX953 OP-AMP SMALL-SIGNAL TRANSIENT RESPONSE



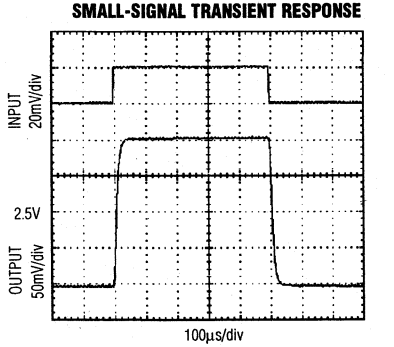
NONINVERTING, A_{VCL} = 1V/V, LOAD = 100kΩ || 100pF to V_{SS}, V_{SUPPLY} = 5V

MAX951/MAX953 OP-AMP LARGE-SIGNAL TRANSIENT RESPONSE



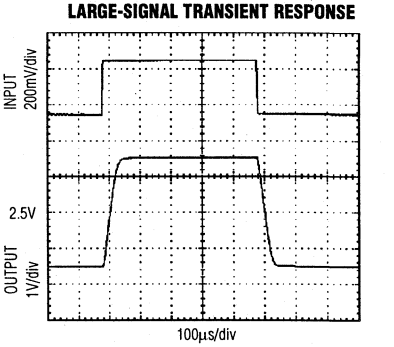
NONINVERTING, A_{VCL} = 1V/V, LOAD = 100kΩ || 100pF to V_{SS}, V_{SUPPLY} = 5V

MAX952/MAX954 OP-AMP SMALL-SIGNAL TRANSIENT RESPONSE



NONINVERTING, A_{VCL} = 10V/V, LOAD = 100kΩ || 100pF to V_{SS}, V_{SUPPLY} = 5V

MAX952/MAX954 OP-AMP LARGE-SIGNAL TRANSIENT RESPONSE



NONINVERTING, A_{VCL} = 10V/V, LOAD = 100kΩ || 100pF to V_{SS}, V_{SUPPLY} = 5V

Ultra-Low-Power, Single-Supply Op Amp + Comparator + Reference

Pin Description

PIN		NAME	FUNCTION
MAX951 MAX952	MAX953 MAX954		
1	1	AMPOUT	Op-Amp Output
2	2	AMPIN-	Inverting Op-Amp Input
3	3	AMPIN+	Noninverting Op-Amp Input
4	4	V_{SS}	Negative Supply or Ground
5	5	COMPIN+	Noninverting Comparator Input
6	—	REF	1.200V Reference Output. Also connected to inverting comparator input.
—	6	COMPIN-	Inverting Comparator Input
7	7	COMPOUT	Comparator Output
8	8	V_{DD}	Positive Supply

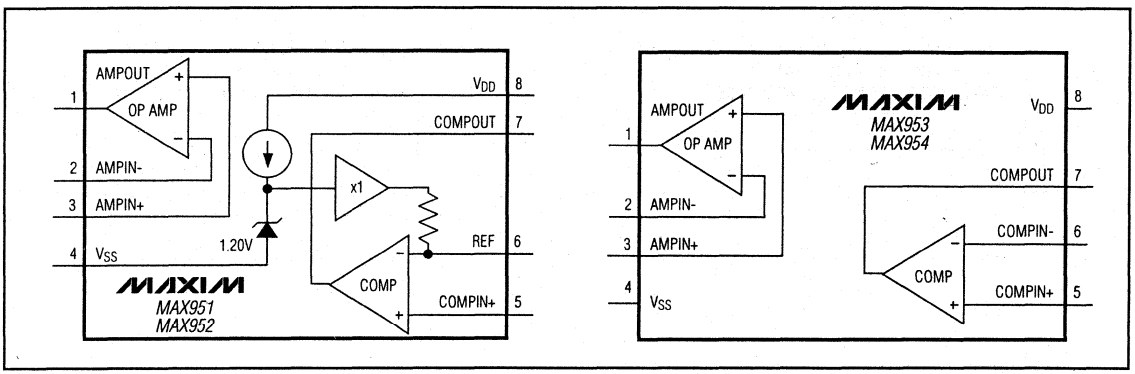


Figure 1. MAX951–MAX954 Functional Diagrams

Detailed Description

The MAX951–MAX954 are combinations of a micropower op amp, comparator, and reference in an 8-pin package, as shown in Figure 1. In the MAX951/MAX952, the comparator's negative input is connected to a 1.20V ±2% bandgap reference. All four devices are optimized to operate from a single supply. Supply current is less than 10µA (7µA typical) for the MAX951/MAX952 and less than 8µA (5µA typical) for the MAX953/MAX954.

Op Amp

The op amps in the MAX951/MAX953 are internally compensated to be unity-gain stable, while the op amps in the MAX952/MAX954 feature 125kHz typical gain bandwidth, 66V/ms slew rate, and stability for gains of 10V/V or greater. All these op amps feature high-impedance differential inputs and a common-mode input voltage range that extends from the negative supply rail to within 1.6V of the positive rail. They have a CMOS output stage that swings rail to rail and is driven by a proprietary high gain stage, which enables them to operate with an ultra-low supply current while maintaining linearity under loaded conditions. Careful design results in good DC characteristics over their entire operating temperature range, minimizing input referred errors.

Comparator

The comparator in the MAX951–MAX954 has a high-impedance differential input stage with a common-mode input voltage range that extends from the negative supply rail to within 1.6V of the positive rail. Their CMOS output stage swings rail to rail and can

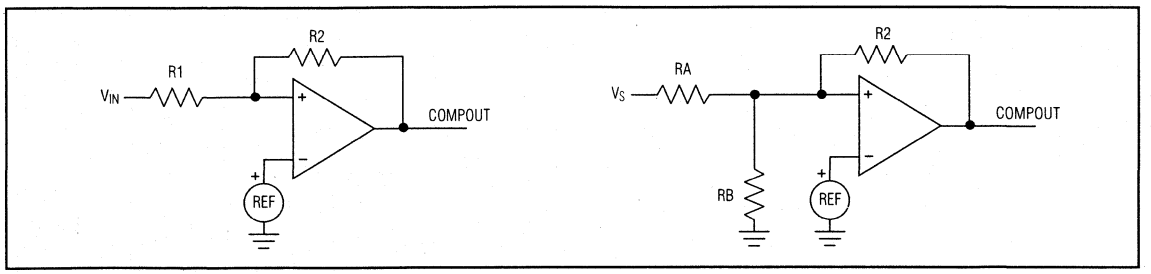


Figure 2. External Hysteresis

continuously source as much as 40mA. The comparators eliminate power-supply glitches that commonly occur when changing logic states, minimizing parasitic feedback and making them easier to use. In addition, they include internal hysteresis (±3mV) to ensure clean output switching, even with slow-moving input signals. The inputs can be taken above and below the supply rails up to 300mV without damage. Input voltages beyond this range can forward bias the ESD-protection diodes and should be avoided.

The MAX951–MAX954 comparator outputs swing rail to rail (from V_{DD} to V_{SS}). TTL compatibility is assured by using a +5V ±10% supply.

The MAX951–MAX954 comparator continuously outputs source currents as high as 40mA and sink currents of over 5mA, while keeping quiescent currents in the microampere range. The output can source 100mA (at V_{DD} = 5V) for short pulses, as long as the package's maximum power dissipation is not exceeded. The output stage does not generate crowbar switching currents during transitions; this minimizes feedback through the supplies and helps ensure stability without bypassing.

Reference

The internal reference in the MAX951/MAX952 has an output of 1.20V with respect to V_{SS}. Its accuracy is ±2% in the -40°C to +85°C temperature range. It is comprised of a trimmed bandgap reference fed by a proportional-to-absolute-temperature (PTAT) current source and buffered by a micropower unity-gain amplifier. The REF output is typically capable of sourcing and sinking 20µA. Do not bypass the reference output. The reference is stable for capacitive loads less than 100pF.

Applications Information

The micropower MAX951–MAX954 are designed to extend battery life in portable instruments and add functionality in power-limited industrial controls. Following are some practical considerations for circuit design and layout.

Comparator Hysteresis

Hysteresis increases the comparator's noise immunity by increasing the upper threshold and decreasing the lower threshold. The comparator in these devices contain a ±3mV wide internal hysteresis band to ensure clean output switching, even with slow-moving signals.

When necessary, hysteresis can be increased by using external resistors to add positive feedback, as shown in Figure 2. This circuit increases hysteresis at the expense of more supply current and a slower response. The design procedure is as follows:

1) Set R2. The leakage current in COMPIN+ is less than 5nA (up to +85°C), so current through R2 can be as little as 500nA and still maintain good accuracy. If R2 = 2.4MΩ, the current through R2 at the upper trip point is V_{REF} / R2 or 500nA.

2) Choose the width of the hysteresis band. In this example choose V_{EHYST} = 50mV.

$$R1 = R2\frac{[V_{EHYST} - 2V_{IHYST}]}{(V_{DD} + 2V_{IHYST})}$$

where the internal hysteresis is V_{IHYST} = 3mV.

3) Determine R1. If the supply voltage is 5V, then R1 = 24kΩ.

4) Check the hysteresis trip points. The upper trip point is

$$V_{IN(H)} = \frac{(R1 + R2)}{R2}(V_{REF} + V_{IHYST})$$

or 1.22V in our example. The lower trip point is 50mV less, or 1.17V in our example.

If a resistor divider is used for R1, the calculations should be modified using a Thevenin equivalent model.

5) Determine R_A:

Ultra-Low-Power, Single-Supply Op Amp + Comparator + Reference

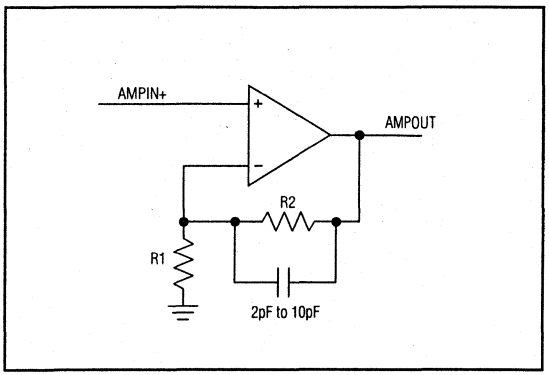


Figure 3. Compensation for Feedback-Node Capacitance

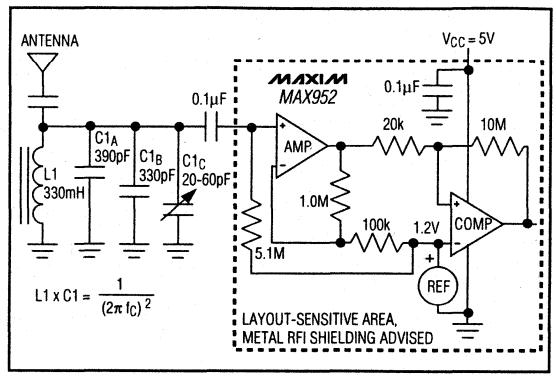


Figure 4. Low-Frequency Radio Receiver Application

$$R_A \approx R2\frac{V_{SHYST}}{V_{DD}}, \text{ for } V_{SHYST} >> V_{IHYST}$$

In the example, R_A is again 24kΩ.

6) Select the upper trip point $V_{S(H)}$. Our example is set at 4.75V.

7) Calculate R_B.

$$R_B = \frac{(V_{REF} + V_{IHYST})(R2)(R_A)}{(R2)(V_{S(H)}) - (V_{REF} + V_{IHSYT})(R_A + R2)}$$

R_B is 8.19kΩ, or approximately 8.2kΩ.

Input Noise Considerations

Because low power requirements often demand high-impedance circuits, effects from radiated noise are more significant. Thus, traces between the op-amp or comparator inputs and any resistor networks attached should be kept as short as possible.

Crosstalk

Reference

Internal crosstalk to the reference from the comparator is package dependent. Typical values (V_{DD} = 5V) are 45mV for the plastic DIP package and 32mV for the SO package. Applications using the reference for the op amp or external circuitry can eliminate this crosstalk by using a simple RC lowpass filter, as shown in Figure 5.

Op Amp

Internal crosstalk to the op amp from the comparator is package dependent, but not input referred. Typical values (V_{DD} = 5V) are 4mV for the plastic DIP package and 280µV for the SO package.

Op-Amp Stability and Board Layout Considerations

Unlike other industry-standard micropower CMOS op amps, the op amps in the MAX951–MAX954 maintain stability in their minimum gain configuration while driving heavy capacitive loads, as demonstrated in the MAX951/MAX953 Op-Amp Percent Overshoot vs. Capacitive Load graph in the *Typical Operating Characteristics*.

Although this family is primarily designed for low-frequency applications, good layout is extremely important. Low-power, high-impedance circuits may increase the effects of board leakage and stray capacitance. For example, the combination of a 10MΩ resistance (from leakage between traces on a contaminated, poorly designed PC board) and a 1pF stray capacitance provides a pole at approximately 16kHz, which is near the amplifier's bandwidth. Board routing and layout should minimize leakage and stray capacitance. In some cases, stray capacitance may be unavoidable and it may be necessary to add a 2pF to 10pF capacitor across the feedback resistor to compensate; select the smallest capacitor value that ensures stability.

Input Overdrive

With 100mV overdrive, comparator propagation delay is typically 6µs. The *Typical Operating Characteristics* show propagation delay for various overdrive levels.

Supply current can increase when the op amp in the MAX951–MAX954 is overdriven to the negative supply rail. For example, when connecting the op amp as a comparator and applying a -100mV input overdrive, supply current rises by around 15µA and 32µA for supply voltages of 2.8V and 7V, respectively.

Ultra-Low-Power, Single-Supply Op Amp + Comparator + Reference

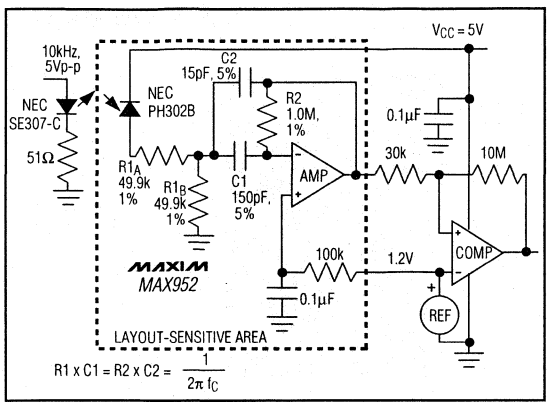


Figure 5. Infrared Receiver Application

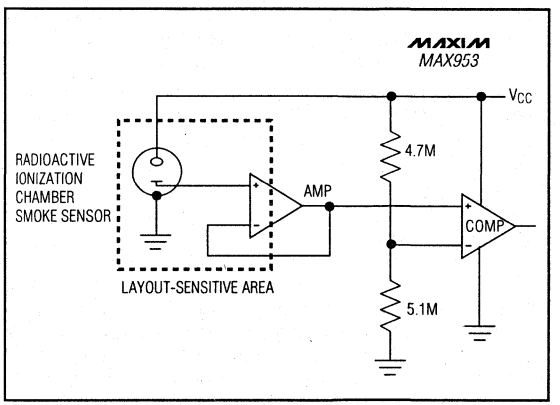


Figure 6. Sensor Preamp and Alarm Trigger Application

Power-Supply Bypassing

Power-supply bypass capacitors are not required if the supply impedance is low. For single-supply applications, it is good general practice to bypass V_{DD} with a. 0.1µF capacitor to ground. Do not bypass the reference output.

Application Circuits

Low-Frequency Radio Receiver for Alarms and Detectors

Figure 4's circuit is useful as a front end for low-frequency RF alarms. The unshielded inductor (M7334-ND from Digikey) is used with capacitors $C1_A$, $C1_B$, and $C1_C$ in a resonant circuit to provide frequency selectivity. The op amp from a MAX952 amplifies the signal received. The comparator improves noise immunity, provides a signal strength threshold, and translates the received signal into a pulse train. Carrier frequencies are limited to around 10kHz. 10kHz is used in the example in Figure 4.

The layout and routing of components for the amplifier should be tight to minimize 60Hz interference and crosstalk from the comparator. Metal shielding is recommended to prevent RFI from the comparator or digital circuitry from exciting the receiving antenna. The transmitting antenna can be long parallel wires spaced about 7.2cm apart, with equal but opposite currents. Radio waves from this antenna will be detectable when the receiver is brought within close proximity, but cancel out at greater distances.

Infrared Receiver Front End for Remote Controls and Data Links

The circuit in Figure 5 uses the MAX952 as a PIN photodiode preamplifier and discriminator for an infrared receiver. The op amp is configured as a Delyiannis-Friend bandpass filter to reduce disturbances from noise and eliminate low-frequency interference from sunlight, fluorescent lights, etc. This circuit is applicable for TV remote controls and low-frequency data links up to 20kbps. Carrier frequencies are limited to around 10kHz. 10kHz is used in the example circuit.

Component layout and routing for the amplifier should be tight to reduce stray capacitance, 60Hz interference, and RFI from the comparator. Crosstalk from comparator edges will distort the amplifier signal. In order to minimize the effect, a lowpass RC filter is added to the connection from the reference to the noninverting input of the op amp.

Sensor Preamp and Alarm Trigger for Smoke Detectors

The high-impedance CMOS inputs of the MAX951–MAX954 op amp are ideal for buffering high-impedance sensors, such as smoke detector ionization chambers, piezoelectric transducers, gas detectors, and pH sensors. Input bias currents are typically less than 3pA at room temperature. A 5µA typical quiescent current for the MAX953 will minimize battery drain without resorting to complex sleep schemes, allowing continuous monitoring and immediate detection.

Ionization-type smoke detectors use a radioactive source, such as Americium, to ionize smoke particles. A positive voltage on a plate attached to the source repels the positive smoke ions and accelerates them toward an outer electrode connected to ground. Some ions collect on an intermediate plate. With careful design, the voltage on this plate will stabilize at a little less than one-half the supply voltage under normal conditions, but rise higher when smoke increases the ion current. This voltage is buffered

Ultra-Low-Power, Single-Supply Op Amp + Comparator + Reference

by the high input impedance op amp of a MAX951 (Figure 6). The comparator and resistor voltage divider set an alarm threshold to indicate a fire.

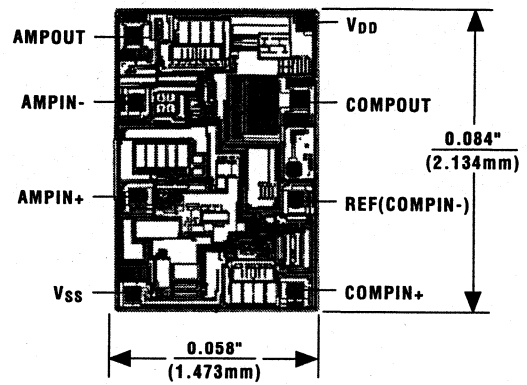
Design and fabrication of the connection from the intermediate plate of the ionization chamber to the noninverting input of the op amp is critical, since the impedance of this node must be well above 50MΩ. This connection must be as short and direct as possible to prevent charge leakage and 60Hz interference. Where possible, the grounded outer electrode or chassis of the ionization chamber should shield this connection to reduce 60Hz interference. Pay special attention to board cleaning, to prevent leakage due to ionic compounds such as chlorides, flux, and other contaminants from the manufacturing process. Where applicable, a coating of high-purity wax may be used to insulate this connection and prevent leakage due to surface moisture or an accumulation of dirt.

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX951C/D	0°C to +70°C	Dice*
MAX951EPA	-40°C to +85°C	8 Plastic DIP
MAX951ESA	-40°C to +85°C	8 SO
MAX951EUA	-40°C to +85°C	8 µMAX
MAX951MJA	-55°C to +125°C	8 CERDIP**
MAX952C/D	0°C to +70°C	Dice*
MAX952EPA	-40°C to +85°C	8 Plastic DIP
MAX952ESA	-40°C to +85°C	8 SO
MAX952EUA	-40°C to +85°C	8 µMAX
MAX952MJA	-55°C to +125°C	8 CERDIP**
MAX953C/D	0°C to +70°C	Dice*
MAX953EPA	-40°C to +85°C	8 Plastic DIP
MAX953ESA	-40°C to +85°C	8 SO
MAX953EUA	-40°C to +85°C	8 µMAX
MAX953MJA	-55°C to +125°C	8 CERDIP**
MAX954C/D	0°C to +70°C	Dice*
MAX954EPA	-40°C to +85°C	8 Plastic DIP
MAX954ESA	-40°C to +85°C	8 SO
MAX954EUA	-40°C to +85°C	8 µMAX
MAX954MJA	-55°C to +125°C	8 CERDIP**

** Dice are tested at T_A = +25°C, DC parameters only.*
*** Contact factory for availability and processing to MIL-STD-883.*

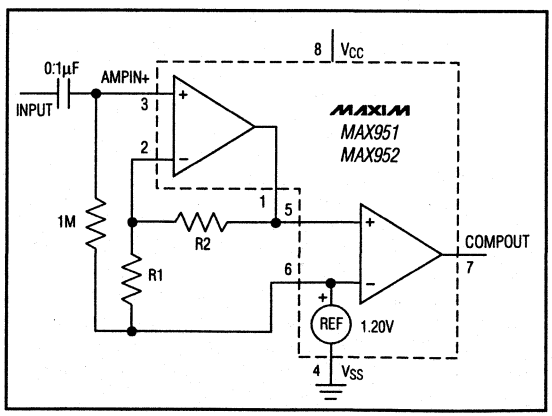
Chip Topography



( ) ARE FOR MAX953/MAX954

TRANSISTOR COUNT: 163
SUBSTRATE CONNECTED TO V_{DD}

Typical Operating Circuit



19-1129; Rev 0; 9/96

MAXIM

High-Speed, 3V/5V, Rail-to-Rail, Single-Supply Comparators

General Description

The MAX961/MAX962 are high-speed, single/dual comparators with internal hysteresis. These devices are optimized for single +3V or +5V operation. The input common-mode range extends beyond both supply rails, and the outputs can sink or source 4mA to within 0.5V of GND and V_{CC}. Propagation delay is under 7ns (5mV overdrive), while supply current is 8.5mA/comparator..

The single MAX961 features complementary outputs, a low-power shutdown mode, and a latch-enable function. The latch function enables the user to hold a valid comparator output. In shutdown mode, the MAX961 consumes only 500µA (max) supply current. The single MAX961 and dual MAX962 are available in 8-pin SO and space-saving µMAX packages.

Features

- **Ultra-Fast, 7ns Propagation Delay**
- **Optimized for +3V and +5V Single-Supply Applications**
- **Rail-to-Rail Input Voltage Range**
- **Internal Hysteresis for Clean Switching**
- **Output Latch (MAX961)**
- **TTL/CMOS-Compatible Complementary Outputs**
- **500µA (max) Shutdown Current (MAX961)**
- **8-Pin SO/µMAX Packages**

Applications

3V/5V Systems

Battery-Powered Systems

Threshold Detectors/Discriminators

Line Receivers

Zero-Crossing Detectors

High-Speed Sampling Circuits

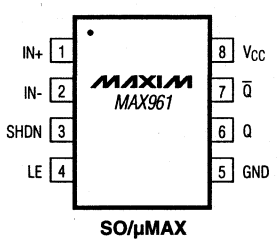
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX961ESA	-40°C to +85°C	8 SO
MAX961EUA	-40°C to +85°C	8 µMAX
MAX962ESA	-40°C to +85°C	8 SO
MAX962EUA	-40°C to +85°C	8 µMAX

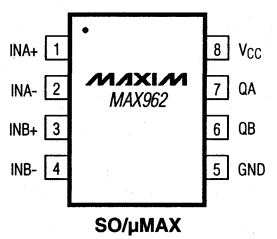
3

Pin Configurations

TOP VIEW



SO/µMAX



SO/µMAX

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

High-Speed, 3V/5V, Rail-to-Rail, Single-Supply Comparators

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} to GND.....+9V to -0.3V
All Other Pins.....-0.3V to (V_{CC} + 0.3V)
Duration of Output Short Circuit to GND or V_{CC} .....Continuous
Continuous Power Dissipation (T_A = +70°C)
SO (derate 5.88mW/°C above +70°C).....471mW
µMAX (derate 4.1mW/°C above +70°C) 330mW

Operating Temperature Range
MAX96_E .....-40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +8V, V_{CM} = 0V, C_{OUT} = 5pF, V_{SHDN} = 0V, V_{LE} = 0V, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		T_A = +25°C			T_{MIN} to T_{MAX}		UNITS
				MIN	TYP	MAX	MIN	MAX	
Supply Voltage	V_{CC}	Inferred by PSRR		2.7		8	2.7	8	V
Input Voltage Range	V_{CMR}	(Note 2)		-0.1		V_{CC} + 0.1	-0.1	V_{CC} + 0.1	V
Input-Referred Trip Points	V_{TRIP}	V_{CM} = 0V or V_{CC}, V_{CC} = 5V (Note 3)	MAX96_SA		1.0	3.5		4.0	mV
			MAX96_UA		1.0	3.5		5.2	
Input Offset Voltage	V_{OS}	V_{CM} = 0V or V_{CC}, V_{CC} = 5V (Note 4)	MAX96_SA		0.5	1.5		2.0	mV
			MAX96_UA		0.5	1.5		3.5	
Input Bias Current	I_B	V_{IN+} = V_{IN-} = 0V or V_{CC}, V_{CC} = 5V	MAX96_SA			±15		±15	µA
			MAX96_UA			±15		±30	
Differential Input Clamp Voltage		V_{CC} = 8V, V_{IN-} = 0V, I(IN+) = 100µA				3.6			V
Input Capacitance					3				pF
Differential Input Impedance	R_{IND}	V_{CC} = 5V			8				kΩ
Common-Mode Input Impedance	R_{INCM}	V_{CC} = 5V			130				kΩ
Common-Mode Rejection Ratio	CMRR	V_{CC} = 5V, V_{CM} = -0.1V to 5.1V (Note 5)			0.1	0.3		0.5	mV/V
Power-Supply Rejection Ratio	PSRR	V_{CM} = 0V (Note 6)			0.05	0.3		0.3	mV/V
Output High Voltage	V_{OH}	I_{SOURCE} = 4mA		V_{CC} - 0.52			V_{CC} - 0.52		V
Output Low Voltage	V_{OL}	I_{SINK} = 4mA				0.52		0.52	V
Capacitive Slew Current		V_{OUT} = 1.4V, V_{CC} = 2.7V		30	60				mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.7V to +8V, V_{CM} = 0V, C_{OUT} = 5pF, V_{SHDN} = 0V, V_{LE} = 0V, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			T_{MIN} to T_{MAX}		UNITS
			MIN	TYP	MAX	MIN	MAX	
Output Capacitance				4				pF
Supply Current	I_S	MAX961, V_{CC} = 5V		8.5	11		11	mA
		MAX962, V_{CC} = 5V		11	16		17	mA
Shutdown Supply Current	I_{SHDN}	MAX961, V_{CC} = 5V		0.27	0.5		0.5	mA
Shutdown Output Current		MAX961, V_{OUT} = 0.5V and V_{CC} - 0.5V			1		10	µA
Rise/Fall Time	t_R, t_F	V_{CC} = 5V		2.3				ns
Logic Input High	V_{IH}		(V_{CC} / 2) + 0.4	V_{CC} / 2		(V_{CC} / 2) + 0.4		V
Logic Input Low	V_{IL}			V_{CC} / 2	(V_{CC} / 2) - 0.4		(V_{CC} / 2) - 0.4	V
Logic Input Current	I_{IL}, I_{IH}	V_{LOGIC} = 0V or V_{CC}			15		15	µA
Propagation Delay	t_{PD}	(Note 7)		4.5	7		8.5	ns
Differential Propagation Delay	t_{PD}	Between any two channels or outputs ($Q/\overline{Q}$)		0.3				ns
Propagation-Delay Skew	t_{SKEW}	Between t_{pd-} and t_{pd+}		0.3				ns
Data-to-Latch Setup Time	t_{SU}	(Note 8)			5		5	ns
Latch-to-Data Hold Time	t_H	(Note 8)			5		5	ns
Latch Pulse Width	t_{LPW}	(Note 8)			5		5	ns
Latch Propagation Delay	t_{LPD}	(Note 8)			10		10	ns
Shutdown Time	t_{ESHDN}	Delay until output is high-Z (>10Ω)		150				ns
Shutdown Disable Time	t_{DSHDN}	Delay until output is valid		250				ns

Note 1: V_{CM} is defined as the average voltage of V_{IN+} and V_{IN-}.

Note 2: Inferred by CMRR. Either input can be driven to the absolute maximum limit without false output inversion, as long as the other input is within the input voltage range.

Note 3: The input-referred trip points are the extremities of the differential input voltage required to make the comparator output change state. The difference between the upper and lower trip points is equal to the width of the input-referred hysteresis zone. See Figure 1.

Note 4: Input offset voltage is defined as the mean of the trip points.

Note 5: CMRR = (V_{OS} - V_{OSV4}) / 5.2V, where V_{OSL} is the offset at V_{CM} = -0.1V and V_{OSV4} is the offset at V_{CM} = 5.1V.

Note 6: PSRR = ($V_{OS}2.7$ - $V_{OS}8$) / 5.3V, where $V_{OS}2.7$ is the offset voltage at V_{CC} = 2.7V, and $V_{OS}8$ is the offset voltage at V_{CC} = 8V.

Note 7: 5mV overdrive, C_{OUT} = 5pF, either direction, guaranteed by sample test. Transitions are measured from the point where V_{IN+} crosses V_{IN-}, to the point where the output crosses V_{CC} / 2. Overdrive is above and beyond the offset voltage.

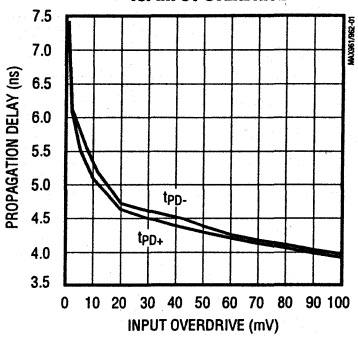
Note 8: Guaranteed by design.

High-Speed, 3V/5V, Rail-to-Rail, Single-Supply Comparators

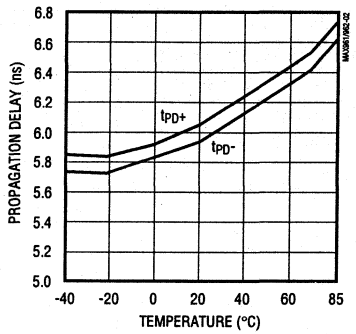
Typical Operating Characteristics

(V_{CC} = +3.0V, 5mV of overdrive, T_A = +25°C, unless otherwise noted.)

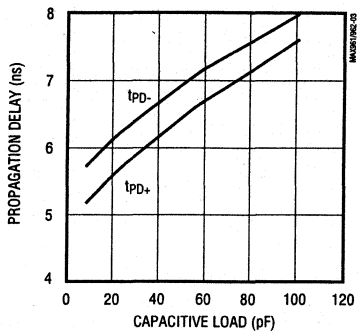
PROPAGATION DELAY vs. INPUT OVERDRIVE



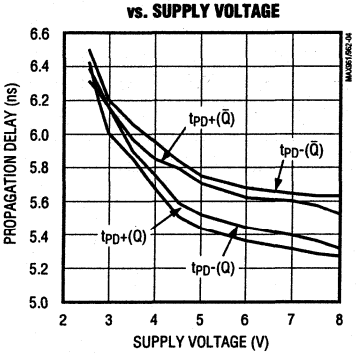
PROPAGATION DELAY vs. TEMPERATURE



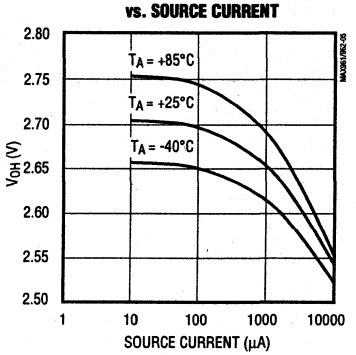
PROPAGATION DELAY vs. CAPACITIVE LOAD



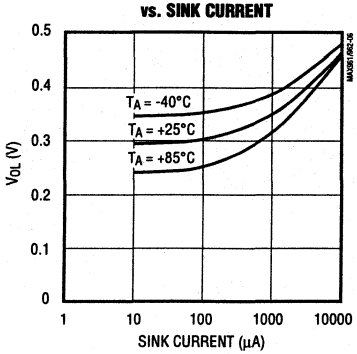
PROPAGATION DELAY vs. SUPPLY VOLTAGE



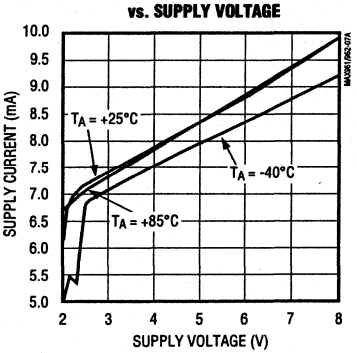
OUTPUT HIGH VOLTAGE vs. SOURCE CURRENT



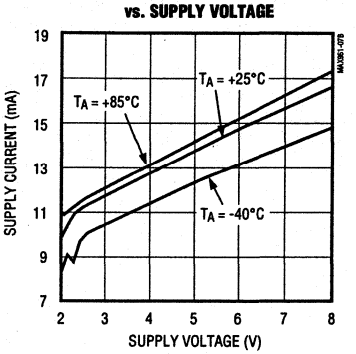
OUTPUT LOW VOLTAGE vs. SINK CURRENT



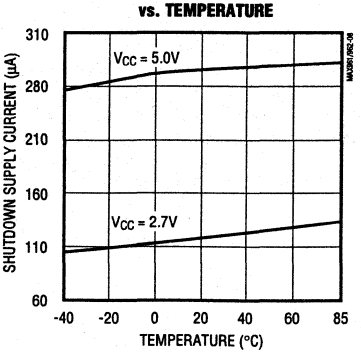
MAX961 SUPPLY CURRENT vs. SUPPLY VOLTAGE



MAX962 SUPPLY CURRENT vs. SUPPLY VOLTAGE



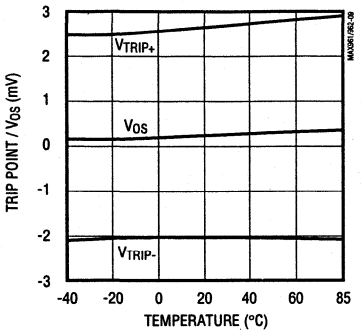
MAX961 SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



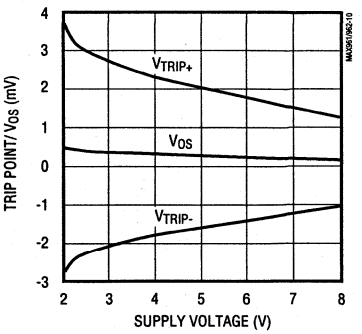
Typical Operating Characteristics (continued)

(V_{CC} = +3.0V, 5mV of overdrive, T_A = +25°C, unless otherwise noted.)

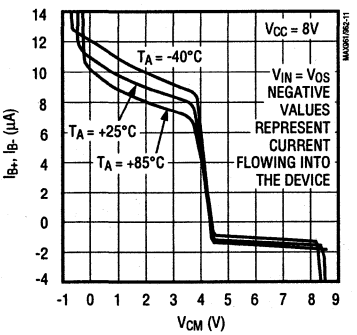
VOLTAGE TRIP POINT/INPUT OFFSET VOLTAGE vs. TEMPERATURE



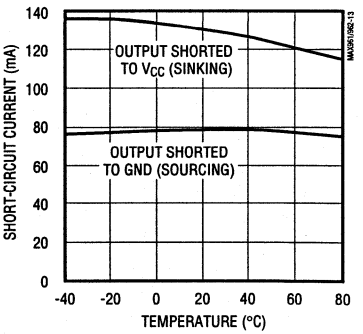
VOLTAGE TRIP POINTS/INPUT OFFSET VOLTAGE vs. SUPPLY VOLTAGE



INPUT BIAS CURRENT (I_{B+}, I_{B-}) vs. COMMON-MODE VOLTAGE



SHORT-CIRCUIT OUTPUT CURRENT vs. TEMPERATURE

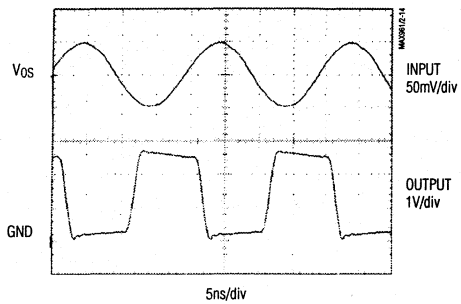


High-Speed, 3V/5V, Rail-to-Rail, Single-Supply Comparators

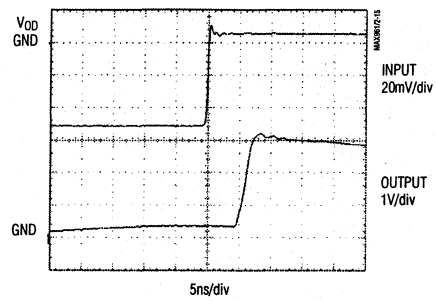
Typical Operating Characteristics (continued)

(V_{CC} = +3.0V, 5mV of overdrive, T_A = +25°C, unless otherwise noted.)

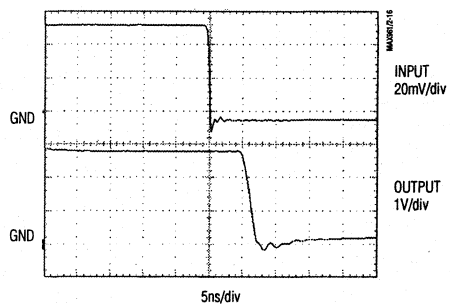
50MHz RESPONSE



PROPAGATION DELAY (t_{PD+})



PROPAGATION DELAY (t_{PD-})



Pin Description

PIN		NAME	FUNCTION
MAX961	MAX962		
1	—	IN+	Comparator Noninverting Input
2	—	IN-	Comparator Inverting Input
—	1	INA+	Comparator A Noninverting Input
—	2	INA-	Comparator A Inverting Input
3	—	SHDN	Shutdown Input. MAX961 shuts down when SHDN is high
—	3	INB+	Comparator B Noninverting Input
—	4	INB-	Comparator B Inverting Input
4	—	LE	Latch Enable Input. The output latches when LE is high. The latch is transparent when LE is low.
5	5	GND	Ground
—	6	QB	Comparator B Output
6	—	Q	Comparator Output
—	7	QA	Comparator A Output
7	—	$\overline{Q}$	Comparator Complementary Output
8	8	V_{CC}	Positive Supply Input (V_{CC} to GND must be ≤8V)

Detailed Description

The MAX961/MAX962 single-supply comparators feature internal hysteresis, high speed, and low power. Their outputs are guaranteed to pull within 0.52V of either rail without external pull-up or pull-down circuitry. Rail-to-rail input voltage range and low-voltage, single-supply operation make these devices ideal for portable equipment. The MAX961/MAX962 both interface directly to CMOS logic.

Timing

Most high-speed comparators oscillate in the linear region because of noise or undesirable parasitic feedback. This can occur when the voltage on one input is close to or equal to the voltage on the other input. The MAX961/MAX962 have a small amount of internal hysteresis to counter parasitic effects and noise.

The added hysteresis of the MAX961/MAX962 creates two trip points: one for the rising input voltage and one for the falling input voltage (Figure 1). The difference between the trip points is the hysteresis. When the comparator's input voltages are equal, the hysteresis effectively causes one comparator input voltage to move quickly past the other, thus taking the input out of the region where oscillation occurs. Standard comparators require hysteresis to be added with external resistors. The MAX961/MAX962's fixed internal hysteresis eliminates these resistors.

Figure 1 illustrates the case where IN- is fixed and IN+ is varied. If the inputs were reversed, the figure would look the same, except for an inverted output.

The MAX961 includes an internal latch that allows storage of comparison results. LE has a high input impedance. If LE is low, the latch is transparent (i.e., the comparator operates as though the latch is not present). The comparator's output state is stored when LE is pulled high. All timing constraints must be met when using the latch function (Figure 2).

Input Stage Circuitry

The MAX961/MAX962 include internal protection circuitry that prevents damage to the precision input stage from large differential input voltages. This protection circuitry consists of two groups of five front-to-back diodes between IN+ and IN-, as well as two 200Ω resistors (Figure 3). The diodes limit the differential voltage applied to the internal circuitry of the comparators to no more than $5V_F$, where V_F is the diode's forward-voltage drop (about 0.7V at +25°C).

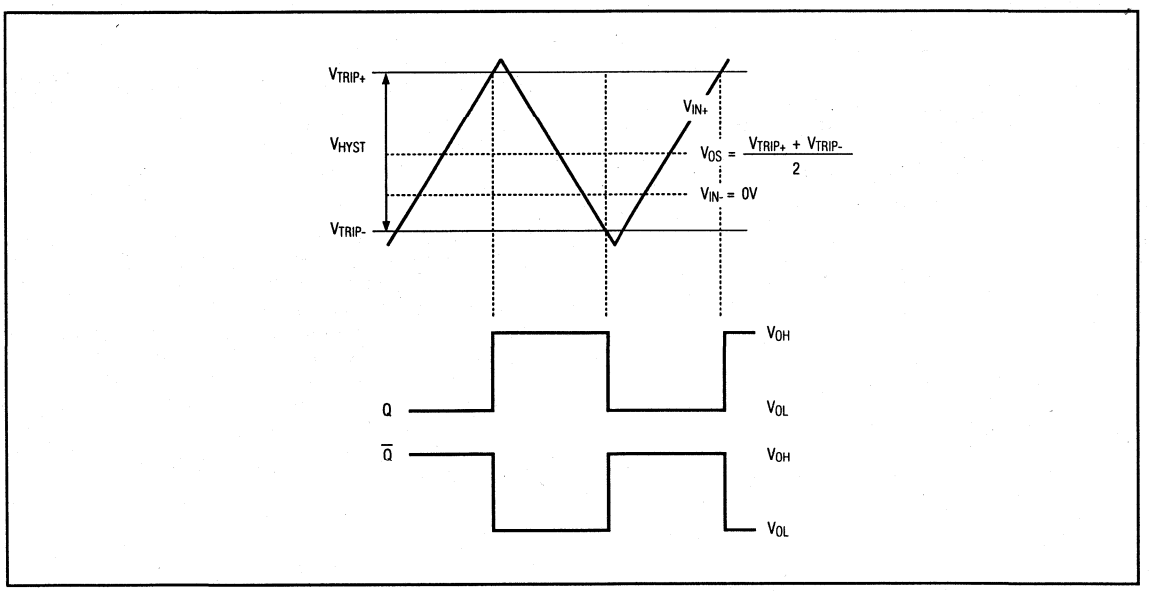


Figure 1. Input and Output Waveform, Noninverting Input Varied

High-Speed, 3V/5V, Rail-to-Rail, Single-Supply Comparators

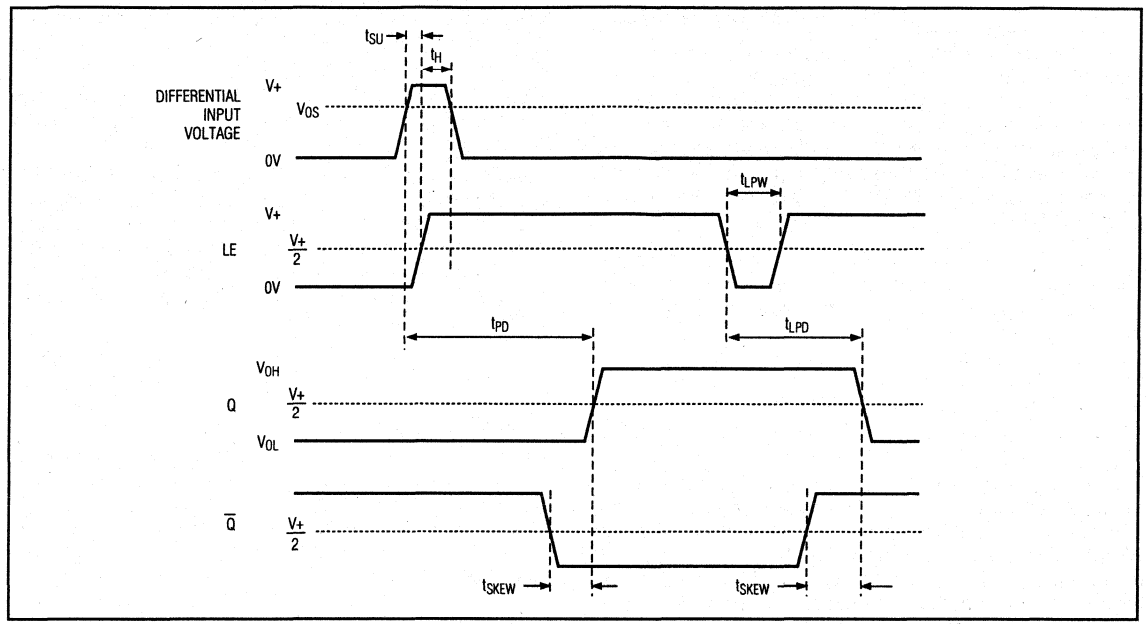


Figure 2. MAX961 Timing Diagram

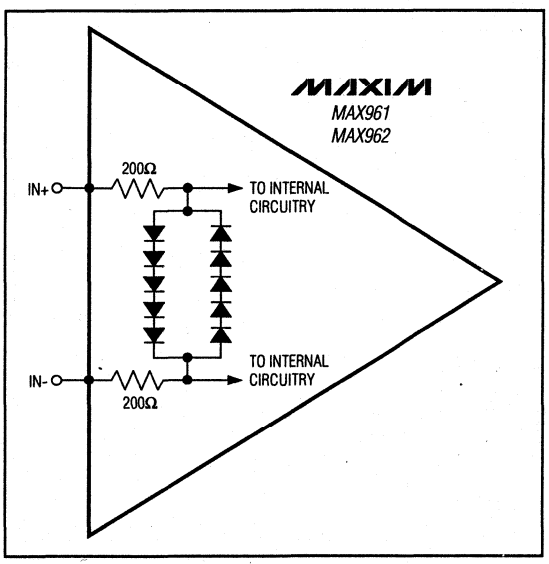


Figure 3. Input Stage Circuitry

For a large differential input voltage (exceeding $5V_F$), this protection circuitry increases the input bias current at IN+ (source) and IN- (sink).

$$\text{Input current} = \frac{(IN+ - IN-) - 5V_F}{2 \times 200}$$

Input currents with large differential input voltages should not be confused with input bias currents (I_B). As long as the differential input voltage is less than $5V_F$, this input current is less than $2I_B$. The protection circuitry also allows for the MAX961/MAX962's input common-mode range to extend beyond both power-supply rails. The output remains in the correct logic state if one or both inputs are within the common-mode range. Taking either input outside the common-mode range causes the output to saturate and the propagation delay to worsen.

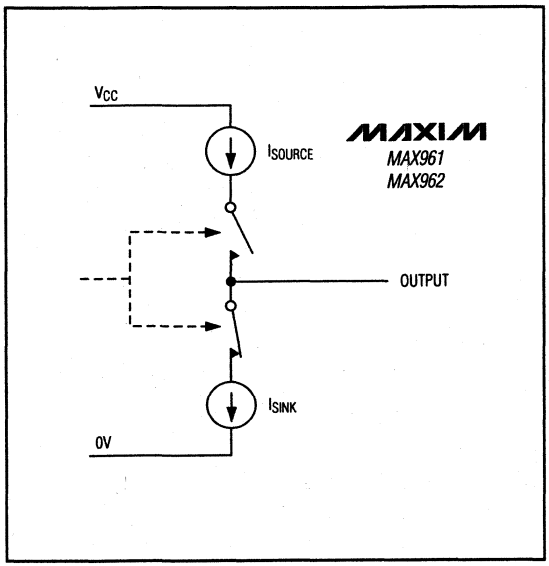


Figure 4. Output Stage Circuitry

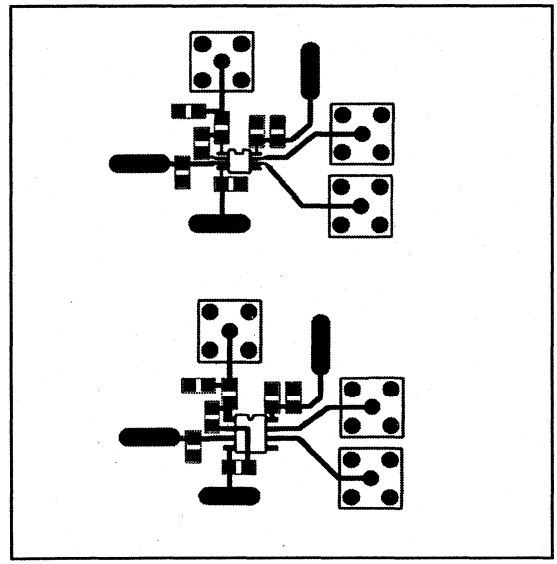


Figure 5. MAX961 PC Layout

Output-Stage Circuitry

The MAX961/MAX962 contain a current-driven output stage, as shown in Figure 4. During an output transition, I_{SOURCE} or I_{SINK} is pushed or pulled to the output pin. The output source or sink current is high during the transition, creating a rapid slew rate. Once the output voltage reaches V_{OH} or V_{OL}, the source or sink current decreases to a small value, capable of maintaining the V_{OH} or V_{OL} in static condition. This decrease in current conserves power after an output transition has occurred.

One consequence of a current-driven output stage is a linear dependence between the slew rate and the load capacitance. A heavy capacitive load slows down the voltage output transition. This is useful in noise-sensitive applications, where fast edges may cause interference.

Shutdown Mode

The MAX961 shuts down when SHDN is high. When shut down, the supply current drops to less than 500µA, and the outputs become high impedance. SHDN has a high input impedance. Connect the SHDN pin to GND for normal operation. Exit shutdown with LE low; otherwise, the output is indeterminate.

Applications Information

Circuit Layout Bypassing

The high-gain bandwidth of the MAX961/MAX962 requires a high-speed layout:

1) Use a printed circuit board with a good, unbroken, low-inductance ground plane.
2) Place a decoupling capacitor (a 0.1µF ceramic surface-mount capacitor is a good choice) as close to V_{CC} as possible.
3) On the inputs and outputs, keep lead lengths short to avoid unwanted parasitic feedback around the comparators. Keep inputs away from outputs. Keep impedance between the inputs low.
4) Solder the device directly to the printed circuit board rather than using a socket.
5) Figure 5 depicts the recommended circuit layout.

Chip Information

TRANSISTOR COUNT: 286

19-0450; Rev 0; 11/95

MAXIM

Ultra-Low-Power, Open-Drain, Single/Dual-Supply Comparators

General Description

The MAX971–MAX974 and MAX981–MAX984 single/dual/quad low-voltage comparators feature the lowest power consumption available. These micropower devices draw less than 4µA supply current over temperature (MAX971/MAX972, MAX981/MAX982), and include an internal 1.182V ±1% (MAX971/MAX973/MAX974) or ±2% (MAX981–MAX984) voltage reference and programmable hysteresis.

Ideal for 3V or 5V single-supply applications, these devices operate from a single +2.5V to +11V supply (or ±1.25V to ±5.5V dual supplies), and each comparator's input voltage ranges from the negative supply rail to within 1.3V of the positive supply.

The single MAX971 and MAX981 and the dual MAX973 and MAX982/MAX983 provide a unique, simple method for adding hysteresis without feedback or complicated equations, simply by using the HYST pin plus two resistors.

The MAX971–MAX974 and MAX981–MAX984's open-drain outputs permit wire-ORed configurations. Thanks to an 11V output range and separate GND pin for the output transistor (MAX971/MAX974, MAX981/MAX984), these devices are ideal for level translators and bipolar to single-ended converters. For similar devices with complementary output stages, see the MAX921–MAX924 (1% reference) and the MAX931–MAX934 (2% reference).

PART	INTERNAL PRECISION REFERENCE	COMPARATORS PER PACKAGE	INTERNAL HYSTERESIS	PACKAGE
MAX971	1%	1	Yes	8-Pin DIP/SO/µMAX
MAX972	None	2	No	8-Pin DIP/SO/µMAX
MAX973	1%	2	Yes	8-Pin DIP/SO/µMAX
MAX974	1%	4	No	16-Pin DIP/SO
MAX981	2%	1	Yes	8-Pin DIP/SO/µMAX
MAX982	2%	2	Yes	8-Pin DIP/SO/µMAX
MAX983	2%	2	Yes	8-Pin DIP/SO/µMAX
MAX984	2%	4	No	16-Pin DIP/SO

Features

- ♦ **µMAX Package—Smallest 8-Pin SO (MAX9_1/MAX9_2/MAX9_3)**
- ♦ **Ultra-Low 4µA Max Quiescent Current Over Extended Temp. Range (MAX971/MAX981)**
- ♦ **Power Supplies: Single +2.5V to +11V**
  Dual ±1.25V to ±5.5V
- ♦ **Input Voltage Range Includes Negative Supply**
- ♦ **Internal 1.182V ±1% Bandgap Reference**
- ♦ **12µs Propagation Delay (10mV Overdrive)**
- ♦ **Output Has Separate GND Pin (MAX9_1/MAX9_4)**

Applications

Battery-Powered Systems
Threshold Detectors
Window Comparators
Level Translators
Oscillator Circuits

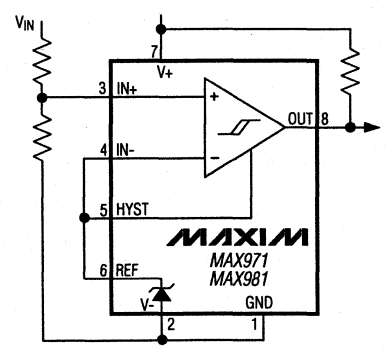
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX971CPA	0°C to +70°C	8 Plastic DIP
MAX971CSA	0°C to +70°C	8 SO
MAX971CUA	0°C to +70°C	8 µMAX
MAX971C/D	0°C to +70°C	Dice*

Ordering Information continued at end of data sheet.

** Dice are tested at T_A = +25°C, DC parameters only.*

Typical Operating Circuit



THRESHOLD DETECTOR

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Ultra-Low-Power, Open-Drain, Single/Dual-Supply Comparators

ABSOLUTE MAXIMUM RATINGS

V+ to V-, V+ to GND, GND to V- ..... -0.3V, +12V
Inputs
  Current: IN_+, IN_-, HYST 20mA
  Voltage: IN_+, IN_-, HYST ..... (V+ + 0.3V) to (V- - 0.3V)
Outputs
  Current: REF 20mA
    OUT_ 50mA
  Voltage: REF ..... (V+ + 0.3V) to (V- - 0.3V)
    OUT_ (MAX9_1/9_4) ..... +12V to (GND - 0.3V)
    (MAX9_2/9_3) ..... +12V to (V- - 0.3V)
  OUT_ Short-Circuit Duration ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
  8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) ... 727mW
  8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
  8-Pin µMAX (derate 4.1mW/°C above +70°C) 330mW
  8-Pin CERDIP (derate 8.00mW/°C above +70°C) 640mW
  16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) .. 842mW
  16-Pin SO (derate 8.70mW/°C above +70°C) 696mW
  16-Pin CERDIP (derate 10.00mW/°C above +70°C) 800mW
Operating Temperature Ranges
  MAX97_C_ _/MAX98_C_ _ ..... 0°C to +70°C
  MAX97_E_ _/MAX98_E_ _ ..... -40°C to +85°C
  MAX97_MJ_/MAX98_MJ_ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: 5V OPERATION

(V+ = 5V, V- = GND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
POWER REQUIREMENTS							
Supply Voltage Range	(Note 1)			2.5		11	V
Output Voltage Range				0		11	V
Supply Current	IN+ = IN- + 100mV	MAX9_1, HYST = REF	T_A = +25°C		2.5	3.2	µA
			C/E temp. ranges			4	
			M temp. range			5	
		MAX972	T_A = +25°C		2.5	3.2	
			C/E temp. ranges			4	
			M temp. range			5	
		MAX982/ MAX9_3, HYST = REF	T_A = +25°C		3.1	4.5	
			C/E temp. ranges			6	
			M temp. range			7.5	
		MAX9_4	T_A = +25°C		5.5	6.5	
			C/E temp. ranges			8.5	
			M temp. range			11	
COMPARATOR							
Input Offset Voltage	V_{CM} = 2.5V					±10	mV
Input Leakage Current (IN-, IN+)	IN+ = IN- = 2.5V		C/E temp. ranges		±0.01	±5	nA
			M temp. range			±40	
Input Leakage Current (HYST)	MAX9_1/MAX982/MAX9_3				±0.02		nA
Input Common-Mode Voltage Range				V-		V+ - 1.3	V
Common-Mode Rejection Ratio	V- to (V+ - 1.3V)				0.1	1.0	mV/V
Power-Supply Rejection Ratio	V+ = 2.5V to 11V				0.1	1.0	mV/V
Voltage Noise	100Hz to 100kHz				20		$µV_{RMS}$
Hysteresis Input Voltage Range	MAX9_1/MAX982/MAX9_3			REF - 0.05		REF	V
Response Time (high-to-low transition)	T_A = +25°C, 100pF load, 1MΩ pull-up to V+		Overdrive = 10mV		12		µs
			Overdrive = 100mV		4		
Response Time (low-to-high transition) (Note 2)	T_A = +25°C, 100pF load, 1MΩ pull-up to V+				300		µs

ELECTRICAL CHARACTERISTICS: 5V OPERATION (continued)

(V+ = 5V, V- = GND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Low Voltage	MAX9_2/MAX9_3, I_{OUT} = 1.8mA for C/E temp. ranges, I_{OUT} = 1.2mA for M temp. range			V- + 0.4	V
	MAX9_1/MAX9_4, I_{OUT} = 1.8mA for C/E temp. ranges, I_{OUT} = 1.2mA for M temp. range			GND + 0.4	
Output Leakage Current	V_{OUT} = 11V			100	nA
REFERENCE (MAX9_1/MAX982/MAX9_3/MAX9_4 ONLY)					
Reference Voltage	C temp. range	1.170	1.182	1.194	V
	E temp. range	1.158		1.206	
	M temp. range	1.147		1.217	
Source Current	T_A = +25°C	15	25		µA
	C/E temp. ranges	6			
	M temp. range	4			
Sink Current	T_A = +25°C	8	15		µA
	C/E temp. ranges	4			
	M temp. range	2			
Voltage Noise	100Hz to 100kHz		100		μV_{RMS}

ELECTRICAL CHARACTERISTICS: 3V OPERATION

(V+ = 5V, V- = GND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
POWER REQUIREMENTS							
Supply Current	HYST = REF, IN+ = (IN- + 100mV)	MAX9_1	T_A = +25°C		2.4	3.0	µA
			C/E temp. ranges			3.8	
			M temp. range			4.8	
		MAX972	T_A = +25°C		2.4	3.0	
			C/E temp. ranges			3.8	
			M temp. range			4.8	
		MAX982/ MAX9_3	T_A = +25°C		3.4	4.3	
			C/E temp. ranges			5.8	
			M temp. range			7.2	
		MAX9_4	T_A = +25°C		5.2	6.2	
			C/E temp. ranges			8.0	
			M temp. range			10.5	
COMPARATOR							
Input Offset Voltage	V_{CM} = 1.5V					±10	mV
Input Leakage Current (IN-, IN+)	IN+ = IN- = 1.5V		C/E temp. ranges		±0.01	±5	nA
			M temp. range			±40	
Input Leakage Current (HYST)	MAX9_1/MAX982/MAX9_3				±0.02		nA
Input Common-Mode Voltage Range				V-		V+ - 1.3	V
Common-Mode Rejection Ratio	V- to (V+ - 1.3V)				0.2	1	mV/V
Power-Supply Rejection Ratio	V+ = 2.5V to 11V				0.1	1	mV/V

Ultra-Low-Power, Open-Drain, Single/Dual-Supply Comparators

ELECTRICAL CHARACTERISTICS: 3V OPERATION (continued)

(V+ = 5V, V- = GND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Voltage Noise	100Hz to 100kHz			20		μV_{RMS}
Hysteresis Input Voltage Range	MAX9_1/MAX982/MAX9_3		REF - 0.05		REF	V
Response Time (high-to-low transition)	T_A = +25°C, 100pF load, 1MΩ pull-up to V+	Overdrive = 10mV		12		µs
		Overdrive = 100mV		4		
Response Time (low-to-high transition) (Note 2)	T_A = +25°C, 100pF load, 1MΩ pull-up to V+			300		µs
Output Low Voltage	MAX9_2/MAX9_3, I_{OUT} = 0.8mA for C/E temp. ranges, I_{OUT} = 0.6mA for M temp. range				V- + 0.4	V
	MAX9_1/MAX9_4, I_{OUT} = 0.8mA for C/E temp. ranges, I_{OUT} = 0.6mA for M temp. range				GND + 0.4	
Output Leakage Current	V_{OUT} = 11V				100	nA
REFERENCE						
Reference Voltage	C temp. range		1.170	1.182	1.194	V
	E temp. range		1.158		1.206	
	M temp. range		1.147		1.217	
Source Current	T_A = +25°C		15	25		µA
	C/E temp. ranges		6			
	M temp. range		4			
Sink Current	T_A = +25°C		8	15		µA
	C/E temp. ranges		4			
	M temp. range		2			
Voltage Noise	100Hz to 100kHz			100		μV_{RMS}

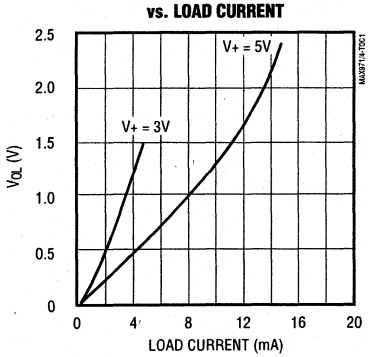
Note 1: MAX974/MAX984 comparators work below 2.5V; see *Low-Voltage* Operation section for more details.

Note 2: Low-to-high response time is the result of the 1MΩ pull-up and the 100pF capacitive load, based on three time constants. A faster response time is achieved with a smaller RC.

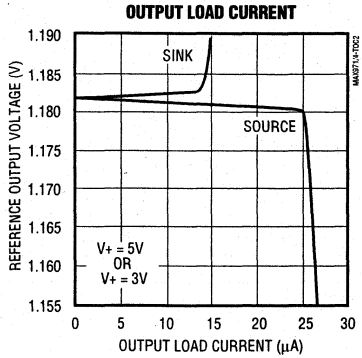
Typical Operating Characteristics

(V+ = 5V, V- = GND, T_A = +25°C, unless otherwise noted.)

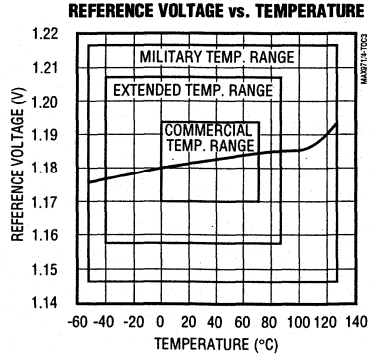
OUTPUT VOLTAGE LOW vs. LOAD CURRENT



REFERENCE OUTPUT VOLTAGE vs. OUTPUT LOAD CURRENT



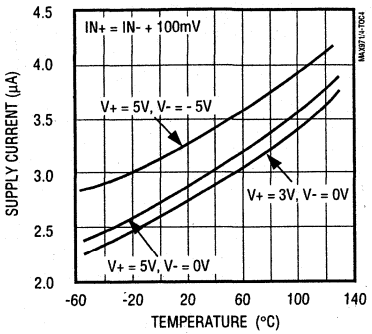
MAX971/MAX973/MAX974 REFERENCE VOLTAGE vs. TEMPERATURE



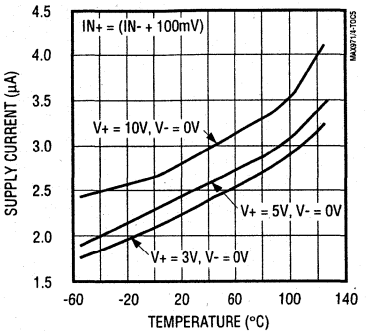
Typical Operating Characteristics (continued)

(V+ = 5V, V- = GND, T_A = +25°C, unless otherwise noted.)

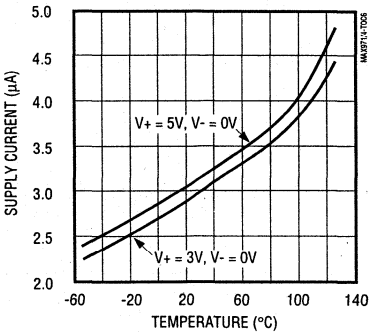
MAX9_1 SUPPLY CURRENT vs. TEMPERATURE



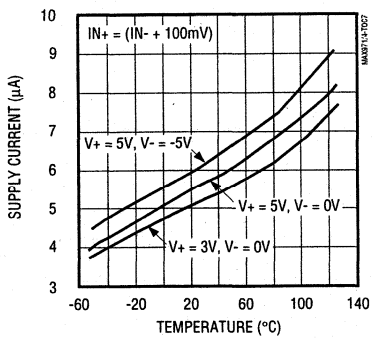
MAX972 SUPPLY CURRENT vs. TEMPERATURE



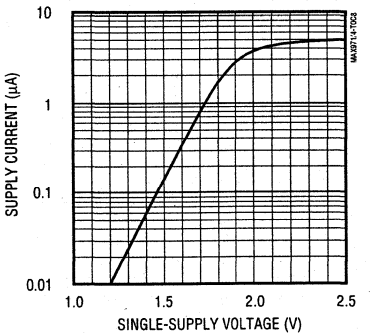
MAX982/MAX9_3 SUPPLY CURRENT vs. TEMPERATURE



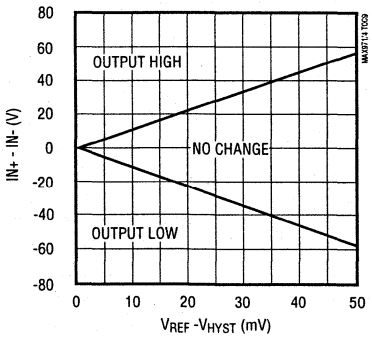
MAX9_4 SUPPLY CURRENT vs. TEMPERATURE



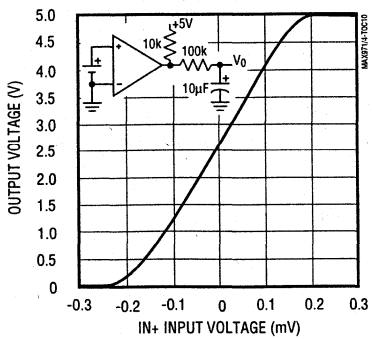
MAX9_4 SUPPLY CURRENT vs. LOW SUPPLY VOLTAGES



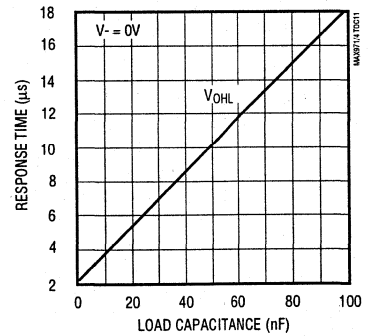
MAX9_1/MAX982/MAX9_3 HYSTERESIS CONTROL



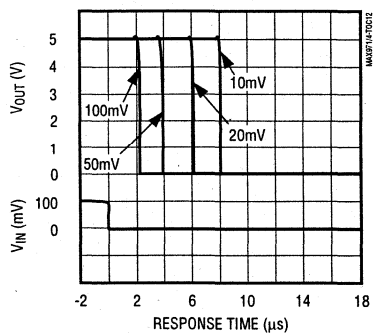
MAX9_1/MAX972/MAX9_4 TRANSFER FUNCTION



RESPONSE TIME vs. LOAD CAPACITANCE



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES (V_{OHL})

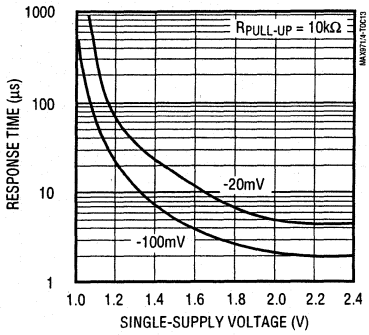


Ultra-Low-Power, Open-Drain, Single/Dual-Supply Comparators

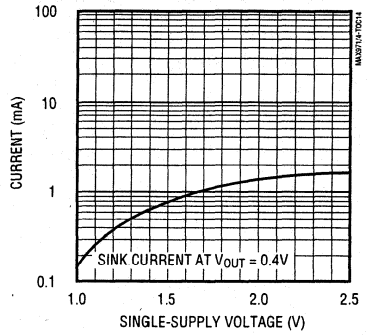
Typical Operating Characteristics (continued)

(V+ = 5V, V- = GND, T_A = +25°C, unless otherwise noted.)

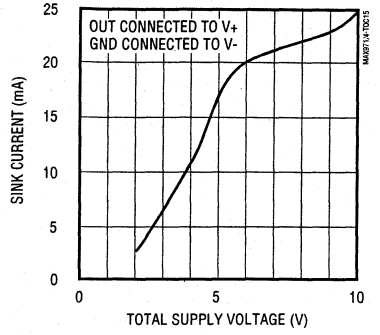
RESPONSE TIME AT LOW SUPPLY VOLTAGES (V_{OHL})



MAX924 RESPONSE TIME AT LOW SUPPLY VOLTAGES



SHORT-CIRCUIT SINK CURRENT vs. SUPPLY VOLTAGE



Pin Descriptions

PIN				NAME	FUNCTION
MAX971 MAX981	MAX972	MAX982	MAX973 MAX983		
1	—	—	—	GND	Ground. Connect to V- for single-supply operation. Output transistor pulls to GND.
—	1	1	1	OUTA	Comparator A Open-Drain Output. Sinks current to V-.
2	2	2	2	V-	Negative Supply. Connect to ground for single-supply operation (MAX9_1).
3	—	—	—	IN+	Noninverting Comparator Input
—	3	3	3	INA+	Noninverting Input of Comparator A
4	—	—	—	IN-	Inverting Comparator Input
—	4	—	—	INA-	Inverting Input of Comparator A
—	5	—	4	INB-	Inverting Input of Comparator B
—	6	4	—	INB+	Noninverting Input of Comparator B
5	—	5	5	HYST	Hysteresis Input. Connect to REF if not used. Input voltage range is from V_{REF} to V_{REF} - 50mV.
6	—	6	6	REF	Reference Output. 1.182V with respect to V-.
7	7	7	7	V+	Positive Supply
8	—	—	—	OUT	Comparator Output. Sinks current to GND.
—	8	8	8	OUTB	Comparator B Open-Drain Output. Sinks current to V-.

Pin Descriptions (continued)

PIN MAX974 MAX984	NAME	FUNCTION
1	OUTB	Comparator B Open-Drain Output. Sinks current to GND.
2	OUTA	Comparator A Open-Drain Output. Sinks current to GND.
3	V+	Positive Supply
4	INA-	Inverting Input of Comparator A
5	INA+	Noninverting Input of Comparator A
6	INB-	Inverting Input of Comparator B
7	INB+	Noninverting Input of Comparator B
8	REF	Reference Output. 1.182V with respect to V-.
9	V-	Negative Supply. Connect to ground for single-supply operation.
10	INC-	Inverting Input of Comparator C
11	INC+	Noninverting Input of Comparator C
12	IND-	Inverting Input of Comparator D
13	IND+	Noninverting Input of Comparator D
14	GND	Ground. Connect to V- for single-supply operation.
15	OUTD	Comparator D Open-Drain Output. Sinks current to GND.
16	OUTC	Comparator C Open-Drain Output. Sinks current to GND.

Ultra-Low-Power, Open-Drain, Single/Dual-Supply Comparators

Detailed Description

The MAX971–MAX974 and MAX981–MAX984 comprise various combinations of a micropower 1.182V reference and micropower comparators. The *Typical Operating Circuit* shows the MAX971/MAX981 configuration, and Figures 1a–1d show the MAX9_2–MAX9_4 configurations.

Internal hysteresis in the MAX9_1, MAX982, and MAX9_3 provides the easiest method for implementing hysteresis. It also produces faster hysteresis action and consumes much less current than circuits using external positive feedback.

Power-Supply and Input Signal Ranges

This family of devices operates from a single +2.5V to +11V power supply. The MAX9_1 and MAX9_4 have a separate ground for the output driver, allowing operation with dual supplies ranging from ±1.25V to ±5.5V. Connect V- to GND when operating the MAX9_1 or MAX9_4 from a single supply. The maximum total supply voltage in this case is still 11V.

For proper comparator operation, the input signal can range from the negative supply (V-) to within one volt of the positive supply (V+ - 1V). The guaranteed common-mode input voltage range extends from V- to (V+ - 1.3V). The inputs can be taken above and below the supply rails by up to 300mV without damage.

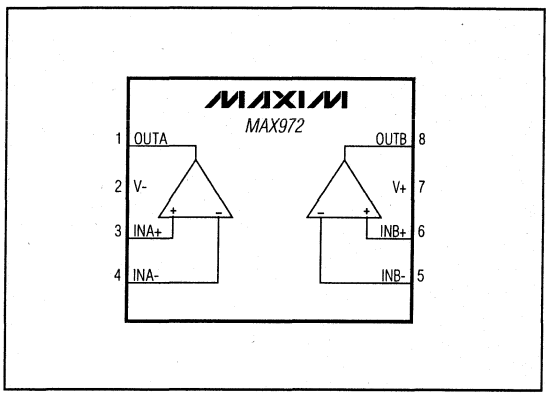


Figure 1a. MAX972 Functional Diagram

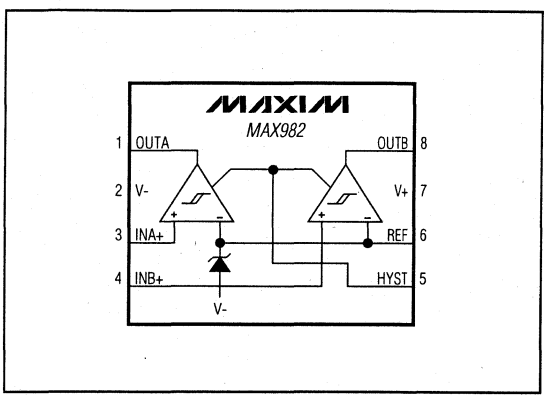


Figure 1b. MAX982 Functional Diagram

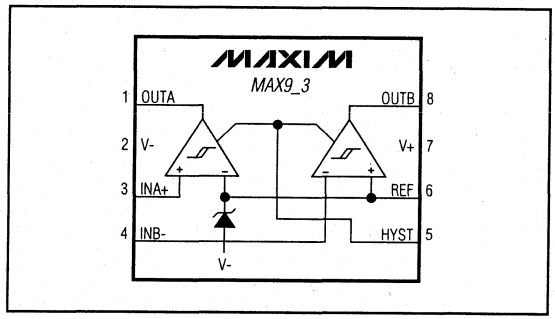


Figure 1c. MAX973/MAX983 Functional Diagram (Window Comparator)

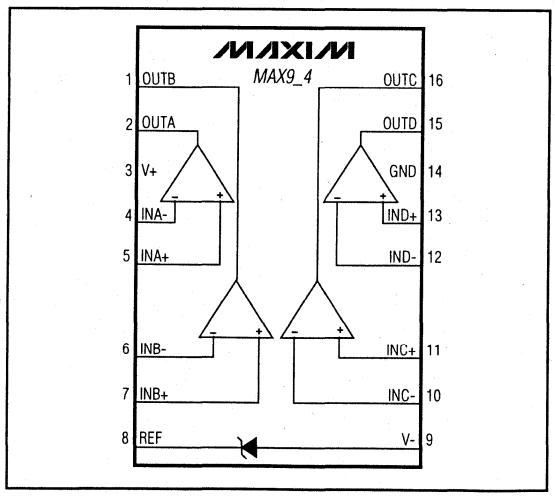


Figure 1d. MAX974/MAX984 Functional Diagram

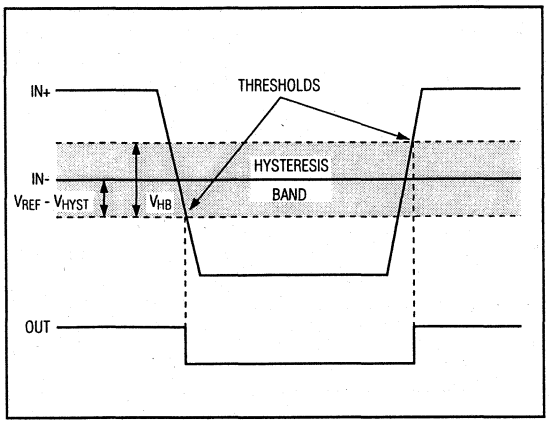


Figure 2. Threshold Hysteresis Band

Low-Voltage Operation: V+ = 1V (MAX9_4 Only)

The guaranteed minimum operating voltage is 2.5V (or ±1.25V). As the total supply voltage falls below 2.5V, performance degrades and the supply current falls. The reference will not function below about 2.2V, although the comparators will continue to operate with a total supply voltage as low as 1V. While the MAX9_4 has comparators that may be used at supply voltages below 2V, the MAX9_1/MAX9_2/MAX9_3 may not be used with supply voltages below 2.5V.

At low supply voltages, the comparators' output sink capability is reduced and the propagation delay increases (see *Typical Operating Characteristics*). The useful input voltage range extends from the negative supply to a little under 1V below the positive supply, which is slightly closer to the positive rail than when the device operates from higher supply voltages. Test your prototype over the full temperature and supply-voltage range if you anticipate operation below 2.5V.

Comparator Output

With 100mV of overdrive, propagation delay is typically 3µs. The *Typical Operating Characteristics* show the propagation delay for various overdrive levels. The open-drain outputs are intended for wire-ORed and level-shifting applications. The maximum output voltage is 11V above V-, and may be applied even when no supply voltage is present (V+ = V-).

The MAX9_1 and MAX9_4 outputs sink current to GND, making these devices ideal for bipolar to single-ended conversion and level-shifting applications.

The negative supply does not affect the output sink current. The positive supply provides gate drive for the output N-channel MOSFET and heavily influences the output current capability, especially at low supply voltages (see *Typical Operating Characteristics* section).

The MAX9_2 and MAX9_3 have no GND pin, and their outputs sink current to V-.

Voltage Reference

The internal bandgap voltage reference has an output of 1.182V above V-. Note that the REF voltage is referenced to V-, not to GND. Its accuracy is ±1% (MAX971/MAX973/MAX974) or ±2% (MAX981–MAX984) in the 0°C to +70°C range. The REF output is typically capable of sourcing 25µA and sinking 15µA. Do not bypass the REF output.

Noise Considerations

Although the comparators have a very high gain, useful gain is limited by noise. This is shown in the Transfer Function graph (see *Typical Operating Characteristics*). As the input voltage approaches the comparator's offset, the output begins to bounce back and forth; this peaks when $V_{IN} = V_{OS}$. (The lowpass filter shown on the graph averages out the bouncing, making the transfer function easy to observe.) Consequently, the comparator has an effective wideband peak-to-peak noise of around 300µV. The voltage reference has peak-to-peak noise approaching 1mV. Thus, when a comparator is used with the reference, the combined peak-to-peak noise is about 1mV. This, of course, is much higher than the RMS noise of the individual components. Take care in your layout to avoid capacitive coupling from any output to the reference pin. Crosstalk can significantly increase the actual noise of the reference.

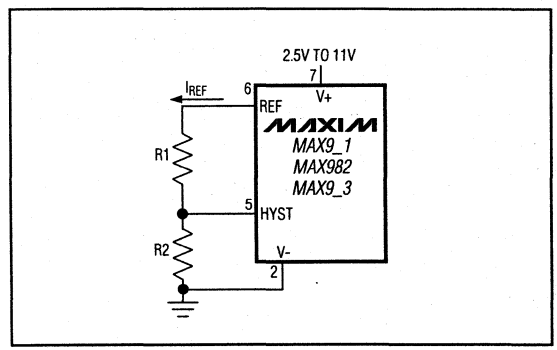


Figure 3. Programming the HYST Pin

Ultra-Low-Power, Open-Drain, Single/Dual-Supply Comparators

Applications Information

Hysteresis

Hysteresis increases the comparators' noise margin by increasing the upper threshold and decreasing the lower threshold (Figure 2).

Hysteresis (MAX9_1/MAX982/MAX9_3)

To add hysteresis to the MAX9_1, MAX982, or MAX9_3, connect resistor R1 between REF and HYST, and connect resistor R2 between HYST and V- (Figure 3). If no hysteresis is required, connect HYST to REF. When hysteresis is added, the upper threshold increases by the same amount that the lower threshold decreases. The hysteresis band (the difference between the upper and lower thresholds, V_{HB}) is approximately equal to twice the voltage between REF and HYST. The HYST input can be adjusted to a maximum voltage of REF and to a minimum voltage of (REF - 50mV). The maximum difference between REF and HYST (50mV) will therefore produce a 100mV max hysteresis band. Use the following equations to determine R1 and R2:

$$R1 = \frac{V_{HB}}{(2 \times I_{REF})}$$

$$R2 = \frac{\left(1.182 - \frac{V_{HB}}{2}\right)}{I_{REF}}$$

where I_{REF} (the current sourced by the reference) should not exceed the REF source capability, and should be significantly larger than the HYST input current. I_{REF} values between 0.1µA and 4µA are usually appropriate. If 2.4MΩ is chosen for R2 (I_{REF} = 0.5µA), the equation for R1 and V_{HB} can be approximated as:

$$R1\ (k\Omega) = V_{HB}(mV)$$

When hysteresis is obtained in this manner for the MAX982/MAX9_3, the same hysteresis applies to both comparators.

Hysteresis (MAX972/MAX9_4)

Hysteresis can be implemented with any comparator using positive feedback, as shown in Figure 4. This approach generally draws more current than circuits using the HYST pin on the MAX9_1/MAX982/MAX9_3, and the high feedback impedance slows hysteresis. In addition, because the output does not source current, any increase in the upper threshold is dependent on the load or pull-up resistor on the output.

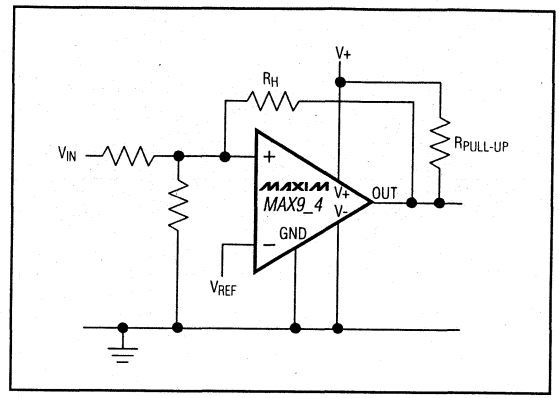


Figure 4. External Hysteresis

Board Layout and Bypassing

Power-supply bypass capacitors are not needed if the supply impedance is low, but 100nF bypass capacitors should be used when the supply impedance is high or when the supply leads are long. Minimize signal lead lengths to reduce stray capacitance between the input and output that might cause instability. Do not bypass the reference output.

Window Detector

The MAX9_3 is ideal for making window detectors (undervoltage/overvoltage detectors). The schematic is shown in Figure 5, with component values selected for a 4.5V undervoltage threshold and a 5.5V overvoltage threshold. Choose different thresholds by changing the values of R1, R2, and R3. To prevent chatter at the output when the supply voltage is close to a threshold, hysteresis has been added using R4 and R5. Taken alone, OUTA would provide an active-low undervoltage indication, and OUTB would give an active-low overvoltage indication. Wired-ORing the two outputs provides an active-high, power-good signal.

The design procedure is as follows:

1) Choose the required hysteresis level and calculate values for R4 and R5 according to the formulas in the *Hysteresis (MAX9_1/MAX982/MAX9_3)* section. In this example, ±5mV of hysteresis has been added *at the comparator input* ($V_H = V_{HB} / 2$). This means that the hysteresis apparent at V_{IN} will be larger because of the input resistor divider.

2) Select R1. The leakage current into INB- is normally under 1nA, so the current through R1 should exceed 100nA for the thresholds to be accurate. R1 values up to about 10MΩ can be used, but values in the 100kΩ to 1MΩ range are usually easier to deal with. In this example, choose R1 = 294kΩ.

3) Calculate R2 + R3. The overvoltage threshold should be 5.5V when V_{IN} is rising. The design equation is as follows:

$$R2 + R3 = R1 \times \left(\frac{V_{OTH}}{V_{REF} + V_H} - 1 \right)$$

$$= 294k \times \left(\frac{5.5}{(1.182 + 0.005)} - 1 \right)$$

$$= 1.068M\Omega$$

4) Calculate R2. The undervoltage threshold should be 4.5V when V_{IN} is falling. The design equation is as follows:

$$R2 = (R1 + R2 + R3) \times \frac{(V_{REF} - V_H)}{V_{UTH}} - R1$$

$$= (294k + 1.068M) \times \frac{(1.182 - 0.005)}{4.5} - 294k$$

$$= 62.2k\Omega$$

Choose R2 = 61.9kΩ (1% standard value).

5) Calculate R3:

$$R3 = (R2 + R3) - R2$$

$$= 1.068M - 61.9k$$

$$= 1.006M\Omega$$

Choose R3 = 1MΩ (1% standard value)

6) Verify the resistor values. The equations are as follows, evaluated for the above example:

Overvoltage Threshold:

$$V_{OTH} = (V_{REF} + V_H) \times \frac{(R1 + R2 + R3)}{R1}$$

$$= 5.474V$$

Undervoltage Threshold:

$$V_{UTH} = (V_{REF} - V_H) \times \frac{(R1 + R2 + R3)}{(R1 + R2)}$$

$$= 4.484V$$

where the hysteresis voltage $V_H = V_{REF} \times \frac{R5}{R4}$.

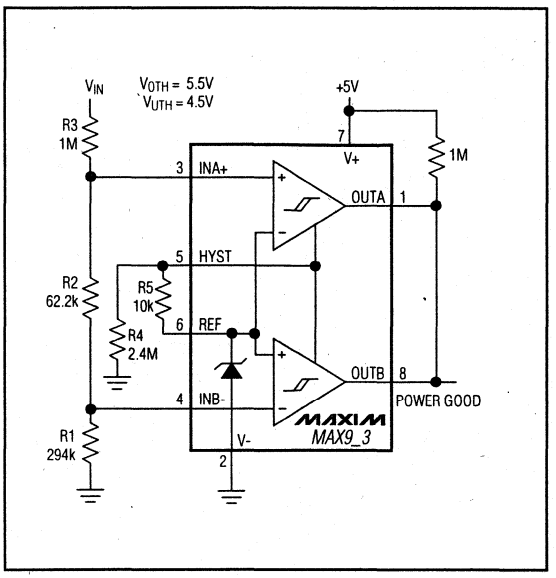


Figure 5. Window Detector

Battery Switchover Circuit

The switchover from line-powered DC to a backup battery is often accomplished with diodes. But this simple method is sometimes unacceptable, due to the voltage drop and associated power loss across the diode in series with the battery. Figure 6's circuit replaces the diode with a P-channel MOSFET controlled by one of the MAX9_3 comparator outputs.

When the DC wall adapter drops below 4V (determined by R1 and R2), OUTA goes low, turning on Q1. Comparator B is used to measure the battery voltage, and gives a "low-battery" indication when the battery drops below 3.6V.

Level Shifter

Figure 7 shows a circuit to shift from bipolar ±5V inputs to single-ended +5V outputs. The 10kΩ resistors protect the comparator inputs, and do not materially affect the circuit's operation.

Ultra-Low-Power, Open-Drain, Single/Dual-Supply Comparators

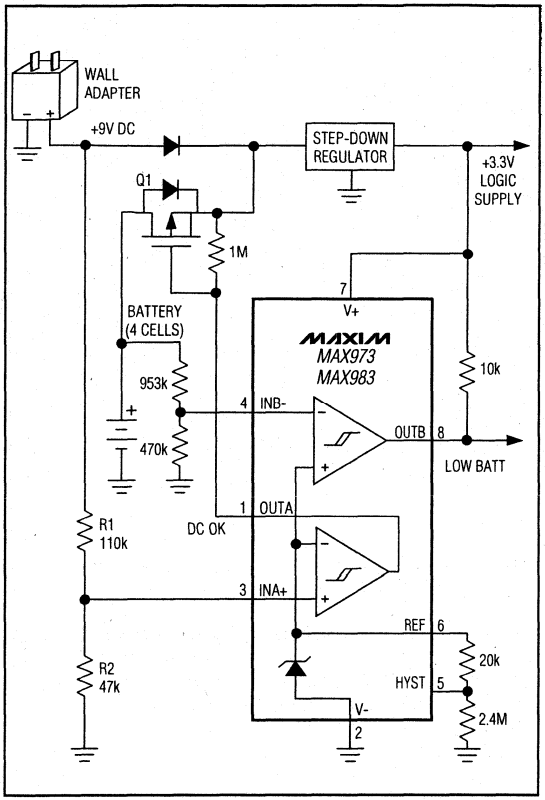


Figure 6. Battery Switchover Circuit

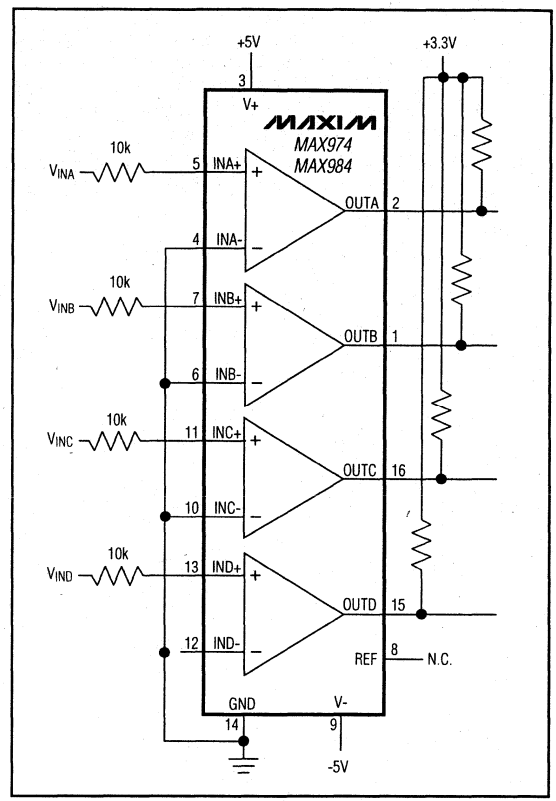
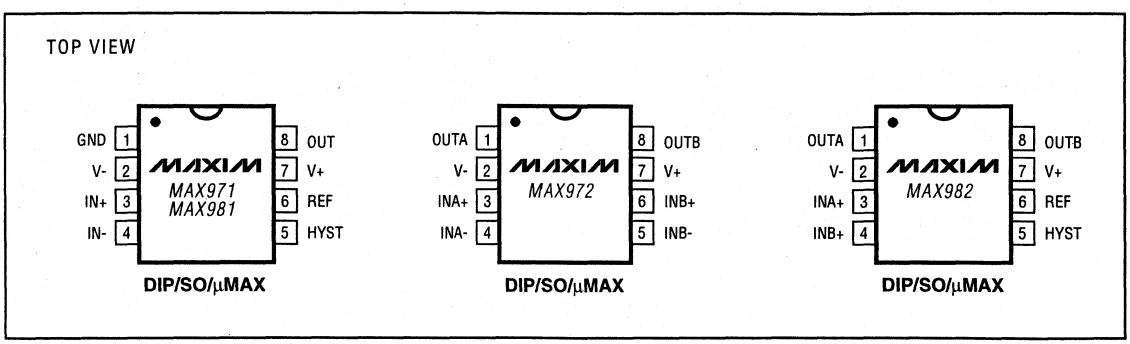


Figure 7. Level Shifter: ±5V Input to Single-Ended +3.3V Output

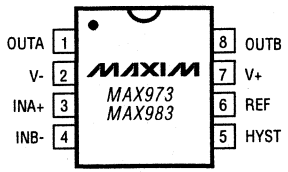
Pin Configurations



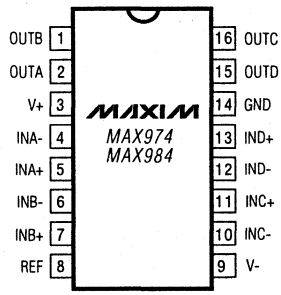
Ultra-Low-Power, Open-Drain, Single/Dual-Supply Comparators

Pin Configurations (continued)

TOP VIEW



DIP/SO/µMAX



DIP/Narrow SO

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX971EPA	-40°C to +85°C	8 Plastic DIP
MAX971ESA	-40°C to +85°C	8 SO
MAX971MJA	-55°C to +125°C	8 CERDIP**
MAX972CPA	0°C to +70°C	8 Plastic DIP
MAX972CSA	0°C to +70°C	8 SO
MAX972CUA	0°C to +70°C	8 µMAX
MAX972C/D	0°C to +70°C	Dice*
MAX972EPA	-40°C to +85°C	8 Plastic DIP
MAX972ESA	-40°C to +85°C	8 SO
MAX972MJA	-55°C to +125°C	8 CERDIP**
MAX973CPA	0°C to +70°C	8 Plastic DIP
MAX973CSA	0°C to +70°C	8 SO
MAX973CUA	0°C to +70°C	8 µMAX
MAX973C/D	0°C to +70°C	Dice*
MAX973EPA	-40°C to +85°C	8 Plastic DIP
MAX973ESA	-40°C to +85°C	8 SO
MAX973MJA	-55°C to +125°C	8 CERDIP**
MAX974CPE	0°C to +70°C	16 Plastic DIP
MAX974CSE	0°C to +70°C	16 Narrow SO
MAX974C/D	0°C to +70°C	Dice*
MAX974EPE	-40°C to +85°C	16 Plastic DIP
MAX974ESE	-40°C to +85°C	16 Narrow SO
MAX974MJE	-55°C to +125°C	16 CERDIP**

PART	TEMP. RANGE	PIN-PACKAGE
MAX981CPA	0°C to +70°C	8 Plastic DIP
MAX981CSA	0°C to +70°C	8 SO
MAX981CUA	0°C to +70°C	8 µMAX
MAX981EPA	-40°C to +85°C	8 Plastic DIP
MAX981ESA	-40°C to +85°C	8 SO
MAX982CPA	0°C to +70°C	8 Plastic DIP
MAX982CSA	0°C to +70°C	8 SO
MAX982CUA	0°C to +70°C	8 µMAX
MAX982EPA	-40°C to +85°C	8 Plastic DIP
MAX982ESA	-40°C to +85°C	8 SO
MAX983CPA	0°C to +70°C	8 Plastic DIP
MAX983CSA	0°C to +70°C	8 SO
MAX983CUA	0°C to +70°C	8 µMAX
MAX983EPA	-40°C to +85°C	8 Plastic DIP
MAX983ESA	-40°C to +85°C	8 SO
MAX984CPE	0°C to +70°C	16 Plastic DIP
MAX984CSE	0°C to +70°C	16 Narrow SO
MAX984EPE	-40°C to +85°C	16 Plastic DIP
MAX984ESE	-40°C to +85°C	16 Narrow SO

* *Dice are tested at T_A = +25°C, DC parameters only.*
** *Contact factory for availability and processing to MIL-STD-883.*

Ultra-Low-Power, Open-Drain, Single/Dual-Supply Comparators

Chip Information

MAX971/MAX972/MAX973

TRANSISTOR COUNT: 164
SUBSTRATE CONNECTED TO V+

MAX974

TRANSISTOR COUNT: 267
SUBSTRATE CONNECTED TO V+

19-1141; Rev 0; 9/96

MAXIM

Single/Dual, +3V/+5V Dual-Speed Comparators with Auto-Standby

General Description

The MAX975/MAX977 single/dual comparators feature three different operating modes, and are optimized for +3V and +5V single-supply applications. The operating modes are as follows: high speed, high speed with auto-standby, and low power. Propagation delay is 28ns in high-speed mode, while supply current is only 300µA. Supply current is reduced to 3µA in low-power mode.

The auto-standby feature allows the comparator to automatically change from low-power mode to high-speed mode upon receipt of an input signal. In the absence of an input signal, the comparator reverts back to low-power mode after an adjustable timeout period. The timeout period for the MAX975 to enter standby is set by a single capacitor. The dual MAX977 features independently adjustable timeout periods for each comparator using separate capacitors.

The MAX975/MAX977's inputs have a common-mode voltage range of -0.2V to (V_{CC} - 1.2V). The differential input voltage range extends rail to rail. The outputs are capable of rail-to-rail operation without external pull-up circuitry, making these devices ideal for interface with CMOS/TTL logic. All inputs and outputs can tolerate a continuous short-circuit fault condition to either rail. The comparator's internal hysteresis in high-speed mode ensures clean output switching, even with slow-moving input signals.

The single MAX975 is available in 8-pin SO and 8-pin µMAX packages, while the dual MAX977 is available in 14-pin SO and 16-pin QSOP packages.

Applications

Battery-Powered Systems
RF ID Tags
Keyless Entry
Threshold Detectors/Discriminators
3V Systems
IR Receivers
Digital-Line Receivers

Pin Configurations appear at end of data sheet.

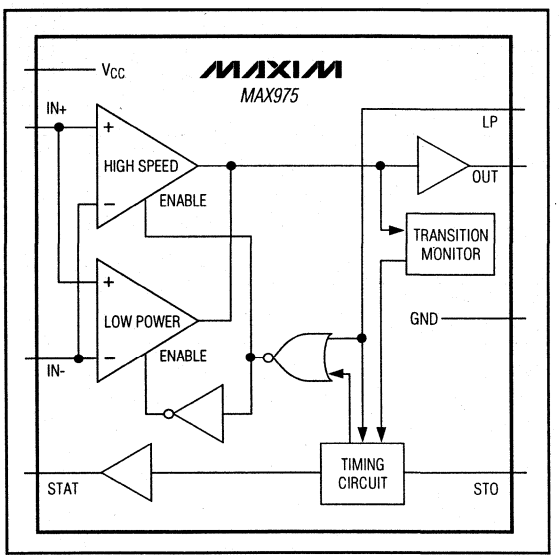
Features

- **Three Operating Modes:**
  High Speed
  High Speed with Auto-Standby
  Low Power
- **28ns Propagation Delay (high-speed mode)**
- **5µA Max Supply Current in Low-Power/ Auto-Standby Modes**
- **+3V/+5V Single-Supply Operation**
- **Rail-to-Rail Outputs**
- **Ground-Sensing Input**
- **Internal Hysteresis (high-speed mode)**
- **Adjustable Timeout Period**
- **µMAX Package (MAX975)**
  QSOP-16 Package (MAX977)

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX975ESA	-40°C to +85°C	8 SO
MAX975EUA	-40°C to +85°C	8 µMAX
MAX977ESD	-40°C to +85°C	14 SO
MAX977EEE	-40°C to +85°C	16 QSOP

Functional Diagram



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Single/Dual, +3V/+5V Dual-Speed Comparators with Auto-Standby

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) .....+6V
All Other Pins.....-0.3V to (V_{CC} + 0.3V)
Duration of Output Short Circuit to GND_ or V_{CC} .....Continuous
Continuous Power Dissipation (T_A = +70°C)
8-Pin SO (derate 5.88mW/°C above +70°C).....471mW
8-Pin µMAX (derate 4.10mW/°C above +70°C).....330mW
14-Pin SO (derate 8.33mW/°C above +70°C).....667mW
16-Pin QSOP (derate 8.33mW/°C above +70°C).....667mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.25V, specifications are for high-speed mode, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
POWER SUPPLY								
Supply-Voltage Operating Range	V_{CC}				2.7		5.25	V
Supply Current Per Comparator	I_{CC}	High-speed mode				300	500	µA
		Auto-standby/low-power modes		SO		3	5	
				µMAX/QSOP		3	6	
Power-Supply Rejection Ratio	PSRR	V_{CM} = 1V, 2.7V ≤ V_{CC} ≤ 5.25V	High-speed mode		63	90		dB
			Low-power mode			77		
COMPARATOR INPUTS								
Common-Mode Voltage Range	V_{CMR}	(Note 1)			-0.2		V_{CC} - 1.2	V
Input Offset Voltage (Note 2)	V_{OS}	V_{CM} = 1V, V_{CC} = 5V	High-speed mode, T_A = +25°C			+0.2	±2	mV
			High-speed mode, T_A = T_{MIN} to T_{MAX}				±3	
			Auto-standby/ low-power modes, T_A = T_{MIN} to T_{MAX}	SO		±1	±5	
				µMAX/QSOP		±1	±7	
Input-Referred Hysteresis	V_{HYS}	V_{CM} = 1V, V_{CC} = 5V (Note 3)		SO	0.5	2	4	mV
				µMAX/QSOP	0.3	2	4	
Input Bias Current	I_B	High-speed mode		SO		-100	-300	nA
				µMAX/QSOP		-100	-400	
		Auto-standby/low-power modes				-5		
Input Offset Current	I_{OS}					±20	±100	nA
Input Capacitance	C_{IN}					3		pF
Common-Mode Rejection Ratio	CMRR	-0.2V ≤ V_{CM} ≤ V_{CC} - 1.2V	High-speed mode	SO	66	90		dB
				µMAX/QSOP	54			
			Low-power mode			82		

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.7V to +5.25V, specifications are for high-speed mode, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL INPUTS							
LP Input Voltage High	V_{LPIH}			0.7xV_{CC}	V_{CC} / 2	0.3xV_{CC}	V
LP Input Voltage Low	V_{LPIL}				V_{CC} / 2	0.3xV_{CC}	V
LP Fall Time	t_{LP}	(Note 4)				10	µs
LP Input Current	I_{LPB}				0.01	±1	µA
STO_ Input Voltage Low	V_{CIL}				V_{CC} / 2	0.3 x V_{CC}	V
STO_ Source Current	I_{STO}	V_{CC} = 3V			0.15		µA
DIGITAL OUTPUTS							
OUT_ Output Voltage High	V_{OH}	I_{SOURCE} = 2mA, all modes		V_{CC} - 0.4	V_{CC} - 0.1		V
OUT_ Output Voltage Low	V_{OL}	I_{SINK} = 2mA, all modes			0.1	0.4	V
Propagation Delay, Low to High (Note 5)	t_{PD+}	C_{LOAD} = 10pF, V_{CC} = 5V	High-speed mode, overdrive = 5mV		28	50	ns
			Low-power mode, overdrive = 10mV		0.82	1.6	µs
Propagation Delay, High to Low (Note 5)	t_{PD-}	C_{LOAD} = 10pF, V_{CC} = 5V	High-speed mode, overdrive = 5mV		28	50	ns
			Low-power mode, overdrive = 10mV		0.48	1.6	µs
Propagation-Delay Skew (Note 5)	t_{SKEW}	C_{LOAD} = 10pF			2		ns
Propagation-Delay Matching	Δt_{PD}	MAX977 only, C_{LOAD} = 10pF			1		ns
Rise/Fall Time		C_{LOAD} = 10pF, V_{CC} = 5.0V	High-speed mode		1.6		ns
			Low-power mode		1.6		
STAT_ Output Voltage High	V_{SH}	I_{SOURCE} = 3mA, all modes		V_{CC} - 0.4			V
STAT_ Output Voltage Low	V_{SL}	I_{SINK} = 400µA, all modes				0.4	V

Note 1: Inferred by CMRR. Either input can be driven to the absolute maximum limit without false output inversion, as long as the other input is within the specified common-mode input voltage range.

Note 2: V_{OS} is defined as the mean of trip points. The trip points are the extremities of the differential input voltage required to make the comparator output change state (Figure 1).

Note 3: The difference between the upper and lower trip points is equal to the width of the input-referred hysteresis zone (Figure 1).

Note 4: Guaranteed by design. The LP pin is sensitive to noise. If fall times larger than 10µs are expected, bypass LP to ground using a 0.1µF capacitor.

Note 5: Propagation delay cannot be measured in automatic test equipment with low input overdrive values. The MAX975ESA/MAX977ESD are sample tested to 0.1% AQL, with a 200mV step and 100mV overdrive at +25°C. Correlation tests show that t_{PD} can be guaranteed with this test, since additional DC tests are performed that guarantee that all internal bias conditions are correct. Propagation delay on the µMAX and QSOP packages is guaranteed by design. For low-overdrive conditions, V_{OS} is added to the overdrive. The following equation defines propagation-delay skew: $t_{SKEW} = t_{PD+} - t_{PD-}$.

Single/Dual, +3V/+5V Dual-Speed Comparators with Auto-Standby

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.7V to +5.25V, specifications are for high-speed mode, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
AUTO-STANDBY/LOW-POWER TIMING (Note 6; Figure 2)							
Auto-Standby Timeout	t_{ASB}	(Note 7)	SO	6	10	14	ms
			µMAX/QSOP	5		16	
Auto-Standby Enable Time	t_{ASBE}	(Note 8)			3		µs
Auto-Standby Wake-Up Time	t_{ASD}	10mV overdrive (Note 9)			2	4	µs
Auto-Standby Wake-Up Input or LP Pulse Width	t_{PWD}	10mV overdrive (Note 10)		1.6			µs
Auto-Standby Comparator Disable	t_{ASCD}	(Note 11)			0.8		µs
Low-Power Enable Time	t_{LPE}	(Note 12)			3		µs
High-Speed Enable Time	t_{HSE}	(Note 13)			1.1	4	µs
Low-Power Comparator Disable	t_{LPCD}	(Note 14)			0.7		µs
Low-Power STAT_ High	t_{LPSH}	(Note 15)			20		ns

Note 6: Timing specifications are sample tested to 0.1% AQL for SO packages, and are guaranteed by design for µMAX and QSOP packages.

Note 7: Set by 1000pF external capacitor at the STO_ pin. t_{ASB} is defined as the time from last input transition to STAT_ = high. Does not include time to go into standby condition (t_{ASBE}).

Note 8: t_{ASBE} is defined as the time from when STAT_ goes high to when the supply current drops to 5µA.

Note 9: t_{ASD} is defined as the time from the last input transition to when STAT_ goes low. The comparator is in high-speed mode before STAT_ is low.

Note 10: t_{PWD} is defined as the minimum input or LP pulse width to trigger fast-mode operation from auto-standby.

Note 11: t_{ASCD} is defined as the time from the last input transition to when the supply current increases to 300µA.

Note 12: t_{LPE} is defined as the time from when LP is driven high to when the supply current drops to 5µA.

Note 13: t_{HSE} is defined as the time from when LP goes low to when STAT goes low. The comparator is in high-speed mode before STAT_ is low.

Note 14: t_{LPCD} is defined as the time from when LP goes low to when the supply current increases to 300µA.

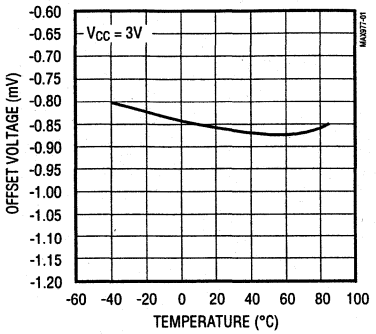
Note 15: t_{LPSH} is defined as the time from when LP goes high to when STAT_ goes high.

Single/Dual, +3V/+5V Dual-Speed Comparators with Auto-Standby

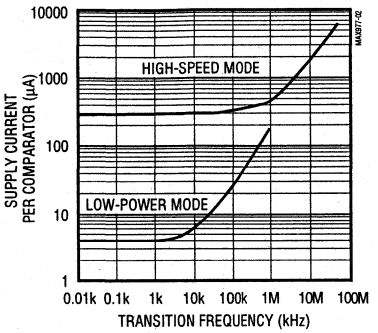
Typical Operating Characteristics

(V_{CC} = 3.0V, T_A = +25°C, unless otherwise noted.)

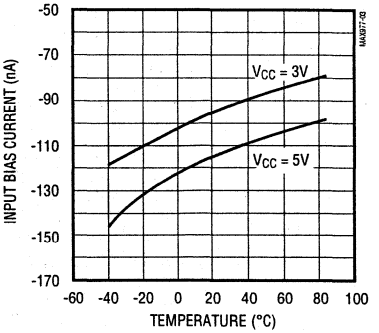
LOW-POWER OFFSET VOLTAGE vs. TEMPERATURE



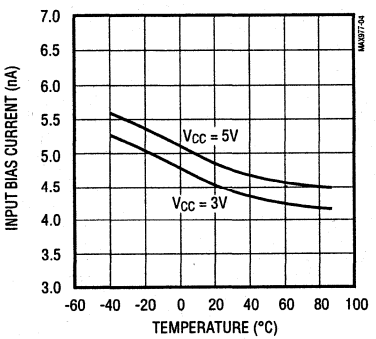
SUPPLY CURRENT PER COMPARATOR vs. OUTPUT TRANSITION FREQUENCY



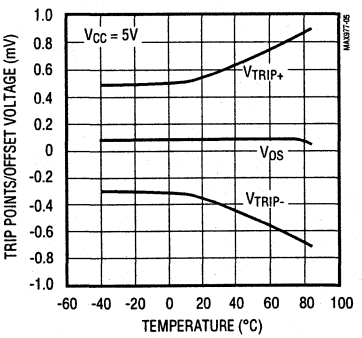
HIGH-SPEED INPUT BIAS CURRENT vs. TEMPERATURE



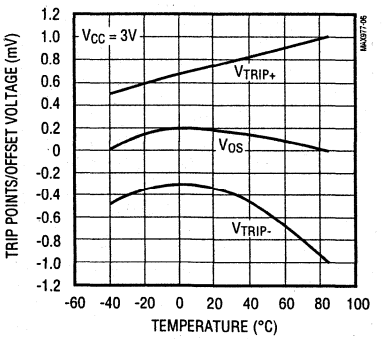
LOW-POWER INPUT BIAS CURRENT vs. TEMPERATURE



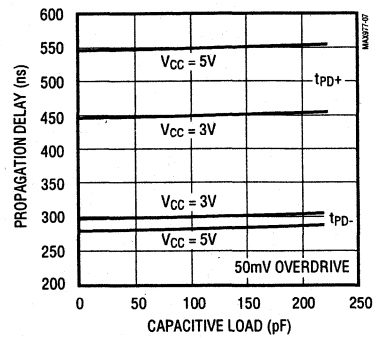
HIGH-SPEED VOLTAGE TRIP POINTS/INPUT OFFSET VOLTAGE vs. TEMPERATURE



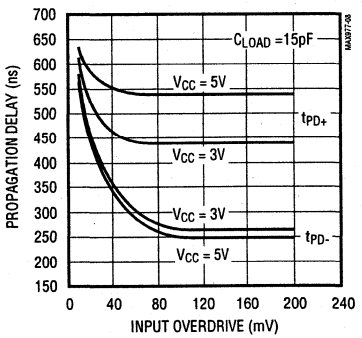
HIGH-SPEED VOLTAGE TRIP POINTS/INPUT OFFSET VOLTAGE vs. TEMPERATURE



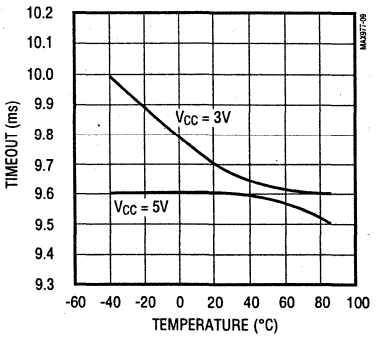
LOW-POWER PROPAGATION DELAY vs. CAPACITIVE LOAD



LOW-POWER PROPAGATION DELAY vs. INPUT OVERDRIVE



AUTO-STANDBY TIMEOUT vs. TEMPERATURE

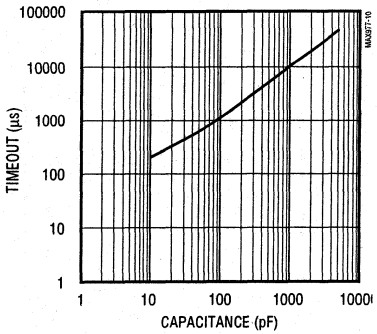


Single/Dual, +3V/+5V Dual-Speed Comparators with Auto-Standby

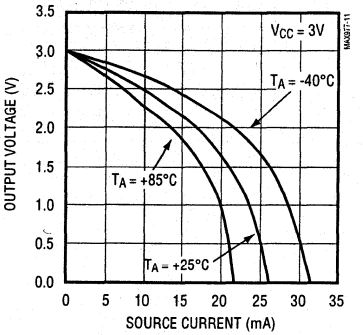
Typical Operating Characteristics (continued)

(V_{CC} = 3.0V, T_A = +25°C, unless otherwise noted.)

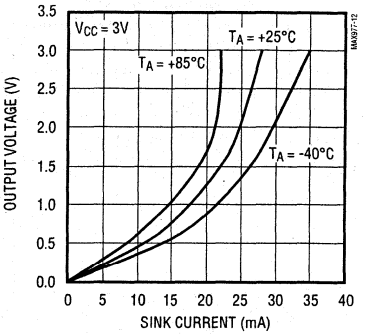
AUTO-STANDBY TIMEOUT vs. TIMEOUT CAPACITOR



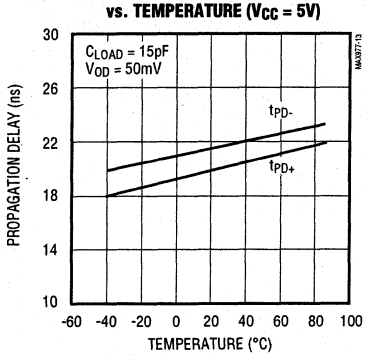
OUTPUT HIGH VOLTAGE vs. OUTPUT SOURCE CURRENT



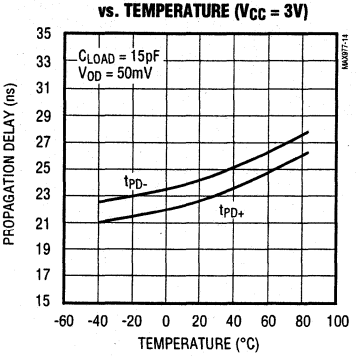
OUTPUT LOW VOLTAGE vs. OUTPUT SINK CURRENT



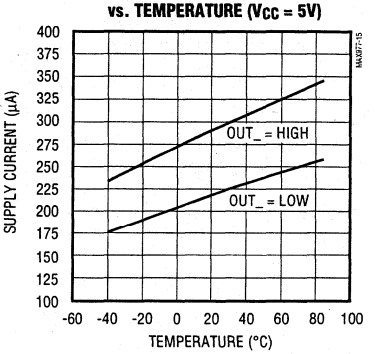
HIGH-SPEED PROPAGATION DELAY vs. TEMPERATURE (V_{CC} = 5V)



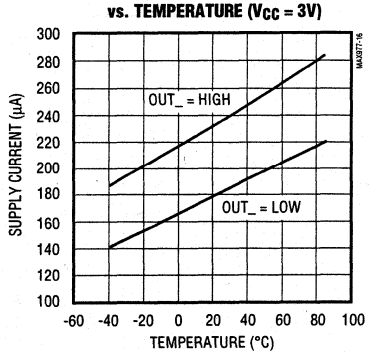
HIGH-SPEED PROPAGATION DELAY vs. TEMPERATURE (V_{CC} = 3V)



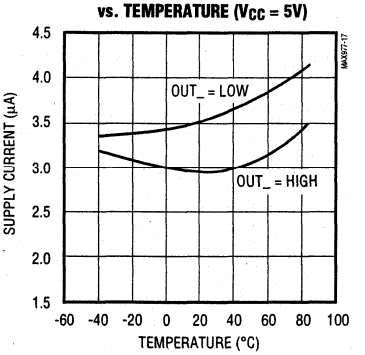
HIGH-SPEED SUPPLY CURRENT PER COMPARATOR vs. TEMPERATURE (V_{CC} = 5V)



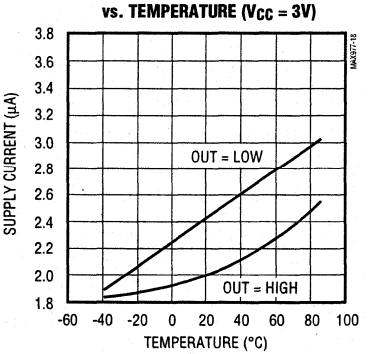
HIGH-SPEED SUPPLY CURRENT PER COMPARATOR vs. TEMPERATURE (V_{CC} = 3V)



STANDBY/LOW-POWER SUPPLY CURRENT PER COMPARATOR vs. TEMPERATURE (V_{CC} = 5V)



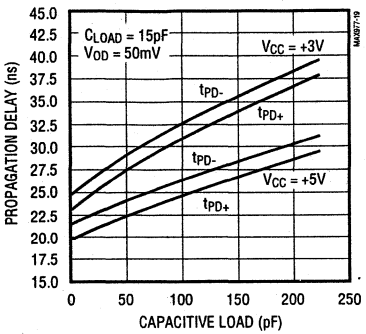
STANDBY/LOW POWER-SUPPLY CURRENT PER COMPARATOR vs. TEMPERATURE (V_{CC} = 3V)



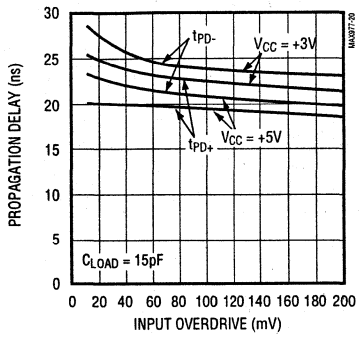
Typical Operating Characteristics (continued)

(V_{CC} = 3.0V, T_A = +25°C, unless otherwise noted.)

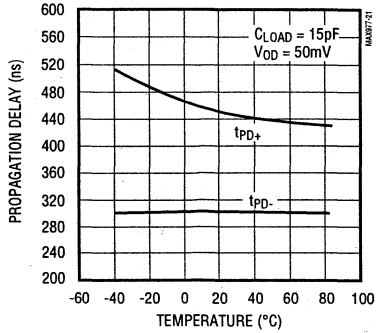
HIGH-SPEED PROPAGATION DELAY vs. CAPACITIVE LOAD



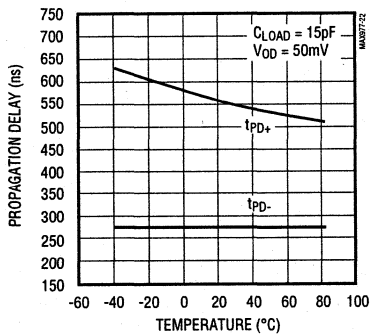
HIGH-SPEED PROPAGATION DELAY vs. INPUT OVERDRIVE



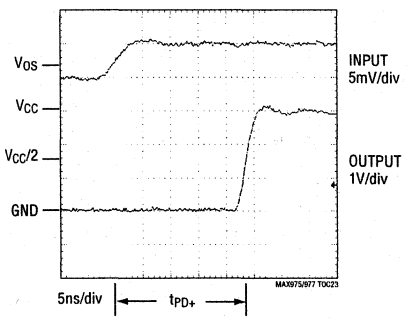
LOW-POWER PROPAGATION DELAY vs. TEMPERATURE (V_{CC} = 3V)



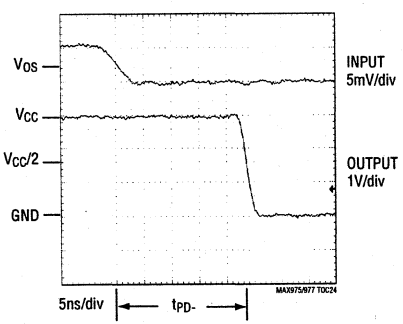
LOW-POWER PROPAGATION DELAY vs. TEMPERATURE (V_{CC} = 5V)



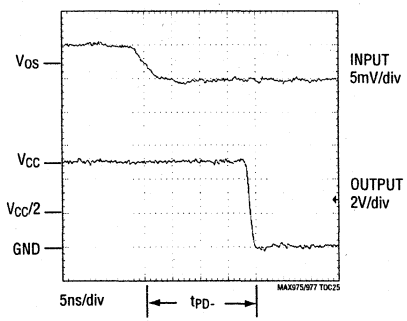
PROPAGATION DELAY t_{PD+} HIGH-SPEED MODE (V_{CC} = +3V)



PROPAGATION DELAY t_{PD-} HIGH-SPEED MODE (V_{CC} = +3V)



PROPAGATION DELAY t_{PD-} HIGH-SPEED MODE (V_{CC} = +5V)

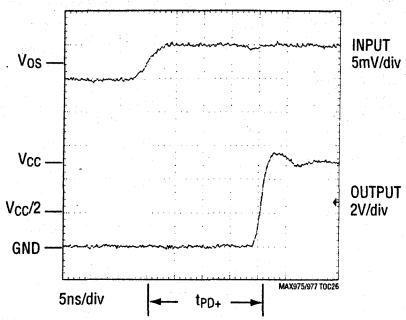


Single/Dual, +3V/+5V Dual-Speed Comparators with Auto-Standby

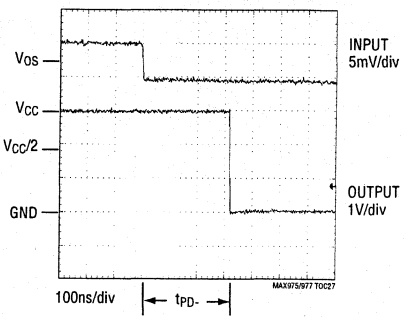
Typical Operating Characteristics (continued)

(V_{CC} = 3.0V, T_A = +25°C, unless otherwise noted.)

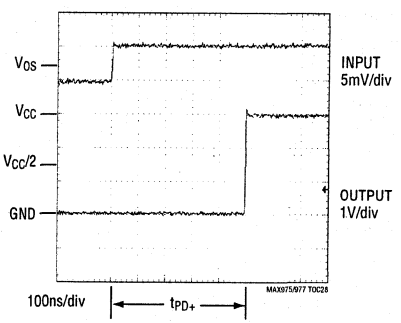
PROPAGATION DELAY t_{PD+} HIGH-SPEED MODE (V_{CC} = +5V)



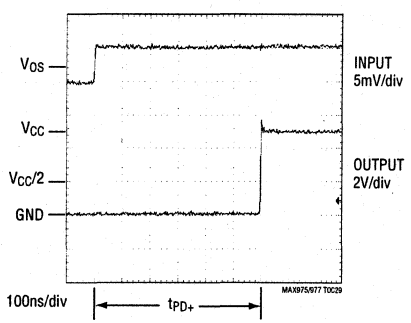
PROPAGATION DELAY t_{PD-} LOW-POWER MODE (V_{CC} = +3V)



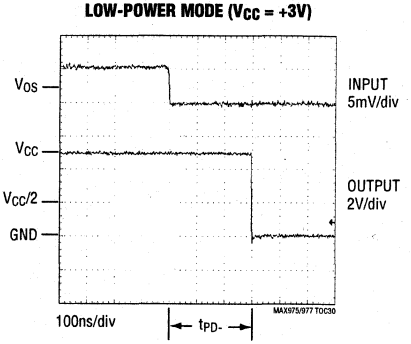
PROPAGATION DELAY t_{PD+} LOW-POWER MODE (V_{CC} = +3V)



PROPAGATION DELAY t_{PD+} LOW-POWER MODE (V_{CC} = +5V)



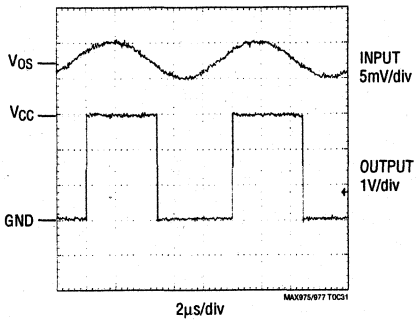
PROPAGATION DELAY t_{PD-} LOW-POWER MODE (V_{CC} = +3V)



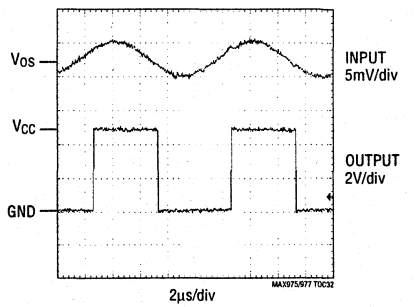
Typical Operating Characteristics (continued)

(V_{CC} = 3.0V, T_A = +25°C, unless otherwise noted.)

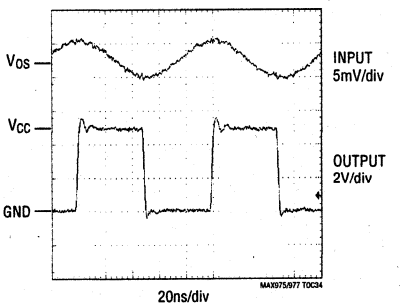
100kHz RESPONSE LOW-POWER MODE (V_{CC} = +3V)



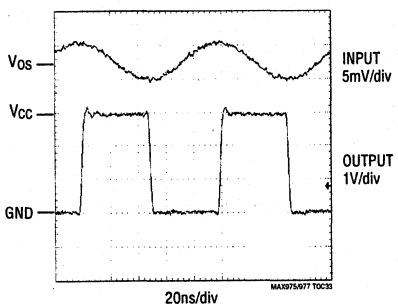
100kHz RESPONSE LOW-POWER MODE (V_{CC} = +5V)



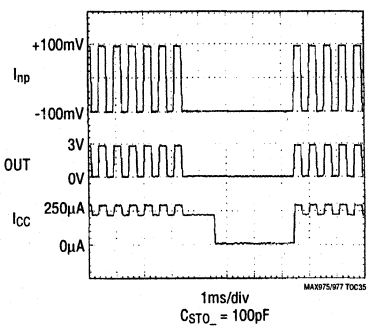
10MHz RESPONSE HIGH-SPEED MODE (V_{CC} = +5V)



10MHz RESPONSE HIGH-SPEED MODE (V_{CC} = +3V)



MAX975 AUTO-STANDBY OPERATION



Single/Dual, +3V/+5V Dual-Speed Comparators with Auto-Standby

Pin Descriptions

MAX975

PIN	NAME	FUNCTION
1	V_{CC}	Positive Supply Voltage, +2.7V to +5.25V
2	IN+	Noninverting Comparator Input
3	IN-	Inverting Comparator Input
4	STAT	Mode Status Pin. Indicates the operating mode. STAT is high for auto-standby mode or low-power mode, and during the transition to high-speed mode. STAT = low indicates that the comparator is in high-speed mode. STAT can source 3mA to power additional circuitry.
5	STO	Set Timeout Input. Connect a capacitor from STO to GND to program the time the comparator may remain idle before entering standby mode. Connect STO to GND to disable the auto-standby feature. Calculate timeout with the following relationship: tASB = 10 x C µs, where C is in pF.
6	GND	Ground
7	OUT	Comparator Output
8	LP	Low Power Mode Input. Drive LP high for low-power mode. Drive LP low for high-speed mode (STO = GND) or for high-speed mode with auto-standby. Connect to GND if low-power mode will not be used. Connect to V_{CC} if high-speed mode will not be used.

MAX977

SO	QSOP	NAME	FUNCTION
1, 8	1, 9	STOA, STOB	Set Idle Timeout Input A/B. Connect a capacitor from STOA/STOB to GND to program the time in which comparator A/B may remain idle before entering standby mode. Connect STOA/STOB to GND to disable the auto-standby feature for comparator A/B. Calculate timeout with the following relationship: t_{ASB} = 10 x C µs, where C is in pF.
2, 9	2, 10	GNDA, GNDB	Ground for Comparator A/B
3, 10	3, 11	OUTA, OUTB	Output for Comparator A/B
4	4, 5	V_{CC}	Positive Supply Voltage, +2.7V to +5.25V. For QSOP, connect pin 4 to pin 5.
5, 12	6, 14	INB+, INA+	Noninverting Input for Comparator B/A
6, 13	7, 15	INB-, INA-	Inverting Input for Comparator B/A
7, 14	8, 16	STATB, STATA	Mode Status Pin B/A. Indicates the operating mode of comparator B/A. STATB/STATA is high for auto-standby mode or for low-power mode, and during the transition to high-speed mode. STATB/STATA = low indicates that comparator B/A is in high-speed mode. STATB/STATA can source 3mA to power additional circuitry.
—	12	N.C.	No connection. Not internally connected.
11	13	LP	Low Power Mode Input for both comparators. Drive LP high for low-power mode. Drive LP low for high-speed mode (STO_ = GND) or for high-speed mode with auto-standby. Connect to GND if low-power mode will not be used. Connect to V_{CC} if high-speed mode will not be used.

Table 1. Programming

INPUTS			MODE	STAT OUTPUT
LP	STO_	IDLE TIME		
L	$t_{ASB} = C_{STO} \times 10\mu s/pF$	$<t_{ASB}$	High speed (Auto-standby enabled)	L
L	$t_{ASB} = C_{STO} \times 10\mu s/pF$	$\geq t_{ASB}$	Auto-standby	H
↓ (falling edge)	L	X	High speed (Auto-standby mode disabled)	L
H	X	X	Low power	H

Detailed Description

The MAX975/MAX977 single/dual comparators have three operating modes, and use a +2.7V to +5.25V single supply. The operating modes are as follows: high speed, high speed with auto-standby, and low power. Propagation delay is typically 28ns in high-speed mode, while typical supply current is 300µA. In low-power mode, propagation delay is typically 480ns and power consumption is only 3µA. The auto-standby feature switches into low-power standby for each comparator with unchanging outputs in high-speed mode. The timeout period, or the time that OUT_ must be idle (unchanged state) for the MAX975/MAX977 to enter auto-standby, is adjustable by means of an external capacitor. All inputs and outputs can tolerate a continuous short-circuit fault condition to either rail. Internal hysteresis in high-speed mode ensures clean output switching, even with slow-moving input signals.

The MAX975 functional diagram shows two paralleled comparators, a timing circuit, a transition detector, and logic gates. The upper comparator is high speed, while the lower comparator is a slower low-power comparator. The dual MAX977 features independent timeout adjustment. The following sections discuss the details of operation.

Hysteresis (High-Speed Mode Only)

Most high-speed comparators can oscillate in the linear operating region because of noise or undesired parasitic feedback. This tends to occur when the voltage on one input is equal to or very close to the voltage on the other input. The MAX975/MAX977 have internal hysteresis to counter parasitic effects and noise.

The hysteresis in a comparator creates two trip points: one for the rising input voltage and one for the falling input voltage (Figure 1). The difference between the trip points is the hysteresis. When the comparators' input voltages are equal, the hysteresis effectively causes one comparator input voltage to move quickly past the other, taking the input out of the region where oscillation occurs.

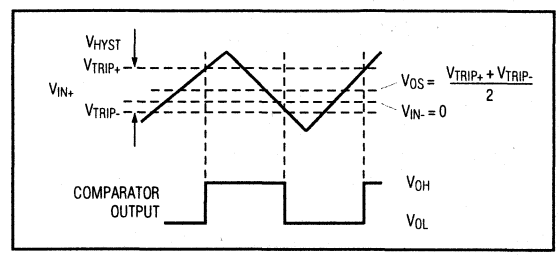


Figure 1. Input and Output Waveforms, Noninverting Input Varied

Figure 1 illustrates the case where IN- has a fixed voltage applied and IN+ is varied. If the inputs were reversed, the figure would be the same, except with an inverted output.

Auto-Standby Mode

The MAX975/MAX977's auto-standby function operates only in high-speed mode. The device enters auto-standby when OUT_ remains unchanged for a preprogrammed timeout period. In auto-standby mode, the low-power comparator is enabled while the high-speed comparator is disabled and STAT_ goes high. The logic state and sink/source capabilities of OUT_ remain unchanged, but propagation delay increases to 480ns. In this mode, the timing circuitry is powered down, and the transition detector monitors the low-power comparator for a transition. When an output transition occurs (OUT_ changes state), the timing circuitry is

Single/Dual, +3V/+5V Dual-Speed Comparators with Auto-Standby

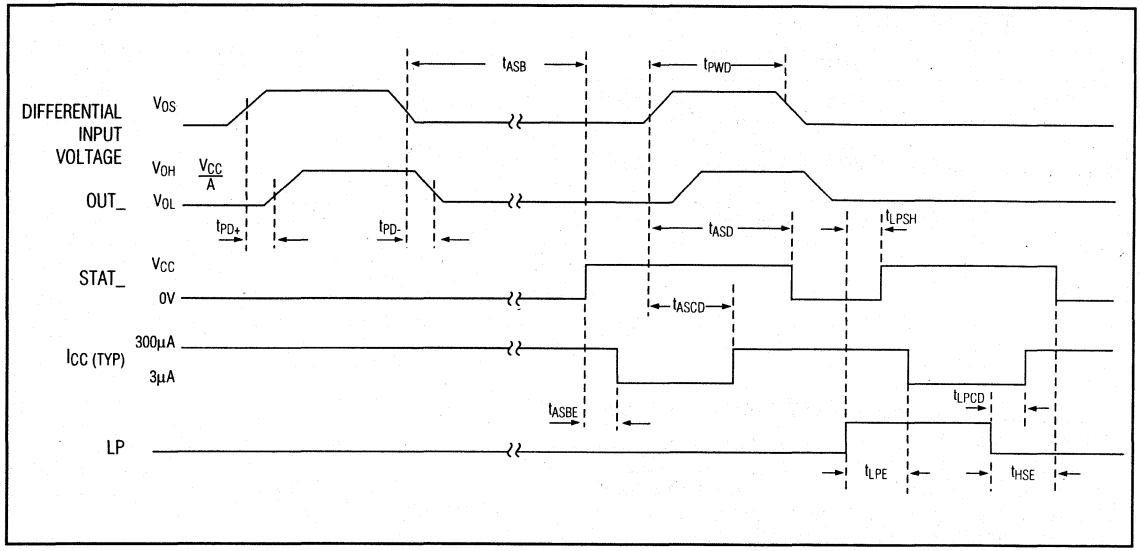


Figure 2. Timing Diagram

powered up, the high-speed comparator is enabled, the low-power comparator is disabled, and STAT goes high, placing the MAX975 back into high-speed mode (Figure 2).

Use an external capacitor, C_{STO}, to program the timeout period required for the comparator to enter auto-standby mode. Determine the capacitor required for a particular timeout period by the relationship t_{ASB} = 10 x Cµs, where C is in pF. For example, connecting a 0.1µF capacitor to STO_ results in a timeout period of 1sec. The propagation delay of OUT_ when exiting auto standby mode is equivalent to the low-power-mode propagation delay. When STAT_ goes low, the low-power comparator is disabled and the high-speed comparator is ready for operation. To bring the comparator out of auto-standby mode without a transition occurring on OUT_, toggle LP low-high-low. The LP pin is sensitive to noise. If fall times larger than 10µs are expected, bypass LP with a 0.1µF capacitor to GND. To disable auto-standby mode, drive STO_ low or connect it to ground. Note that driving STO_ low while in auto-standby mode will not bring the comparator out of auto-standby mode. Also, if driving STO_ with an open drain, leakage must be less than 1nA. On power-up, the device is in high-speed mode unless LP is high. The MAX977 operates in the same manner as the MAX975.

Low-Power Mode

Driving LP high switches the MAX975/MAX977 to low-power mode. In this mode, the supply current drops to a maximum of 5µA, and propagation delay increases typically to 480ns. The high-speed comparator is disabled and the low-power comparator is enabled for continuous operation. Return to high-speed mode by driving LP low. The LP pin is sensitive to noise. If fall times larger than 10µs are expected, bypass LP with a 0.1µF capacitor to GND. The logic state and sink/source capabilities of OUT_ remain unchanged in low-power mode.

Input-Stage Circuitry

The MAX975/MAX977 input common-mode range is from -0.2V to (V_{CC} - 1.2V). But the voltage range for each comparator input extends to both V_{CC} and GND rails. The output remains in the correct logic state while one or both of the inputs are within the common-mode range. If both input levels are out of the common-mode range, input-stage current saturation occurs and the output becomes unpredictable.

Single/Dual, +3V/+5V Dual-Speed Comparators with Auto-Standby

Applications Information

Powering Circuitry with STAT

STAT's function is to indicate the comparator's operating mode. When STAT is low, the comparator is in high-speed mode and will meet the guaranteed propagation delay. When STAT is high, the comparator is in auto-standby mode, in low-power mode, or in transition to high-speed mode. An additional feature of this pin is that it can source 3mA of current. When STAT is high, additional circuitry can be powered. This circuitry can be automatically powered up or powered down, depending on the input signal or lack of input signal received by the MAX975/MAX977.

STO_ Considerations

The charge currents for the capacitor connected to STO_ are on the order of 100nA. This necessitates caution in capacitor type selection and board layout. Capacitor leakage currents must be less than 1nA to prevent timing errors. Ceramic capacitors are available in values up to 1µF, and are an excellent choice for this application. If a larger capacitance value is needed, use parallel ceramic capacitors to get the required capacitance. Aluminum and tantalum electrolytic capacitors are not recommended due to their higher leakage currents.

Board layout can create timing errors due to parasitic effects. Make the STO_ traces as short as possible to reduce capacitance and coupling effects. When driving STO_ to disable auto-standby mode, use standard CMOS logic isolated with a low-leakage (<1nA) diode, such as National's FJT1100 (Figure 3). 15nA leakage typically results in 10% error.

The MAX977 has separate timing inputs (STOA and STOB). These pins must have separate capacitors. The timing circuits will not operate correctly if a single capacitor is used with STOA and STOB connected together.

The relationship between the timeout period and the STO_ capacitor is $t_{ASB} = 10 \times C_{STO_}$ µs, where $C_{STO_}$ is in pF. This equation is for larger capacitance values, and does not take into account variations due to board capacitance and board leakage. If less than 1ms is desired, subtract the ~3pF STO_ parasitic capacitance from the calculated value.

Circuit Layout and Bypassing

The MAX975/MAX977's high gain bandwidth requires design precautions to realize the comparator's full high-speed capability. The following precautions are recommended:

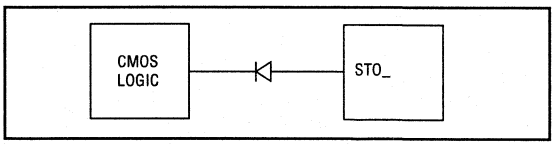


Figure 3. Driving STO_ with CMOS Logic

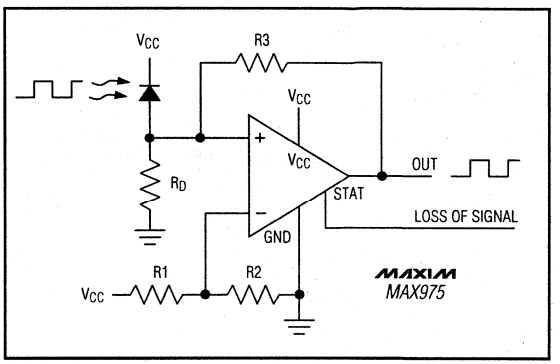


Figure 4. IR Receiver

1) Use a printed circuit board with an unbroken, low-inductance ground plane.
2) Place a decoupling capacitor (a 0.1µF ceramic capacitor is a good choice) as close to V_{CC} as possible.
3) Keep lead lengths short on the inputs and outputs, to avoid unwanted parasitic feedback around the comparators.
4) Solder the devices directly to the printed circuit board instead of using a socket.
5) Minimize input impedance.
6) For slowly varying inputs, use a small capacitor (~1000pF) across the inputs to improve stability.

IR Receiver

Figure 4 shows an application using the MAX975 as an infrared receiver. The infrared photodiode creates a current relative to the amount of infrared light present. This current creates a voltage across R_D. When this voltage level crosses the voltage applied by the voltage divider to the inverting input, the output transitions. If the photodiode is not receiving enough signal to cause transitions on the MAX975's output, STAT is used as a loss-of-signal indicator. R3 adds additional hysteresis for noise immunity.

Single/Dual, +3V/+5V Dual-Speed Comparators with Auto-Standby

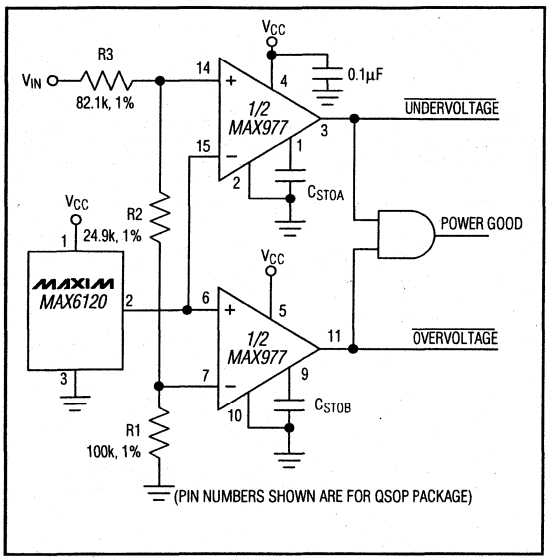


Figure 5. Window Comparator

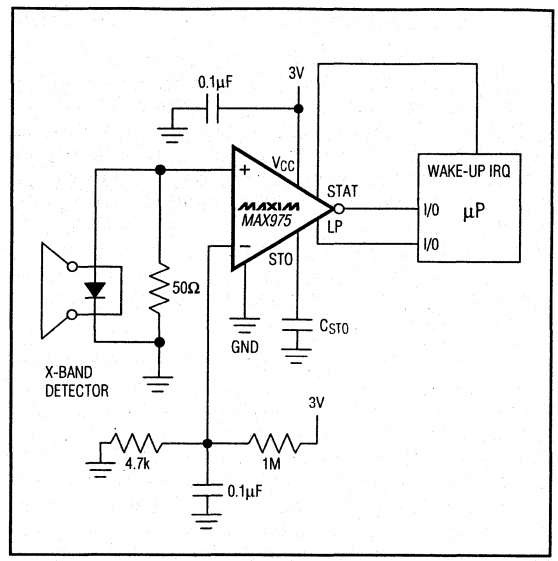


Figure 6. Toll-Tag Reader

Window Comparator

The MAX977 is ideal for making a window detector (undervoltage/overvoltage detector). The schematic shown in Figure 5 uses a MAX6120 reference and component values selected for a 2.0V undervoltage threshold and a 2.5V overvoltage threshold. Choose different thresholds by changing the values of R1, R2, and R3. OUTA provides an active-low undervoltage indication, and OUTB gives an active-low overvoltage indication. ANDing the two outputs provides an active-high, power-good signal. The design procedure is as follows:

1) Select R1. The leakage current into INB- is normally 100nA, so the current through R1 should exceed 10µA for the thresholds to be accurate. R1 values in the 50kΩ to 100kΩ range are typical.

2) Choose the overvoltage threshold (V_{OTH}) when V_{IN} is rising, and calculate R2 and R3 with the following formula:

$$R2 + R3 = R1 \times [V_{OTH} / (V_{REF} + V_H) - 1]$$

where $V_H = 1/2V_{HYST}$.

3) Choose the undervoltage threshold (V_{UTH}) when V_{IN} is falling, and calculate R2 with the following formula:

$$R2 = (R1 + R2 + R3) \times [(V_{REF} - V_H) / V_{UTH}] - R1$$

where $V_H = 1/2V_{HYST}$.

4) Calculate R3 with the following formula:

$$R3 = (R2 + R3) - R2$$

5) Verify the resistor values. The equations are as follows:

$$V_{OTH} = (V_{REF} + V_H) \times (R1 + R2 + R3) / R1$$

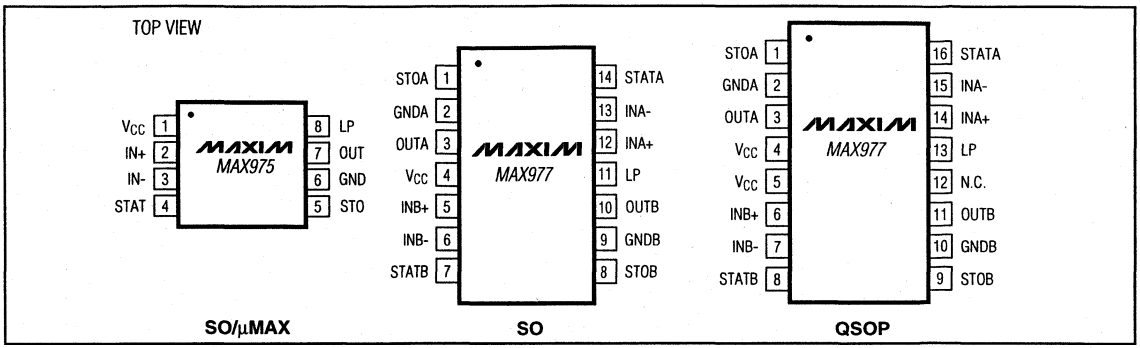
$$V_{UTH} = (V_{REF} - V_H) \times (R1 + R2 + R3) / (R1 + R2)$$

Toll-Tag Circuit

The circuit shown in Figure 6 uses a MAX975 in a very low standby-power AM demodulator circuit that wakes up a toll tag (part of an automated roadway toll-collection system). This application requires very long standby times with brief and infrequent interrogations. In the awake state, it is capable of demodulating the typical 600kHz AM carrier riding on the 2.4GHz RF signal. In this state, the comparator draws its 300µA high-speed current. After communications have ceased, or when instructed by the microcontroller, the comparator returns to its low-power state. The comparator draws only 3µA in this state, while monitoring for RF activity. Typically, this application requires two comparators and a discrete power-management and signal-switchover circuit. The MAX975 circuit is smaller, simpler, less costly, and saves design time.

Single/Dual, +3V/+5V Dual-Speed Comparators with Auto-Standby

Pin Configurations



Chip Information

TRANSISTOR COUNT: 522 (MAX975)
1044 (MAX977)

3

ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
10/96

MAXIM

Dual/Quad, +3V/+5V High-Speed Comparators

General Description

The MAX976/MAX978 dual/quad high-speed comparators are optimized for +3V/+5V single-supply applications. Propagation delay is 28ns, while supply current is only 300µA. The MAX976/MAX978's inputs have a common-mode voltage range of -0.2V to (V_{CC} - 1.2V). The differential input voltage range extends rail to rail. The outputs swing rail to rail without external pull-up circuitry, making these devices ideal for both CMOS and TTL logic. All inputs and outputs can tolerate a continuous short-circuit fault condition to either rail. The comparator's internal hysteresis ensures clean output switching, even with slow-moving input signals.

The dual MAX976 is available in 8-pin SO and µMAX packages, while the quad MAX978 is available in 14-pin SO and 16-pin QSOP packages.

Features

- ♦ **28ns Propagation Delay (5mV Overdrive)**
- ♦ **300µA Supply Current**
- ♦ **+3V/+5V Single-Supply Operation**
- ♦ **Rail-to-Rail Outputs**
- ♦ **Internal Hysteresis**
- ♦ **8-Pin µMAX Package (MAX976)**
  16-Pin QSOP Package (MAX978)

Applications

Battery-Powered Systems
Threshold Detectors/Discriminators
3V Systems
IR Receivers
Digital Line Receivers

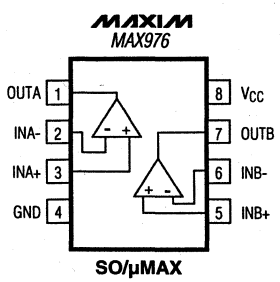
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX976ESA	-40°C to +85°C	8 SO
MAX976EUA	-40°C to +85°C	8 µMAX
MAX978ESD	-40°C to +85°C	14 SO
MAX978EEE	-40°C to +85°C	16 QSOP

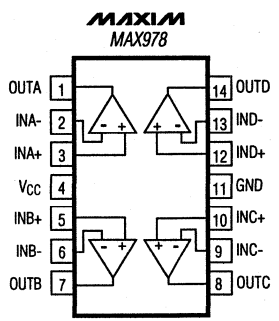
3

Pin Configurations

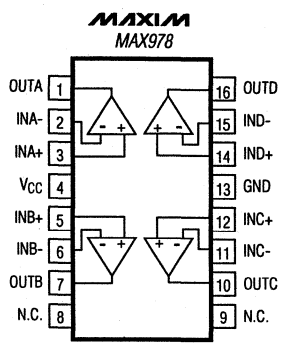
TOP VIEW



SO/µMAX



SO



QSOP

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19-1087; Rev 0; 8/96

MAXIM

Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply Rail-to-Rail I/O Op Amps

General Description

The MAX4122–MAX4129 family of operational amplifiers combines wide bandwidth and excellent DC accuracy with rail-to-rail operation at the inputs and outputs. These devices require only 650µA per amplifier, and operate from either a single supply (+2.7V to +6.5V) or dual supplies (±1.35V to ±3.25V) with a common-mode voltage range that extends beyond V_{EE} and V_{CC}. They are capable of driving 250Ω loads. The MAX4122/MAX4123/MAX4126/MAX4127/MAX4129 have a 5MHz gain bandwidth product, while the decompensated MAX4124/MAX4125/MAX4128 (stable at closed-looped gains of 10 or greater) have a 25MHz gain bandwidth product. In addition, the MAX4123/MAX4125/MAX4127 feature a shutdown mode in which the outputs are in a high-impedance state and the supply current is reduced to only 25µA per amplifier.

With their rail-to-rail input common-mode range and output swing, these amplifiers are ideal for low-voltage single-supply operation. Although the minimum operating voltage is specified at 2.7V, the devices typically operate down to 1.8V. In addition, low offset voltage and high speed make them the ideal signal-conditioning stages for precision, low-voltage data-acquisition systems. **The MAX4122 and MAX4124 come in the space-saving 5-pin SOT23-5 package.**

Selection Table

PART	BW (MHz)	AMPS/ PKG.	SHUT-DOWN MODE	PIN-PACKAGE
MAX4122	5	1	—	5 SOT23-5
MAX4123	5	1	Yes	8 SO/µMAX
MAX4124	25	1	—	5 SOT23-5
MAX4125	25	1	Yes	8 SO/µMAX
MAX4126	5	2	—	8 SO/µMAX
MAX4127	5	2	Yes	14 SO
MAX4128	25	2	—	8 SO/µMAX
MAX4129	5	4	—	14 SO

Applications

Battery-Powered Instruments
Portable Equipment
Data-Acquisition Systems
Signal Conditioning
Low-Power, Low-Voltage Applications

Features

- ♦ **5-Pin SOT23-5 Package (MAX4122/4)**
- ♦ **+2.7V to +6.5V Single-Supply Operation**
- ♦ **Rail-to-Rail Input Common-Mode Voltage Range**
- ♦ **Rail-to-Rail Output Voltage Swing**
- ♦ **5MHz Gain-Bandwidth Product (MAX4122/3/6/7/9)**
  25MHz Gain-Bandwidth Product (MAX4124/5/8)
- ♦ **650µA Quiescent Current per Amplifier**
- ♦ **Optional Shutdown Function (MAX4123/5/7)**
- ♦ **200µV Offset Voltage**
- ♦ **No Phase Reversal for Overdriven Inputs**
- ♦ **Drive 250Ω Loads**
- ♦ **Stable with 500pF Capacitive Loads**
- ♦ **Unity-Gain Stable (MAX4122/3/6/7/9)**
  Stable at Gains ≥ 10V/V (MAX4124/5/8)

Ordering Information

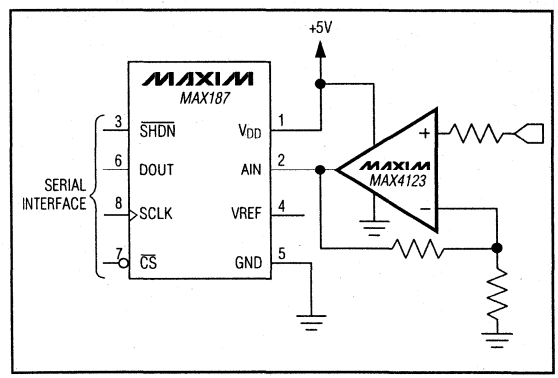
PART	TEMP. RANGE	PIN-PACKAGE	MARKING INFO.
MAX4122EUK	-40°C to +85°C	5 SOT23-5	AAAZ
MAX4123C/D	0°C to +70°C	Dice*	—
MAX4123ESA	-40°C to +85°C	8 SO	—
MAX4123EUA	-40°C to +85°C	8 µMAX	—

Ordering Information continued at end of data sheet.

**Dice are specified at T_A = +25°C, DC parameters only.*

Pin Configurations appear at end of data sheet.

Typical Operating Circuit



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Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply Rail-to-Rail I/O Op Amps

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}-V_{EE}) 7.5V
IN+, IN-, $\overline{SHDN}$ Voltage ..... (V_{CC} + 0.3V) to (V_{EE} - 0.3V)
Output Short-Circuit Duration (Note 1) ..... Continuous
(short to either supply)
Continuous Power Dissipation (T_A = +70°C)
5-pin SOT23-5 (derate 7.1mW/°C above +70°C) 571mW
8-pin SO (derate 5.88mW/°C above +70°C) 471mW
8-pin µMAX (derate 4.10mW/°C above +70°C) 330mW
14-pin SO (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Range
MAX412_E__ ..... -40°C to +85°C
Maximum Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: Provided that the maximum package power-dissipation rating is met.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +6.5V, V_{EE} = 0V, V_{CM} = 0V, V_{OUT} = V_{CC} / 2, R_L tied to V_{CC} / 2, $\overline{SHDN}$ ≥ 2V (or open), **T_A = +25°C**, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{CM} = V_{EE} to V_{CC}	MAX4123ESA/MAX4125ESA		±0.20	±0.60	mV
		MAX4122EUK/MAX4124EUK		±0.35	±1.00	
		MAX4123EUA/MAX4125EUA		±0.35	±1.20	
		MAX4126ESA/MAX4127ESD/MAX4128ESA		±0.25	±0.75	
		MAX4126EUA/MAX4128EUA		±0.40	±1.50	
		MAX4129ESD		±0.35	±1.50	
Input Bias Current	V_{CM} = V_{EE} to V_{CC}			±50	±150	nA
Input Offset Current	V_{CM} = V_{EE} to V_{CC}			±1	±12	nA
Differential Input Resistance	-1.5V < V_{DIFF} < 1.5V			500		kΩ
Common-Mode Input Voltage Range			V_{EE} - 0.25		V_{CC} + 0.25	V
Common-Mode Rejection Ratio	(V_{EE} - 0.25) < V_{CM} < (V_{CC} + 0.25V)	MAX4123ESA/MAX4125ESA	78	98		dB
		MAX4122EUK/MAX4124EUK	70	90		
		MAX4123EUA/MAX4125EUA	68	88		
		MAX4126ESA/MAX4127ESD/MAX4128ESA	74	94		
		MAX4126EUA/MAX4128EUA	66	86		
		MAX4129ESD	64	84		
Power-Supply Rejection Ratio	V_{CC} = 2.7V to 6.5V		78	100		dB
Output Resistance	A_V = 1			0.1		Ω
Off-Leakage Current	$\overline{SHDN}$ < 0.8V, V_{OUT} = 0V to V_{CC}			±0.1	±1	µA
Large-Signal Voltage Gain	V_{CC} = 2.7V	V_{OUT} = 0.25V to 2.45V, R_L = 100kΩ	92	104		dB
		V_{OUT} = 0.4V to 2.3V, R_L = 250Ω	72	80		
	V_{CC} = 5V	V_{OUT} = 0.25V to 4.75V, R_L = 100kΩ	94	106		
		V_{OUT} = 0.4V to 4.6V, R_L = 250Ω	75	84		

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.7V to +6.5V, V_{EE} = 0V, V_{CM} = 0V, V_{OUT} = V_{CC} / 2, R_L tied to V_{CC} / 2, $\overline{SHDN}$ ≥ 2V (or open), **T_A = +25°C**, unless otherwise noted.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Output Voltage Swing	MAX4122/ MAX4123/ MAX4124/ MAX4125	R_L = 100kΩ	V_{CC} - V_{OH}		12	20	mV
			V_{OL} - V_{EE}		20	35	
		R_L = 250Ω	V_{CC} - V_{OH}		240	290	
			V_{OL} - V_{EE}		125	170	
	MAX4126/ MAX4127/ MAX4128/ MAX4129	R_L = 100kΩ	V_{CC} - V_{OH}		15	30	
			V_{OL} - V_{EE}		25	40	
		R_L = 250Ω	V_{CC} - V_{OH}		280	330	
			V_{OL} - V_{EE}		180	230	
Output Short-Circuit Current					50		mA
$\overline{SHDN}$ Logic Threshold	MAX4123/MAX4125/MAX4127		Low			0.8	V
			High	2.0			
$\overline{SHDN}$ Input Current	MAX4123/MAX4125/MAX4127				±1	±3	µA
Operating Supply-Voltage Range				2.7		6.5	V
Supply Current per Amplifier	V_{CM} = V_{OUT} = V_{CC} / 2		V_{CC} = 2.7V		650	750	µA
			V_{CC} = 5V		725	825	
Shutdown Supply Current per Amplifier	$\overline{SHDN}$ > 0.8V, MAX4123/MAX4125/MAX4127		V_{CC} = 2.7V		25	40	µA
			V_{CC} = 5V		40	60	

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +6.5V, V_{EE} = 0V, V_{CM} = 0V, V_{OUT} = V_{CC} / 2, R_L tied to V_{CC} / 2, $\overline{SHDN}$ ≥ 2V (or open), **T_A = -40°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{CM} = V_{EE} to V_{CC}	MAX4123ESA/MAX4125ESA			±0.75	mV
		MAX4122EUK/MAX4124EUK			±3.50	
		MAX4123EUA/MAX4125EUA			±4.40	
		MAX4126ESA/MAX4127ESD/MAX4128ESA			±0.95	
		MAX4126EUA/MAX4128EUA			±4.70	
		MAX4129ESD			±4.00	
Input Offset Voltage Tempco				±2		µV/°C
Input Bias Current	V_{CM} = V_{EE} to V_{CC}				±160	nA
Input Offset Current	V_{CM} = V_{EE} to V_{CC}				±18	nA
Common-Mode Input Voltage Range			V_{EE} - 0.20		V_{CC} + 0.20	V
Common-Mode Rejection Ratio	(V_{EE} - 0.2V) < V_{CM} < (V_{CC} + 0.2V)	MAX4123ESA/MAX4125ESA	76			dB
		MAX4122EUK/MAX4124EUK	62			
		MAX4123EUA/MAX4125EUA	60			
		MAX4126ESA/MAX4127ESD/MAX4128ESA	74			
		MAX4126EUA/MAX4128EUA	58			
		MAX4129ESD	60			

Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply Rail-to-Rail I/O Op Amps

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.7V to +6.5V, V_{EE} = 0V, V_{CM} = 0V, V_{OUT} = V_{CC} / 2, R_L tied to V_{CC} / 2, $\overline{SHDN}$ ≥ 2V (or open), **T_A = -40°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Power-Supply Rejection Ratio	V_{CC} = 2.7V to 6.5V			74			dB
Off-Leakage Current	$\overline{SHDN}$ < 0.8V, V_{OUT} = 0V to V_{CC}					±12	µA
Large-Signal Voltage Gain	V_{CC} = 2.7V	V_{OUT} = 0.25V to 2.45V, R_L = 100kΩ		84			dB
		V_{OUT} = 0.4V to 2.3V, R_L = 250Ω		66			
	V_{CC} = 5V	V_{OUT} = 0.25V to 4.75V, R_L = 100kΩ		86			
		V_{OUT} = 0.4V to 4.6V, R_L = 250Ω		68			
Output Voltage Swing	MAX4122/ MAX4123/ MAX4124/ MAX4125	R_L = 100kΩ	V_{CC} - V_{OH}			25	mV
			V_{OL} - V_{EE}			40	
		R_L = 250Ω	V_{CC} - V_{OH}			300	
			V_{OL} - V_{EE}			190	
	MAX4126/ MAX4127/ MAX4128/ MAX4129	R_L = 100kΩ	V_{CC} - V_{OH}			35	
			V_{OL} - V_{EE}			50	
		R_L = 250Ω	V_{CC} - V_{OH}			350	
			V_{OL} - V_{EE}			250	
$\overline{SHDN}$ Logic Threshold	MAX4123/MAX4125/MAX4127		Low			0.8	V
			High	2.0			
$\overline{SHDN}$ Input Current	MAX4123/MAX4125/MAX4127					±3	µA
Operating Supply-Voltage Range				2.7		6.5	V
Supply Current per Amplifier	V_{CM} = V_{OUT} = V_{CC} / 2		V_{CC} = 2.7V			775	µA
			V_{CC} = 5V			850	
Shutdown Supply Current per Amplifier	$\overline{SHDN}$ < 0.8V, MAX4123/MAX4125/MAX4127		V_{CC} = 2.7V			50	µA
			V_{CC} = 5V			70	

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +6.5V, V_{EE} = 0V, $\overline{SHDN}$ ≥ 2V (or open), **T_A = +25°C**, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Gain-Bandwidth Product	MAX4122/23/26/27/29		5		MHz
	MAX4124/25/28 (A_V ≥ 10)		25		
Phase Margin	MAX4122/23/26/27/29		64		degrees
	MAX4124/25/28 (A_V ≥ 10)		60		
Gain Margin	MAX4122/23/26/27/29		12		dB
	MAX4124/25/28 (A_V ≥ 10)		10		
Total Harmonic Distortion	f = 10kHz, V_{OUT} = 2Vp-p, MAX4122/23/26/27/29 (A_V = 1)		0.003		%
Slew Rate	MAX4122/23/26/27/29		2		V/µs
	MAX4124/25/28 (A_V ≥ 10)		10		
Settling Time to 0.01%	MAX4122/23/26/27/29 (A_V = 1), V_{OUT} = 2V step		2.0		µs
	MAX4124/25/28 (A_V ≥ 10), V_{OUT} = 2V step		1.3		
Turn-On Time	V_{CC} = 0V to 3V step, V_{OUT} = V_{CC} / 2		1		µs

AC ELECTRICAL CHARACTERISTICS (continued)

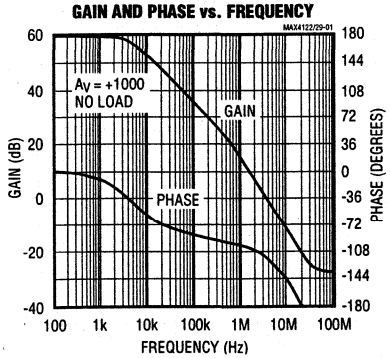
(V_{CC} = +2.7V to +6.5V, V_{EE} = 0V, $\overline{SHDN}$ ≥ 2V (or open), **T_A = +25°C**, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{SHDN}$ Delay	V_{CC} = 3V, V_{OUT} = V_{CC} / 2, MAX4123/25/27	Enable		1		µs
		Disable		0.2		
Input Capacitance				3		pF
Input Noise Voltage Density	f = 1kHz			22		nV/√Hz
Input Noise Current Density	f = 1kHz			0.4		pA/√Hz
Amp-Amp Isolation	MAX4126/27/28/29			135		dB
Capacitive Load Stability	MAX4122/23/26/27/29 (A_V = 1)			500		pF
	MAX4124/25/28 (A_V ≥ 10)			500		

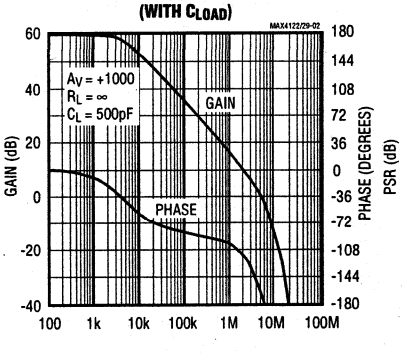
Typical Operating Characteristics

(V_{CC} = +5V, V_{EE} = 0V, V_{CM} = V_{CC} / 2, T_A = +25°C, unless otherwise noted.)

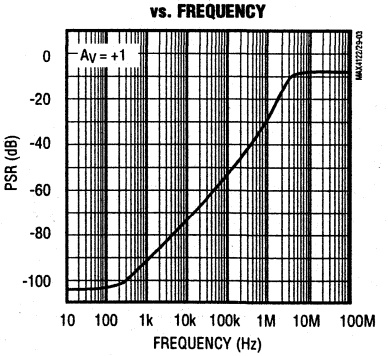
MAX4122/23/26/27/29
GAIN AND PHASE vs. FREQUENCY



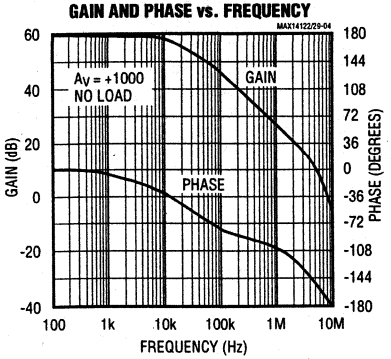
MAX4122/23/26/27/29
GAIN AND PHASE vs. FREQUENCY
(WITH C_{LOAD})



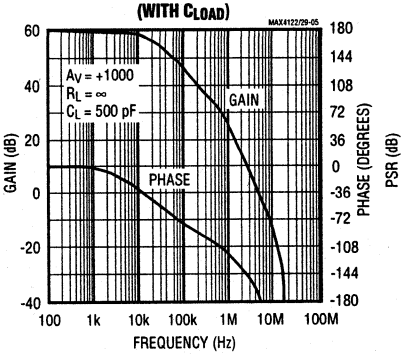
MAX4122/23/26/27/29
POWER-SUPPLY REJECTION
vs. FREQUENCY



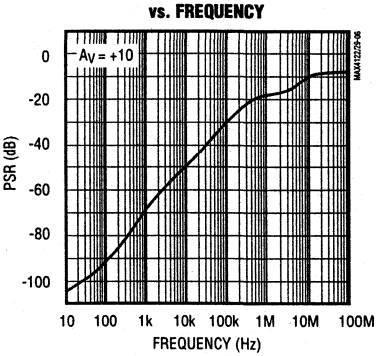
MAX4124/25/28
GAIN AND PHASE vs. FREQUENCY



MAX4124/25/28
GAIN AND PHASE vs. FREQUENCY
(WITH C_{LOAD})



MAX4124/25/28
POWER-SUPPLY REJECTION
vs. FREQUENCY

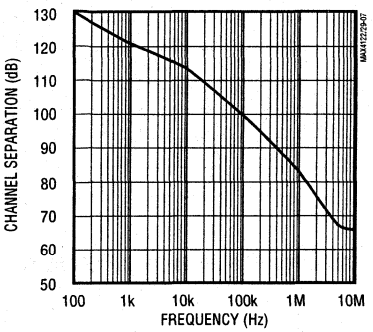


Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply Rail-to-Rail I/O Op Amps

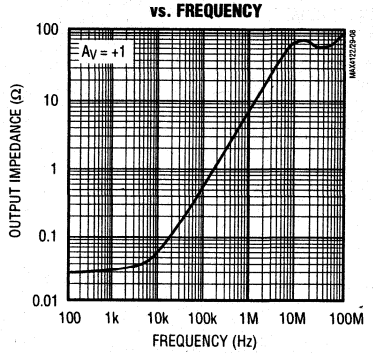
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = 0V, V_{CM} = V_{CC} / 2, T_A = +25°C, unless otherwise noted.)

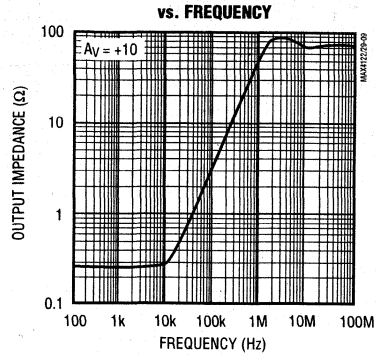
MAX4126/27/28/29
CHANNEL SEPARATION vs. FREQUENCY



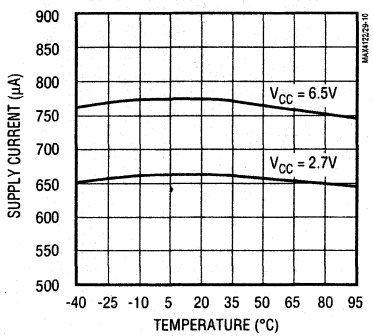
MAX4122/23/26/27/29
OUTPUT IMPEDANCE vs. FREQUENCY



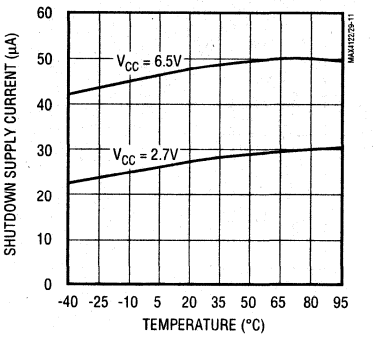
MAX4124/25/28
OUTPUT IMPEDANCE vs. FREQUENCY



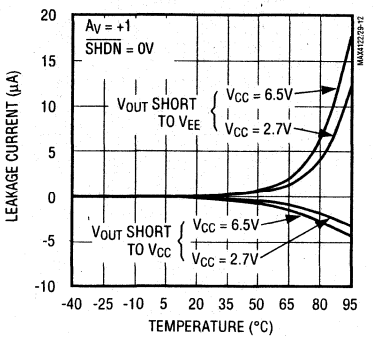
SUPPLY CURRENT PER AMPLIFIER vs. TEMPERATURE



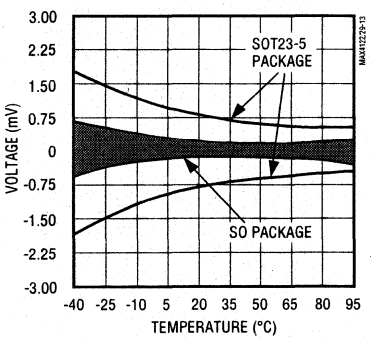
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



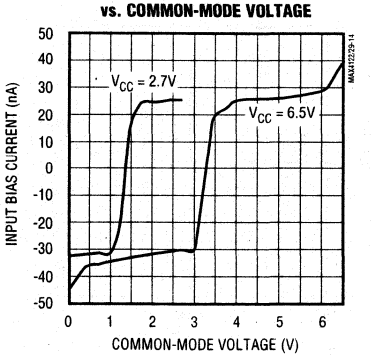
OUTPUT LEAKAGE CURRENT vs. TEMPERATURE



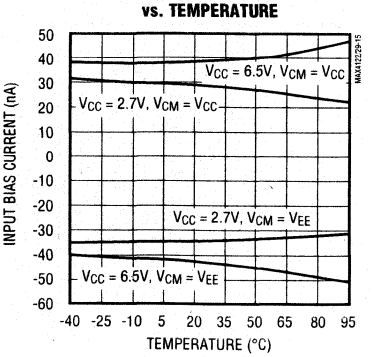
INPUT OFFSET VOLTAGE vs. TEMPERATURE



INPUT BIAS CURRENT vs. COMMON-MODE VOLTAGE



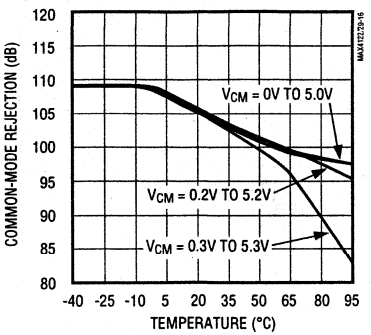
INPUT BIAS CURRENT vs. TEMPERATURE



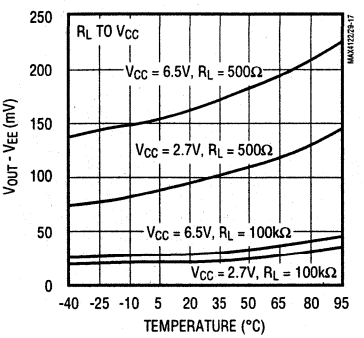
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = 0V, V_{CM} = V_{CC} / 2, T_A = +25°C, unless otherwise noted.)

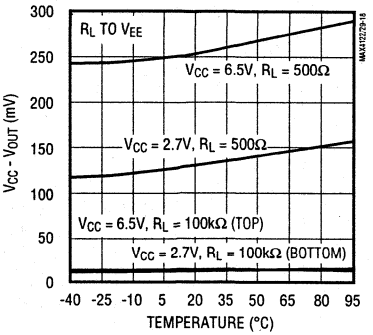
COMMON-MODE REJECTION vs. TEMPERATURE



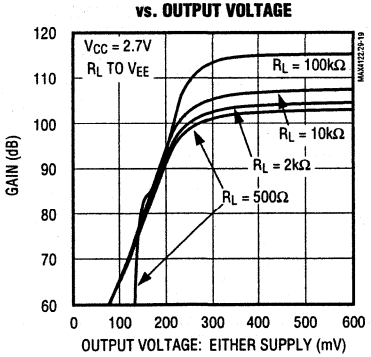
MINIMUM OUTPUT VOLTAGE vs. TEMPERATURE



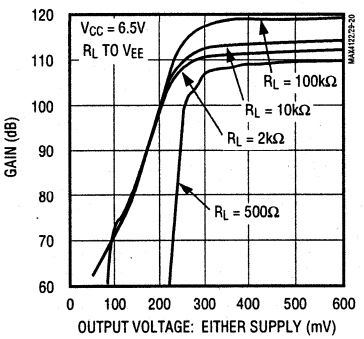
MAXIMUM OUTPUT VOLTAGE vs. TEMPERATURE



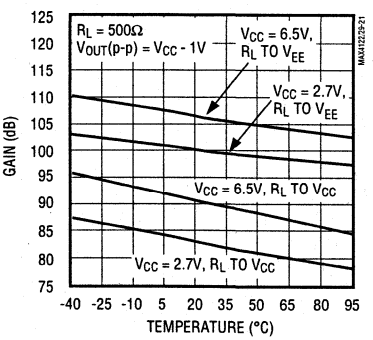
LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE



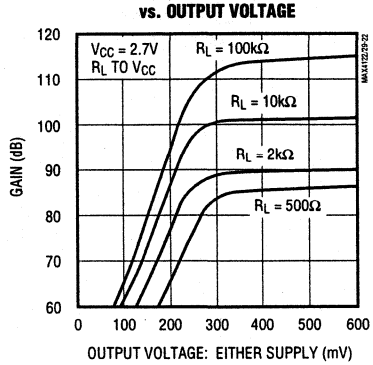
LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE



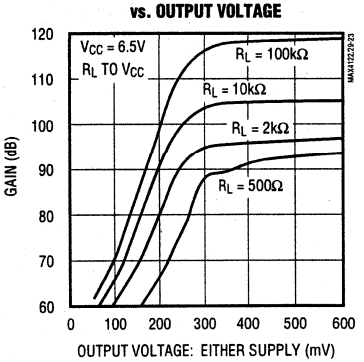
LARGE-SIGNAL GAIN vs. TEMPERATURE



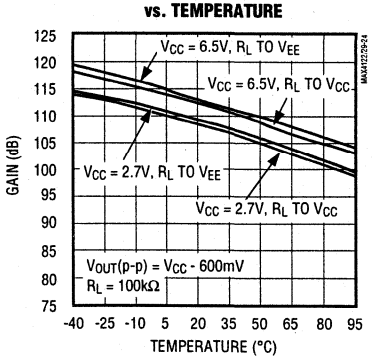
LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE



LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE



LARGE-SIGNAL GAIN vs. TEMPERATURE

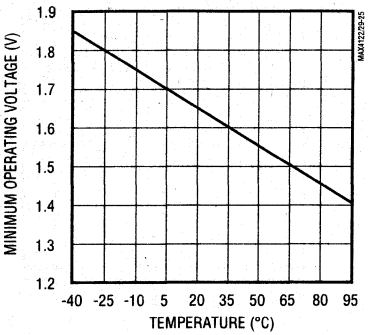


Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply Rail-to-Rail I/O Op Amps

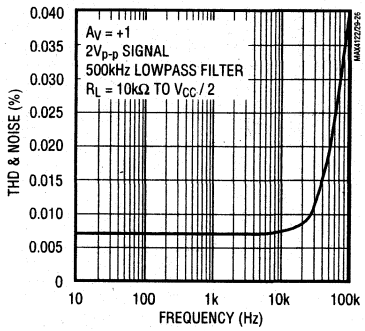
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = 0V, V_{CM} = V_{CC} / 2, T_A = +25°C, unless otherwise noted.)

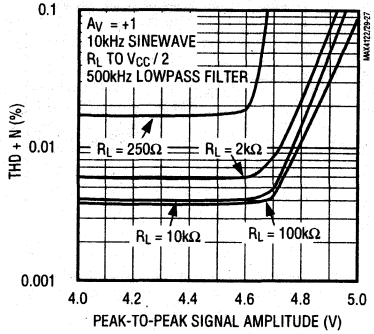
MAX4123
MINIMUM OPERATING VOLTAGE vs. TEMPERATURE



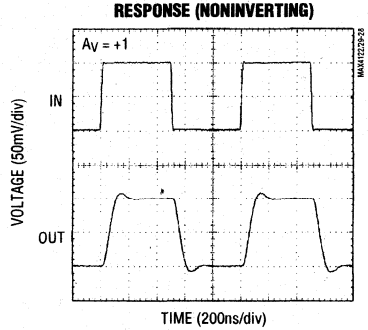
MAX4122/23/26/27/29 TOTAL HARMONIC DISTORTION AND NOISE vs. FREQUENCY



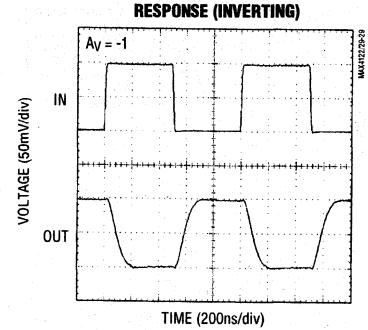
MAX4123
TOTAL HARMONIC DISTORTION AND NOISE vs. PEAK-TO-PEAK SIGNAL AMPLITUDE



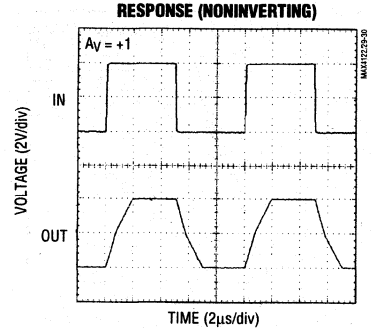
MAX4122/23/26/27/29
SMALL-SIGNAL TRANSIENT RESPONSE (NONINVERTING)



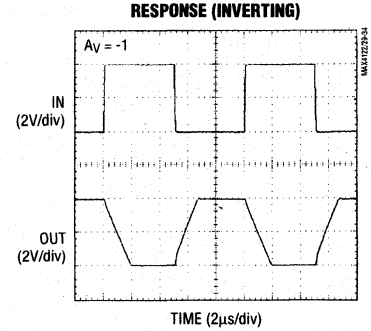
MAX4122/23/26/27/29
SMALL-SIGNAL TRANSIENT RESPONSE (INVERTING)



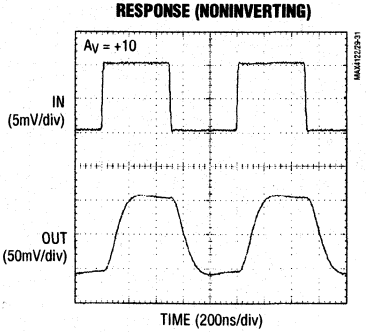
MAX4122/23/26/27/29
LARGE-SIGNAL TRANSIENT RESPONSE (NONINVERTING)



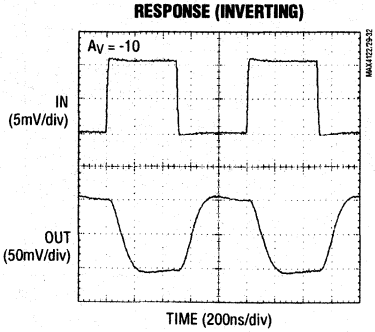
MAX4122/23/26/27/29
LARGE-SIGNAL TRANSIENT RESPONSE (INVERTING)



MAX4124/25/28
SMALL-SIGNAL TRANSIENT RESPONSE (NONINVERTING)



MAX4124/25/28
SMALL-SIGNAL TRANSIENT RESPONSE (INVERTING)

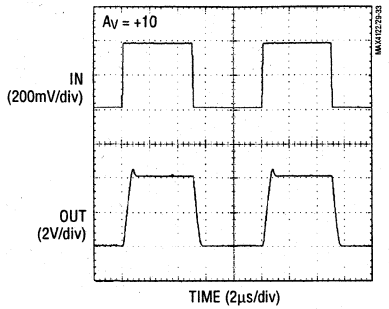


Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply Rail-to-Rail I/O Op Amps

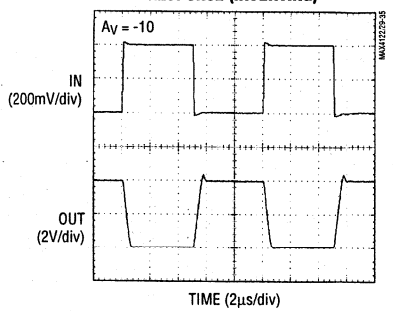
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = 0V, V_{CM} = V_{CC} / 2, T_A = +25°C, unless otherwise noted.)

MAX4124/25/28 LARGE-SIGNAL TRANSIENT RESPONSE (NONINVERTING)



MAX4124/25/28 LARGE-SIGNAL TRANSIENT RESPONSE (INVERTING)



Pin Description

PIN					NAME	FUNCTION
MAX4122 MAX4124	MAX4123 MAX4125	MAX4126 MAX4128	MAX4127	MAX4129		
1	6	—	—	—	OUT	Output
2	4	4	4	11	V_{EE}	Negative Supply. Ground for single-supply operation.
3	3	—	—	—	IN+	Noninverting Input
4	2	—	—	—	IN-	Inverting Input
5	7	8	14	4	V_{CC}	Positive Supply
—	1, 5	—	5, 7, 8, 10	—	N.C.	No Connect
—	8	—	—	—	$\overline{SHDN}$	Shutdown Control. Tie high or leave floating to enable amplifier.
—	—	1, 7	1, 13	1, 7	OUT1, OUT2	Outputs for amps 1 and 2
—	—	2, 6	2, 12	2, 6	IN1-, IN2-	Inverting Inputs for amps 1 and 2
—	—	3, 5	3, 11	3, 5	IN1+, IN2+	Noninverting Inputs for amps 1 and 2
—	—	—	6, 9	—	$\overline{SHDN1}$, $\overline{SHDN2}$	Shutdown Control for amps 1 and 2. Tie high or leave floating to enable amplifier.
—	—	—	—	8, 14	OUT3, OUT4	Outputs for amps 3 and 4
—	—	—	—	9, 13	IN3-, IN4-	Inverting Inputs for amps 3 and 4
—	—	—	—	10, 12	IN3+, IN4+	Noninverting Inputs for amps 3 and 4

Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply Rail-to-Rail I/O Op Amps

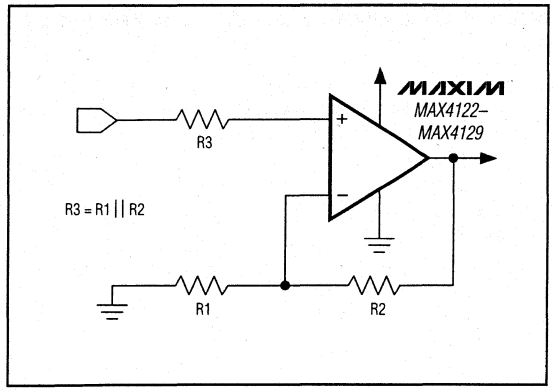


Figure 1a. Reducing Offset Error Due to Bias Current (Noninverting)

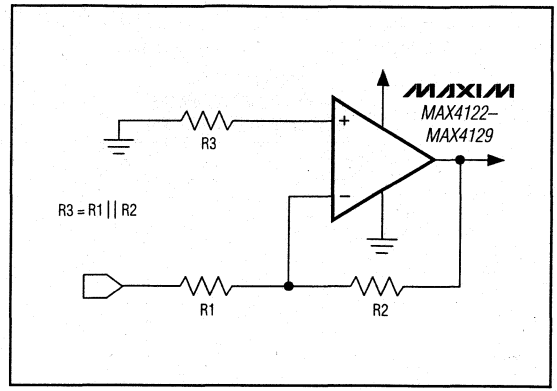


Figure 1b. Reducing Offset Error Due to Bias Current (Inverting)

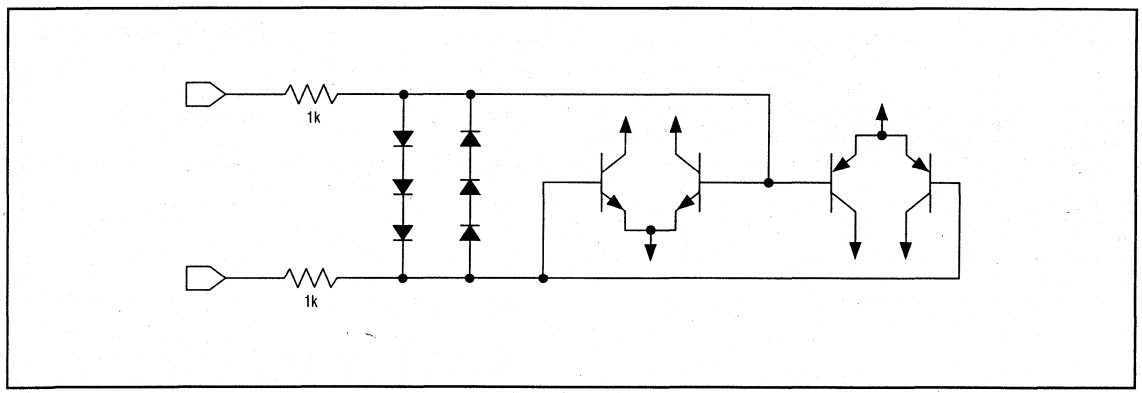


Figure 2. Input Protection Circuit

Applications Information

Rail-to-Rail Input Stage

Devices in the MAX4122–MAX4129 family of high-speed amplifiers have rail-to-rail input and output stages designed for low-voltage single-supply operation. The input stage consists of separate NPN and PNP differential stages, which combine to provide an input common-mode range extending 0.2V beyond the supply rails. The PNP stage is active for input voltages close to the negative rail, and the NPN stage is active for input voltages near the positive rail. The input offset voltage is typically below 200µV. The switchover transition region, which occurs near $V_{CC}/2$, has been extended to minimize the slight degradation in CMRR caused by the mismatch of the input pairs. Their low offset voltage, high bandwidth, and rail-to-rail common-mode range make these op amps excellent choices for precision low-voltage data-acquisition systems.

Since the input stage switches between the NPN and PNP pairs, the input bias current changes polarity as the input voltage passes through the transition region. To reduce the offset error caused by input bias currents flowing through external source impedances, match the effective impedance seen by each input (Figures 1a, 1b). High source impedances, together with the input capacitance, can create a parasitic pole that produces an underdamped signal response. Reducing the input impedance or placing a small (2pF to 10pF) capacitor across the feedback resistor improves the response.

The MAX4122–MAX4129's inputs are protected from large differential input voltages by 1kΩ series resistors and back-to-back triple diodes across the inputs (Figure 2). For differential input voltages less than 1.8V the input resistance is typically 500kΩ. For differential input voltages greater than 1.8V the input resistance is approximately 2kΩ, and the input bias current is determined by the following equation:

$$I_{BIAS} = \frac{V_{DIFF} - 1.8V}{2k\Omega}$$

Rail-to-Rail Output Stage

The minimum output voltage will be within millivolts of ground for single-supply operation where the load is referenced to ground (V_{EE}). Figure 3 shows the input voltage range and output voltage swing of a MAX4123 connected as a voltage follower. With a +3V supply and the load tied to ground, the output swings from 0.00V to 2.90V. The maximum output voltage swing depends on the load, but will be within 150mV of a +3V supply, even with the maximum load (500Ω to ground).

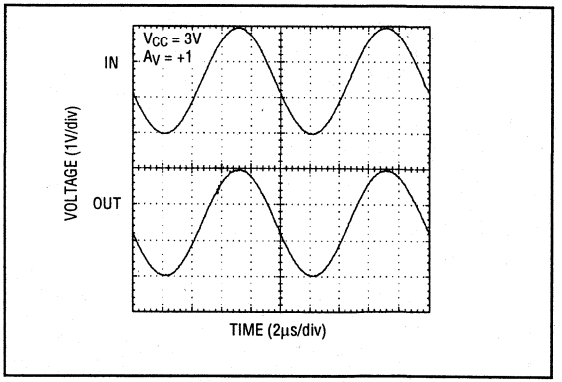


Figure 3. Rail-to-Rail Input /Output Voltage Range

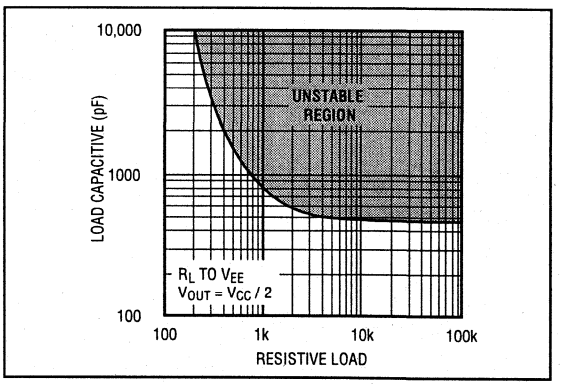


Figure 4. Capacitive-Load Stability

Driving a capacitive load can cause instability in most high-speed op amps, especially those with low quiescent current. The MAX4122–MAX4129 have a high tolerance for capacitive loads. They are stable with capacitive loads up to 500pF. Figure 4 gives the stable operating region for capacitive loads. Figures 5–8 show the response with capacitive loads, and the results of adding an isolation resistor in series with the output (Figure 9). The resistor improves the circuit's phase margin by isolating the load capacitor from the op amp's output.

Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply Rail-to-Rail I/O Op Amps

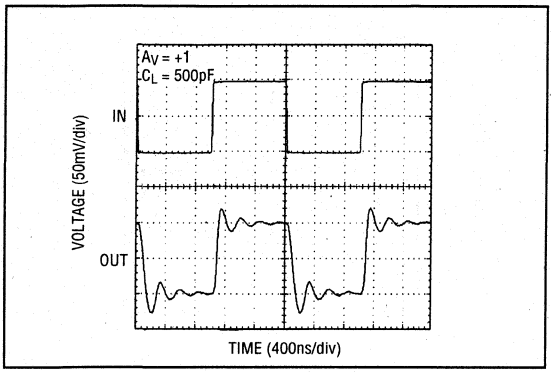


Figure 5. MAX4122/23/26/27/29 Small-Signal Transient Response with Capacitive Load

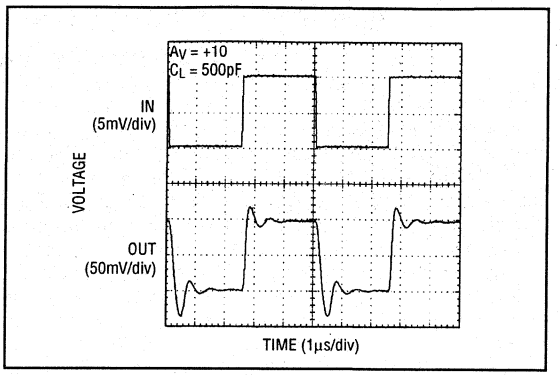


Figure 6. MAX4124/25/28 Small-Signal Transient Response with Capacitive Load

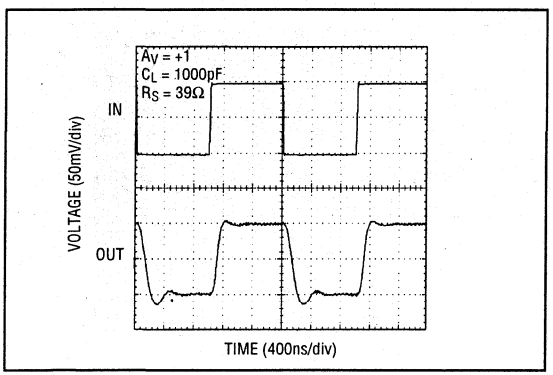


Figure 7. MAX4122/23/26/27/29 Transient Response to Capacitive Load with Isolation Resistor

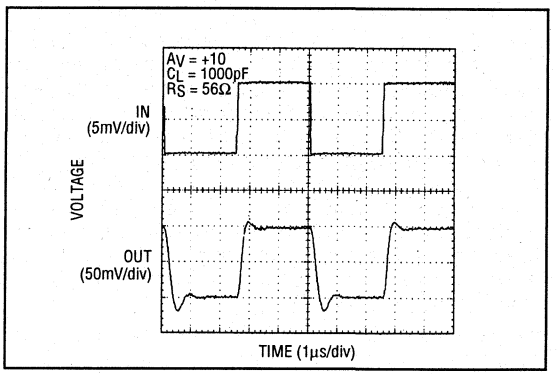


Figure 8. MAX4124/25/28 Transient Response to Capacitive Load with Isolation Resistor

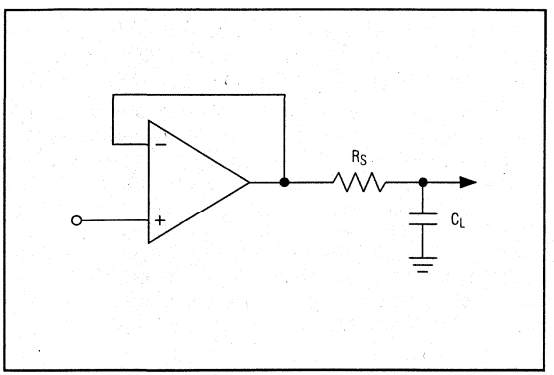


Figure 9. Capacitive-Load-Driving Circuit

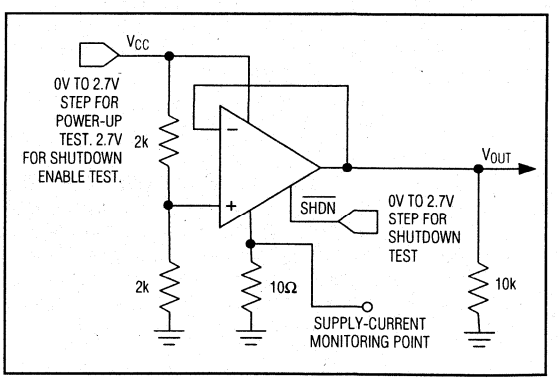


Figure 10. Power-Up/Shutdown Test Circuit

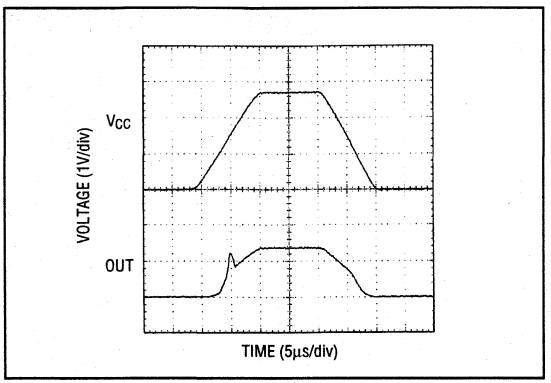


Figure 11. Power-Up Output Voltage

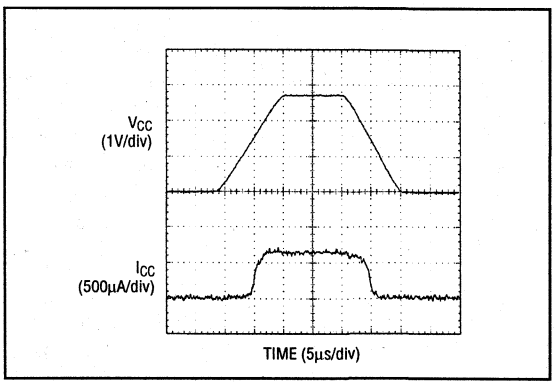


Figure 12. Power-Up Supply Current

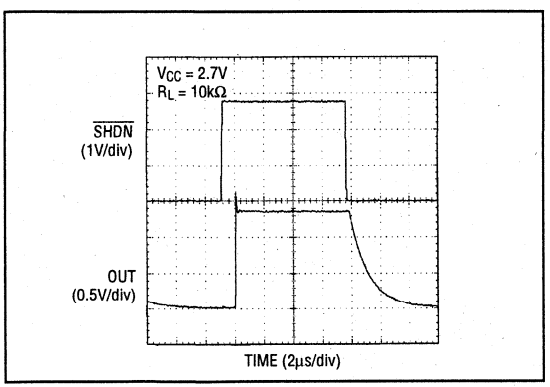


Figure 13. Shutdown Output Voltage

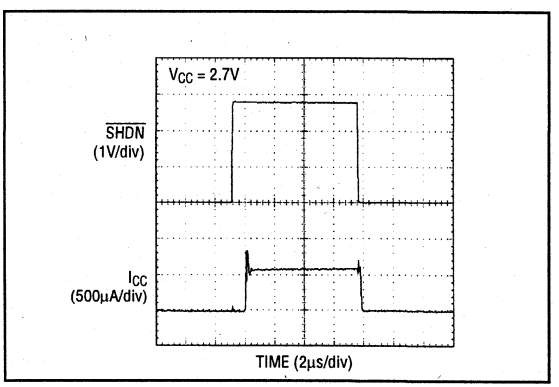


Figure 14. Shutdown Enable/Disable Supply Current

Power-Up and Shutdown Mode

The MAX4122–MAX4129 amplifiers typically settle within 1µs after power-up. Using the test circuit of Figure 10, Figures 11 and 12 show the output voltage and supply current on power-up.

The MAX4123, MAX4125, and MAX4127 have a shutdown option. When the shutdown pin ($\overline{SHDN}$) is pulled low, the supply current drops below 25µA per amplifier and the amplifiers are disabled with the outputs in a high-impedance state. Pulling $\overline{SHDN}$ high or leaving it floating enables the amplifier. In the dual-amplifier MAX4129, the shutdown functions operate independently. Figures 13 and 14 show the output voltage and supply current responses of the MAX4123 to a shutdown pulse.

Power Supplies and Layout

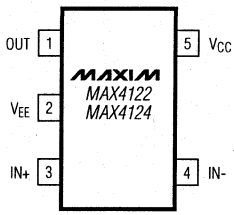
The MAX4122–MAX4129 operate from a single +2.7V to +6.5V power supply, or from dual supplies of ±1.35V to ±3.25V. For single-supply operation, bypass the power supply with a 0.1µF ceramic capacitor in parallel with at least 1µF. For dual supplies, bypass each supply to ground.

Good layout improves performance by decreasing the amount of stray capacitance at the op amp's inputs and outputs. To decrease stray capacitance, minimize trace lengths and resistor leads by placing external components close to the op amp's pins.

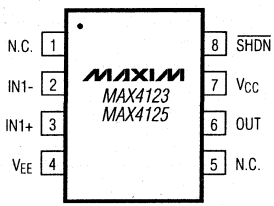
Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply Rail-to-Rail I/O Op Amps

Pin Configurations

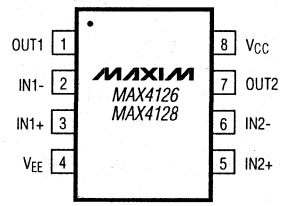
TOP VIEW



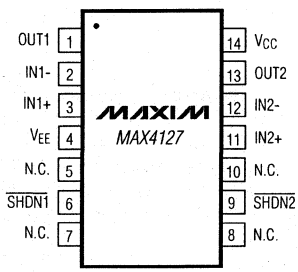
SOT23-5



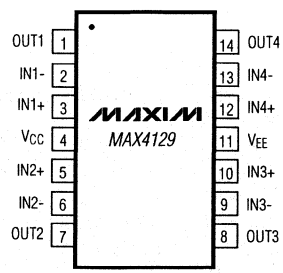
SO/μMAX



SO/μMAX



SO



SO

Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply Rail-to-Rail I/O Op Amps

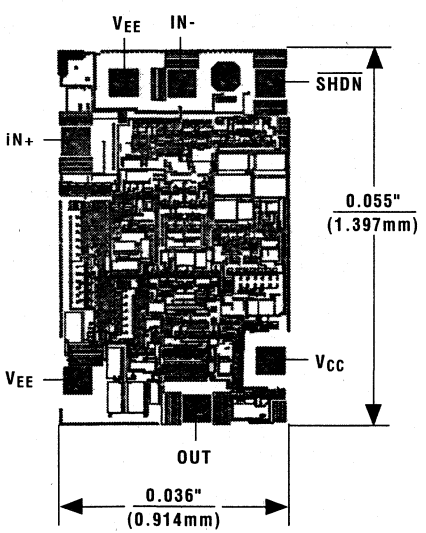
_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	MARKING INFO.
MAX4124EUK	-40°C to +85°C	5 SOT23-5	AABA
MAX4125ESA	-40°C to +85°C	8 SO	—
MAX4125EUA	-40°C to +85°C	8 µMAX	—
MAX4126ESA	-40°C to +85°C	8 SO	—
MAX4126EUA	-40°C to +85°C	8 µMAX	—
MAX4127C/D	0°C to +70°C	Dice*	—
MAX4127ESD	-40°C to +85°C	14 SO	—
MAX4128ESA	-40°C to +85°C	8 SO	—
MAX4128EUA	-40°C to +85°C	8 µMAX	—
MAX4129ESD	-40°C to +85°C	14 SO	—

**Dice are specified at T_A = +25°C, DC parameters only.*

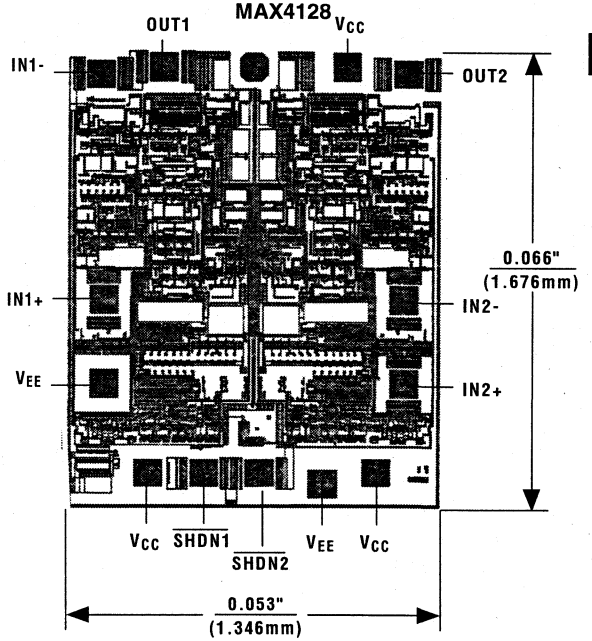
Chip Topographies

MAX4123/ MAX4125



TRANSISTOR COUNT: 170
SUBSTRATE CONNECTED TO V_{EE}

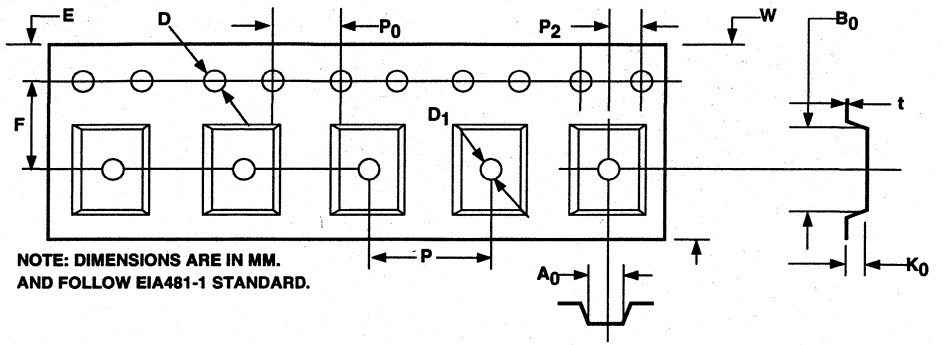
MAX4127/ MAX4128



TRANSISTOR COUNT: 340
SUBSTRATE CONNECTED TO V_{EE}

Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply Rail-to-Rail I/O Op Amps

Tape-and-Reel Information



NOTE: DIMENSIONS ARE IN MM.
AND FOLLOW EIA481-1 STANDARD.

A_0	3.200	±0.102
B_0	3.099	±0.102
D	1.499	+0.102 +0.000
D_1	0.991	+0.254 +0.000

E	1.753	±0.102
F	3.505	±0.051
K_0	1.397	±0.102
P	3.988	±0.102

P_0	3.988	±0.102
$P_0$10	40.005	±0.203
P_2	2.007	±0.051
t	0.254	±0.127
W	8.001	+0.305 -0.102

5 SOT23-5

19-1089; Rev 0; 8/96

MAXIM

Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps

General Description

The MAX4130–MAX4134 family of operational amplifiers combines 10MHz gain-bandwidth product and excellent DC accuracy with rail-to-rail operation at the inputs and outputs. These devices require only 900µA per amplifier, and operate from either a single supply (+2.7V to +6.5V) or dual supplies (±1.35V to ±3.25V) with a common-mode voltage range that extends beyond V_{EE} and V_{CC}. They are capable of driving 250Ω loads and are unity-gain stable. In addition, the MAX4131/MAX4133 feature a shutdown mode in which the outputs are in a high-impedance state and the supply current is reduced to only 25µA per amplifier.

With their rail-to-rail input common-mode range and output swing, the MAX4130–MAX4134 are ideal for low-voltage, single-supply operation. Although the minimum operating voltage is specified at 2.7V, the devices typically operate down to 1.8V. In addition, low offset voltage and high speed make them the ideal signal-conditioning stages for precision, low-voltage data-acquisition systems. **The MAX4130 comes in the space-saving SOT23-5 package.**

Selection Table

PART	AMPS PER PACKAGE	SHUTDOWN MODE	PIN-PACKAGE
MAX4130	1	—	5 SOT23-5
MAX4131	1	Yes	8 SO/µMAX
MAX4132	2	—	8 SO/µMAX
MAX4133	2	Yes	14 SO
MAX4134	4	—	14 SO

Applications

Battery-Powered Instruments

Portable Equipment

Data-Acquisition Systems

Signal Conditioning

Low-Power, Low-Voltage Applications

Pin Configurations appear at end of data sheet.

Features

- ♦ **5-Pin SOT23-5 Package (MAX4130)**
- ♦ **+2.7V to +6.5V Single-Supply Operation**
- ♦ **Rail-to-Rail Input Common-Mode Voltage Range**
- ♦ **Rail-to-Rail Output Voltage Swing**
- ♦ **10MHz Gain-Bandwidth Product**
- ♦ **900µA Quiescent Current per Amplifier**
- ♦ **Optional Shutdown Function (MAX4131/MAX4133)**
- ♦ **200µV Offset Voltage**
- ♦ **No Phase Reversal for Overdriven Inputs**
- ♦ **Drive 250Ω Loads**
- ♦ **Stable with 160pF Capacitive Loads**
- ♦ **Unity-Gain Stable**

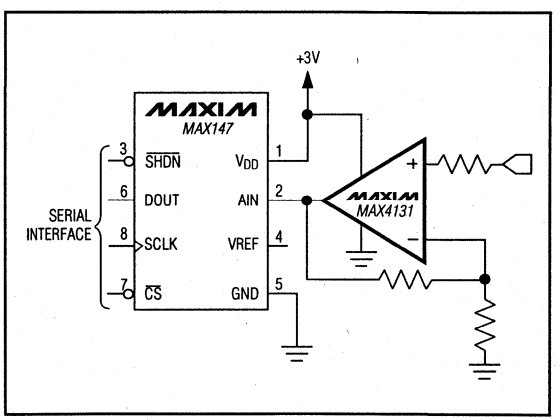
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	MARKING INFO.
MAX4130EUK	-40°C to +85°C	5 SOT23-5	AABB
MAX4131C/D	0°C to +70°C	Dice*	—
MAX4131EUA	-40°C to +85°C	8 µMAX	—
MAX4131ESA	-40°C to +85°C	8 SO	—

Ordering Information continued at end of data sheet.

**Dice are specified at T_A = +25°C, DC parameters only.*

Typical Operating Circuit



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} - V_{EE}) 7.5V
IN+, IN-, $\overline{SHDN}$ Voltage ..... (V_{CC} + 0.3V) to (V_{EE} - 0.3V)
Output Short-Circuit Duration (Note 1) ..... Continuous
(short to either supply)
Continuous Power Dissipation (T_A = +70°C)
5-pin SOT23-5 (derate 7.1mW/°C above +70°C) 571mW
8-pin SO (derate 5.88mW/°C above +70°C) 471mW
8-pin µMAX (derate 4.10mW/°C above +70°C) 330mW
14-pin SO (derate 8.00mW/°C above +70°C) 640mW
Operating Temperature Range
MAX413_E_ _ ..... -40°C to +85°C
Maximum Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: Provided maximum package power-dissipation rating is met.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +6.5V, V_{EE} = 0V, V_{CM} = 0V, V_{OUT} = V_{CC}/2, R_L tied to V_{CC}/2, $\overline{SHDN}$ ≥ 2V or open, T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{CM} = V_{EE} to V_{CC}	MAX4130EUK		±0.35	±1.0	mV
		MAX4131ESA		±0.20	±0.60	
		MAX4131EUA		±0.35	±1.2	
Input Bias Current	V_{CM} = V_{EE} to V_{CC}			±50	±150	nA
Input Offset Current	V_{CM} = V_{EE} to V_{CC}			±1	±12	nA
Differential Input Resistance	-1.5V < V_{DIFF} < 1.5V			500		kΩ
Common-Mode Input Voltage Range			V_{EE} - 0.25		V_{CC} + 0.25	V
Common-Mode Rejection Ratio	(V_{EE} - 0.25V) < V_{CM} < (V_{CC} + 0.25V)	MAX4130EUK	70	90		dB
		MAX4131ESA	78	98		
		MAX4131EUA	68	88		
Power-Supply Rejection Ratio	V_{CC} = 2.7V to 6.5V		78	100		dB
Output Resistance	A_V = 1			0.1		Ω
Off-Leakage Current	$\overline{SHDN}$ < 0.8V, V_{OUT} = 0V to V_{CC}			±0.1	±1	µA
Large-Signal Voltage Gain	V_{CC} = 2.7V	V_{OUT} = 0.25V to 2.45V, R_L = 100kΩ	94	108		dB
		V_{OUT} = 0.4V to 2.3V, R_L = 250Ω	72	82		
	V_{CC} = 5.0V	V_{OUT} = 0.25V to 4.75V, R_L = 100kΩ	96	110		
		V_{OUT} = 0.4V to 4.6V, R_L = 250Ω	76	88		
Output Voltage Swing	R_L = 100kΩ	V_{CC} - V_{OH}		12	20	mV
		V_{OL} - V_{EE}		20	35	
	R_L = 250Ω	V_{CC} - V_{OH}		240	290	
		V_{OL} - V_{EE}		125	170	
Output Short-Circuit Current				50		mA

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.7V to +6.5V, V_{EE} = 0V, V_{CM} = 0V, V_{OUT} = V_{CC}/2, R_L tied to V_{CC}/2, $\overline{SHDN}$ ≥ 2V or open, T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{SHDN}$ Logic Threshold	MAX4131	Low			0.8	V
		High	2.0			
$\overline{SHDN}$ Input Current	MAX4131			±1	±3	µA
Operating Supply-Voltage Range			2.7		6.5	V
Supply Current per Amplifier	V_{CM} = V_{OUT} = V_{CC}/2	V_{CC} = 2.7V		900	1050	µA
		V_{CC} = 5.0V		1000	1150	
Shutdown Supply Current per Amplifier	MAX4131, $\overline{SHDN}$ < 0.8V	V_{CC} = 2.7V		25	40	µA
		V_{CC} = 5.0V		40	60	

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +6.5V, V_{EE} = 0V, V_{CM} = 0V, V_{OUT} = V_{CC}/2, R_L tied to V_{CC}/2, $\overline{SHDN}$ ≥ 2V or open, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{CM} = V_{EE} to V_{CC}	MAX4130EUK			±3.5	mV
		MAX4131ESA			±0.75	
		MAX4131EUA			±4.4	
Input Offset Voltage Tempco				±2		µV/°C
Input Bias Current	V_{CM} = V_{EE} to V_{CC}				±160	nA
Input Offset Current	V_{CM} = V_{EE} to V_{CC}				±18	nA
Common-Mode Input Voltage Range			V_{EE} - 0.20		V_{CC} + 0.20	V
Common-Mode Rejection Ratio	(V_{EE} - 0.2V) < V_{CM} < (V_{CC} + 0.2V)	MAX4131ESA	76			dB
		MAX4130EUK	62			
		MAX4131EUA	60			
Power-Supply Rejection Ratio	V_{CC} = 2.7V to 6.5V		74			dB
Off-Leakage Current	$\overline{SHDN}$ < 0.8V, V_{OUT} = 0V to V_{CC}				±12	µA
Large-Signal Voltage Gain	V_{CC} = 2.7V	V_{OUT} = 0.25V to 2.45V, R_L = 100kΩ	86			dB
		V_{OUT} = 0.4V to 2.3V, R_L = 250Ω	68			
	V_{CC} = 5.0V	V_{OUT} = 0.25V to 4.75V, R_L = 100kΩ	88			
		V_{OUT} = 0.4V to 4.6V, R_L = 250Ω	70			
Output Voltage Swing	R_L = 100kΩ	V_{CC} - V_{OH}			25	mV
		V_{OL} - V_{EE}			40	
	R_L = 250Ω	V_{CC} - V_{OH}			300	
		V_{OL} - V_{EE}			190	

Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.7V to +6.5V, V_{EE} = 0V, V_{CM} = 0V, V_{OUT} = V_{CC}/2, R_L tied to V_{CC}/2, $\overline{SHDN}$ ≥ 2V or open, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{SHDN}$ Logic Threshold	MAX4131	Low			0.8	V
		High	2.0			
$\overline{SHDN}$ Input Current	MAX4131				±3	µA
Operating Supply-Voltage Range			2.7		6.5	V
Supply Current per Amplifier	V_{CM} = V_{OUT} = V_{CC}/2	V_{CC} = 2.7V			1100	µA
		V_{CC} = 5.0V			1200	
Shutdown Supply Current per Amplifier	MAX4131, $\overline{SHDN}$ < 0.8V	V_{CC} = 2.7V			50	µA
		V_{CC} = 5.0V			70	

AC ELECTRICAL CHARACTERISTICS

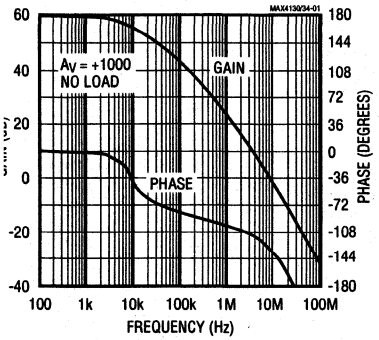
(V_{CC} = +2.7V to +6.5V, V_{EE} = 0V, $\overline{SHDN}$ ≥ 2V or open, T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Gain-Bandwidth Product				10		MHz
Phase Margin				62		degrees
Gain Margin				12		dB
Total Harmonic Distortion	f = 10kHz, V_{OUT} = 2Vp-p (A_V = 1)			0.003		%
Slew Rate				4		V/µs
Settling Time to 0.01%	A_V = 1, V_{OUT} = 2V step			2.0		µs
Turn-On Time	V_{CC} = 0V to 3V step, V_{OUT} = V_{CC}/2			1		µs
$\overline{SHDN}$ Delay	MAX4131, V_{CC} = 3V, V_{OUT} = V_{CC}/2	Enable		1		µs
		Disable		0.2		
Input Capacitance				3		pF
Input Noise Voltage Density	f = 1kHz			22		nV/Hz
Input Noise Current Density	f = 1kHz			0.4		pA/Hz
Capacitive Load Stability	A_V = 1			160		pF

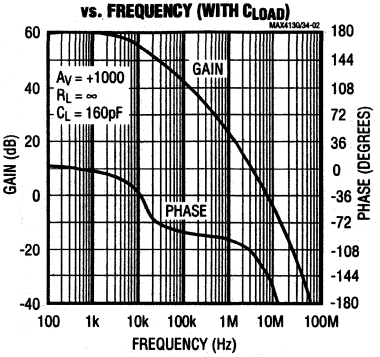
Typical Operating Characteristics

(V_{CC} = +5V, V_{EE} = 0V, V_{CM} = V_{CC}/2, T_A = +25°C, unless otherwise noted.)

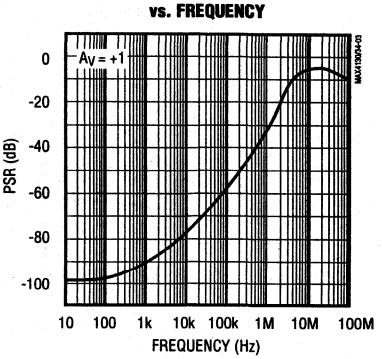
GAIN AND PHASE vs. FREQUENCY



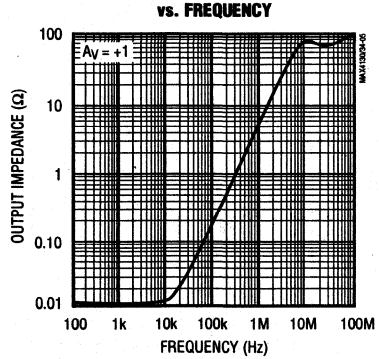
GAIN AND PHASE vs. FREQUENCY (WITH C_{LOAD})



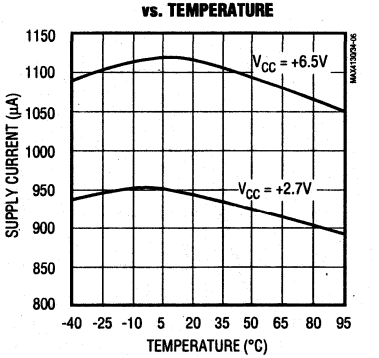
POWER-SUPPLY REJECTION vs. FREQUENCY



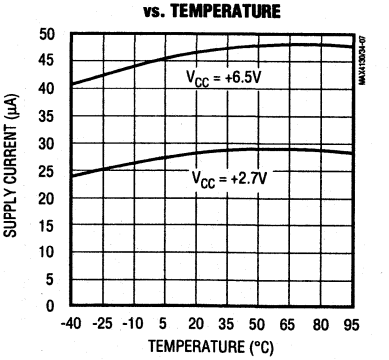
OUTPUT IMPEDANCE vs. FREQUENCY



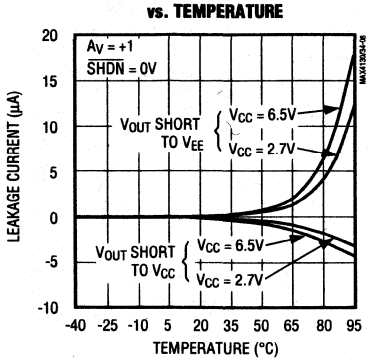
SUPPLY CURRENT PER AMPLIFIER vs. TEMPERATURE



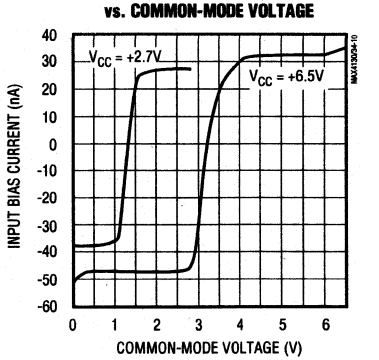
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



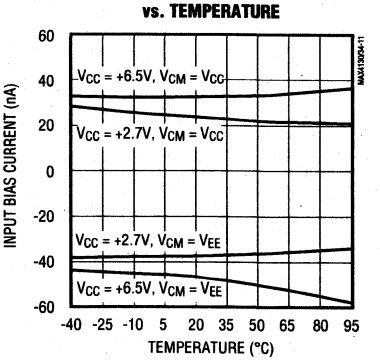
OUTPUT LEAKAGE CURRENT vs. TEMPERATURE



INPUT BIAS CURRENT vs. COMMON-MODE VOLTAGE



INPUT BIAS CURRENT vs. TEMPERATURE

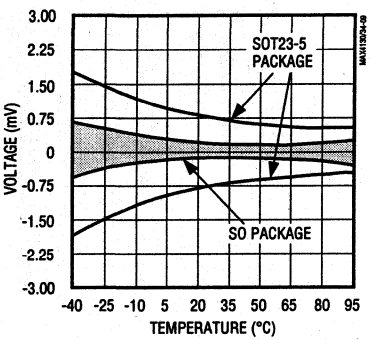


Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps

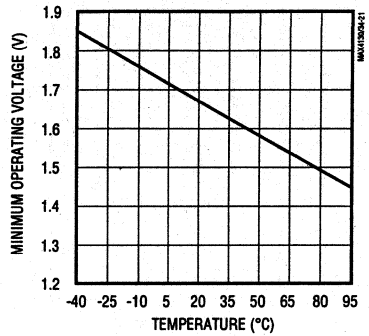
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = 0V, V_{CM} = V_{CC}/2, T_A = +25°C, unless otherwise noted.)

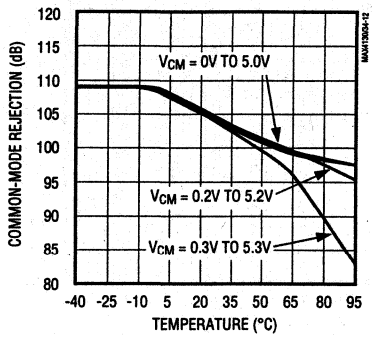
INPUT OFFSET VOLTAGE vs. TEMPERATURE



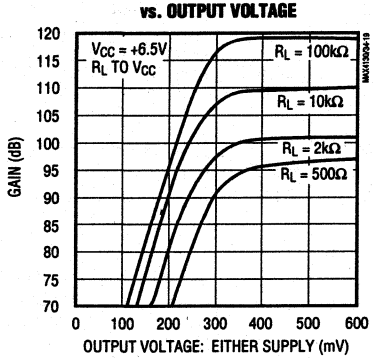
MINIMUM OPERATING VOLTAGE vs. TEMPERATURE



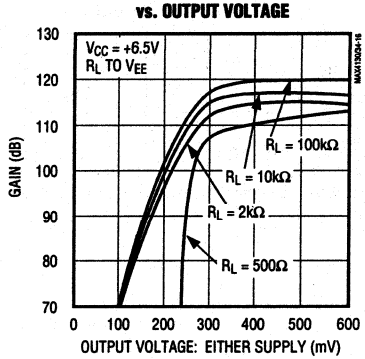
COMMON-MODE REJECTION vs. TEMPERATURE



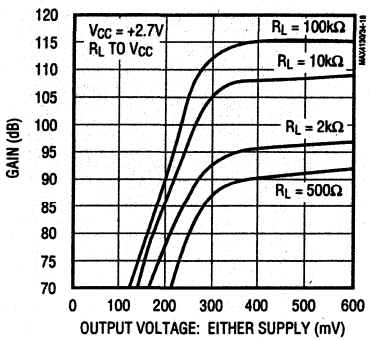
LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE



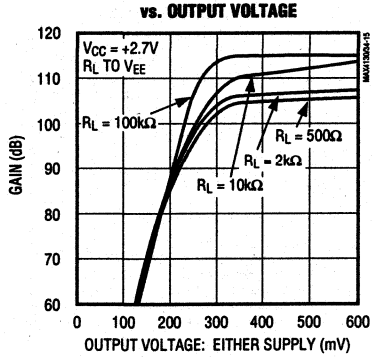
LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE



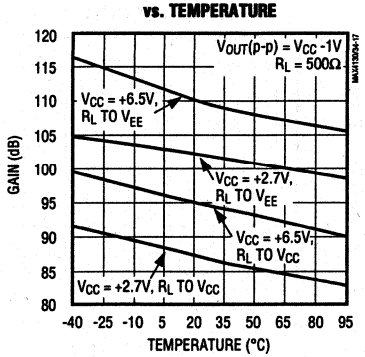
LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE



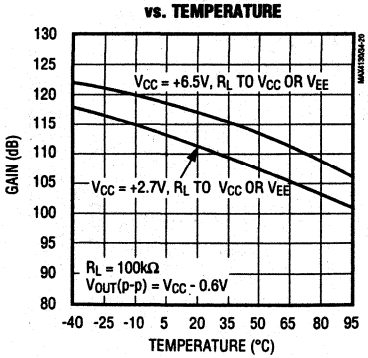
LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE



LARGE-SIGNAL GAIN vs. TEMPERATURE



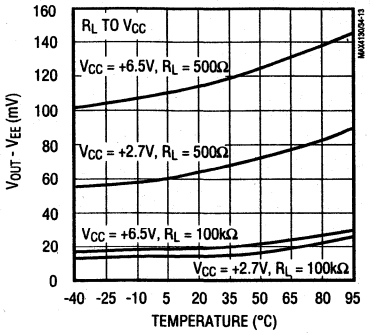
LARGE-SIGNAL GAIN vs. TEMPERATURE



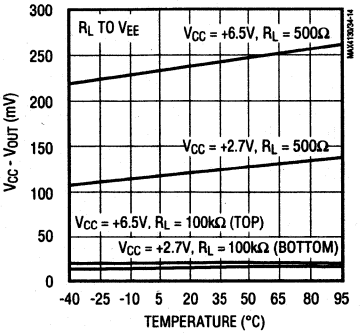
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = 0V, V_{CM} = V_{CC}/2, T_A = +25°C, unless otherwise noted.)

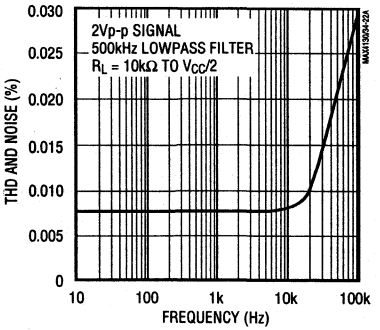
MINIMUM OUTPUT VOLTAGE vs. TEMPERATURE



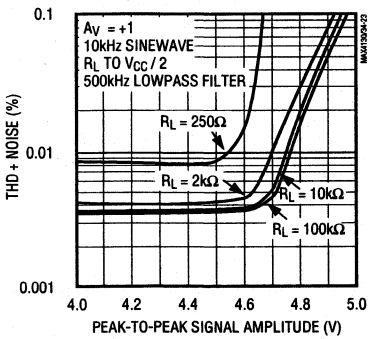
MAXIMUM OUTPUT VOLTAGE vs. TEMPERATURE



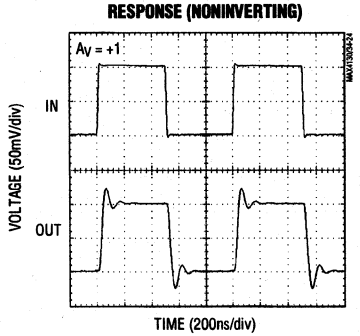
TOTAL HARMONIC DISTORTION AND NOISE vs. FREQUENCY



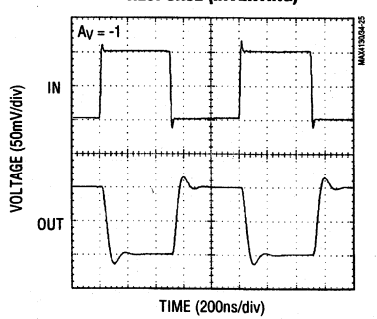
TOTAL HARMONIC DISTORTION AND NOISE vs. PEAK-TO-PEAK SIGNAL AMPLITUDE



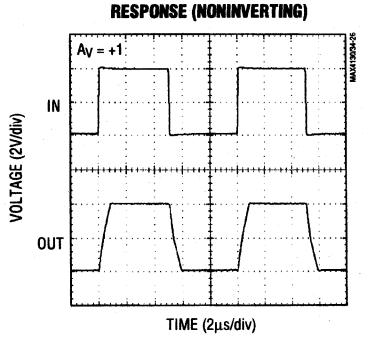
MAX4131 SMALL-SIGNAL TRANSIENT RESPONSE (NONINVERTING)



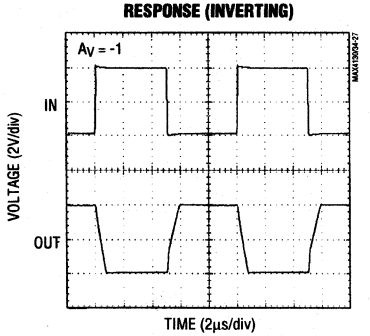
MAX4131 SMALL-SIGNAL TRANSIENT RESPONSE (INVERTING)



MAX4131 LARGE-SIGNAL TRANSIENT RESPONSE (NONINVERTING)



MAX4131 LARGE-SIGNAL TRANSIENT RESPONSE (INVERTING)



Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps

Pin Description

MAX4130	MAX4131	MAX4132	MAX4133	MAX4134	NAME	FUNCTION
1	6	—	—	—	OUT	Output
2	4	4	4	11	V_{EE}	Negative Supply. Ground for single-supply operation.
3	3	—	—	—	IN+	Noninverting Input
4	2	—	—	—	IN-	Inverting Input
5	7	8	14	4	V_{CC}	Positive Supply
—	1, 5	—	5, 7, 8, 10	—	N.C.	No Connect. Not internally connected.
—	8	—	—	—	$\overline{SHDN}$	Shutdown Control. Tie high or leave floating to enable amplifier.
—	—	1, 7	1, 13	1, 7	OUT1, OUT2	Outputs for amps 1 and 2
—	—	2, 6	2, 12	2, 6	IN1-, IN2-	Inverting Inputs for amps 1 and 2
—	—	3, 5	3, 11	3, 5	IN1+, IN2+	Noninverting Inputs for amps 1 and 2
—	—	—	6, 9	—	$\overline{SHDN1}$, $\overline{SHDN2}$	Shutdown Control, independent for amps 1 and 2. Tie high or leave floating to enable amplifier.
—	—	—	—	8, 14	OUT3, OUT4	Outputs for amps 3 and 4
—	—	—	—	9, 13	IN3-, IN4-	Inverting Inputs for amps 3 and 4
—	—	—	—	10, 12	IN3+, IN4+	Noninverting Inputs for amps 3 and 4

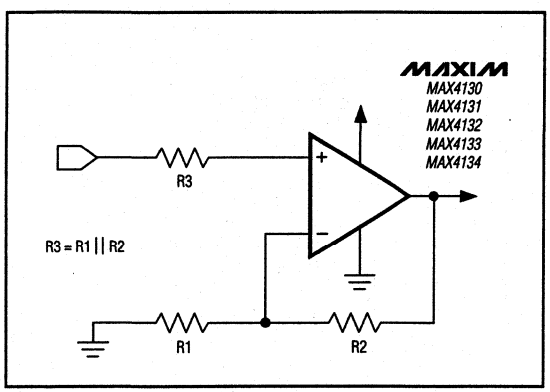


Figure 1a. Reducing Offset Error Due to Bias Current (Noninverting)

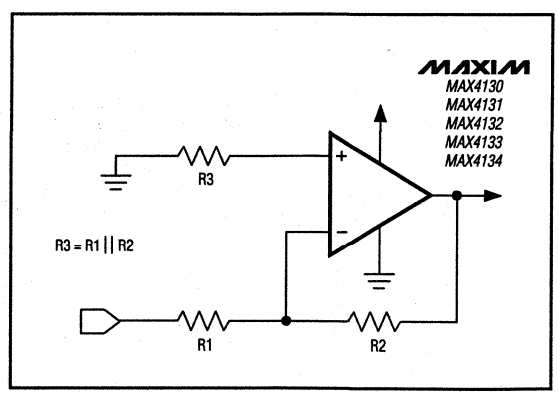


Figure 1b. Reducing Offset Error Due to Bias Current (Inverting)

Applications Information

Rail-to-Rail Input Stage

Devices in the MAX4130–MAX4134 family of high-speed amplifiers have rail-to-rail input and output stages designed for low-voltage, single-supply operation. The input stage consists of separate NPN and PNP differential stages that combine to provide an input common-mode range that extends 0.2V beyond the supply rails. The PNP stage is active for input voltages close to the negative rail, and the NPN stage is active for input voltages near the positive rail. The input offset voltage is typically below 200µV. The switchover transition region, which occurs near $V_{CC}/2$, has been extended to minimize the slight degradation in common-mode rejection ratio caused by the mismatch of the input pairs. Their low offset voltage, high bandwidth, and rail-to-rail common-mode range make these op amps excellent choices for precision, low-voltage data-acquisition systems.

Since the input stage switches between the NPN and PNP pairs, the input bias current changes polarity as the input voltage passes through the transition region. Reduce the offset error caused by input bias currents flowing through external source impedances by matching the effective impedance seen by each input (Figures 1a, 1b). High source impedances, together with input capacitance, can create a parasitic pole that produces an underdamped signal response. Reducing the input impedance or placing a small (2pF to 10pF) capacitor across the feedback resistor improves response.

The MAX4130–MAX4134's inputs are protected from large differential input voltages by 1kΩ series resistors and back-to-back triple diodes across the inputs (Figure 2). For differential input voltages less than 1.8V, input resistance is typically 500kΩ. For differential input voltages greater than 1.8V, input resistance is approximately 2kΩ. The input bias current is given by the following equation:

$$I_{BIAS} = \frac{V_{DIFF} - 1.8V}{2k\Omega}$$

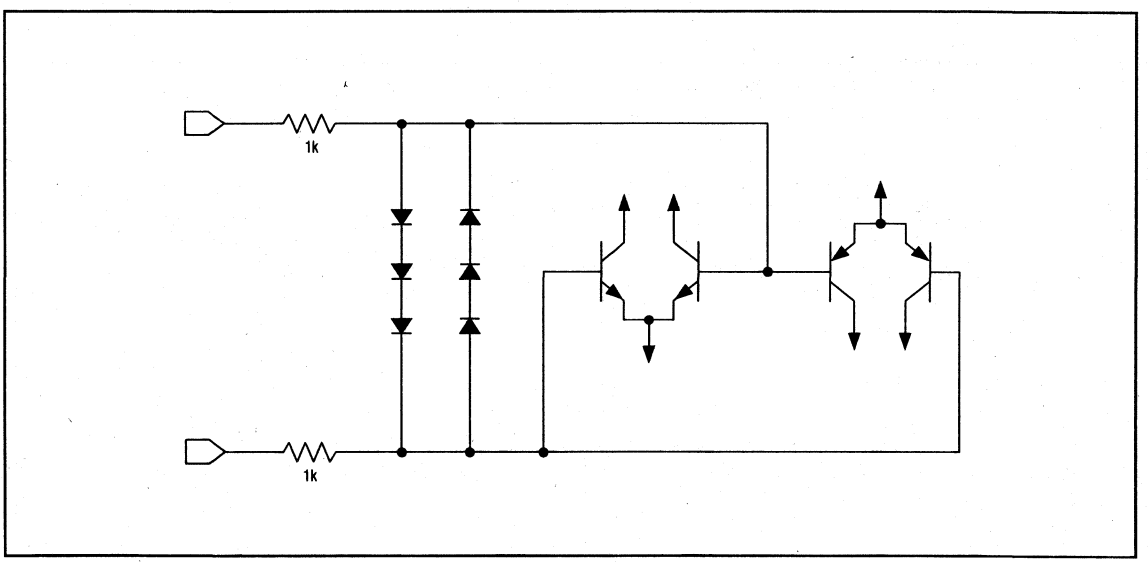


Figure 2. Input Protection Circuit

Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps

Rail-to-Rail Output Stage

The minimum output voltage is within millivolts of ground for single-supply operation where the load is referenced to ground (V_{EE}). Figure 3 shows the input voltage range and output voltage swing of a MAX4131 connected as a voltage follower. With a +3V supply and the load tied to ground, the output swings from 0.00V to 2.90V. The maximum output voltage swing depends on the load, but will be within 150mV of a +3V supply, even with the maximum load (500Ω to ground).

Driving a capacitive load can cause instability in most high-speed op amps, especially those with low quiescent current. The MAX4130–MAX4134 have a high tolerance for capacitive loads. They are stable with capacitive loads up to 160pF. Figure 4 gives the stable operating region for capacitive loads. Figures 5 and 6 show the response with capacitive loads and the results of adding an isolation resistor in series with the output (Figure 7). The resistor improves the circuit's phase margin by isolating the load capacitor from the op amp's output.

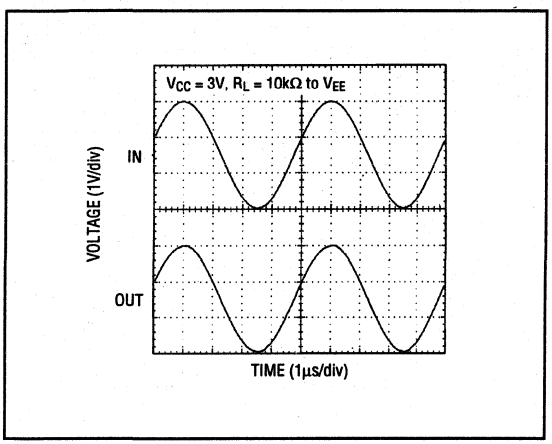


Figure 3. Rail-to-Rail Input/Output Voltage Range

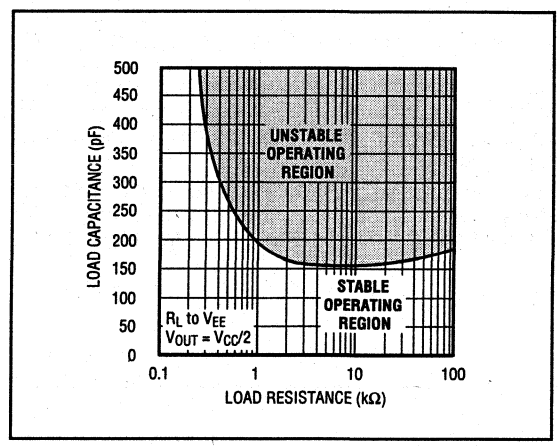


Figure 4. Capacitive-Load Stability

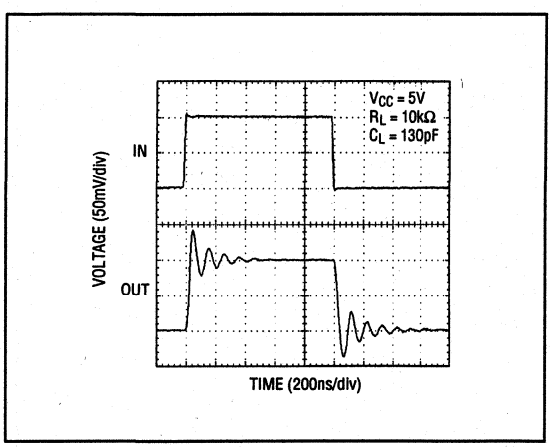


Figure 5. MAX4131 Small-Signal Transient Response with Capacitive Load

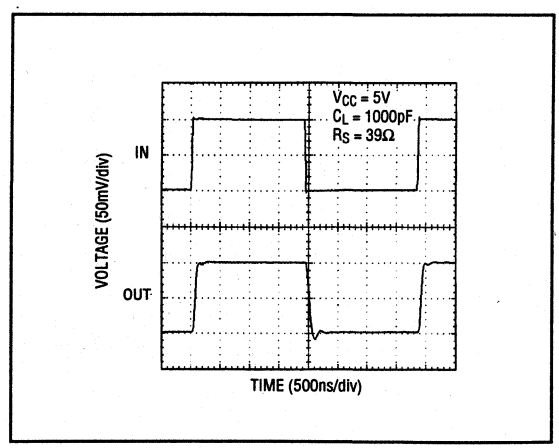


Figure 6. MAX4131 Transient Response to Capacitive Load with Isolation Resistor

Power-Up and Shutdown Mode

The MAX4130–MAX4134 amplifiers typically settle within 1µs after power-up. Figures 9 and 10 show the output voltage and supply current on power-up, using the test circuit of Figure 8.

The MAX4131 and MAX4133 have a shutdown option. When the shutdown pin ($\overline{SHDN}$) is pulled low, the supply current drops below 25µA per amplifier and the amplifiers are disabled with the outputs in a high-impedance state. Pulling $\overline{SHDN}$ high or leaving it floating enables the amplifier. In the dual-amplifier MAX4133, the shutdown functions operate independently. Figures 11 and 12 show the output voltage and supply current responses of the MAX4131 to a shutdown pulse, using the test circuit of Figure 8.

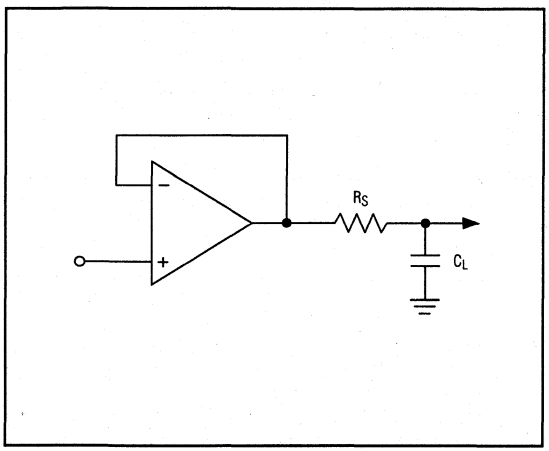


Figure 7. Capacitive-Load Driving Circuit

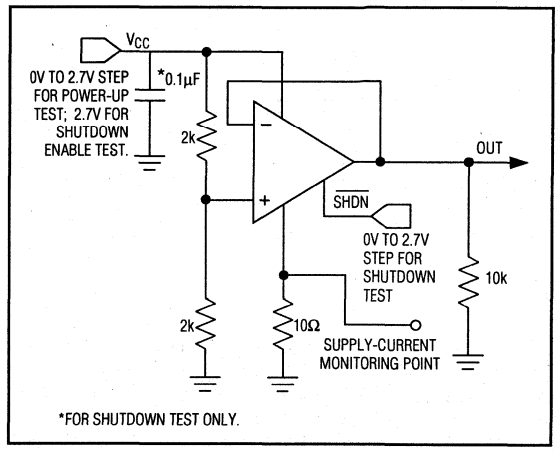


Figure 8. Power-Up/Shutdown Test Circuit

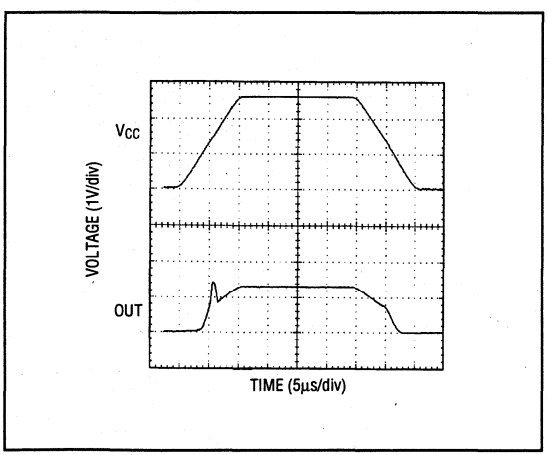


Figure 9. Power-Up Output Voltage

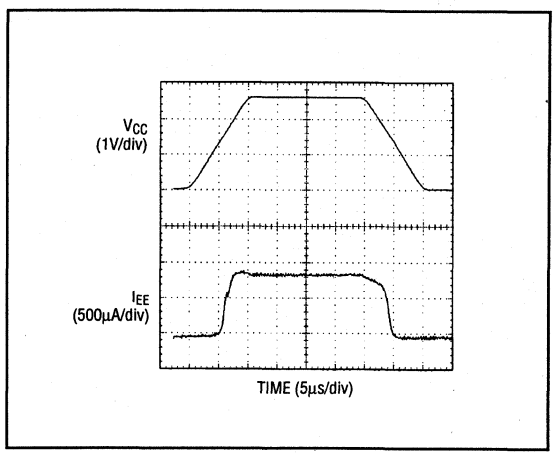


Figure 10. Power-Up Supply Current

Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps

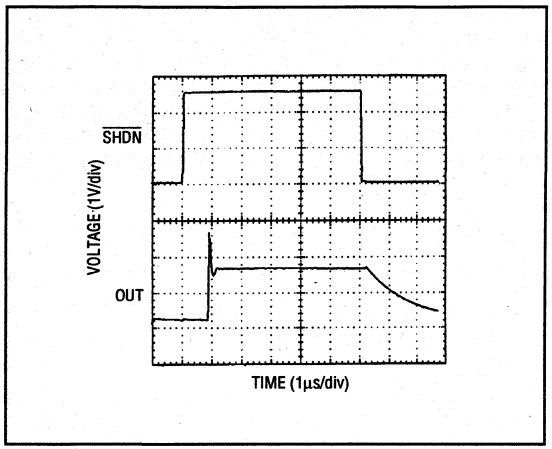


Figure 11. Shutdown Output Voltage

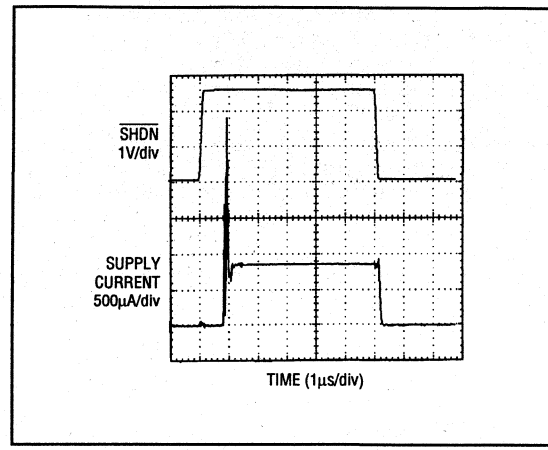


Figure 12. Shutdown Enable/Disable Supply Current

Power Supplies and Layout

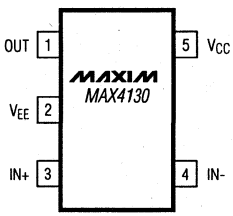
The MAX4130–MAX4134 operate from a single +2.7V to +6.5V power supply, or from dual supplies of ±1.35V to ±3.25V. For single-supply operation, bypass the power supply with a 0.1µF ceramic capacitor in parallel with at least 1µF. For dual supplies, bypass each supply to ground.

Good layout improves performance by decreasing the amount of stray capacitance at the op amp's inputs and outputs. Decrease stray capacitance by placing external components close to the op amp's pins, minimizing trace lengths and resistor leads.

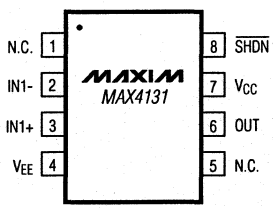
Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps

Pin Configurations

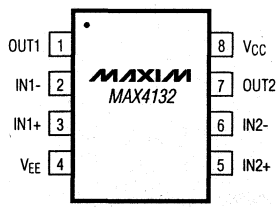
TOP VIEW



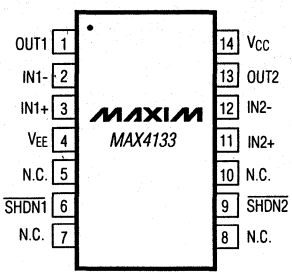
SOT23-5



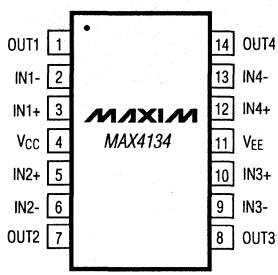
SO/µMAX



SO/µMAX



SO



SO

Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	MARKING INFO.
MAX4132ESA†	-40°C to +85°C	8 SO	—
MAX4132EUA†	-40°C to +85°C	8 µMAX	—
MAX4133C/D†	0°C to +70°C	Dice*	—
MAX4133ESD†	-40°C to +85°C	14 SO	—
MAX4134ESD†	-40°C to +85°C	14 SO	—

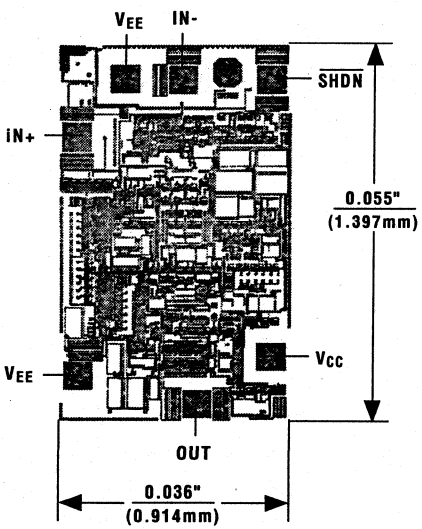
*Dice are specified at T_A = +25°C, DC parameters only.
†Contact factory for availability.

_Chip Information

MAX4130 TRANSISTOR COUNT: 170
MAX4132 TRANSISTOR COUNT: 340
MAX4134 TRANSISTOR COUNT: 680

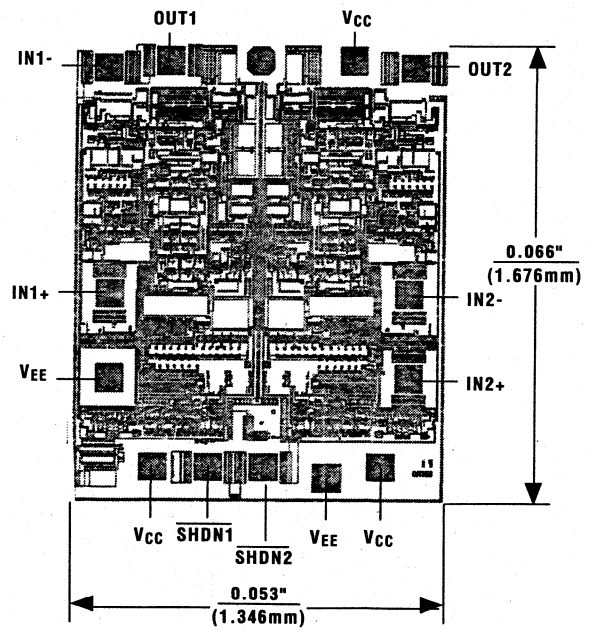
_Chip Topographies

MAX4131



TRANSISTOR COUNT: 170
SUBSTRATE CONNECTED TO V_{EE}

MAX4133



TRANSISTOR COUNT: 340
SUBSTRATE CONNECTED TO V_{EE}

MAXIM

Power-Supply Circuits

Power-Supply Circuits, Product Tables and Trees 4-3

MAX606 Low-Profile, 0.8MHz, Step-Up DC-DC Converter for Type 1 Flash Memory/PCMCIA Cards 4-11
MAX607 Low-Profile, 0.4MHz, Step-Up DC-DC Converter for Type 2 and 3 Flash Memory/ PCMCIA Cards 4-11
MAX608 Low-Input-Voltage, High-Efficiency, Step-Up DC-DC Controller 4-23
MAX710 3V/5V-Output, Step-Up DC-DC Converter 4-35*
MAX711 Adjustable-Output, Step-Up DC-DC Converter 4-35*
MAX798 Step-Down, PWM Controller with Synchronous Rectifier for CPU Power, Adjustable from 5.5V to 1.6V 4-37*
MAX828 Ultra-Small, 25mA Inverting Charge Pumps in SOT23 4-39
MAX829 Ultra-Small, 25mA Inverting Charge Pumps in SOT23 4-39
MAX846A Cost-Saving, Chemistry-Independent Battery-Charger System 4-47
MAX848 1 to 3 Cell, High Power, Low-Noise, Step-Up DC-DC Converter with 0.5A MOSFET Power Switch 4-59
MAX849 1 to 3 Cell, High Power, Low-Noise, Step-Up DC-DC Converter with 1A MOSFET Power Switch 4-59
MAX863 Dual-Output, High-Efficiency, PFM, Step-Up DC-DC Controller 4-75*
MAX864 Dual-Output, Doubling/Inverting Charge-Pump Voltage Converter with Shutdown 4-77
MAX865 Dual-Output, Doubling/Inverting Charge-Pump Voltage Converter in µMAX 4-87
MAX887 Low-Noise, Adjustable-Output, Step-Down DC-DC Converter with Synching Capability 4-95
MAX890L 90mΩ, 1A, Current-Limited Power Switch 4-107
MAX891L 150mΩ, 0.5A, Current-Limited Power Switch 4-115*
MAX892L 300mΩ, 0.25A, Current-Limited Power Switch 4-115*
MAX894L 150mΩ, 0.5A, Dual Current-Limited Power Switch 4-117
MAX895L 300mΩ, 0.25A, Dual Current-Limited Power Switch 4-117
MAX1600 Dual-Channel CardBus and PCMCIA VCC/VPP Power-Switching Network 4-125
MAX1601 Dual-Channel CardBus and PCMCIA Power-Switch with SMBus Serial Interface 4-137
MAX1602 Single-Channel PCMCIA VCC/VPP Power-Switching Network 4-153
MAX1603 Dual-Channel CardBus and PCMCIA VCC/VPP Power-Switching Network 4-125
MAX1604 Dual-Channel CardBus and PCMCIA Power-Switch with SMBus Serial Interface 4-137
MAX1610 Digitally Controlled CCFL Backlight Power Supply 4-165
MAX1611 Digitally Controlled CCFL Backlight Power Supply with SMBus Interface 4-165
MAX1620 Digitally Adjustable LCD Bias Supply 4-185*
MAX1621 Digitally Adjustable LCD Bias Supply with SMBus Interface 4-185*
MAX1624 High-Speed Step-Down Controller with Synchronous Rectification for CPU Power 4-187*
MAX1625 High-Speed Step-Down Controller with Synchronous Rectification for CPU Power 4-187*
MAX1626 100% Duty Cycle, PFM, 5V or 3.3V, Pin-Selectable, Step-Down DC-DC Controller 4-189
MAX1627 100% Duty Cycle, PFM, 1.3V to Input Adjustable, Step-Down DC-DC Controller 4-189
MAX1630 High-Efficiency, 3.3V/5V (or adj.), 12V-Output Controller for Notebooks 4-205
MAX1631 High-Efficiency, 3.3V/5V (or adj.), 12V-Output Controller for Notebooks 4-205

*Advance Information–first page of data sheet in preparation.

Power-Supply Circuits (continued)

MAX1632	High-Efficiency, 3.3V/5V (or adj.), 12V-Output Controller for Notebooks	4-205
MAX1633	High-Efficiency, 3.3V/5V (or adj.), 12V-Output Controller for Notebooks	4-205
MAX1634	High-Efficiency, 3.3V/5V (or adj.), 12V-Output Controller for Notebooks	4-205
MAX1635	High-Efficiency, 3.3V/5V (or adj.), 12V-Output Controller for Notebooks	4-205
MAX1640	PWM Current Source with High-Side Sense	4-233*
MAX1641	PWM Current Source with Low-Side Sense	4-233*
MAX1642	1-Cell, High-Efficiency, Step-Up DC-DC Converter with Shutdown	4-235*
MAX1643	1-Cell, High-Efficiency, Step-Up DC-DC Converter with 2 LBI/LBOs	4-235*
MAX1647	Chemistry-Independent Battery Charger with SMBus Serial Interface	4-237*
MAX1648	Chemistry-Independent Battery Charger	4-237*
MAX8862	Low-Cost, Low-Dropout, Dual Linear Regulator	4-239
MAX8863	Low-Noise 50mA LDO Linear Regulator in SOT23	4-251
MAX8864	Low-Noise 50mA LDO Linear Regulator in SOT23 with C_{OUT} Discharge	4-251
MAX8865	Dual, Low-Dropout, 100mA Linear Regulator	4-261
MAX8866	Dual, Low-Dropout, 100mA Linear Regulator with Auto-Discharge	4-261

*Advance Information–first page of data sheet in preparation.

Power Management

Multi-Function Supplies

1-Cell Portables

† ☆ MAX848
(2.7V to 5V step-up, with A/D battery monitoring, 200mA, 3.3V out)

★☆ MAX849
(2.7V to 5V step-up, with A/D battery monitoring, 200mA, 3.3V out)

2- or 3-Cell Portables

MAX687
(3V and 3.3V LDO linear reg.)

☆ MAX688
(3V and 3.3V LDO linear reg.)

☆ MAX689
(3V and 3.3V LDO linear reg.)

☆ MAX717
(3.3V & 12V flash prog.)

☆ MAX718
(3.3V or 5V & 12V flash prog.)

☆ MAX719
(3V or 5V & 12V flash prog.)

MAX720
(3.3V or 5V & 12V flash prog.)

MAX721
(3V or 5V & 12V flash prog.)

☆ MAX722
(3.3V or 5V_{OUT}, neg. LCD)

☆ MAX723
(3V or 5V_{OUT}, neg. LCD)

† ☆ MAX848
(600mA, 5V out)

★☆ MAX849
(600mA, 5V out)

† ☆ MAX863
(dual PFM boost controller in small package)

5- to 12-Cell Portables/ Notebooks

† ☆ MAX1630-1635
(3.3V, 5V, 12V)

MAX781
(3.3V, battery charger, PCMCIA)

☆ MAX782
(3.3V, 5V, PCMCIA)

☆ MAX783
(3.3V, 5V, PCMCIA, optimized for 6-cell inputs)

☆ MAX786
(3.3V, 5V)

3V & 5V PCMCIA Card & Hosts

★ MAX1600/1603
(dual card-slot power network with internal switches)

★ MAX1601/1604
(dual card-slot power network with internal switches & SMBus serial interface)

★ MAX1602
(single card-slot power network with internal switches)

MAX613
(PCMCIA controller, dual V_{PP})

MAX614
(PCMCIA controller, single V_{PP})

MAX624
(dual output (5V & adj.), 1MHz switcher)

MAX780
(PCMCIA controller, 4 level translators, dual V_{PP}, power ready)

Isolated Power

☆ MAX845
(750mW isolated transformer driver)

High-Side MOSFET Drivers

MAX620 (quad driver)

MAX622
(V_{OUT} = V_{IN} + 11V)

Current-Limited Power Switches

★ MAX890L
(90mΩ, 1A, 8-SO)

† MAX891L/892L
(150/300mΩ, 500/250mA, 8-µMAX)

★ MAX894L/895L
(dual, 150/300mΩ, 500/250mA, 8-SO)

Battery Chargers

† ☆ MAX1640/1641
(PWM current source)

† ☆ MAX1647
(SBS level 2 smart charger: Li+, NiMH, NiCd)

† ☆ MAX1648
(precision switch-mode universal charger: Li+, NiMH, NiCd)

☆ MAX2003
(NiCd/NiMH, temp. slope detection)

☆ MAX2003A
(improved MAX2003)

MAX471/472
(current-sense amp, fuel gauge)
(see Op Amp table)

☆ MAX712
(NiCd/NiMH, zero voltage-slope detection)

☆ MAX713
(NiCd/NiMH, negative voltage-slope detection)

★☆ MAX846A
(cost-saving system for Li+, NiMH, NiCd)

Low-Side MOSFET Drivers

MAX4420
(6A, 1.5Ω, single noninverting)

MAX4426
(1.5A, 4Ω, dual inverting)

MAX4427
(1.5A, 4Ω, dual noninverting)

MAX4428
(1.5A, 4Ω, dual mixed)

MAX4429
(6A, 1.5Ω, single inverting)

MAX626
(2A, 4Ω, dual inverting)

MAX627
(2A, 4Ω, dual noninverting)

MAX628
(2A, 4Ω, dual mixed)

ICL7667
(1.5A, 4Ω, dual inverting)

TSC426
(1.5A, 6Ω, dual inverting)

TSC427
(1.5A, 6Ω, dual noninverting)

TSC428
(1.5A, 6Ω, dual mixed)

★ New product
† Future product
☆ Evaluation kit available

DC-DC Converters

Low-Dropout Linear Regulators

Positive

MAX603/604
(5V/3.3V or adj., 500mA, 1.8W 8-pin SO)

MAX663
(5V or adj., I_Q = 6µA)

MAX666
(5V or adj., I_Q = 6µA, low-battery detect)

MAX667
(5V or adj., I_Q = 20µA, 120mV dropout, 200mA, low-battery detect)

MAX687
(3.3V ±3%, 0.073V dropout at 500mA, 0.80V dropout at 4A)

☆ MAX688/689
(3.3V/3V ±3%, 0.073V dropout at 500mA, 0.80V dropout at 4A)

MAX882
(3.3V or adj., P-Ch, 200mA, low-battery detector, 1.5W 8-pin SO)

MAX883/884
(5V/3.3V or adj., P-Ch, 200mA, low-battery detector, 1.5W 8-pin SO, 1mA OFF mode)

ICL7663A (adj., 40mA)

★ MAX8862
(Dual 250mA/100mA low-noise LDO)

★ MAX8863/8864
(100mA low-noise LDO in SOT23)

★ MAX8865/8866
(Dual 100mA low-noise LDO in µMAX)

Negative

MAX664
(-5V or adj., I_Q = 6µA)

ICL7664A (±1%V_{OUT})

ICL7664B
(±5% V_{OUT})

Switching Regulators

Step-Up

PWM

☆ MAX731 (2V_{IN} to 5V_{OUT})

☆ MAX732/733/752 (12V/5V/adj.)

☆ MAX734 (12V, flash prog.)

† ☆ MAX848 (1-3 cells to 2.7V–5V, 200mA)

★ ☆ MAX849 (1-3 cells to 2.7V–5V, 100mA)

PFM

† ☆ MAX1642/1643 (0.85V_{IN} start-up with synchronous rectifier)

☆ MAX1771 (12V or adj. controller)

MAX4193 (adj.)

☆ MAX606/607 (5V or 12V or adj., 8-pin µMAX, for PCMCIA, 1MHz)

☆ MAX608 (5V or adj. controller, 2V_{IN}, 300kHz)

MAX630 (adj.)

MAX631/632/633 (5V/12V/15V or adj.)

MAX641/642/643 (5V/12V/15V or adj. controller)

☆ MAX756/757 (3.3V or 5V/adj., 1.8V_{IN}, 250mA)

☆ MAX761 (12V, 120mA, flash prog.)

☆ MAX762 (15V or adj.)

☆ MAX770/771/772 (5V/12V/15V or adj., controller)

MAX773 (5V, 12V, 15V, or adj., controller)

☆ MAX777L/778L/779L (5V/3.3V or 3V/adj., 1V start-up)

☆ MAX856/857 (3.3V or 5V/adj., 1.8V_{IN}, 150mA)

☆ MAX858/859 (3.3V or 5V/adj., 1.8V_{IN}, 35mA)

† ☆ **MAX863** (dual high-efficiency controllers, 1.8V_{IN})

☆ MAX866/867 (3.3V or 5V/adj., 0.9V_{IN}, 90mA)

Inverting

PFM

MAX634 (adj.)

MAX635/636/637 (-5V/-12V/-15V or adj.)

MAX749 (digital adj.)

☆ MAX764/765/766 (-5V/-12V/-15V or adj.)

☆ MAX774/775/776 (-5V/-12V/-15V or adj. ☆ controller)

PWM

MAX735/755 (-5V/adj., max ΔV = 11.7V)

☆ MAX736/737/739/759
(-12V/-15V/-5V/adj., max ΔV = 22V)

Step-Down

PWM

† ☆ MAX1624
(2.1V–3.5V, Pentium Pro™ VID, adjustable synchronous rectifier)

† ☆ MAX1625
1.1–3.5V, adjustable synchronous rectifier)

† ☆ MAX1630-1635
(3.3V, 5V, 12V)

† ☆ MAX1640/1641
(current-source)

MAX724 (adj., 5A)

MAX726/727/728/729
(adj./5V/3.3V/3V, 2A)

☆ MAX730A (5V)

☆ MAX738A (5V)

☆ MAX744A (5V, optimized for cellular comm.)

☆ MAX748A (3.3V)

☆ MAX750A (adj.)

☆ MAX758A (adj.)

☆ MAX763A (3.3V)

☆ MAX767 (3.3V)

☆ MAX781
(3.3V, battery charger, PCMCIA)

☆ MAX782
(3.3V & 5V, PCMCIA)

☆ MAX783
(3.3V & 5V, PCMCIA for 6-cell inputs)

☆ MAX786 (3.3V & 5V)

MAX787/788/789
(5V/3.3V/3V, 5A)

☆ MAX796/797/799
(5V, 3.3V, 2.9V, or adj. controllers)

† ☆ MAX798
(adj. to 1.6V)

☆ MAX830/831
(adj./5V, 1A, 16-pin SOIC)

☆ MAX832/833
(3.3V/3V, 1A, 16-pin SOIC)

★ ☆ MAX887
(3.3V/adj, 500mA, synchronous rectifier)

PFM

★ ☆ MAX1626/1627
(3.3V or 5V/adj., 100% duty cycle)

☆ MAX1649/1651
(5V/3.3V or adj. controller)

MAX638 (5V or adj.)

☆ MAX639/640/653
(5V/3.3V/3V or adj., >90% efficiency)

DISPLAY

★ ☆ MAX1610 (CCFL with digital adj.)

★ ☆ MAX1611 (CCFL with SMBus digital adj.)

† ☆ MAX1620 (LCD bias supply with digital adj.)

† ☆ MAX1621 (LCD bias supply with SMBus digital adj.)

DUAL-OUTPUT PWM

☆ MAX742 (±12V or ±15V controller)

☆ MAX743 (±12V or ±15V)

Step-Up/Down

† ☆ MAX710/711
(250mA, step-up + linear)

☆ MAX761 (200mA, SEPIC)

☆ MAX877L/878L/879L (5V/3V or 3.3V/adj., can start output from 1V to 6.2V input)

Charge Pumps

-V_{IN} or (2 x V_{IN})

MAX1044
(60kHz osc. freq. boost)

MAX660
(100mA, V_{IN} up to 5V)

MAX665
(100mA, V_{IN} up to 8V)

MAX828/829
(25mA in SOT-23)

MAX860/861
(50mA, V_{IN} up to 5.5V, 250kHz osc. freq.)

ICL7660
(µMAX, V_{IN} up to 10V)

ICL7662
(V_{IN} up to 20V)

SI7661
(V_{IN} up to 20V)

-V_{IN} and (2 x V_{IN})

★ MAX864
(5kHz to 200kHz, 1µF caps, shutdown)

★ MAX865
(30kHz, µMAX package)

12V, 30mA

☆ MAX662A
(programs flash memories, "E" temp. range)

5V, 50mA

☆ MAX619

Regulated GaAsFET Bias Supply

☆ MAX850/851/852/853
(4.5V_{IN}, low-noise, neg. GaAsFET bias)

-2V/Adj., 4mA

☆ MAX840/843/844
(2.5V_{IN}, low-noise, neg. GaAsFET bias)

★ New product
† Future product
☆ Evaluation kit available

Part Number	Input Voltage Range (V)	Output Voltage (V)	Quiescent Supply Current (mA), max(typ)	Output (mA)	Control Scheme	Pins-Package Options*	Temp. Ranges**	EV Kit	Features	Price† 1000-up ($)
STEP-UP SWITCHING REGULATORS										
MAX606/607	3 to 5.5	5 or 12 or adj.	0.5(0.25)/0.3(0.15)	200	PFM	8-µMAX	E	Yes	1MHz switching frequency fits Type 1 PCMCIA cards	3.25
MAX608	1.8 to 16.5	5 or adj.	0.11(0.085)	1A	PFM	8-DIP, 8-SO	E	Yes	Same as MAX1771, but accepts low input voltages	1.89
MAX624	3 to 5.5	5 & 12 or adj.	0.6(0.3)	200 @ 5V 80 @ 12V	PFM	16-NSO	I		1.2MHz switching frequency fits Type 1 PCMCIA cards	5.25
MAX630	2 to 16.5	Adj.	0.125(0.070)	30mW	PFM	8-DIP, 8-SO	C,E,M		Improved RC4123 second source	2.88
MAX631/632/633	1.5 to 5.6/ 12.6/15.6	5/12/15 or adj.	0.4(0.135)/ 2(0.5)/2.5(0.75)	40/25/20	PFM	8-DIP, 8-SO	C,E,M		Only two external components	2.56
MAX641/642/643	1.5 to 5.6/ 12.6/15.6	5/12/15 or adj.	0.4(0.135)/ 2(0.5)/2.5(0.75)	300/550/ 325	PFM	8-DIP, 8-SO	C,E,M		PFM controller	2.87
MAX731	1.8 to 5.25	5	4(2)	200	PWM	8-DIP, 16-WSO	C,E,M	Yes		2.60
MAX732	4 to 9.3	12	3(1.7)	200	PWM	8-DIP, 16-WSO	C,E,M	Yes		2.76
MAX733	4 to 11	15	3(1.7)	125	PWM	8-DIP, 16-WSO	C,E,M	Yes		2.60
MAX734	1.9 to 12	12	2.5(1.2)	120	PWM	8-DIP, 8-SO	C,E,M	Yes	12V flash memory, hot insert	2.23
MAX752	1.8 to 16	Adj.	3(1.7)	2.4W	PWM	8-DIP, 8-SO	C,E,M	Yes		2.94
MAX756/757	1.1 to 5.5	(3.3 or 5)/adj.	0.060(0.045)	250	PFM	8-DIP, 8-SO	C,E	Yes	Best combination of low I_Q & high 86% efficiency	1.95
MAX761/762	2 to 16.5	12/15 or adj. to 16.5	0.1(0.080)	120	PFM	8-DIP, 8-SO	C,E,M	Yes	12V flash memory, lowest I_Q, 1.8V/3V/5V inputs	2.23
MAX770/771/772	2 to 16.5	5/12/15 or adj.	0.1(0.085)	1A	PFM	8-DIP, 8-SO	C,E,M	Yes	Controllers, high efficiency over wide I_{OUT} range	1.80
MAX1771	2 to 16.5	12 or adj.	0.1(0.085)	1A	PFM	8-DIP, 8-SO	C,E,M	Yes	Same as MAX771, but with single 100mV current-sense limit	1.80
MAX773	3 to 16.5	Adj.	0.1(0.085)	1A	PFM	14-DIP, 14-NSO	C,E,M		Controller, high-voltage applications	1.80
MAX777L/778L/779L	1 to 4.5	5/(3 or 3.3)/adj.	0.310(0.220)	300	PFM	8-DIP, 8-SO	C,E,M	Yes	On-chip active diode, true turn-off in shutdown	2.65
MAX848/849	0.7 to 5.5	3.3 or 2.7 to 5	0.06	100 to 600	PWM	16-NSO	E	Yes	1-3 cell step-up, low-noise, fixed-frequency PWM	††/2.38
MAX856/857	0.5 to 6	(3.3 or 5)/adj.	0.060(0.025)	100	PFM	8-SO, 8-µMAX	C,E	Yes	Smallest, best combination of low I_Q & high 85% efficiency	1.72
MAX858/859	0.5 to 6	(3.3 or 5)/adj	0.060(0.025)	25	PFM	8-SO, 8-µMAX	C,E	Yes	Smallest, best combination of low I_Q & high efficiency	1.72
MAX863	1.5 to 11	2 pos. adj.	65(40)	1A	PFM	16-QSOP	E	Yes	Lowest I_Q, high efficiency	††
MAX866/867	0.5 to 6	(3.3 or 5)/adj.	0.06(0.027)	90	PFM	8-SO	E	Yes	Guaranteed 0.9V start-up, low I_Q	1.76
MAX1642/1643	0.7 to 5.5	3.3 or adj.	16(10)	90	PFM	8-µMAX	E	Yes	High efficiency, synchronous rectifier, dual LBI/LBO	††
STEP-UP/DOWN SWITCHING REGULATORS										
MAX710/711	1.8 to 11	3.3 or 5/adj.(2.7 to 5)	0.1(0.08)	250	PFM	16-NSO	E	Yes	No transformer, step-up and linear	††
MAX761	2.7 to 12	Adj. (1.5 to 6)	0.1(0.08)	200	PFM	8-DIP, 8-SO	C,E,M		No transformer, SEPIC	2.23
MAX877L/878L/879L	1 to 4.5	5/(3.3 or 3)/adj.	0.310(0.220)	240	PFM	8-DIP, 8-SO	C,E,M	Yes	Gives regulated output when input above and below the output, no transformer	2.95
STEP-DOWN SWITCHING REGULATORS										
MAX638	2.6 to 16.5	5, adj.	0.6(0.135)	75	PFM	8-DIP, 8-SO	C,E,M			2.56
MAX639/640/653	4 to 11.5	5/3.3/3 or adj.	0.02(0.01)	225	PFM	8-DIP, 8-SO	C,E,M	Yes	Ultra-low I_Q	2.96
MAX1649/1651	3 to 16	5/3.3 or adj.	0.1(0.080)	2A	PFM	8-DIP, 8-SO	C,E	Yes	Drives external P-channel FET, low I_Q, but with 96.5% duty cycle and single 100mV current-sense limit	1.60
MAX1626/1627	3 to 16.5	3.3 or 5/adj.	0.080(0.060)	2A	PFM	8-SO	E	Yes	Same as MAX1651, but with 100% duty cycle, high efficiency, and controller	1.88
MAX724	0 to 60	Adj.	11(8.5)	5A	PWM	7-TO220	C,E			4.52
MAX726	0 to 40	Adj.	11(8.5)	2A	PWM	7-TO220	C,E			3.00
MAX727/728/729	0 to 40	5/3.3/3	11(8.5)	2A	PWM	7-TO220	C,E			3.00
MAX730A	5.2 to 11	5	3(1.7)	300	PWM	8-DIP, 8-SO	C,E,M	Yes	No subharmonic switching noise	2.15
MAX738A	6 to 16	5	3(1.7)	750	PWM	8-DIP, 16-WSO	C,E,M	Yes	No subharmonic switching noise	2.60

* Package Options: DIP = Dual-In-Line Package, SO = Small Outline (N = Narrow, W = Wide), SSOP = Shrink Small-Outline Package, µMAX = Micro Max, TO-__ = Can

** Temperature Ranges: C = 0°C to +70°C, E = -40°C to +85°C, I = -25°C to +85°C, M = -55°C to +125°C

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchanges.

†† Future product—contact factory for pricing and availability. Specifications are preliminary.

Part Number	Input Voltage Range (V)	Output Voltage (V)	Quiescent Supply Current (mA), max(typ)	Output (mA)	Control Scheme	Pins-Package Options*	Temp. Ranges**	EV Kit	Features	Price† 1000-up ($)
MAX744A	4.75 to 16	5	2.5(1.2)	750	PWM	8-DIP, 16-WSO	C,E,M	Yes	Optimized for cellular communications, no subharmonic switching noise	2.90
MAX748A	3.3 to 16	3.3	3(1.7)	750	PWM	8-DIP, 16-WSO	C,E,M	Yes	No subharmonic switching noise	2.60
MAX750A	4 to 11	Adj.	3(1.7)	1.5W	PWM	8-DIP, 8-SO	C,E,M	Yes	No subharmonic switching noise	2.15
MAX758A	4 to 16	Adj.	3(1.7)	3.75W	PWM	8-DIP, 16-WSO	C,E,M	Yes	No subharmonic switching noise	2.60
MAX763A	3.3 to 11	3.3	2.5(1.4)	500	PWM	8-DIP, 8-SO	C,E,M	Yes	No subharmonic switching noise	2.15
MAX1640/1641	5.5 to 30	6 to 30	4(2)	50W	PWM	16-QSOP	E	Yes	High-efficiency current-source, synchronous rectifier	††
MAX767	4.5 to 5.5	3.3, 3.45 (R), or 3.6 (S)	0.75	1.5A to 10A	PWM	20-SSOP	C,E	Yes	Dedicated 5V-to-3.3V, high-efficiency, small size	3.40
MAX787/788/789	0 to 60	5/3.3/3	11(8.5)	5A	PWM	7-TO220	C,E			4.52
MAX796/797/799	4.5 to 30	5.05/3.3/2.9/adj.	1(0.7)	50W	PWM	16-DIP, 16-NSO	C,E,M	Yes	Synchronous rectifier, secondary output regulation, high efficiency over full I_{OUT} range	3.65
MAX798	4.5 to 30	1.6/adj.	1(0.7)	50W	PWM	16-NSO	E		Synchronous rectifier, secondary output regulation, high efficiency over full I_{OUT} range	††
MAX830/831	0 to 30	Adj./5	–	1A	PWM	16-SO	C	Yes	Small package	3.99
MAX832/833	0 to 30	3.3/3	–	1A	PWM	16-SO	C	Yes	Small package	3.99
MAX887	4 to 11	Adj.(1.27 to 9)	0.5(0.2)	500mA	PFM/PWM	8-SO	E	Yes	Internal synchronous rectifier, high efficiency, synchronizable	2.44
MAX1624	4.5 to 5.5	1.1 to 3.5	0.3	to 20A	PWM	24-SSOP	E	Yes	High accuracy Pentium Pro™ VID programming, synchronous rectifier, power-good output	††
MAX1625	4.5 to 5.5	1.1 to 3.5	0.3	to 20A	PWM	16-SO	E	Yes	High accuracy, synchronous rectifier, power-good output	††
INVERTING SWITCHING REGULATORS										
MAX735	4 to 6.2	-5	3(1.6)	275	PWM	8-DIP, 8-SO	C,E,M		>80% efficiencies	2.15
MAX736	4 to 8.6	-12	3(1.6)	125	PWM	14-DIP, 16-WSO	C,E,M	Yes	>80% efficiencies	2.75
MAX737	4 to 5.5	-15	4.5(2.5)	100	PWM	14-DIP, 16-WSO	C,E,M	Yes	>80% efficiencies	2.75
MAX739	4 to 15	-5	3(1.6)	500	PWM	14-DIP, 16-WSO	C,E,M	Yes	>80% efficiencies	2.75
MAX749	2 to 6	Digital adj.	0.06	5W	PFM	8-DIP, 8-SO	C,E,M	Yes	Digital adjust for negative LCD	2.49
MAX755	2.7 to 9	Adj.	3.5(1.8)	1.4W	PWM	8-DIP, 8-SO	C,E,M		>80% efficiencies	2.15
MAX759	4 to 15	Adj.	4(2.1)	1.5W	PWM	14-DIP, 16-WSO	C,E,M	Yes	LCD driver, >80% efficiencies	2.75
MAX764/765/766	3 to 16.5	-5/-12/-15 or adj. to 21ΔV	0.1	200	PFM	8-DIP, 8-SO	C,E,M	Yes	Lowest I_Q	2.38
MAX774/775/776	3 to 16.5	-5/-12/-15 or adj.	0.1	1A	PFM	8-DIP, 8-SO	C,E,M	Yes	Controllers, high efficiency over wide I_{OUT} range	2.20
DUAL-OUTPUT SWITCHING REGULATORS										
MAX624	3 to 5.5	5 & 12 or adj.	0.6(0.3)	200 @ 5V 80 @ 12V	PFM	16-NSO	I		1.2MHz switching frequency fits Type 1 PCMCIA cards	5.25
MAX742	4.2 to 10	±12, ±15	15(8)	±15W	PWM	20-DIP, 20-WSO	C,E,M	Yes	Drives external MOSFETs	3.91
MAX743	4.2 to 6	±12, ±15	30(20)	±1.5W	PWM	16-DIP, 16-WSO	C,E,M	Yes	Internal power MOSFETs	4.49
MAX863	1.5 to 11	2 pos. adj.	65(40)	1A	PFM	16-QSOP	E	Yes	Lowest I_Q, high efficiency	††

* Package Options: DIP = Dual-In-Line Package, SO = Small Outline (N = Narrow, W = Wide), SSOP = Shrink Small-Outline Package, μMAX = Micro Max, TO-__ = Can

** Temperature Ranges: C = 0°C to +70°C, I = -25°C to +85°C, E = -40°C to +85°C, M = -55°C to +125°C

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchanges rates.

†† Future product—contact factory for pricing and availability. Specifications are preliminary.

Part Number	Input Voltage Range (V)	Output Voltage (V)	Quiescent Supply Current (mA), max(typ)	Output (mA)	Pins-Package Options*	Temp. Ranges**	Features	Price† 1000-up ($)
CHARGE-PUMP CONVERTERS—UNREGULATED								
MAX1044	1.5 to 10	$-V_{IN}$, $+2 \times V_{IN}$	0.200(0.03)	20	8-DIP, 8-SO	C,E,M	60kHz oscillator boost mode	1.19
MAX660	1.5 to 5.5	$-V_{IN}$, $+2 \times V_{IN}$	0.5(0.12)	100	8-DIP, 8-SO	C,E,M	8-pin SO	2.95
MAX665	1.5 to 8	$-V_{IN}$, $+2 \times V_{IN}$	0.5(0.12)	100	8-DIP, 16-WSO	C,E,M		3.96
MAX680	2 to 6	$\pm 2 \times V_{IN}$	2(1)	±10	8-DIP, 8-SO	C,E,M	Dual output	1.62
MAX828/829	1.25 to 5.5	$-V_{IN}$	0.09(0.06)	25	5-SOT23	E	Better than ICL7660, smaller capacitors, ultra-small, lower R_{OUT}	1.30
MAX860/861	1.5 to 5.5	$-V_{IN}$, $+2 \times V_{IN}$	0.33(0.18)	50	8-SO, 8-µMAX	C,E,M	Up to 250kHz oscillation frequency	1.45
MAX864	1.5 to 6.2	$\pm 2 \times V_{IN}$	0.3(0.2)	±10	16-QSOP	E	5kHz to 200kHz frequency select, 1µA shutdown	1.50
MAX865	1.5 to 6.2	$\pm 2 \times V_{IN}$	1.0(0.6)	±10	8-µMAX	E	Ultra-small µMAX package	1.30
ICL7660	1.5 to 10	$-V_{IN}$, $+2 \times V_{IN}$	0.175(0.110)	20	8-DIP, 8-SO, 8-TO99, 8-µMAX	C,E,M	µMAX package	1.09
ICL7662	4.5 to 20	$-V_{IN}$, $+2 \times V_{IN}$	0.6(0.25)	10	8-DIP, 8-SO, 8-TO99	C,I		1.86
Si7661	4.5 to 20	$-V_{IN}$, $+2 \times V_{IN}$	2(0.3)	10	8-DIP, 8-SO, 8-TO99	C,I		1.86

Part Number	Input Voltage Range (V)	Output Voltage (V)	Quiescent Supply Current (mA), max(typ)	Output (mA)	Pins-Package Options*	Temp. Ranges**	EV Kit	Features	Price† 1000-up ($)
CHARGE-PUMP CONVERTERS—REGULATED									
MAX619	2 to 3.6	5	0.15	60	8-DIP, 8-SO	C,E,M	Yes	No inductors, battery backup	1.60
MAX622	3.5 to 16.5	V_{IN} + 11	0.5(0.07)	500µA	8-DIP, 8-SO	C,E		High-side switching	1.86
MAX662A	4.5 to 5.5	12	0.5(0.19)	30mA, guaranteed over temp.	8-DIP, 8-SO	C,E,M	Yes	World's smallest 12V flash memory programmer	2.09
MAX840/843/844	2.5 to 10	-2 or adj.	1.1(0.75)	10	8-SO	I,E	Yes	Low-voltage negative GaAsFET bias, low noise, 1µA shutdown	1.75
MAX850-853	4.5 to 10	-4.1 or adj.	3(2)	5	8-SO	I,E	Yes	Negative GaAsFET bias, low noise, 1µA shutdown	1.65

PCMCIA Switch Matrices

Part Number	Input Voltages (V)	Outputs	Controls	Pins-Package Options*	Temp. Ranges**	Features	Price† 1000-up ($)
MAX1600/1603	3.3/5/12	2 card slots	Std. PCMCIA	28-SSOP	E	Internal V_{CC} and V_{PP} switches, current limit, thermal protection	5.95/5.25
MAX1601/1604	3.3/5/12	2 card slots	SMBus	28-SSOP	E	Internal V_{CC} and V_{PP} switches, current limit, thermal protection	5.95/5.25
MAX1602	3.3/5/12	1 card slots	Std. PCMCIA	16-QSOP	E	Internal V_{CC} and V_{PP} switches, current limit, thermal protection	2.35
MAX613	3.3/5/12	2 card slots	Std. PCMCIA	14-DIP, 14-SO	C,E	Internal V_{PP} switches, external V_{CC} drivers	1.68
MAX614	3.3/5/12	1 card slot	Std. PCMCIA	8-DIP, 8-SO	C,E	Internal V_{PP} switches, external V_{CC} drivers	1.48
MAX780A–C	3.3/5/12	2 card slots	Std. PCMCIA	24-DIP, 24-SSOP	C,E	Internal V_{PP} switches, external V_{CC} drivers, V_{PP} valid output	2.25/2.00/2.05
MAX780D	3.3/5/12	2 card slots	Std. PCMCIA	20-DIP, 20-SSOP	C,E	Internal V_{PP} switches, external V_{CC} drivers	1.80

* Package Options: DIP = Dual-In-Line Package, SO = Small Outline (N = Narrow, W = Wide), SSOP = Shrink Small-Outline Package, µMAX = Micro Max, TO-__ = Can

** Temperature Ranges: C = 0°C to +70°C, I = -25°C to +85°C, E = -40°C to +85°C, M = -55°C to +125°C

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchanges rates.

Linear Voltage Regulators

Part Number	Input Voltage Range (V)	Output Voltage (V)	Dropout Voltage (V)	Quiescent Current (µA), max(typ)	Output Voltage Accuracy (%)	Shutdown	Pins-Package Options*	EV Kit	Temp. Ranges**	Price† 1000-up ($)
DC LINEAR REGULATORS—POSITIVE OUTPUT										
MAX603	2.7 to 11.5	5 or adj. (1.3 to 11.5)	0.32 at 500mA	35(15)	±5	2µA off	8-DIP, 8-SO (P_{DISS} = 1.8W)		C,E,M	1.85
MAX604	2.7 to 11.5	3.3 or adj. (1.3 to 11.5)	0.48 at 400mA	35(15)	±5	2µA off	8-DIP, 8-SO (P_{DISS} = 1.8W)		C,E,M	1.85
MAX663	2 to 16.5	Fixed 5 or adj.(1.3 to 15)	0.9 at 40mA	12(6)	±5	Yes	8-DIP, 8-SO		C,E,M	1.25
MAX666	2 to 16.5	Fixed 5 or adj.(1.3 to 15)	0.9 at 40mA	12(6)	±5	Yes	8-DIP, 8-SO		C,E,M	1.38
MAX667	3.5 to 16.5	Fixed 5 or adj.(1.3 to 15)	0.15 at 200mA	25(20)	±4	Yes	8-DIP, 8-SO		C,E,M	2.35
MAX687	2.7 to 11	Fixed 3.3	0.073 at 500mA, 0.80 at 4A	250(150)	±3	Yes 25µA, off 1µA	8-DIP, 8-SO, 8-µMAX		C,E	1.60
MAX688/689	2.7 to 11	Fixed 3.3/3.0	0.073 at 500mA, 0.80 at 4A	250(150)	±3	Yes 25µA, off 1µA	8-DIP, 8-SO, 8-µMAX	Yes	C,E	1.60
MAX882	2.7 to 11.5	3.3 or adj. (1.5 to 11.5)	0.32 at 200mA	15(10)	±5	15µA standby	8-DIP, 8-SO (P_{DISS} = 1.5W)		C,E,M	1.45
MAX883	2.7 to 11.5	5 or adj. (1.5 to 11.5)	0.22 at 200mA	15(10)	±5	1µA off	8-DIP, 8-SO (P_{DISS} = 1.5W)		C,E,M	1.45
MAX884	2.7 to 11.5	3.3 or adj. (1.5 to 11.5)	0.32 at 200mA	15(10)	±5	1µA off	8-DIP, 8-SO (P_{DISS} = 1.5W)		C,E,M	1.45
MAX8862	2.5 to 11.5	2.85/3.18/4.9 or adj. (2 to 11)	0.16 at 200mA	330(200)	±3.5	10nA off	16-NSO		E	2.20
MAX8863/8864	2.5 to 5.5	1.25 to V_{IN}	0.12 at 50mA	170(70)	±3.5	Yes	5-SOT23		E	0.79
MAX8865/8866	8.5 to 5.5	2.8/2.84/3.15 or adj. (1.3 to 5.5)	0.055 at 50mA	270(105)	±2.5	2nA off	8-µMAX		E	0.79
ICL7663/A	1.5 to 16/2 to 16	Adj.(1.3 to 15)	0.9 at 40mA	10(3.5)	±8/±1.9	Yes	8-DIP, 8-SO, 8-TO99		C,E,I,M	1.81/1.99
DC LINEAR REGULATORS—NEGATIVE OUTPUT										
MAX664	-2 to -16.5	Fixed -5 or -1.3 to -15	0.35 at 40mA	12(6)	±5	Yes	8-DIP, 8-SO		C,E,M	1.75
ICL7664A	-2 to -16	-1.3 to -15	0.4 at 30mA	10(3.5)	±1	Yes	8-DIP, 8-SO, 8-TO99		C,I,M	2.40
ICL7664B	-2 to -16	-1.3 to -15	0.4 at 30mA	10(3.5)	±5	Yes	8-DIP, 8-SO, 8-TO99		C,I,M	1.85

Battery Chargers

Part Number	No. of Cells Charged	Cell Chemistry	Charge Rate	Charge Termination Method	Pins-Package Options*	Temp. Ranges**	EV Kit	Features	Price† 1000-up ($)
MAX1640/1641	1 to 16	Li+/NiCd/NiMH	Fast, trickle, top-off	Voltage and current limit	16-QSOP	E	Yes	High-efficiency PWM current-source, synchronous rectifier	††
MAX1647	1 to 8	Universal	Digitally programmed	Voltage and current limit, thermistor	120-SSOP	E	Yes	SBS level 2 smart-battery charger with SMBus interface	††
MAX1648	1 to 8	Universal	User set	Voltage and current limit thermistor	16-SO	E	Yes	User-programmable voltage/current set points	††
MAX2003	1 to 16	NiCd and/ or NiMH	Fast, trickle, top-off	Temp slope, neg. ΔV, max temp, max time	16-DIP, 16-WSO 16-NSO	C	Yes	Linear or switcher, built-in term. algorithms, discharge-before-charge	3.25
MAX2003A	1 to 16	NiCd and/ or NiMH	Fast, trickle, top-off	Temp slope, neg. ΔV, max temp, max time	16-DIP, 16-WSO 16-NSO	C	Yes	Improved MAX2003, better loop response and pulse trickle-charge	3.80
MAX712	1 to 16	NiMH	Fast, trickle	0ΔV, max V, max temp, max time	16-DIP, 16-NSO	C,E,M	Yes	Linear or switcher, supplies load while charging, built-in term. algorithms	3.09
MAX713	1 to 16	NiCd	Fast, trickle	Neg. ΔV, max V, max temp, max time	16-DIP, 16-NSO	C,E,M	Yes	Linear or switcher, supplies load while charging, built-in term. algorithms	3.09
MAX846A	1 to 10	Li+/NiCd/NiMH	Fast, trickle, top-off	Universal charger, user set	16-QSOP	E	Yes	Complete system, 1% accurate V_{OUT} for Li+, built-in 1% LDO, drives PNP, cost-saving, independent V & I reg loops	3.25

* Package Options: DIP = Dual-In-Line Package, SO = Small Outline (N = Narrow, W = Wide), TO-__ = Can

** Temperature Ranges: C = 0°C to +70°C, I = -25°C to +85°C, E = -40°C to +85°C, M = -55°C to +125°C

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†† Future product—contact factory for pricing and availability. Specifications are preliminary.

Multiple-Output, System-Integrated Power Management Supplies

Part Number	Input Voltage Range (V)	Linear Output Voltage (V)	DC-DC Output Voltages (V)	Auxiliary Outputs (V)	Quiescent Supply Current, Over Temp. (µA max)	Pins-Package Options*	Temp. Ranges**	EV Kit	Features	Price† 1000-up ($)
2- to 3-CELL INPUTS										
MAX717-721	0.9 to 5.5 (battery), 7 to 18 (plug-in adapter)	–	3.3 (MAX717), 3.3 or 5 (MAX718/720), 3 or 5 (MAX719/721)	5 or 12 (all)	60, 40 shutdown	16-NSO	C,E	Yes (MAX717-MAX719)	Built-in switchover from main battery to plug-in adapter power, low-voltage warning, AC detect, clock & RAM keep-alive mini-switcher from backup battery	4.95
MAX722/723	0.85 to 5.5 (battery), 7 to 18 (plug-in adapter)	–	3.3 or 5 (MAX722), 3 or 5 (MAX723)	Neg. LCD (0 to -40)	60, 40 shutdown	16-NSO	C,E	Yes	Built-in switchover from main battery to plug-in adapter power, low-voltage warning	4.63
MAX863	1.5 to 11	–	Main = 3.3 or 5 or adj./1A Aux. = adj./1A	LBI/LBO low-battery detector	45 w/main on, 65 w/both on, 1 in shutdown	16-QSOP	E	Yes	Two high-efficiency boost controllers on one IC, for PDAs and organizers	††
5- to 16-CELL (30V) INPUTS										
MAX1630/ 1632/1633/ 1635	4.2 to 30	5.0 at 50mA	3.3 or adj. 5.0 or adj.	12V @ 120mA	10 shutdown, 30 standby (typ), 2.5mW (typ) both outputs enabled	28-SSOP		Yes	High-efficiency controller for notebook computers, include 12V Li+ and secondary winding controller, MAX1630/32 include OVP/VVP	††
MAX1631/ 1634	4.2 to 30	5.0 at 50mA	3.3 or adj. 5.0 or adj.	Programmable secondary	10 shutdown, 30 standby, 1.5mW (typ) both outputs enabled	28-SSOP		Yes	High-efficiency controller for notebook computers, include secondary winding controller, MAX1631 includes OVP/VVP	††
MAX781	5 to 18	3.3 at 10mA 5.0 at 25mA	3.3, 14, battery charger	Battery charger, current source, dual V_{PP} outputs	100 shutdown, 750 standby, 2mA operating	36-SSOP	C,E		High-power controller to 50W or more,dual PCMCIA V_{PP} outputs, analog mux, SPI interface	8.80
MAX782	5.5 to 30	3.3 at 5mA 5 at 25mA	3.3‡, 5, 14	Dual V_{PP} outputs	70 standby, 750 per output enabled	36-SSOP	C,E	Yes	High-power dual controller to 50W or more, dual PCMCIA V_{PP} outputs, three precision voltage monitors	5.95
MAX783	5.5 to 30	3.3 at 5mA 5.0 at 25mA	3.3‡, 5, 14	Dual V_{PP} outputs	70 standby 750 per output enabled	36-SSOP	C,E	Yes	High-power dual controller to 50W or more, dual PCMCIA V_{PP} outputs, three precision voltage monitors, optimized for 6-cell operation	5.95
MAX786	5.5 to 30	3.3 at 5mA 5.0 at 25mA	3.3‡, 5	–	40 shutdown, 70 standby 750 per output enabled	28-SSOP	C,E	Yes	High-power dual controller to 50W or more, two precision voltage monitors	4.15
BATTERY-CHARGING SYSTEM										
MAX846A	3.5 to 20	Up to 2A	N/A	1%, 3.3V, 20mA LDO	500 (on) 1 (off)	16-QSOP	E	Yes	Cost-saving universal charging system, 0.5% reference for Li+, drives low-cost PNP, independent I and V loops, 1% LDO is power to µC and reference for ADC	3.25

* Package Options: DIP = Dual-In-Line Package, SO = Small Outline (N = Narrow, W = Wide), SSOP = Shrink Small-Outline Package

** Temperature Ranges: C = 0°C to +70°C, E = -40°C to +85°C, I = -25°C to +85°C, M = -55°C to +125°C

‡ Or 3.45V ("R" version), 3.6V ("S" version)

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LCD & CCFL Display Power Supplies

Part Number	Input Voltage Range (V)	DC-DC Output Voltages (V)	Quiescent Supply Current (µA)	Pins-Package Options*	EV Kit	Features	Price† 1000-up ($)
MAX1044	1.5 to 10	$-V_{IN}$ or 2 x V_{IN}	30	8-DIP, 8-SO		No inductors, 60kHz boost pin, pager LCD supply	1.19
MAX1610	4.5 to 28	CCFL drive, configurable	2mA	16-SO	Yes	Internal MOSFET, digital adjust, open and shorted lamp protection	3.85
MAX1611	4.5 to 28	CCFL drive, configurable	2mA	16-SO	Yes	Internal MOSFET, digital SMBus adjust, open and shorted lamp protection	3.85
MAX1620	4.5 to 24	Positive or negative LCD, configurable	500	16-QSOP		Digital adjust, 32 levels	††
MAX1621	4.5 to 24	Positive or negative LCD, configurable	500	16-QSOP		SMBus adjust, 32 levels	††
MAX1771	2 to 16.5	Positive LCD, adjustable	85	8-DIP, 8-SO	Yes	PFM controller, high efficiency, 5µA shutdown	1.80
MAX749	2 to 6	Negative LCD	60	8-DIP, 8-SO	Yes	Digital LCD adjustment	2.49
MAX753	6 to 24	CCFL drive, configurable; negative LCD, configurable	100	16-DIP, 16-NSO		Digital CCFT and LCD adjustment	4.45
MAX754	6 to 24	CCFL drive, configurable; positive LCD, configurable	100	16-DIP, 16-NSO		Digital CCFT and LCD adjustment	4.45
MAX759	4 to 15	Negative LCD, adjustable	1.2mA	14-DIP, 16-WSO	Yes	Internal MOSFET	2.75
MAX774/775/776	3 to 16.5	Negative LCD, adjustable	85	8-DIP, 8-SO	Yes	PFM controller, high efficiency, 5µA shutdown	2.20
MAX860/861	1.5 to 5.5	$-V_{IN}$ or 2 x V_{IN}	180	8-SO, 8-µMAX		No inductors, up to 250kHz oscillator, 2.2µF caps, smallest pager LCD supply	1.45
ICL7660	1.5 to 10	$-V_{IN}$ or 2 x V_{IN}	110	8-DIP, 8-SO, 8-µMAX		No inductors, low-cost pager LCD supply, µMAX package	1.09

MOSFET Drivers

Part Number	Output Resistance (Ω) max(typ)	Rise/Fall, T_A = +25°C (ns max)	Rise/Fall, Over Temp. (ns max)	Peak Output Current (A)	Supply Voltage (V)	Pins-Package Options*	Temp. Ranges**	Features	Price† 1000-up ($)
MAX4420/4429	2.5(1.5)	30/30(2500pF)	60/60(2500pF)	6	4.5 to 18	8-DIP, 8-SO	C,E,M	Single noninverting/single inverting	1.71
MAX4426/4427/4428	10(4)	30/30(1000pF)	40/40(1000pF)	1.5	4.5 to 18	8-DIP, 8-SO	C,E,M	Dual inverting/dual noninverting/dual mixed	1.61
MAX626/627/628	15(4)	30/30(1000pF)	40/40(1000pF)	2	4.5 to 18	8-DIP, 8-SO	C,E,M	Dual inverting/dual noninverting/dual mixed	1.49
ICL7667	12(4)	30/30(1000pF)	40/40(1000pF)	1.5	4.5 to 15	8-DIP, 8-SO	C,E,M	Dual inverting	1.12
TSC426/427/428	15(6)	30/30(1000pF)	60/40(1000pF)	1.5	4.5 to 18	8-DIP, 8-SO	C,E,M	Dual inverting/dual noninverting/dual mixed	1.06

Miscellaneous Power Supplies

Part Number	Description	Pins-Package Options*	Temp. Range**	EV Kit	Features	Price† 1000-up ($)
MAX845	Isolated transformer driver	8-SO, 8-µMAX	E	Yes	750mW output, thin transformer, fits PCMCIA cards	1.55
MAX890L	Current-limited power switch	8-SO	E		90mΩ, 1A switch	1.25
MAX891L/892L	Current-limited power switches	8-µMAX	E		150mΩ/0.5A (MAX891L), 300mΩ/0.25A (MAX892L)	††
MAX894L/895L	Dual current-limited power switches	8-SO	E		Dual, 150mΩ/0.5A (MAX894L), 300mΩ/0.25A (MAX895L)	1.99

* Package Options: DIP = Dual-In-Line Package, SO = Small Outline (N = Narrow, W = Wide), SSOP = Shrink Small-Outline Package

** Temperature Ranges: C = 0°C to +70°C, E = -40°C to +85°C, M = -55°C to +125°C

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19-0459; Rev 0; 1/96

EVALUATION KIT AVAILABLE

MAXIM

Low-Profile, 5V/12V or Adjustable, Step-Up DC-DC Converters for Flash Memory/PCMCIA Cards

General Description

The MAX606/MAX607 are the smallest CMOS, step-up DC-DC converters available for flash memory and PC (PCMCIA) cards. They switch at up to 1MHz, permitting the entire circuit to fit in 0.25in², yet remain under 1.35mm high to fit Type 1, 2, and 3 card standards. These devices operate from a 3V to 5.5V input and provide a ±4%-accurate output that is preset to 5V or 12V, or adjustable from V_{IN} to 12.5V. Their guaranteed output current is 60mA at 12V.

The MAX606 switches at up to 1MHz and fits Type 1 (thinnest standard) flash memory and PCMCIA cards. It uses a thin, 1.19mm high, 5µH inductor and small, 0.68µF output capacitors. The entire circuit fits in 0.25in² and is less than 1.35mm high.

The MAX607 switches at up to 500kHz, fitting Type 2 and 3 cards, as well as hand-held devices where height requirements are not as critical. It uses less board area than the MAX606, fitting in 0.16in², but requires 2.5mm of height. It also has a lower no-load supply current than the MAX606.

Both devices use a unique, current-limited pulse-frequency-modulation (PFM) control scheme that optimizes efficiency over all input and output voltages. Other features include 1µA logic-controlled shutdown and user-controlled soft-start to minimize inrush currents.

The MAX606/MAX607 come in 8-pin µMAX and SO packages. The µMAX package uses half the board area of a standard 8-pin SO and has a maximum height of just 1.11mm.

Applications

PCMCIA Cards

Memory Cards

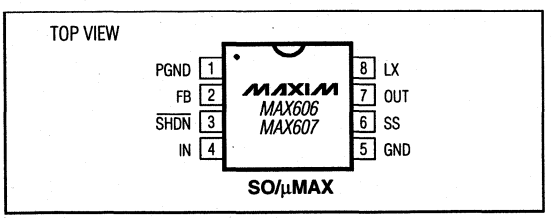
Single PCMCIA Slot Programming

Digital Cameras

Flash Memory Programming

Hand-Held Equipment

Pin Configuration



Features

- ♦ **Lowest-Height Circuit (1.35mm, max)**
- ♦ **±4% Regulated Output (5V, 12V, or Adjustable)**
- ♦ **Guaranteed 60mA Output at 12V**
- ♦ **1MHz Switching Frequency (MAX606)**
- ♦ **1µA Logic-Controlled Shutdown**
- ♦ **3V to 5.5V Input Voltage Range**
- ♦ **Compact 8-Pin µMAX Package**

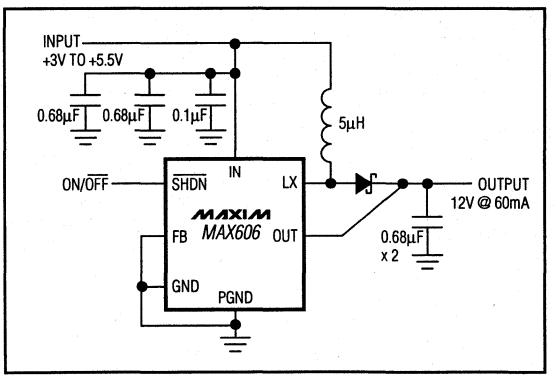
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX606C/D	0°C to +70°C	Dice*
MAX606ESA	-40°C to +85°C	8 SO
MAX606EUA	-40°C to +85°C	8 µMAX
MAX607C/D	0°C to +70°C	Dice*
MAX607ESA	-40°C to +85°C	8 SO
MAX607EUA	-40°C to +85°C	8 µMAX

** Contact factory for dice specifications.*

4

Typical Operating Circuit



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Low-Profile, 5V/12V or Adjustable, Step-Up DC-DC Converters for Flash Memory/PCMCIA Cards

ABSOLUTE MAXIMUM RATINGS

IN to GND ..... -0.3V to +6V
LX, OUT to GND ..... -0.3V to +15V
PGND to GND ..... ±0.3V
FB to GND ..... -0.3V to (V_{CC} + 0.3V)
SS, $\overline{SHDN}$ to GND ..... -0.3V to +6V

Continuous Power Dissipation (T_A = +70°C)
SO (derate 5.88mW/°C above +70°C) 471mW
µMAX (derate 4.10mW/°C above +70°C) 330mW
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature ..... +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.3V, GND = PGND = FB = 0V, $\overline{SHDN}$ = IN, T_A = 0°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage			3.0		5.5	V
Undervoltage Lockout Threshold				2.4	2.8	V
Output Voltage	3V < V_{IN} < 5.5V (Note 1)	FB = IN, I_{LOAD} = 0mA to 90mA	4.8	5.0	5.2	V
		FB = GND, I_{LOAD} = 0mA to 60mA	11.5	12.0	12.5	
FB Regulation Setpoint	0.1V < V_{FB} < (V_{IN} - 0.1V)		1.96	2.00	2.04	V
Adjustable Output Voltage Range	0.1V < V_{FB} < (V_{IN} - 0.1V)		V_{IN}		12.5	V
Line Regulation	V_{IN} = 3V to 5.5V			0.5		%
Switch On-Resistance				0.4	1	Ω
Switch Off Leakage	V_{LX} = 12V				10	µA
Switch Current Limit			0.7		1.1	A
SS Resistance	$V_{\overline{SHDN}}$ = V_{IN}, V_{SS} = 150mV		30	45	60	kΩ
	$V_{\overline{SHDN}}$ = V_{SS} = 0V				0.5	
Quiescent Supply Current	V_{OUT} = 13V	MAX606		250	500	µA
		MAX607		150	300	
Shutdown Quiescent Current	$V_{\overline{SHDN}}$ = 0V, OUT = IN			0.01	10	µA
OUT Input Current	V_{OUT} = 13V				80	µA
Switch On-Time Constant (K)	3V < V_{IN} < 5.5V (t_{ON} = K / V_{IN})	MAX606	1.9	3.0	4.3	µs-V
		MAX607	3.8	6.0	8.6	
Switch Off-Time Ratio	2V < (V_{OUT} + 0.5V - V_{IN}) < 8V (see *Pulse-Frequency-Modulation Control Scheme* section)		0.3		0.7	
$\overline{SHDN}$ Input Low Voltage	V_{IN} = 3V				0.25V_{IN}	V
$\overline{SHDN}$ Input High Voltage	V_{IN} = 5.5V		0.66V_{IN}			V
$\overline{SHDN}$ Input Current	$V_{\overline{SHDN}}$ = 0V or V_{IN}				±1	µA
FB Input Low Voltage	V_{IN} = 3V to 5.5V. For V_{FB} below this voltage, output regulates to 12V.				0.1	V
FB Input High Voltage	V_{IN} = 3V to 5.5V. For V_{FB} above this voltage, output regulates to 5V.		V_{IN} - 0.1			V
FB Input Current	V_{FB} = 2.05V, V_{OUT} = 13V				200	nA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.3V, GND = PGND = FB = 0V, $\overline{SHDN}$ = IN, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage			3.0		5.5	V
Undervoltage Lockout Threshold					2.8	V
Output Voltage	3V < V_{IN} < 5.5V (Note 1)	FB = IN, I_{LOAD} = 0mA to 90mA	4.75		5.25	V
		FB = GND, I_{LOAD} = 0mA to 60mA	11.4		12.6	
FB Regulation Setpoint	0.1V < V_{FB} < (V_{IN} - 0.1V)		1.94		2.06	V
Adjustable Output Voltage Range	0.1V < V_{FB} < (V_{IN} - 0.1V)		V_{IN}		12.5	V
Switch On-Resistance					1	Ω
Switch Off Leakage	V_{LX} = 12V				10	µA
Switch Current Limit			0.55		1.25	A
SS Resistance	$V_{\overline{SHDN}}$ = V_{IN}, V_{SS} = 150mV		30		60	kΩ
	$V_{\overline{SHDN}}$ = V_{SS} = 0V				0.5	
Quiescent Supply Current	V_{OUT} = 13V	MAX606			500	µA
		MAX607			300	
Shutdown Quiescent Current	$V_{\overline{SHDN}}$ = 0V, OUT = IN				10	µA
OUT Input Current	V_{OUT} = 13V				85	µA
Switch On-Time Constant (K)	3V < V_{IN} < 5.5V (t_{ON} = K/V_{IN})	MAX606	1.8		4.5	µs-V
		MAX607	3.5		9.0	
Switch Off-Time Ratio	2V < (V_{OUT} + 0.5V - V_{IN}) < 8V (see *Pulse-Frequency-Modulation Control Scheme* section)		0.3		0.7	
$\overline{SHDN}$ Input Low Voltage	V_{IN} = 3V				0.25V_{IN}	V
$\overline{SHDN}$ Input High Voltage	V_{IN} = 5.5V		0.66V_{IN}			V
$\overline{SHDN}$ Input Current	$V_{\overline{SHDN}}$ = 0V or V_{IN}				±1	µA
FB Input Low Voltage	V_{IN} = 3V to 5.5V. For V_{FB} below this voltage, output regulates to 12V.				0.1	V
FB Input High Voltage	V_{IN} = 3V to 5.5V. For V_{FB} above this voltage, output regulates to 5V.		V_{IN} - 0.1			V
FB Input Current	V_{FB} = 2.05V, V_{OUT} = 13V				200	nA

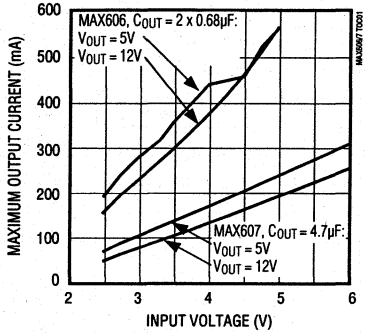
Note 1: The load specification is guaranteed by DC parametric tests and is not production tested in circuit.
Note 2: Specifications to -40°C are guaranteed by design, not production tested.

Low-Profile, 5V/12V or Adjustable, Step-Up DC-DC Converters for Flash Memory/PCMCIA Cards

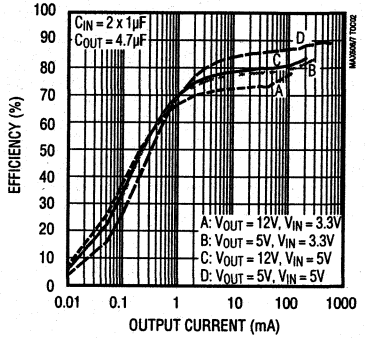
Typical Operating Characteristics

(V_{IN} = 3.3V, T_A = +25°C, unless otherwise noted.)

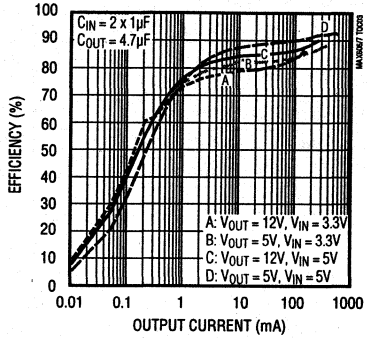
MAXIMUM OUTPUT CURRENT vs. INPUT VOLTAGE



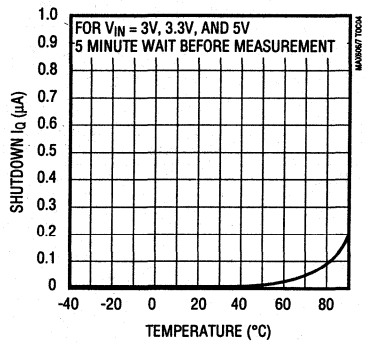
MAX606 EFFICIENCY vs. OUTPUT CURRENT



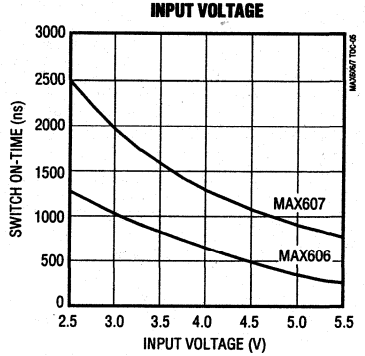
MAX607 EFFICIENCY vs. OUTPUT CURRENT



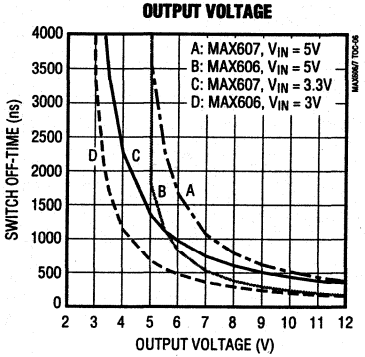
SHUTDOWN QUIESCENT CURRENT vs. TEMPERATURE



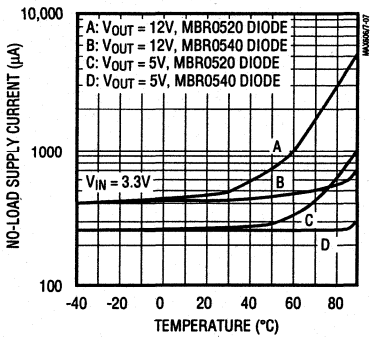
SWITCH ON-TIME vs. INPUT VOLTAGE



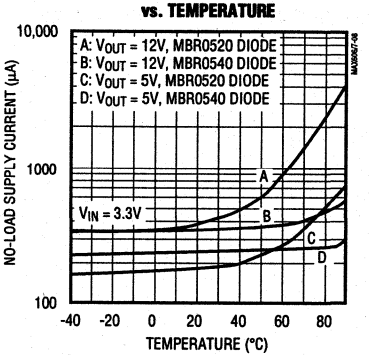
SWITCH OFF-TIME vs. OUTPUT VOLTAGE



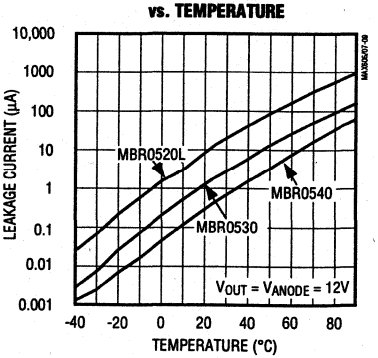
MAX606 NO-LOAD SUPPLY CURRENT vs. TEMPERATURE



MAX607 NO-LOAD SUPPLY CURRENT vs. TEMPERATURE



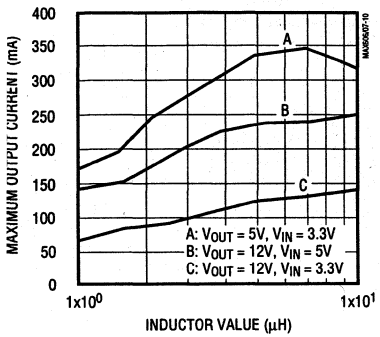
DIODE LEAKAGE CURRENT vs. TEMPERATURE



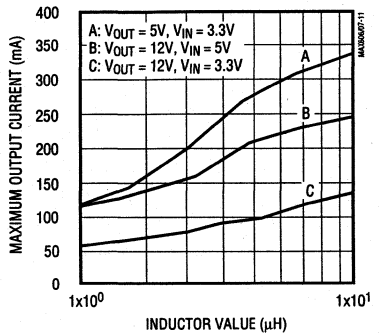
Typical Operating Characteristics (continued)

(V_{IN} = 3.3V, T_A = +25°C, unless otherwise noted.)

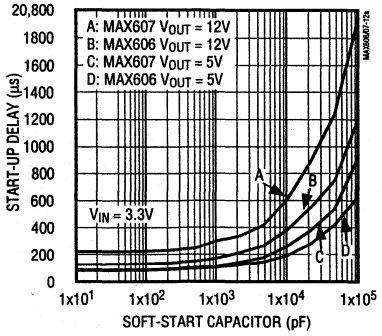
MAX606
MAXIMUM OUTPUT CURRENT vs. INDUCTOR VALUE



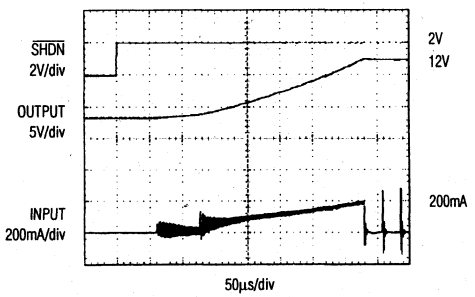
MAX607
MAXIMUM OUTPUT CURRENT vs. INDUCTOR VALUE



START-UP DELAY vs. SOFT START CAPACITOR

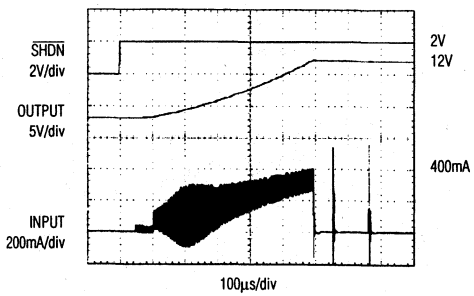


MAX606
START-UP DELAY AND INRUSH CURRENT



I_{LOAD} = 1mA, INPUT = 3.3V, C_{SS} = 10nF, C_{OUT} = 2 x 0.68µF

MAX607
START-UP DELAY AND INRUSH CURRENT



I_{LOAD} = 1mA, INPUT = 3.3V, C_{SS} = 10nF, C_{OUT} = 4.7µF

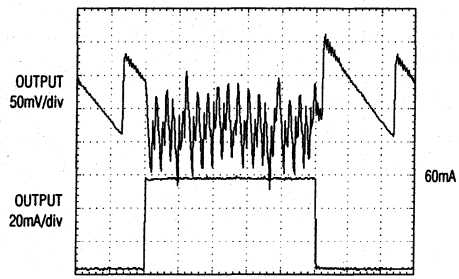
4

Low-Profile, 5V/12V or Adjustable, Step-Up DC-DC Converters for Flash Memory/PCMCIA Cards

Typical Operating Characteristics (continued)

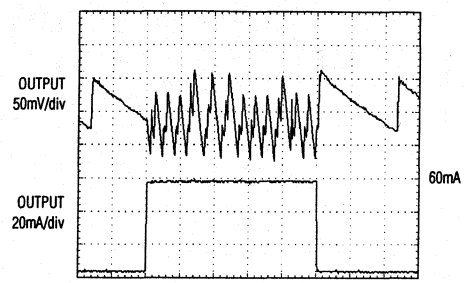
(V_{IN} = 3.3V, T_A = +25°C, unless otherwise noted.)

MAX606
LOAD-TRANSIENT RESPONSE



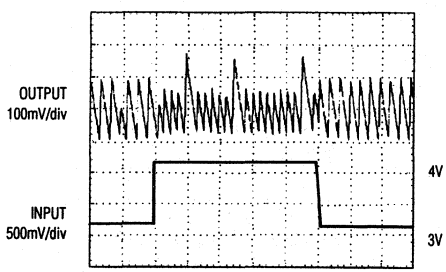
I_{LOAD} = 5mA to 60mA, OUTPUT = 12V, INPUT = 3.3V

MAX607
LOAD-TRANSIENT RESPONSE



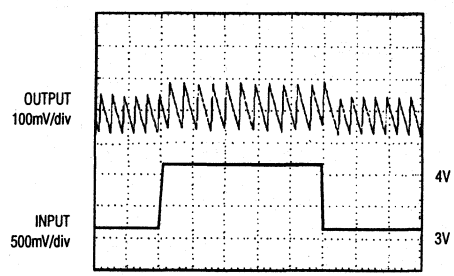
I_{LOAD} = 5mA to 60mA, OUTPUT = 12V, INPUT = 3.3V

MAX606
LINE-TRANSIENT RESPONSE



I_{LOAD} = 10mA, OUTPUT = 12V, INPUT = 3.3V TO 4.3V

MAX607
LINE-TRANSIENT RESPONSE



I_{LOAD} = 10mA, OUTPUT = 12V, INPUT = 3.3V TO 4.3V

Pin Description

PIN	NAME	FUNCTION
1	PGND	Power Ground. Source of N-channel power MOSFET.
2	FB	Feedback Input. Connect to IN for 5V output, to GND for 12V output, or to a resistive voltage divider between OUT and GND for an adjustable output between IN and 12.5V.
3	$\overline{SHDN}$	Shutdown Input, active low. Connect to GND to power down, or to IN for normal operation. Output power FET is held off when $\overline{SHDN}$ is low.
4	IN	Supply Voltage Input: 3.0V to 5.5V
5	GND	Analog Ground
6	SS	Soft-Start Input
7	OUT	Output. Always connect directly to the circuit output.
8	LX	Drain of N-channel power MOSFET

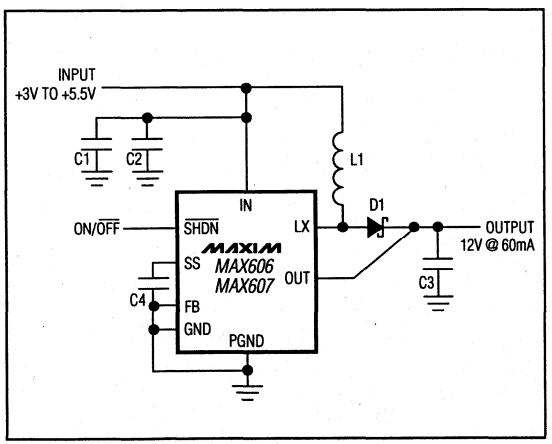


Figure 1. 12V Standard Application Circuit

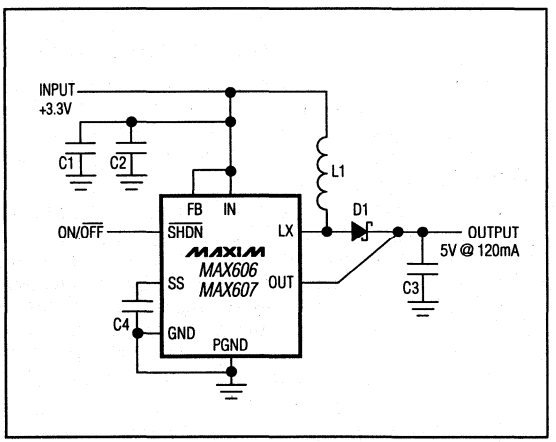


Figure 2. 5V Standard Application Circuit

Standard Application Circuits

This data sheet provides two predesigned standard application circuits. The circuit of Figure 1 produces 12V at 60mA from a 3V to 5.5V input. Table 1 lists component values and part numbers for both the MAX606 and MAX607 variations of this circuit. The circuit of Figure 2 produces 5V at a typical output current of 120mA from a 3.3V input. Each application circuit is designed to deliver the full rated output load current over the temperature range listed. Component values and part numbers for this circuit are listed in Table 2. See Table 3 for component suppliers' phone and fax numbers.

Low-Profile, 5V/12V or Adjustable, Step-Up DC-DC Converters for Flash Memory/PCMCIA Cards

Table 1. Suggested Components for 12V Standard Application Circuit of Figure 2

DESIGNATION	MAX606	MAX607
L1	5µH inductor Dale ILS-3825-XX	10µH inductor Sumida CLS62-100
D1	0.5A, 20V diode Motorola MBR0520L	0.5A, 20V diode Motorola MBR0520L
C1	0.1µF ceramic cap.	0.1µF ceramic cap.
C2	2 x 0.68µF ceramic cap. Marcon THCR20E1E684Z	2.2µF ceramic cap. Marcon THCR30E1E225M
C3	2 x 0.68µF ceramic cap. Marcon THCR20E1E684Z	2 x 1µF ceramic cap. Marcon THCR30E1E105M
C4	10nF ceramic cap.	10nF ceramic cap.

Table 2. Suggested Components for 5V Standard Application Circuit of Figure 1

DESIGNATION	MAX606	MAX607
L1	5µH, 1A inductor Dale ILS-3825-XX	10µH, 0.7A inductor Sumida CLS62B-100
D1	0.5A, 20V diode Motorola MBR0520L	0.5A, 20V diode Motorola MBR0520L
C1	0.1µF ceramic cap.	0.1µF ceramic cap.
C2	2 x 0.68µF ceramic cap. Marcon THCR20E1E684Z	2.2µF ceramic cap. Marcon THCR30E1E225M
C3	4.7µF ceramic cap. Marcon THCR30E1E475M	4.7µF ceramic cap. Marcon THCR30E1E475M
C4	10nF ceramic cap.	10nF ceramic cap.

Detailed Description

The remainder of this document contains the detailed information you'll need to design a circuit that differs from the two Standard Application Circuits. If you are using one of the predesigned circuits, the following sections are purely informational.

The MAX606/MAX607 CMOS, step-up DC-DC converters employ a current-limited pulse-frequency modulation (PFM) control scheme. This PFM control scheme regulates a boost topology to convert input voltages between 3V and 5.5V into either a pin-programmable 5V/12V output, or an adjustable output between V_{IN} and 12.5V. It optimizes performance over all input and output voltages, and guarantees output accuracy to ±4%.

The ultra-high switching frequency (typically 1MHz for the MAX606 and 0.5MHz for the MAX607) permits the use of extremely small external components, making these converters ideal for use in Types 1, 2, and 3 flash memory and PCMCIA applications.

Pulse-Frequency-Modulation Control Scheme

The MAX606/MAX607 employ a proprietary, current-limited PFM control scheme that combines the ultra-low supply current of traditional pulse-skipping PFM converters with the high full-load efficiency of current-mode pulse-width-modulation (PWM) converters. This particular control scheme is similar to the one used in previous current-limited PFM devices, which governed the switching current via maximum on-time, minimum off-time, and current limit, except it varies the on and off times according to the input and output voltages. This important feature enables the MAX606/MAX607 to achieve ultra-high switching frequencies while maintaining high output accuracy, low output ripple, and high efficiency over a wide range of loads and input/output voltages.

Table 3. Component Suppliers

SUPPLIER	PHONE	FAX
Dale Inductors	(605) 668-4131	(605) 665-1627
Motorola	(602) 244-3576	(602) 244-4015
Sumida USA	(708) 956-0666	(708) 956-0702
Sumida Japan	(03) 607-5111	(03) 607-5144
Marcon/United Chemi-Con	(708) 696-2000	(708) 518-9985

Figure 3 shows the functional diagram of the MAX606/MAX607. The internal power MOSFET is turned on when the error comparator senses that the output is out of regulation. The power switch stays on until either the timing circuit turns it off at the end of the on-time, or the switch current reaches the current limit. Once off, the switch remains off during the off-time. Subsequently, if the output is still out of regulation, another switching cycle is initiated. Otherwise, the switch remains turned off as long as the output is in regulation.

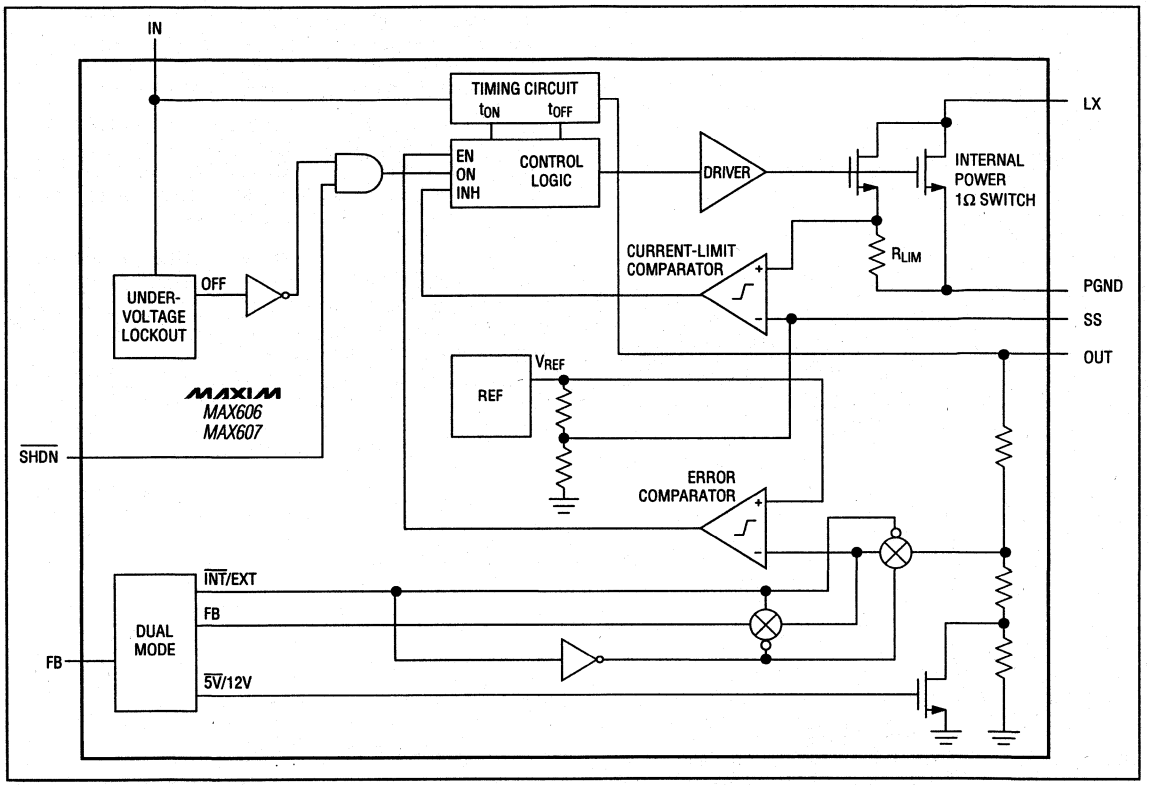


Figure 3. Functional Diagram

The on/off times are determined by the input and output voltages:

$$t_{ON} = K / V_{IN}$$

$$t_{OFF} = 0.5 \times K / (V_{OUT} + V_{DIODE} - V_{IN})$$

K is typically 3µs-V for the MAX606 and 6µs-V for the MAX607. This factor is chosen to set the optimum switching frequency and the one-cycle current limit, which determines the no-load output ripple at low output-to-input voltage differentials. The factor of 0.5 in the off-time equation is the typical switch off-time ratio. This ratio guarantees high efficiency under a heavy load by allowing the inductor to operate in continuous-conduction mode. For example, a switch off-time ratio of 1 would cause the device to operate on the edge of discontinuous-conduction mode.

To determine the actual switch off-time ratio for a particular device, measure t_{ON}, t_{OFF}, V_{IN}, and V_{OUT}, and then solve for the ratio by substituting these values into the off-time equation.

Unlike PWM converters, the MAX606/MAX607 generate variable-frequency switching noise. However, the amplitude of this noise does not exceed the product of the switch current limit and the output capacitor equivalent series resistance (ESR). Traditional clocked-PFM or pulse-skipping converters cannot make this claim.

Output Voltage Selection

The MAX606/MAX607 output voltage is pin-programmable to 5V and 12V, and also adjustable to voltages between V_{IN} and 12.5V. Connect FB to IN for a 5V output, to GND for a 12V output, or to a resistive divider between the output and GND for an adjustable output. Always connect OUT to the output.

When FB is connected to IN or GND, an internal voltage divider is configured to produce a predetermined

Low-Profile, 5V/12V or Adjustable, Step-Up DC-DC Converters for Flash Memory/PCMCIA Cards

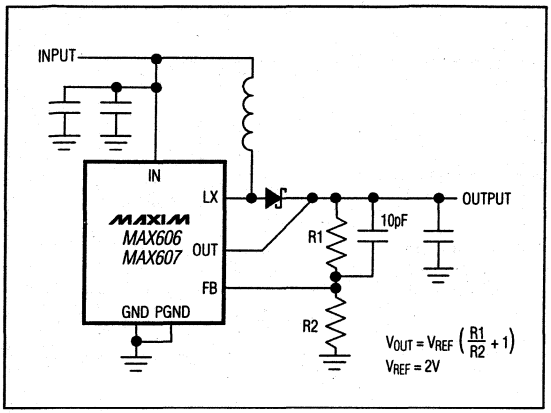


Figure 4. Adjustable Output Voltage

output. However, when the voltage at FB is between 0.1V above ground and 0.1V below V_{IN}, the device is in the adjustable output mode. In this mode, the MAX606/MAX607 output voltage is set by two external resistors, R1 and R2 (Figure 4), which form a voltage divider between the output and FB. Use the following equation to determine the output voltage:

$$V_{OUT} = V_{REF} (R1 / R2 + 1)$$

where V_{REF} = 2V. To simplify the resistor selection:

$$R1 = R2 [(V_{OUT} / V_{REF}) - 1]$$

Since the input current at FB is 200nA maximum, large values (up to 100kΩ) can be used for R2 with no significant loss of accuracy. For 1% error, the current through R2 should be at least 100 times the FB input bias current.

Soft-Start

Connecting a capacitor to the Soft-Start (SS) pin ensures a gradually increasing current limit during power-up or when exiting shutdown, thereby reducing initial inrush currents. This feature can be useful, for example, when an old battery's increased series resistance limits initial inrush currents. Using the soft-start feature in a situation like this minimizes the risk of overloading the incoming supply.

Soft-start timing is controlled by the value of the SS capacitor. On power-up, the SS capacitor is charged by the 2V reference through an internal, 45kΩ pull-up resistor. As the voltage on the SS pin increases, the voltage at the SS clamp output also increases, which in turn raises the current-limit threshold. The Start-Up Delay vs. SS Capacitor graph in the *Typical Operating Characteristics* shows typical timing characteristics for selected capacitor values and circuit conditions. The soft-start capacitor is discharged each time the MAX606 or MAX607 is put into shutdown, including during undervoltage lockout and when powering down at IN.

If the circuit is required to start up with no load, as in flash memory programming supplies, soft-start is not required. Omitting the soft-start capacitor permits a minimum output voltage rise time from the shutdown state, improving flash memory access time.

Undervoltage Lockout

The MAX606/MAX607 monitor the supply voltage at IN and operate for supply voltages greater than 2.8V. When an undervoltage condition is detected, control logic turns off the output power FET and discharges the soft-start capacitor to ground. The control logic holds the output power FET in an off state until the supply voltage rises above the undervoltage threshold, at which time a soft-start cycle begins.

Shutdown Mode

Connecting $\overline{SHDN}$ to GND will hold the MAX606/MAX607 in shutdown mode. In shutdown, the output power FET is off, but there is still an external path from IN to the load via the inductor and diode. The internal reference also turns off, which causes the soft-start capacitor to discharge. Typical device standby current in shutdown mode is 0.01µA. For normal operation, connect $\overline{SHDN}$ to IN. A soft-start cycle is initiated when the MAX606/MAX607 exit shutdown.

Applications Information

Inductor Selection

Use a 5µH inductor for the MAX606 and a 10µH inductor for the MAX607. See Table 3 for a list of component suppliers. Higher inductor values allow greater load currents due to operation in continuous-conduction mode, while lower inductor values lead to smaller physical size due to lower energy-storage requirements and lower output-filter-capacitor requirements. Potential drawbacks of using lower inductor values are increased output ripple, lower efficiency, and lower output-current capability due to operation in discontinuous-conduction mode. (See the Maximum Output Current vs. Inductor Value graph in the *Typical Operating Characteristics*.)

The inductor must have a saturation (incremental) current rating equal to the peak switch-current limit, which is 1.1A. For highest efficiency, minimize the inductor's DC resistance.

Diode Selection

The MAX606/MAX607's high switching frequency demands a high-speed rectifier. Use a Schottky diode with at least a 0.5A average current rating and a 1.2A peak current rating, such as an MBR0520L. See Table 3 for a list of component suppliers.

Capacitor Selection

Output Filter Capacitor

The output voltage ripple is a function of the output capacitor's equivalent series resistance (ESR) and capacitance. For best performance, use ceramic capacitors. Higher-ESR capacitors, such as tantalums, will cause excessive ripple. See Table 3 for a list of component suppliers.

The output voltage ripple is approximately 100mVp-p for the 12V Standard Application Circuit (Figure 1) and 50mV for the 5V circuit (Figure 2). To further reduce this ripple, or to reduce the ripple on a different application circuit, increase the value of the output filter capacitor. If this capacitor is low ESR (e.g., ceramic), the output voltage ripple will be dominated by this capacitance.

Input Bypass Capacitors

For applications where the MAX606/MAX607 are physically close to the input supply's filter capacitor (e.g., in PCMCIA drivers from the host computer), the input bypass capacitor may not be necessary.

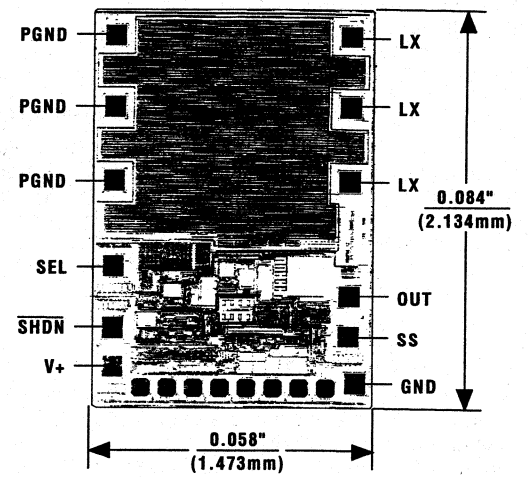
In other applications where the MAX606/MAX607 are more than a few inches a away from the supply (such as memory cards), the input bypass capacitor is needed to reduce reflected current ripple to the supply and improve efficiency by creating a low-impedance path for the ripple current. Under these circumstances, the associated high Q and low ESR of ceramic capacitors do not diminish the problem. Therefore, include some low-Q, moderate-ESR capacitance (e.g., tantalum) at the input in order to reduce ringing. See Table 3 for a list of component suppliers.

Layout

The MAX606/MAX607's high-frequency operation and high peak currents make PC board layout critical to minimize ground bounce and noise. Locate input bypass and output filter capacitors as close to the device pins as possible. All connections to OUT (and to FB when operating in adjustable-output mode) should also be kept as short as possible. A ground plane is recommended. Solder GND and PGND directly to the ground plane. Refer to the MAX606/MAX607 evaluation kit manual for a suggested surface-mount layout.

Low-Profile, 5V/12V or Adjustable, Step-Up DC-DC Converters for Flash Memory/PCMCIA Cards

Chip Topography



TRANSISTOR COUNT: 613

SUBSTRATE CONNECTED TO GND.

19-0438; Rev 0; 9/95

EVALUATION KIT AVAILABLE

MAXIM

5V or Adjustable, Low-Voltage, Step-Up DC-DC Controller

General Description

The MAX608 low-voltage step-up controller operates from a 1.8V to 16.5V input voltage range. Pulse-frequency-modulation (PFM) control provides high efficiency at heavy loads, while using only 85µA (typical) when operating with no load. In addition, a logic-controlled shutdown mode reduces supply current to 2µA typical. The output voltage is factory-set at 5V or can be adjusted from 3V to 16.5V with an external resistor divider.

The MAX608 is ideal for two- and three-cell battery-powered systems. An operating frequency of up to 300kHz allows use with small surface-mount components.

The MAX608 operates in "bootstrapped" mode only (with the chip supply, OUT, connected to the DC-DC output). For a 12V output without external resistors, or for nonbootstrapped applications (chip supply connected to input voltage), refer to the pin-compatible MAX1771. The MAX608 is available in 8-pin DIP and SO packages.

Features

- **1.8V to 16.5V Input Range**
- **85% Efficiency for 30mA to 1.5A Load Currents**
- **Up to 10W Output Power**
- **110µA Max Supply Current**
- **5µA Max Shutdown Current**
- **Preset 5V or Adjustable Output (3V to 16.5V)**
- **Current-Limited PFM Control Scheme**
- **Up to 300kHz Switching Frequency**
- **Evaluation Kit Available**

Applications

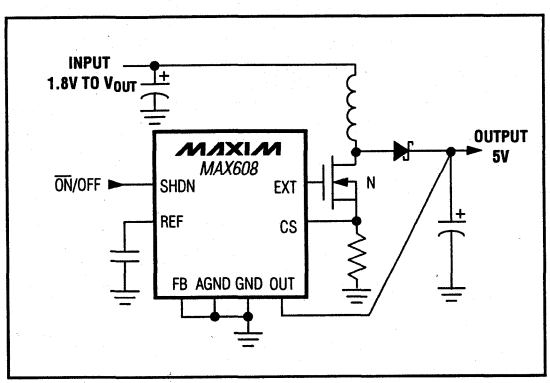
High-Efficiency DC-DC Converters
Battery-Powered Applications
Positive LCD-Bias Generators
Portable Communicators

Ordering Information

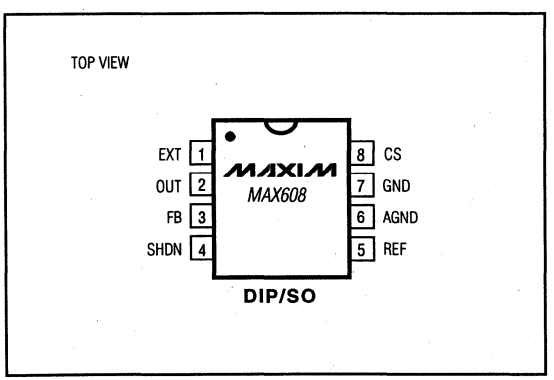
PART	TEMP. RANGE	PIN-PACKAGE
MAX608C/D	0°C to +70°C	Dice*
MAX608EPA	-40°C to +85°C	8 Plastic DIP
MAX608ESA	-40°C to +85°C	8 SO

** Contact factory for dice specifications.*

Typical Operating Circuit



Pin Configuration



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

5V or Adjustable, Low-Voltage, Step-Up DC-DC Controller

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
  OUT to GND ..... -0.3V, 17V
EXT, CS, REF, SHDN, FB to GND ..... -0.3V, (V_{OUT} + 0.3V)
GND to AGND ..... 0.1V, -0.1V
Continuous Power Dissipation (T_A = +70°C)
  Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
  SO (derate 5.88mW/°C above +70°C) 471mW

Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{OUT} = 5V, I_{LOAD} = 0mA, T_A = -40°C to +85°C where indicated. T_A = -25°C to +85°C for all other limits. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range (Note 2)		T_A = -25°C to +85°C		1.8		16.5	V
		T_A = -40°C to +85°C (Note 1)		1.9		16.5	
Minimum Start-Up Voltage		No load			1.6	1.8	V
Supply Current		V_{OUT} = 16.5V, SHDN ≤ 0.4V	T_A = -25°C to +85°C		85	110	µA
			T_A = -40°C to +85°C (Note 1)			120	
		V_{OUT} = 10V, SHDN ≥ 1.6V	T_A = -25°C to +85°C		2	5	µA
			T_A = -40°C to +85°C (Note 1)			10	
Output Voltage (Note 3)		V_{IN} = 2.0V to 5.0V, over full load range, circuit of Figure 2a	T_A = -25°C to +85°C	4.825	5.0	5.175	V
			T_A = -40°C to +85°C (Note 1)	4.800	5.0	5.200	
Output Voltage Line Regulation (Note 4)		V_{IN} = 2.7V to 4.0V, V_{OUT} = 5V, I_{LOAD} = 500mA, circuit of Figure 2a			7		mV/V
Output Voltage Load Regulation (Note 4)		V_{IN} = 2V, V_{OUT} = 5V, I_{LOAD} = 0mA to 500mA, circuit of Figure 2a			60		mV/A
Maximum Switch On-Time	t_{ON}(max)			12	16	20	µs
Minimum Switch Off-Time	t_{OFF}(min)			1.8	2.3	2.8	µs
Efficiency		V_{IN} = 4V, V_{OUT} = 5V, I_{LOAD} = 500mA, circuit of Figure 2a			87		%
Reference Voltage	V_{REF}	I_{REF} = 0µA	T_A = -25°C to +85°C	1.4625	1.5	1.5375	V
			T_A = -40°C to +85°C (Note 1)	1.4475		1.5525	
REF Load Regulation		0µA ≤ I_{REF} ≤ 100µA			-4	10	mV
REF Line Regulation		3V ≤ V_{OUT} ≤ 16.5V			40	100	µV/V
FB Trip Point Voltage (Note 5)	V_{FB}	T_A = -25°C to +85°C		1.4625	1.5	1.5375	V
		T_A = -40°C to +85°C (Note 1)		1.4475		1.5525	
FB Input Current	I_{FB}	T_A = -25°C to +85°C			-4	±20	nA
		T_A = -40°C to +85°C (Note 1)				±40	
SHDN Input High Voltage	V_{IH}	V_{OUT} = 1.8V to 16.5V		1.6			V
SHDN Input Low Voltage	V_{IL}	V_{OUT} = 1.8V to 16.5V				0.4	V
SHDN Input Current	I_{IN}	V_{OUT} = 16.5V, SHDN = 0V or 16.5V				±1	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{OUT} = 5V, I_{LOAD} = 0mA, T_A = -40°C to +85°C where indicated. T_A = -25°C to +85°C for all other limits. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Current-Limit Trip Level	V_{CS}	V_{OUT} = 3V to 16.5V	T_A = -25°C to +85°C	85	100	115	mV
			T_A = -40°C to +85°C (Note 1)	80		120	
CS Input Current	I_{CS}				0.01	±1	µA
EXT Rise Time		V_{OUT} = 5V, 1nF from EXT to GND			50		ns
EXT Fall Time		V_{OUT} = 5V, 1nF from EXT to GND			50		
EXT On-Resistance		EXT = high or low			15	30	Ω

Note 1: Limits over this temperature range are guaranteed by design.

Note 2: The MAX608 must be operated in bootstrapped mode with OUT connected to the DC-DC circuit output. The minimum output voltage set point is +3V.

Note 3: Output voltage guaranteed using preset voltages. See Figures 4a–4d for output current capability versus input voltage.

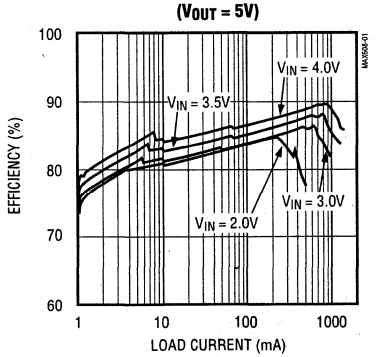
Note 4: Output voltage line and load regulation depend on external circuit components.

Note 5: Operation in the external-feedback mode is guaranteed to be accurate to the V_{FB} trip level, and does not include resistor tolerance.

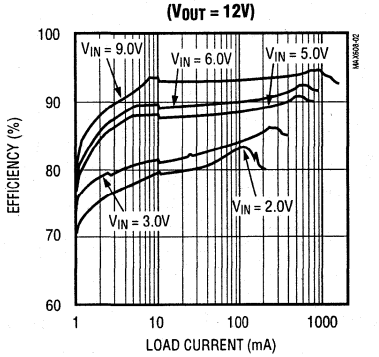
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

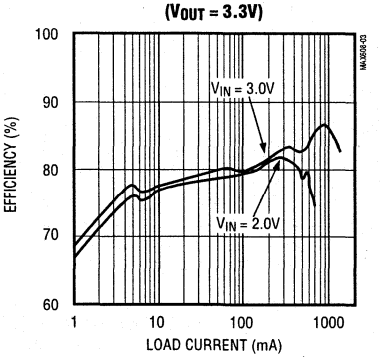
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 5V)



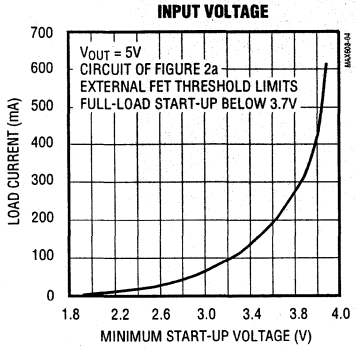
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 12V)



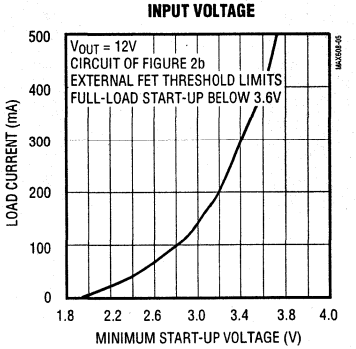
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 3.3V)



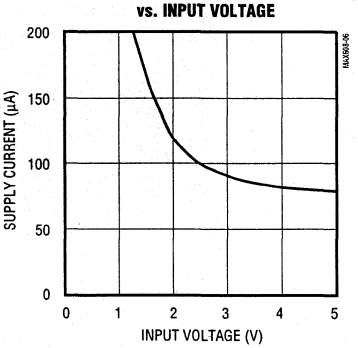
LOAD CURRENT vs. MINIMUM START-UP INPUT VOLTAGE



LOAD CURRENT vs. MINIMUM START-UP INPUT VOLTAGE



SUPPLY CURRENT vs. INPUT VOLTAGE

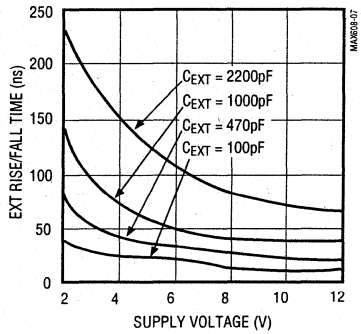


5V or Adjustable, Low-Voltage, Step-Up DC-DC Controller

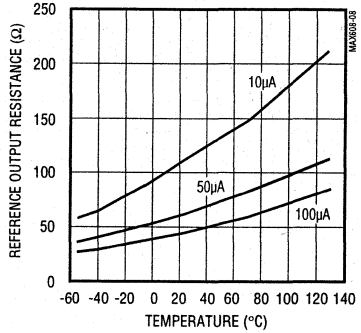
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

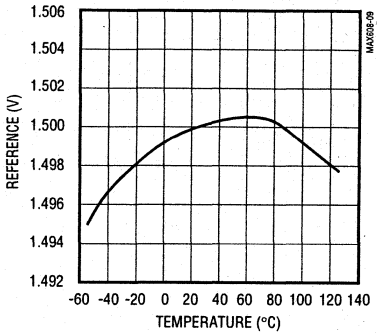
EXT RISE/FALL TIME vs. SUPPLY VOLTAGE



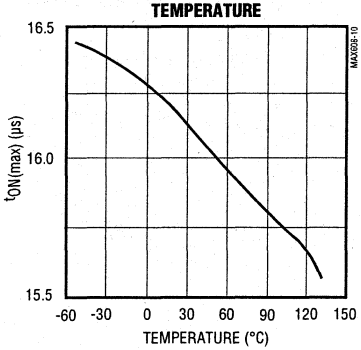
REFERENCE OUTPUT RESISTANCE vs. TEMPERATURE



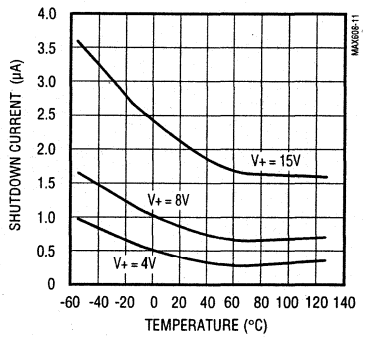
REFERENCE vs. TEMPERATURE



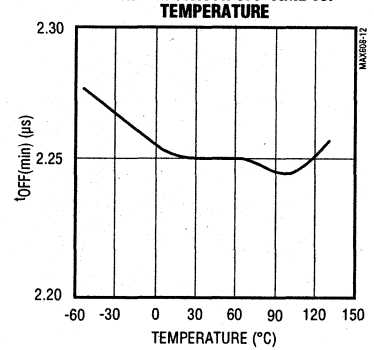
MAXIMUM SWITCH ON-TIME vs. TEMPERATURE



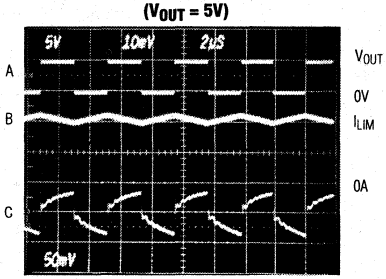
SHUTDOWN CURRENT vs. TEMPERATURE



MINIMUM SWITCH OFF-TIME vs. TEMPERATURE



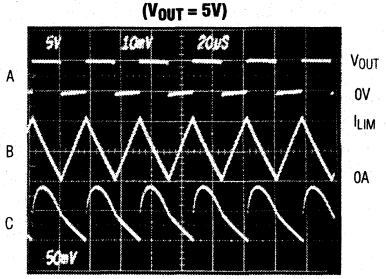
HEAVY-LOAD SWITCHING WAVEFORMS (V_{OUT} = 5V)



2µs/div

V_{IN} = 3V, I_{OUT} = 930mA, V_{OUT} = 5V
A = EXT VOLTAGE, 5V/div
B = INDUCTOR CURRENT, 1A/div
C = V_{OUT} RIPPLE, 50mV/div, AC-COUPLED

MEDIUM-LOAD SWITCHING WAVEFORMS (V_{OUT} = 5V)



20µs/div

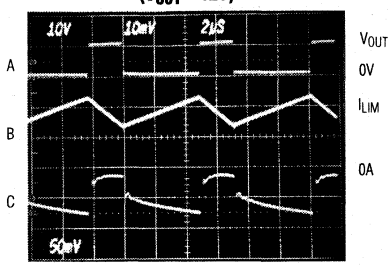
V_{IN} = 3V, I_{OUT} = 490mA, V_{OUT} = 5V
A = EXT VOLTAGE, 5V/div
B = INDUCTOR CURRENT, 1A/div
C = V_{OUT} RIPPLE, 50mV/div, AC-COUPLED

5V or Adjustable, Low-Voltage, Step-Up DC-DC Controller

Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

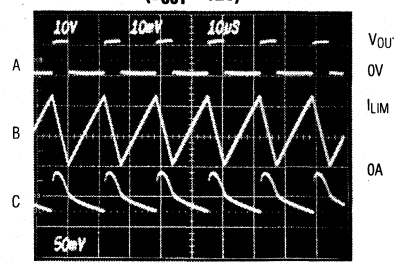
HEAVY-LOAD SWITCHING WAVEFORMS
(V_{OUT} = 12V)



2µs/div

V_{IN} = 4V, I_{OUT} = 490mA, V_{OUT} = 12V
A = EXT VOLTAGE, 10V/div
B = INDUCTOR CURRENT, 1A/div
C = V_{OUT} RIPPLE, 50mV/div, AC-COUPLED

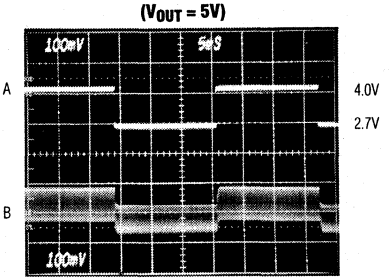
MEDIUM-LOAD SWITCHING WAVEFORMS
(V_{OUT} = 12V)



10µs/div

V_{IN} = 4V, I_{OUT} = 300mA, V_{OUT} = 12V
A = EXT VOLTAGE, 10V/div
B = INDUCTOR CURRENT, 1A/div
C = V_{OUT} RIPPLE, 50mV/div, AC-COUPLED

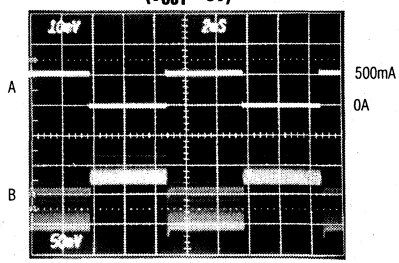
LINE-TRANSIENT RESPONSE
(V_{OUT} = 5V)



5ms/div

I_{OUT} = 500mA, V_{OUT} = 5V
A = V_{IN}, 2.7V TO 4.0V, 1V/div
B = V_{OUT} RIPPLE, 100mV/div, AC-COUPLED

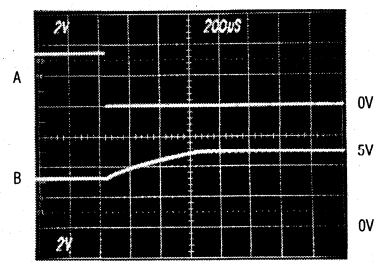
LOAD-TRANSIENT RESPONSE
(V_{OUT} = 5V)



2ms/div

V_{IN} = 2V, V_{OUT} = 5V
A = LOAD CURRENT, 0mA TO 500mA, 500mA/div
B = V_{OUT} RIPPLE, 50mV/div, AC-COUPLED

EXITING SHUTDOWN



200µs/div

I_{OUT} = 500mA, V_{IN} = 3.5V
A = SHDN, 2V/div
B = V_{OUT}, 2V/div

5V or Adjustable, Low-Voltage, Step-Up DC-DC Controller

Pin Description

PIN	NAME	FUNCTION
1	EXT	Gate Drive for External N-Channel Power Transistor
2	OUT	Power-Supply and Voltage-Sense Input. Always connect OUT to circuit output.
3	FB	Feedback Input for Adjustable-Output Operation. Connect to ground for fixed-output operation. Use a resistor divider network to adjust the output voltage. See *Setting the Output Voltage* section.
4	SHDN	Active-High TTL/CMOS Logic-Level Shutdown Input. In shutdown mode, V_{OUT} is a diode drop below the input voltage (due to the DC path from the input voltage to the output). Connect to ground for normal operation.
5	REF	1.5V Reference Output that can source 100µA for external loads. Bypass to GND with 0.1µF. The reference is disabled in shutdown.
6	AGND	Analog Ground
7	GND	High-Current Ground Return for the Output Driver
8	CS	Positive Input to the Current-Sense Amplifier. Connect the current-sense resistor between CS and AGND.

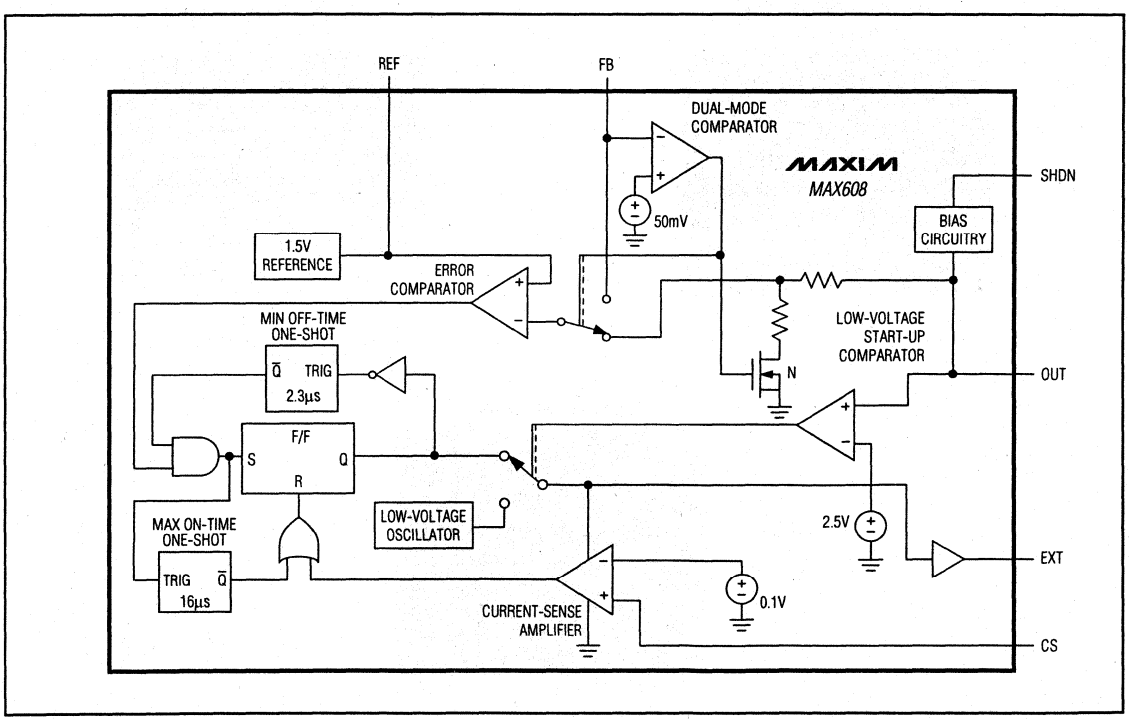


Figure 1. Functional Diagram

5V or Adjustable, Low-Voltage, Step-Up DC-DC Controller

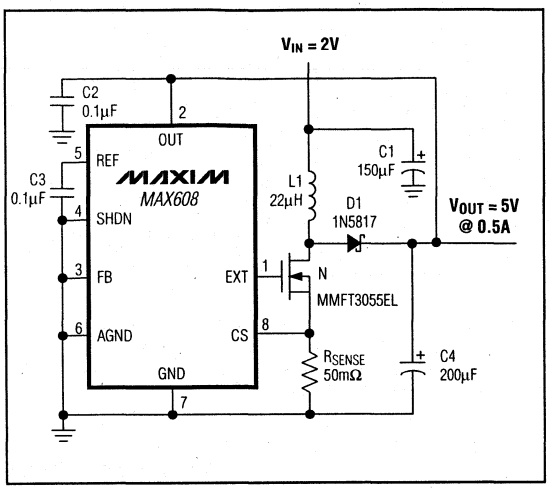


Figure 2a. 5V Preset Output

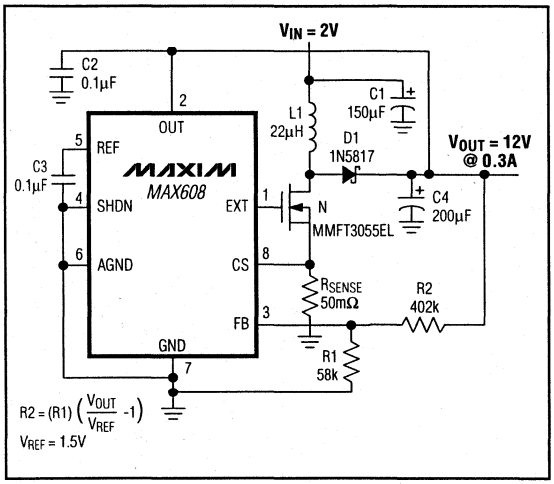


Figure 2b. 12V Output

Detailed Description

The MAX608 is a BiCMOS, step-up, switch-mode power-supply controller that provides a preset 5V output, in addition to adjustable-output operation. Its unique control scheme combines the advantages of pulse-frequency modulation (low supply current) and pulse-width modulation (high efficiency with heavy loads), providing high efficiency over a wide output current range, as well as increased output current capability over previous PFM devices. In addition, the external sense resistor and power transistor allow the user to tailor the output current capability for each application. Figure 1 shows the MAX608 functional diagram. The device has a shutdown mode that reduces the supply current to 5µA max.

Figure 2 shows the standard application circuits. The IC is powered from the output, and the input voltage range is 1.8V to VOUT (this configuration is commonly known as bootstrap operation). The voltage applied to the gate of the external power transistor is switched from VOUT to ground.

The MAX608's output voltage can be set to 5V by connecting FB to ground; it can also be adjusted from 3V to 16.5V using external resistors. Use 1% external feedback resistors when operating in adjustable-output mode (Figures 2b, 2c) to achieve an overall output voltage accuracy of ±5%.

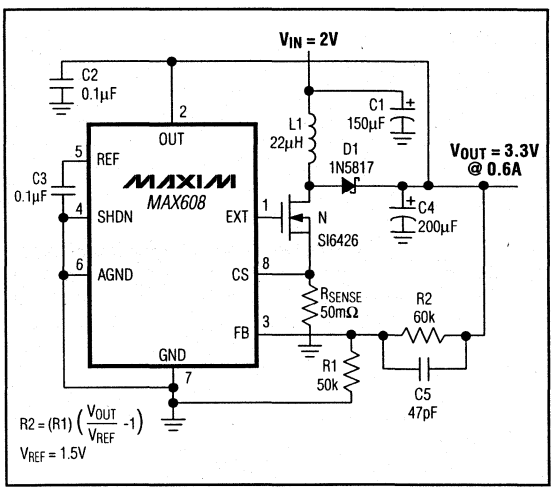


Figure 2c. 3.3V Output

PFM Control Scheme

The MAX608 uses a proprietary current-limited PFM control scheme to provide high efficiency over a wide range of load currents. This control scheme combines the ultra-low supply current of PFM converters (or pulse skippers) with the high full-load efficiency of PWM converters.

5V or Adjustable, Low-Voltage, Step-Up DC-DC Controller

Unlike traditional PFM converters, the MAX608 uses a sense resistor to control the peak inductor current. The device also operates with high switching frequencies (up to 300kHz), allowing the use of miniature external components.

As with traditional PFM converters, the power transistor is not turned on until the voltage comparator senses the output is out of regulation. However, unlike traditional PFM converters, the MAX608 switch uses the combination of a peak current limit and a pair of one-shots that set the maximum on-time (16µs) and minimum off-time (2.3µs); there is no oscillator. Once off, the minimum off-time one-shot holds the switch off for 2.3µs. After this minimum time, the switch either 1) stays off if the output is in regulation, or 2) turns on again if the output is out of regulation.

The control circuitry allows the IC to operate in continuous-conduction mode (CCM) while maintaining high efficiency with heavy loads. When the power switch is turned on, it stays on until either 1) the maximum on-time one-shot turns it off (typically 16µs later), or 2) the switch current reaches the peak current limit set by the current-sense resistor.

The MAX608 switching frequency is variable (depending on load current and input voltage), causing variable switching noise. However, the subharmonic noise generated does not exceed the peak current limit times the filter capacitor equivalent series resistance (ESR). For example, when generating a 5V output at 500mA from a 2V input, only 75mV of output ripple occurs, using the circuit of Figure 2a.

Low-Voltage Start-Up Oscillator

The MAX608 features a low input voltage start-up oscillator that guarantees start-up with no load for input voltages down to 1.8V. At these low voltages, the output voltage is not large enough for proper error-comparator operation and internal biasing. The start-up oscillator has a fixed 50% duty cycle and the MAX608 disregards the error-comparator output when the output voltage is less than 2.5V. Above 2.5V, the error-comparator and normal one-shot timing circuitry are used.

Shutdown Mode

When SHDN is high, the MAX608 enters shutdown mode. In this mode, the internal biasing circuitry is turned off (including the reference), and V_{OUT} falls to a diode drop below V_{IN} (due to the DC path from the input to the output). In shutdown mode, the supply current drops to less than 5µA. SHDN is a TTL/CMOS logic-level input. Connect SHDN to GND for normal operation.

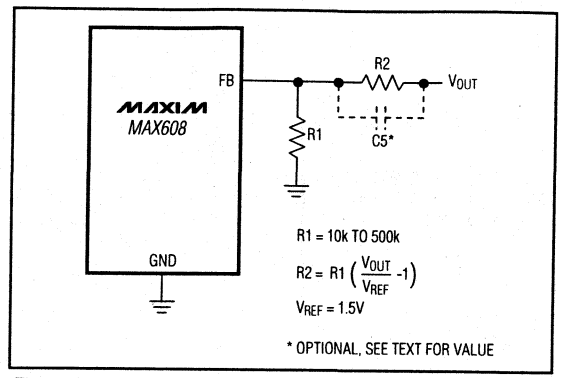


Figure 3. Adjustable Output Circuit

Design Procedure

Setting the Output Voltage

The MAX608's output voltage is preset to 5V (FB = 0V), or it can be adjusted from 16.5V down to 3V using external resistors R1 and R2, configured as shown in Figure 3. For adjustable-output operation, select feedback resistor R1 in the 10kΩ to 500kΩ range. R2 is given by:

$$R2 = (R1)\left(\frac{V_{OUT}}{V_{REF}} - 1\right)$$

where V_{REF} equals 1.5V.

OUT must always be connected to the circuit output.

Figure 2 shows various circuit configurations for preset/adjustable operation.

Determining R_{SENSE}

Use the theoretical output current curves shown in Figures 4a–4d to select R_{SENSE}. They are derived using the minimum (worst-case) current-limit comparator threshold value over the extended temperature range (-40°C to +85°C). No tolerance was included for R_{SENSE}. The voltage drop across the diode is assumed to be 0.5V, and the drop across the power switch $r_{DS(ON)}$ and coil resistance is assumed to be 0.3V.

Determining the Inductor (L)

Practical inductor values range from 10µH to 300µH. 22µH is a good choice for most applications. In applications with large input/output differentials, the IC's output-current capability will be much less when the inductance value is too low, because the IC will always operate in discontinuous mode. If the inductor value is too low, the

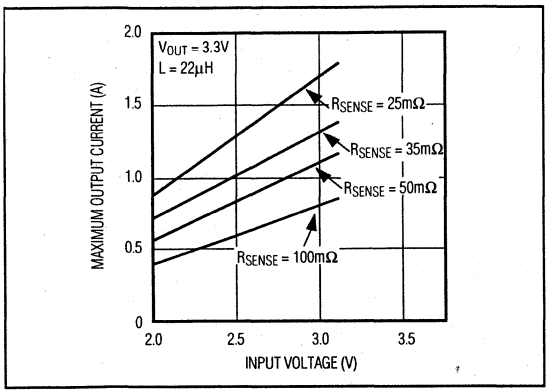


Figure 4a. Maximum Output Current vs. Input Voltage (V_{OUT} = 3.3V)

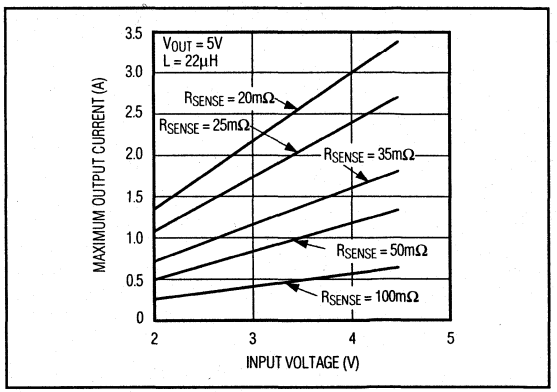


Figure 4b. Maximum Output Current vs. Input Voltage (V_{OUT} = 5V)

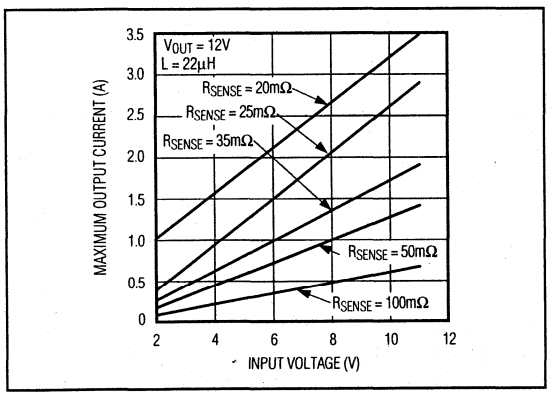


Figure 4c. Maximum Output Current vs. Input Voltage (V_{OUT} = 12V)

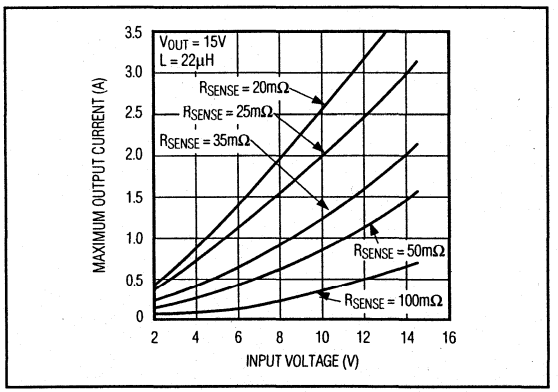


Figure 4d. Maximum Output Current vs. Input Voltage (V_{OUT} = 15V)

current will ramp up to a high level before the current-limit comparator can turn off the switch. The minimum on-time for the switch (t_{ON}(min)) is approximately 2µs; select an inductor that allows the current to ramp up to I_{LIM}.

The standard operating circuits use a 22µH inductor. If a different inductance value is desired, select L such that:

$$L \geq \frac{V_{IN}(max) \times 2\mu s}{I_{LIM}}$$

Larger inductance values tend to increase the start-up time slightly, while smaller inductance values allow the coil current to ramp up to higher levels before the switch turns off, increasing the ripple at light loads.

Inductors with a ferrite core or equivalent are recommended; powder iron cores are not recommended for use with high switching frequencies. Make sure the inductor's saturation current rating (the current at which the core begins to saturate and the inductance starts to fall) exceeds the peak current rating set by R_{SENSE}. However, it is generally acceptable to bias the inductor into saturation by approximately 20% (the point where the inductance is 20% below the nominal value). For highest efficiency, use a coil with low DC resistance, preferably under 20mΩ. To minimize radiated noise, use a toroid, a pot core, or a shielded coil.

Table 1 lists inductor suppliers and specific recommended inductors.

5V or Adjustable, Low-Voltage, Step-Up DC-DC Controller

Power Transistor Selection

Use an N-channel MOSFET power transistor with the MAX608.

Use logic-level or low-threshold N-FETs to ensure the external N-channel MOSFET (N-FET) is turned on completely and that start-up occurs. N-FETs provide the highest efficiency because they do not draw any DC gate-drive current.

When selecting an N-FET, some important parameters to consider are the total gate charge (Q_g), on-resistance ($r_{DS(ON)}$), reverse transfer capacitance (C_{RSS}), maximum drain to source voltage (V_{DS} max), maximum gate to source voltage (V_{GS} max), and minimum threshold voltage (V_{TH} min).

Q_g takes into account all capacitances associated with charging the gate. Use the typical Q_g value for best results; the maximum value is usually grossly overspecified since it is a guaranteed limit and not the measured value. The typical total gate charge should be 50nC or less. With larger numbers, the EXT pins may not be able to adequately drive the gate. The EXT rise/fall time varies with different capacitive loads as shown in the *Typical Operating Characteristics*.

The two most significant losses contributing to the N-FET's power dissipation are I^2R losses and switching losses. Select a transistor with low $r_{DS(ON)}$ and low C_{RSS} to minimize these losses.

Determine the maximum required gate-drive current from the Q_g specification in the N-FET data sheet.

Select an N-FET with a $BV_{DSS} > V_{OUT}$, $BV_{GSS} > V_{OUT}$, and a minimum V_{TH} of 0.5V below the minimum input voltage.

When using a power supply that decays with time (such as a battery), the N-FET transistor will operate in its linear region when the voltage at EXT approaches the threshold voltage of the FET, dissipating excessive power. Prolonged operation in this mode may damage the FET. To avoid this condition, make sure V_{EXT} is above the V_{TH} of the FET, or use a voltage detector (such as the MAX8211) to put the IC in shutdown mode once the input supply voltage falls below a predetermined minimum value. Excessive loads with low input voltages can also cause this condition.

The MAX608's maximum allowed switching frequency during normal operation is 300kHz. However, at start-up, the maximum frequency can be 500kHz, so the maximum current required to charge the N-FET's gate is f(max) x Q_g(typ). Use the typical Q_g number from the transistor data sheet. For example, the MMFT3055EL has a Q_g(typ) of 7nC (at V_{GS} = 5V), therefore the current required to charge the gate is:

$$I_{GATE}\,(max) = (500kHz)\,(7nC) = 3.5mA.$$

Figure 2a's application circuit uses a 4-pin MMFT3055EL surface-mount N-FET that has 150mΩ on-resistance with 4.5V V_{GS}, and a guaranteed V_{TH} of less than 2V. Figure 2c's application circuit uses an Si6426DQ logic-level N-FET with a threshold voltage (V_{TH}) of 1V.

Diode Selection

The MAX608's high switching frequency demands a high-speed rectifier. Schottky diodes such as the 1N5817–1N5822 are recommended. Make sure the Schottky diode's average current rating exceeds the peak current limit set by R_{SENSE}, and that its breakdown voltage exceeds V_{OUT}. For high-temperature applications, Schottky diodes may be inadequate due to their high leakage currents; high-speed silicon diodes such as the MUR105 or EC11FS1 can be used instead. At heavy loads and high temperatures, the benefits of a Schottky diode's low forward voltage may outweigh the disadvantage of high leakage current.

Capacitor Selection

Output Filter Capacitor

The primary criterion for selecting the output filter capacitor (C4) is low effective series resistance (ESR). The product of the peak inductor current and the output filter capacitor's ESR determines the amplitude of the ripple seen on the output voltage. Two OS-CON 100µF, 16V output filter capacitors in parallel with 35mΩ of ESR each typically provide 75mV ripple when stepping up from 2V to 5V at 500mA (Figure 2a). Smaller-value and/or higher-ESR capacitors are acceptable for light loads or in applications that can tolerate higher output ripple.

Since the output filter capacitor's ESR affects efficiency, use low-ESR capacitors for best performance. See Table 1 for component selection.

Input Bypass Capacitors

The input bypass capacitor (C1) reduces peak currents drawn from the voltage source and also reduces noise caused by the switching action of the MAX608 at the voltage source. The input voltage source impedance determines the size of the capacitor required at the OUT input. As with the output filter capacitor, a low-ESR capacitor is recommended. For output currents up to 1A, 150µF (C1) is adequate, although smaller bypass capacitors may also be acceptable.

Bypass the IC with a 0.1µF ceramic capacitor (C2) placed as close as possible to the OUT and GND pins.

Reference Capacitor

Bypass REF with a 0.1µF capacitor (C3). REF can source up to 100µA of current for external loads.

PRODUCTION	INDUCTORS	CAPACITORS	TRANSISTORS	DIODES
Surface Mount	Sumida CD54 series CDR125 series Coiltronics CTX20 series Coilcraft DO3316 series DO3340 series	Matsuo 267 series Sprague 595D series AVX TPS series Sanyo OS-CON series	Siliconix Si9410DY Si4410DY Si6426DQ Si6946DQ Motorola MTP3055EL MTD20N03HDL MMFT3055ELT1	Central Semiconductor CMPSH-3 CMPZ5240 Nihon EC11 FS1 series (high-speed silicon) Motorola MBRS1100T3 MMBZ5240BL
Through Hole	Sumida RCH855 series RCH110 series	Sanyo OS-CON series Nichicon PL series		Motorola 1N5817–1N5822 MUR105 (high-speed silicon)

Feed-Forward Capacitor

When adjusting the output voltage, it may be necessary to parallel a 47pF to 220pF capacitor across R2, as shown in Figures 2 and 3. Choose the lowest capacitor value that insures stability; high capacitance values may degrade line regulation.

Applications Information

Starting Up Under Load

The *Typical Operating Characteristics* show the Start-Up Voltage vs. Load Current graphs for 5V and 12V output voltages. These graphs depend on the type of power switch used. The MAX608 is not designed to start up under full load with low input voltages.

Layout Considerations

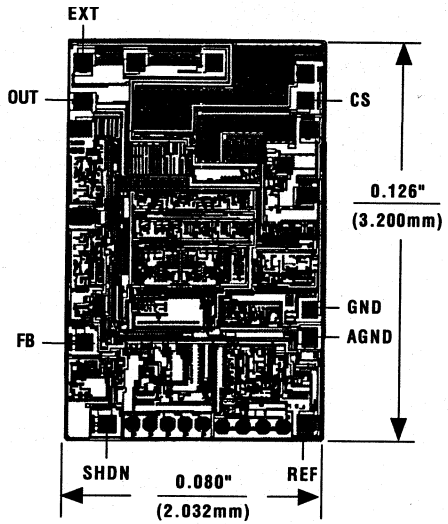
Due to high current levels and fast switching waveforms, which radiate noise, proper PC board layout is essential. Protect sensitive analog grounds by using a star ground configuration. Minimize ground noise by connecting GND, the input bypass capacitor ground lead, and the output filter capacitor ground lead to a single point (star ground configuration). Also, minimize lead lengths to reduce stray capacitance, trace resistance, and radiated noise. Place input bypass capacitor C2 as close as possible to OUT and GND.

If an external resistor divider is used (Figures 2 and 3), the trace from FB to the resistors must be extremely short.

SUPPLIER	PHONE	FAX
AVX	USA: (803) 448-9411	(803) 448-1943
Central Semiconductor	USA: (516) 435-1110	(516) 435-1824
Coilcraft	USA: (708) 639-6400	(708) 639-1469
Coiltronics	USA: (561) 241-7876	(561) 241-9339
Matsuo	USA: (714) 969-2491 Japan: 81-6-337-6450	(714) 960-6492 81-6-337-6456
Motorola	USA: (800) 521-6274	(602) 952-4190
Nichicon	USA: (708) 843-7500	(708) 843-2798
Nihon	USA: (805) 867-2555	(805) 867-2556
Sanyo	USA: (619) 661-6835 Japan: 81-7-2070-1005	(619) 661-1055 81-7-2070-1174
Siliconix	USA: (800) 554-5565	(408) 970-3950
Sprague	USA: (603) 224-1961	(603) 224-1430
Sumida	USA: (708) 956-0666 Japan: 81-3-3607-5111	(708) 956-0702 81-3-3607-5144

5V or Adjustable, Low-Voltage, Step-Up DC-DC Controller

Chip Topography



TRANSISTOR COUNT: 501
SUBSTRATE CONNECTED TO OUT

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

10/96

MAXIM

3.3V/5V or Adjustable, Step-Up/Down DC-DC Converters

General Description

The MAX710/MAX711 integrate a step-up DC-DC converter with a linear regulator to provide step-up/down voltage conversion. They are optimized for battery applications where the input varies above and below the regulated output voltage. They have an input range from 1.8V to 11V.

The on-board P-channel linear regulator follows a high-efficiency (85% typical) step-up converter. The MAX710/MAX711 can be set in two modes using the N/$\overline{E}$ pin: one optimized for lowest noise, the other for highest efficiency. Shutdown control turns off the part completely, disconnecting the input from the output. Standby control turns off only the step-up converter, providing maximum efficiency when using the linear regulator.

The MAX710 has a preset 3.3V or 5V output voltage. The MAX711 has an adjustable output that can be set from 2.7V to 5V with two resistors. Both devices come in 16-pin narrow SO packages.

Applications

Single-Cell Lithium-Powered Portable Devices

Digital Cameras

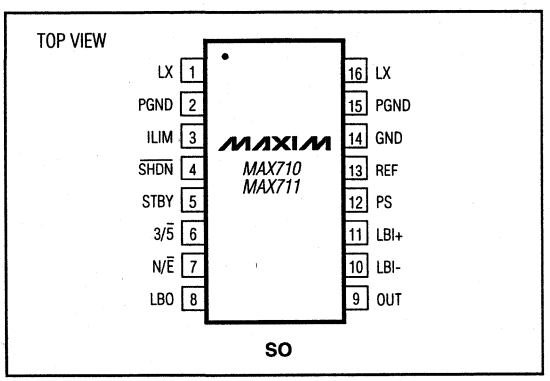
2 AA Alkaline Hand-Held Equipment

3.3V and Other Low-Voltage Systems

3-Cell and 4-Cell Battery-Powered Equipment

Battery-Powered Devices with AC Input Adapters

Pin Configuration



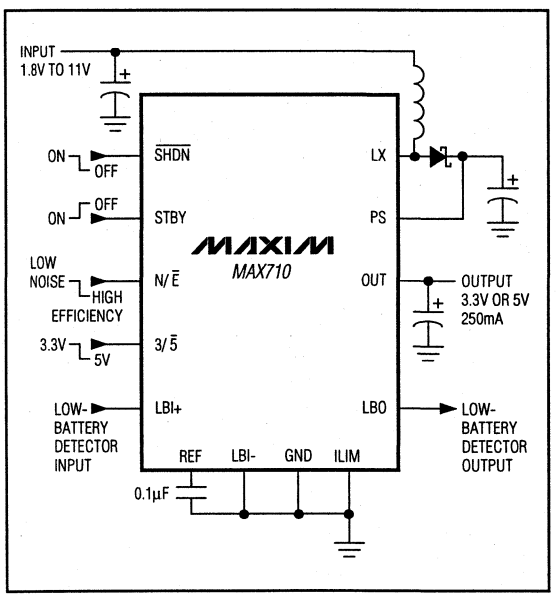
Features

- **Step-Up/Down Function**
- **1.8V to 11V Input Range**
- **250mA Output Current**
- **No External FETs Required**
- **Output is Fully Off During Shutdown**
- **Less than 125µA Battery Drain when On (no load)**
- **1µA Battery Drain when Off**
- **Low-Noise and High-Efficiency Modes**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX710C/D	0°C to +70°C	Dice
MAX710ESE	-40°C to +85°C	16 Narrow SO
MAX711C/D	0°C to +70°C	Dice
MAX711ESE	-40°C to +85°C	16 Narrow SO

Typical Operating Circuit



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

10/96

MAXIM

High-Accuracy, Step-Down Controller with Synchronous Rectifier for CPU Power

General Description

The MAX798 high-performance, step-down DC-DC converter provides main CPU power in battery-powered systems. This buck controller achieves 96% efficiency by using synchronous rectification and Maxim's proprietary Idle Mode™ control scheme to extend battery life at full-load (up to 10A) and no-load outputs. The MAX798's high accuracy meets the demanding requirements of the latest generation CPUs. Excellent dynamic response corrects output transients caused by the latest dynamic-clock CPUs within five 300kHz clock cycles. Unique bootstrap circuitry drives inexpensive N-channel MOSFETs, reducing system cost and eliminating the crowbar switching currents found in some PMOS/NMOS switch designs.

The MAX798 has a logic-controlled and synchronizable fixed-frequency pulse-width-modulating (PWM) operating mode, which reduces noise and RF interference in sensitive mobile-communications and pen-entry applications. The $\overline{SKIP}$ override input allows automatic switchover to idle-mode operation (for high-efficiency pulse skipping) at light loads, or forces fixed-frequency mode for lowest noise at all loads.

The MAX798 is available in a 16-pin narrow SO package.

Applications

Notebook and Subnotebook Computers

PDAs and Mobile Communicators

Features

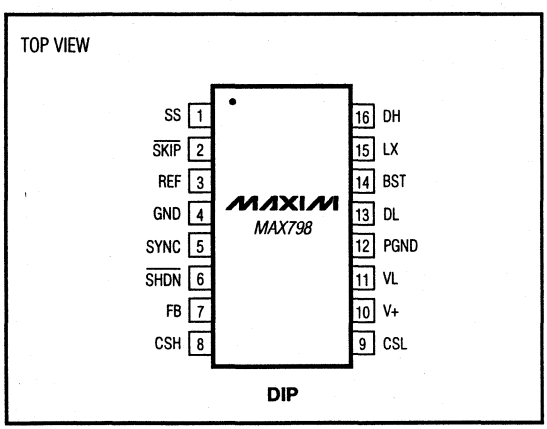
- ♦ **96% Efficiency**
- ♦ **+4.5V to +30V Input Range**
- ♦ **1.6V to 6V Adjustable Precision Output**
- ♦ **±0.4% Max Total Load-Regulation Error**
- ♦ **0.06%/V Max Line-Regulation Error**
- ♦ **5V Linear-Regulator Output**
- ♦ **Precision 2.505V Reference Output**
- ♦ **Automatic Bootstrap Circuit**
- ♦ **150kHz/300kHz Fixed-Frequency PWM Operation**
- ♦ **Programmable Soft-Start**
- ♦ **375µA Quiescent Current (V_{IN} = 12V, V_{OUT} = 5V)**
- ♦ **1µA Shutdown Current**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX798C/D	0°C to +70°C	Dice*
MAX798ESE	-40°C to +85°C	16 Narrow SO

**Contact factory for dice specifications.*

Pin Configuration



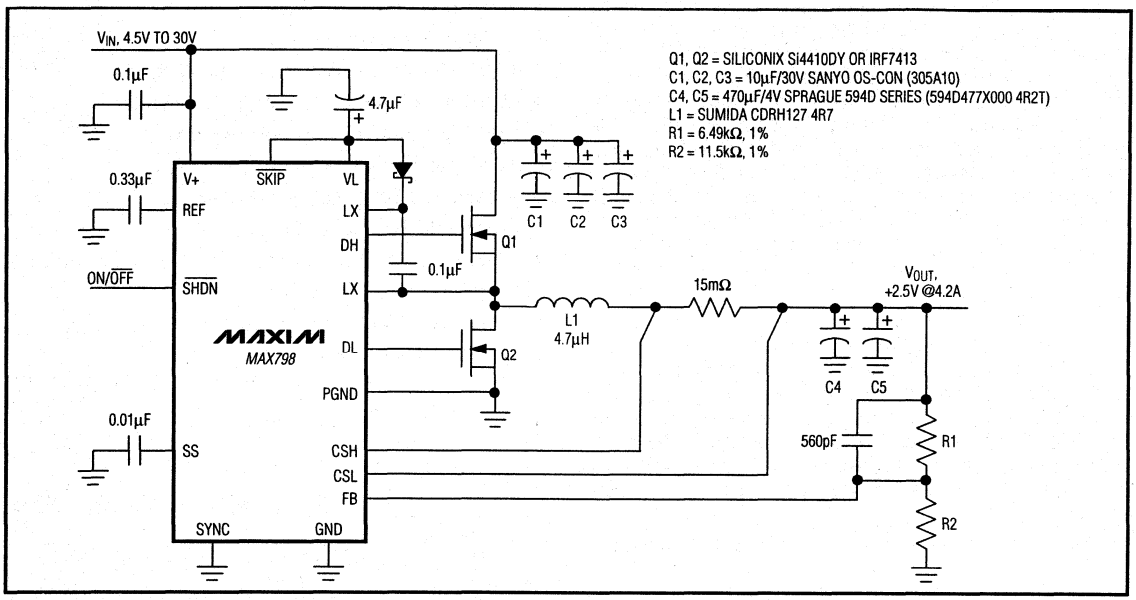
Idle Mode is a trademark of Maxim Intergrated Products.

†U.S. and foreign patents pending.

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

High-Accuracy, Step-Down Controller with Synchronous Rectifier for CPU Power

Typical Application Circuit



19-0495; Rev 1; 7/96

MAXIM

Switched-Capacitor Voltage Inverters

General Description

The ultra-small MAX828/MAX829 monolithic, CMOS charge-pump inverters accept input voltages ranging from +1.5V to +5.5V. The MAX828 operates at 12kHz, and the MAX829 operates at 35kHz. Their high efficiency (greater than 90% over most of the load-current range) and low operating current (60µA for the MAX828) make these devices ideal for both battery-powered and board-level voltage-conversion applications.

The MAX828/MAX829 combine low quiescent current and high efficiency. Oscillator control circuitry and four power MOSFET switches are included on-chip. Applications include generating a -5V supply from a +5V logic supply to power analog circuitry. Both parts come in a 5-pin SOT23-5 package and can deliver 25mA with a voltage drop of 500mV.

For applications requiring more power, the MAX860 delivers up to 50mA with a voltage drop of 600mV, in a space-saving µMAX package.

Applications

Small LCD Panels
Cell Phones
Medical Instruments
Handy-Terminals, PDAs
Battery-Operated Equipment

Features

- **5-Pin SOT23-5 Package**
- **95% Voltage Conversion Efficiency**
- **Inverts Input Supply Voltage**
- **60µA Quiescent Current (MAX828)**
- **+1.5V to +5.5V Input Voltage Range**
- **Requires Only Two Capacitors**
- **25mA Output Current**

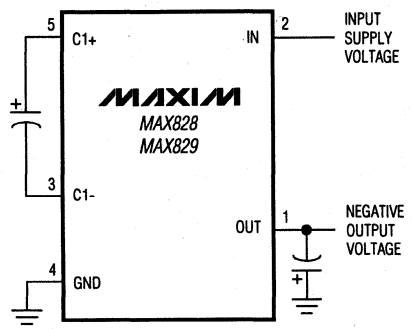
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX828C/D	0°C to +70°C	Dice*
MAX828EUK	-40°C to +85°C	5 SOT23-5
MAX829C/D	0°C to +70°C	Dice*
MAX829EUK	-40°C to +85°C	5 SOT23-5

** Dice are tested at T_A = +25°C.*

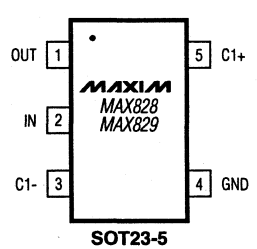
4

Typical Operating Circuit



NEGATIVE VOLTAGE CONVERTER

Pin Configuration



SOT23-5

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Switched-Capacitor Voltage Inverters

ABSOLUTE MAXIMUM RATINGS

IN to GND .....+6.0V, -0.3V
OUT to GND .....-6.0V, +0.3V
OUT Output Current 50mA
OUT Short-Circuit to GND .....Indefinite
Continuous Power Dissipation (T_A = +70°C)
SOT23-5 (derate 7.1mW/°C above +70°C).....571mW

Operating Temperature Range
MAX828EUK/MAX829EUK .....-40°C to +85°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = +5V, C1 = C2 = 10µF (MAX828), C1 = C2 = 3.3µF (MAX829), T_A = 0°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current	T_A = +25°C	MAX828		60	90	µA
		MAX829		150	260	
Minimum Supply Voltage	R_{LOAD} = 10kΩ	T_A = +25°C	1.25	1.0		V
		T_A = 0°C to + 85°C	1.5			
Maximum Supply Voltage	R_{LOAD} = 10kΩ				5.5	V
Oscillator Frequency	T_A = +25°C	MAX828	8.4	12	15.6	kHz
		MAX829	24.5	35	45.5	
Power Efficiency	R_{LOAD} = 10kΩ, T_A = +25°C			98		%
Voltage Conversion Efficiency	R_{LOAD} = ∞		95	99.9		%
Output Resistance	I_{OUT} = 5mA	T_A = +25°C		20	50	Ω
		T_A = 0°C to + 85°C			65	

Note 1: Capacitor contribution is approximately 20% of the output impedance [ESR + 1 / (pump frequency x capacitance)].

ELECTRICAL CHARACTERISTICS

(V_{IN} = +5V, C1 = C2 = 10µF (MAX828), C1 = C2 = 3.3µF (MAX829), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

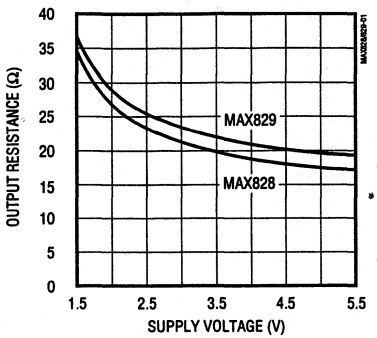
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	MAX828			115	µA
	MAX829			325	
Supply Voltage Range	R_{LOAD} = 10kΩ	1.5		5.5	V
Oscillator Frequency	MAX828	6		20	kHz
	MAX829	19		54.3	
Output Resistance	I_{OUT} = 5mA			65	Ω

Note 2: All -40°C to +85°C specifications above are guaranteed by design.

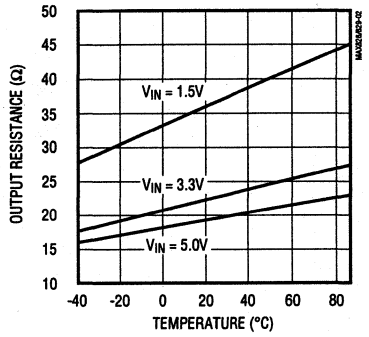
Typical Operating Characteristics

(Circuit of Figure 1, V_{IN} = +5V, C1 = C2 = C3, T_A = +25°C, unless otherwise noted.)

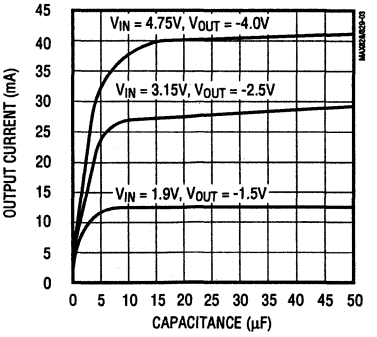
OUTPUT RESISTANCE vs. SUPPLY VOLTAGE



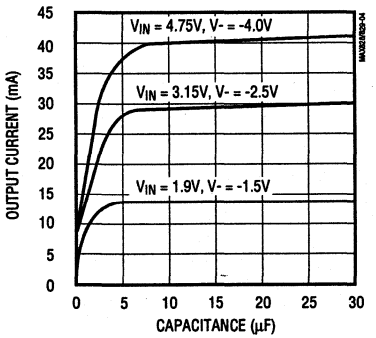
OUTPUT RESISTANCE vs. TEMPERATURE



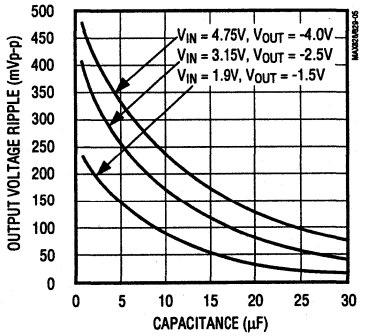
MAX828 OUTPUT CURRENT vs. CAPACITANCE



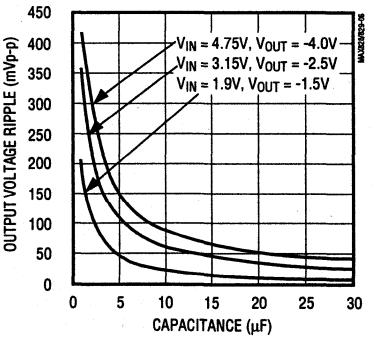
MAX829 OUTPUT CURRENT vs. CAPACITANCE



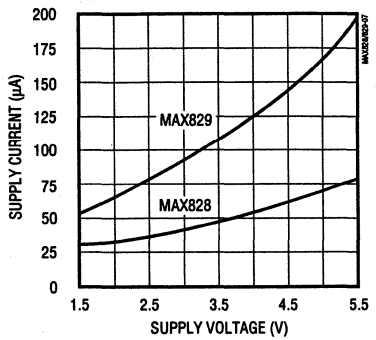
MAX828 OUTPUT VOLTAGE RIPPLE vs. CAPACITANCE



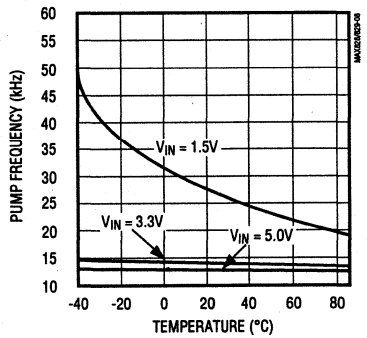
MAX829 OUTPUT VOLTAGE RIPPLE vs. CAPACITANCE



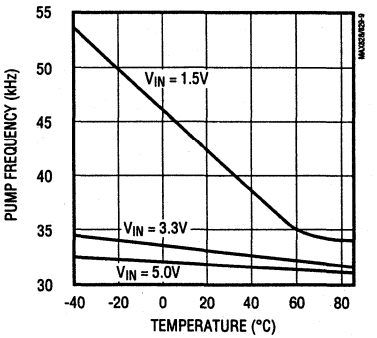
SUPPLY CURRENT vs. SUPPLY VOLTAGE



MAX828 PUMP FREQUENCY vs. TEMPERATURE



MAX829 PUMP FREQUENCY vs. TEMPERATURE

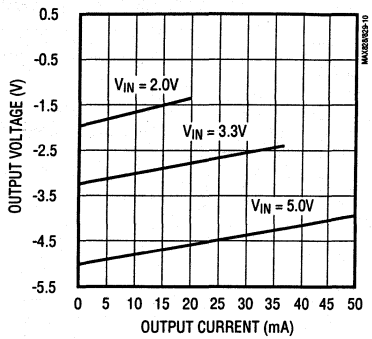


Switched-Capacitor Voltage Inverters

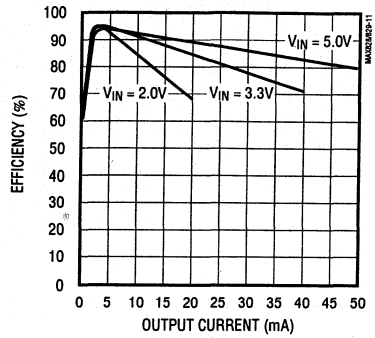
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = +5V, C1 = C2 = C3, T_A = +25°C, unless otherwise noted.)

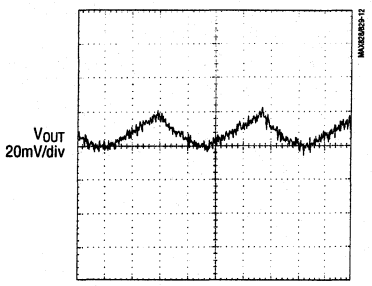
OUTPUT VOLTAGE vs. OUTPUT CURRENT



EFFICIENCY vs. OUTPUT CURRENT

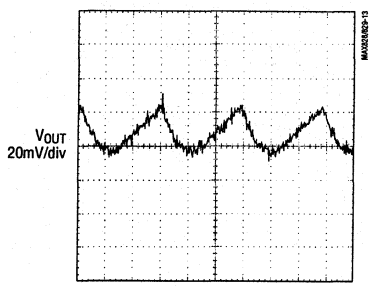


MAX828 OUTPUT NOISE AND RIPPLE



V_{IN} = 3.3V, V_{OUT} = -3.2V, I_{OUT} = 5mA, AC COUPLED

MAX829 OUTPUT NOISE AND RIPPLE



V_{IN} = 3.3V, V_{OUT} = -3.2V, I_{OUT} = 5mA, AC COUPLED

Pin Description

PIN	NAME	FUNCTION
1	OUT	Inverting Charge-Pump Output
2	IN	Positive Power-Supply Input
3	C1-	Flying Capacitor's Negative Terminal
4	GND	Ground
5	C1+	Flying Capacitor's Positive Terminal

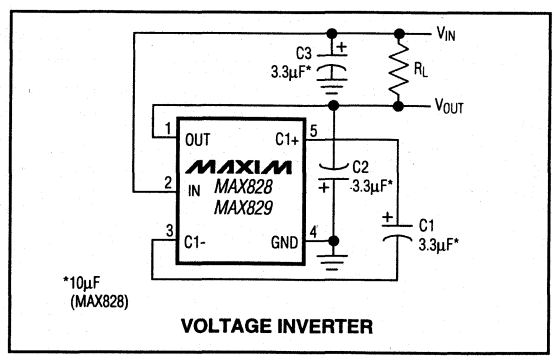


Figure 1. Test Circuit

Detailed Description

The MAX828/MAX829 capacitive charge pumps invert the voltage applied to their input. For highest performance, use low equivalent series resistance (ESR) capacitors.

During the first half-cycle, switches S2 and S4 open, switches S1 and S3 close, and capacitor C1 charges to the voltage at IN (Figure 2). During the second half-cycle, S1 and S3 open, S2 and S4 close, and C1 is level shifted downward by V_{IN} volts. This connects C1 in parallel with the reservoir capacitor C2. If the voltage across C2 is smaller than the voltage across C1, then charge flows from C1 to C2 until the voltage across C2 reaches $-V_{IN}$. The actual voltage at the output is more positive than $-V_{IN}$, since switches S1–S4 have resistance and the load drains charge from C2.

Charge-Pump Output

The MAX828/MAX829 are not voltage regulators: the charge pump's output source resistance is approximately 20Ω at room temperature (with V_{IN} = +5V), and V_{OUT} approaches -5V when lightly loaded. V_{OUT} will droop toward GND as load current increases. The droop of the negative supply (V_{DROOP-}) equals the current draw from OUT (I_{OUT}) times the negative converter's source resistance (RS-):

$$V_{DROOP-} = I_{OUT} \times RS-$$

The negative output voltage will be:

$$V_{OUT} = -(V_{IN} - V_{DROOP-})$$

Efficiency Considerations

The power efficiency of a switched-capacitor voltage converter is affected by three factors: the internal losses in the converter IC, the resistive losses of the pump capacitors, and the conversion losses during charge transfer between the capacitors. The total power loss is:

$$\Sigma P_{LOSS} = P_{INTERNAL\ LOSSES} + P_{SWITCH\ LOSSES} + P_{PUMP\ CAPACITOR\ LOSSES} + P_{CONVERSION\ LOSSES}$$

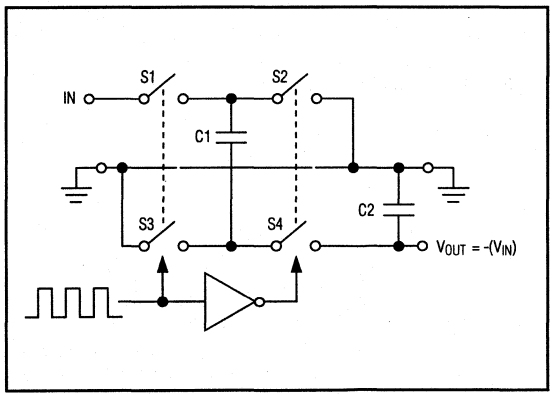


Figure 2. Ideal Voltage Inverter

The internal losses are associated with the IC's internal functions, such as driving the switches, oscillator, etc. These losses are affected by operating conditions such as input voltage, temperature, and frequency.

The next two losses are associated with the voltage converter circuit's output resistance. Switch losses occur because of the on-resistance of the MOSFET switches in the IC. Charge-pump capacitor losses occur because of their ESR. The relationship between these losses and the output resistance is as follows:

$$P_{PUMP\ CAPACITOR\ LOSSES} + P_{CONVERSION\ LOSSES} = I_{OUT}^2 \times R_{OUT}$$

$$R_{OUT} \cong \frac{1}{(f_{OSC}) \times C1} + 4(2R_{SWITCHES} + ESR_{C1}) + ESR_{C2}$$

where f_{OSC} is the oscillator frequency. The first term is the effective resistance from an ideal switched-capacitor circuit. See Figures 3a and 3b.

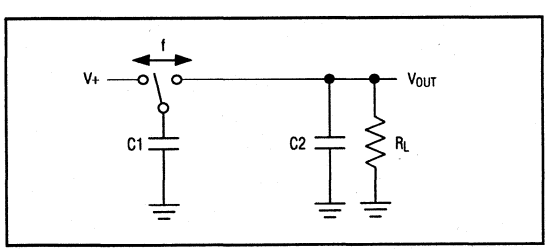


Figure 3a. Switched-Capacitor Model

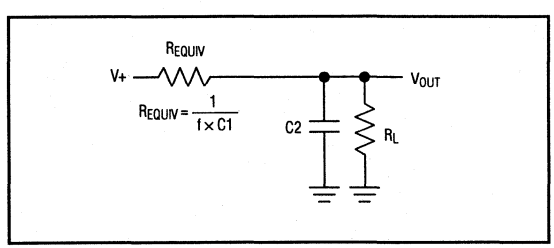


Figure 3b. Equivalent Circuit

Switched-Capacitor Voltage Inverters

Conversion losses occur during the charge transfer between C1 and C2 when there is a voltage difference between them. The power loss is:

$$P_{CONV.LOSS} = [1/2\,C1\,(V_{IN}^2 - V_{OUT}^2) + 1/2\,C2\,(V_{RIPPLE}^2 - 2V_{OUT}V_{RIPPLE})] \times f_{OSC}$$

Applications Information

Capacitor Selection

To maintain the lowest output resistance, use capacitors with low ESR (Table 1). The charge-pump output resistance is a function of C1's and C2's ESR. Therefore, minimizing the charge-pump capacitor's ESR minimizes the total output resistance.

Flying Capacitor (C1)

Increasing the flying capacitor's size reduces the output resistance. Small C1 values increase the output resistance. Above a certain point, increasing C1's capacitance has a negligible effect, because the output resistance becomes dominated by the internal switch resistance and capacitor ESR.

Output Capacitor (C2)

Increasing the output capacitor's size reduces the output ripple voltage. Decreasing its ESR reduces both output resistance and ripple. Smaller capacitance values can be used with light loads if higher output ripple can be tolerated. Use the following equation to calculate the peak-to-peak ripple:

$$V_{RIPPLE} = \frac{I_{OUT}}{f_{OSC} \times C2} + 2 \times I_{OUT} \times ESR_{C2}$$

Input Bypass Capacitor

Bypass the incoming supply to reduce its AC impedance and the impact of the MAX828/MAX829's switching noise. The recommended bypassing depends on the circuit configuration and on where the load is connected.

When the inverter is loaded from OUT to GND, current from the supply switches between 2 x I_{OUT} and zero. Therefore, use a large bypass capacitor (e.g., equal to the value of C1) if the supply has a high AC impedance.

When the inverter is loaded from IN to OUT, the circuit draws 2 x I_{OUT} constantly, except for short switching spikes. A 0.1µF bypass capacitor is sufficient.

Voltage Inverter

The most common application for these devices is a charge-pump voltage inverter (Figure 1). This application requires only two external components—capacitors C1 and C2—plus a bypass capacitor, if necessary. Refer to the *Capacitor Selection* section for suggested capacitor types and values.

Cascading Devices

Two devices can be cascaded to produce an even larger negative voltage (Figure 4). The unloaded output voltage is normally -2 x V_{IN}, but this is reduced slightly by the output resistance of the first device multiplied by the quiescent current of the second. When cascading more than two devices, the output resistance rises dramatically. For applications requiring larger negative voltages, see the MAX864 and MAX865 data sheets.

Paralleling Devices

Paralleling multiple MAX828s or MAX829s reduces the output resistance. Each device requires its own pump capacitor (C1), but the reservoir capacitor (C2) serves all devices (Figure 5). Increase C2's value by a factor of n, where n is the number of parallel devices. The equation for calculating output resistance is also shown in Figure 5.

Combined Doubler/Inverter

In the circuit of Figure 6, capacitors C1 and C2 form the inverter, while C3 and C4 form the doubler. C1 and C3 are the pump capacitors; C2 and C4 are the reservoir

Table 1. Low-ESR Capacitor Manufacturers

MANUFACTURER		PHONE	FAX	DEVICE TYPE
AVX		(803) 946-0690 (800) 282-4975	(803) 626-3123	Surface-mount, TPS series
Matsuo		(714) 969-2491	(714) 960-6492	Surface-mount, 267 series
Sanyo	USA	(619) 661-6835	(619) 661-1055	Through-hole, OS-CON series
	Japan	81-7-2070-6306	81-7-2070-1174	
Sprague		(603) 224-1961	(603) 224-1430	Surface-mount, 595D series

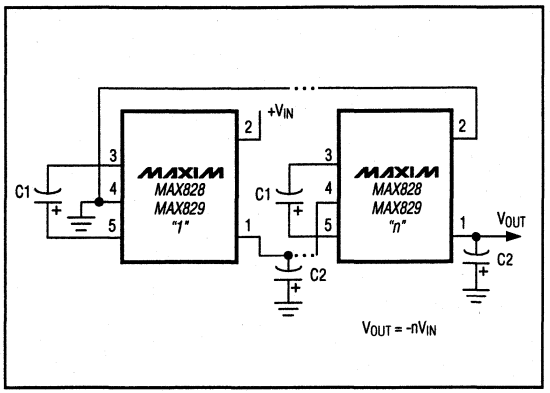


Figure 4. Cascading MAX828s or MAX829s to Increase Output Voltage

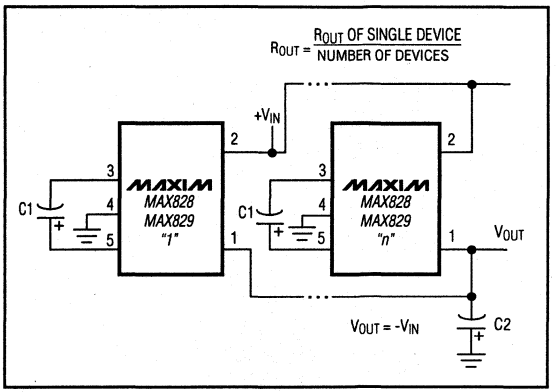


Figure 5. Paralleling MAX828s or MAX829s to Reduce Output Resistance

capacitors. Because both the inverter and doubler use part of the charge-pump circuit, loading either output causes both outputs to decline toward GND. Make sure the sum of the currents drawn from the two outputs does not exceed 40mA.

Heavy Output Current Loads

When under heavy loads, where higher supply is sourcing current into OUT, the OUT supply must not be pulled above ground. Applications that sink heavy current into OUT require a Schottky diode (1N5817) between GND and OUT, with the anode connected to OUT (Figure 7).

Layout and Grounding

Good layout is important, primarily for good noise performance. To ensure good layout, mount all components as close together as possible, keep traces short to minimize parasitic inductance and capacitance, and use a ground plane.

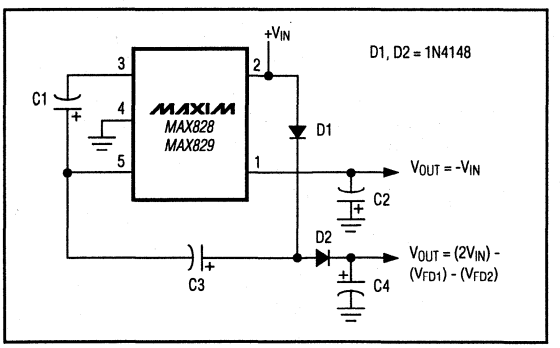


Figure 6. Combined Doubler and Inverter

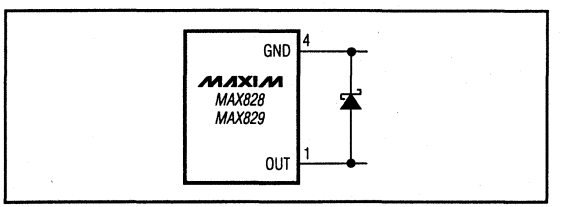
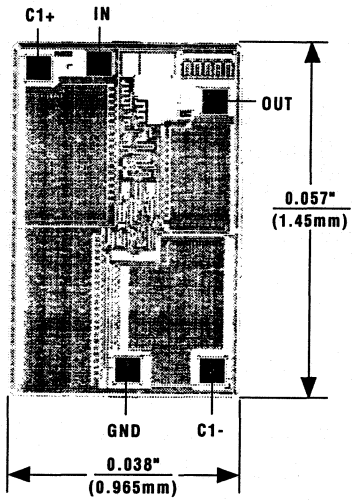


Figure 7. High V- Load Current

Switched-Capacitor Voltage Inverters

Chip Topography



TRANSISTOR COUNT: 58

SUBSTRATE CONNECTED TO IN

19-1121; Rev 0; 9/96

EVALUATION KIT AVAILABLE

MAXIM

Cost-Saving Multichemistry Battery-Charger System

General Description

The MAX846A is a cost-saving multichemistry battery-charger system that comes in a space-saving 16-pin QSOP. This integrated system allows different battery chemistries (Li-Ion, NiMH or NiCd cells) to be charged using one circuit.

In its simplest application, the MAX846A is a stand-alone, current-limited float voltage source that charges Li-Ion cells. It can also be paired up with a low-cost microcontroller (µC) to build a universal charger capable of charging Li-Ion, NiMH, and NiCd cells.

An internal 0.5%-accurate reference allows safe charging of Li-Ion cells that require tight voltage accuracy. The voltage- and current-regulation loops used to control a low-cost external PNP transistor (or P-channel MOSFET) are independent of each other, allowing more flexibility in the charging algorithms.

The MAX846A has a built-in 1%, 3.3V, 20mA linear regulator capable of powering the µC and providing a reference for the µC's analog-to-digital converters. An on-board reset notifies the controller upon any unexpected loss of power. The µC can be inexpensive, since its only functions are to monitor the voltage and current and to change the charging algorithms.

Applications

Li-Ion Battery Packs

Desktop Cradle Chargers

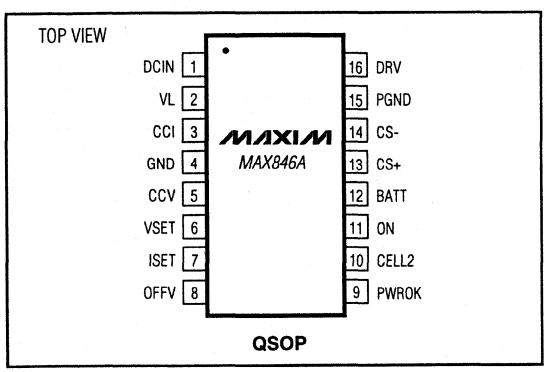
Li-Ion/NiMH/NiCd Multichemistry Battery Chargers

Cellular Phones

Notebook Computers

Hand-Held Instruments

Pin Configuration



Features

- ♦ **Multichemistry Charger System (Li-Ion, NiMH, NiCd)**
- ♦ **Independent Voltage and Current Loops**
- ♦ **±0.5% Internal Reference for Li-Ion Cells**
- ♦ **Lowers Cost:**
  - **—Stands Alone or Uses Low-Cost µC**
  - **—Built-In 1% Linear Regulator Powers µC**
  - **—Linear Regulator Provides Reference to µC ADCs**
  - **—Built-In µC Reset**
  - **—Controls Low-Cost External PNP Transistor or P-Channel MOSFET**
- ♦ **Space-Saving 16-Pin QSOP**
- ♦ **Charging-Current-Monitor Output**
- ♦ **<1µA Battery Drain when Off**

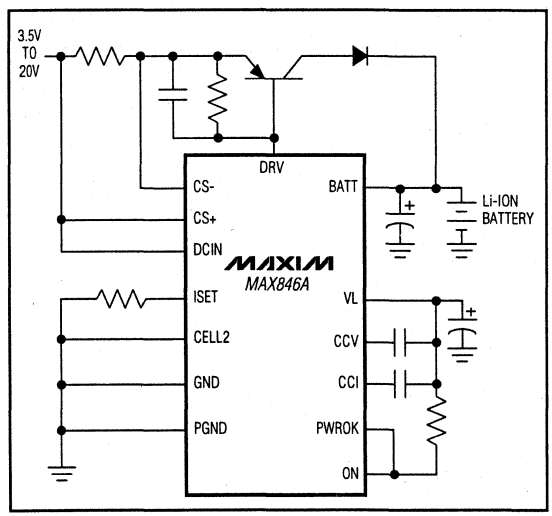
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX846AC/D	0°C to +70°C	Dice*
MAX846AEEE	-40°C to +85°C	16 QSOP

Dice are tested at T_A = +25°C only. Contact factory for details.

4

Typical Operating Circuit



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Cost-Saving Multichemistry Battery-Charger System

ABSOLUTE MAXIMUM RATINGS

DCIN, DRV, CS+, CS-, BATT to GND .....-0.3V, +21V
PGND to GND .....±0.3V
VL to GND .....-0.3V, 7V
I_{PWROK} 10mA
PWROK, ISET, CCI, CCV, OFFV, VSET,
CELL2, ON to GND .....-0.3V, VL + 0.3V
CS+ to CS- .....±0.3V
VL Short to GND .....Continuous
I_{DRV} 100mA

Continuous Power Dissipation (T_A = +70°C)
QSOP (derate 8.3mW/°C above +70°C) 667mW
Operating Temperature Range
MAX846AEEE .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DCIN} = 10V, ON = VL, I_{VL} = I_{VSET} = 0mA, V_{CS-} = V_{CS+} = 10V, V_{BATT} = 4.5V, V_{OFFV} = V_{CELL2} = 0V, T_A = 0°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VL REGULATOR					
DCIN Supply Current	V_{DCIN} = 20V, I_{DRV} = I_{VL} = 0mA			5	mA
Operating Range		3.7		20.0	V
Output Voltage	0mA < I_{VL} < 20mA, 3.7V < V_{DCIN} < 20V	3.267	3.305	3.333	V
Short-Circuit Current Limit	VL = GND		50		mA
PWROK Trip Level	Rising VL edge, 2% hysteresis	2.9	3.0	3.1	V
VL Undervoltage-Lockout Level		2.5		2.9	V
REFERENCE					
Output Voltage	Measured at VSET, I_{VSET} = 0mA, V_{ON} = 0V	-0.5%	1.650	+ 0.5%	V
Output Resistance		-2%	20	+ 2%	kΩ
CURRENT-SENSE AMPLIFIER					
Transconductance	V_{ISET} = 1.7V, V_{CS+} - V_{CS-} = 165mV	0.95	1	1.05	mA/V
Output Offset Current	V_{CS+} = 4V			3	µA
Input Common-Mode Range	Measured at V_{CS-}, V_{CS+} - V_{CS-} = 165mV	2.1		20.0	V
Maximum Differential Input Voltage	V_{CS-} = V_{ISET} = 2.1V, CSA transconductance >0.9mA/V	225			mV
CS- Lockout Voltage	When V_{CS-} is less than this voltage, DRV is disabled.	1.9		2.1	V
CS+, CS- Input Current	V_{CS+} = 20V, V_{CS+} -V_{CS-} = 165mV			250	µA
CS+, CS- Off Input Current	DCIN = VL = ON = GND		0.01	10	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DCIN} = 10V, ON = VL, I_{VL} = I_{VSET} = 0mA, V_{CS-} = V_{CS+} = 10V, V_{BATT} = 4.5V, V_{OFFV} = V_{CELL2} = 0V, T_A = 0°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VOLTAGE LOOP					
Voltage-Loop Set Point	V_{VSET} = 1.650V, V_{CELL2} = 0V, I_{DRV} = 1mA, V_{DRV} = 10V	-0.25%	4.2	+ 0.25%	V
	V_{VSET} = 1.650V, V_{CELL2} = VL, I_{DRV} = 1mA, V_{DRV} = 10V	-0.25%	8.4	+ 0.25%	
VSET Common-Mode Input Range		1.25		2.0	V
CCV Output Impedance			150		kΩ
Voltage-Loop Load Regulation	1mA < I_{DRV} < 5mA		0.05		%
BATT Input Current	V_{BATT} = 10V, CELL2 = GND or VL			225	µA
BATT Off Input Current	V_{BATT} = 10V, ON = GND, CELL2 = GND or VL		0.01	1	µA
CURRENT LOOP					
Current-Loop Set Point	I_{DRV} = 5mA, V_{DRV} = 10V	1.634	1.650	1.666	V
CA Voltage Gain			5		V/V
CCI Output Impedance			50		kΩ
Overcurrent Trip Level	When V_{ISET} exceeds this voltage, DRV current is disabled.	1.90		2.1	V
DRIVER					
DRV Sink Current	V_{DRV} = 3V	20			mA
DRV Off Current	V_{DRV} = 20V, V_{ON} = 0V		0.1	100	µA
LOGIC INPUTS AND OUTPUTS					
Input High Level	CELL2, ON, OFFV	2.4		VL	V
Input Low Level	CELL2, ON, OFFV	0		0.8	V
Input Current	CELL2, ON, OFFV		0.01	1	µA
PWROK Output Low Level	I_{PWROK} = 1mA, V_{DCIN} = V_{VL} = 2.5V			0.4	V
PWROK Output High Leakage	V_{PWROK} = 3.3V		0.01	1	µA

Cost-Saving Multichemistry Battery-Charger System

ELECTRICAL CHARACTERISTICS (Note 1)

(V_{DCIN} = 10V, ON = VL, I_{VL} = I_{VSET} = 0mA, V_{CS-} = V_{CS+} = 10V, V_{BATT} = 4.5V, V_{OFFV} = V_{CELL2} = 0V, T_A = -40°C to +85°C, unless otherwise noted.)

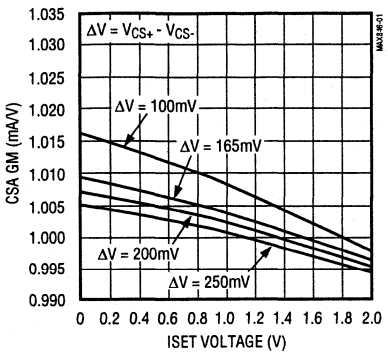
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VL REGULATOR					
DCIN Supply Current	V_{DCIN} = 20V, I_{DRV} = I_{VL} = 0mA			5	mA
Output Voltage	0mA < I_{VL} < 20mA, 3.7V < V_{DCIN} < 20V	3.259		3.341	V
PWROK Trip Level	Rising VL edge, 2% hysteresis	2.9		3.1	V
VL Undervoltage-Lockout Level		2.5		3.0	V
REFERENCE					
Output Voltage	Measured at VSET, I_{VSET} = 0mA, V_{ON} = 0V	-0.7%	1.650	+ 0.7%	V
Output Resistance		-2%	20	+ 2%	kΩ
CURRENT-SENSE AMPLIFIER					
Transconductance	V_{ISET} = 1.7V, V_{CS+} - V_{CS-} = 165mV	0.93		1.07	mA/V
Output Offset Current	V_{CS+} = 4V			5	µA
CS+, CS- Off Input Current	V_{ON} = 0V, V_{CS+} = V_{CS-} = 10V			10	µA
VOLTAGE LOOP					
Voltage-Loop Set Point	V_{VSET} = 1.650V, V_{CELL2} = 0V, I_{DRV} = 1mA, V_{DRV} = 10V	-0.35%	4.2	+ 0.35%	V
	V_{VSET} = 1.650V, V_{CELL2} = VL, I_{DRV} = 1mA, V_{DRV} = 10V	-0.35%	8.4	+ 0.35%	
BATT Off Input Current	V_{BATT} = 10V, ON = GND, CELL2 = GND or VL			1	µA
CURRENT LOOP					
Current-Loop Set Point	I_{DRV} = 5mA, V_{DRV} = 10V	1.625		1.675	V
Overcurrent Trip Level	When V_{ISET} exceeds this voltage, DRV current is disabled.	1.86		2.14	V
DRIVER					
DRV Sink Current	V_{DRV} = 3V	20			mA
DRV Off Current	V_{DRV} = 20V, ON = GND			100	µA

Note 1: Specifications to -40°C are guaranteed by design and not production tested.

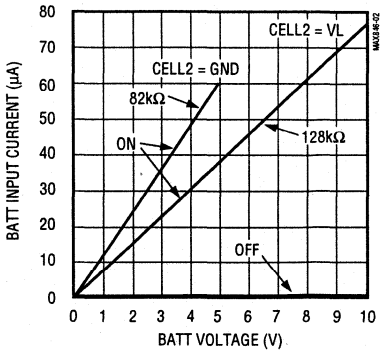
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

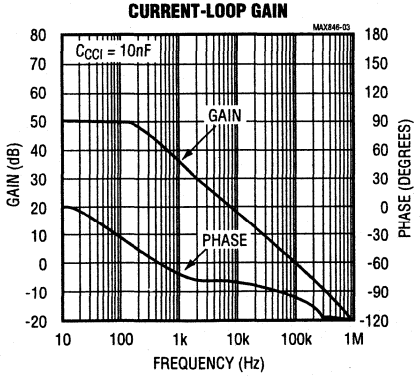
CURRENT-SENSE AMPLIFIER TRANSCONDUCTANCE vs. ISET VOLTAGE



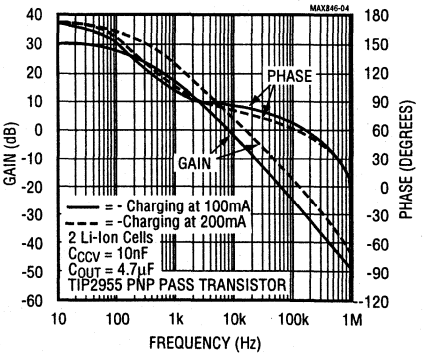
BATTERY INPUT CURRENT vs. BATTERY VOLTAGE



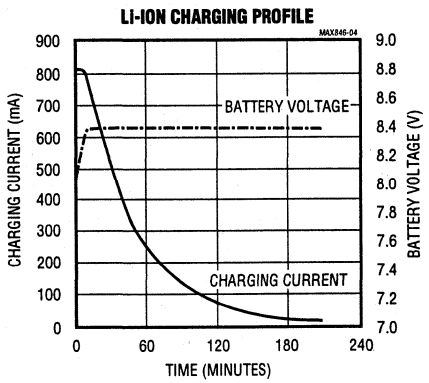
CURRENT-LOOP GAIN



VOLTAGE-LOOP GAIN



LI-ION CHARGING PROFILE



Cost-Saving Multichemistry Battery-Charger System

Pin Description

PIN	NAME	FUNCTION
1	DCIN	Supply Input from External DC Source. 3.7V ≤ V_{DCIN} ≤ 20V.
2	VL	3.3V, 20mA, 1% Linear-Regulator Output. VL powers the system µC and other components. Bypass to GND with a 4.7µF tantalum or ceramic capacitor.
3	CCI	Current-Regulation-Loop Compensation Pin. Connect a compensation capacitor (typically 10nF) from CCI to VL.
4	GND	Ground
5	CCV	Voltage-Regulation-Loop Compensation Pin. Connect a compensation capacitor (typically 10nF) from CCV to VL.
6	VSET	Float-Voltage Reference-Adjust Input. Leave VSET open for a 4.2V default. See the *Applications Information* section for adjustment information.
7	ISET	Current-Set Input/Current-Monitor Output. ISET sets the current-regulation point. Connect a resistor from ISET to GND to monitor the charging current. ISET voltage is regulated at 1.65V by the current-regulation loop. To adjust the current-regulation point, either modify the resistance from ISET to ground or connect a fixed resistor and adjust the voltage on the other side of the resistor (Figure 5). The transconductance of the current-sense amplifier is 1mA/V.
8	OFFV	Logic Input that disables the voltage-regulation loop. Set OFFV high for NiCd or NiMH batteries.
9	PWROK	Open-Drain, Power-Good Output to µC. PWROK is low when VL is less than 3V. The reset timeout period can be set externally using an RC circuit (Figure 3).
10	CELL2	Digital Input. CELL2 programs the number of Li-Ion cells to be charged. A high level equals two cells; a low level equals one cell.
11	ON	Charger ON/OFF Input. When low, the driver section is turned off and I_{BATT} <1µA. The VL regulator is always active.
12	BATT	Battery Input. Connect BATT to positive battery terminal.
13	CS+	Current-Sense Amplifier High-Side Input. Connect CS+ to the sense resistor's power-source side. The sense resistor may be placed on either side of the pass transistor.
14	CS-	Current-Sense Amplifier Low-Side Input. Connect CS- to the sense resistor's battery side.
15	PGND	Power Ground
16	DRV	External Pass Transistor (P-channel MOSFET or PNP) Base/Gate Drive Output. DRV sinks current only.

Detailed Description

The MAX846A battery-charging controller combines three functional blocks: a 3.3V precision, low-dropout linear regulator (LDO), a precision voltage reference, and a voltage/current regulator (Figure 1).

Linear Regulator

The LDO regulator output voltage (VL) is two times the internal reference voltage; therefore, the reference and LDO track. VL delivers up to 20mA to an external load and is short-circuit protected. The power-good output (PWROK) provides microcontroller (µC) reset and charge-current inhibition.

Voltage Reference

The precision internal reference provides a voltage to accurately set the float voltage for lithium-ion (Li-Ion) battery charging. The reference output connects in series with an internal, 2%-accurate, 20kΩ resistor. This allows the float voltage to be adjusted using one external 1% resistor (R_{VSET}) to form a voltage divider (Figure 4). The float-voltage accuracy is important for battery life and to ensure full capacity in Li-Ion batteries. Table 1 shows the accuracies attainable using the MAX846A.

Cost-Saving Multichemistry Battery-Charger System

Voltage/Current Regulator

The voltage/current regulator consists of a precision attenuator, voltage loop, current-sense amplifier, and current loop. The attenuator can be pin programmed to set the regulation voltage for one or two Li-Ion cells (4.2V and 8.4V, respectively). The current-sense amplifier is configured to sense the battery current on the high side. It is, in essence, a transconductance amplifier converting the voltage across an external sense resistor (R_{CS}) to a current, and applying this current to an external load resistor (R_{ISET}). Set the charge current by selecting R_{CS} and R_{ISET}. The charge current can also be adjusted by varying the voltage at the low side of R_{ISET} or by summing/subtracting current from the ISET node (Figure 5). The voltage and current loops are individually compensated using external capacitors at CCV and CCI, respectively. The outputs of these two loops are OR'ed together and drive an open-drain, internal N-channel MOSFET transistor sinking current to ground. An external P-channel MOSFET or PNP transistor pass element completes the loop.

Stability

The *Typical Operating Characteristics* show the loop gains for the current loop and voltage loop. The dominant pole for each loop is set by the compensation capacitor connected to each capacitive compensation pin (CCI, CCV). The DC loop gains are about 50dB for the current loop and about 33dB for the voltage loop, for a battery impedance of 250mΩ.

The CCI output impedance (50kΩ) and the CCI capacitor determine the current-loop dominant pole. In Figure 2, the recommended C_{CCV} is 10nF, which places a dominant pole at 300Hz. There is a high-frequency pole, due to the external PNP, at approximately f_T/β. This pole frequency (on the order of a few hundred kilohertz) will vary with the type of PNP used. Connect a 10nF capacitor between the base and emitter of the PNP to prevent self-oscillation (due to the high-impedance base drive).

Similarly, the CCV output impedance (150kΩ) and the CCV capacitor set the voltage-loop dominant pole. In Figure 2, the compensation capacitance is 10nF, which places a dominant pole at 200Hz.

The battery impedance directly affects the voltage-loop DC and high-frequency gain. At DC, the loop gain is proportional to the battery resistance. At higher frequencies, the AC impedance of the battery and its connections introduces an additional high-frequency zero. A 4.7µF output capacitor in parallel with the battery, mounted close to BATT, minimizes the impact of this impedance. The effect of the battery impedance on DC gain is noticeable in the Voltage-Loop-Gain graph (see *Typical Operating Characteristics*). The solid line represents voltage-loop gain versus frequency for a fully charged battery, when the battery energy level is high and the ESR is low. The charging current is 100mA. The dashed line shows the loop gain with a 200mA charging current, a lower amount of stored energy in the battery, and a higher battery ESR.

Applications Information

Stand-Alone Li-Ion Charger

Figure 2 shows the stand-alone configuration of the MAX846A. Select the external components and pin configurations as follows:

- Program the number of cells: Connect CELL2 to GND for one-cell operation, or to VL for two-cell operation.
- Program the float voltage: Connect a 1% resistor from VSET to GND to adjust the float voltage down, or to VL to adjust it up. If VSET is unconnected, the float voltage will be 4.2V per cell. Let the desired float voltage per cell be V_F, and calculate the resistor value as follows:

Table 1. Float-Voltage Accuracy

ERROR SOURCE	ERROR
Internal-reference accuracy	±0.5%
VSET error due to external divider. Calculated from a 2% internal 20kΩ resistor tolerance and a 1% external R_{VSET} resistor tolerance. The total error is 3% x (adjustment). Assume max adjustment range of 5%.	±0.15%
VSET amplifier and divider accuracy	±0.25%
TOTAL	**±0.9%**

Cost-Saving Multichemistry Battery-Charger System

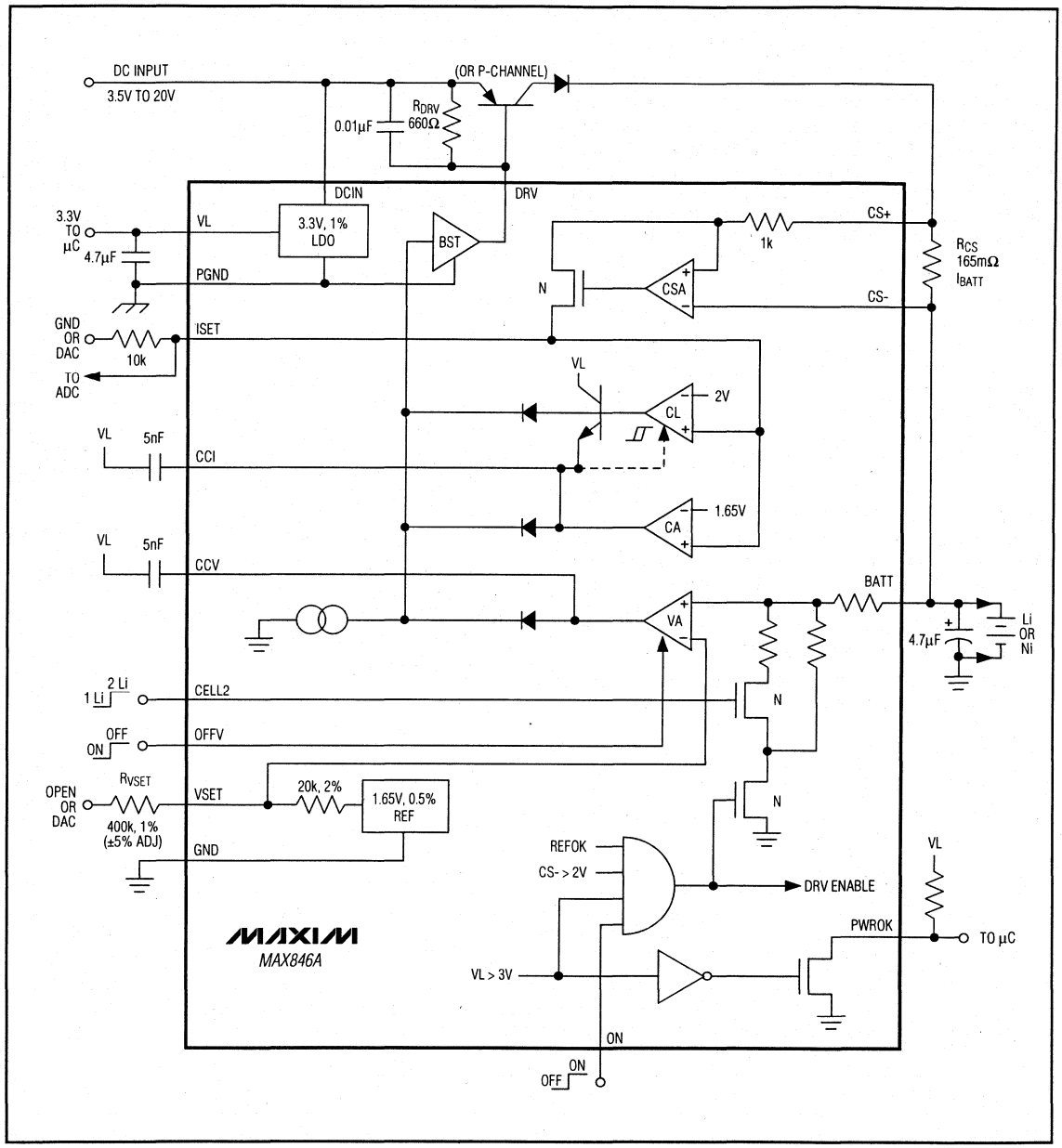


Figure 1. Functional Diagram

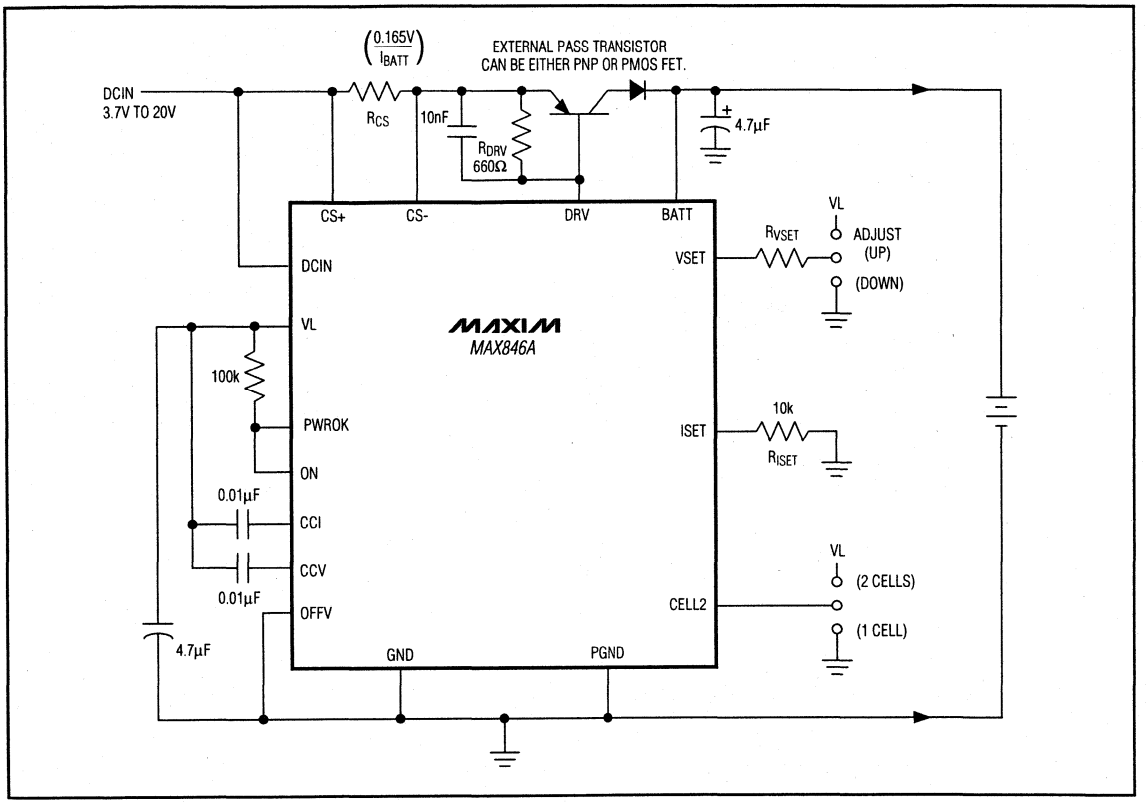


Figure 2. Stand-Alone Li-Ion Charger

$$R_{VSET} = 20k\Omega \left(\frac{\frac{4.2}{1.65} V_X - V_F}{V_F - 4.2} \right)$$

where VX is either GND or VL, and V_F is the per-cell float voltage. In the circuit of Figure 1, R_{VSET} is 400kΩ. R_{VSET} and the internal 20kΩ resistor form a divider, resulting in an adjustment range of approximately ±5%.

The current-regulation loop attempts to maintain the voltage on ISET at 1.65V. Selecting resistor R_{ISET} determines the reflected voltage required at the current-sense amplifier input.

- Calculate R_{CS} and R_{ISET} as follows:

  $R_{CS} = V_{CS} / I_{BATT}$

  R_{ISET} (in kΩ) = 1.65V / V_{CS}

  where the recommended value for V_{CS} is 165mV.

- Connect ON to PWROK to prevent the charge current from turning on until the voltages have settled.

Minimize power dissipation in the external pass transistor. Power dissipation can be controlled by setting the DCIN input supply as low as possible, or by making V_{DCIN} track the battery voltage.

Microprocessor-Controlled Multichemistry Operation

The MAX846A is highly adjustable, allowing for simple interfacing with a low-cost µC to charge Ni-based and Li-Ion batteries using one application circuit (Figure 3).

Cost-Saving Multichemistry Battery-Charger System

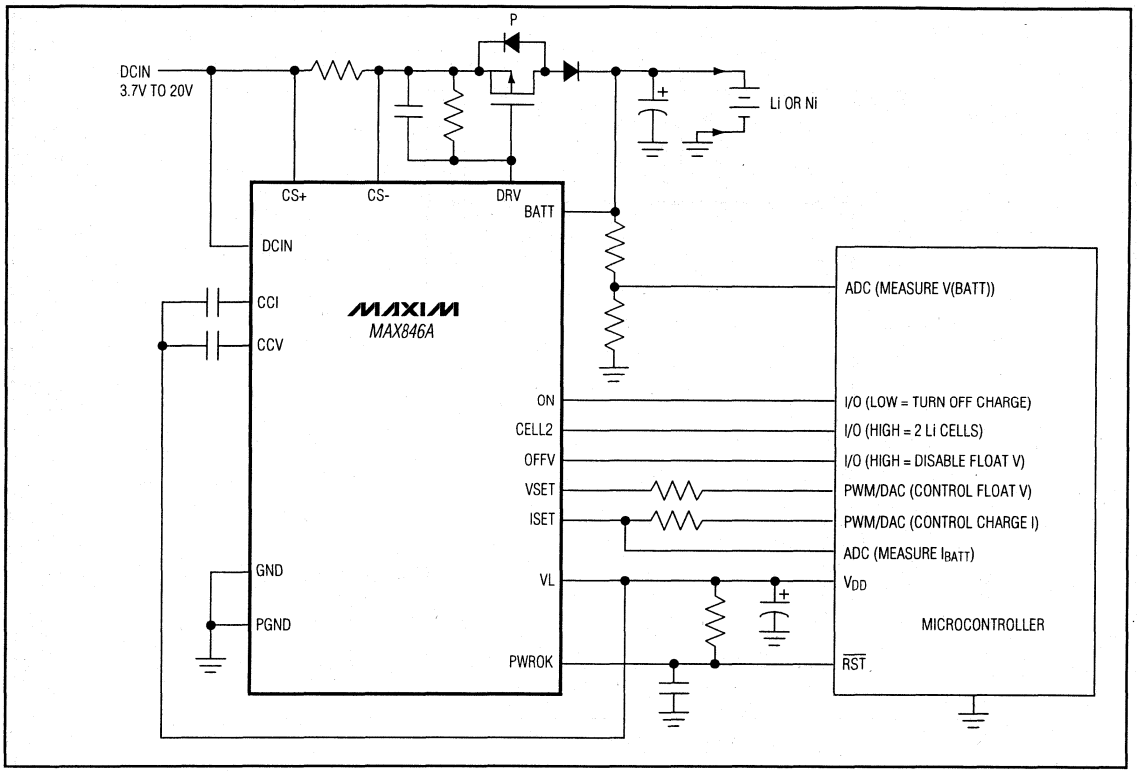


Figure 3. Desktop Multichemistry Charger Concept

Component selection is similar to that of stand-alone operation. By using DACs or µC PWM outputs, the float voltage and charging current can be adjusted by the µC. When a Ni-based battery is being charged, disable the float-voltage regulation using the OFFV input. The µC can also monitor the charge current through the battery by reading the ISET output's voltage using its ADC. Similarly, the battery voltage can be measured using a voltage divider from the battery.

Note that the µC only needs to configure the system for correct voltage and current levels for the battery being charged, and for Ni-based batteries to detect end-of-charge and adjust the current level to trickle. The controller is not burdened with the regulation task.

Float-voltage accuracy is important for battery life and for reaching full capacity for Li-Ion batteries. Table 1 shows the accuracy attainable using the MAX846A.

For best float-voltage accuracy, set the DRV current to 1mA (R_{DRV} = 660Ω for a PNP pass transistor).

High-Power Multichemistry Offline Charger

The circuit in Figure 6 minimizes power dissipation in the pass transistor by providing optical feedback to the input power source. The offline AC/DC converter maintains 1.2V across the PNP. This allows much higher charging currents than can be used with conventional power sources.

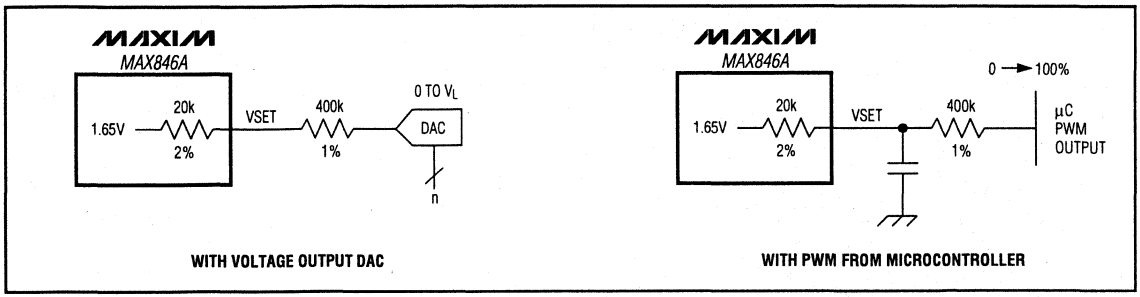


Figure 4. VSET Adjustment Methods

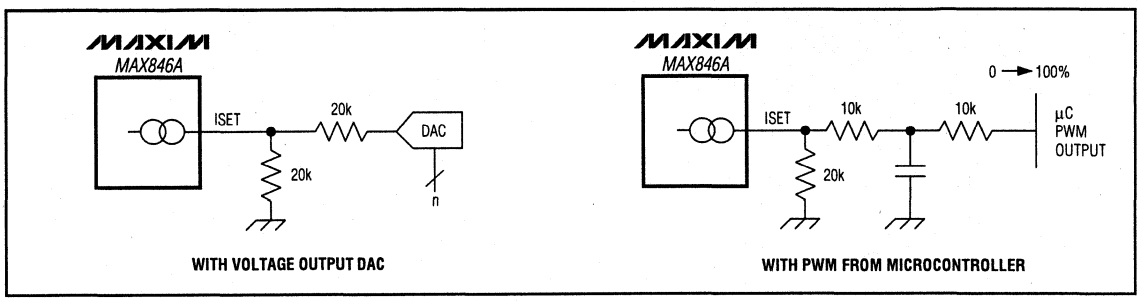


Figure 5. ISET Adjustment Methods

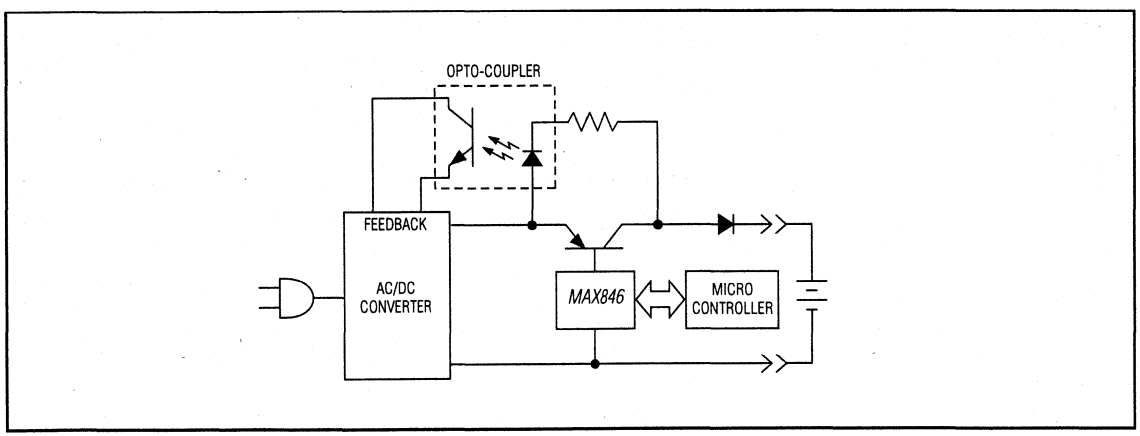
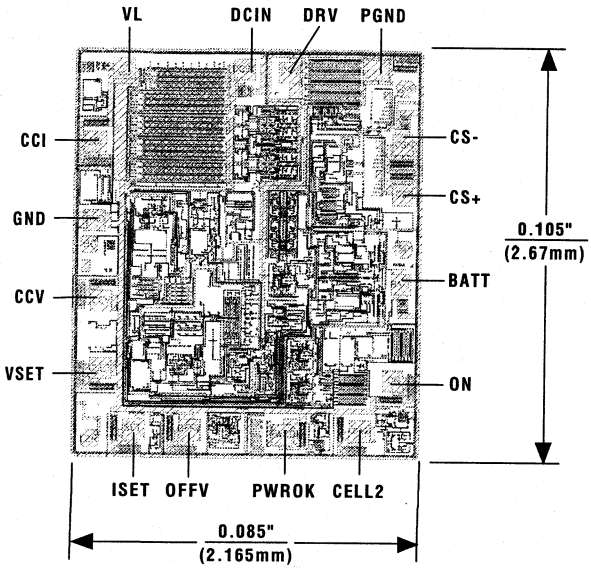


Figure 6. Low-Cost Desktop Multichemistry Charger Concept

Cost-Saving Multichemistry Battery-Charger System

Chip Topography



SUBSTRATE CONNECTED TO GND
TRANSISTOR COUNT: 349

19-1095; Rev 1; 10/96

MAXIM

1-Cell to 3-Cell, High-Power, Low-Noise, Step-Up DC-DC Converters

General Description

The MAX848/MAX849 boost converters set a new standard of high efficiency and high integration for noise-sensitive power-supply applications, such as portable phones and small systems with RF data links. The heart of the these devices is a synchronous boost-topology regulator that generates a fixed 3.3V output (or 2.7V to 5.5V adjustable output) from one to three NiCd/NiMH cells or one Li-Ion cell.

Synchronous rectification provides a 5% efficiency improvement over similar nonsynchronous boost regulators. In standby mode, pulse-skipping PFM operation keeps the output voltage alive with only 150µW quiescent power consumption. Fixed-frequency PWM operation ensures that the switching noise spectrum is limited to the 300kHz fundamental and its harmonics, allowing easy post-filtering noise reduction. For even tighter noise spectrum control, synchronize to a 200kHz to 400kHz external clock.

Battery monitoring is provided by a two-channel, voltage-to-frequency analog-to-digital converter (ADC). One channel is intended for a single-cell battery input (0.625V to 1.875V range), while the other channel is for monitoring higher voltages (0V to 2.5V range).

Two control inputs are provided for push-on, push-off control via a momentary pushbutton switch. Upon power-up, an internal comparator monitors the output voltage to generate a power-good output (POK).

The devices differ only in the current limit of the N-channel MOSFET power switch: 0.8A for the MAX848, and 1.4A for the MAX849.

Features

- ♦ **Up to 95% Efficiency (see *Typical Output Selector Guide* below)**
- ♦ **3.3V Dual Mode™ or 2.7V to 5.5V Adj. Output**
- ♦ **0.7V to 5.5V Input Range**
- ♦ **0.15mW Standby Mode**
- ♦ **300kHz PWM Mode or Synchronizable**
- ♦ **Two-Channel ADC with Serial Output**
- ♦ **Power-Good Function**

Applications

Digital Cordless Phones	PCS Phones
Cellular Phones	Hand-Held Instruments
Palmtop Computers	Personal Communicators
Local 3.3V to 5V Supplies	

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX848ESE	-40°C to +85°C	16 Narrow SO
MAX849ESE	-40°C to +85°C	16 Narrow SO

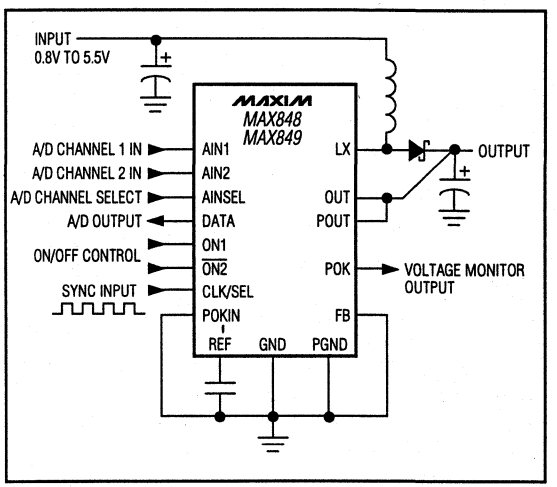
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Typical Output Selector Guide

V_{IN} (V)	V_{OUT} (V)	MAX849 I_{OUT} (mA)	MAX848 I_{OUT} (mA)
0.9	3.3	100	70
	5	70	40
1.2	3.3	300	110
	5	200	70
2.4	3.3	750	200
	5	500	130
2.7	3.3	800	250
	5	600	150
3.6	5	1000	300

Pin Configuration at end of data sheet.
Dual Mode is a trademark of Maxim Integrated Products.

Typical Operating Circuit



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

1-Cell to 3-Cell, High-Power, Low-Noise, Step-Up DC-DC Converters

ABSOLUTE MAXIMUM RATINGS

ON1, $\overline{ON2}$, OUT, POUT to GND .....-0.3V, +6V
PGND to GND .....-0.3V, +0.3V
LX to PGND .....-0.3V, (V_{POUT} + 0.3V)
CLK/SEL, DATA, POKIN, REF,
AINSEL, AIN1, AIN2, FB, POK to GND .....-0.3V, (V_{OUT} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
Narrow SO (derate 8.7mW/°C above +70°C) 696mW

Operating Temperature Range
MAX848ESE/MAX849ESE .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{OUT} = 3.6V, GND = PGND = CLK/SEL = ON1 = $\overline{ON2}$ = AINSEL = AIN1 = AIN2 = FB = POKIN, POUT = OUT, **T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Minimum Operating Voltage (Note 1)					0.7		V
REFERENCE							
Reference Output Voltage	I_{REF} = 0mA			1.23	1.25	1.27	V
REF Load Regulation	-1µA < I_{REF} < 50µA				5	15	mV
REF Supply Rejection	2.5V < V_{OUT} < 5V				0.2	5	mV
DC-DC CONVERTER							
Output Voltage (Note 2)	V_{FB} < 0.1V, CLK/SEL = OUT			3.17	3.34	3.40	V
Output Current	V_{IN} = 1.2V	V_{OUT} = 3.3V	MAX848		110		mA
			MAX849		300		
		V_{OUT} = 5V	MAX848		70		
			MAX849		200		
	V_{IN} = 2.4V	V_{OUT} = 3.3V	MAX848		200		
			MAX849		750		
		V_{OUT} = 5V	MAX848		130		
			MAX849		500		
	V_{IN} = 2.7V	V_{OUT} = 3.3V	MAX848		250		
			MAX849		600		
		V_{OUT} = 5V	MAX848		150		
			MAX849		800		
	V_{OUT} = 5V	MAX848, V_{IN} = 3.3V			300		
		MAX849, V_{IN} = 3.6V			1000		
FB Regulation Voltage	Adjustable output, CLK/SEL = OUT			1.215	1.240	1.265	V
FB Input Current	V_{FB} = 1.25V					200	nA
Output Voltage Adjust Range				2.7		5.5	V
Output Voltage Lockout Range	(Note 3)			2.1		2.4	V
Load Regulation (Note 4)	CLK/SEL = OUT				-1.6		%
Minimum Start-Up Voltage (Note 5)	I_{LOAD} < mA, T_A > +25°C				0.9	1.1	V
Frequency in Start-Up Mode	V_{OUT} = 1.5V			40		300	kHz
Operating Current in Shutdown	Current into OUT pin, $V_{\overline{ON2}}$ = 3.6				4	20	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{OUT} = 3.6V, GND = PGND = CLK/SEL = ON1 = $\overline{ON2}$ = AINSEL = AIN1 = AIN2 = FB = POKIN, POUT = OUT, **T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Current in Low-Power Mode (Note 6)	Current into OUT pin, CLK/SEL = GND			35	90	µA
Operating Current in Low-Noise Mode (Note 6)	Current into OUT pin, CLK/SEL = OUT, does not include switching losses			150	300	µA
DC-DC SWITCHES						
POUT Leakage Current	V_{LX} = 0V, $V_{\overline{ON2}}$ = V_{OUT} = 5.5V			0.1	20	µA
LX Leakage Current	V_{LX} = $V_{\overline{ON2}}$ = V_{OUT} = 5.5V			0.1	20	µA
Switch On-Resistance	N-channel	CLK/SEL = GND		0.3	0.6	Ω
		CLK/SEL = OUT		0.13	0.25	
	P-channel	CLK/SEL = OUT		0.25	0.5	
N-Channel Current Limit	CLK/SEL = OUT	MAX848		0.3	0.6	mA
		MAX849	1100	1350	1600	
	$V_{CLK/SEL}$ = 0V (Note 7)	MAX848	120	200	300	
		MAX849	250	400	550	
ADC						
Data Output Voltage Low	I_{SINK} = 1mA				0.4	V
Data Output Voltage High	I_{SOURCE} = 1mA		V_{OUT} - 0.4			V
AIN1 Input Range	AINSEL = GND		0.625		1.875	V
AIN2 Input Range	AINSEL = OUT		0		2.5	V
AIN1, AIN2 Input Current	f_{CLK} = 400kHz, V_{AIN1} = V_{AIN2} = 2.5V			1	2	µA
Accuracy	f_{CLK} = 400kHz, 5ms conversion, monotonic to 8 bits				±4	% FSR
POWER-GOOD						
Internal Trip Level	Rising V_{OUT}, V_{POKIN} < 0.1V		2.95		3.10	V
External Trip Level	Rising V_{POKIN}		1.225		1.275	V
POK Low Voltage	I_{SINK} = 1mA, V_{OUT} = 3.6V or I_{SINK} = 20µA, V_{OUT} = 1V				0.4	V
POK High Leakage Current	V_{OUT} = V_{POK} = 5.5V			0.01	1	µA
POKIN Leakage Current	V_{POKIN} = 1.5V				50	nA
LOGIC AND CONTROL INPUTS						
Input Low Voltage	1.2V < V_{OUT} < 5.5V, ON1 and $\overline{ON2}$ (Note 8)				0.2V_{OUT}	V
	V_{OUT} = 2.7V, AINSEL and CLK/SEL				0.2V_{OUT}	
Input High Voltage	1.2V < V_{OUT} < 5.5V, ON1 and $\overline{ON2}$ (Note 8)		0.8V_{OUT}			V
	V_{OUT} = 5.5V, AINSEL and CLK/SEL		0.8V_{OUT}			
Logic Input Current	ON1, $\overline{ON2}$, AINSEL and CLK/SEL				1	µA
Internal Oscillator Frequency	CLK/SEL = OUT		260	300	340	kHz
Oscillator Maximum Duty Cycle			80	85	90	%
External Clock Frequency Range			200		400	kHz
CLK/SEL Pulse Width	Not tested		200			ns
CLK/SEL Rise/Fall Time	Not tested				100	ns

1-Cell to 3-Cell, High-Power, Low-Noise, Step-Up DC-DC Converters

ELECTRICAL CHARACTERISTICS

(V_{OUT} = 3.6V, GND = PGND = CLK/SEL = ON1 = $\overline{ON2}$ = AINSEL = AIN1 = AIN2 = FB = POKIN, POUT = OUT, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 9)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
REFERENCE						
Reference Output Voltage	I_{REF} = 0mA		1.225		1.275	V
DC-DC CONVERTER						
Output Voltage (Note 3)	V_{FB} < 0.1V, CLK/SEL = OUT, includes load-regulation error		3.13		3.47	V
FB Regulation Voltage	Adjustable output, CLK/SEL = OUT		1.21		1.27	V
Output Voltage Lockout Range	(Note 3)		2.05		2.45	V
OUT Supply Current in Shutdown	$V_{\overline{ON2}}$ = 3.6V				20	µA
OUT Supply Current in Low-Power Mode (Note 6)	CLK/SEL = GND				90	µA
OUT Supply Current in Low-Noise Mode (Note 6)	CLK/SEL = OUT, does not include switching losses				300	µA
DC-DC SWITCHES						
Switch On-Resistance	N-channel	CLK/SEL = GND			0.6	Ω
		CLK/SEL = OUT			0.25	
	P-channel	CLK/SEL = OUT			0.5	
N-Channel Current Limit	CLK/SEL = OUT	MAX848	600		1100	mA
		MAX849	1100		1800	
	CLK/SEL = GND (Note 7)	MAX848	120		300	
		MAX849	250		550	
ADC						
Accuracy	f_{CLK} = 400kHz, 5ms conversion				±4	% FSR
POWER-GOOD						
Internal Trip Level	Rising V_{OUT}, V_{POKIN} < 0.1V		2.95		3.10	V
External Trip Level	Rising V_{POKIN}		1.225		1.275	V
LOGIC CONTROL INPUTS						
Internal Oscillator Frequency	CLK/SEL = OUT		260		340	kHz
Oscillator Maximum Duty Cycle			80		90	%

Note 1: Minimum operating voltage. Because the MAX848/MAX849 are bootstrapped to the output, it will operate down to a 0.7V input.

Note 2: In low-power mode (CLK/SEL = GND), the output voltage regulates 1% higher than in low-noise mode (CLK/SEL = OUT or synchronized).

Note 3: The part is in start-up mode until it reaches this voltage level. Do not apply full-load current.

Note 4: Load regulation is measured from no load to full load, where full load is determined by the N-channel switch current limit.

Note 5: Start-up is tested with Figure 2's circuit. Output current is measured when the input and output voltages are applied.

Note 6: Supply current from the 3.34V output is measured between the 3.34V output and the OUT pin. This current correlates directly with actual battery supply current, but is reduced in value according to the step-up ratio and efficiency. V_{OUT} = 3.6V to keep the internal switch open when measuring the current into the device.

Note 7: When $V_{CLK/SEL}$ = 0V, the inductor is forced into constant-peak-current, discontinuous operation. This is guaranteed by testing in Figure 2's circuit.

Note 8: ON1 and $\overline{ON2}$ inputs have approximately 0.15V_{OUT} hysteresis.

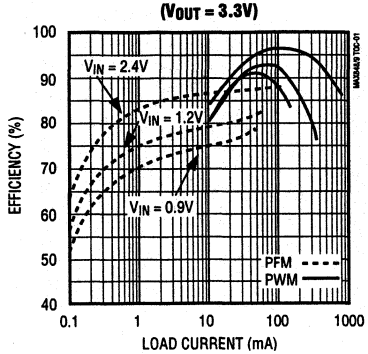
Note 9: Specifications to -40°C are guaranteed by design, not production tested.

1-Cell to 3-Cell, High-Power, Low-Noise, Step-Up DC-DC Converters

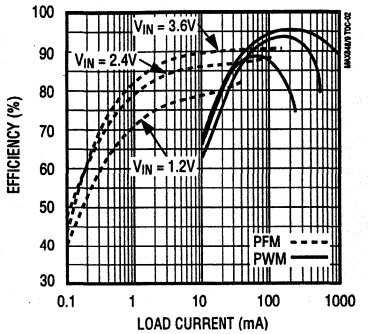
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

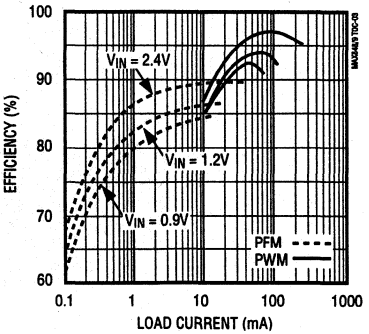
MAX849
EFFICIENCY vs. LOAD CURRENT
(V_{OUT} = 3.3V)



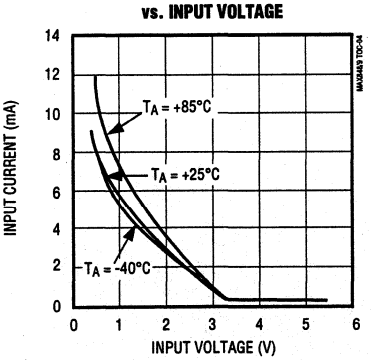
MAX849
EFFICIENCY vs. LOAD CURRENT
(V_{OUT} = 5V)



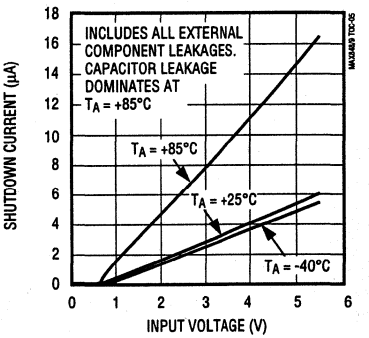
MAX848
EFFICIENCY vs. LOAD CURRENT
(V_{OUT} = 3.3V)



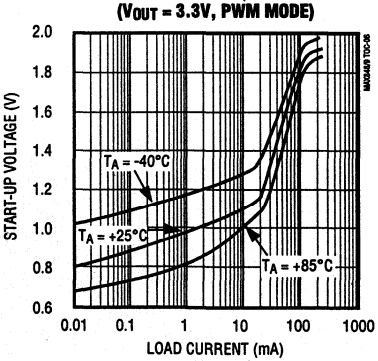
NO-LOAD BATTERY CURRENT
vs. INPUT VOLTAGE



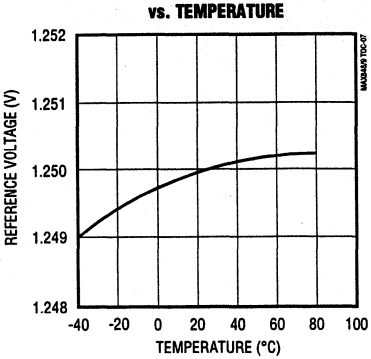
SHUTDOWN CURRENT
vs. INPUT VOLTAGE



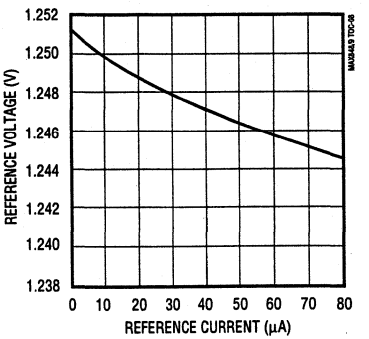
START-UP VOLTAGE vs. LOAD CURRENT
(V_{OUT} = 3.3V, PWM MODE)



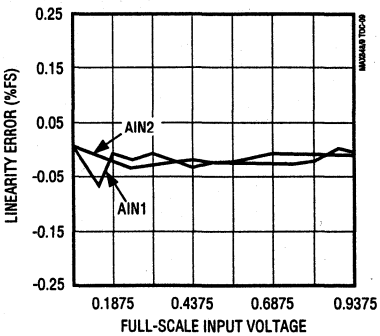
REFERENCE VOLTAGE
vs. TEMPERATURE



REFERENCE VOLTAGE
vs. REFERENCE CURRENT



ADC LINEARITY ERROR
vs. FULL-SCALE INPUT VOLTAGE

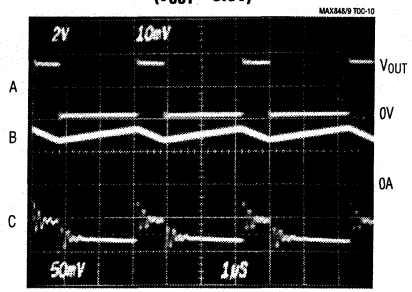


1-Cell to 3-Cell, High-Power, Low-Noise, Step-Up DC-DC Converters

Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

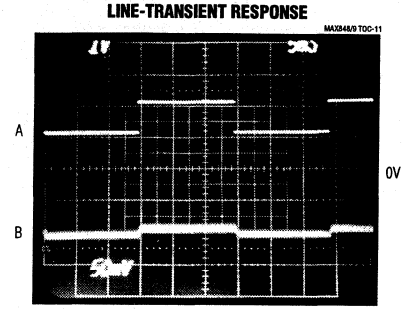
HEAVY-LOAD SWITCHING WAVEFORMS (V_{OUT} = 3.3V)



1µs/div

V_{IN} = 1.1V, I_{OUT} = 200mA, V_{OUT} = 3.3V
A = LX VOLTAGE, 2V/div
B = INDUCTOR CURRENT, 0.5A/div
C = V_{OUT} RIPPLE, 50mV/div, AC COUPLED

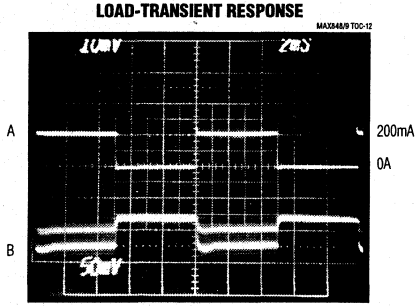
LINE-TRANSIENT RESPONSE



5ms/div

I_{OUT} = 0mA, V_{OUT} = 3.3V
A = V_{IN}, 1.1V TO 2.1V, 1V/div
B = V_{OUT} RIPPLE, 50mV/div, AC COUPLED

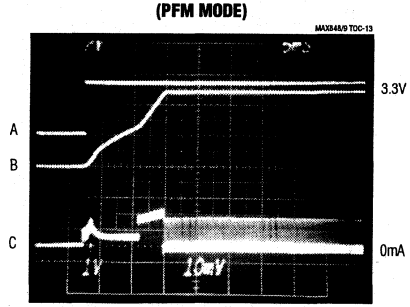
LOAD-TRANSIENT RESPONSE



2ms/div

V_{IN} = 1.1V, V_{OUT} = 3.3V
A = LOAD CURRENT, 0mA TO 200mA, 0.2A/div
B = V_{OUT} RIPPLE, 50mV/div, AC COUPLED

POWER-ON DELAY (PFM MODE)



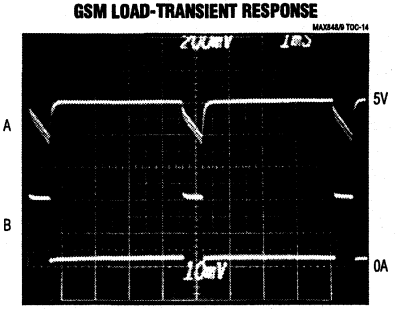
5ms/div

A = V_{ON1}, 2V/div
B = V_{OUT}, 1V/div
C = INPUT CURRENT, 0.2A/div

Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

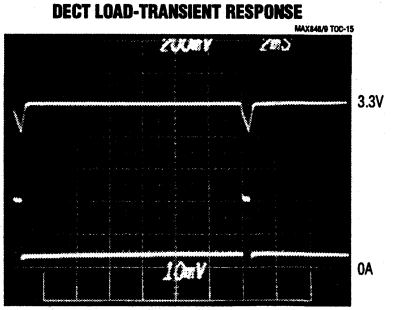
MAX849
GSM LOAD-TRANSIENT RESPONSE



1ms/div

V_{IN} = 3.6V, V_{OUT} = 5V, C_{OUT} = 440µF
A = V_{OUT} RIPPLE, 200mV/div, AC COUPLED
B = LOAD CURRENT, 100mA TO 1A, 0.5A/div,
PULSE WIDTH = 577µs

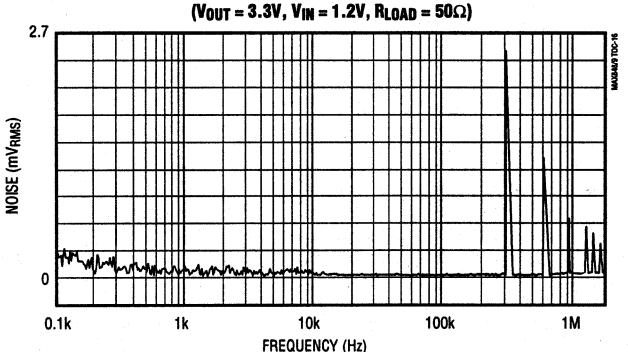
MAX849
DECT LOAD-TRANSIENT RESPONSE



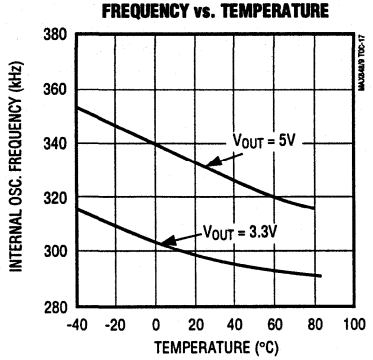
2ms/div

V_{IN} = 1.2V, V_{OUT} = 3.3V, C_{OUT} = 440µF
A = V_{OUT} RIPPLE, 200mV/div, AC COUPLED
B = LOAD CURRENT, 50mA TO 400mA, 0.2A/div,
PULSE WIDTH = 416µs

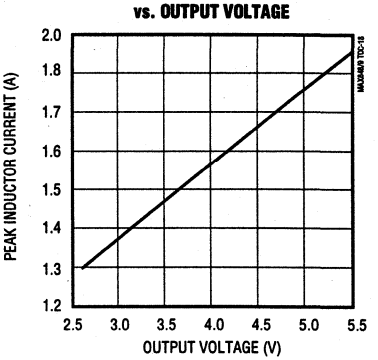
MAX849 NOISE SPECTRUM
(V_{OUT} = 3.3V, V_{IN} = 1.2V, R_{LOAD} = 50Ω)



MAX849 INTERNAL OSCILLATOR
FREQUENCY vs. TEMPERATURE



MAX849 PEAK INDUCTOR CURRENT
vs. OUTPUT VOLTAGE



1-Cell to 3-Cell, High-Power, Low-Noise, Step-Up DC-DC Converters

Pin Description

PIN	NAME	FUNCTION
1	AIN1	ADC's Channel 1 Input. Analog input voltage range is 0.625V to 1.875V.
2	AIN2	ADC's Channel 2 Input. Analog input voltage range is 0V to 2.5V.
3	REF	Reference Output. Bypass with a 0.22µF capacitor to GND.
4	GND	Ground. Use for low-current ground paths. Connect to PGND with a short trace.
5	OUT	Output Sense Input. The IC is powered from OUT. Bypass to GND with a 0.1µF ceramic capacitor. Connect OUT to POUT through a 10Ω series resistor.
6	POKIN	Power-Good Comparator Input. Connect to GND for fixed threshold (V_{OUT} x 0.9). To adjust the threshold, connect to a resistor divider from OUT to GND.
7	FB	Dual Mode DC-DC Converter Feedback Input. Connect to GND for fixed 3.3V output voltage. Connect to a resistor divider from OUT to GND to adjust the output voltage. Minimize noise coupling from switching signals to FB.
8	POK	Power-Good Output. This open-drain output is pulled low when the output voltage (V_{OUT}) drops below the internally set threshold (fixed threshold), or when the voltage at POKIN drops below V_{REF} (adjustable threshold).
9	AINSEL	ADC's Input Channel Selector. Pull low to select AIN1 and drive high to select AIN2.
10	DATA	ADC's Serial Output. Pulsed output, RZ format. Full scale is $f_{OSC}/2$ ($f_{CLK}/2$ in external sync mode). The DATA output is low when $V_{CLK/SEL}$ = 0V (PFM mode).
11	CLK/SEL	External Clock Input/Regulator's Switching Mode Selector. CLK/SEL = low: low-power, low-quiescent PFM mode. Delivers 100mW of output power. CLK/SEL = high: low-noise, high-power PWM mode, switching at a constant frequency (300kHz). CLK/SEL = driven with external clock: low-noise, high-power, synchronized PWM mode. The internal oscillator is synchronized to the external clock (200kHz ~ 400kHz). Turning the DC-DC converter on with $V_{CLK/SEL}$ = 0V also serves as a soft-start function, since the peak inductor current is limited to 30% of the nominal value.
12	PGND	Source of the Internal N-Channel Power MOSFET. Connect to high-current ground path.
13	LX	Drain of the Internal N-Channel Power MOSFET and P-Channel Synchronous Rectifier
14	POUT	Source of the Internal P-Channel Synchronous Rectifier MOSFET. Connect an external Schottky diode from LX to POUT. Bypass to PGND with a 0.1µF ceramic capacitor as close to the IC as possible.
15	$\overline{ON2}$	OFF Control Input. When ON1 = 0 and $\overline{ON2}$ = 1, the IC is off.
16	ON1	ON Control Input. When ON1 = 1 or $\overline{ON2}$ = 0, the IC is on.

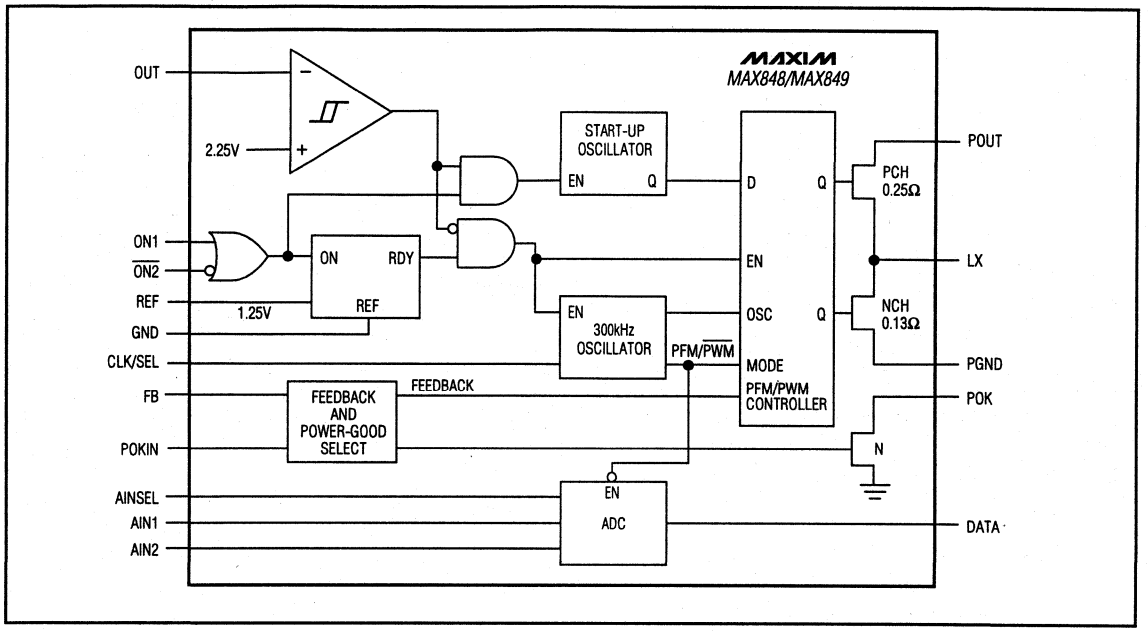


Figure 1. Functional Diagram

Detailed Description

The MAX848/MAX849 combine a switching regulator, N-channel power MOSFET, P-channel synchronous rectifier, precision reference voltage, power-good indicator, and battery voltage monitor, all in a single monolithic device. The MAX848/MAX849 are powered directly from the output. The output voltage is factory preset to 3.3V or adjustable from 2.7V to 5V with external resistors (Dual Mode™ operation). These devices start from a low 1V input voltage and remain operational down to 0.7V. The MAX848/MAX849 operate with either one to three NiCd/NiMH cells or one Li-Ion cell.

At power-up, an internal low-voltage oscillator drives the N-channel power switch, and the output voltage slowly builds up. The oscillator has a 25% nominal duty cycle to prevent current build-up in the inductor. An output voltage in excess of the nominal 2.25V lockout voltage activates the error comparator and internal timing circuitry. The device resumes operation in either pulse-frequency-modulation (PFM) low-power mode or pulse-width-modulation (PWM) low-noise mode, selected by the logic control, CLK/SEL. Figure 2 shows the standard application circuit for the MAX849 configured in the high-power PWM mode.

On/Off Control

The MAX848/MAX849 are turned on or off by logic input pins ON1 and $\overline{ON2}$ (Table 1). When ON1 = 1 or $\overline{ON2}$ = 0, the part is on. When ON1 = 0 and $\overline{ON2}$ = 1, the part is off. Both inputs have logic trip points near 0.5 x V_{OUT} with 0.15 x V_{OUT} hysteresis.

Table 1. On/Off Logic Control

ON1	$\overline{ON2}$	MAX848/MAX849
0	0	On
0	1	Off
1	0	On
1	1	On

Operating Modes

The MAX848/MAX849 operate in either PFM, PWM, or PWM synchronized to an externally applied clock signal. Table 2 lists each operating mode.

1-Cell to 3-Cell, High-Power, Low-Noise, Step-Up DC-DC Converters

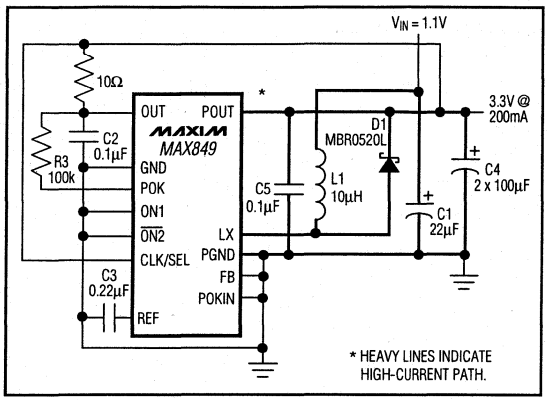


Figure 2. 3.3V Preset Output

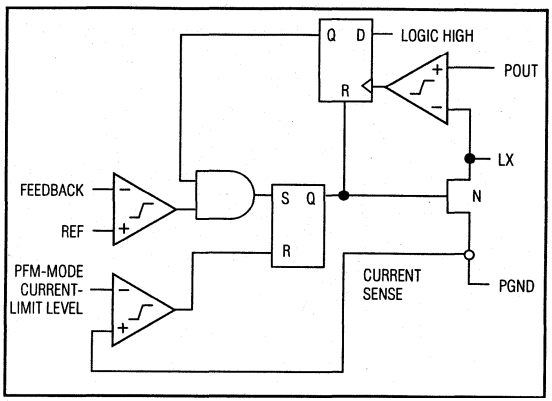


Figure 3. Controller Block Diagram in PFM Mode

Table 2. Selecting Operating Mode

CLK/SEL	MODE
0	PFM
1	PWM
External clock (200kHz ~ 400kHz)	Synchronized PWM

Low-Power PFM Mode

When CLK/SEL is pulled low, the MAX848/MAX849 operate in low-power, low-supply-current PFM mode. Pulse-frequency modulation provides the highest efficiency at light loads. The P-channel rectifier is turned off to reduce gate-charge losses, and the regulator operates in discontinuous mode. The N-channel power MOSFET is kept on until the inductor current ramps to 30% of the current limit. The inductor energy is delivered to the output capacitor when the switch turns off. A new cycle is inhibited until the inductor current crosses zero. Zero current detection is accomplished by sensing the LX voltage crossing the output voltage. Figure 3 shows the block diagram for the PFM controller.

Low-Noise PWM Mode

When CLK/SEL is pulled high, the MAX848/MAX849 operate in high-power, low-noise, current-mode PWM, switching at the 300kHz nominal internal oscillator frequency. The internal rectifier is active in this mode, and the regulator operates in continuous mode. The N-channel power MOSFET turns on until either the output voltage is in regulation or the inductor current limit is reached (0.8A for the MAX848 and 1.4A for the MAX849). The switch turns off for the remainder of the cycle and the inductor energy is delivered to the output capacitor. A new cycle is initiated on the next oscillator cycle. In low-noise applications, the fundamental and the harmonics generated by the fixed switching frequency can easily be filtered. Figure 4 shows the block diagram for the PWM controller.

The MAX848/MAX849 enter synchronized current-mode PWM when a clock signal (200kHz < f_{CLK} < 400kHz) is applied to CLK/SEL. The internal synchronous rectifier is active and the switching frequency is synchronized to the externally applied clock signal. For wireless applications, this ensures that the harmonics of the switching frequencies are predictable and can be kept outside the IF band(s). High-frequency operation permits low-magnitude output ripple voltage.

The MAX848/MAX849 are capable of providing a stable output even with a rapidly pulsing load (GSM, DECT), such as from a transmitter power amplifier in digital cordless phones (see *Typical Operating Characteristics*).

In PWM mode, the use of the synchronous rectifier ensures constant-frequency operation, regardless of the load current.

Setting the Output Voltage Externally

The MAX848/MAX849 feature Dual Mode operation. The output voltage is preset to 3.3V (FB = 0V), or it can be adjusted from 2.7V to 5.5V with external resistors R1, R2, and R3, as shown in Figure 5. To set the output voltage externally, select resistor R3 in the 10kΩ to 100kΩ range. The values for R1 and R2 are given by:

$$R2 = R3(V_{OUT} / V_{TRIP} - 1)$$

$$R1 = (R3 + R2)(V_{TRIP} / V_{REF} - 1)$$

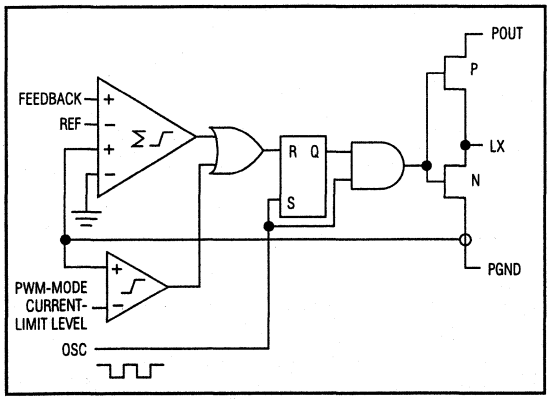


Figure 4. Controller Block Diagram in PWM Mode

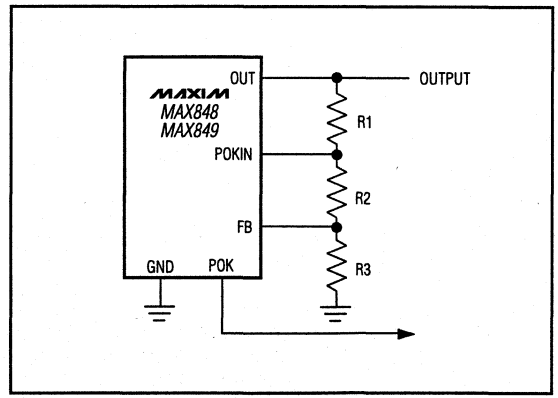


Figure 5. Adjustable Output Voltage and Power-Good Trip Level

where V_{REF} = 1.25V, V_{OUT} is the desired output voltage, and V_{TRIP} is the desired trip level for the power-good comparator.

Power-OK

The MAX848/MAX849 feature a power-good comparator. This comparator's open-drain output, POK, is pulled low when the output voltage falls below the nominal internal threshold level of 3V with POKIN = 0V. To set the power-good trip level externally, refer to the *Setting the Output Voltage Externally* section.

Analog-to-Digital Converter (ADC)

The MAX848/MAX849 have an internal, two-channel, serial ADC. The ADC converts an analog input voltage into a digital stream available at the DATA pin. The converter skips clock pulses in proportion to the input voltage. Output format is a return-to-zero bit stream with a bit duration of $1/f_{CLK}$. At zero-scale input voltage, all pulses are skipped and DATA remains low; with a positive full-scale input voltage, no pulses are skipped; and at mid-scale, every other pulse is skipped. The ADC's clock is one-half of the externally applied clock signal or one-half of the internal 300kHz clock available at LX. In PFM mode, the converter is not active and DATA is driven low.

Channel 1, AIN1, has an input voltage range of 0.625V to 1.875V and is selected when AINSEL is low. Channel 2, AIN2, accepts inputs in the 0V to 2.5V range and is selected when AINSEL is pulled high (Figure 6).

The ADC is a switched-capacitor type; therefore, an anti-aliasing filter might be required at the inputs. Insert a 1kΩ series resistor and a 0.01µF filter capacitor in noisy environments.

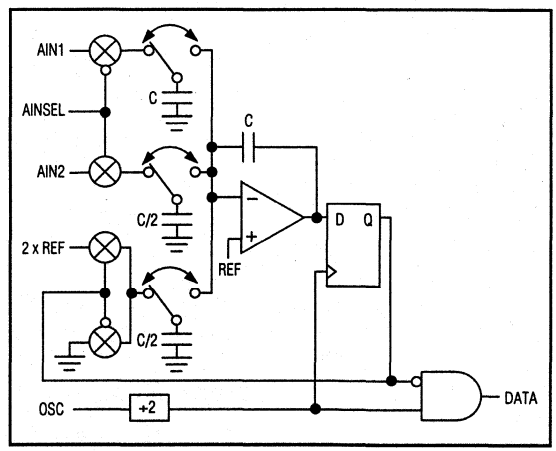


Figure 6. A/D Converter Block Diagram

Timer Function Implementation

Implement the necessary counter functions either with discrete hardware or with microcontroller (µC) implementations. The output resolution depends on how many of the ADC clock pulses are counted, as shown in Figure 7.

Hardware Implementation

A complete hardware solution can be implemented using either two counters or an ASIC. Resolution depends on how many pulses are counted. The main advantage of the discrete hardware implementation is that accuracy is not affected by interrupt latency associated with the µC solution.

1-Cell to 3-Cell, High-Power, Low-Noise, Step-Up DC-DC Converters

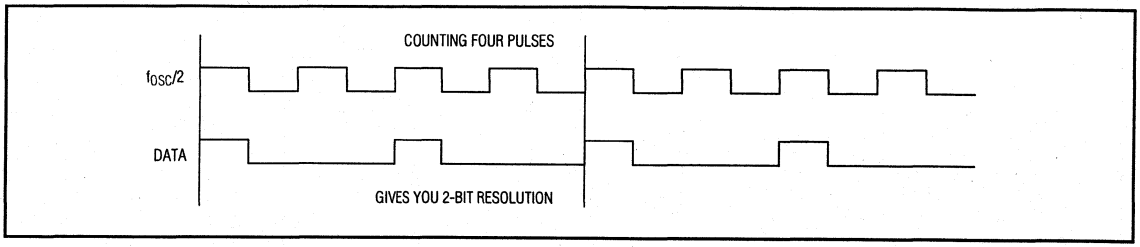


Figure 7. Bit Stream at 1/2 Full Scale

When using two counters of the same length, as shown in Figure 8, one counter (A) just counts the A/D clock pulses (fOSC/2), and the other counter (B) counts DATA output pulses. When counter A overflows (for example, after 256 clock cycles for an 8-bit counter), counter B is disabled. The controller reads the counter B output data and calculates the analog voltage present at the ADC's input.

All µC Implementation

This implementation uses a µC timer and a counter. The timer and the counter are reset at the same time. The counter counts data-output pulses applied at its input. When the timer times out, an interrupt is asserted. The µC then reads the state of the counter register. The interrupt-handling overhead can cause the counter to count more pulses than desired. Accuracy depends on how long the µC needs to read the counter. No errors will occur if the counter is disabled within one clock period. Interrupt latency reduces accuracy. The main advantage of this implementation is that no external hardware is required.

Design Procedure

Inductor Selection

The MAX848/MAX849's high switching frequency allows the use of a small inductor. Use a 10µH inductor for the MAX849 and a 22µH inductor for the MAX848. Inductors with a ferrite core or equivalent are recommended; powder iron cores are not recommended for use with high switching frequencies. Make sure the inductor's saturation rating (the current at which the core begins to saturate and inductance starts to fall) exceeds the internal current limit: 0.8A for the MAX848 and 1.4A for the MAX849. However, it is generally acceptable to bias the inductor into saturation by approximately 20% (the point where the inductance is 20% below the nominal value). For highest efficiency, use a coil with low DC resistance, preferably under 100mΩ. To minimize radiated noise, use a toroid, pot core, or shielded inductor. See Table 5 for a list of suggested inductor suppliers.

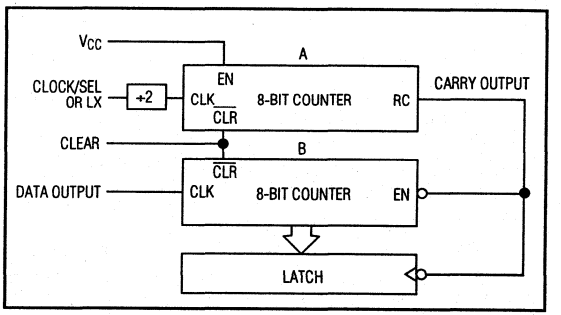


Figure 8. Discrete Hardware Solution for Counting A/D Output Data Pulses

Diode Selection

The MAX848/MAX849's high switching frequency demands a high-speed rectifier. Schottky diodes, such as the 1N5817 or MBR0520L, are recommended. Make sure the diode's current rating exceeds the maximum load current and that its breakdown voltage exceeds VOUT.

The Schottky rectifier diode carries load currents only in the PFM operating mode, since the P-channel synchronous rectifier is disabled. Therefore, the current rating need not be high (0.5A is sufficient). In PFM mode, the voltage drop across the rectifier diode causes efficiency loss. However, when operating in PWM mode, the internal P-channel synchronous rectifier is active and efficiency loss due to the rectifier diode is minimized.

For high-temperature applications, Schottky diodes may be inadequate due to their high leakage currents; use high-speed silicon diodes such as the MUR105 or EC11FS1. At heavy loads and high temperatures, the benefits of a Schottky diode's low forward voltage may outweigh the disadvantage of high leakage current. See Table 4 for a list of suggested diode suppliers.

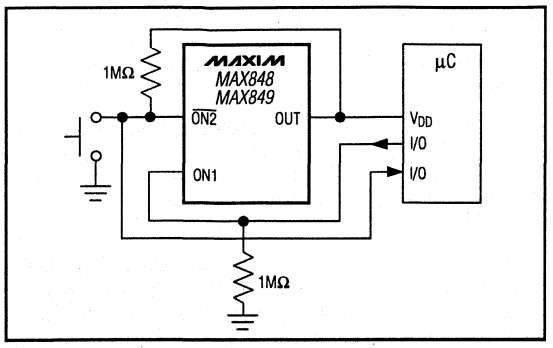


Figure 9. Momentary Pushbutton On/Off Switch

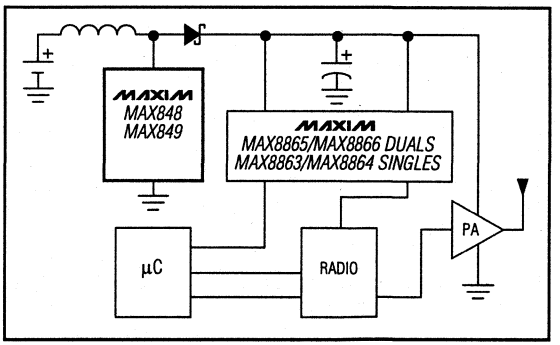


Figure 10. Typical Phone Application

Capacitor Selection

Input Bypass Capacitors

A 22µF, low-ESR input capacitor will reduce peak currents and reflected noise due to inductor current ripple. Smaller ceramic capacitors may also be used for light loads or in applications that can tolerate higher input ripple.

Output Filter Capacitors

Two 100µF (single 100µF for the MAX848), 10V, low-ESR, output filter capacitors typically exhibit 30mV ripple when stepping up from 1.2V to 3.3V at 200mA (100mA for the MAX848). Bypass the MAX848/MAX849 supply input, OUT, with a 0.1µF ceramic capacitor to GND. Also bypass POUT to PGND with a 0.1µF ceramic capacitor.

The filter capacitors' equivalent series resistance (ESR) affects efficiency and output ripple. The output voltage ripple is the product of the peak inductor current and the output capacitor's ESR. Low-ESR, surface-mount tantalum capacitors are currently available from Sprague (595D series) and AVX (TPS series). Sanyo OS-CON organic-semiconductor, through-hole capacitors also exhibit very low ESR, and are especially useful for operation at cold temperatures. See Table 5 for a list of suggested capacitor suppliers.

Applications Information

Using a Momentary On/Off Switch

A momentary pushbutton switch can be used to turn the MAX848/MAX849 on and off.

As shown in Figure 9, ON1 is pulled low and $\overline{ON2}$ is pulled high when the part is off. When the momentary switch is pressed, $\overline{ON2}$ is pulled low and the regulator turns on. The switch should be on long enough for the µC to exit reset. The controller issues a logic high to ON1, which guarantees that the part will stay on, regardless of the switch state.

To turn off the regulator, the switch is pressed and held. The controller reads the switch status and pulls ON1 low. The switch is released and $\overline{ON2}$ is pulled high.

Power Amplifier (PA) and Radio Supply in a Typical Phone Application

The MAX849 is an ideal power supply for the power amplifier (PA) and the radio used in digital cordless and PCS phones (Figure 10). The PA is directly powered by the MAX849 for maximum output swing. Post-linear regulators power the controller and the radio. In addition, they reduce switching noise and ripple. Table 3 lists the output power available when operating with one or more NiCd/NiMH cells or one Li-Ion cell.

Table 3. Available Output Power

NUMBER OF CELLS	INPUT VOLTAGE (V)	OUTPUT VOLTAGE: PA POWER SUPPLY (V)	OUTPUT POWER (W)
1 NiCd/NiMH	1.2	3.3	0.9
2 NiCd/NiMH	2.4	3.3	2.4
2 NiCd/NiMH	2.4	5.0	2.6
3 NiCd/NiMH or 1 Li-Ion	3.6	5.0	4.3

1-Cell to 3-Cell, High-Power, Low-Noise, Step-Up DC-DC Converters

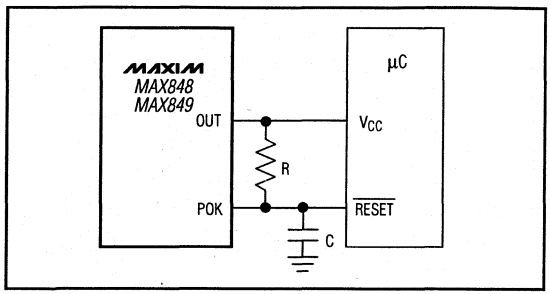


Figure 11. Power-On Reset Delay

Power-On Reset Delay

Adding a timing capacitor from POK to GND generates a power-on reset delay. The reset time constant is determined by the pull-up resistor and timing capacitor (Figure 11). When power is turned on, POK is low and the capacitor is shorted. When the output voltage reaches regulation, POK goes high and the capacitor slowly charges to the output voltage.

The timing resistor value depends on the controller's RESET input leakage current. The voltage drop across the timing resistor should not exceed the difference between the output voltage and the µC reset threshold voltage. This resistor should be large enough to minimize the shutdown current.

µC-Controlled Shutdown

The MAX848/MAX849 turn on when ON1 = 1 or $\overline{ON2}$ = 0. The µC monitors the battery voltage and turns off the device (forces ON1 low and $\overline{ON2}$ high) when the battery is weak.

Layout Considerations

Due to high inductor current levels and fast switching waveforms, which radiate noise, proper PC board layout is essential. Protect sensitive analog grounds by using a star ground configuration. Minimize ground noise by connecting PGND, the input bypass capacitor ground lead, and the output filter capacitor ground lead to a single point (star ground configuration). Also, minimize lead lengths to reduce stray capacitance and trace resistance.

If an external resistor divider is used to set the output voltage (Figure 5), the trace from FB to the resistors must be extremely short and must be shielded from switching signals, such as CLK, DATA, or LX.

Table 4. Component Selection Guide

PRODUCTION	INDUCTORS	CAPACITORS	DIODES
Surface Mount	Sumida CDR63B, CD73, CDR73B, CD74B series Coilcraft DO1608, DO3308, DT3316 series	Matsuo 267 series Sprague 595D series AVX TPS series	Motorola MBR0520L
Through Hole	Sumida RCH654 series	Sanyo OS-CON series Nichicon PL series	Motorola 1N5817

Table 5. Component Suppliers

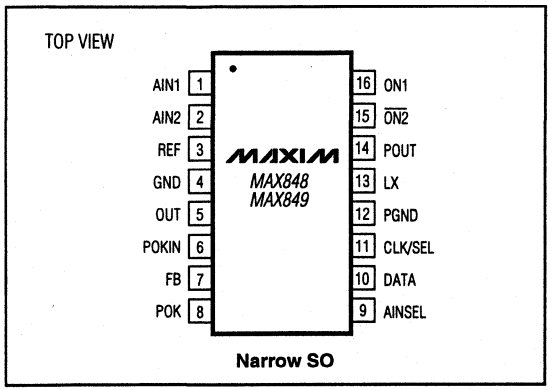
SUPPLIER	PHONE	FAX
AVX	USA: (803) 946-0690 (800) 282-4975	(803) 626-3123
Coilcraft	USA: (847) 639-6400	(847) 639-1469
Matsuo	USA: (714) 969-2491	(714) 960-6492
Motorola	USA: (602) 303-5454	(602) 994-6430
Sanyo	USA: (619) 661-6835 Japan: 81-7-2070-6306	(619) 661-1055 81-7-2070-1174
Sumida	USA: (847) 956-0666 Japan: 81-3-3607-5111	(847) 956-0702 81-3-3607-5144

Chip Information

TRANSISTOR COUNT: 2059

1-Cell to 3-Cell, High-Power, Low-Noise, Step-Up DC-DC Converters

Pin Configuration



ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
11/96

MAXIM

Dual-Output, Low-Supply-Current, Dual DC-DC Boost Controller

General Description

The MAX863 contains two DC-DC step-up controllers in a single compact package. With its monolithic CMOS design, it draws only 65µA with both controllers on. The input range extends down to 1.5V, permitting use in organizers, translators, and other low-power hand-held products.

The MAX863 is 80% to 85% efficient at output loads from 5mA to over 1A. It saves space by fitting in a 16-pin QSOP package that is the same area as an 8-pin SOIC.

A current-limited, pulse-frequency-modulated (PFM) control scheme reduces start-up surge currents. Each controller uses an external N-channel MOSFET switch, so switch size can be optimized for any output current or voltage.

In larger systems, two MAX863s can be used to generate 5V, 3.3V, 12V, and 28V from just two or three battery cells.

Features

- ♦ **Smallest Dual Boost Converter: 16-Pin QSOP**
- ♦ **65µA Total Quiescent Supply Current**
- ♦ **Main Supply and LCD from One IC**
- ♦ **2 or 3 NiCd/NiMH or 1 Li-Ion Cell Input**
- ♦ **Step-Up/Down Configurable**
- ♦ **Drives Surface-Mount, Dual N-Channel MOSFETs**
- ♦ **1µA Shutdown Current**
- ♦ **Low-Battery Input/Output Comparator**
- ♦ **Independent Shutdown Controls**
- ♦ **Current Limiting**

Applications

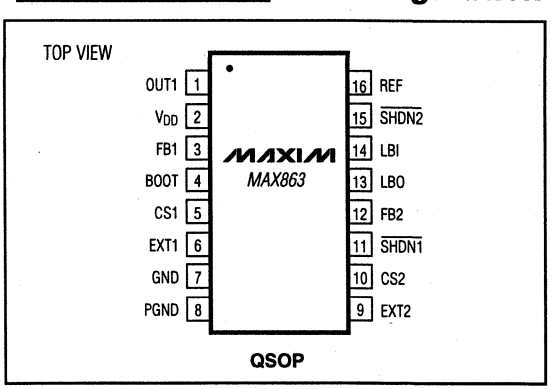
Organizers
Translators
Hand-Held Instruments
Palmtop Computers
PDAs

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX863EEE	-40°C to +85°C	16 QSOP
MAX863E/D	-40°C to +85°C	Dice*

**Contact factory for dice specifications.*

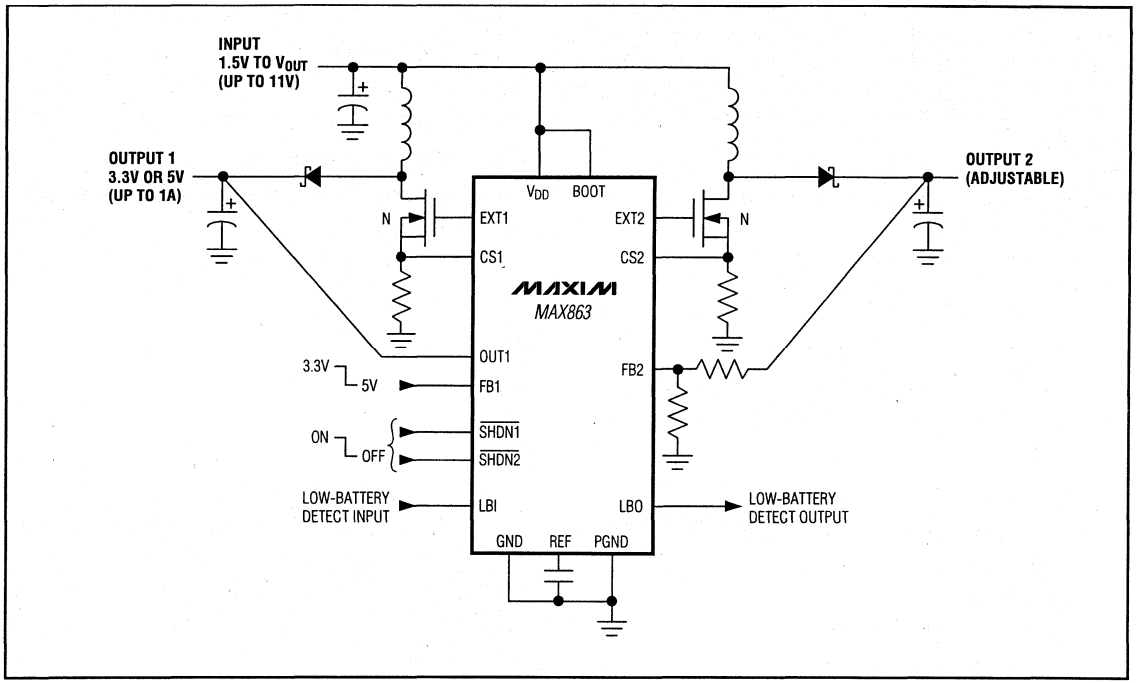
Pin Configuration



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Dual-Output, Low-Supply-Current, Dual DC-DC Boost Controller

Typical Operating Circuit



19-0478; Rev 0; 3/96

MAXIM

Dual-Output Charge Pump with Shutdown

General Description

The MAX864 CMOS, charge-pump, DC-DC voltage converter produces a positive and a negative output from a single positive input, and requires only four capacitors. The charge pump first doubles the input voltage, then inverts the doubled voltage. The input voltage ranges from +1.75V to +6.0V.

The internal oscillator can be pin-programmed from 7kHz to 185kHz, allowing the quiescent current, capacitor size, and switching frequency to be optimized. The 55Ω output impedance permits useful output currents up to 20mA. The MAX864 also has a 1µA logic-controlled shutdown.

The MAX864 comes in a 16-pin QSOP package that uses the same board area as a standard 8-pin SOIC. For more space-sensitive applications, the MAX865 is available in an 8-pin µMAX package, which uses half the board area of the MAX864.

Applications

Low-Voltage GaAsFET Bias in Wireless Handsets

VCO and GaAsFET Supply

Split Supply from 2 to 4 Ni Cells or 1 Li+ Cell

Low-Cost Split Supply for Low-Voltage Data-Acquisition Systems

Split Supply for Analog Circuitry

LCD Panels

Features

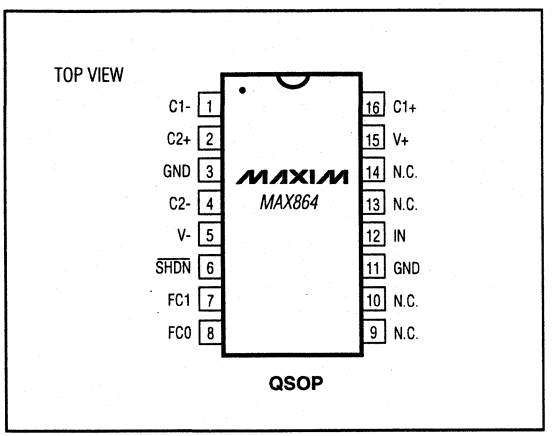
- **Requires Only Four Capacitors**
- **Dual Outputs (Positive and Negative)**
- **Low Input Voltages: +1.75V to +6.0V**
- **1µA Logic-Controlled Shutdown**
- **Selectable Frequencies Allow Optimization of Capacitor Size and Supply Current**

Ordering Information

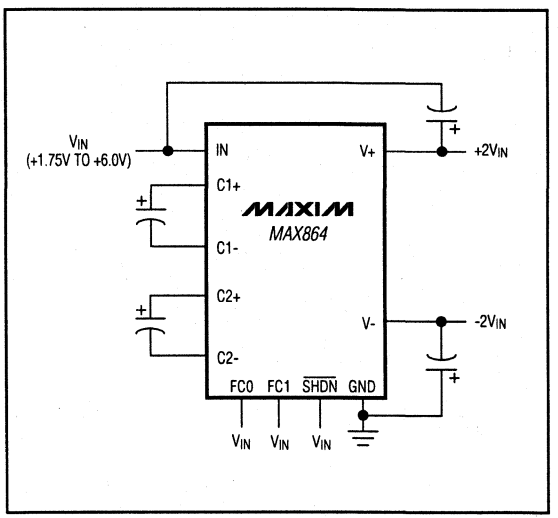
PART	TEMP. RANGE	PIN-PACKAGE
MAX864C/D	0°C to +70°C	Dice*
MAX864EEE	-40°C to +85°C	16 QSOP

** Contact factory for dice specifications.*

Pin Configuration



Typical Operating Circuit



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Dual-Output Charge Pump with Shutdown

ABSOLUTE MAXIMUM RATINGS

V+ to GND .....-0.3V to +12V
$\overline{SHDN}$, FC0, FC1 to GND .....-0.3V to (V+ + 0.3V)
IN to GND .....-0.3V to +6.2V
V- to GND .....+0.3V to -12V
V- Output Current 100mA
V- Short Circuit to GND .....Indefinite

Operating Temperature Range
MAX864EEE.....-40°C to +85°C
Continuous Power Dissipation (T_A = +70°C)
QSOP (derate 8.70mW/°C above +70°C).....696mW
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 1)

(V_{IN} = 5V, $\overline{SHDN}$ = V_{IN}, circuit of Figure 1, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

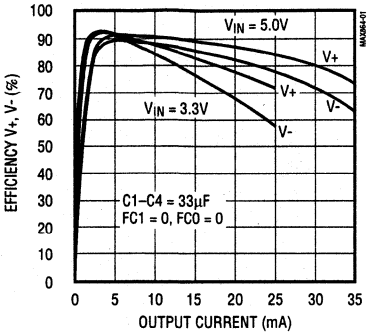
PARAMETER	SYMBOL		MIN	TYP	MAX	UNITS
SUPPLY						
Minimum Start-Up Voltage	R_{LOAD} = 10kΩ	T_A = +25°C	1.75	1.25		V
		T_A = T_{MIN} to T_{MAX}	2.00			
Maximum Supply Voltage	R_{LOAD} = 10kΩ				6.0	V
Supply Current	FC1 = FC0 = GND, f = 7kHz			0.6	1.0	mA
	FC1 = GND, FC0 = IN, f = 33kHz			2.4	3.65	
	FC1 = IN, FC0 = GND, f = 100kHz			7	11	
	FC1 = FC0 = IN, f = 185kHz			12	18	
Shutdown Current	FC1 = FC0 = IN or GND, $\overline{SHDN}$ = GND			0.1	1	µA
Oscillator Frequency	FC1 = FC0 = GND		5	7	10	kHz
	FC1 = GND, FC0 = IN		24	33	48	
	FC1 = IN, FC0 = GND		70	100	140	
	FC1 = FC0 = IN		130	185	260	
INPUTS AND OUTPUTS						
Logic Input Low Voltage	$\overline{SHDN}$, FC0, FC1			2.2	1.0	V
Logic Input High Voltage	$\overline{SHDN}$, FC0, FC1		3.5	2.8		V
Logic Input Bias Current	$\overline{SHDN}$, FC0 = FC1 = GND or IN		-1		1	µA
V+ to IN Shutdown Resistance	I_{V+} = 10mA			22	100	Ω
V- to GND Shutdown Resistance	I_{V-} = 10mA			6	50	Ω
Output Resistance (Note 1)	I_{V+} = 10mA, I_{V-} = 0mA	T_A = +25°C		55	75	Ω
		T_A = T_{MIN} to T_{MAX}			100	
	V+ = 10V, I_{V-} = 10mA (forced)	T_A = +25°C		34	50	
		T_A = T_{MIN} to T_{MAX}			60	
Voltage Conversion Efficiency	V+, R_L = ∞		95	99		%
	V-, R_L = ∞		95	99		

Note 1: Measured using the capacitor values in Table 1. Capacitor ESR contributes approximately 10% of the output impedance [ESR + 1 / (pump frequency x capacitance)].

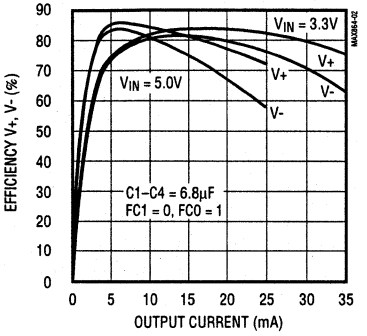
Typical Operating Characteristics

(V_{IN} = 5.0V, capacitor values in Table 1, T_A = +25°C, unless otherwise noted.)

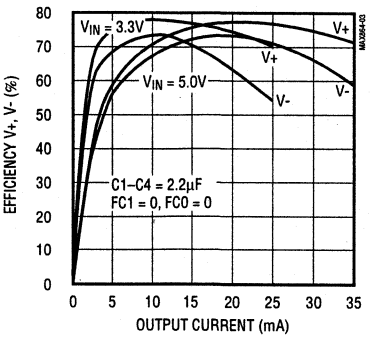
EFFICIENCY vs. OUTPUT CURRENT @ 7kHz PUMP FREQUENCY



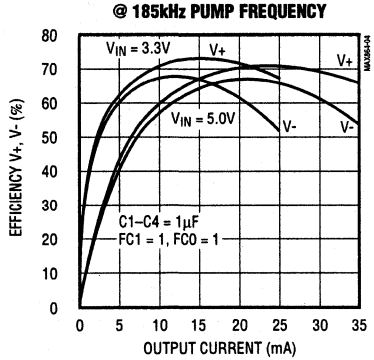
EFFICIENCY vs. OUTPUT CURRENT @ 33kHz PUMP FREQUENCY



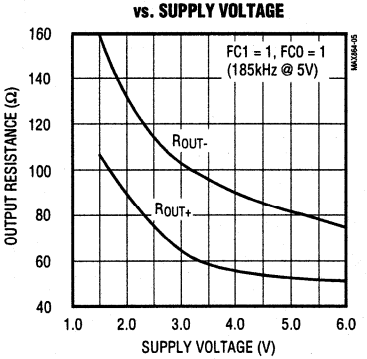
EFFICIENCY vs. OUTPUT CURRENT @ 100kHz PUMP FREQUENCY



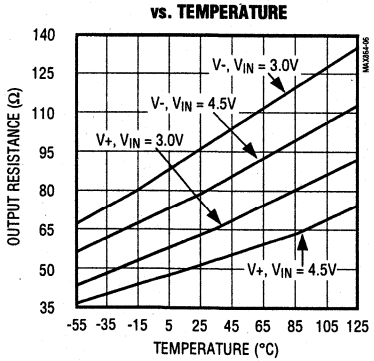
EFFICIENCY vs. OUTPUT CURRENT @ 185kHz PUMP FREQUENCY



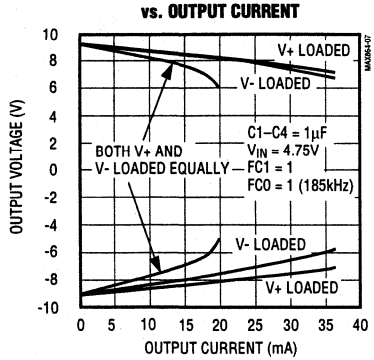
OUTPUT RESISTANCE vs. SUPPLY VOLTAGE



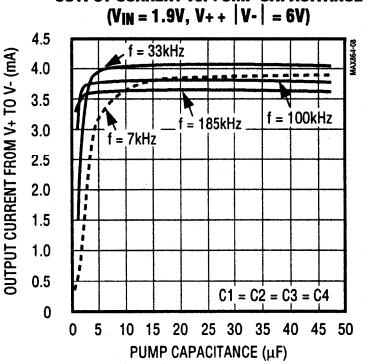
OUTPUT RESISTANCE vs. TEMPERATURE



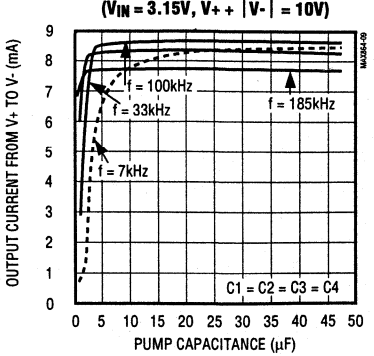
OUTPUT VOLTAGE vs. OUTPUT CURRENT



OUTPUT CURRENT vs. PUMP CAPACITANCE (V_{IN} = 1.9V, V+ + |V-| = 6V)



OUTPUT CURRENT vs. PUMP CAPACITANCE (V_{IN} = 3.15V, V+ + |V-| = 10V)

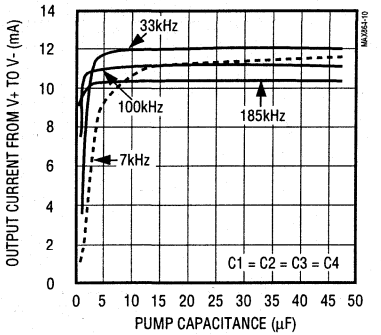


Dual-Output Charge Pump with Shutdown

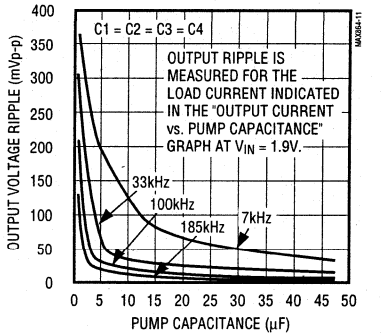
Typical Operating Characteristics (continued)

(V_{IN} = 5.0V, capacitor values in Table 1, T_A = +25°C, unless otherwise noted.)

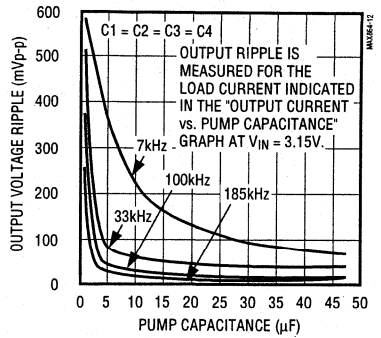
OUTPUT CURRENT vs. PUMP CAPACITANCE
(V_{IN} = 4.75V, V+ + |V-| = 16V)



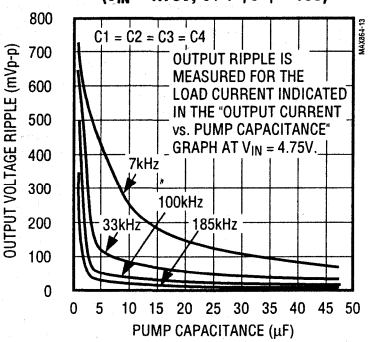
OUTPUT VOLTAGE RIPPLE vs. PUMP CAPACITANCE
(V_{IN} = 1.9V, V+ + |V-| = 6V)



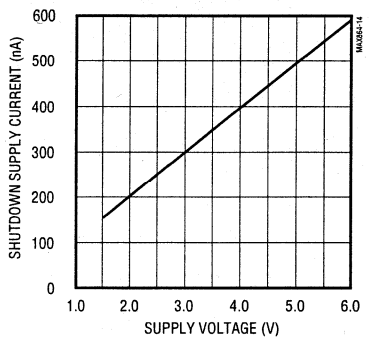
OUTPUT VOLTAGE RIPPLE vs. PUMP CAPACITANCE
(V_{IN} = 3.15V, V+ + |V-| = 10V)



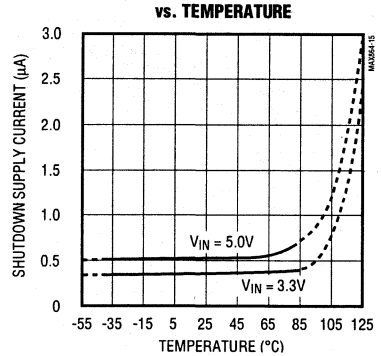
OUTPUT VOLTAGE RIPPLE vs. PUMP CAPACITANCE
(V_{IN} = 4.75V, V+ + |V-| = 16V)



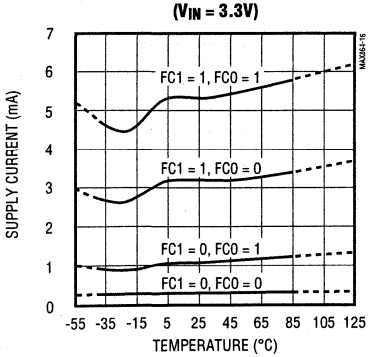
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



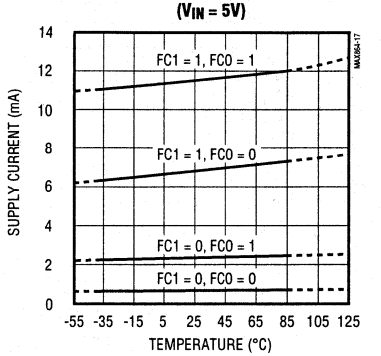
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



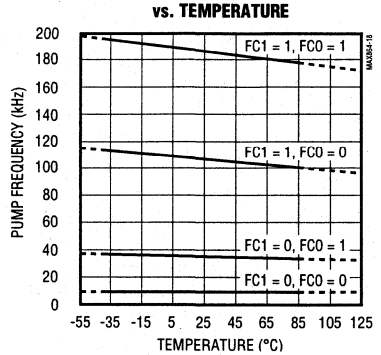
SUPPLY CURRENT vs. TEMPERATURE
(V_{IN} = 3.3V)



SUPPLY CURRENT vs. TEMPERATURE
(V_{IN} = 5V)



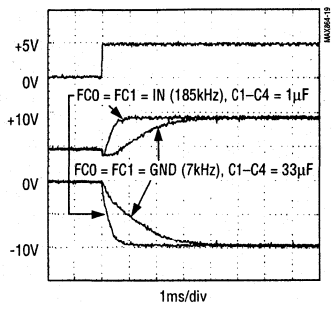
PUMP FREQUENCY vs. TEMPERATURE



Typical Operating Characteristics (continued)

(V_{IN} = 5.0V, capacitor values in Table 1, T_A = +25°C, unless otherwise noted.)

TIME TO EXIT SHUTDOWN



Pin Description

PIN	NAME	FUNCTION
1	C1-	Negative Terminal of the Flying Boost Capacitor
2	C2+	Positive Terminal of the Flying Inverting Capacitor
3, 11	GND	Ground (connect pins 3 and 11 together)
4	C2-	Negative Terminal of the Flying Inverting Capacitor
5	V-	Output of the Inverting Charge Pump
6	$\overline{SHDN}$	Active-Low Shutdown Input. With $\overline{SHDN}$ low, the part is in shutdown mode and its supply current is less than 1µA. In shutdown mode, V+ connects to IN through a 22Ω switch, and V- connects to GND through a 6Ω switch.
7	FC1	Frequency Select, MSB (see Table 1)
8	FC0	Frequency Select, LSB (see Table 1)
9, 10, 13, 14	N.C.	No Connect—no internal connection. Connect these to ground to improve thermal dissipation.
12	IN	Positive Power-Supply Input
15	V+	Output of the Boost Charge Pump
16	C1+	Positive Terminal of the Flying Boost Capacitor

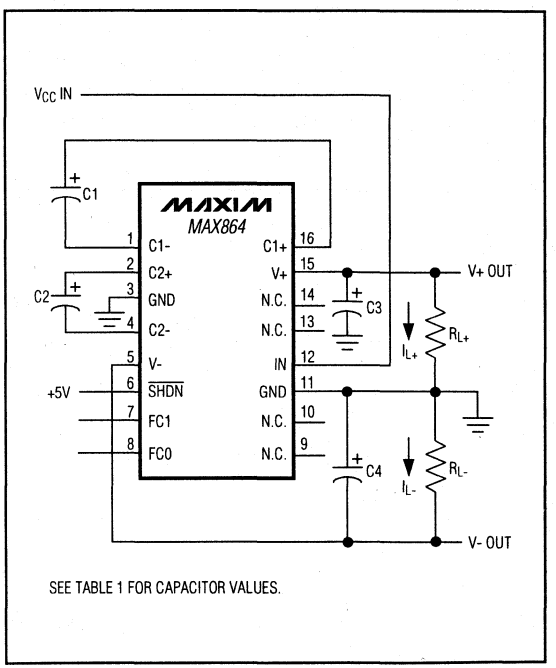


Figure 1. Test Circuit

Dual-Output Charge Pump with Shutdown

Detailed Description

The MAX864 requires only four external capacitors to implement a voltage doubler/inverter. These may be ceramic or polarized capacitors (electrolytic or tantalum) with values ranging from 0.47µF to 100µF.

Figure 2a illustrates the ideal operation of the positive voltage doubler. The on-chip oscillator generates a 50% duty-cycle clock signal. During the first half cycle, switches S2 and S4 open, switches S1 and S3 close, and capacitor C1 charges to the input voltage (V_{IN}). During the second half cycle, switches S1 and S3 open, switches S2 and S4 close, and capacitor C1 is level shifted upward by V_{IN} volts. Assuming ideal switches and no load on C3, charge transfers into C3 from C1 such that the voltage on C3 will be $2V_{IN}$, generating the positive supply output (V+).

Figure 2b illustrates the ideal operation of the negative converter. The switches of the negative converter are out of phase from the positive converter. During the second half cycle, switches S6 and S8 open, and switches S5 and S7 close, charging C2 from V+ (pumped up to $2V_{IN}$ by the positive charge pump) to GND. In the first half of the clock cycle, switches S5 and S7 open, switches S6 and S8 close, and the charge on capacitor C2 transfers to C4, generating the negative supply. The eight switches are CMOS power MOSFETs. Switches S1, S2, S4, and S5 are P-channel devices, while switches S3, S6, S7, and S8 are N-channel devices.

Charge-Pump Frequency and Capacitor Selection

The MAX864 offers four different charge-pump frequencies. To select a desired frequency, define pins FC0 and FC1 as shown in Table 1. Lower charge-pump frequencies produce lower average supply currents, while higher charge-pump frequencies require smaller capacitors.

Table 1 also lists the recommended charge-pump capacitor values for each pump frequency. Using values larger than those recommended will have little effect on the output current. Using values smaller than those recommended will reduce the available output current and increase the output ripple. To cut the output ripple in half, double the values of C3 and C4.

To maintain the lowest output resistance, use capacitors with low effective series resistance (ESR). At each switching frequency, the charge-pump output resistance is a function of C1, C2, C3, and C4's ESR. Minimizing the charge-pump capacitors' ESR minimizes output resistance. Use ceramic capacitors for best results.

Table 1. Frequency Selection

FC1	FC0	FREQUENCY (kHz)	CAPACITORS C1–C4 (µF)
0	0	7	33
0	1	33	6.8
1	0	100	2.2
1	1	185	1

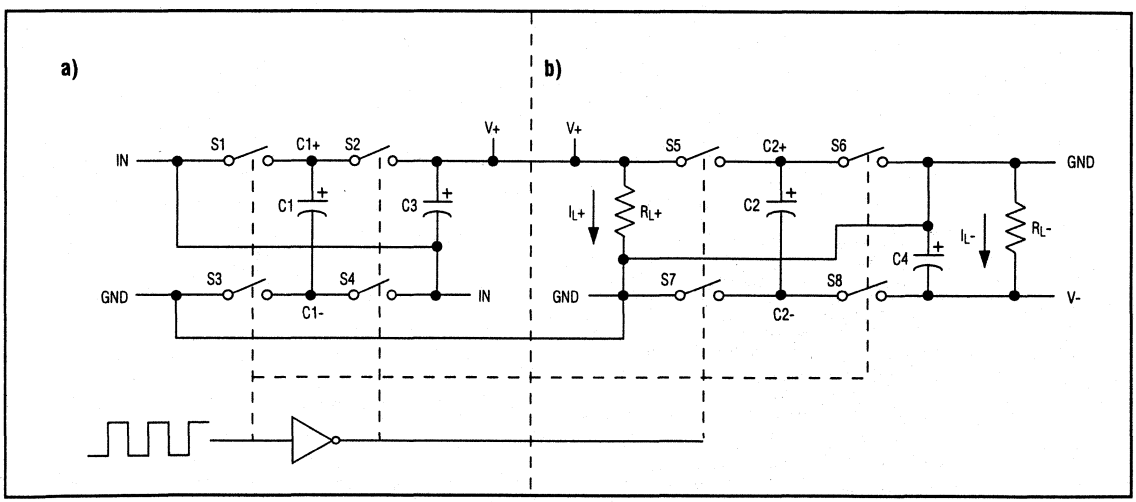


Figure 2. Idealized Voltage Quadrupler: a) Positive Charge Pump; b) Negative Charge Pump

Dual-Output Charge Pump with Shutdown

Charge-Pump Output

The MAX864 is not a voltage regulator: the output source resistance of either charge pump is approximately 55Ω at room temperature (with V_{IN} = 5V); and V+ and V- approach +10V and -10V, respectively, when lightly loaded. Both V+ and V- will droop toward GND as the current draw from either V+ or V- increases, since V- is derived from V+. Treating each converter separately, the droop of the negative supply (V_{DROOP-}) is the product of the current draw from V- (I_{V-}) and the source resistance of the negative converter (RS-):

$$V_{DROOP-} = I_{V-} \times RS-$$

The droop of the positive supply (V_{DROOP+}) is the product of the current draw from the positive supply (I_{LOAD+}) and the source resistance of the positive converter (RS+), where I_{LOAD+} is the combination of I_{V-} and the external load on V+ (I_{V+}):

$$V_{DROOP+} = I_{LOAD+} \times RS+ = (I_{V+} + I_{V-}) \times RS+$$

Determine V+ and V- as follows:

$$V+ = 2V_{IN} - V_{DROOP+}$$
$$V- = (V+ - V_{DROOP})$$
$$= -(2V_{IN} - V_{DROOP+} - V_{DROOP-})$$

The output resistances for the positive and negative charge pumps are tested and specified separately. The positive charge pump is tested with V- unloaded. The negative charge pump is tested with V+ supplied from an external source, isolating the negative charge pump.

Current draw from either V+ or V- is supplied by the reservoir capacitor alone during one half cycle of the clock. Calculate the resulting ripple voltage on either output as follows:

$$V_{RIPPLE} = \frac{1}{2} I_{LOAD} (1 / f_{PUMP}) (1 / C_{RESERVOIR})$$

where I_{LOAD} is the load on either V+ or V-. For example, with an f_{PUMP} of 33kHz and 6.8µF reservoir capacitors, the ripple is 26mV when I_{LOAD} is 12mA. Remember that, in most applications, the total load on V+ is the V+ load current (I_{V+}) and the current taken by the negative charge pump (I_{V-}).

Shutdown

The MAX864 features a shutdown mode that reduces the maximum supply current to 1µA over temperature. The $\overline{SHDN}$ pin is an active-low TTL logic-level input. If the shutdown feature is unused, connect $\overline{SHDN}$ to IN. In shutdown mode, V+ connects to IN through a 22Ω switch and V- connects to GND through a 6Ω switch.

Efficiency Considerations

Theoretically, a charge-pump voltage multiplier can approach 100% efficiency under the following conditions:

- The charge-pump switches have virtually no offset, and extremely low on-resistance.
- The drive circuitry consumes minimal power.
- The impedances of the reservoir and pump capacitors are negligible.

For the MAX864, the energy loss per clock cycle is the sum of the energy loss in the positive and negative converters, as follows:

$$LOSS_{CYCLE} = LOSS_{POS} + LOSS_{NEG}$$
$$= \frac{1}{2} C1 \left[(V+)^2 - 2(V+)(V_{IN}) \right] + \frac{1}{2} C2 \left[(V+)^2 - (V-)^2 \right]$$

where V+ and V- are the actual measured output voltages.

The average power loss is simply:

Resulting in an efficiency of:

$$P_{LOSS} = LOSS_{CYCLE} \times f_{PUMP}$$

$$\eta = \text{Total Output Power} / (\text{Total Output Power} - P_{LOSS})$$

There will be a substantial voltage difference between (V+ - V_{IN}) and V_{IN} for the positive pump, and between V+ and V- if the impedances of the pump capacitors (C1 and C2) are large with respect to their respective output loads.

Larger reservoir capacitor (C3 and C4) values will reduce output ripple. Larger values of both pump and reservoir capacitors will improve efficiency.

Dual-Output Charge Pump with Shutdown

Applications Information

Positive and Negative Converter

The most common application of the MAX864 is as a dual charge-pump voltage converter that provides positive and negative outputs of two times a positive input voltage for biasing analog circuitry (Figure 3). Select a charge-pump frequency high enough so it does not interfere with other circuitry, but low enough to maintain low supply current. See Table 1 for the correct device configuration.

Paralleling Devices

Paralleling multiple MAX864s reduces the output resistance of both the positive and negative converters (Figure 4). The effective output resistance is the output resistance of one device divided by the total number of devices. Separate C1 and C2 charge-pump capacitors are required for each MAX864, but the reservoir capacitors C3 and C4 can be shared.

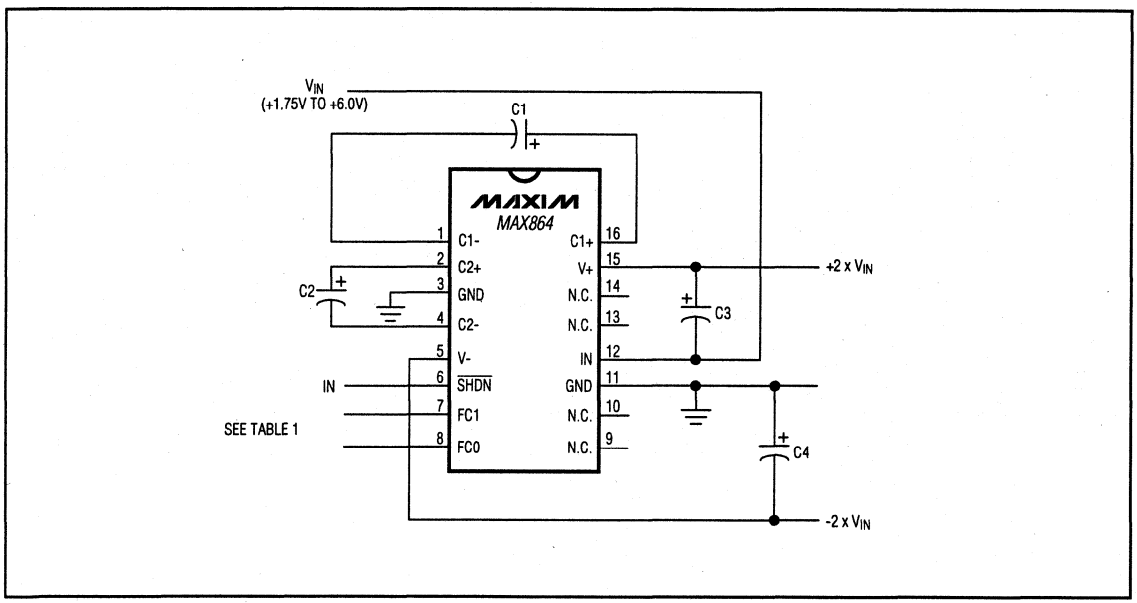


Figure 3. Positive and Negative Converter

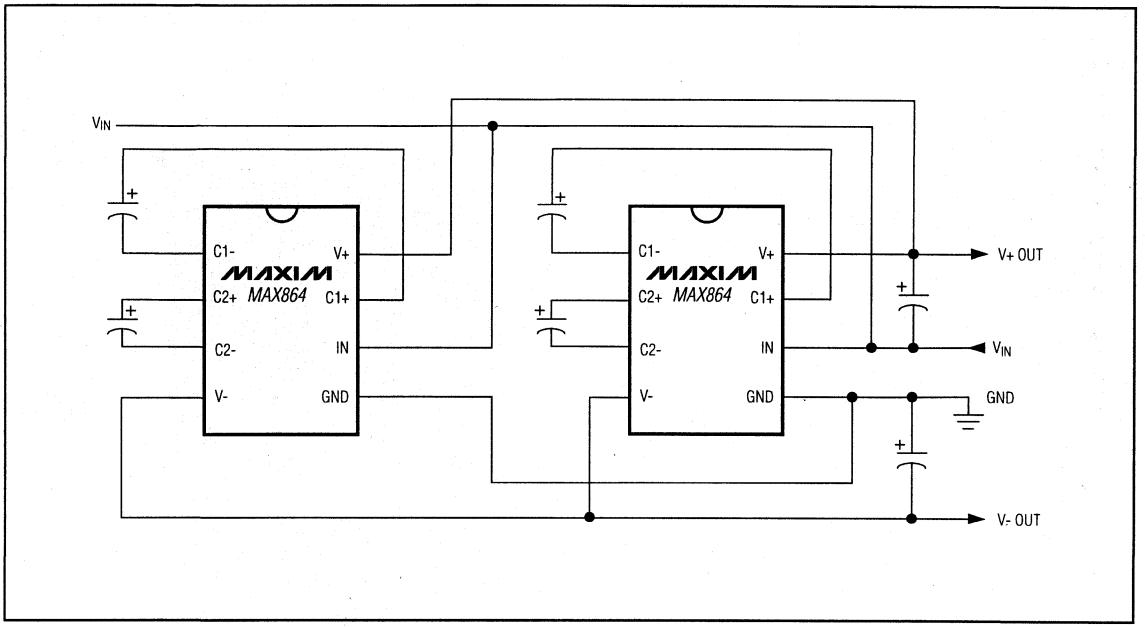


Figure 4. Paralleling Two MAX864s

Heavy Output Current Loads

When under heavy loads, where V+ is sourcing current into V- (i.e., load current flows from V+ to V-, rather than from supply to ground), do not allow the V- supply to pull above ground. In applications where large currents flow from V+ to V-, use a Schottky diode (1N5817) between GND and V-, with the anode connected to GND (Figure 5).

Layout and Grounding

Good layout is important, primarily for good noise performance. To ensure good layout, mount all components as close together as possible, keep traces short to minimize parasitic inductance and capacitance, and use a ground plane. Connecting all N.C. pins to a ground plane improves thermal dissipation.

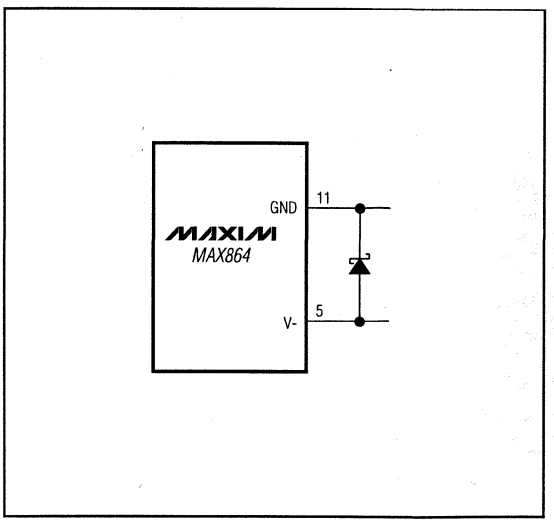
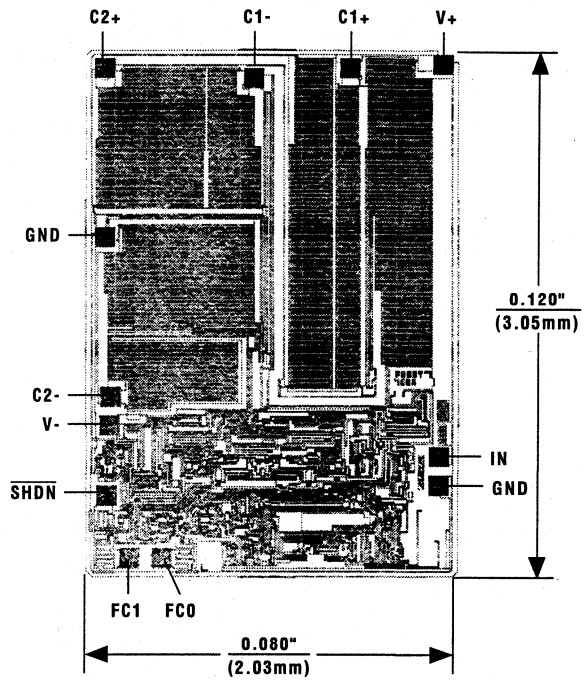


Figure 5. High V- Load Circuit

Dual-Output Charge Pump with Shutdown

Chip Topography



TRANSISTOR COUNT: 143

SUBSTRATE CONNECTED TO V+

19-0472; Rev 0; 2/96

MAXIM

Compact, Dual-Output Charge Pump

General Description

The MAX865 is a CMOS charge-pump DC-DC converter in an ultra-small µMAX package. It produces positive and negative outputs from a single positive input, and requires only four capacitors. The charge pump first doubles the input voltage, then inverts the doubled voltage. The input voltage ranges from +1.5V to +6.0V.

The internal oscillator is guaranteed to be between 20kHz and 38kHz, keeping noise above the audio range while consuming minimal supply current. A 75Ω output impedance permits useful output currents up to 20mA.

The MAX865 comes in a 1.11mm-high, 8-pin µMAX package that occupies half the board area of a standard 8-pin SOIC. For a device with selectable frequencies and logic-controlled shutdown, refer to the MAX864 data sheet.

Applications

Low-Voltage GaAsFET Bias in Wireless Handsets

VCO and GaAsFET Supplies

Split Supply from 3 Ni Cells or 1 Li+ Cell

Low-Cost Split Supply for Low-Voltage Data-Acquisition Systems

Split Supply for Analog Circuitry

LCD Panels

Features

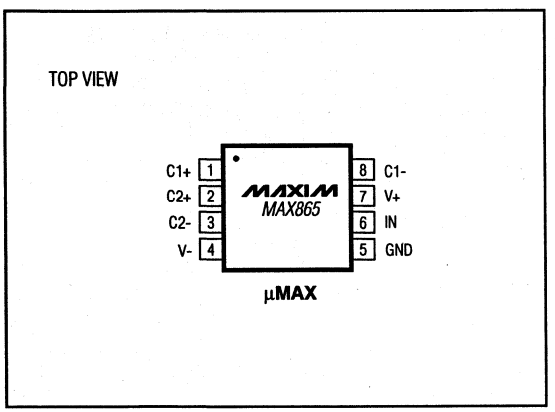
- **1.11mm-High µMAX Package**
- **Compact: Circuit Fits in 0.08in²**
- **Requires Only Four Capacitors**
- **Dual Outputs (positive and negative)**
- **+1.5V to +6.0V Input Voltage**
- **20kHz (min) Frequency (above the audio range)**

Ordering Information

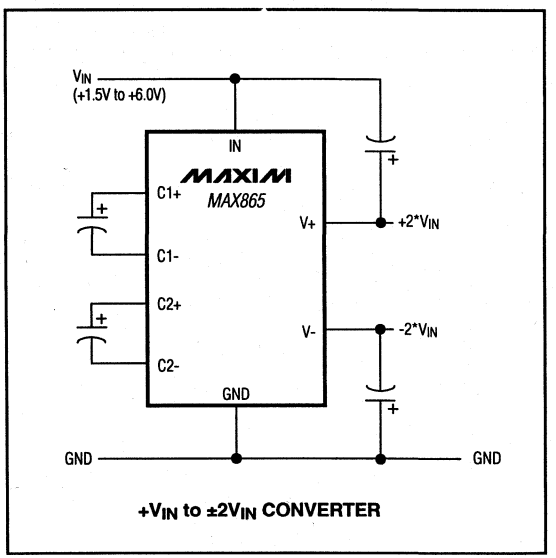
PART	TEMP. RANGE	PIN-PACKAGE
MAX865C/D	0°C to +70°C	Dice
MAX865EUA	-40°C to +85°C	8 µMAX

4

Pin Configuration



Typical Operating Circuit



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Compact, Dual-Output Charge Pump

ABSOLUTE MAXIMUM RATINGS

V+ to GND .....+12V, -0.3V
IN to GND .....+6.2V, -0.3V
V- to GND .....-12V, +0.3V
V- Output Current 100mA
V- Short-Circuit to GND .....Indefinite
Continuous Power Dissipation (T_A = +70°C)
μMAX (derate 4.1mW/°C above +70°C) 330mW

Operating Temperature Range
MAX865EUA .....-40°C to +85°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

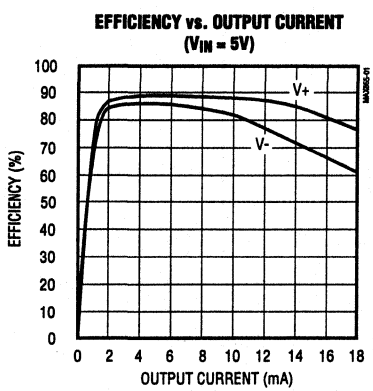
(V_{IN} = 5V, C1 = C2 = C3 = C4 = 3.3μF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

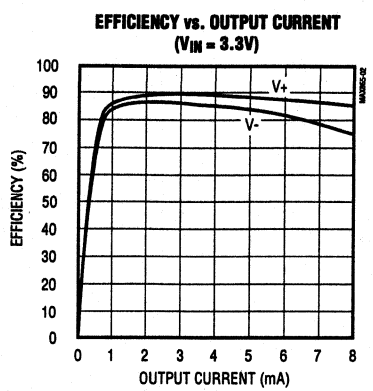
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Supply Voltage	R_{LOAD} = 10kΩ		2.0	1.5		V
Maximum Supply Voltage	R_{LOAD} = 10kΩ				6.0	V
Supply Current	T_A = +25°C			0.6	1.05	mA
	T_A = -40°C to +85°C (Note 1)				1.15	
Oscillator Frequency	T_A = +25°C		19.5	24	32.5	kHz
	T_A = -40°C to +85°C (Note 1)		18		34	
Output Resistance	I_{V+} = 1mA, I_{V-} = 0mA	T_A = +25°C		150	200	Ω
		T_A = T_{MIN} to T_{MAX}			280	
	V+ = 10V (forced), I_{V-} = 1mA	T_A = +25°C		75	100	
		T_A = T_{MIN} to T_{MAX}			140	
Power Efficiency	I_L = 5mA			85		%
Voltage Conversion Efficiency	V+, R_L = ∞		95	99		%
	V-, R_L = ∞		90	98		

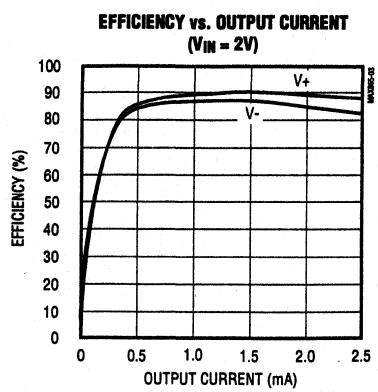
Note 1: These specifications are guaranteed by design and are not production tested.

Typical Operating Characteristics

(Circuit of Figure 1, V_{IN} = 5V, T_A = +25°C, unless otherwise noted.)



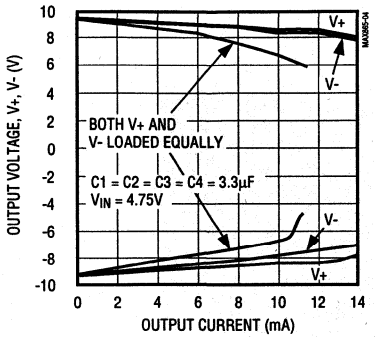




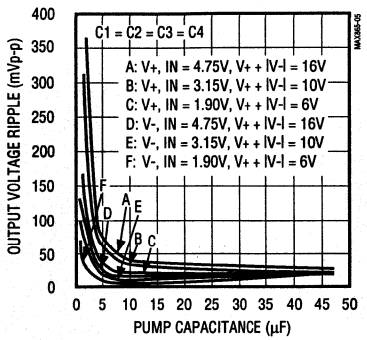
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 5V, T_A = +25°C, unless otherwise noted.)

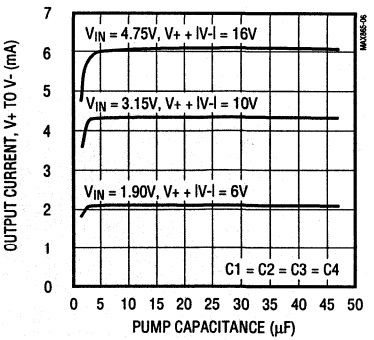
OUTPUT VOLTAGE vs. OUTPUT CURRENT



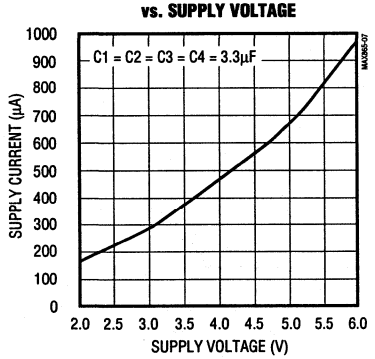
OUTPUT VOLTAGE RIPPLE vs. PUMP CAPACITANCE



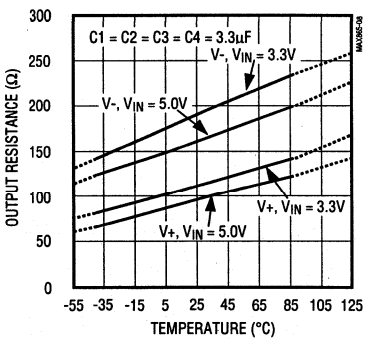
OUTPUT CURRENT vs. PUMP CAPACITANCE



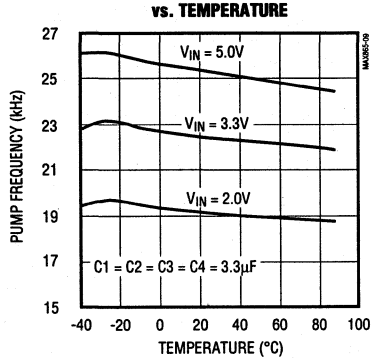
SUPPLY CURRENT vs. SUPPLY VOLTAGE



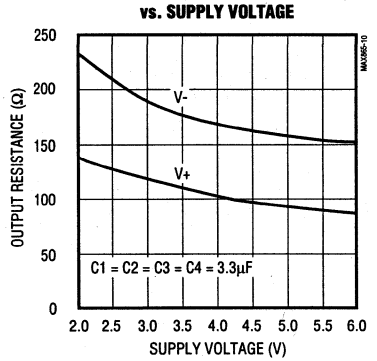
OUTPUT RESISTANCE vs. TEMPERATURE



PUMP FREQUENCY vs. TEMPERATURE



OUTPUT RESISTANCE vs. SUPPLY VOLTAGE

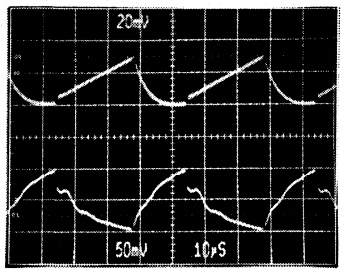


Compact, Dual-Output Charge Pump

Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 5V, T_A = +25°C, unless otherwise noted.)

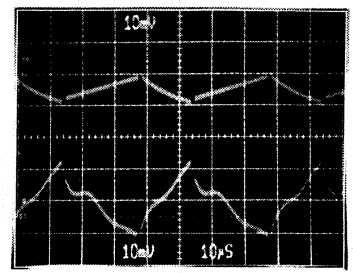
OUTPUT RIPPLE
(C1 = C2 = C3 = C4 = 1µF)



10µs/div

V_{IN} = 4.75V, 1mA LOAD

OUTPUT RIPPLE
(C1 = C2 = C3 = C4 = 3.3µF)



10µs/div

V_{IN} = 4.75V, 1mA LOAD

Pin Description

PIN	NAME	FUNCTION
1	C1+	Positive Terminal of the Flying Boost Capacitor
2	C2+	Positive Terminal of the Flying Inverting Capacitor
3	C2-	Negative Terminal of the Flying Inverting Capacitor
4	V-	Output of the Inverting Charge Pump
5	GND	Ground
6	IN	Positive Power-Supply Input
7	V+	Output of the Boost Charge Pump
8	C1-	Negative Terminal of the Flying Boost Capacitor

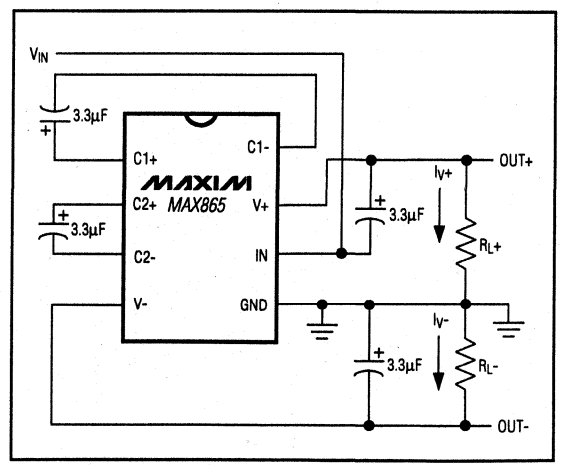


Figure 1. Test Circuit

Detailed Description

The MAX865 contains all the circuitry needed to implement a voltage doubler/inverter. Only four external capacitors are needed. These may be polarized electrolytic or ceramic capacitors with values ranging from 1µF to 100µF.

Figure 2a shows the ideal operation of the positive voltage doubler. The on-chip oscillator generates a 50% duty-cycle clock signal. During the first half cycle, switches S2 and S4 open, switches S1 and S3 close, and capacitor C1 charges to the input voltage (V_{IN}). During the second half cycle, switches S1 and S3 open, switches S2 and S4 close, and capacitor C1 is level shifted upward by V_{IN}. Assuming ideal switches and no load on C3, charge transfers into C3 from C1 such that the voltage on C3 will be $2V_{IN}$, generating the positive supply output (V+).

Figure 2b illustrates the ideal operation of the negative converter. The switches of the negative converter are out of phase with the positive converter. During the second half cycle, switches S6 and S8 open and switches S5 and S7 close, charging C2 from V+ (pumped up to $2V_{IN}$ by the positive charge pump) to GND. In the first half of the clock cycle, switches S5 and S7 open, switches S6 and S8 close, and the charge on capacitor C2 transfers to C4, generating the negative supply. The eight switches are CMOS power MOSFETs. Switches S1, S2, S4, and S5 are P-channel devices, while switches S3, S6, S7, and S8 are N-channel devices.

Charge-Pump Output

The MAX865 is not a voltage regulator: the output source resistance of either charge pump is approximately 150Ω at room temperature with V_{IN} = +5V, and V+ and V- will approach +10V and -10V, respectively, when lightly loaded. Both V+ and V- will droop toward GND as the current draw from either V+ or V- increases, since V- is derived from V+. Treating each converter separately, the droop of the negative supply (V_{DROOP-}) is the product of the current draw from V- (I_{V-}) and the source resistance of the negative converter (RS-):

$$V_{DROOP-} = I_{V-} \times RS-$$

The droop of the positive supply (V_{DROOP+}) is the product of the current draw from the positive supply (I_{LOAD+}) and the source resistance of the positive

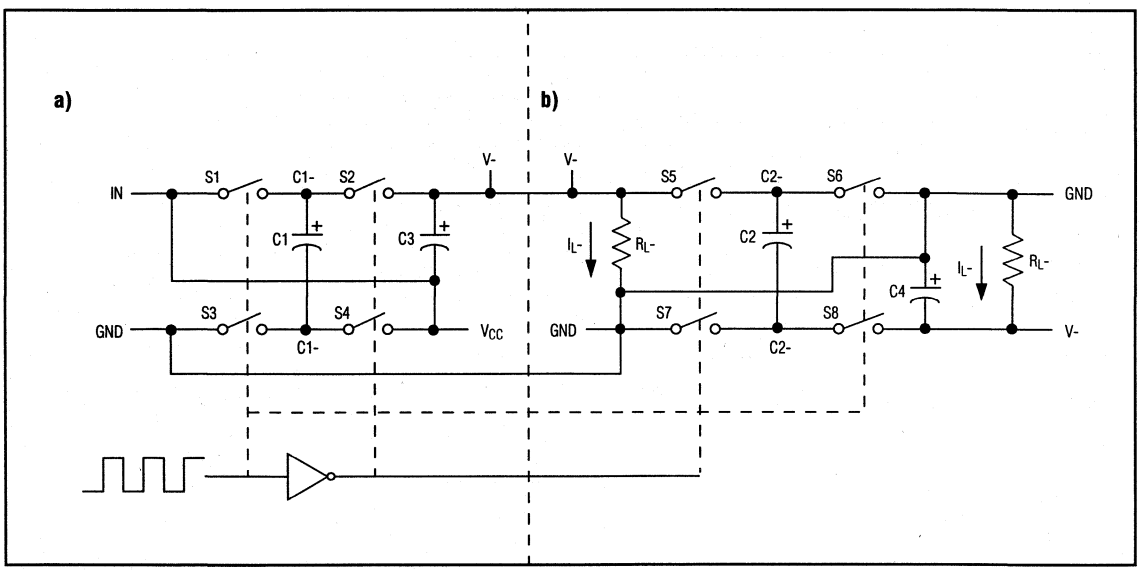


Figure 2. Idealized Voltage Quadrupler: a) Positive Charge Pump; b) Negative Charge Pump

Compact, Dual-Output Charge Pump

converter (RS+), where I_{LOAD+} is the combination of I_{V-} and the external load on V+ (I_{V+}):

$$V_{DROOP+} = I_{LOAD+} \times RS+ = (I_{V+} + I_{V-}) \times RS+$$

Determine V+ and V- as follows:

$$V+ = 2V_{IN} - V_{DROOP+}$$
$$V- = (V+ - V_{DROOP}) = -(2V_{IN} - V_{DROOP+} - V_{DROOP-})$$

The output resistance for the positive and negative charge pumps are tested and specified separately. The positive charge pump is tested with V- unloaded. The negative charge pump is tested with V+ supplied from an external source, isolating the negative charge pump.

Current draw from either V+ or V- is supplied by the reservoir capacitor alone during one half cycle of the clock. Calculate the resulting ripple voltage on either output as follows:

$$V_{RIPPLE} = \frac{1}{2} I_{LOAD} (1 / f_{PUMP}) (1 / C_{RESERVOIR})$$

where I_{LOAD} is the load on either V+ or V-. For the typical f_{PUMP} of 30kHz with 3.3µF reservoir capacitors, the ripple is 25mV when I_{LOAD} is 5mA. Remember that, in most applications, the total load on V+ is the V+ load current (I_{V+}) and the current taken by the negative charge pump (I_{V-}).

Efficiency Considerations

Theoretically, a charge-pump voltage multiplier can approach 100% power efficiency under the following conditions:

- The charge-pump switches have virtually no offset and extremely low on-resistance.
- The drive circuitry consumes minimal power.
- The impedances of the reservoir and pump capacitors are negligible.

For the MAX865, the energy loss per clock cycle is the sum of the energy loss in the positive and negative converters, as follows:

$$LOSS_{CYCLE} = LOSS_{POS} + LOSS_{NEG}$$
$$= \frac{1}{2} C1 \left[(V+)^2 - 2(V+)(V_{IN}) \right] + \frac{1}{2} C2 \left[(V+)^2 - (V-)^2 \right]$$

The average power loss is simply:

$$P_{LOSS} = LOSS_{CYCLE} \times f_{PUMP}$$

Resulting in an efficiency of:

$$\eta = \text{Total Output Power} / (\text{Total Output Power} - P_{LOSS})$$

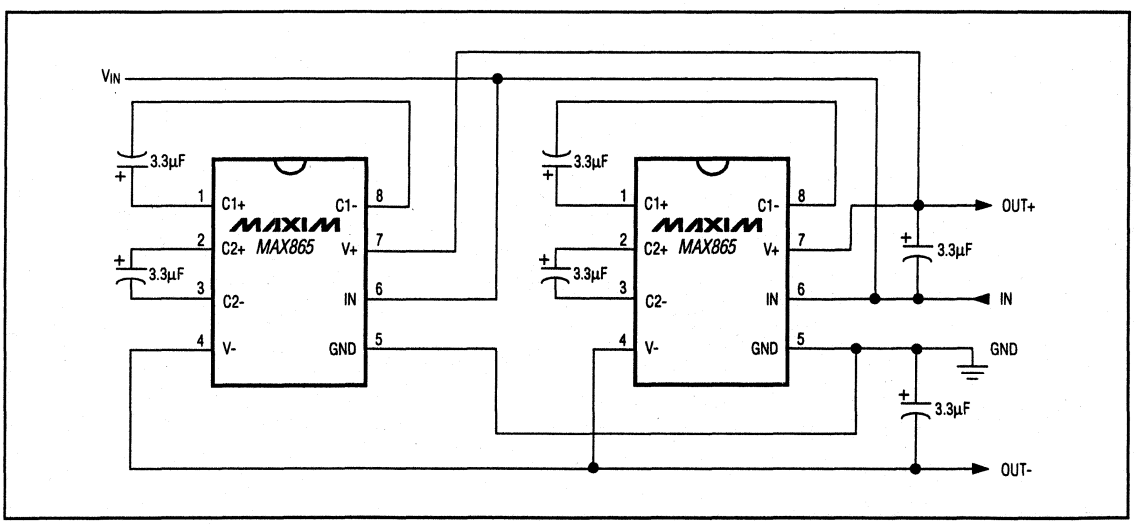


Figure 3. Paralleling MAX865s

A substantial voltage difference exists between (V+ - VIN) and VIN for the positive pump, and between |V+| and |V-| if the impedances of the pump capacitors (C1 and C2) are large with respect to their output loads.

Larger values of reservoir capacitors (C3 and C4) reduce output ripple. Larger values of both pump and reservoir capacitors improve power efficiency.

Charge-Pump Capacitor Selection

To maintain the lowest output resistance, use capacitors with low effective series resistance (ESR). The charge-pump output resistance is a function of C1, C2, C3, and C4's ESR. Therefore, minimizing the charge-pump capacitors' ESR minimizes the total output resistance.

Applications Information

Positive and Negative Converter

The MAX865 is most commonly used as a dual charge-pump voltage converter that provides positive and negative outputs of two times a positive input voltage. The *Typical Operating Circuit* shows that only four external components are needed: capacitors C1 and C3 for the positive pump, C2 and C4 for the negative pump. In most applications, all four capacitors are low-cost, 3.3µF polarized electrolytics. For applications where PC board space is at a premium and very low currents are being drawn from the MAX865, 1µF capacitors may be used for the pump capacitors C1 and C2, with 1µF reservoir capacitors C3 and C4. Capacitors C2 and C4 must be rated at 12V or greater.

Paralleling Devices

Paralleling multiple MAX865s (Figure 3) reduces the output resistance of both the positive and negative converters. The effective output resistance is the output resistance of one device divided by the number of devices. Separate C1 and C2 charge-pump capacitors are required for each MAX865, but the reservoir capacitors C3 and C4 can be shared.

Heavy Output Current Loads

When under heavy loads, where V+ is sourcing current into V- (i.e., load current flows from V+ to V-, rather than from supply to ground), do not allow the V- supply to pull above ground. In applications where large currents flow from V+ to V-, use a Schottky diode (1N5817) between GND and V-, with the anode connected to GND (Figure 4).

Layout and Grounding

Good layout is important, primarily for good noise performance. To ensure good layout:

- Mount all components as close together as possible
- Keep traces short to minimize parasitic inductance and capacitance
- Use a ground plane.

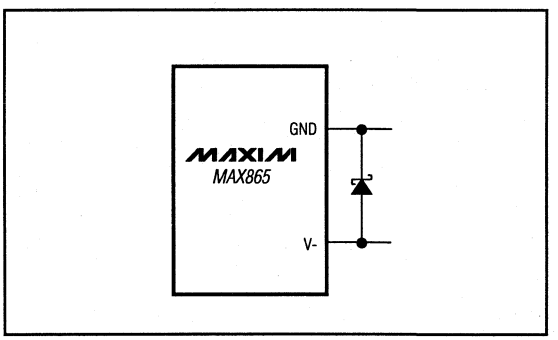


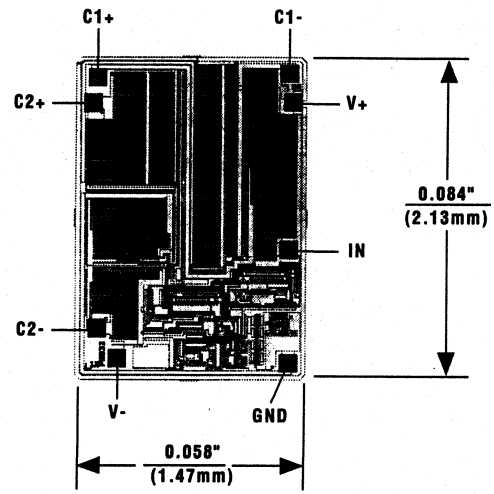
Figure 4. A Schottky diode protects the MAX865 when large currents flow from V+ to V-.

Compact, Dual-Output Charge Pump

Chip Topography

TRANSISTOR COUNT: 80

SUBSTRATE CONNECTED TO V+



19-1142 Rev 0; 9/96

EVALUATION KIT AVAILABLE

MAXIM

100% Duty Cycle, Low-Noise, Step-Down, PWM DC-DC Converter

General Description

The MAX887 high-efficiency, step-down DC-DC converter provides an adjustable output from 1.25V to 10.5V. It accepts inputs from 3.5V to 11V and delivers 600mA. Operation to 100% duty cycle minimizes dropout voltage (300mV typ at 500mA). Synchronous rectification reduces output rectifier losses, resulting in efficiency as high as 95%.

Fixed-frequency pulse-width modulation (PWM) reduces noise in sensitive communications applications. Using a high-frequency internal oscillator allows tiny surface-mount components to reduce PC board area, and eliminates audio-frequency interference. A SYNC input allows synchronization to an external clock to avoid interference with sensitive RF and data-acquisition circuits.

The MAX887 features current-mode operation for superior load/line-transient response. Cycle-by-cycle current limiting protects the internal MOSFET and rectifier. A low-current (2.5µA typ) shutdown mode conserves battery life.

Features

- ♦ **95% Efficiency**
- ♦ **600mA Output Current**
- ♦ **Cycle-by-Cycle Current Limiting**
- ♦ **Low-Dropout, 100% Duty-Cycle Operation, 300mV at 500mA**
- ♦ **Internal 0.6Ω (typ) MOSFET**
- ♦ **Internal Synchronous Rectifier**
- ♦ **High-Frequency Current-Mode PWM**
- ♦ **External SYNC or Internal 300kHz Oscillator**
- ♦ **Guaranteed 260kHz to 340kHz Internal Oscillator Frequency Limits**
- ♦ **2.5µA Shutdown Mode**

Applications

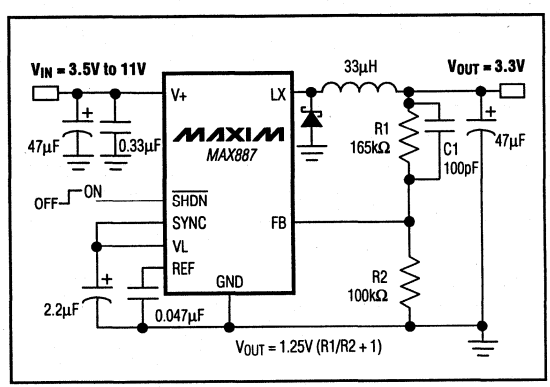
Portable Instruments
Cellular Phones and Radios
Personal Communicators
Distributed Power Systems
Computer Peripherals

Ordering Information

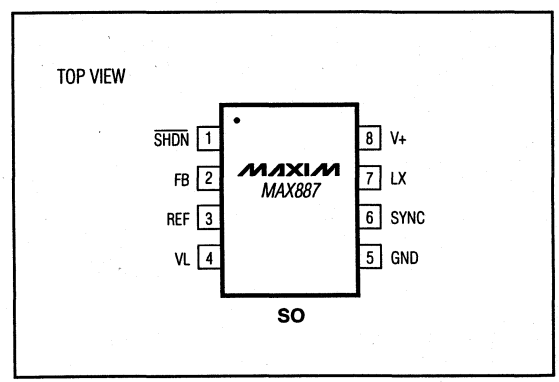
PART	TEMP. RANGE	PIN-PACKAGE
MAX887HC/D	0°C to +70°C	Dice*
MAX887HESA	-40°C to +85°C	8 SO

Contact factory for availability. Dice are tested at T_A = +25°C.

Typical Operating Circuit



Pin Configuration



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

100% Duty Cycle, Low-Noise, Step-Down, PWM DC-DC Converter

ABSOLUTE MAXIMUM RATINGS

REF, FB, SYNC, VL to GND ..... -0.3V to +6V
V+ to GND ..... -0.3V to +12V
$\overline{SHDN}$, LX to GND ..... -0.3V to (V+ + 0.3V)
PGND to GND ..... -0.3V to +0.3V
Continuous Power Dissipation (T_A = +70°C)
SO (derate 9.09mW/°C above +70°C) 471mW

Operating Temperature Ranges
MAX887HC/D.....0°C to +70°C
MAX887HESA.....-40°C to +85°C
Storage Temperature Range ..... -65°C to +165°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +7V, PGND = GND = 0V, $\overline{SHDN}$ = V+, **(T_A = 0°C to T_{MAX})**, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Range	V+		3.5		11.0	V
Quiescent Supply Current (PWM Mode)	$I_{V+, PWM}$	I_{OUT} = 0mA, SYNC = 3.0V		2.7	4.0	mA
Quiescent Supply Current (PFM Mode)	$I_{V+, PFM}$	I_{OUT} = 0mA, SYNC = GND		0.2	0.5	mA
Shutdown Supply Current	$I_{V+, SHDN}$	$\overline{SHDN}$ = GND		2.5	5	µA
Output Voltage Range	$V_{OUT, RANGE}$	Circuit of Figure 2	1.25		10.50	V
Load Regulation		I_{OUT} = 0mA to 500mA		0.005		%/mA
Line Regulation		V_{IN} = 4V to 11V, PWM mode		0.2		%/V
PWM FB Feedback Threshold	V_{FB}	SYNC = 3.0V, PWM duty cycle = 50%	1.225	1.250	1.275	V
FB Input Current	I_{FB}	FB = 1.30V			±0.10	µA
SYNC Frequency	f_{SYNC}		25		440	kHz
SYNC Pulse Width High or Low	SYNC, PW		500			ns
PWM Maximum Duty Cycle	PWM, DUTY	SYNC = 3.0V, FB = 1.18V	100			%
PWM Switching Frequency	f_{OSC}	SYNC = 3.0V	260	300	340	kHz
High-Side Current Limit	I_{LIM+}		0.75	1.0	1.40	A
LX On-Resistance	$R_{ON, LX}$	I_{LX} = ±100mA		0.6		Ω
LX Leakage Current	I_{LXLKG}	V+ = 12V, LX = GND to 12V	-10	1.0	10	µA
LX Reverse Leakage Current, Regulator Off	I_{LXLKGR}	V+ = floating, LX = 5V, $\overline{SHDN}$ = GND		1.0	20	µA
Undervoltage Lockout	$V_{+, UVLO}$	V+ falling		3.0	3.3	V
Startup Voltage	$V_{+, START}$	V+ rising		3.1	3.5	V
SYNC Input High Voltage	$V_{IH, SYNC}$		2.5			V
SYNC Input Low Voltage	$V_{IL, SYNC}$				0.5	V
SYNC Input Current	$I_{IN, SYNC}$	SYNC = GND or 3V			±1	µA
$\overline{SHDN}$ Input High Voltage	$V_{IH, \overline{SHDN}}$		2.4			V
$\overline{SHDN}$ Input Low Voltage	$V_{IL, \overline{SHDN}}$				0.8	V
$\overline{SHDN}$ Input Current, Sinking	$I_{IN-, \overline{SHDN}}$	$\overline{SHDN}$ = GND or V+			±1	µA
$\overline{SHDN}$ Input Capacitance	$C_{IN, \overline{SHDN}}$	(Note 1)			10	pF
VL Output Voltage	V_L	I_{VL} = 0mA to 1mA		3.3		V
REF Output Voltage	V_{REF}	0µA to 30µA		1.25		V

Note 1: Guaranteed by design and not production tested.

100% Duty Cycle, Low-Noise, Step-Down, PWM DC-DC Converter

ELECTRICAL CHARACTERISTICS

(V+ = +7V, PGND = GND = 0V, $\overline{SHDN}$ = V+, **(T_A = -40°C to +85°C)**, unless otherwise noted.) (Note 2)

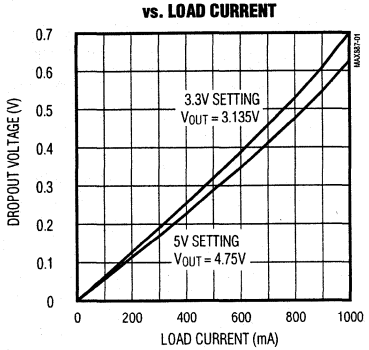
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Range	V+		3.5		11.0	V
Quiescent Supply Current (PWM Mode)	$I_{V+, PWM}$	I_{OUT} = 0mA, SYNC = 3.0V		2.7	4.0	mA
Quiescent Supply Current (PFM Mode)	$I_{V+, PFM}$	I_{OUT} = 0mA, SYNC = GND		0.2	0.6	mA
Shutdown Supply Current	$I_{V+, SHDN}$	$\overline{SHDN}$ = GND		2.5	5	µA
Output Voltage Range	$V_{OUT, RANGE}$	Circuit of Figure 2	1.25		10.50	V
PWM FB Feedback Threshold	V_{FB}	SYNC = 3.0V, PWM duty cycle = 50%	1.222	1.250	1.278	V
FB Input Current	I_{FB}	FB = 1.30V			±0.10	µA
PWM Switching Frequency	f_{OSC}	SYNC = 3.0V	250	300	350	kHz
High-Side Current Limit	I_{LIM+}		0.75	1.00	1.50	A
Undervoltage Lockout	$V_{+, UVLO}$	V+ falling		3.0	3.3	V
Startup Voltage	$V_{+, START}$	V+ rising		3.1	3.5	V

Note 2: Specifications from 0°C to -40°C are guaranteed by design and not production tested.

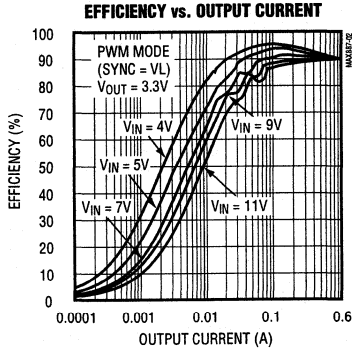
Typical Operating Characteristics

(Circuit of Figure 2, T_A = +25°C, unless otherwise noted.)

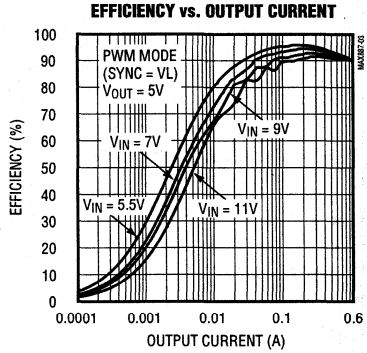
DROPOUT VOLTAGE vs. LOAD CURRENT



EFFICIENCY vs. OUTPUT CURRENT



EFFICIENCY vs. OUTPUT CURRENT

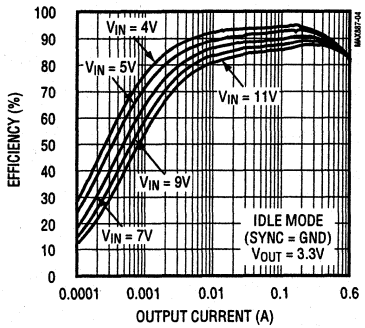


100% Duty Cycle, Low-Noise, Step-Down, PWM DC-DC Converter

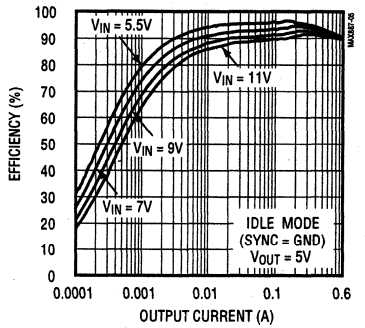
Typical Operating Characteristics (continued)

(Circuit of Figure 2, T_A = +25°C, unless otherwise noted.)

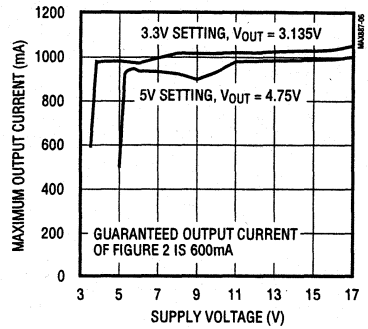
EFFICIENCY vs. OUTPUT CURRENT



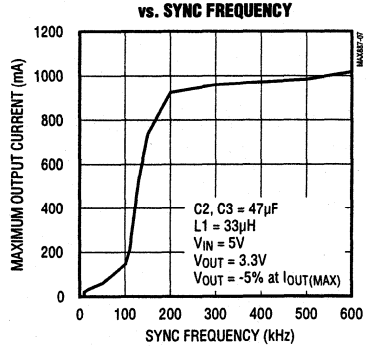
EFFICIENCY vs. OUTPUT CURRENT



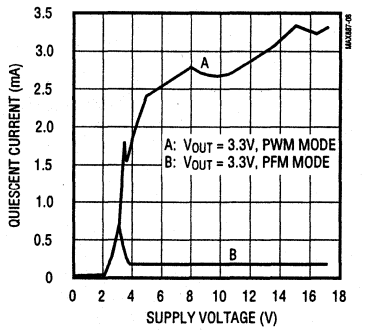
MAXIMUM OUTPUT CURRENT vs. SUPPLY VOLTAGE



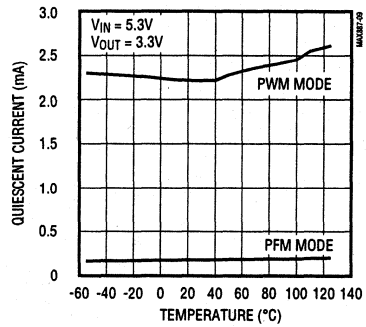
MAXIMUM OUTPUT CURRENT vs. SYNC FREQUENCY



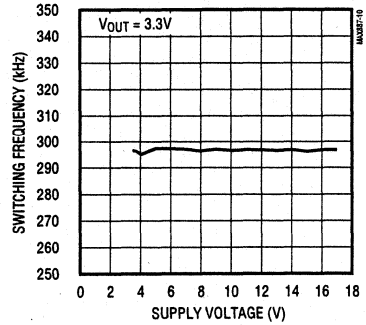
QUIESCENT SUPPLY CURRENT vs. SUPPLY VOLTAGE



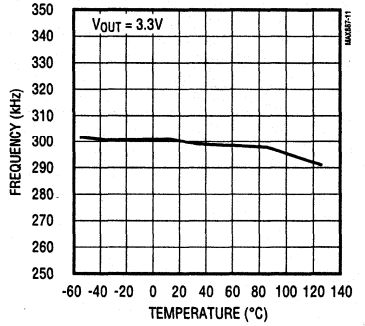
QUIESCENT CURRENT vs. TEMPERATURE



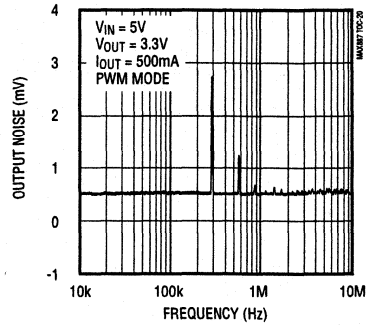
SWITCHING FREQUENCY vs. SUPPLY VOLTAGE



SWITCHING FREQUENCY vs. TEMPERATURE



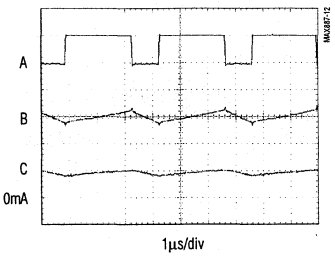
OUTPUT RIPPLE AND HARMONICS



Typical Operating Characteristics (continued)

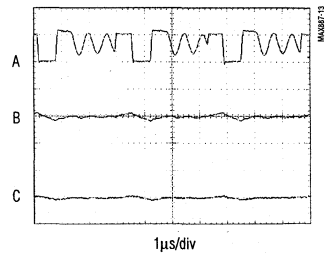
(Circuit of Figure 2, T_A = +25°C, unless otherwise noted.)

HEAVY-LOAD, PWM-MODE SWITCHING WAVEFORMS



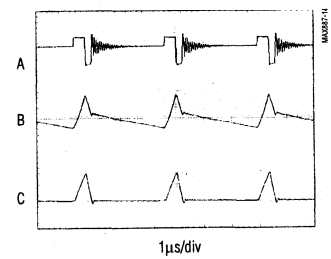
V_{IN} = 5V, V_{OUT} = 3.3V, LOAD = 500mA
A: LX, 5V/div
B: V_{OUT}, 20mV/div, AC COUPLED
C: INDUCTOR CURRENT, 500mA/div

LIGHT-LOAD, PWM-MODE SWITCHING WAVEFORMS



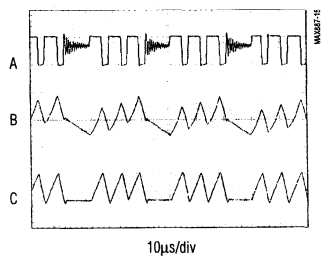
V_{IN} = 5V, V_{OUT} = 3.3V, LOAD = 0mA
A: LX, 5V/div
B: V_{OUT}, 20mV/div, AC COUPLED
C: INDUCTOR CURRENT, 500mA/div

LIGHT-LOAD, PFM-MODE SWITCHING WAVEFORMS



V_{IN} = 5V, V_{OUT} = 3.3V, LOAD = 0mA
A: LX, 5V/div
B: V_{OUT}, 20mV/div, AC COUPLED
C: INDUCTOR CURRENT, 200mA/div

MEDIUM-LOAD, PFM-MODE SWITCHING WAVEFORMS



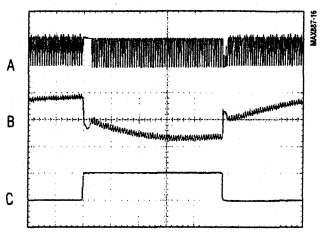
V_{IN} = 5V, V_{OUT} = 3.3V, LOAD = 70mA
A: LX, 5V/div
B: V_{OUT}, 20mV/div, AC COUPLED
C: INDUCTOR CURRENT, 200mA/div

100% Duty Cycle, Low-Noise, Step-Down, PWM DC-DC Converter

Typical Operating Characteristics (continued)

(Circuit of Figure 2, T_A = +25°C, unless otherwise noted.)

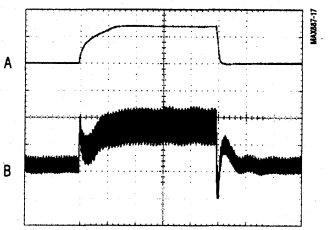
LOAD-TRANSIENT RESPONSE



40µs/div

V_{IN} = 5V, V_{OUT} = 3.3V,
LOAD = 0mA TO 500mA, PWM MODE
A: LX, 5V/div
B: V_{OUT}, 50mV/div, AC COUPLED
C: LOAD CURRENT, 500mA/div

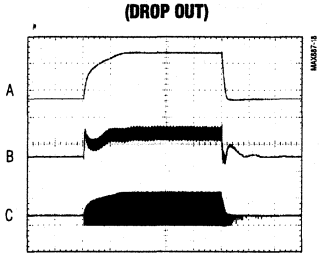
LINE-TRANSIENT RESPONSE



200µs/div

V_{IN} = 5V TO 11V, V_{OUT} = 3.3V,
LOAD = 500mA, PWM MODE
A: V_{IN}, 5V/div
B: V_{OUT}, 20mV/div, AC COUPLED

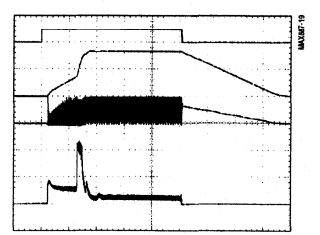
RECOVERY FROM 100% DUTY CYCLE (DROP OUT)



200µs/div

V_{IN} = 3.3V TO 11V, V_{OUT} = 3.3V,
LOAD = 500mA, PWM MODE
A: V_{IN}, 5V/div
B: V_{OUT}, 50mV/div, AC COUPLED
C: LX, 10V/div

SHUTDOWN AND STARTUP RESPONSE



500µs/div

V_{IN} = 5V, V_{OUT} = 3.3V,
LOAD = 100mA, PWM MODE
A: $\overline{SHDN}$, 5V/div
B: V_{OUT}, 2V/div, AC COUPLED
C: LX, 5V/div
D: INDUCTOR CURRENT, 500mA/div

100% Duty Cycle, Low-Noise, Step-Down, PWM DC-DC Converter

Pin Description

PIN	NAME	FUNCTION
1	$\overline{SHDN}$	Shutdown, Active-Low, Logic-Level Input. Connect $\overline{SHDN}$ to V+ for normal operation.
2	FB	Feedback Input. Connect FB to a resistor voltage divider between the output and GND.
3	REF	Reference Bypass Output. Connect a 0.047µF capacitor to GND very close to the MAX887, within 0.2 in. (5mm).
4	VL	3.3V Internal Logic Regulator Output. Bypass VL to GND with a 2.2µF capacitor very close to the MAX887, within 0.2 in. (5mm).
5	GND	Ground
6	SYNC	Oscillator Synchronization and PWM Control Input. SYNC is a logic-level input. Tie SYNC to VL for internal 300kHz PWM operation at all loads. The oscillator synchronizes to the negative edge of an external clock between 10kHz and 400kHz. The MAX887 operates in PWM mode when SYNC is clocked. Tying SYNC to GND allows a reduced supply-current mode at light loads.
7	LX	Inductor Connection to the drain of an internal P-channel MOSFET
8	V+	Supply-Voltage Input. 3.5V min to 11V max. Bypass V+ to GND with a 0.33µF and large-value electrolytic capacitor in parallel. These capacitors must be as close to the V+ and GND pins as possible. Place the 0.33µF capacitor within 0.2 in. (5mm) of the MAX887.

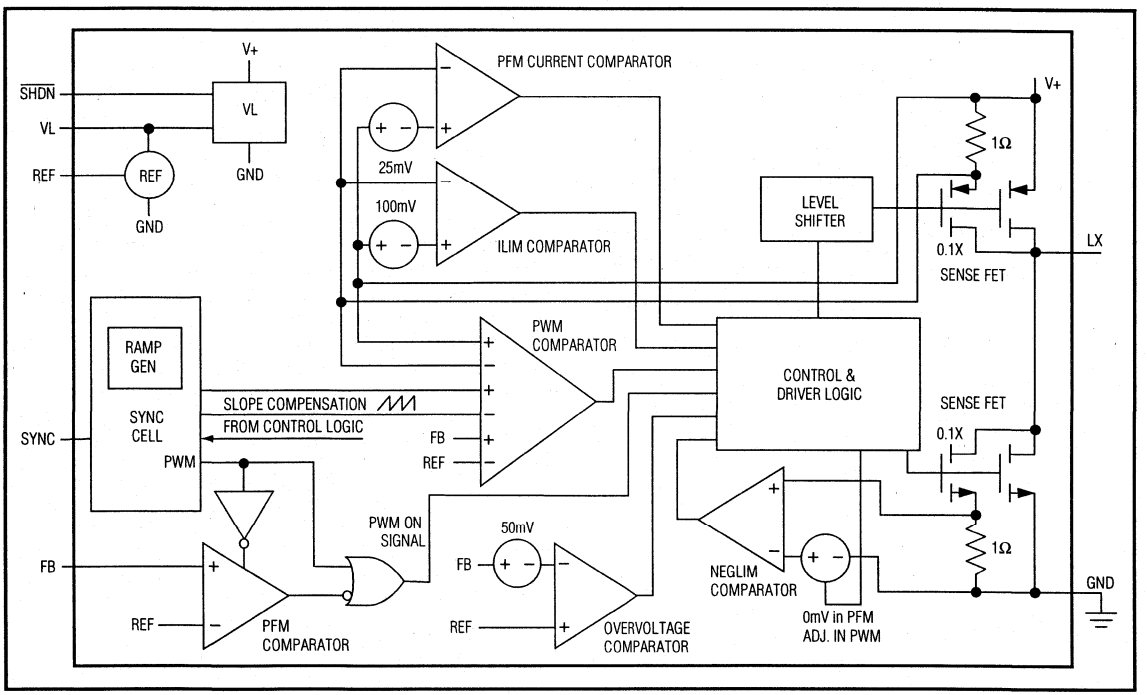


Figure 1. Simplified Functional Block Diagram

100% Duty Cycle, Low-Noise, Step-Down, PWM DC-DC Converter

Detailed Description

The MAX887 is a step-down, pulse-width modulation (PWM) DC-DC converter that provides an adjustable output from 1.25V to 10.5V. It accepts inputs from 3.5V to 11V and delivers up to 600mA. An internal MOSFET and synchronous rectifier reduce PC board area while maintaining high efficiency. Cycle-by-cycle current limiting protects the internal MOSFETs and reduces system stress during overload conditions. Operation with up to 100% duty cycle for an output of 3V and higher minimizes dropout voltage. Fixed-frequency PWM operation reduces interference in sensitive communications and data-acquisition applications. A SYNC input allows synchronization to an external clock. When enabled, Idle Mode™ extends battery life under light loads by placing the regulator in low quiescent current (200µA typ) pulse-frequency modulation (PFM) operation. Shutdown quiescent current is 2.5µA typ.

PWM Control Scheme

The MAX887 uses an oscillator-triggered minimum/maximum on-time current-mode control scheme. The minimum on-time is approximately 280ns unless in dropout. The maximum on-time is approximately $4/f_{OSC}$, allowing operation to 100% duty cycle. Current-mode feedback provides cycle-by-cycle current limiting for superior load and line response and protection of the internal MOSFET and rectifier.

At each falling edge of the internal oscillator, the SYNC cell sends a PWM ON signal to the control and drive logic, turning on the internal P-channel MOSFET (main switch) (Figures 1 and 2). This allows current to ramp up through the inductor (Figure 2) to the load, and stores energy in a magnetic field. The switch remains on until either the current-limit (ILIM) comparator is tripped, the maximum on-time is reached (not shown),

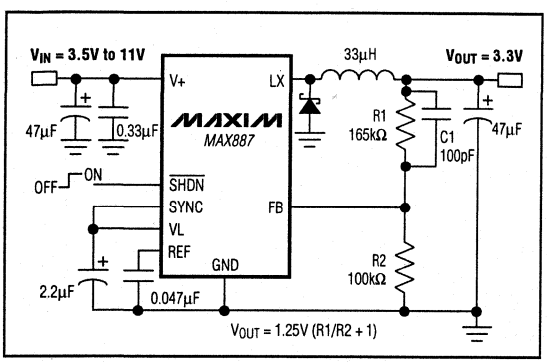


Figure 2. Typical Operating Circuit

or the PWM comparator signals that the output is in regulation. When the switch turns off, during the second half of each cycle, the inductor's magnetic field collapses, releasing the stored energy and forcing current through the output diode to the output filter capacitor and load. The output filter capacitor stores charge when the inductor current is high and releases it when the inductor current is low, smoothing the voltage across the load.

During normal operation, the MAX887 regulates output voltage by switching at a constant frequency and then modulating the power transferred to the load per pulse using the PWM comparator. A multi-input comparator sums three weighted differential signals (the output voltage with respect to the reference, the main switch current sense, and the slope-compensation ramp) and changes states when a threshold is reached. It modulates output power by adjusting the inductor peak current during the first half of each cycle, based on the output error voltage. The MAX887's loop gain is relatively low to enable the use of a small, low-valued output filter capacitor. The resulting load regulation is 2.5% typ at 500mA. Slope compensation is added to account for the inductor current waveform's down slope during the second half of each cycle, and to eliminate the inductor current staircasing characteristic of current-mode controllers at high duty cycles.

100% Duty-Cycle Operation

For the internal oscillator frequency, the $f_{OSC}/4$ maximum on-time exceeds one cycle and permits operation to 100% duty cycle. As the input voltage drops, the duty cycle increases until the P-channel MOSFET is held on continuously and 100% duty cycle is reached. Dropout voltage in 100% duty cycle is the output current multiplied by the on-resistance of the internal switch and inductor around 300mV (I_{OUT} = 500mA). In PWM mode, subharmonic oscillation can occur near dropout, but subharmonic voltage ripple is small, since the ripple current is low. When using synchronization to an external oscillator, 100% duty cycle is available for SYNC frequencies higher than $f_{OSC}/4$.

Synchronous Rectification

Although an external Schottky diode is used as the primary output rectifier, an N-channel synchronous rectifier turns on to reduce power loss across the diode and improve efficiency. During the second half of each cycle, when the inductor current ramps below the threshold set by the NEGLIM comparator or when the end of the oscillator period is reached, the synchronous rectifier turns off. This keeps excess current from flowing

backward through the inductor, from the output filter capacitor to GND, or through the switch and synchronous rectifier to GND.

During PWM operation, the NEGLIM threshold adjusts to permit small amounts of reverse current to flow from the output during light loads. This allows regulation with a constant switching frequency and eliminates minimum load requirements. The NEGLIM comparator threshold is 0mA if VFB < 1.25V, and decreases as VFB exceeds 1.25V to prevent the output from rising. The NEGLIM threshold in PFM mode is 0mA. (See *Forced PWM and Idle Mode operation.*)

Forced PWM and Idle Mode Operation

Connect SYNC to VL for normal forced PWM operation. Forced PWM operation is desirable in sensitive RF and data-acquisition applications, to ensure that switching-noise harmonics do not interfere with sensitive IF and data-sampling frequencies. A minimum load is not required during forced PWM operation, since the synchronous rectifier passes reverse inductor current as needed to allow constant-frequency operation with no load.

Connecting SYNC to GND enables Idle Mode operation. This proprietary control scheme places the MAX887 in PFM mode at light loads to improve efficiency and reduce quiescent current to 200µA typ. With Idle Mode enabled, the MAX887 initiates PFM operation when the output current drops below 100mA. During PFM operation, the MAX887 switches only as needed to service the load, reducing the switching frequency and associated losses in the internal switch and synchronous rectifier, Schottky diode, and external inductor.

During PFM mode, a switching cycle is initiated when the PFM comparator senses that the output voltage has dropped too low. The P-channel MOSFET switch turns on and conducts current to the output filter capacitor and load until the inductor current reaches the PFM peak current limit (100mA). Then the switch turns off and the magnetic field in the inductor collapses, forcing current through the output diode to the output filter capacitor and load. The output filter capacitor stores charge when the inductor current is high and releases charge when it is low, smoothing the voltage across the load. Then the MAX887 waits until the PFM comparator senses a low output voltage again. During PFM mode, the synchronous rectifier is disabled and the external Schottky diode is used as an output rectifier.

The PFM current comparator controls both entry into PWM mode and the peak switching current during PFM mode. Consequently, some jitter is normal during transition from PFM to PWM modes with loads around 100mA, and has no adverse impact on regulation. Output ripple is higher during PFM operation, and the output filter capacitor should be selected on this basis when PFM mode is used. Output ripple and noise are higher during PFM operation.

SYNC Input and Frequency Control

The MAX887H comes with an internal oscillator set for a fixed switching frequency of 300kHz. Connect SYNC to VL for normal forced-PWM operation. Do not leave SYNC floating. Connecting SYNC to GND enables Idle Mode operation to reduce supply current at light loads.

SYNC is a logic-level input useful for operating-mode selection and frequency control. It is a negative edge triggered input that allows synchronization to an external frequency between 25kHz and 440kHz. When SYNC is clocked by an external signal, the converter operates in PWM mode. If SYNC is low or high for more than 100µs, the oscillator defaults to 300kHz. Operating at a lower switching frequency reduces quiescent current, but reduces maximum load current as well (Table 1). For example, at 330kHz, maximum output current is 600mA, while at 30kHz, maximum output current is only 30mA. Note that 100% duty cycle will only occur for $f_{SYNC} > f_{OSC}/4$.

VL Regulator

The MAX887 uses an internal 3.3V linear regulator for logic power in the IC. This logic supply is brought out using the VL pin for bypassing and compensation with an external 2.2µF capacitor to GND. Connect this capacitor close to the MAX887, within 0.2in (5mm).

Shutdown

Connecting $\overline{SHDN}$ to GND places the MAX887 in a low-current shutdown mode (I_Q = 2.5µA typ at V+ = 7V). In shutdown, the reference, VL regulator, control circuitry, internal switching MOSFET, and the synchronous rectifier turn off and the output falls to 0V. Connect $\overline{SHDN}$ to V+ for normal operation.

Current-Sense Comparators

Several internal current-sense comparators are used inside the MAX887. In PWM operation, the PWM comparator is used for current-mode control. Current-mode control imparts cycle-by-cycle current limiting and provides improved load and line response, allowing tighter specification of the inductor saturation current limit to reduce inductor cost. A second 100mA current-sense comparator is used across the P-channel switch to control entry into PFM mode. A third current-sense comparator monitors current through the internal N-channel MOSFET to set the NEGLIM threshold and determine

100% Duty Cycle, Low-Noise, Step-Down, PWM DC-DC Converter

when to turn off this synchronous rectifier. A fourth comparator (ILIM) is used at the P-channel MOSFET switch for overcurrent detection. This protects the system, external components, and internal MOSFETs under overload conditions.

Design Information

Output Voltage Selection

To select an output voltage between 1.25V and 10.5V, connect FB to a resistor voltage divider between the output and GND (Figure 2). Select feedback resistor R2 in the 5kΩ to 100kΩ range, since FB input leakage is ±100nA max. R1 is then given by:

$$R1 = R2\left(\frac{V_{OUT}}{V_{FB}} - 1\right)$$

where V_{FB} = 1.25V. A small ceramic capacitor (C1) around 100pF to 470pF should be added in parallel with R1 to compensate for stray capacitance at the FB pin, and output capacitor equivalent series resistance (ESR).

Inductor Selection

A 1.3A inductor with the value recommended in Table 1 is sufficient for most applications. However, the exact inductor value is not critical, and values within 50% of those in Table 1 are acceptable. For best efficiency, the inductor's DC resistance should be less than 0.25Ω. The inductor saturation current rating must exceed the 1A I_{LIM} current limit. Table 2 lists component suppliers.

Capacitor Selection

Input and output filter capacitors should be chosen to service inductor currents with acceptable voltage ripple. The input filter capacitor also reduces peak currents and noise at the voltage source. See Table 1 for suggested values. The MAX887's loop gain is relatively low, to enable the use of small, low-valued output filter capacitors. Higher values provide improved output ripple and transient response. Lower oscillator frequencies require a larger-value output capacitor. When Idle Mode is used, verify capacitor selection with light loads during PFM operation, since output ripple is higher under these conditions.

Low-ESR capacitors are recommended. Capacitor ESR is a major contributor to output ripple (usually more than 60%). Ordinary aluminum-electrolytic capacitors have high ESR and should be avoided. Low-ESR aluminum-electrolytic capacitors are acceptable and relatively inexpensive. Low-ESR tantalum capacitors are better and provide a compact solution for space-constrained surface-mount designs. Do not exceed the ripple current ratings of tantalum capacitors.

Ceramic capacitors have the lowest ESR overall, and OS-CON capacitors have the lowest ESR of the high-value electrolytic types. It is generally not necessary to use ceramic and OS-CON capacitors for the MAX887; they need only be considered in very compact, high-reliability, or wide-temperature applications, where the expense is justified. When using very-low-ESR capacitors, such as ceramic or OS-CON, check for stability while examining load-transient response, and increase the compensation capacitor C1 if needed. Table 2 lists suppliers for the various components used with the MAX887.

Table 1. Inductor and Output Filter vs. Sync Frequency

SYNC RANGE (kHz)	L1 (µH)	C_{OUT} (µF)
300–400	33	33
200–300	47	47
150–200	68	68
100–150	100	100
75–100	150	150

Table 2. Component Suppliers

COMPANY		PHONE	FAX
AVX	USA	(803) 946-0690 (800) 282-4975	(803) 626-3123
Coilcraft	USA	(847) 639-6400	(847) 639-1469
Coiltronics	USA	(561) 241-7876	(561) 241-9339
Dale	USA	(605) 668-4131	(605) 665-1627
International Rectifier	USA	(310) 322-3331	(310) 322-3332
Motorola	USA	(602) 303-5454	(602) 994-6430
Nichicon	USA Japan	(847) 843-7500 81-7-5231-8461	(847) 843-2798 81-7-5256-4158
Nihon	USA Japan	(805) 867-2555 81-3-3494-7411	(805) 867-2698 81-3-3494-7414
Sanyo	USA Japan	(619) 661-6835 81-7-2070-6306	(619) 661-1055 81-7-2070-1174
Siliconix	USA	(408) 988-8000 (800) 554-5565	(408) 970-3950
Sprague	USA	(603) 224-1961	(603) 224-1430
Sumida	USA Japan	(847) 956-0666 81-3-3607-5111	(847) 956-0702 81-3-3607-5144
United Chemi-Con	USA	(714) 255-9500	(714) 255-9400

Bypass V+ to GND using a 0.33µF capacitor. Also bypass VL to GND with a 2.2µF capacitor, and VREF to GND using a 0.047µF capacitor. These capacitors should be placed within 0.2in (5mm) of their respective pins. A small ceramic capacitor (C1) of around 100pF to 470pF should be added in parallel with R1 to compensate for stray capacitance at the FB pin and output capacitor ESR.

Output Diode Selection

A 1A external diode (D1) is required as an output rectifier to pass inductor current during the second half of each cycle. This diode operates in PFM mode and during transition periods while the synchronous rectifier is off. Use a Schottky diode to prevent the slow internal diode of the N-channel MOSFET from turning on.

PC Board Layout and Routing

High switching frequencies and large peak currents make PC board layout a very important part of design. Poor design can result in excessive EMI on the feedback paths and voltage gradients in the ground plane, both of which can result in instability or regulation errors. Power components, such as the MAX887, inductor, input filter capacitor, and output filter capacitor should be placed as close together as possible, and their traces kept short, direct, and wide. Connect their ground pins at a common node in a star-ground configuration. Keep the extra copper on the board and integrate into ground as a pseudo-ground plane. The external voltage-feedback network should be very close to the FB pin, within 0.2in (5mm). Keep noisy traces, such as from the LX pin, away from the voltage-feedback network, and separate using grounded copper. Place the small bypass capacitors (C1, C3, C5, and C6) within 0.2in (5mm) of their respective pins. The MAX887 evaluation kit manual illustrates an example PC board layout, routing, and pseudo-ground plane.

Chip Information

TRANSISTOR COUNT: 2006

SUBSTRATE CONNECTED TO GND

19-1146; Rev 0; 9/96

MAXIM

1A, Current-Limited, High-Side P-Channel Switch with Thermal Shutdown

General Description

The MAX890L smart, low-voltage, P-channel, MOSFET power switch is intended for high-side load-switching applications. This switch operates with inputs from 2.7V to 5.5V, making it ideal for both 3V and 5V systems. Internal current-limiting circuitry protects the input supply against overload. Thermal-overload protection limits power dissipation and junction temperatures.

The MAX890L's maximum current limit is 1A. The current limit through the switch is programmed with a resistor from SET to ground. The quiescent supply current is a low 10µA. When the switch is off, the supply current decreases to 0.1µA.

The MAX890L is available in an 8-pin SO package.

Features

- ♦ **2.7V to 5.5V Input Range**
- ♦ **Programmable Current Limit**
- ♦ **Low Quiescent Current:**
  10µA (typ) at V_{IN} = 3.3V
  0.1µA (typ) with Switch Off
- ♦ **Thermal Shutdown**
- ♦ **$\overline{FAULT}$ Indicator Output**
- ♦ **0.09Ω (typ) On-Resistance**

Applications

PCMCIA Slots

Access Bus Slots

Portable Equipment

Ordering Information

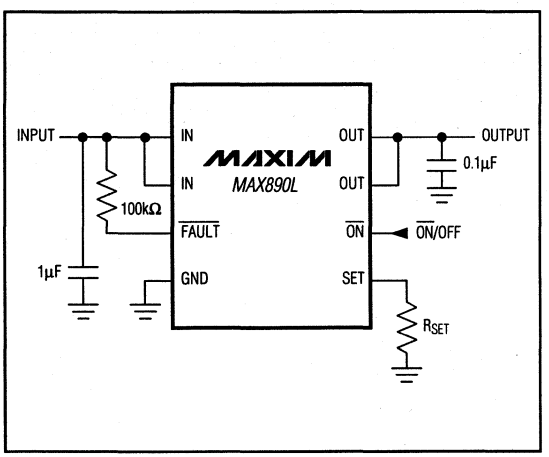
PART*	TEMP. RANGE	PIN-PACKAGE	CURRENT LIMIT
MAX890LC/D	0°C to +70°C	Dice**	1A
MAX890LESA	-40°C to +85°C	8 SO	1A

** To order this unit in tape and reel, add (-T) to the end of the part number.*

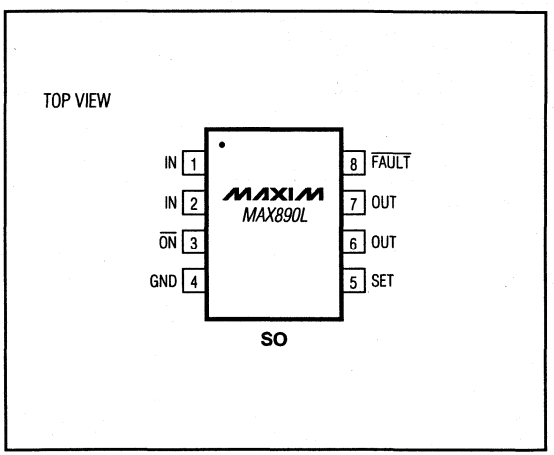
*** Dice are tested at T_A = +25°C.*

4

Typical Operating Circuit



Pin Configuration



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

1A, Current-Limited, High-Side P-Channel Switch with Thermal Shutdown

ABSOLUTE MAXIMUM RATINGS

IN to GND .....-0.3V to 6V
$\overline{ON}$, $\overline{FAULT}$ to GND .....-0.3V to 6V
SET, OUT to GND ..... -0.3V to (V_{IN} + 0.3V)
Maximum Continuous Switch Current 1.5A
Continuous Power Dissipation (T_A = +70°C)
SO (derate 5.88mW/°C above +70°C) 471mW

Operating Temperature Range
MAX890LESA .....-40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3V, **T_A = 0°C to +85°C,** unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage		2.7		5.5	V
Quiescent Current	V_{IN} = 5V, $\overline{ON}$ = GND, I_{OUT} = 0		13	20	µA
Off-Supply Current	$\overline{ON}$ = IN, V_{IN} = V_{OUT} = 5.5V		0.03	1	µA
Off-Switch Current	$\overline{ON}$ = IN, V_{IN} = 5.5V, V_{OUT} = 0		0.04	3	µA
Undervoltage Lockout	Rising edge, 1% hysteresis	2.0	2.4	2.6	V
On-Resistance	V_{IN} = 4.5V		75	130	mΩ
	V_{IN} = 3.0V		90	150	
Current-Limit-Amplifier Threshold	V_{SET} required to turn the switch off (Note 1)	1.178	1.240	1.302	V
Maximum Output Current Limit			1		A
I_{OUT} to I_{SET} Current Ratio	I_{OUT} = 500mA, V_{OUT} = 1.6V to 2.8V	970	1110	1300	A/A
$\overline{ON}$ Input Low Voltage	V_{IN} = 2.7V to 5.5V			0.8	V
$\overline{ON}$ Input High Voltage	V_{IN} = 2.7V to 3.6V	2.0			V
	V_{IN} = 4.5V to 5.5V	2.4			
$\overline{ON}$ Input Leakage	$V_{\overline{ON}}$ = 5.5V		0.01	1	µA
I_{SET} Bias Current	V_{SET} = 1.24V, I_{OUT} = 0		0.5	3	µA
$\overline{FAULT}$ Logic Output Low Voltage	I_{SINK} = 1mA, V_{SET} = 1.4V			0.4	V
$\overline{FAULT}$ Logic Output High Leakage Current	$V_{\overline{FAULT}}$ = 5.5V, V_{SET} = 1V		0.05	1	µA
Slow-Current-Loop Response Time	20% current overdrive, V_{CC} = 5V		5		µs
Fast-Current-Loop Response Time			2		µs
Turn-On Time	V_{IN} = 5V, I_{OUT} = 500mA		120	200	µs
	V_{IN} = 3V, I_{OUT} = 500mA		185		
Turn-Off Time	V_{IN} = 5V	2	5		µs

Note 1: Tested with I_{OUT} = 100mA and V_{SET} raised until V_{IN} - V_{OUT} ≥ 0.8V.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3V, **T_A = -40°C to +85°C,** unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage		2.9		5.5	V
Quiescent Current	V_{IN} = 5V, $\overline{ON}$ = GND, I_{OUT} = 0			50	µA
Off-Supply Current	$\overline{ON}$ = IN, V_{IN} = V_{OUT} = 5.5V			2.2	µA
Off-Switch Current	$\overline{ON}$ = IN, V_{IN} = 5.5V, V_{OUT} = 0			8	µA
Undervoltage Lockout	Rising edge, 1% hysteresis	2.0		2.9	V
On-Resistance	V_{IN} = 4.5V			130	mΩ
	V_{IN} = 3.0V			150	
Current-Limit-Amplifier Threshold	V_{SET} required to turn the switch off (Note 1)	1.14		1.34	V
I_{OUT} to I_{SET} Current Ratio	I_{OUT} = 500mA, V_{OUT} = 1.6V to 2.8V	925		1390	A/A
$\overline{FAULT}$ Logic Output Low Voltage	I_{SINK} = 1mA, V_{SET} = 1V			0.4	V
Turn-On Time	V_{IN} = 5V			200	µs
Turn-Off Time	V_{IN} = 5V	1		20	µs

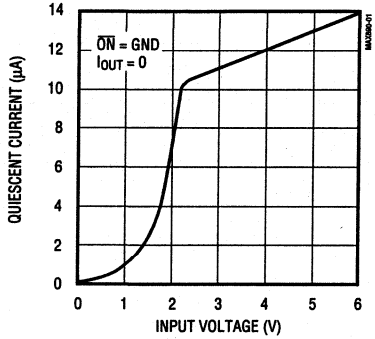
Note 2: Specifications to -40°C are guaranteed by design, not production tested.

1A, Current-Limited, High-Side P-Channel Switch with Thermal Shutdown

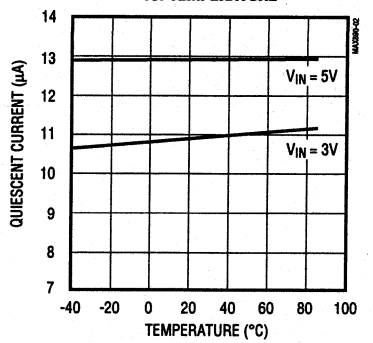
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

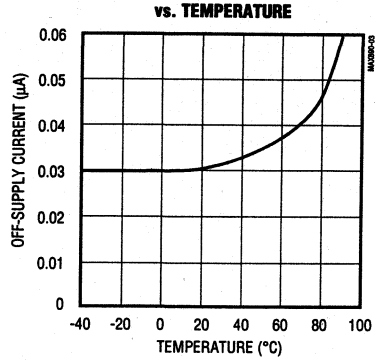
QUIESCENT CURRENT vs. INPUT VOLTAGE



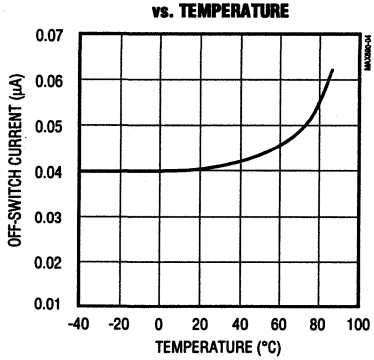
QUIESCENT CURRENT vs. TEMPERATURE



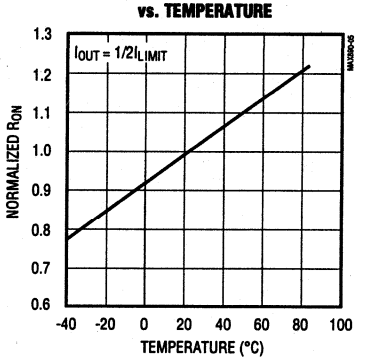
OFF-SUPPLY CURRENT vs. TEMPERATURE



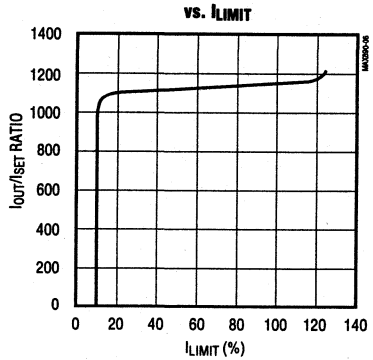
OFF-SWITCH CURRENT vs. TEMPERATURE



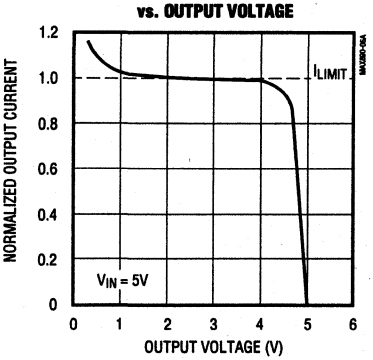
NORMALIZED ON-RESISTANCE vs. TEMPERATURE



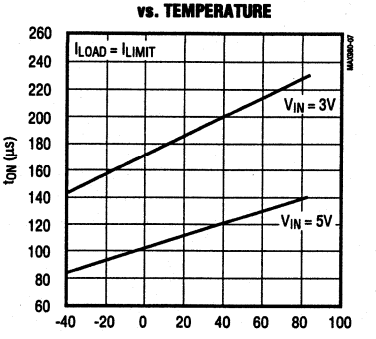
IOUT/ISET RATIO vs. ILIMIT



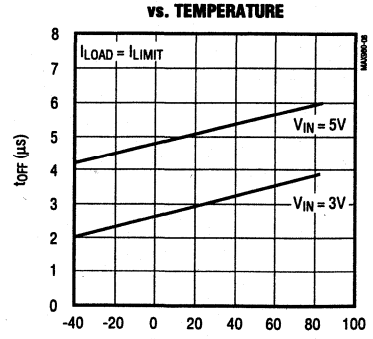
NORMALIZED OUTPUT CURRENT vs. OUTPUT VOLTAGE



TURN-ON TIME vs. TEMPERATURE



TURN-OFF TIME vs. TEMPERATURE

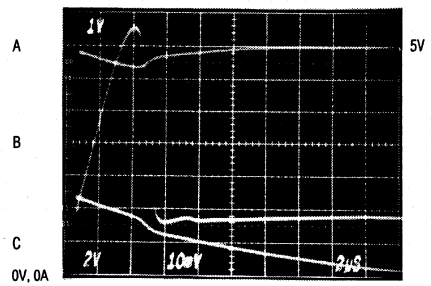


1A, Current-Limited, High-Side P-Channel Switch with Thermal Shutdown

Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

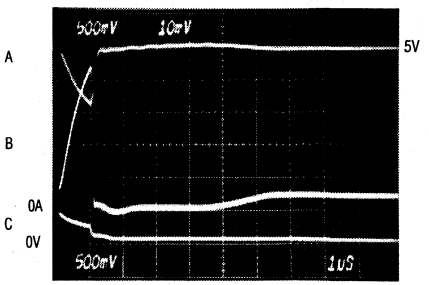
CURRENT-LIMIT RESPONSE
(R_L = 0.6Ω)



2µs/div

C_{IN} = 100µF, C_{OUT} = 0.1µF
A: V_{IN}, 1V/div, AC COUPLED
B: I_{OUT}, 1A/div
C: V_{OUT}, 2V/div

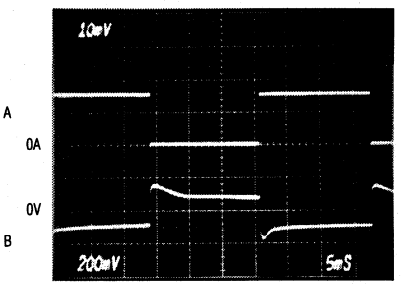
CURRENT-LIMIT RESPONSE
(R_L = 0.5Ω)



1µs/div

C_{IN} = 47µF, C_{OUT} = 0.1µF
A: V_{IN}, 500mV/div, AC COUPLED
B: I_{OUT}, 2A/div
C: V_{OUT}, 5V/div

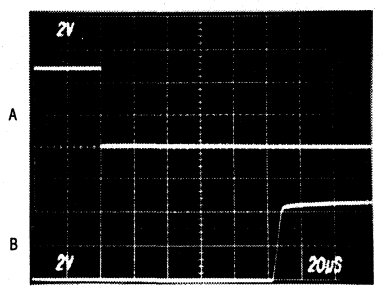
LOAD-TRANSIENT RESPONSE



5ms/div

V_{IN} = 5V
A: I_{OUT} = 0mA TO 750mA, 0.5A/div
B: V_{OUT} RIPPLE, 200mV/div, AC COUPLED

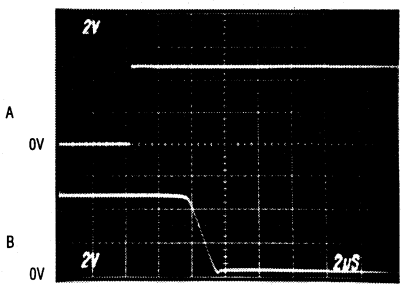
SWITCH TURN-ON TIME



20µs/div

V_{IN} = 5V, I_{OUT} = I_{LIMIT}
A: V_{ON}, 2V/div
B: V_{OUT}, 2V/div

SWITCH TURN-OFF TIME



2µs/div

V_{IN} = 5V, I_{OUT} = I_{LIMIT}
A: $V_{\overline{ON}}$, 2V/div
B: V_{OUT}, 2V/div

1A, Current-Limited, High-Side P-Channel Switch with Thermal Shutdown

Pin Description

PIN	NAME	FUNCTION
1, 2	IN	Input. P-channel MOSFET source. Bypass IN with a 1µF capacitor to ground.
3	$\overline{ON}$	Active-Low Switch On Input. A logic low turns the switch on.
4	GND	Ground
5	SET	Set Current-Limit Input. A resistor from SET to ground sets the current limit for the switch. $R_{SET} = 1.38 \times 10^3 / I_{LIMIT}$, where I_{LIMIT} is the desired current limit in amperes.
6, 7	OUT	Switch Output. P-channel MOSFET drain. Bypass OUT with a 0.1µF capacitor to ground.
8	$\overline{FAULT}$	Fault-Indicator Output. This open-drain output goes low when in current limit or when the die temperature exceeds +135°C.

Detailed Description

The MAX890L P-channel MOSFET power switch limits output current to a programmed level. When the output current is increased beyond the programmed current limit, or 1A (I_{MAX}), the current also increases through the replica switch ($I_{OUT}/1110$) and through R_{SET} (Figure 1). The current-limit error amplifier compares the voltage across R_{SET} to the internal 1.24V reference, and regulates the current back to the lesser of the programmed limit (I_{LIMIT}) or 1A.

This switch is not bidirectional; therefore, the input voltage must be higher than the output voltage.

Setting the Current Limit

The MAX890L features internal current-limiting circuitry with a maximum programmable value (I_{MAX}) of 1A. For best performance, set the current limit (I_{LIMIT}) between $0.2\ I_{MAX} \le I_{LIMIT} \le I_{MAX}$. This current limit remains in effect throughout the input supply-voltage range.

Program the current limit with a resistor (R_{SET}) from SET to ground (Figure 2) as follows:

$$I_{SET} = I_{LIMIT} / 1110$$

$$R_{SET} = 1.24V / I_{SET} = 1.38 \times 10^3 / I_{LIMIT}$$

where I_{LIMIT} is the desired current limit.

Short-Circuit Protection

The MAX890L is a short-circuit-protected switch. In the event of an output short circuit or current-overload condition, the current through the switch is limited by the internal current-limiting error amplifier to 1.5 x I_{LIMIT}. When the fault condition is removed, the replica error amplifier will set the current limit back to I_{LIMIT}.

For a high dV_{DS}/dt during an output short-circuit condition, the switch turns off and disconnects the input supply from the output. The current-limiting amplifier then slowly turns the switch on with the output current limited to 1.5 x I_{LIMIT}. When the fault condition is removed, the current limit is set back to I_{LIMIT}. Refer to Output Short-Circuit Fast-Loop Response and Output Short-Circuit Slow-Loop Response in the *Typical Operating Characteristics*.

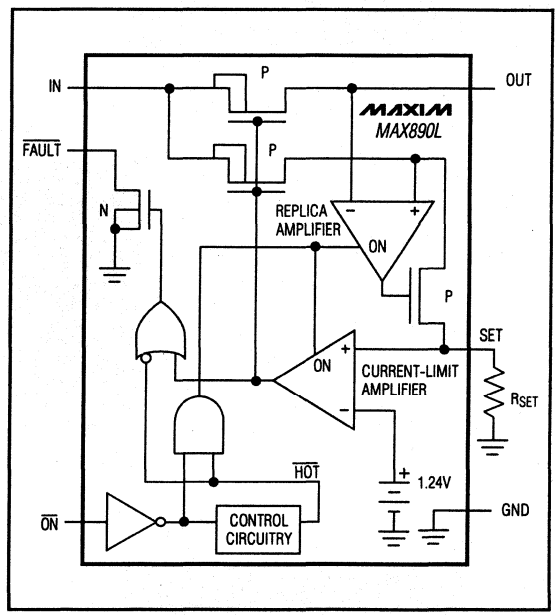


Figure 1. Functional Diagram

1A, Current-Limited, High-Side P-Channel Switch with Thermal Shutdown

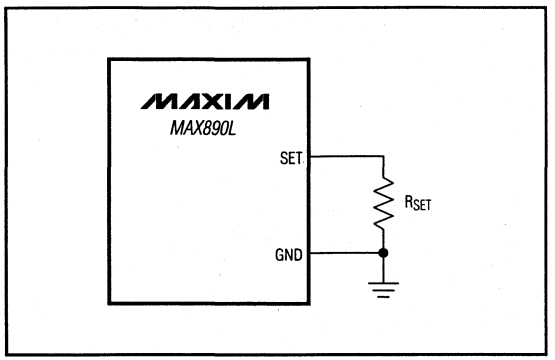


Figure 2. Setting the Current Limit

Thermal Shutdown

The MAX890L features thermal shutdown. The switch turns off when the junction temperature exceeds +135°C. Once the device cools by 10°C, the switch turns back on. If the fault short-circuit condition is not removed, the switch will cycle on and off, resulting in a pulsed output.

Fault Indicator

The MAX890L provides a fault output ($\overline{FAULT}$). This open-drain output goes low when in current limit or when the die temperature exceeds +135°C. A 100kΩ pull-up resistor from $\overline{FAULT}$ to IN provides a logic-control signal.

Applications Information

Input Capacitor

To limit the input voltage drop during momentary output short-circuit conditions, connect a capacitor from IN to GND. A 1µF ceramic capacitor will be adequate for most applications; however, higher capacitor values will further reduce the voltage drop at the input.

Output Capacitor

Connect a 0.1µF capacitor from OUT to GND. One function of this capacitor is to prevent inductive parasitics from pulling OUT negative during turn-off.

Layout and Thermal-Dissipation Consideration

To take full advantage of the switch-response time to output short-circuit conditions, it is very important to keep all traces as short as possible to reduce the effect of undesirable parasitic inductance. Place input and output capacitors as close as possible to the device (no more than 5mm).

Under normal operating conditions, the package can dissipate and channel heat away. Calculate the maximum power as follows:

$$P = I^2_{LIMIT} \times R_{ON}$$

where R_{ON} is the on-resistance of the switch.

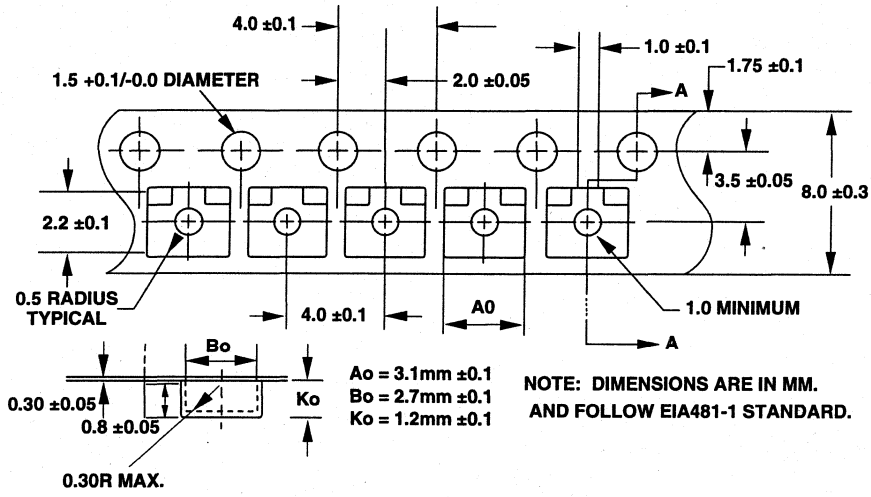
When the output is short circuited, the voltage drop across the switch equals the input supply. Hence, the power dissipated across the switch increases, as does the die temperature. If the fault condition is not removed, the thermal-overload-protection circuitry turns the switch off until the die temperature falls by 10°C. A ground plane in contact with the device will help dissipate additional heat.

Chip Information

TRANSISTOR COUNT: 396

1A, Current-Limited, High-Side P-Channel Switch with Thermal Shutdown

Tape-and-Reel Information



ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

10/96

MAXIM

Current-Limited, High-Side P-Channel Switches with Thermal Shutdown

General Description

The MAX891L/MAX892L smart, low-voltage, P-channel, MOSFET power switches are intended for high-side load-switching applications. These switches operate with inputs from +2.7V to +5.5V, making them ideal for both 3V and 5V systems. Internal current-limiting circuitry protects the input supply against overload. Thermal-overload protection limits power dissipation and junction temperatures.

The MAX891L/MAX892L's maximum current limits are 500mA and 250mA, respectively. The current through the switch is programmed with a resistor from SET to ground. The quiescent supply current is a low 10µA. When the switch is off, the quiescent current decreases to 0.1µA.

The MAX891L/MAX892L are available in 8-pin µMAX packages.

Applications

PCMCIA Slots

Access Bus Slots

Portable Equipment

Features

- **+2.7V to +5.5V Input Range**
- **Programmable Current Limit**
- **Low Quiescent Current:**
  10µA (typ) at V_{IN} = 3.3V
  0.1µA (typ) with Switch Off
- **Thermal Shutdown**
- **$\overline{FAULT}$ Indicator Output**
- **Tiny µMax Package**

Ordering Information

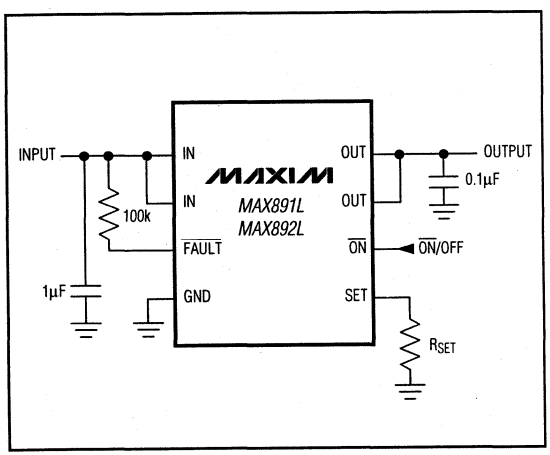
PART*	TEMP. RANGE	PIN-PACKAGE	CURRENT LIMIT
MAX891LC/D	0°C to +70°C	Dice**	500mA
MAX891LEUA	-40°C to +85°C	8 µMAX	500mA
MAX892LC/D	0°C to +70°C	Dice**	250mA
MAX892LEUA	-40°C to +85°C	8 µMAX	250mA

** To order these units in tape and reel, add (-T) to the end of the part number.*

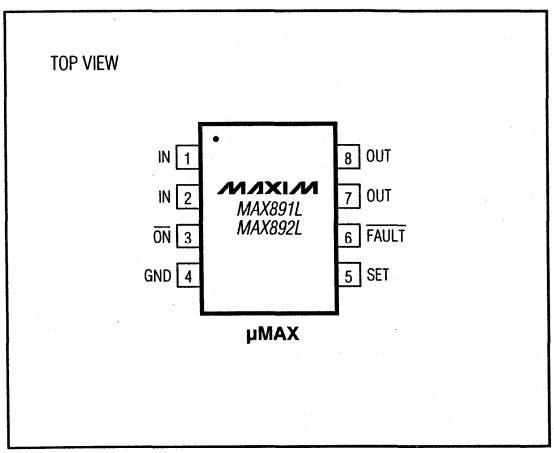
*** Dice are tested at T_A = +25°C.*

4

Typical Operating Circuit



Pin Configuration



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

19-1153; Rev 0a; 1/97

MAXIM

Dual, Current-Limited, High-Side P-Channel Switches with Thermal Shutdown

General Description

The MAX894L/MAX895L smart, dual, low-voltage, P-channel, MOSFET power switches are intended for high-side load-switching applications. These switches operate with inputs from +2.7V to +5.5V, making them ideal for both 3V and 5V systems. Internal current-limiting circuitry protects the input supply against overload. Thermal-overload protection limits power dissipation and junction temperature.

The MAX894L/MAX895L's maximum current limits are 500mA and 250mA, respectively. The current limit through the switches is programmed with resistors from SET A/SET B to ground. When the switches are on, the quiescent supply current is a low 16µA. When the switches are off, the supply current decreases to 0.1µA.

The MAX894L/MAX895L are available in an 8-pin SO package.

Applications

PCMCIA Slots

Access Bus Slots

Portable Equipment

Features

- ♦ **+2.7V to +5.5V Input Range**
- ♦ **Programmable Current Limits**
- ♦ **Low Supply Current:**
  16µA I_Q at V_{IN} = 3.3V
  0.1µA with Switch Off
- ♦ **Thermal Shutdown**

Ordering Information

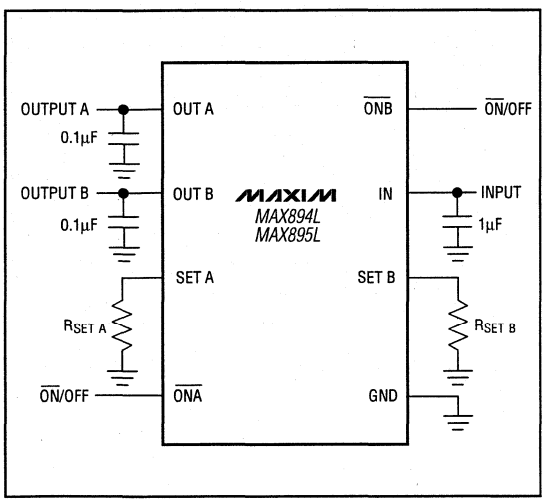
PART*	TEMP. RANGE	PIN-PACKAGE	CURRENT LIMIT
MAX894LC/D	0°C to +70°C	Dice**	500mA
MAX894LESA	-40°C to +85°C	8 SO	500mA
MAX895LC/D	0°C to +70°C	Dice**	250mA
MAX895LESA	-40°C to +85°C	8 SO	250mA

*To order these units in tape and reel, add (-T) to the end of the part number.

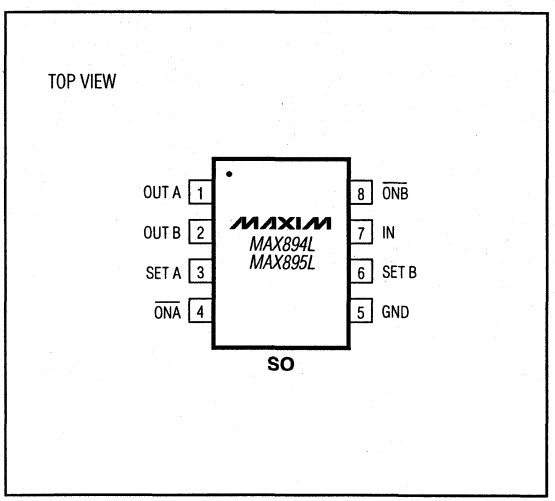
**Dice are tested at T_A = +25°C.

4

Typical Operating Circuit



Pin Configuration



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Dual, Current-Limited, High-Side P-Channel Switches with Thermal Shutdown

ABSOLUTE MAXIMUM RATINGS

IN to GND .....-0.3V to 6V
$\overline{ONA}$, $\overline{ONB}$ to GND .....-0.3V to 6V
SET A, SET B, OUT A, OUT B to GND .....-0.3V to (V_{IN} + 0.3V)
Maximum Continuous Switch Current
MAX894L 0.75A
MAX895L 0.375A

Continuous Power Dissipation (T_A = +70°C)
SO (derate 5.88mW/°C above +70°C) 471mW
Operating Temperature Range
MAX89_LESA .....-40°C to +85°C
Storage Temperature Range .....-65°C to+150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3V, **T_A = 0°C to +85°C,** unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITION		MIN	TYP	MAX	UNITS
Operating Voltage			2.7		5.5	V
Quiescent Current	V_{IN} = 5V, $\overline{ONA}$ = $\overline{ONB}$ = GND, $I_{OUT\ A}$ = $I_{OUT\ B}$ = 0			18	30	µA
Off-Supply Current	$\overline{ONA}$ = $\overline{ONB}$ = IN, V_{IN} = $V_{OUT\ A}$ = $V_{OUT\ B}$ = 5.5V			0.03	1	µA
Off-Switch Current	$\overline{ONA}$ = $\overline{ONB}$ = IN, V_{IN} = 5.5V, $V_{OUT\ A}$ = $V_{OUT\ B}$ = 0			0.04	3	µA
Undervoltage Lockout	Rising edge, 1% hysteresis		2.0	2.4	2.6	V
On-Resistance	V_{IN} = 4.5V	MAX894L		120	225	mΩ
		MAX895L		250	420	
	V_{IN} = 3.0V	MAX894L		150	300	
		MAX895L		300	500	
Current-Limit-Amplifier Threshold	V_{SET} required to turn the switch off (Note 1)		1.178	1.240	1.302	V
Maximum Output Current	MAX894L			500		mA
	MAX895L			250		
I_{OUT} to I_{SET} Current Ratio	V_{OUT} = 1.6V to 2.8V	MAX894L, I_{OUT} = 250mA	945	1085	1270	A/A
		MAX895L, I_{OUT} = 125mA	910	1050	1235	
$\overline{ONA}$, $\overline{ONB}$ Input Low Voltage	V_{IN} = 2.7V to 5.5V				0.8	V
$\overline{ONA}$, $\overline{ONB}$ Input High Voltage	V_{IN} = 2.7V to 3.6V		2.0			V
	V_{IN} = 4.5V to 5.5V		2.4			
$\overline{ONA}$, $\overline{ONB}$ Input Leakage	$V_{\overline{ONA}}$ = $V_{\overline{ONB}}$ = 5.5V			0.01	1	µA
I_{SETA}, I_{SETB} Bias Current	$V_{SET\ A}$ = 1.24V, $\overline{ONA}$ = 0, $\overline{ONB}$ = V_{IN}, $I_{OUT\ A}$ = 0			0.5	3	µA
	$V_{SET\ B}$ = 1.24V, $\overline{ONB}$ = 0, $\overline{ONA}$ = V_{IN}, $I_{OUT\ B}$ = 0			0.5	3	
Slow-Current-Loop Response Time	20% current overdrive, V_{CC} = 5V			5		µs
Fast-Current-Loop Response Time				2		µs
Turn-On Time	V_{IN} = 5V, I_{OUT} = 250mA (MAX894L), 125mA (MAX895L)			100	200	µs
	V_{IN} = 3V, I_{OUT} = 250mA (MAX894L), 125mA (MAX895L)			150		
Turn-Off Time			0.8	1.2	20	µs

Note 1: Tested with I_{OUT} = 50mA for the MAX894L and 25mA for the MAX895L, and V_{SET} raised until V_{IN} - V_{OUT} ≥ 0.8V.

ELECTRICAL CHARACTERISTICS (Note 2)

(V_{IN} = 3V, **T_A = -40°C to +85°C,** unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITION		MIN	TYP	MAX	UNITS
Operating Voltage			3.0		5.5	V
Quiescent Current	V_{IN} = 5V, $\overline{ONA}$ = $\overline{ONB}$ = GND, $I_{OUT\ A}$ = $I_{OUT\ B}$ = 0				50	µA
Off-Supply Current	$\overline{ONA}$ = $\overline{ONB}$ = IN, V_{IN} = $V_{OUT\ A}$ = $V_{OUT\ B}$ = 5.5V				2.2	µA
Off-Switch Current	$\overline{ONA}$ = $\overline{ONB}$ = IN, V_{IN} = 5.5V, $V_{OUT\ A}$ = $V_{OUT\ B}$ = 0				8	µA
Undervoltage Lockout	Rising edge, 1% hysteresis		2.0		2.9	V
On-Resistance	V_{IN} = 4.5V	MAX894L			250	mΩ
		MAX895L			420	
	V_{IN} = 3.0V	MAX894L			300	
		MAX895L			500	
Current-Limit-Amplifier Threshold	$V_{SET_}$ required to turn the switch off (Note 1)		1.14		1.34	V
I_{OUT} to I_{SET} Current Ratio	V_{SET} = 1.24V, V_{OUT} = 1.6V to 2.8V	MAX894L, I_{OUT} = 250mA	910		1360	A/A
		MAX895L, I_{OUT} = 125mA	880		1315	
Turn-On Time	V_{IN} = 5V				200	µs
Turn-Off Time			0.25		20	µs

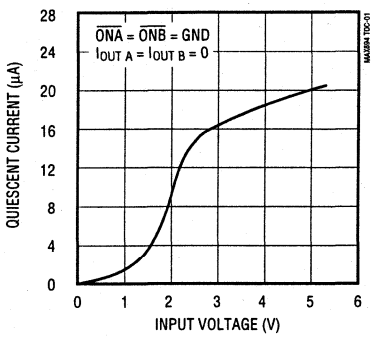
Note 2: Specifications to -40°C are guaranteed by design, not production tested.

Dual, Current-Limited, High-Side P-Channel Switches with Thermal Shutdown

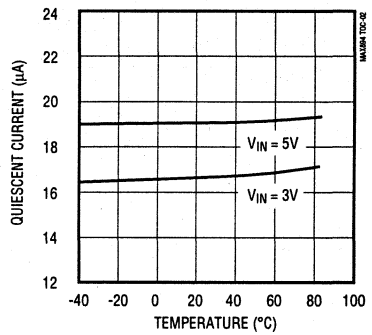
Typical Operating Characteristics

(Typical Operating Circuit, T_A = +25°C, unless otherwise noted.)

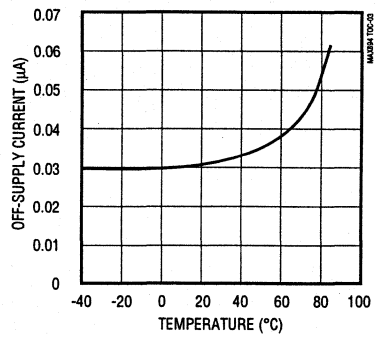
QUIESCENT CURRENT vs. INPUT VOLTAGE



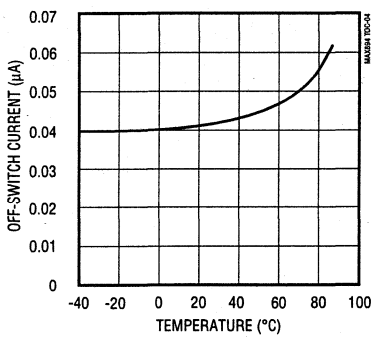
QUIESCENT CURRENT vs. TEMPERATURE



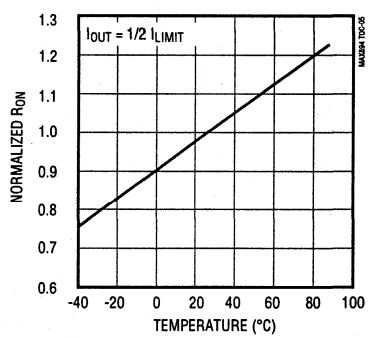
OFF-SUPPLY CURRENT vs. TEMPERATURE



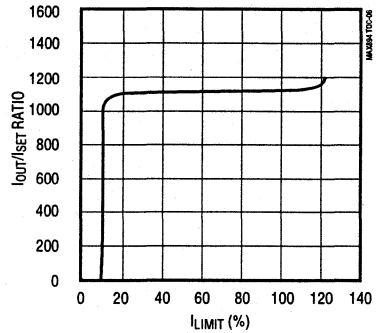
OFF-SWITCH CURRENT vs. TEMPERATURE



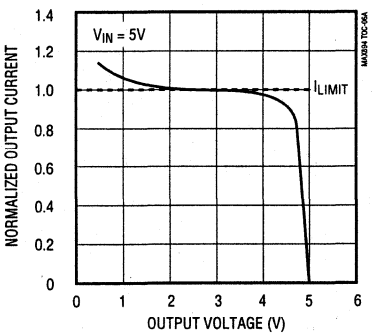
NORMALIZED ON-RESISTANCE vs. TEMPERATURE



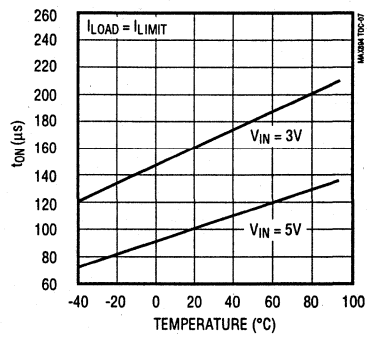
IOUT/ISET vs. ILIMIT



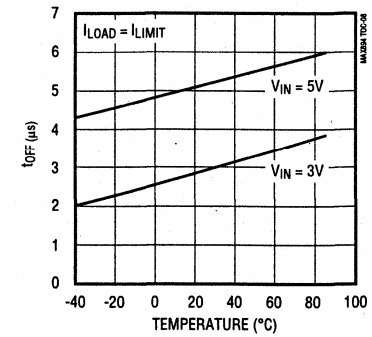
NORMALIZED OUTPUT CURRENT vs. OUTPUT VOLTAGE



TURN-ON TIME vs. TEMPERATURE



TURN-OFF TIME vs. TEMPERATURE

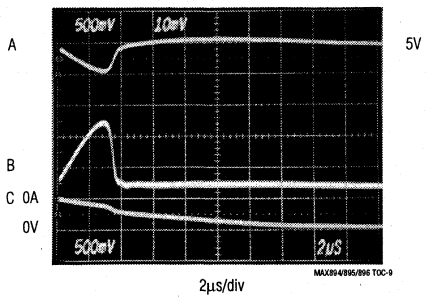


Dual, Current-Limited, High-Side P-Channel Switches with Thermal Shutdown

Typical Operating Characteristics (continued)

(Typical Operating Circuit, T_A = +25°C, unless otherwise noted.)

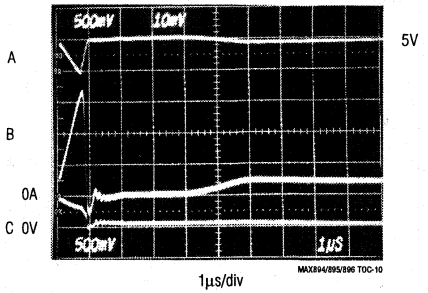
CURRENT-LIMIT RESPONSE (MAX894L, R_L = 1Ω)



2µs/div

C_{IN} = 47µF, C_{OUT} = 0.1µF
A: V_{IN}, 500mV/div, AC coupled
B: I_{OUT}, 2A/div
C: V_{OUT}, 5V/div

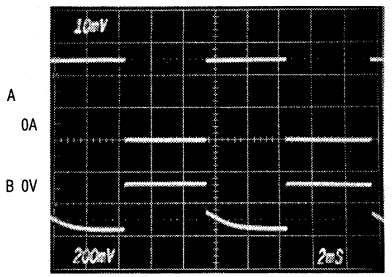
CURRENT-LIMIT RESPONSE (MAX894L, R_L = 0.7Ω)



1µs/div

C_{IN} = 47µF, C_{OUT} = 0.1µF
A: V_{IN}, 500mV/div, AC coupled
B: I_{OUT}, 2A/div
C: V_{OUT}, 5V/div

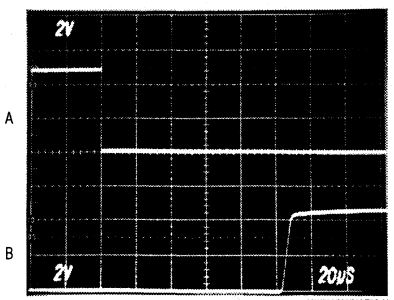
LOAD-TRANSIENT RESPONSE (MAX894L)



2ms/div

V_{IN} = 5V
A: I_{OUT} = 0 to 500mA, 0.2A/div
B: V_{OUT} RIPPLE, 200mV/div, AC COUPLED

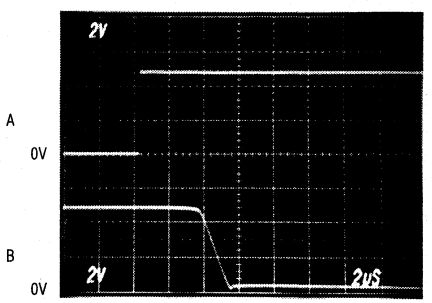
SWITCH TURN-ON TIME



20µs/div

V_{IN} = 5V, I_{OUT} = I_{LIMIT}
A: V_{ON}, 2V/div
B: V_{OUT}, 2V/div

SWITCH TURN-OFF TIME



2µs/div

V_{IN} = 5V, I_{OUT} = I_{LIMIT}
A: V_{ON}, 2V/div
B: V_{OUT}, 2V/div

Dual, Current-Limited, High-Side P-Channel Switches with Thermal Shutdown

Pin Description

PIN	NAME	FUNCTION
1	OUT A	Switch A Output. P-channel MOSFET drain. Bypass OUT A with a 0.1µF capacitor to ground.
2	OUT B	Switch B Output. P-channel MOSFET drain. Bypass OUT B with a 0.1µF capacitor to ground.
3	SET A	Set Current-Limit Input. A resistor from SET A to ground sets the current limit for switch A. See *Setting the Current Limit* section.
4	$\overline{ONA}$	Active-Low Switch A On Input. A logic low turns switch A on.
5	GND	Ground
6	SET B	Set Current-Limit Input. A resistor from SET B to ground sets the current limit for switch B. See *Setting the Current Limit* section.
7	IN	Input, Switches A and B. P-channel MOSFET source. Bypass IN with a 1µF capacitor to ground.
8	$\overline{ONB}$	Active-Low Switch B On Input. A logic low turns switch B on.

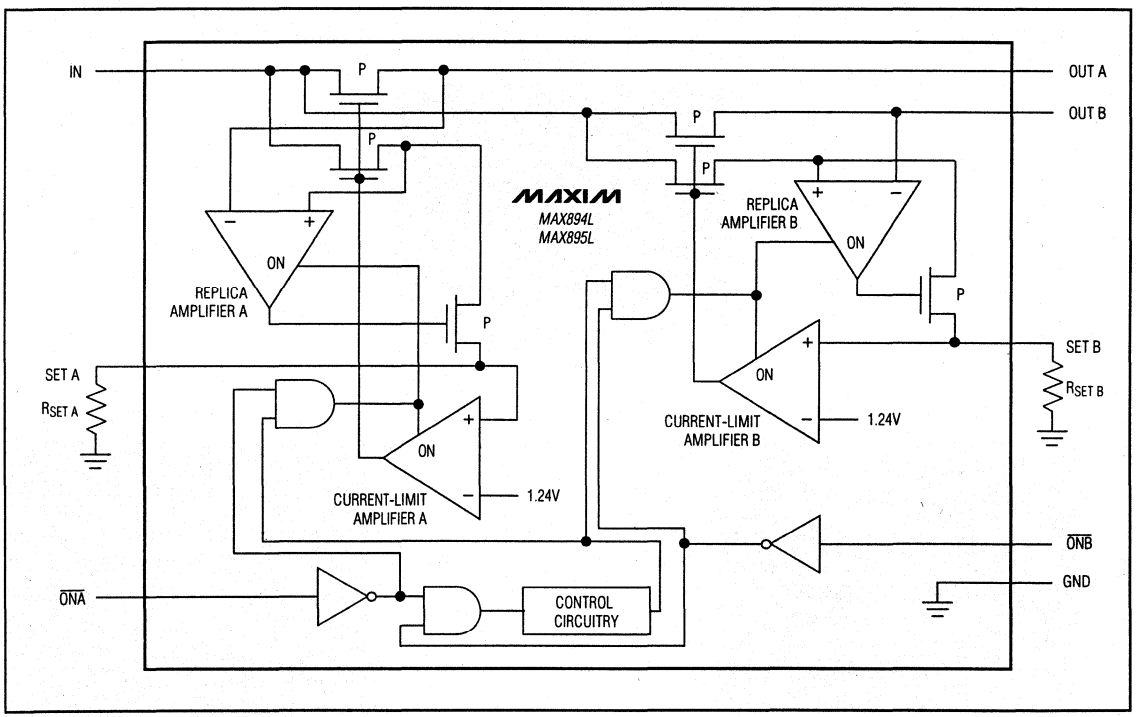


Figure 1. Functional Diagram

Dual, Current-Limited, High-Side P-Channel Switches with Thermal Shutdown

Detailed Description

The MAX894L/MAX895L P-channel MOSFET power switches limit output current to a user-programmed level. When the output current is increased beyond the set current level, the current also increases through the replica switch ($I_{OUT}/1050$) (MAX895) and through R_{SET} (Figure 1). The current-limit error amplifier compares the voltage across R_{SET} to the internal 1.24V reference, and regulates the current back to the lesser of the programmed current limit (I_{LIMIT}) or the maximum current limit (I_{MAX}).

These switches are not bidirectional; therefore, the input voltage must be higher than the output voltage.

Setting the Current Limit

The MAX894L/MAX895L feature internal current-limiting circuitry with maximum programmable values (I_{MAX}) of 500mA, and 250mA, respectively. For best performance, set the current limit (I_{LIMIT}) between $0.2I_{MAX} \le I_{LIMIT} \le I_{MAX}$. This current limit remains in effect throughout the input supply-voltage range.

Program the current limit with a resistor ($R_{SET_}$) connected from SET_ to ground (Figure 2) as follows:

$$I_{SET} = I_{LIMIT} / I_{RATIO}$$
$$R_{SET} = 1.24V / I_{SET} = (1.24V \times I_{RATIO}) / I_{LIMIT}$$

where I_{LIMIT} is the desired current limit for either switch and I_{RATIO} is the I_{OUT} to I_{SET} current ratio (1085 for the MAX894L and 1050 for the MAX895L.

Short-Circuit Protection

The MAX894L/MAX895L are short-circuit-protected switches. In the event of an output short circuit or current-overload condition, the current through either switch is limited by the internal current-limiting error amplifier to $1.5 \times I_{LIMIT}$. When the fault condition is removed, the replica error amplifier sets the current limit back to I_{LIMIT}.

For a high $\Delta V_{DS}/\Delta t$ during an output short-circuit condition, the switch turns off and disconnects the input supply from the output. The current-limiting amplifier then slowly turns the switch on with the output current limited to $1.5 \times I_{SET}$. When the fault condition is removed, the current limit is set back to I_{LIMIT}. Refer to Current-Limit Response graphs in the *Typical Operating Characteristics*.

Thermal Shutdown

The MAX894L/MAX895L feature thermal shutdown. The switch turns off when the junction temperature exceeds +135°C. Once the device cools by 10°C, the switch turns back on. If the fault short-circuit condition is not removed, the switch cycles on and off, resulting in a pulsed output.

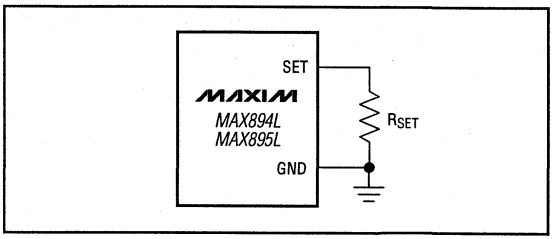


Figure 2. Setting the Current Limit

Applications Information

Input Capacitor

To limit input voltage drop during momentary output short-circuit conditions, place a capacitor from IN to GND. A 1µF ceramic capacitor is adequate for most applications; however, higher capacitor values further reduce voltage drop at the input.

Output Capacitor

Connect a 0.1µF capacitor from OUT to GND. This capacitor prevents inductive parasitics from pulling OUT negative during turn-off.

Layout and Thermal-Dissipation Consideration

To take full advantage of the switch-response time to output short-circuit conditions, it is very important to keep all traces as short as possible, reducing the effect of undesirable parasitic inductance. Place input and output capacitors as close as possible to the device (no more than 5mm).

Under normal operating conditions, the package can dissipate and channel heat away. Calculate the maximum power as follows:

$$P = I^2_{LIMITA} \times R_{\overline{ONA}} + I^2_{LIMITB} \times R_{\overline{ONB}}$$

where $R_{\overline{ONA}}$ and $R_{\overline{ONB}}$ are the on-resistances of switches A and B, respectively.

When one or both outputs are short circuited, the voltage drop across the switch equals the input supply. Hence, the power dissipated across the switch increases, as does the die temperature. If the fault condition is not removed, the thermal-overload-protection circuitry turns the switch off until the die temperature falls by 10°C. A ground plane in contact with the device helps to further dissipate heat.

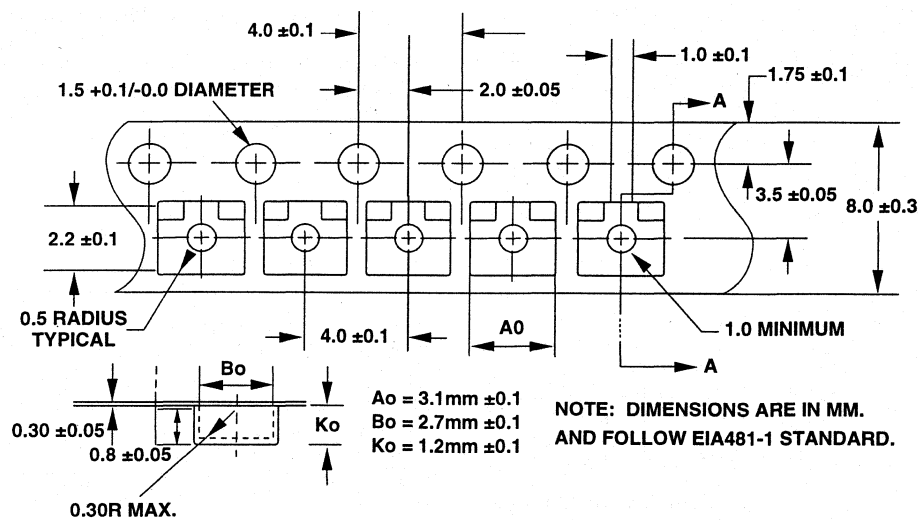
Dual, Current-Limited, High-Side P-Channel Switches with Thermal Shutdown

Chip Information

TRANSISTOR COUNT: 453

SUBSTRATE CONNECTED TO GND.

Tape-and-Reel Information



19-4752; Rev 0; 6/96

MAXIM

Dual-Channel CardBus and PCMCIA VCC/VPP Power-Switching Networks

General Description

The MAX1600/MAX1603 DC power-switching ICs contain a network of low-resistance MOSFET switches that deliver selectable VCC and VPP voltages to two CardBus or PC Card host sockets. Key features include ultra-low-resistance switches, small packaging, soft-switching action, and compliance with PCMCIA specifications for 3V/5V switching. 3.3V-only power switching for fast, 32-bit CardBus applications is supported in two ways: stiff, low-resistance 3.3V switches allow high 3.3V load currents (up to 1A); and completely independent internal charge pumps let the 3.3V switch operate normally, even if the +5V and +12V supplies are disconnected or turned off to conserve power. The internal charge pumps are regulating types that draw reduced input current when the VCC switches are static. Also, power consumption is automatically reduced to 10µA max when the control logic inputs are programmed to high-Z or GND states, unlike other solutions that may require a separate shutdown-control input.

Other key features include guaranteed specifications for output current limit level, and guaranteed specifications for output rise/fall times (in compliance with PCMCIA specifications). Reliability is enhanced by thermal-overload protection, accurate current limiting, an overcurrent-fault flag output, and undervoltage lockout. The CMOS/TTL-logic interface is flexible, and can tolerate logic input levels in excess of the positive supply rail.

The MAX1600 and MAX1603 are identical, except for the MAX1603's VY switch on-resistance (typically 140mΩ). The MAX1600/MAX1603 fit two complete CardBus/ PCMCIA switches into a space-saving, narrow (0.2in. or 5mm wide) SSOP package.

Applications

Desktop Computers	Data Loggers
Notebook Computers	Docking Stations
Handy-Terminals	PCMCIA Read/Write Drives

Ordering Information

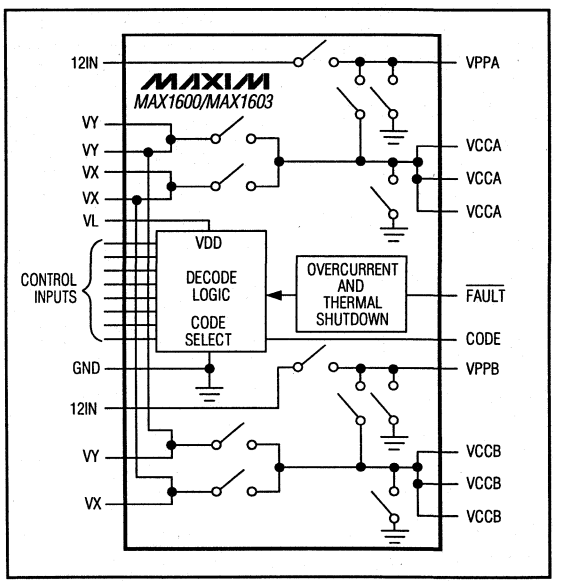
PART	TEMP. RANGE	PIN-PACKAGE
MAX1600EAI	-40°C to +85°C	28 SSOP
MAX1603EAI	-40°C to +85°C	28 SSOP

Pin Configuration appears on last page.

Features

- ♦ **Supports Two PC Card/CardBus Sockets**
- ♦ **1A, 0.08Ω Max 3.3V VCC Switch (MAX1600 only)**
  1A, 0.14Ω Max 5V VCC Switch
- ♦ **Soft Switching for Low Inrush Surge Current**
- ♦ **Overcurrent Protection**
- ♦ **Overcurrent/Thermal-Fault Flag Output**
- ♦ **Thermal Shutdown at T_j = +150°C**
- ♦ **Independent Internal Charge Pumps**
- ♦ **Break-Before-Make Switching Action**
- ♦ **10µA Max Standby Supply Current**
- ♦ **5V and 12V Not Required for Low-$R_{DS(ON)}$ 3.3V Switching**
- ♦ **Complies with PCMCIA 3V/5V Switching Specifications**
- ♦ **Super-Small 28-Pin SSOP Package (0.2in. or 5mm wide)**
- ♦ **Code Compatible with:**
  Cirrus CL-PD67XX Family
  Databook DB86184
  Intel 82365SL (industry-standard coding)

Simplified Block Diagram



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Dual-Channel CardBus and PCMCIA VCC/VPP Power-Switching Networks

ABSOLUTE MAXIMUM RATINGS

Inputs/Outputs to GND
(VL, VX, VY, VCCA, VCCB) (Note 1).....-0.3V, +6V
VPP Inputs/Outputs to GND
(12INA, 12INB, VPPA, VPPB) (Note 1).....-0.3V, +15V
Logic Inputs to GND (A0VCC, A1VCC, B0VCC, B1VCC,
A0VPP, A1VPP, B0VPP, B1VPP) (Note 1).....-0.3V, +6V
CODE Input to GND.....-0.3V, (VL + 0.3V)
VCCA, VCCB Output Current (Note 2).....4A
VPPA, VPPB Output Current (Note 2).....250mA

VCCA, VCCB Short Circuit to GND.....Continuous
VPPA, VPPB Short Circuit to GND.....Continuous
Continuous Power Dissipation (T_A = +70°C)
SSOP (derate 9.52mW/°C above +70°C).....762mW
Operating Temperature Range
MAX160_EAI/MAX1603EAI.....-40°C to +85°C
Storage Temperature Range.....-65°C to +160°C
Lead Temperature (soldering, 10sec).....+300°C

Note 1: There are no parasitic diodes between any of these pins, so there are no power-up sequencing restrictions (for example, logic input signals can be applied even if all of the supply voltage inputs are grounded).
Note 2: VCC and VPP outputs are internally current limited. See the *Electrical Characteristics*.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(VL = VY = 3.3V, VX = 5V, 12INA = 12INB = 12V, T_A = 0°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
POWER-SUPPLY SECTION						
Input Voltage Range	VX, VY or VL		3.0		5.5	V
	12INA, 12INB		11		13	
Undervoltage Lockout Threshold	VL falling edge		2.4	2.5	2.8	V
	12IN falling edge		1.8	3.0		
	12IN rising edge		5.0	8.0	10.0	
	VX, VY falling edge		1.4	2.5	2.8	
Standby Supply Current	VX or VY, all switches 0V or high-Z, control inputs = 0V or VL, T_A = +25°C				1	µA
VY Quiescent Supply Current	Any combination of VY switches on, control inputs = 0V or VL, no VCC loads			20	100	µA
VX Quiescent Supply Current	Any combination of VX switches on, control inputs = 0V or high-Z, no VCC loads			20	100	µA
12IN_ Standby Supply Current	12INA tied to 12INB, all switches 0V or high-Z, control inputs = 0V or VL, T_A = +25°C				1	µA
12IN_ Quiescent Supply Current	12INA tied to 12INB, VPPA and VPPB 12V switches on, control inputs = 0V or VL, no VPP loads			15	100	µA
VL Standby Supply Current	All switches 0V or high-Z, control inputs = 0V or VL, T_A = +25°C			4	10	µA
VL Quiescent Supply Current	Any combination of switches on			25	150	µA
VL Fall Rate	When using VL as shutdown pin (Note 3)				0.05	V/µs
VCC SWITCHES						
Operating Output Current Range	VCCA or VCCB, VX = VY = 3V to 5.5V		0		1	A
On-Resistance, VY Switches	12INA = 12INB = 0V to 13V, VY = 3V, VX = 0V to 5.5V, I_{SWITCH} = 1A, T_A = +25°C	MAX1600		0.06	0.08	Ω
		MAX1603		0.14	0.24	
On-Resistance, VX Switches	12INA = 12INB = 0V to 13V, VX = 4.5V, VY = 0V to 5.5V, I_{SWITCH} = 1A, T_A = +25°C			0.10	0.14	Ω
Output Current Limit	VCCA or VCCB		1.2		4	A

ELECTRICAL CHARACTERISTICS (continued)

(VL = VY = 3.3V, VX = 5V, 12INA = 12INB = 12V, T_A = 0°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Sink Current	VCCA or VCCB < 0.4V, programmed to 0V state	20			mA
Output Leakage Current	VCCA or VCCB forced to 0V, high-Z state, T_A = +25°C			10	µA
Output Propagation Delay Plus Rise Time	VCCA or VCCB, 0V to VX or VY, C_L = 30µF, R_L = 25Ω, 50% of input to 90% of output, T_A = +25°C		2	10	ms
Output Rise Time	VCCA or VCCB, 0V to VX or VY, C_L = 1µF, R_L = open circuit, 10% to 90% points, T_A = +25°C	100	1200		µs
Output Propagation Delay Plus Fall Time	VCCA or VCCB, VX or VY to 0V, C_L = 30µF, R_L = open circuit, 50% of input to 10% of output, T_A = +25°C		60	100	ms
Output Fall Time	VCCA or VCCB, VX or VY to 0V, C_L = 1µF, R_L = 25Ω, 90% to 10% points		6		ms
VPP SWITCHES					
Operating Output Current Range	VPPA or VPPB	0		120	mA
On-Resistance, 12V Switches	12IN = 11.6V, I_{SWITCH} = 100mA, T_A = +25°C		0.70	1	Ω
On-Resistance, VPP = VCC Switches	Programmed to VX (5V) or VY (3.3V), T_A = +25°C		1	3	Ω
Output Current Limit	VPPA or VPPB, programmed to 12V	130	200	260	mA
Output Sink Current	VPPA or VPPB < 0.4V, programmed to 0V state	10			mA
Output Leakage Current	VPPA or VPPB forced to 0V, high-Z state, T_A = +25°C			10	µA
Output Propagation Delay Plus Rise Time	VPPA or VPPB, 0V to 12IN_, C_L = 0.1µF, 50% of input to 90% of output, T_A = +25°C		1.2	30	ms
Output Rise Time	VPPA or VPPB, 0V to 12IN_, C_L = 0.1µF, 10% to 90% points, T_A = +25°C	100	800		µs
Output Propagation Delay Plus Fall Time	VPPA or VPPB, 12IN_ to 0V, C_L = 0.1µF, 50% of input to 10% of output, T_A = +25°C		9	60	ms
Output Fall Time	VPPA or VPPB, 12IN_ to 0V, C_L = 0.1µF, 90% to 10% points		1		ms
INTERFACE AND LOGIC SECTION					
$\overline{FAULT}$ Signal Propagation Delay	VCC_ or VPP_, load step to $\overline{FAULT}$ output, 50% point to 50% point (Note 3)		1		µs
$\overline{FAULT}$ Output Low Voltage	I_{SINK} = 1mA, low state			0.4	V
$\overline{FAULT}$ Output Leakage Current	$V_{\overline{FAULT}}$ = 5.5V, high state	-0.5		0.5	µA
Thermal Shutdown Threshold	Hysteresis = 20°C (Note 4)		150		°C
Logic Input Low Voltage	_VCC, _VPP			0.6	V
Logic Input High Voltage	_VCC, _VPP	1.5			V
Code Input Low Voltage	"Intel" code	0		0.4	V
Code Input High Voltage	"Cirrus" code	VL - 0.4		VL	V
Code Input Mid-Level Voltage	"Databook" code	1.2		VL - 1.2	V
Logic Input Bias Current	_VCC, _VPP, code	-1		1	µA

Dual-Channel CardBus and PCMCIA VCC/VPP Power-Switching Networks

ELECTRICAL CHARACTERISTICS

(VL = VY = 3.3V, VX = 5V, 12INA = 12INB = 12V, T_A = -40°C to +85°C, unless otherwise noted.)

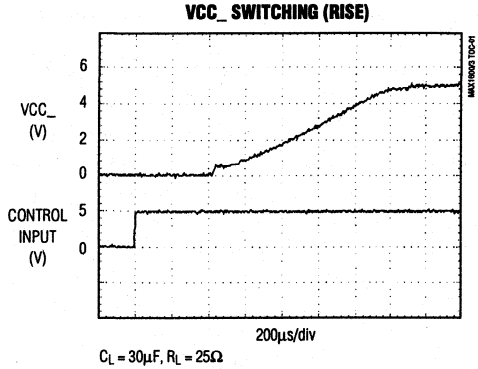
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
POWER-SUPPLY SECTION					
Input Voltage Range	VX, VY or VL	3.0		5.5	V
	12INA, 12INB	11		13	
Undervoltage Lockout Threshold	VL falling edge, hysteresis = 1%	2.3		2.9	V
	12IN falling edge	1.8			
	12IN rising edge	5		10	
	VX, VY falling edge	1.4		2.9	
Standby Supply Current	VX or VY, all switches 0V or high-Z, control inputs = 0V or VL, $T_A = T_{MIN}$ to T_{MAX}			15	µA
VY Quiescent Supply Current	Any combination of VY switches on, control inputs = 0V or VL, no VCC loads			100	µA
VX Quiescent Supply Current	Any combination of VX switches on, control inputs = 0V or high-Z, no VCC loads			100	µA
12IN_ Standby Supply Current	12INA tied to 12INB, all switches 0V or high-Z, control inputs = 0V or VL			15	µA
12IN_ Quiescent Supply Current	12INA tied to 12INB, VPPA and VPB 12V switches on, control inputs = 0V or VL, no VPP loads			100	µA
VL Standby Supply Current	All switches 0V or high-Z, control inputs = 0V or VL			15	µA
VL Quiescent Supply Current	Any combination of switches on			150	µA
$\overline{FAULT}$ Output Low Voltage	I_{SINK} = 1mA, low state			0.4	V
Logic Input Low Voltage	__VCC, __VPP			0.6	V
Logic Input High Voltage	__VCC, __VPP	1.6			V

Note 3: Not production tested.
Note 4: Thermal limit not active in standby state (all switches programmed to GND or high-Z state).

Typical Operating Characteristics

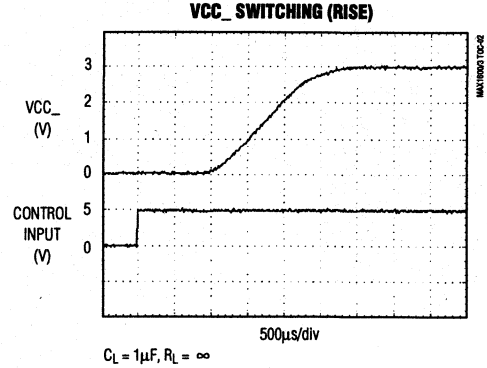
(VL = VY = 3.3V, VX = 5V = 12IN, T_A = +25°C, unless otherwise noted.)

VCC_ SWITCHING (RISE)



C_L = 30µF, R_L = 25Ω

VCC_ SWITCHING (RISE)

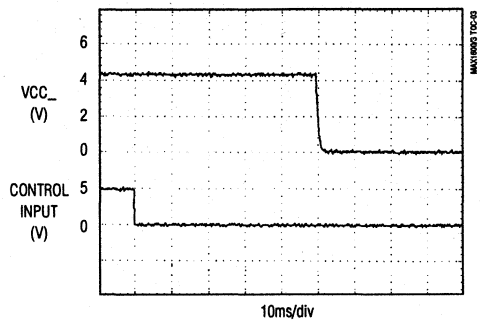


C_L = 1µF, R_L = ∞

Typical Operating Characteristics (continued)

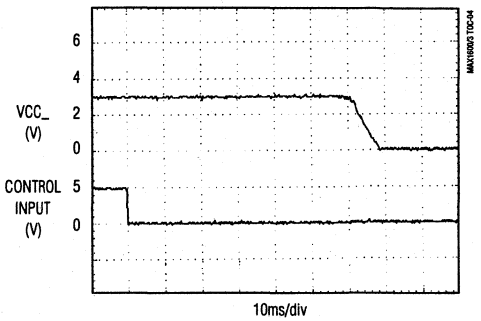
(VL = VY = 3.3V, VX = 5V = 12IN, T_A = +25°C, unless otherwise noted.)

VCC_ SWITCHING (FALL)



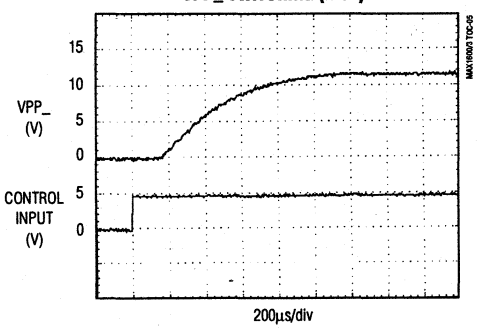
C_L = 33µF, R_L = ∞

VCC_ SWITCHING (FALL)



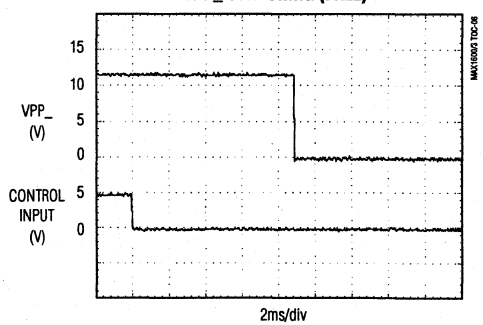
C_L = 1µF, R_L = 25Ω

VPP_ SWITCHING (RISE)



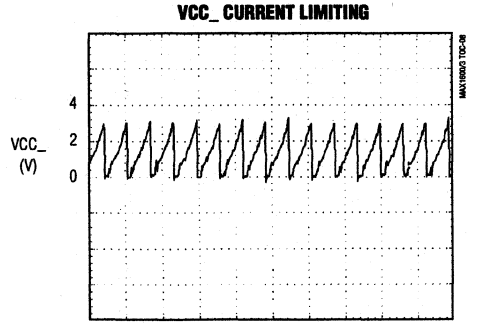
C_L = 0.1µF, R_L = ∞

VPP_ SWITCHING (FALL)



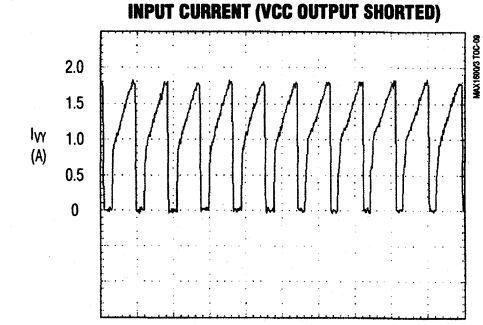
C_L = 0.1µF, R_L = ∞

VCC_ CURRENT LIMITING



C_L = 1µF, RESISTIVE OVERLOAD, R_L = 1Ω

INPUT CURRENT (VCC OUTPUT SHORTED)

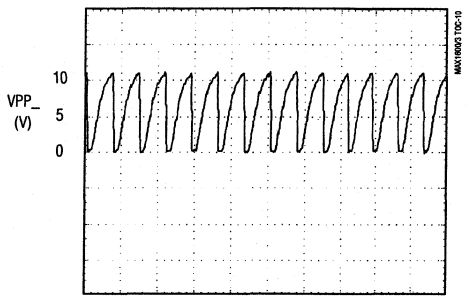


Dual-Channel CardBus and PCMCIA VCC/VPP Power-Switching Networks

Typical Operating Characteristics (continued)

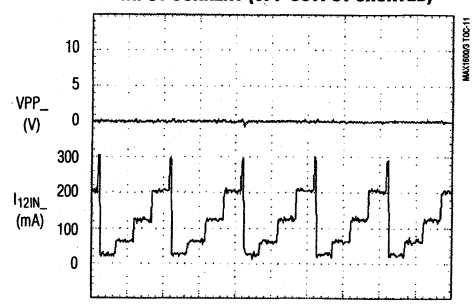
(VL = VY = 3.3V, VX = 5V = 12IN, T_A = +25°C, unless otherwise noted.)

VPP_ CURRENT LIMITING



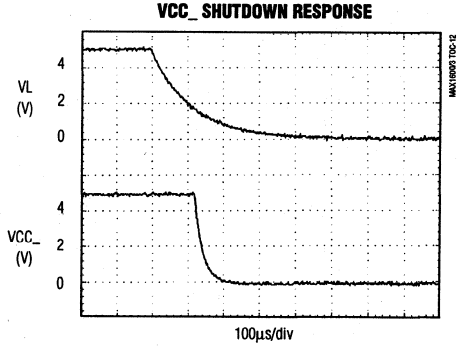
C_L = 1µF, R_L = 50Ω

INPUT CURRENT (VPP OUTPUT SHORTED)



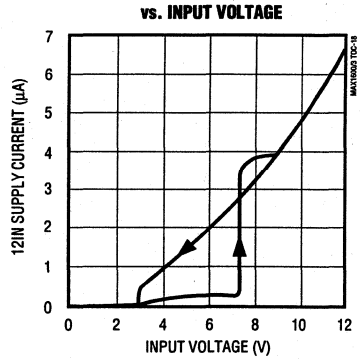
R_L = 0.1Ω

VCC_ SHUTDOWN RESPONSE

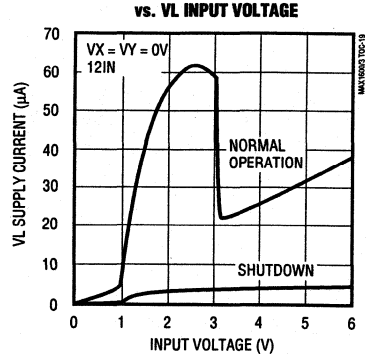


CIRCUIT OF FIGURE 2

12IN SUPPLY CURRENT vs. INPUT VOLTAGE



VL SUPPLY CURRENT vs. VL INPUT VOLTAGE

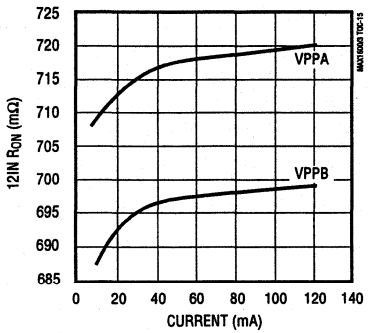


Dual-Channel CardBus and PCMCIA VCC/VPP Power-Switching Networks

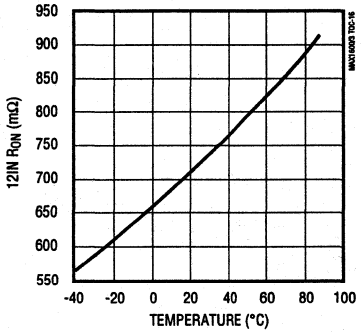
Typical Operating Characteristics (continued)

(VL = VY = 3.3V, VX = 5V = 12IN, T_A = +25°C, unless otherwise noted.)

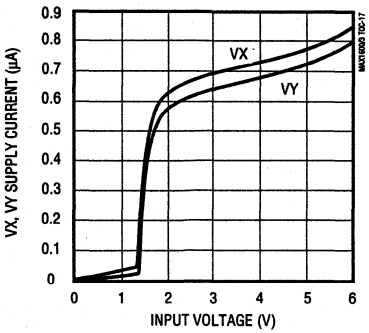
12IN_ ON-RESISTANCE vs. CURRENT



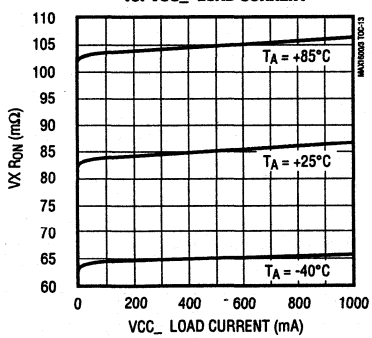
12IN_ ON-RESISTANCE vs. TEMPERATURE



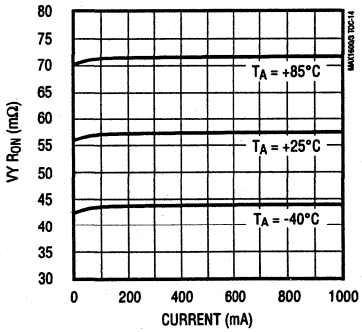
VX, VY SUPPLY CURRENT vs. INPUT VOLTAGE



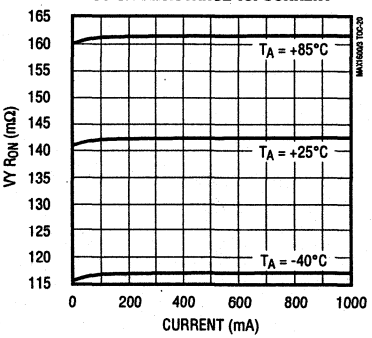
VX ON-RESISTANCE vs. VCC_ LOAD CURRENT



MAX1600 VY ON-RESISTANCE vs. CURRENT



MAX1603 VY ON-RESISTANCE vs. CURRENT



Pin Description

PIN	NAME	FUNCTION
1	GND	Ground
2	A1VPP	Channel A VPP Control Input. See *Logic Truth Tables.*
3	A0VPP	Channel A VPP Control Input. See *Logic Truth Tables.*
4	12INA	+12V Supply Voltage Input, internally connects to channel A VPP switch. Tie to VPPA if not used.
5	VPPA	Channel A VPP Output
6, 8, 10	VX	VX Supply Voltage Inputs. VX pins must be connected to one another. Input range is +3V to +5.5V. VX is normally connected to 5V.
7, 22, 24	VCCA	Channel A VCC Outputs
9, 18, 20	VCCB	Channel B VCC Outputs
11	VPPB	Channel B VPP Output
12	12INB	+12V Supply Voltage Input, internally connects to channel B VPP switch. Tie to VPPB if not used.

Dual-Channel CardBus and PCMCIA VCC/VPP Power-Switching Networks

Pin Description (continued)

PIN	NAME	FUNCTION
13	B0VPP	Channel B VPP Control Input. See *Logic Truth Tables.*
14	B1VPP	Channel B VPP Control Input. See *Logic Truth Tables.*
15	B0VCC	Channel B VCC Control Input. See *Logic Truth Tables.*
16	B1VCC	Channel B VCC Control Input. See *Logic Truth Tables.*
17	$\overline{\text{FAULT}}$	Fault-Detection Output. $\overline{\text{FAULT}}$ goes low during current limit, undervoltage lockout, or thermal limit. $\overline{\text{FAULT}}$ is an open-drain output that requires an external pull-up resistor.
19, 21, 23	VY	VY Supply Voltage Inputs. VY pins must be connected to one another. Input range is +3V to +5.5V. VY is normally connected to 3.3V.
25	CODE	Three-Level Code-Select Input. See *Logic Truth Tables.* Low = Standard "Intel" code High = "Cirrus" code Mid-supply = "Databook" code (Figure 6)
26	A1VCC	Channel A VCC Control Input. See *Logic Truth Tables.*
27	A0VCC	Channel A VCC Control Input. See *Logic Truth Tables.*
28	VL	Logic Supply-Voltage Input. Connect to the +3.3V or +5V host system supply. VL can be supplied via the output of a CMOS-logic gate to produce an overriding shutdown. When used as a shutdown input, VL should have a 1kΩ series resistor with a 0.1µF capacitor to ground (Figure 2). Note that VL must be greater than undervoltage lockout for any switches to be turned on.

Logic Truth Tables

Table 1. Standard "Intel" Code (82365SL), CODE = GND

_1VCC	_0VCC	_1VPP	_0VPP	VCC_	VPP_	MODE
0	0	0	0	GND	GND	STBY
0	0	0	1	GND	GND	STBY
0	0	1	0	GND	GND	STBY
0	0	1	1	GND	GND	STBY
0	1	0	0	VY	GND	ACTIVE
0	1	0	1	VY	VCC_	ACTIVE
0	1	1	0	VY	12IN	ACTIVE
0	1	1	1	VY	High-Z	ACTIVE
1	0	0	0	VX	GND	ACTIVE
1	0	0	1	VX	VCC_	ACTIVE
1	0	1	0	VX	12IN	ACTIVE
1	0	1	1	VX	High-Z	ACTIVE
1	1	0	0	VY	GND	ACTIVE
1	1	0	1	VY	VCC_	ACTIVE
1	1	1	0	VY	12IN	ACTIVE
1	1	1	1	VY	High-Z	ACTIVE

STBY = Standby Mode

Table 2. "Cirrus" Code, CODE = High (VL)

_1VCC	_0VCC	_1VPP	_0VPP	VCC_	VPP_	MODE
0	0	0	0	High-Z	High-Z	STBY
0	0	0	1	High-Z	High-Z	STBY
0	0	1	0	High-Z	High-Z	STBY
0	0	1	1	High-Z	High-Z	STBY
0	1	0	0	VX	GND	ACTIVE
0	1	0	1	VX	VCC_	ACTIVE
0	1	1	0	VX	12IN	ACTIVE
0	1	1	1	VX	High-Z	ACTIVE
1	0	0	0	VY	GND	ACTIVE
1	0	0	1	VY	VCC_	ACTIVE
1	0	1	0	VY	12IN	ACTIVE
1	0	1	1	VY	High-Z	ACTIVE
1	1	0	0	GND	GND	STBY
1	1	0	1	GND	GND	STBY
1	1	1	0	GND	GND	STBY
1	1	1	1	GND	GND	STBY

STBY = Standby Mode

Logic Truth Tables (cont.)

Table 3. "Databook" Code, CODE = Mid-Supply (VL/2)

_1VCC	_0VCC	_1VPP	_0VPP	VCC_	VPP_	MODE
0	0	0	X	GND	High-Z	STBY
0	0	1	X	VY	12IN	ACTIVE
0	1	0	X	GND	GND	STBY
0	1	1	X	VX	12IN	ACTIVE
1	0	0	X	VY	VCC_	ACTIVE
1	0	1	X	VY	GND	ACTIVE
1	1	0	X	VX	VCC_	ACTIVE
1	1	1	X	VX	GND	ACTIVE

STBY = Standby Mode *X = Don't Care*

Detailed Description

The MAX1600/MAX1603 power-switching ICs contain a network of low-resistance MOSFET switches that deliver selectable VCC and VPP voltages to two CardBus or PC Card host sockets. The MAX1600/MAX1603 differ only in the VY switch on-resistance. Figure 1 is the detailed block diagram.

The power-input pins (VY, VX, 12IN_) are completely independent. Low inrush current is guaranteed by controlled switch rise times. VCC's 100µs minimum output rise time is 100% tested with a 1µF capacitive load, and VPP's 1ms minimum rise time is guaranteed with a 0.1µF load. These respective capacitive loads are chosen as worst-case card-insertion parameters. The internal switching control allows VCC and VPP rise times to be

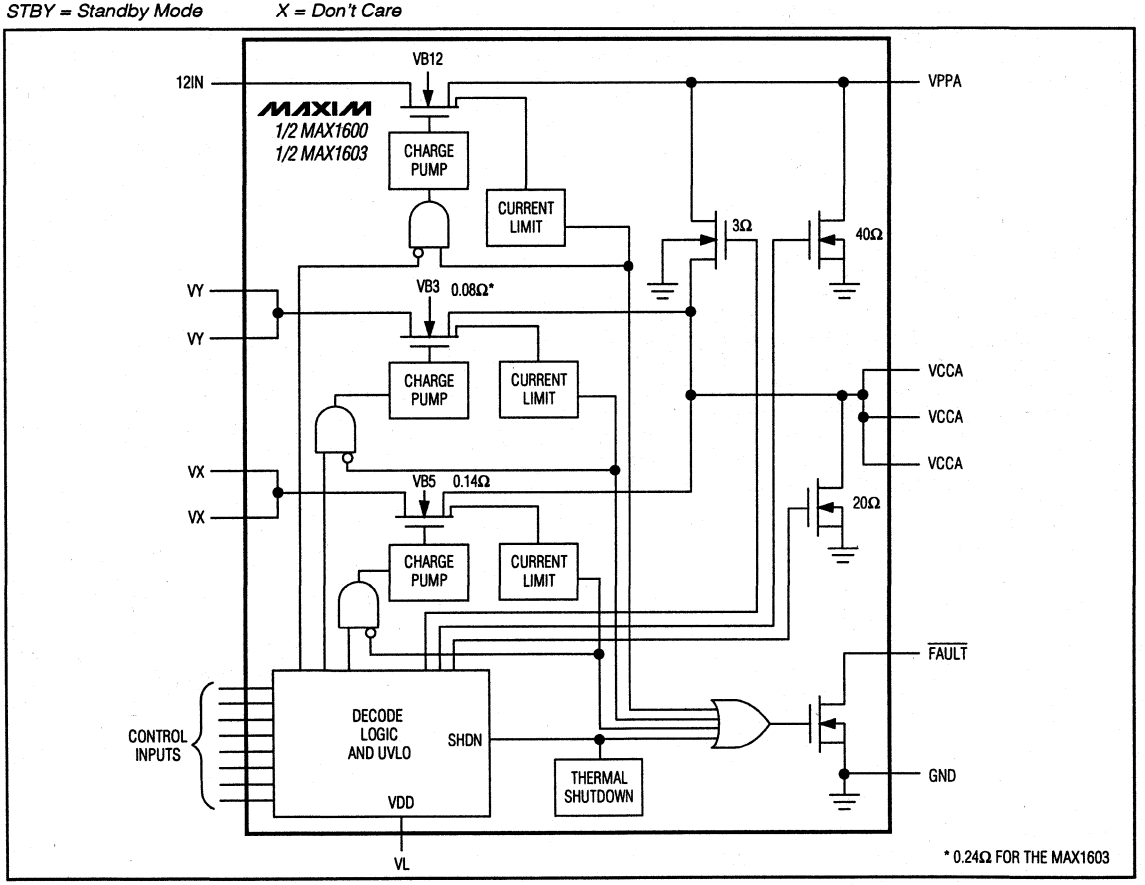


Figure 1. Detailed Block Diagram (one channel of two)

Dual-Channel CardBus and PCMCIA VCC/VPP Power-Switching Networks

controlled, and makes them nearly independent of resistive and capacitive loads (see rise-time photos in the *Typical Operating Characteristics*). Fall times are a function of loading, and are compensated by internal circuitry.

Power savings is automatic: internal charge pumps draw very low current when the VCC switches are static. Standby mode reduces switch supply current to 1µA. Driving the VL pin low with an external logic gate (master shutdown) reduces total supply current to1µA (Figure 2).

Operating Modes

The MAX1600/MAX1603 are compatible with the Cirrus CL-PD67XX, Databook DB86184, and Intel 82365SL PC Card Interface Controllers (PCIC). Eight control inputs select the internal switches' positions and the operating modes according to the input code. Select the proper code format for the chosen controller with the CODE input pin (see *Pin Description* and Tables 1, 2, and 3). CODE reconfigures the logic decoder to one of three interface controllers:

Low = Standard "Intel" code (Figure 5)

High = "Cirrus" code (Figure 4)

Midsupply = "Databook" code (Figure 6)

An additional 1µA (3µA max) of VL supply current will flow if CODE = midsupply (VL / 2).

The MAX1600/MAX1603 have three operating modes: normal, standby, and shutdown. Normal mode supplies the selected outputs with their appropriate supply voltages. Standby mode places all switches at ground, high impedance, or a combination of the two. Shutdown mode turns all switches off, and puts the VCC and VPP outputs into a high-impedance state. Pull VL low to enter shutdown mode. To ensure a 0.05V/µs fall rate on VL, use a 1kΩ series resistor and a 0.1µF capacitor to ground (Figure 2).

Overcurrent Protection

Peak detecting circuitry protects both the VCC and VPP switches against overcurrent conditions. When current through any switch exceeds the internal current limit (4A for VCC switches and 200mA for VPP switches) the switch turns off briefly, then turns on again at the controlled rise rate. If the overcurrent condition lasts more than 2µs, the $\overline{\text{FAULT}}$ output goes low. $\overline{\text{FAULT}}$ is not latched. A continuous short-circuit condition results in a pulsed output current and a pulsed $\overline{\text{FAULT}}$ output until thermal shutdown is reached. $\overline{\text{FAULT}}$ is open-drain and requires an external pull-up resistor.

Thermal Shutdown

If the IC junction temperature rises above +150°C, the thermal shutdown circuitry opens all switches, including the GND switches, and $\overline{\text{FAULT}}$ is pulled low. When the temperature falls below +130°C, the switches turn on again at the controlled rise rate. If the overcurrent condition remains, the part cycles between thermal shutdown and overcurrent.

Undervoltage Lockout

If the VX or VY switch input voltage drops below 1.5V, the associated switch turns off and $\overline{\text{FAULT}}$ goes low. For example, if VY is 3.3V and VX is 0V, and if the interface controller selects VY, the VCCA output will be 3.3V. If VX is selected, VCCA changes to a high-impedance output and $\overline{\text{FAULT}}$ goes low.

When a voltage is initially applied to 12IN_, it must be greater than 8V to allow the switch to operate. Operation continues until the voltage falls below 2V (the VPP output is high impedance).

When VL drops to less than 2.3V, all switches are turned off and the VCC and VPP outputs are high impedance.

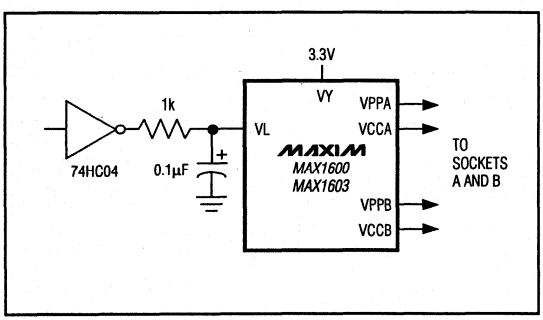


Figure 2. Master Shutdown Circuit

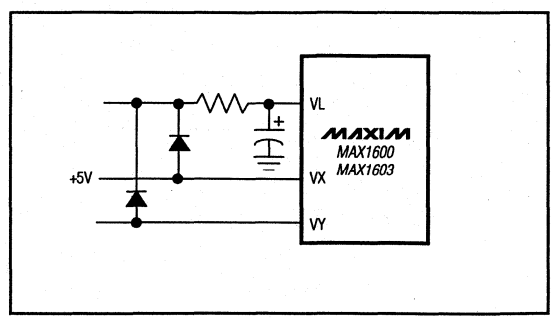


Figure 3. Applying Power to the VL Input

Dual-Channel CardBus and PCMCIA VCC/VPP Power-Switching Networks

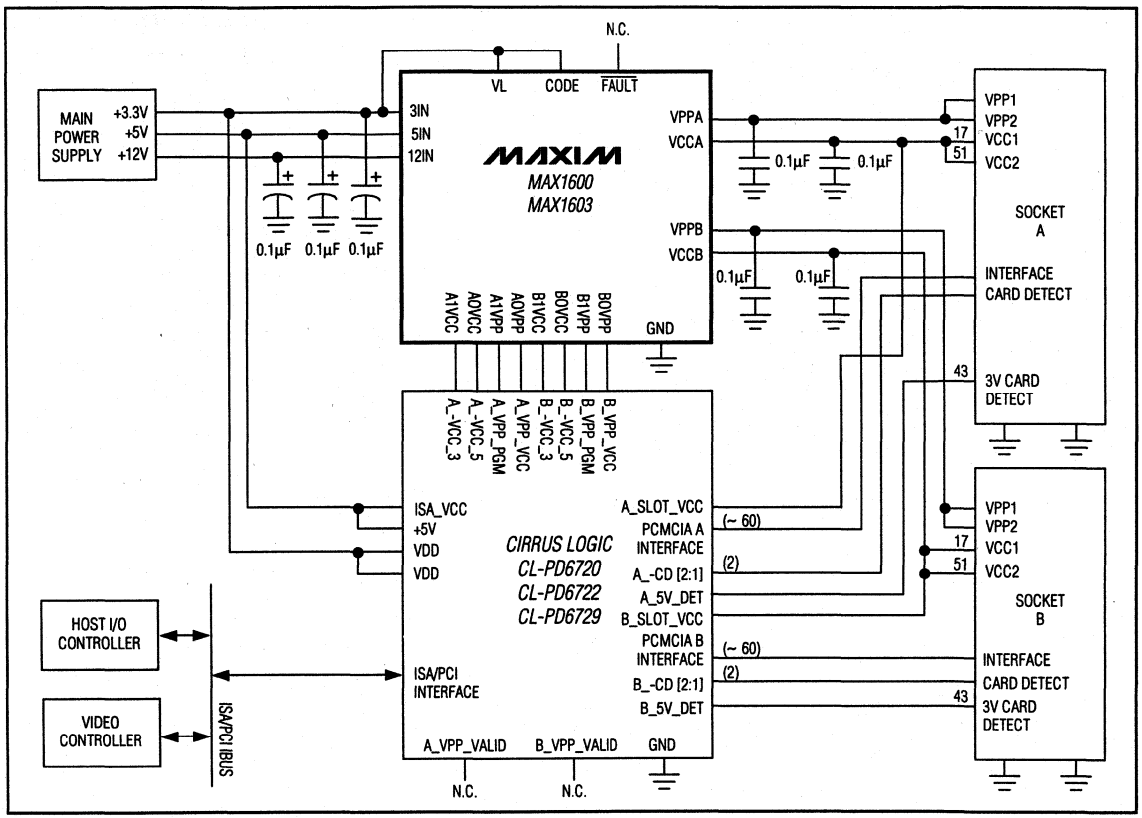


Figure 4. Application with Cirrus Logic Interface

Applications Information

Supply Bypassing

Bypass the VY, VX, and 12IN_ inputs with ceramic 0.1µF capacitors. Bypass the VCC_ and VPP_ outputs with a 0.1µF capacitor for noise reduction and ESD protection.

Power-Up

Apply power to the VL input before any of the switch inputs. If VX, VY, or 12IN receive power before VL rises above 2.8V, the supply current may be artificially high (about 5mA). When the voltage on VL is greater than 2.8V, the part consumes its specified 24µA. To avoid power sequencing, diode-OR VX and VY to VL through a 1kΩ resistor (Figure 3). Take care not to allow VL to drop below the 2.8V maximum undervoltage lockout threshold.

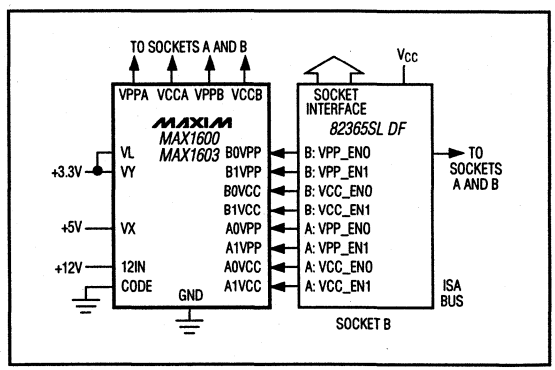


Figure 5. Application with Intel Interface

Dual-Channel CardBus and PCMCIA VCC/VPP Power-Switching Networks

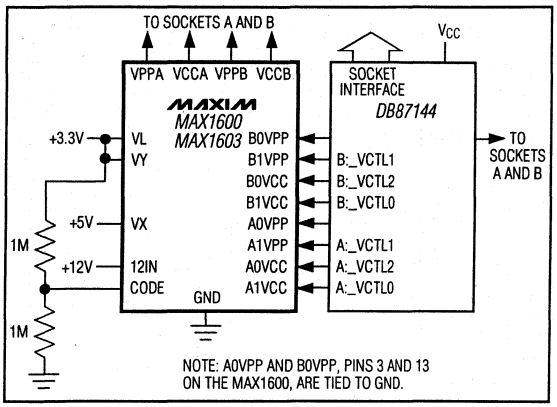
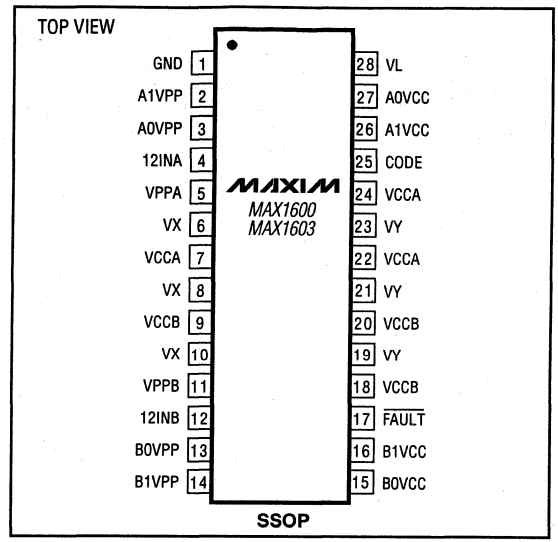


Figure 6. Block Diagram of the Databook DB87144 PCI to CardBus Controller Interface to the MAX1600.

Chip Information

TRANSISTOR COUNT: 4372

Pin Configuration



19-1085; Rev 1: 10/96

MAXIM

Dual-Channel CardBus and PCMCIA Power Switches with SMBus™ Serial Interface

General Description

The MAX1601/MAX1604 DC power-switching ICs contain a network of low-resistance MOSFET switches that deliver selectable VCC and VPP voltages to two CardBus or PC Card host sockets. Key features include ultra-low-resistance switches, small packaging, soft-switching action, and compliance with PCMCIA specifications for 3V/5V switching. 3.3V-only power switching for fast, 32-bit CardBus applications is supported in two ways: stiff, low-resistance 3.3V switches allow high 3.3V load currents (up to 1A); and completely independent internal charge pumps let the 3.3V switch operate normally, even if the +5V and +12V supplies are disconnected or turned off to conserve power. The internal charge pumps are regulating types that draw reduced input current when the VCC switches are static. Also, power consumption is automatically reduced to 10µA max when the switches are programmed to high-Z or GND states over the serial interface, unlike other solutions that may require a separate shutdown-control input.

Other key features include guaranteed specifications for output current limit level, and guaranteed specifications for output rise/fall times (in compliance with PCMCIA specifications). Reliability is enhanced by thermal-overload protection, accurate current limiting, an overcurrent-fault flag output, undervoltage lockout, and extra ESD protection at the VCC/VPP outputs. The SMBus serial interface is flexible, and can tolerate logic input levels in excess of the positive supply rail.

The MAX1604 and MAX1601 are identical, except for the MAX1604's VY switch, which has roughly three-times the on-resistance (typically 140mΩ).The MAX1601/MAX1604 fit two complete CardBus/PCMCIA switches into a space-saving, narrow (0.2in. or 5mm wide) SSOP package.

Applications

Desktop Computers	Data Loggers
Notebook Computers	Digital Cameras
Docking Stations	Printers
Handy-Terminals	PCMCIA Read/Write Drives

Pin Configuration appears on last page.

SMBus is a trademark of Intel Corp.

Features

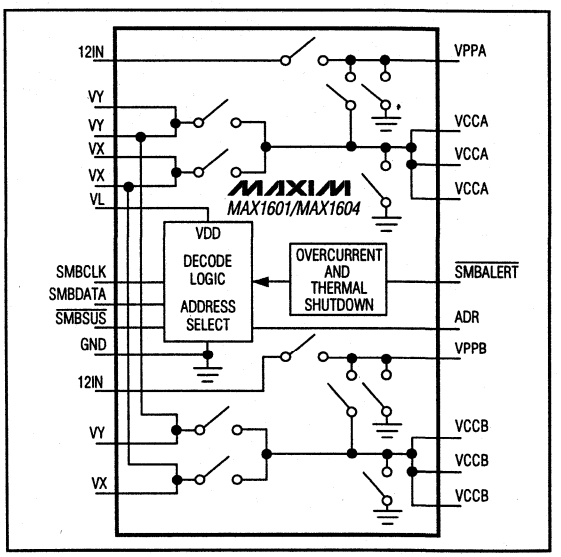
- ♦ **Supports Two CardBus Sockets**
- ♦ **1A, 0.08Ω Max VY VCC Switch (MAX1601 only)**
  1A, 0.14Ω Max VX VCC Switch
- ♦ **Soft Switching for Low Inrush Surge Current**
- ♦ **Overcurrent Protection**
- ♦ **Overcurrent/Thermal-Fault Flag Output**
- ♦ **Thermal Shutdown at T_J = +150°C**
- ♦ **Independent Internal Charge Pumps**
- ♦ **Break-Before-Make Switching Action**
- ♦ **10µA Max Standby Supply Current**
- ♦ **5V and 12V Not Required for Low-$R_{DS(ON)}$ 3.3V Switching**
- ♦ **Complies with PCMCIA 3V/5V Switching Specifications**
- ♦ **Super-Small, 28-Pin SSOP Package (0.2in. or 5mm wide)**
- ♦ **System Management Bus (SMBus) Serial Interface**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1601EAI	-40°C to +85°C	28 SSOP
MAX1604EAI	-40°C to +85°C	28 SSOP

4

Simplified Block Diagram



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Dual-Channel CardBus and PCMCIA Power Switches with SMBus™ Serial Interface

ABSOLUTE MAXIMUM RATINGS

Inputs/Outputs to GND
(VL, VX, VY, VCCA, VCCB) (Note 1).....-0.3V, +6V
VPP Inputs/Outputs to GND
(12INA, 12INB, VPPA, VPPB) (Note 1).....-0.3V, +15V
Inputs and Outputs to GND (SMBCLK, SMBDATA, SMBSUS, $\overline{\text{SMBALERT}}$) (Note 1).....-0.3V, +6V
ADR Input to GND.....-0.3V, (VL + 0.3V)
VCCA, VCCB Output Current (Note 2).....4A
VPPA, VPPB Output Current (Note 2).....250mA

VCCA, VCCB Short Circuit to GND.....Continuous
VPPA, VPPB Short Circuit to GND.....Continuous
Continuous Power Dissipation (T_A = +70°C)
SSOP (derate 9.52mW/°C above +70°C).....762mW
Operating Temperature Range
MAX1601EAI/MAX1604EAI.....-40°C to +85°C
Storage Temperature Range.....-65°C to +160°C
Lead Temperature (soldering, 10sec).....+300°C

Note 1: There are no parasitic diodes between any of these pins, so there are no power-up sequencing restrictions (for example, logic input signals can be applied even if all of the supply voltage inputs are grounded).
Note 2: VCC and VPP outputs are internally current-limited to safe values. See the *Electrical Characteristics* table.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(VL = VY = 3.3V, VX = 5V, 12INA = 12INB = 12V, T_A = 0°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
POWER-SUPPLY SECTION						
Input Voltage Range	VX, VY or VL		3.0		5.5	V
	12INA, 12INB		11		13	
Undervoltage Lockout Threshold	VL falling edge		2.4	2.5	2.8	V
	12IN falling edge		1.8	3.0		
	12IN rising edge		5	8	10	
	VX, VY falling edge		1.4	2.5	2.8	
Standby Supply Current	VX or VY, all switches 0V or high-Z, control inputs = 0V or VL, T_A = +25°C				1	µA
VY Quiescent Supply Current	Any combination of VY switches on, control inputs = 0V or VL, no VCC loads			20	100	µA
VX Quiescent Supply Current	Any combination of VX switches on, control inputs = 0V or high-Z, no VCC loads			20	100	µA
12IN_ Standby Supply Current	12INA tied to 12INB, all switches 0V or high-Z, control inputs = 0V or VL, T_A = +25°C				1	µA
12IN_ Quiescent Supply Current	12INA tied to 12INB, VPPA and VPPB 12V switches on, control inputs = 0V or VL, no VPP loads			15	100	µA
VL Standby Supply Current	All switches 0V or high-Z, control inputs = 0V or VL, T_A = +25°C			4	10	µA
VL Quiescent Supply Current	Any combination of switches on			25	150	µA
VL Fall Rate	When using VL as shutdown pin (Note 3)				0.05	V/µs
VCC SWITCHES						
Operating Output Current Range	VCCA or VCCB, VX = VY = 3V to 5.5V		0		1	A
On-Resistance, VY Switches	12INA = 12INB = 0V to 13V, VY = 3V, VX = 0V to 5.5V, I_{SWITCH} = 1A, T_A = +25°C	MAX1601		0.06	0.08	Ω
		MAX1604		0.14	0.24	
On-Resistance, VX Switches	12INA = 12INB = 0V to 13V, VX = 4.5V, VY = 0V to 5.5V, I_{SWITCH} = 1A, T_A = +25°C			0.10	0.14	Ω

ELECTRICAL CHARACTERISTICS (continued)

(VL = VY = 3.3V, VX = 5V, 12INA = 12INB = 12V, T_A = 0°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Current Limit	VCCA or VCCB	1.2		4.0	A
Output Sink Current	VCCA or VCCB < 0.4V, programmed to 0V state	20			mA
Output Leakage Current	VCCA or VCCB forced to 0V, high-Z state, T_A = +25°C			10	µA
Output Propagation Delay Plus Rise Time	VCCA or VCCB, 0V to VX or VY, C_L = 30µF, R_L = 25Ω, 50% of input to 90% of output, T_A = +25°C		2	10	ms
Output Rise Time	VCCA or VCCB, 0V to VX or VY, C_L = 1µF, R_L = open circuit, 10% to 90% points, T_A = +25°C	100	1200		µs
Output Propagation Delay Plus Fall Time	VCCA or VCCB, VX or VY to 0V, C_L = 30µF, R_L = open circuit, 50% of input to 10% of output, T_A = +25°C		60	100	ms
Output Fall Time	VCCA or VCCB, VX or VY to 0V, C_L = 1µF, R_L = 25Ω, 90% to 10% points		6		ms
VPP SWITCHES					
Operating Output Current Range	VPPA or VPPB	0		120	mA
On-Resistance, 12V Switches	12IN = 11.6V, I_{SWITCH} = 100mA, T_A = +25°C		0.70	1	Ω
On-Resistance, VPP = VCC Switches	Programmed to VX (5V) or VY (3.3V), T_A = +25°C		1	3	Ω
Output Current Limit	VPPA or VPPB, programmed to 12V	130	200	260	mA
Output Sink Current	VPPA or VPPB < 0.4V, programmed to 0V state	10			mA
Output Leakage Current	VPPA or VPPB forced to 0V, high-Z state, T_A = +25°C			10	µA
Output Propagation Delay Plus Rise Time	VPPA or VPPB, 0V to 12IN_, C_L = 0.1µF, 50% of input to 90% of output, T_A = +25°C		1.2	30	ms
Output Rise Time	VPPA or VPPB, 0V to 12IN_, C_L = 0.1µF, 10% to 90% points, T_A = +25°C	100	800		µs
Output Propagation Delay Plus Fall Time	VPPA or VPPB, 12IN_ to 0V, C_L = 0.1µF, 50% of input to 10% of output, T_A = +25°C		9	60	ms
Output Fall Time	VPPA or VPPB, 12IN_ to 0V, C_L = 0.1µF, 90% to 10% points		1		ms
INTERFACE AND LOGIC SECTION					
$\overline{\text{SMBALERT}}$ Signal Propagation Delay	VCC_ or VPP_, load step to $\overline{\text{SMBALERT}}$ output, 50% point to 50% point (Note 3)		3		µs
$\overline{\text{SMBALERT}}$ Output Low Voltage	I_{SINK} = 1mA, low state			0.4	V
$\overline{\text{SMBALERT}}$ Output Leakage Current	$V_{\overline{\text{SMBALERT}}}$ = 5.5V, high state	-0.1		0.1	µA
Thermal Shutdown Threshold	Hysteresis = +20°C (Note 4)		150		°C
Logic Input Low Voltage	$\overline{\text{SMBSUS}}$, SMBCLK, SMBDATA			0.8	V
Logic Input High Voltage	$\overline{\text{SMBSUS}}$, SMBCLK, SMBDATA	2.2			V
Logic Output Low Voltage	SMBDATA, I_{SINK} = 4mA			0.4	V

Dual-Channel CardBus and PCMCIA Power Switches with SMBus™ Serial Interface

ELECTRICAL CHARACTERISTICS (continued)

(VL = VY = 3.3V, VX = 5V, 12INA = 12INB = 12V, T_A = 0°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SMB Input Capacitance	$\overline{SMBSUS}$, SMBCLK, SMBDATA		5		pF
SMBCLK Clock Frequency	SMBus spec = 10kHz min	DC		100	kHz
SMBCLK Clock Low Time	t_{LOW} 10% to 10% points	4.7			µs
SMBCLK Clock High Time	t_{HIGH} 90% to 90% points	4			µs
SMB Repeated Start-Condition Setup Time	$t_{SU:STA}$ 90% to 90% points	250			ns
SMB Start-Condition Hold Time	$t_{HD:STA}$ 10% of SMBDATA to 90% of SMBCLK	4			µs
SMB Stop-Condition Setup Time	$t_{SU:STO}$ 90% of SMBCLK to 10% of SMBDATA	4			µs
SMB Data Valid to SMBCLK Rising-Edge Time	$t_{SU:DAT}$ 10% or 90% of SMBDATA to 10% of SMBCLK	500			ns
SMB Data Hold Time	$t_{HD:DAT}$ (Note 5)	0			ns
Bus Free Time	t_{BUF} between start and stop conditions	4.7			µs
ADR Input Low Voltage				0.6	V
ADR Input High Voltage		1.5			V
Logic Input Bias Current	ADR, $\overline{SMBSUS}$, SMBCLK, SMBDATA	-1		1	µA
SCL Fall to SDA Valid (Master Clocking-In Data)			100	1000	ns
Start-Condition Setup		4.7			µs

Note 3: Not production tested.

Note 4: Thermal limit not active in standby state (all switches programmed to GND or high-Z state).

Note 5: A transition must internally provide at least a hold time in order to bridge the undefined region (300ns max) of the falling edge of SMBCLK.

ELECTRICAL CHARACTERISTICS

(VL = VY = 3.3V, VX = 5V, 12INA = 12INB = 12V, T_A = -40°C to +85°C, unless otherwise noted.)

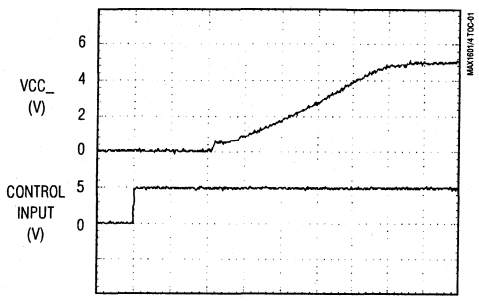
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
POWER-SUPPLY SECTION					
Input Voltage Range	VX, VY or VL	3.0		5.5	V
	12INA, 12INB	11		13	
Undervoltage Lockout Threshold	VL falling edge, hysteresis = 1%	2.3		2.9	V
	12IN falling edge	1.8			
	12IN rising edge	5		10	
	VX, VY falling edge	1.4		2.9	
Standby Supply Current	VX or VY, all switches 0V or high-Z, control inputs = 0V or VL			15	µA
VY Quiescent Supply Current	Any combination of VY switches on, control inputs = 0V or VL, no VCC loads			100	µA
VX Quiescent Supply Current	Any combination of VX switches on, control inputs = 0V or high-Z, no VCC loads			100	µA
12IN_ Standby Supply Current	12INA tied to 12INB, all switches 0V or high-Z, control inputs = 0V or VL			15	µA
12IN_ Quiescent Supply Current	12INA tied to 12INB, VPPA and VPPB 12V switches on, control inputs = 0V or VL, no VPP loads			100	µA
VL Standby Supply Current	All switches 0V or high-Z, control inputs = 0V or VL			15	µA
VL Quiescent Supply Current	Any combination of switches on			150	µA
INTERFACE AND LOGIC SECTION					
$\overline{\text{SMBALERT}}$ Output Low Voltage	I_{SINK} = 1mA, low state			0.4	V
Logic Input Low Voltage	SMBCLK, SMBDATA, $\overline{\text{SMBSUS}}$			0.8	V
Logic Input High Voltage	SMBCLK, SMBDATA, $\overline{\text{SMBSUS}}$	2.2			V
Logic Output Low Voltage	SMBDATA, I_{SINK} = 4mA			0.4	V
ADR Input Low Voltage				0.6	V
ADR Input High Voltage		1.5			V

Dual-Channel CardBus and PCMCIA Power Switches with SMBus™ Serial Interface

Typical Operating Characteristics

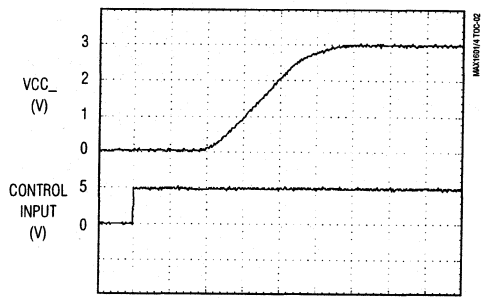
(VL = VY = 3.3V, VX = 5V, 12IN, T_A = +25°C, unless otherwise noted.)

VCC_ SWITCHING (RISE)



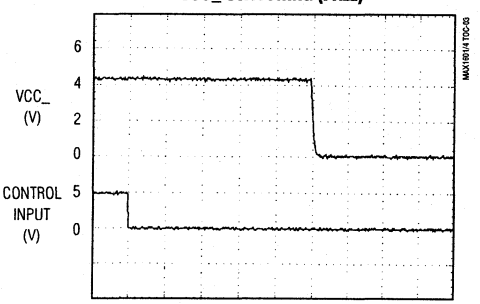
C_L = 30µF, R_L = 25Ω

VCC_ SWITCHING (RISE)



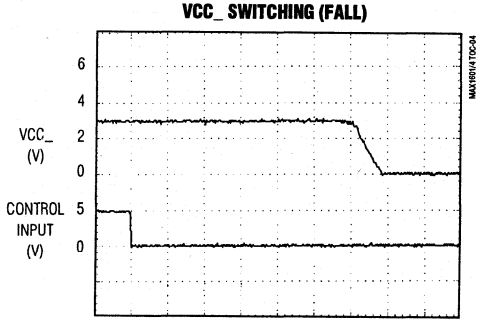
C_L = 1µF, R_L = ∞

VCC_ SWITCHING (FALL)



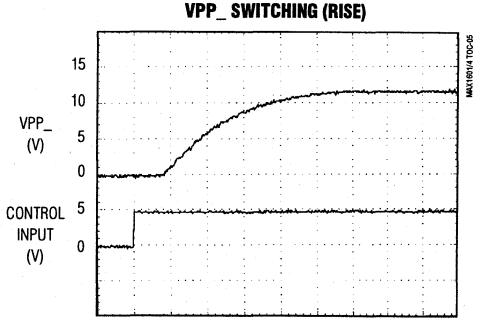
C_L = 33µF, R_L = ∞

VCC_ SWITCHING (FALL)



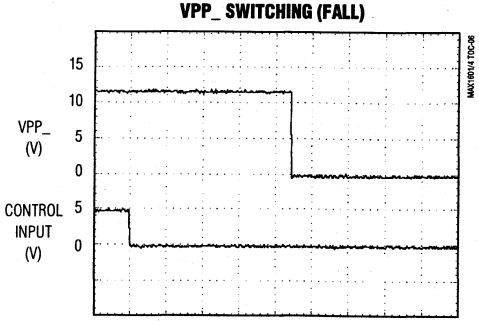
C_L = 1µF, R_L = 25Ω

VPP_ SWITCHING (RISE)



C_L = 0.1µF, R_L = ∞

VPP_ SWITCHING (FALL)

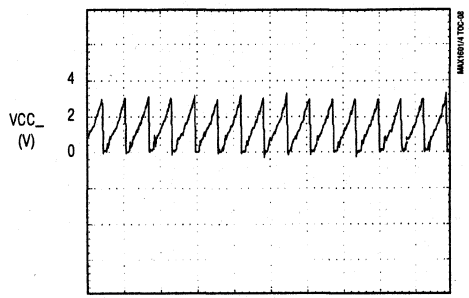


C_L = 0.1µF, R_L = ∞

Typical Operating Characteristics (continued)

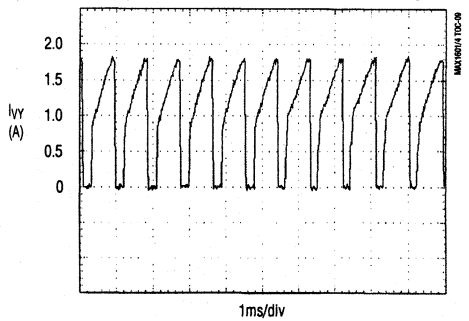
(VL = VY = 3.3V, VX = 5V, 12IN, T_A = +25°C, unless otherwise noted.)

VCC_ CURRENT LIMITING

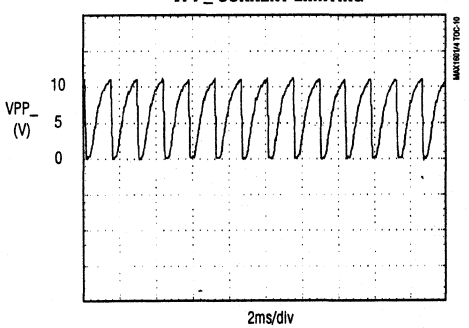


C_L = 1µF, RESISTIVE OVERLOAD, R_L = 1Ω

INPUT CURRENT (VCC OUTPUT SHORTED)

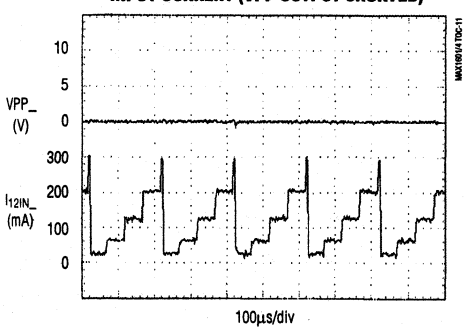


VPP_ CURRENT LIMITING



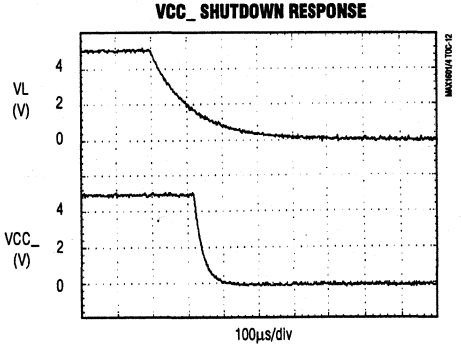
C_L = 1µF, R_L = 50Ω

INPUT CURRENT (VPP OUTPUT SHORTED)



R_L = 0.1Ω

VCC_ SHUTDOWN RESPONSE



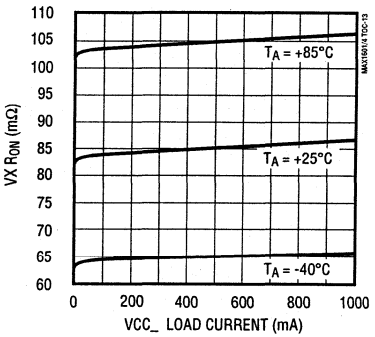
CIRCUIT OF FIGURE 2

Dual-Channel CardBus and PCMCIA Power Switches with SMBus™ Serial Interface

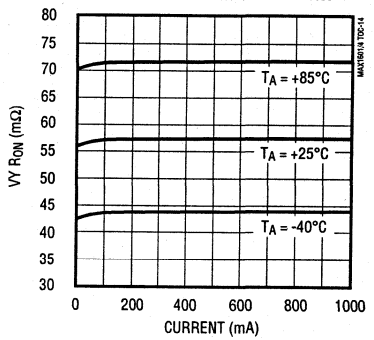
Typical Operating Characteristics (continued)

(VL = VY = 3.3V, VX = 5V, 12IN, T_A = +25°C, unless otherwise noted.)

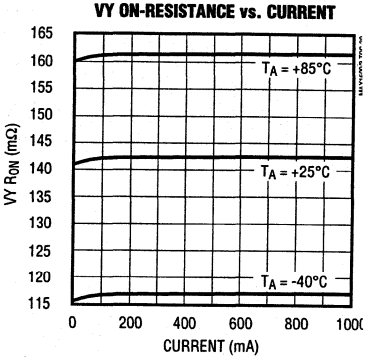
VX ON-RESISTANCE vs. VCC_ LOAD CURRENT



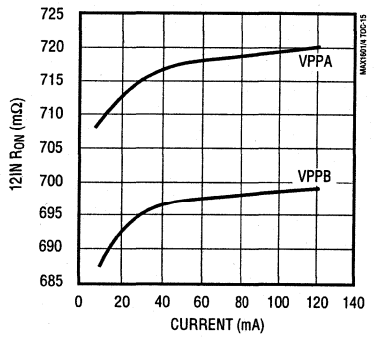
MAX1601 VY ON-RESISTANCE vs. CURRENT



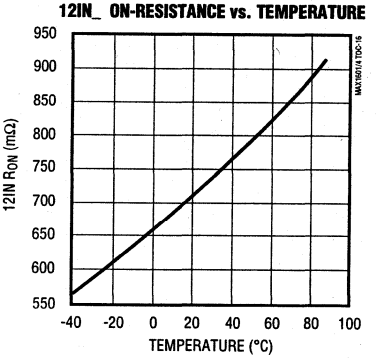
MAX1604 VY ON-RESISTANCE vs. CURRENT



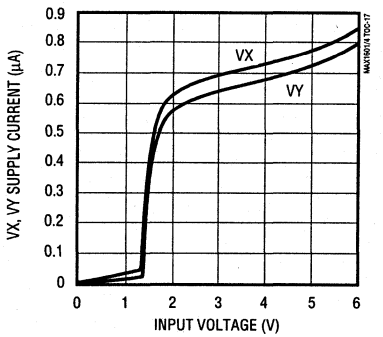
12IN_ ON-RESISTANCE vs. CURRENT



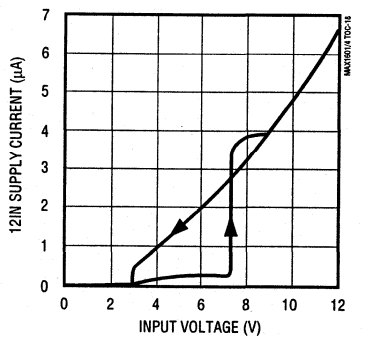
12IN_ ON-RESISTANCE vs. TEMPERATURE



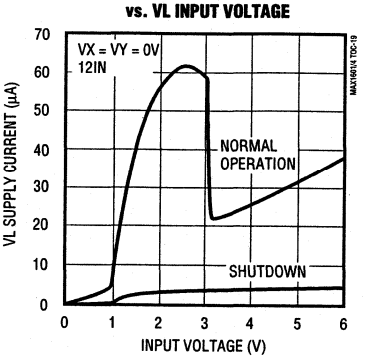
VX, VY SUPPLY CURRENT vs. INPUT VOLTAGE



12IN SUPPLY CURRENT vs. INPUT VOLTAGE



VL SUPPLY CURRENT vs. VL INPUT VOLTAGE



Pin Description

PIN	NAME	FUNCTION
1, 25	GND	Ground
2, 3, 26, 27	N.C.	No internal connection
4	12INA	+12V Supply Voltage Input, internally connects to channel A VPP switch. Tie to VPPA if not used.
5	VPPA	Channel A VPP Output
6, 8, 10	VX	VX Supply-Voltage Inputs. VX pins must be connected together. Input range is 3V to 5.5V. VX is normally connected to 5V.
7, 22, 24	VCCA	Channel A VCC Outputs
9, 18, 20	VCCB	Channel B VCC Outputs
11	VPPB	Channel B VPP Output
12	12INB	+12V Supply Voltage Input, internally connects to channel B VPP switch. Tie to VPPB if not used.
13	ADR	Address Input, sets SMBus address location. See Table 1 for address selection.
14	$\overline{\text{SMBSUS}}$	SMBus Suspend-Mode Control Input. The device will execute commands previously stored in the normal-mode register if $\overline{\text{SMBSUS}}$ is high, or will execute commands previously stored in the suspend-mode register if $\overline{\text{SMBSUS}}$ is low.
15	SMBCLK	SMBus Clock Input
16	SMBDATA	SMBus Data Input/Output, open drain
17	$\overline{\text{SMBALERT}}$	Fault-Detection Interrupt Output. $\overline{\text{SMBALERT}}$ goes low if either channel VCC or VPP switch is current limiting or undervoltage lockout, or if the thermal protection circuit is activated. $\overline{\text{SMBALERT}}$ is an open-drain output that requires an external pull-up resistor.
19, 21, 23	VY	VY Supply-Voltage Inputs. VY pins must be connected together. Input range is 3V to 5.5V. VY is normally connected to 3V.
28	VL	Logic Supply-Voltage Inputs. Connect to the +3.3V or +5V host system supply. VL can be supplied via the output of a CMOS-logic gate to produce an overriding shutdown. When used as a shutdown input, VL should have a 1kΩ series resistor with a 0.1µF capacitor to ground (Figure 2). Note that VL must be greater than undervoltage lockout for any switches to be turned on.

Dual-Channel CardBus and PCMCIA Power Switches with SMBus™ Serial Interface

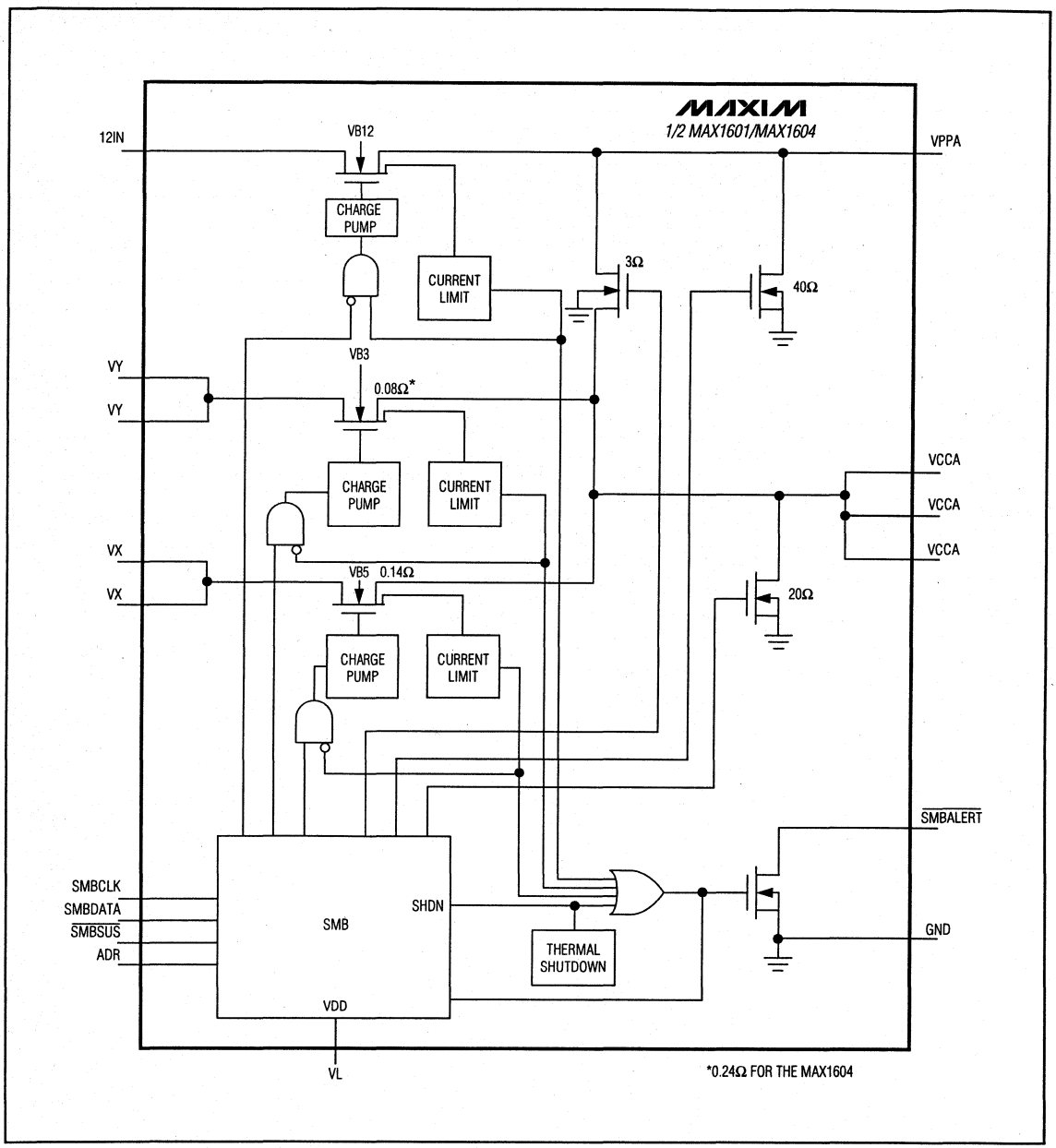


Figure 1. Functional Diagram (one channel of two)

Dual-Channel CardBus and PCMCIA Power Switches with SMBus™ Serial Interface

Detailed Description

The MAX1601/MAX1604 power-switching ICs contain a network of low-resistance MOSFET switches that deliver selectable VCC and VPP voltages to two Cardbus or PC Card host sockets. The MAX1601/MAX1604 differ only in the VY switch on-resistance. Figure 1 is the detailed block diagram.

The power-input pins (VY, VX, 12IN_) are completely independent. Low inrush current is guaranteed by controlled switch rise times. VCC's 100µs minimum output rise time is 100% tested with a 1µF capacitive load, and VPP's 1ms minimum rise time is guaranteed with a 0.1µF load. These respective capacitive loads are chosen as worst-case card-insertion parameters. The internal switching control allows VCC and VPP rise times to be controlled, and makes them nearly independent of resistive and capacitive loads (see rise-time photos in the *Typical Operating Characteristics*). Fall times are a function of loading, and are compensated by internal circuitry.

Power savings is automatic: internal charge pumps draw very low current when the VCC switches are static. Standby mode reduces switch supply current to 1µA. Driving the VL pin low with an external logic gate (master shutdown) reduces total supply current to1µA (Figure 2).

Operating Modes

The MAX1601/MAX1604 have three operating modes: normal, standby, and shutdown. Normal mode supplies the selected outputs with their appropriate supply voltages. Standby mode places all switches at ground, high impedance, or a combination of the two. Shutdown mode turns all switches off, and puts the VCC and VPP outputs into a high-impedance state. Pull VL low to enter shutdown mode. To ensure a 0.05V/µs fall rate on VL, use a 1kΩ series resistor and a 0.1µF capacitor to ground (Figure 2).

Overcurrent Protection

Peak detecting circuitry protects both the VCC and VPP switches against overcurrent conditions. When current through any switch exceeds the internal current limit (4A for VCC switches and 200mA for VPP switches), the switch turns off briefly, then turns on again at the controlled rise rate. If the overcurrent condition lasts more than 2µs, the $\overline{\text{SMBALERT}}$ output latches low. A continuous short-circuit condition results in a pulsed output current until thermal shutdown is reached. $\overline{\text{SMBALERT}}$ is open-drain and requires an external pull-up resistor.

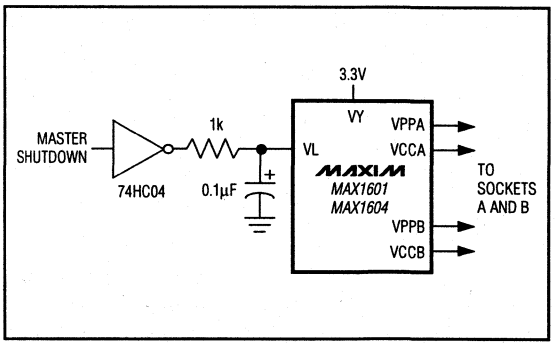


Figure 2. Master Shutdown Circuit

Thermal Shutdown

If the IC junction temperature rises above +150°C, the thermal shutdown circuitry opens all switches, including the GND switches, and $\overline{\text{SMBALERT}}$ is pulled low. When the temperature falls below +130°C, the switches turn on again at the controlled rise rate. If the overcurrent condition remains, the part cycles between thermal shutdown and overcurrent.

Undervoltage Lockout

If the VX or VY switch input voltage drops below 1.5V, the associated switch turns off and $\overline{\text{SMBALERT}}$ goes low. For example, if VY is 3.3V and VX is 0V, and if the interface controller selects VY, the VCCA output will be 3.3V. If VX is selected, VCCA changes to a high-impedance output and $\overline{\text{SMBALERT}}$ goes low.

When a voltage is initially applied to 12IN_, it must be greater than 8V to allow the switch to operate. Operation continues until the voltage falls below 2V (the VPP output is high impedance).

When VL drops to less than 2.3V, all switches are turned off and the VCC and VPP outputs are high impedance.

Dual-Channel CardBus and PCMCIA Power Switches with SMBus™ Serial Interface

SMBus™ Interface Operation

The SMBus serial interface is a two-wire interface with multi-mastering capability, intended to control low-speed peripheral devices in low-power portable equipment applications. SMBus is similar to I²C™ and AccessBus, but has slightly different logic threshold voltage levels, different fixed addresses, and a suspend-mode register capability. To obtain a complete set of specifications on the SMBus interface, call Intel at (800) 253-3696 and ask for product code SBS5220.

SMBus Addressing

These dual-channel PC Card switch devices respond to two of four different addresses, depending on the state of the ADR address pin. Normal writing to the device is done by transmitting one of four addresses, followed by a single data byte, to program the channel selected. Write transmissions to the interrupt pointer address are not supported by these devices. Reading from the device is done by transmitting one of two addresses corresponding to either the A channel address (which will provide data about faults for both A and B channels) or to the interrupt pointer address (discussed later).

The normal start condition consists of a high-to-low transition on SMBDATA while SMBCLK is high. The 7-bit address is followed by a bit that designates a read or write operation: high = read, low = write. If the 7-bit address matches one of the supported function addresses, the IC issues an acknowledge pulse by pulling the SMBDATA line low. If the address is not valid, the IC stays off of the bus and ignores any data on the bus until a new start condition is detected. Once the IC receives a valid address that includes a write bit, it expects to receive one additional byte of data. If a stop condition or new start condition is detected before a complete byte of data is clocked in, the IC interprets this as an error and all of the data is rejected and lost. SMBDATA and SMBCLK are Schmitt triggered and can accommodate slower edges. However, rising edges should still be faster than 1µs, and falling edges should be faster than 300ns.

SMBus Write Operations

If the IC receives a valid address immediately followed by a write bit, the IC becomes a slave receiver. The slave IC generates a first acknowledge after the address and write bit, and a second acknowledge after the command byte. A stop condition following the command (data) byte causes immediate execution of the command, unless the data included a low SUS/OP bit. If the data included a low SUS/OP bit, the command is stored in the suspend-mode register and is executed only when the SMBSUS pin is pulled low (Figure 3).

Table 1. SMBus Addressing

SMB ADDRESS	ADR PIN	WRITE FUNCTION	READ FUNCTION
0001100	Don't care	N/A	Interrupt Pointer
1010000	Grounded	Channel A	Channel A/B faults
1010001	Grounded	Channel B	Channel A/B faults
1010010	Tied to VL	Channel A	Channel A/B faults
1010011	Tied to VL	Channel B	Channel A/B faults

Table 2. Command Format for Channel A Write Operations (address 1010000 or 1010010)

BIT	NAME	POR STATE	FUNCTION
7 (MSB)	OP/SUS	0	Operate/suspend bit. Selects which latch receives data: high = operation, low = suspend.
6	VCCAON	0	Turns on VCCA when high, pulls VCCA to GND when low.
5	VCCA3/5	0	If VCCA is on, a high connects VY to VCCA, and a low connects VX to VCCA.
4	VCCAHIZ	0	Puts VCCA in a high-impedance state when high. Overrides VCCAON.
3	VPPAON	0	Turns on VPPA when high, pulls VPPA to GND when low.
2	VPPAPGM	0	If VPPA is on, a high connects VPPA to 12INA, and a low connects VPPA to VCCA.
1	VPPAHIZ	0	Puts VPPA in a high-impedance state when high. Overrides VPPAON.
0 (LSB)	MASKFLT	0	Masks fault interrupts from both channel A and channel B when high.

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SMBus is a trademark of Intel Corp.

Table 3. Command Format for Channel B Write Operations (address 1010001 or 1010011)

BIT	NAME	POR STATE	FUNCTION
7 (MSB)	OP/SUS	0	Operate/suspend bit. Selects which latch receives data: high = operation, low = suspend.
6	VCCBON	0	Turns on VCCB when high, pulls VCCB to GND when low.
5	VCCB3/5	0	If VCCB is on, a high connects VY to VCCB, and a low connects VX to VCCB.
4	VCCBHIZ	0	Puts VCCB in a high-impedance state when high. Overrides VCCBON.
3	VPPBON	0	Turns on VPPB when high, pulls VPPB to GND when low.
2	VPPBPGM	0	If VPPB is on, a high connects VPPB to 12INB, and a low connects VPPB to VCCB.
1	VPPBHIZ	0	Puts VPPB in a high-impedance state when high. Overrides VPPBON.
0 (LSB)	RFU	0	Reserved for future use.

Table 4. Read Format for Interrupt Pointer Address (0001100)

BIT	NAME	POR STATE	FUNCTION
7 (MSB)	ADD7	0	ADD7 to ADD1 provide a return address for any interrupt query. For these devices, the return addresses are: 1010000 = Channel A, ADD = low 1010001 = Channel B, ADD = low 1010010 = Channel A, ADD = high 1010011 = Channel B, ADD = high
6	ADD6	0	
5	ADD5	0	
4	ADD4	0	
3	ADD3	0	
2	ADD2	0	
1	ADD1	0	
0 (LSB)	ADD0	0	

Table 5. Read Format for Power Switch Address (1010000 or 1010010)

BIT	NAME	POR STATE	LATCHED?	FUNCTION
7 (MSB)	CATFAULT	0	Y	Indicates catastrophic (thermal or undervoltage lockout) fault when high.
6	FAULT1	0	Y	Indicates VCCA overcurrent/undervoltage lockout when high.
5	FAULT2	0	Y	Indicates VPPA overcurrent/undervoltage lockout when high.
4	FAULT3	0	Y	Indicates VCCB overcurrent/undervoltage lockout when high.
3	FAULT4	0	Y	Indicates VPPB overcurrent/undervoltage lockout when high.
2	SIG/DUAL	0	N	Indicates dual part (single-channel devices would read 1).
1	RFU	0	N	Reserved for future use.
0 (LSB)	RFU	0	N	Reserved for future use.

Dual-Channel CardBus and PCMCIA Power Switches with SMBus™ Serial Interface

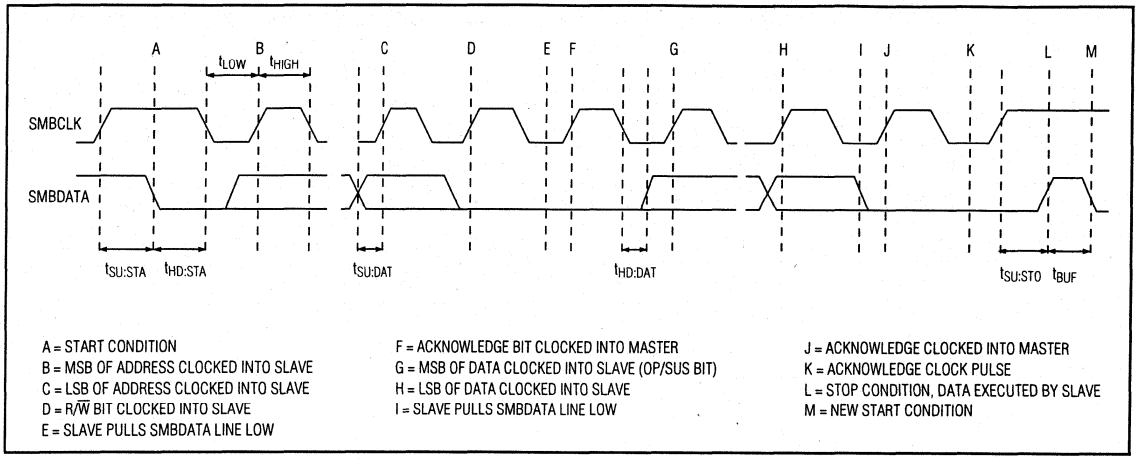


Figure 3. SMBus Write Timing Diagram

SMBus Read Operations

If the IC receives a valid address that includes a read bit, the IC becomes a slave transmitter. After receiving the address data, the IC generates an acknowledge during the acknowledge clock pulse and drives the SMBDATA line in sync with SMBCLK. The SMB protocol requires that the master end the read transmission by not acknowledging during the acknowledge bit of SMBCLK. These PC Card ICs support the repeated start-condition method for changing data-transfer direction; that is, a write transmission followed by a repeated start instead of a stop condition prepares the IC for data reading (Figure 4).

SMBus Interrupts

These PC Card power-switch ICs are slave devices only, and never initiate communications except by asserting an interrupt (by pulling $\overline{\text{SMBALERT}}$ low). Interrupts are generated only for reporting fault conditions, including overcurrent at VCCA, VCCB, VPPA, or VPPB, undervoltage lockout, and IC thermal overload. If an interrupt occurs, it can be an indication of impending system failure. The host system can react by going into suspend mode or taking other action. It can come back later to interrogate the IC via the interrupt pointer to determine status or perform corrective action (such as disabling the appropriate power switch that might be connected to a shorted PC card). The fastest method for turning off the switches in response to a fault condition is to cycle the voltage on VL in order to generate a power-on reset (which clears all of the SMBus registers). Note that the SMBus registers retain their data even if the main VX/VY supplies are turned off, provided that VL remains powered.

When a fault occurs, $\overline{\text{SMBALERT}}$ is immediately asserted and latched low. If the fault is momentary and disappears before the IC is serviced, the data is still latched in the interrupt pointer and $\overline{\text{SMBALERT}}$ remains asserted. Normally, the master (host system or PCMCIA digital controller) now sends out the interrupt pointer address (00011000) followed by a read bit. $\overline{\text{SMBALERT}}$ is cleared and the PC Card IC responds by putting out its address on the bus. If the fault persists, $\overline{\text{SMBALERT}}$ is re-asserted, but the data in the fault registers is not reloaded. The data in the fault latches only reflects the first time $\overline{\text{SMBALERT}}$ is asserted.

When the part enters operating mode, a false interrupt flag may be issued. The user needs to send the interrupt address to clear the false interrupt.

Normally, the master sends out the appropriate PC Card switch address on the bus, followed by a read bit. The data in the fault registers is then clocked out onto the bus (which also clears the fault registers). If the fault persists, the fault bits and $\overline{\text{SMBALERT}}$ are latched again.

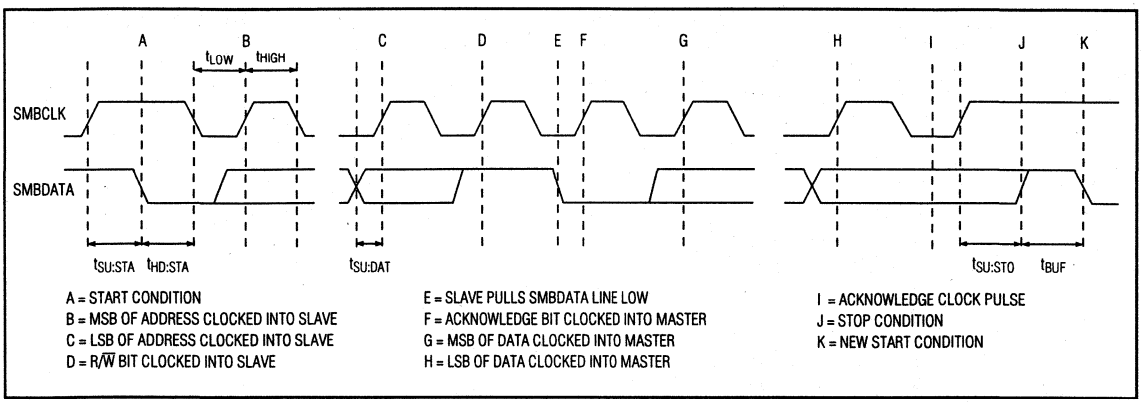


Figure 4. SMBus Read Timing Diagram

The interrupt pointer address provides quick fault identification for simple slave devices that lack the complex, expensive logic needed to be a bus master. The host can read the interrupt pointer to determine which slave device generated an SMBALERT interrupt signal. The interrupt pointer address can activate several different slave devices simultaneously, similar to an I²C general call. Any slave device that generated an interrupt attempts to identify itself by putting its own address on the bus during the first read byte. If more than one slave attempts to respond, bus arbitration rules apply and the device with the lower address code wins. The losing device won't generate an acknowledge and will continue to hold the SMBALERT line low until serviced, which implies that the host interrupt input must be level sensitive.

Applications Information

Supply Bypassing

Bypass the VY, VX, and 12IN_ inputs with ceramic 0.1µF capacitors. Bypass the VCC_ and VPP_ outputs with a 0.1µF capacitor for noise reduction and ESD protection.

Power-Up

Apply power to the VL input before any of the switch inputs. If VX, VY, or 12IN receive power before VL rises above 2.8V, the supply current may be artificially high (about 5mA). When the voltage on VL is greater than 2.8V (operating mode), the part consumes its specified 24µA. To avoid power sequencing, diode-OR VX and VY to VL through a 1kΩ resistor (Figure 5). Take care not to allow VL to drop below the 2.8V maximum undervoltage lockout threshold.

Changing SMBCLK and SMBDATA Simultaneously

When clocking data into the MAX1601/MAX1604, SMBDATA must not fall before SMBCLK. Otherwise, the MAX1601/MAX1604 may interpret this as a start condition. Even when SMBDATA and SMBCLK fall at the same instant, different fall times for the two signals may cause the erroneous generation of a start condition. To ensure that SMBDATA transitions after the falling edge of SMBCLK, add an RC network to SBMDATA (Figure 6).

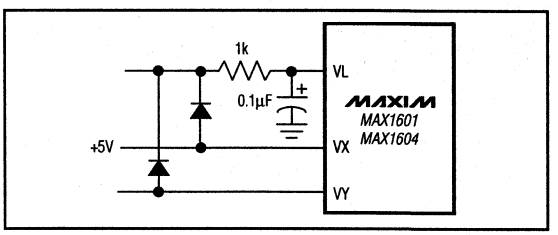


Figure 5. Powering from Either VX or VY

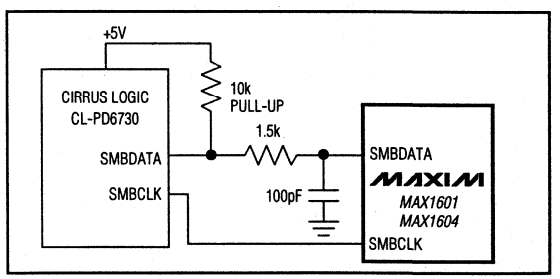
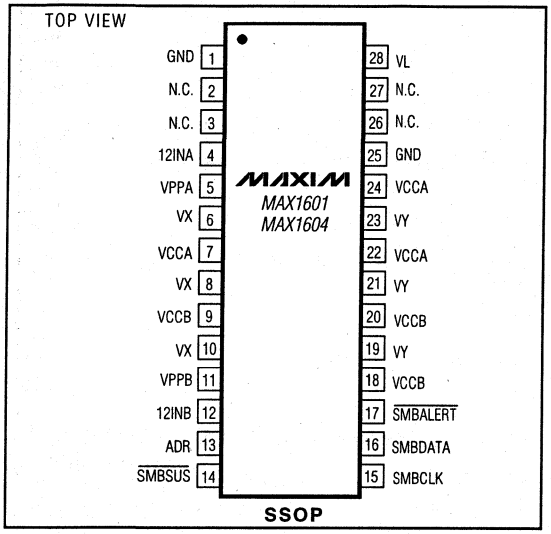


Figure 6. Application with Cirrus Logic Interface

Dual-Channel CardBus and PCMCIA Power Switches with SMBus™ Serial Interface

Pin Configuration



Chip Information

TRANSISTOR COUNT: 4372

19-1125; Rev 0; 9/96

MAXIM

Single-Channel CardBus and PCMCIA VCC/VPP Power-Switching Network

General Description

The MAX1602 DC power-switching IC contains a network of low-resistance MOSFET switches that deliver selectable VCC and VPP voltages to a single CardBus or PC Card host socket. Key features include low-resistance switches, small packaging, soft-switching action, and compliance with PCMCIA specifications for 3V/5V switching. 3.3V-only power switching for fast, 32-bit CardBus applications is supported in two ways: low-resistance 3.3V switches allow high 3.3V load currents (up to 1A); and completely independent internal charge pumps let the 3.3V switch operate normally, even if the +5V and +12V supplies are disconnected or turned off to conserve power. The internal charge pumps are regulating types that draw reduced input current when the VCC switches are static. Power consumption is automatically reduced to 11µA max when the outputs are high-Z or GND.

Other key features include guaranteed specifications for output current limit level, and guaranteed specifications for output rise/fall times (in compliance with PCMCIA specifications). Reliability is enhanced by thermal-overload protection, accurate current limiting, an overcurrent-fault flag output, and undervoltage lockouts. The CMOS/TTL-logic interface is flexible, and can tolerate logic input levels in excess of the positive supply rail.

The MAX1602 fits a complete CardBus/PCMCIA switch into a space-saving, 16-pin QSOP package.

Applications

Data Loggers
Handy-Terminals
Docking Stations
PCMCIA Read/Write Drives

Ordering Information

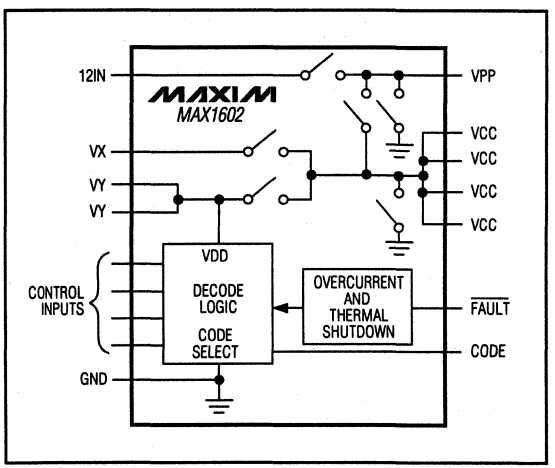
PART	TEMP. RANGE	PIN-PACKAGE
MAX1602EEE	-40°C to +85°C	16 QSOP

Pin Configuration appears on last page.

Features

- ♦ **Supports a Single PC Card/CardBus Socket**
- ♦ **1A, 0.25Ω Max 3.3V VCC Switch**
  1A, 0.25Ω Max 5V VCC Switch
- ♦ **Soft Switching for Low Inrush Surge Current**
- ♦ **Overcurrent Protection**
- ♦ **Overcurrent/Thermal-Fault Flag Output**
- ♦ **Thermal Shutdown at T_J = +150°C**
- ♦ **Independent Internal Charge Pumps**
- ♦ **Break-Before-Make Switching Action**
- ♦ **11µA Max Standby Supply Current**
- ♦ **5V and 12V Not Required for Low-$R_{DS(ON)}$ 3.3V Switching**
- ♦ **Complies with PCMCIA 3V/5V Switching Specifications**
- ♦ **Super-Small 16-Pin QSOP Package**
- ♦ **Code Compatible with:**
  Cirrus CL-PD67XX Family
  Databook DB86184
  Intel 82365SL (industry-standard coding)

Simplified Block Diagram



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Single-Channel CardBus and PCMCIA VCC/VPP Power-Switching Network

ABSOLUTE MAXIMUM RATINGS

Inputs/Outputs to GND
(VX, VY, VCC) (Note 1) ..... -0.3V, +6V
VPP Input/Output to GND
(12IN, VPP) (Note 1) ..... -0.3V, +15V
Logic Inputs to GND (A0VCC, A1VCC,
A0VPP, A1VPP) (Note 1) ..... -0.3V, +6V
CODE Input to GND ..... -0.3V, (VY + 0.3V)
VCC Output Current (Note 2) 4A
VPP Output Current (Note 2) 260mA
VCC Short Circuit to GND ..... Continuous
VPP Short Circuit to GND ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
QSOP (derate 8.3mW/°C above +70°C) 667mW
Operating Temperature Range
MAX1602EEE ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: There are no parasitic diodes between any of these pins, so there are no power-up sequencing restrictions (for example, logic input signals can be applied even if all of the supply voltage inputs are grounded).
Note 2: VCC and VPP outputs are internally current limited. See the *Electrical Characteristics*.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(VY = 3.3V, VX = 5V, 12IN = 12V, T_A = 0°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
POWER-SUPPLY SECTION					
Input Voltage Range	VX, VY	3.0		5.5	V
	12IN	11		13	
Undervoltage Lockout Threshold	VY falling edge	2.4	2.6	2.8	V
	12IN falling edge	1.8	3.0		
	12IN rising edge	5.0	8.0	10.0	
	VX falling edge	1.4	1.9	2.8	
VY Standby Supply Current	All switches 0V or high-Z, control inputs = 0V or VY, T_A = +25°C		3	11	µA
VX Standby Supply Current	VX all switches 0V or high-Z, control inputs = 0V or VY, T_A = +25°C			1	µA
12IN Standby Supply Current	All switches 0V or high-Z, control inputs = 0V or VY, T_A = +25°C			1	µA
VY Quiescent Supply Current	Any combination of VY switches on, control inputs = 0V or VY, no VCC loads		20	200	µA
VX Quiescent Supply Current	Control inputs = 0V or VY, no VCC loads		10	50	µA
12IN Quiescent Supply Current	VPP 12V switches on, control inputs = 0V or VY, no VPP loads		5	100	µA
VCC SWITCHES					
Operating Output Current Range	VCC, VX = VY = 3V to 5.5V	0		1	A
On-Resistance, VY Switches	12IN = 0V to 13V, VY = 3V, VX = 0V to 5.5V, I_{SWITCH} = 1A, T_A = +25°C		0.09	0.25	Ω
On-Resistance, VX Switches	12IN = 0V to 13V, VX = 4.5V, VY = 0V to 5.5V, I_{SWITCH} = 1A, T_A = +25°C		0.09	0.25	Ω
Output Current Limit	VCC	1.2		4	A

ELECTRICAL CHARACTERISTICS (continued)

(VY = 3.3V, VX = 5V, 12IN = 12V, T_A = 0°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Sink Current	VCC < 0.4V, programmed to 0V state	10			mA
Output Leakage Current	VCC forced to 0V, high-Z state, T_A = +25°C		1	10	µA
Output Propagation Delay Plus Rise Time	VCC, 0V to VX or VY, C_L = 30µF, R_L = 25Ω, 50% of input to 90% of output, T_A = +25°C		2	10	ms
Output Rise Time	VCC, 0V to VX or VY, C_L = 1µF, R_L = open circuit, 10% to 90% points, T_A = +25°C	100	1200		µs
Output Propagation Delay Plus Fall Time	VCC, VX or VY to 0V, C_L = 30µF, R_L = open circuit, 50% of input to 10% of output, T_A = +25°C		90	150	ms
Output Fall Time	VCC, VX or VY to 0V, C_L = 1µF, R_L = 25Ω, 90% to 10% points		6		ms
VPP SWITCHES					
Operating Output Current Range	VPP	0		120	mA
On-Resistance, 12V Switches	12IN = 11.6V, I_{SWITCH} = 100mA, T_A = +25°C		0.70	1	Ω
On-Resistance, VPP = VCC Switches	Programmed to VX (5V) or VY (3.3V), T_A = +25°C		3	6	Ω
Output Current Limit	VPP programmed to 12V	130	200	260	mA
Output Sink Current	VPP < 0.4V, programmed to 0V state	10			mA
Output Leakage Current	VPP forced to 0V, high-Z state, T_A = +25°C		0.1	10	µA
Output Propagation Delay Plus Rise Time	VPP, 0V to 12IN, C_L = 0.1µF, 50% of input to 90% of output, T_A = +25°C		1.2	30	ms
Output Rise Time	VPP, 0V to 12IN, C_L = 0.1µF, 10% to 90% points, T_A = +25°C	100	600		µs
Output Propagation Delay Plus Fall Time	VPP, 12IN to 0V, C_L = 0.1µF, 50% of input to 10% of output, T_A = +25°C		9	60	ms
Output Fall Time	VPP, 12IN to 0V, C_L = 0.1µF, R_L = 100Ω 90% to 10% points		6		ms
INTERFACE AND LOGIC SECTION					
$\overline{FAULT}$ Signal Propagation Delay	VCC or VPP, load step to $\overline{FAULT}$ output, 50% point to 50% point (Note 3)		1		µs
$\overline{FAULT}$ Output Low Voltage	I_{SINK} = 1mA, low state			0.4	V
$\overline{FAULT}$ Output Leakage Current	$V_{\overline{FAULT}}$ = 5.5V, high state	-0.5		0.5	µA
Thermal Shutdown Threshold	Hysteresis = 20°C (Note 4)		150		°C
Logic Input Low Voltage	_VCC, _VPP			0.6	V
Logic Input High Voltage	_VCC, _VPP	1.5			V
Code Input Low Voltage	"Intel" code	0		0.4	V
Code Input High Voltage	"Cirrus" code	VY - 0.4		VY	V
Code Input Mid-Level Voltage	"Databook" code	1.2		VY - 1.2	V
Logic Input Bias Current	_VCC, _VPP, code	-1		1	µA

Single-Channel CardBus and PCMCIA VCC/VPP Power-Switching Network

ELECTRICAL CHARACTERISTICS

(VY = 3.3V, VX = 5V, 12IN = 12V, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
POWER-SUPPLY SECTION					
Input Voltage Range	VX, VY	3.0		5.5	V
	12IN	11		13	
Undervoltage Lockout Threshold	VY falling edge, hysteresis = 1%	2.3		2.9	V
	12IN falling edge	1.8			
	12IN rising edge	5		10	
	VX, VY falling edge	1.4		2.9	
VY Standby Supply Current	All switches 0V or high-Z, control inputs = 0V or VY			30	µA
VX Standby Supply Current	VX, all switches 0V or high-Z, control inputs = 0V or VY, $T_A = T_{MIN}$ to T_{MAX}			15	µA
12IN Standby Supply Current	All switches 0V or high-Z, control inputs = 0V or VY			15	µA
VY Quiescent Supply Current	Any combination of VY switches on, control inputs = 0V or VY, no VCC loads			200	µA
VX Quiescent Supply Current	Any combination of VX switches on, control inputs = 0V or high-Z, no VCC loads			50	µA
12IN Quiescent Supply Current	12V switches on, control inputs = 0V or VY, no VPP loads			100	µA
$\overline{FAULT}$ Output Low Voltage	I_{SINK} = 1mA, low state			0.4	V
Logic Input Low Voltage	_VCC, _VPP			0.6	V
Logic Input High Voltage	_VCC, _VPP	1.6			V

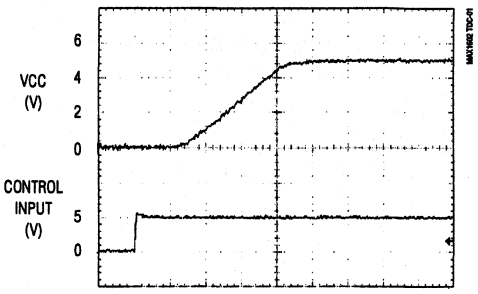
Note 3: Not production tested.

Note 4: Thermal limit not active in standby state (all switches programmed to GND or high-Z state).

Typical Operating Characteristics

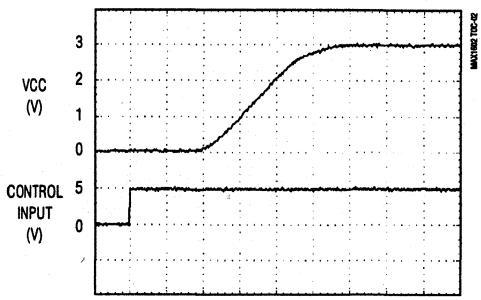
(VY = 3.3V, VX = 5V, 12IN = 12V, T_A = +25°C, unless otherwise noted.)

VCC SWITCHING (RISE)



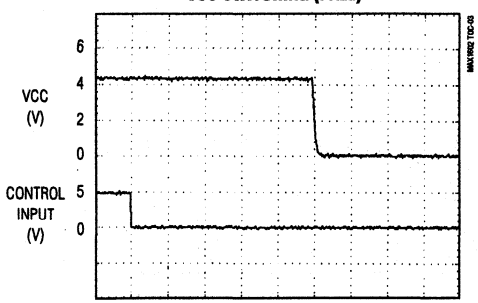
C_L = 30µF, R_L = 25Ω

VCC SWITCHING (RISE)



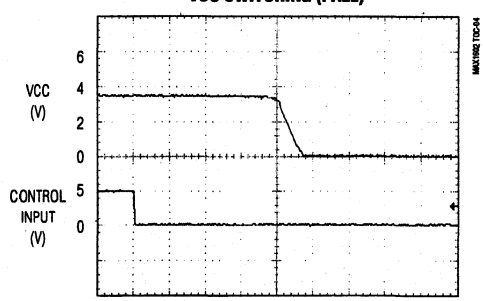
C_L = 1µF, R_L = ∞

VCC SWITCHING (FALL)



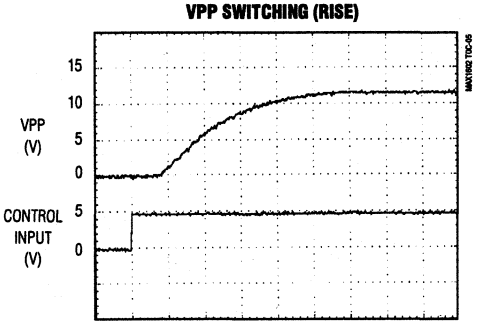
C_L = 33µF, R_L = ∞

VCC SWITCHING (FALL)



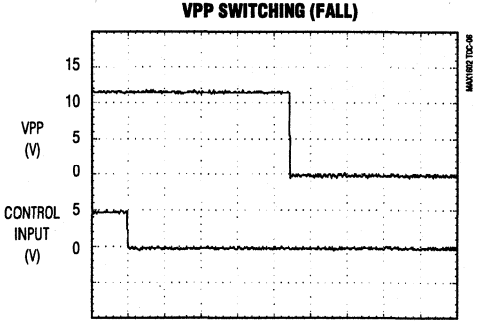
C_L = 1µF, R_L = 25Ω

VPP SWITCHING (RISE)



C_L = 0.1µF, R_L = ∞

VPP SWITCHING (FALL)



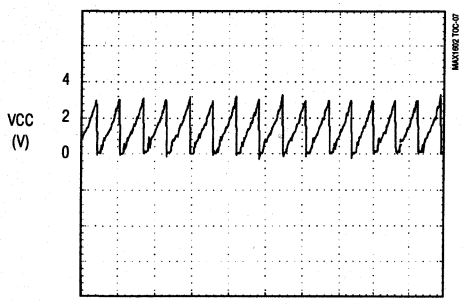
C_L = 0.1µF, R_L = ∞

Single-Channel CardBus and PCMCIA VCC/VPP Power-Switching Network

Typical Operating Characteristics (continued)

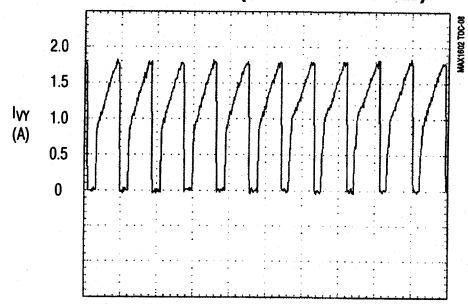
(VY = 3.3V, VX = 5V, 12IN = 12V, T_A = +25°C, unless otherwise noted.)

VCC CURRENT LIMITING

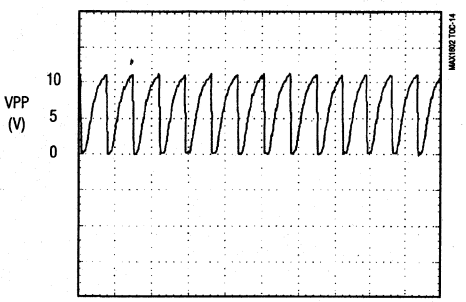


C_L = 1µF, RESISTIVE OVERLOAD, R_L = 1Ω

INPUT CURRENT (VCC OUTPUT SHORTED)

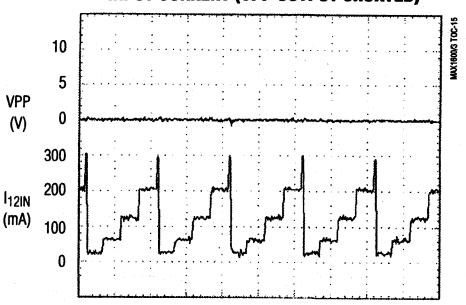


VPP CURRENT LIMITING



C_L = 1µF, R_L = 50Ω

INPUT CURRENT (VPP OUTPUT SHORTED)

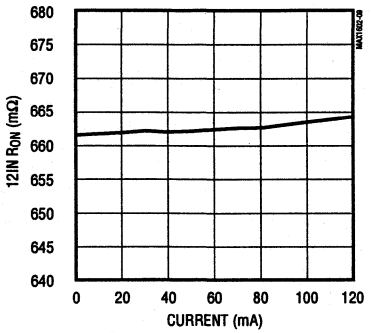


R_L = 0.1Ω

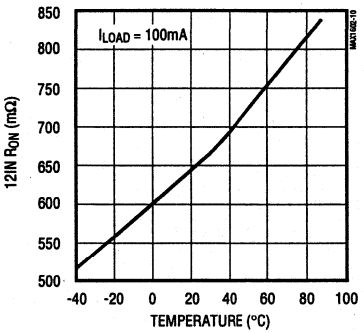
Typical Operating Characteristics (continued)

(VY = 3.3V, VX = 5V, 12IN = 12V, T_A = +25°C, unless otherwise noted.)

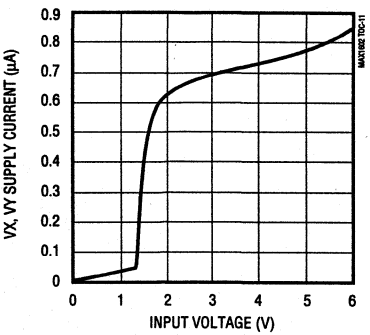
12IN ON-RESISTANCE vs. CURRENT



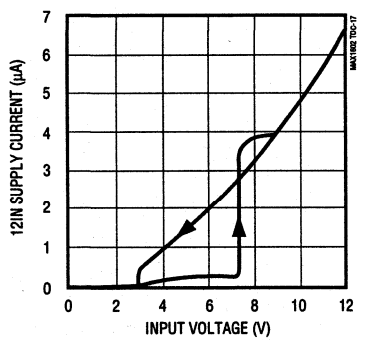
12IN ON-RESISTANCE vs. TEMPERATURE



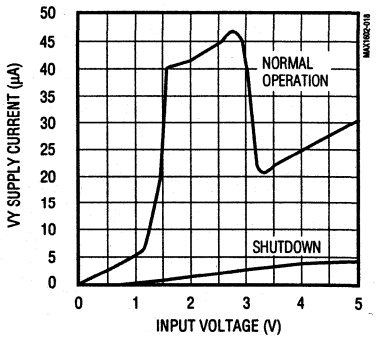
VX SUPPLY CURRENT vs. INPUT VOLTAGE



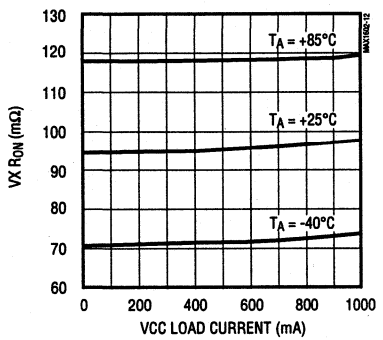
12IN SUPPLY CURRENT vs. INPUT VOLTAGE



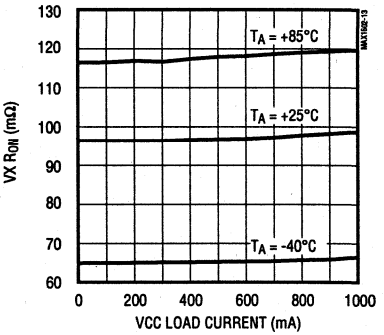
VY SUPPLY CURRENT vs. INPUT VOLTAGE



VX ON-RESISTANCE vs. VCC LOAD CURRENT



VY ON-RESISTANCE vs. VCC LOAD CURRENT



Single-Channel CardBus and PCMCIA VCC/VPP Power-Switching Network

Pin Description

PIN	NAME	FUNCTION
1	GND	Ground
2	12IN	+12V Supply Voltage Input
3	VPP	VPP Output
4, 6, 7, 9	VCC	VCC Output. Connect all four VCC pins together.
5	VX	VX Supply Voltage Input. Input range is +3.0V to +5.5V. VX is normally connected to 5V.
8, 10	VY	VY and Logic Supply Voltage Inputs. VY pins must be connected together. Input range is +3V to +5.5V. VY is normally connected to 3.3V.
11	A0VPP	VPP Control Input (*see Logic Truth Tables).*
12	A1VPP	VPP Control Input (*see Logic Truth Tables).*
13	A0VCC	VCC Control Input (see *Logic Truth Tables).*
14	A1VCC	VCC Control Input (see *Logic Truth Tables).*
15	CODE	Three-Level Code-Select Input (see *Logic Truth Tables):* Low = Standard "Intel" code, High = "Cirrus" code, Mid-Supply = "Databook" code (Figure 4).
16	$\overline{\text{FAULT}}$	Fault-Detection Output. $\overline{\text{FAULT}}$ goes low during current limit, undervoltage lockout, or thermal limit. $\overline{\text{FAULT}}$ is an open-drain output that requires an external pull-up resistor.

Logic Truth Tables

Table 1. Standard "Intel" Code (82365SL), CODE = GND

A1VCC	A0VCC	A1VPP	A0VPP	VCC	VPP	MODE
0	0	0	0	GND	GND	STBY
0	0	0	1	GND	GND	STBY
0	0	1	0	GND	GND	STBY
0	0	1	1	GND	GND	STBY
0	1	0	0	VY	GND	Active
0	1	0	1	VY	VCC	Active
0	1	1	0	VY	12IN	Active
0	1	1	1	VY	High-Z	Active
1	0	0	0	VX	GND	Active
1	0	0	1	VX	VCC	Active
1	0	1	0	VX	12IN	Active
1	0	1	1	VX	High-Z	Active
1	1	0	0	VY	GND	Active
1	1	0	1	VY	VCC	Active
1	1	1	0	VY	12IN	Active
1	1	1	1	VY	High-Z	Active

STBY = Standby Mode

Table 2. "Cirrus" Code, CODE = High (VY)

A1VCC	A0VCC	A1VPP	A0VPP	VCC	VPP	MODE
0	0	0	0	High-Z	High-Z	STBY
0	0	0	1	High-Z	High-Z	STBY
0	0	1	0	High-Z	High-Z	STBY
0	0	1	1	High-Z	High-Z	STBY
0	1	0	0	VX	GND	Active
0	1	0	1	VX	VCC	Active
0	1	1	0	VX	12IN	Active
0	1	1	1	VX	High-Z	Active
1	0	0	0	VY	GND	Active
1	0	0	1	VY	VCC	Active
1	0	1	0	VY	12IN	Active
1	0	1	1	VY	High-Z	Active
1	1	0	0	GND	GND	STBY
1	1	0	1	GND	GND	STBY
1	1	1	0	GND	GND	STBY
1	1	1	1	GND	GND	STBY

STBY = Standby Mode

Logic Truth Tables (cont.)

Table 3. "Databook" Code, CODE = Mid-Supply (VY/2)

A1VCC	A0VCC	AVPP	A0VPP	VCC	VPP	MODE
0	0	0	X	GND	High-Z	STBY
0	0	1	X	VY	12IN	Active
0	1	0	X	GND	GND	STBY
0	1	1	X	VX	12IN	Active
1	0	0	X	VY	VCC	Active
1	0	1	X	VY	GND	Active
1	1	0	X	VX	VCC	Active
1	1	1	X	VX	GND	Active

STBY = Standby Mode, X = Don't Care

Detailed Description

The MAX1602 power-switching IC contains a network of low-resistance MOSFET switches that deliver selectable VCC and VPP voltages to two CardBus or PC Card host socket. Figure 1 is the detailed block diagram.

The power-input pins (VY, VX, 12IN) are completely independent, however, power must always be applied to VY for proper operation. Low inrush current is guaranteed by controlled switch rise times. VCC's 100µs minimum output rise time is 100% tested with a 1µF capacitive load, and VPP's 1ms minimum rise time is guaranteed with a 0.1µF load. These respective capacitive loads are chosen as worst-case card-insertion parameters. The internal switching control allows VCC and VPP rise times to be controlled, and makes them nearly

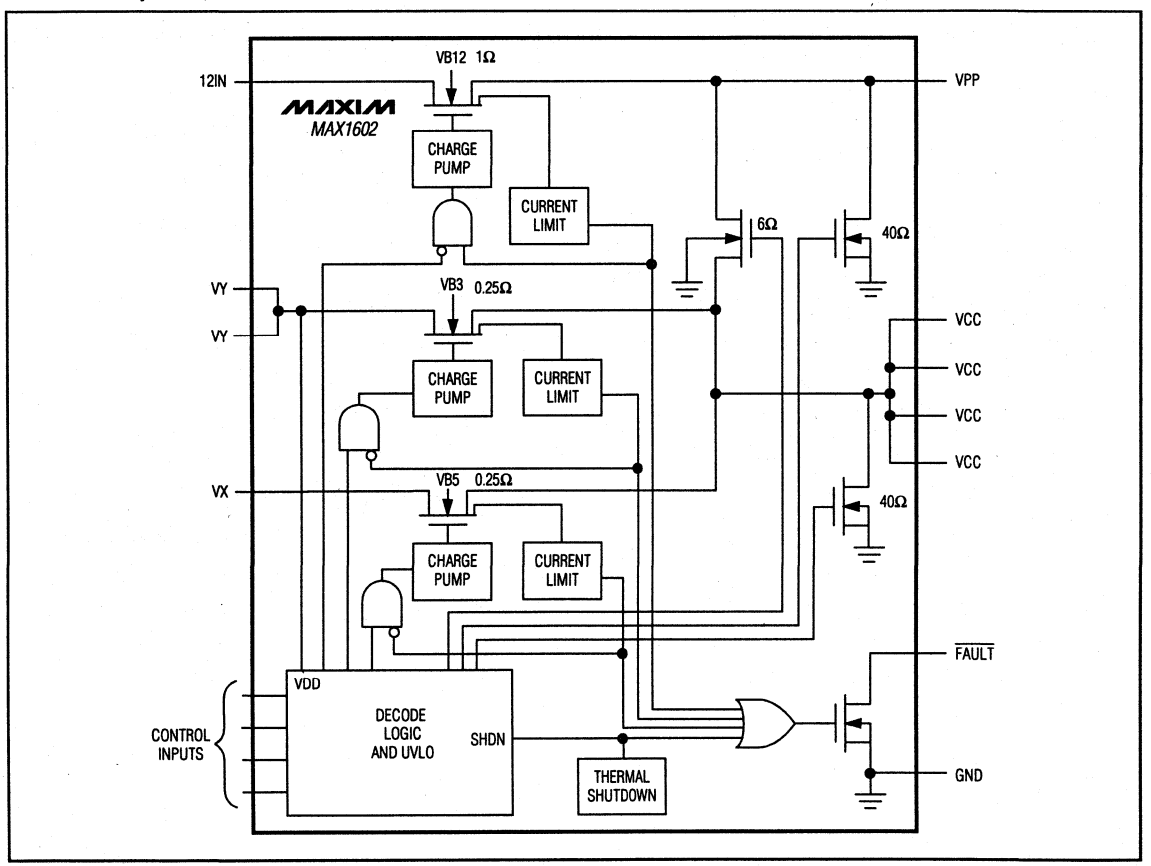


Figure 1. Detailed Block Diagram

Single-Channel CardBus and PCMCIA VCC/VPP Power-Switching Network

independent of resistive and capacitive loads (see rise-time photos in the *Typical Operating Characteristics*). Fall times are a function of loading, and are compensated by internal circuitry.

Power savings is automatic: internal charge pumps draw very low current when the VCC switches are static. Standby mode reduces switch supply current to 11µA.

Operating Modes

The MAX1602 is compatible with the Cirrus CL-PD67XX, Databook DB86184, and Intel 82365SL PC Card Interface Controllers (PCIC). Four control inputs select the internal switches' positions and the operating modes according to the input code. Select the proper code format for the chosen controller with the CODE input pin (see *Pin Description* and Tables 1, 2, and 3). CODE reconfigures the logic decoder to one of three interface controllers:

Low = Standard "Intel" code (Figure 3)

High = "Cirrus" code (Figure 2)

Mid-supply = "Databook" code (Figure 4)

An additional 1µA (3µA max) of VY supply current will flow if CODE = mid-supply (VY/2).

The MAX1602 has two operating modes: normal and standby. Normal mode supplies the selected outputs with their appropriate supply voltages. Standby mode places all switches at ground, high impedance, or a combination of the two.

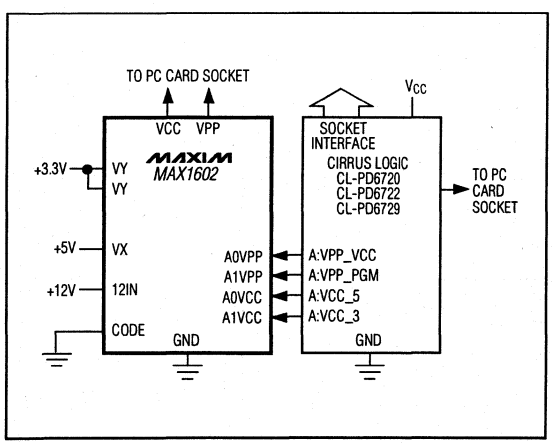


Figure 2. Application with Cirrus Logic Interface

Overcurrent Protection

Peak detecting circuitry protects both the VCC and VPP switches against overcurrent conditions. When current through any switch exceeds the internal current limit (4A for VCC switches and 200mA for VPP switches) the switch turns off briefly, then turns on again at the controlled rise rate. If the overcurrent condition lasts more than 2µs, the $\overline{\text{FAULT}}$ output goes low. $\overline{\text{FAULT}}$ is not latched. A continuous short-circuit condition results in a pulsed output current and a pulsed $\overline{\text{FAULT}}$ output until thermal shutdown is reached. $\overline{\text{FAULT}}$ is open-drain and requires an external pull-up resistor.

Thermal Shutdown

If the IC junction temperature rises above +150°C, the thermal shutdown circuitry opens all switches, including the GND switches, and $\overline{\text{FAULT}}$ is pulled low. When the temperature falls below +130°C, the switches turn on again at the controlled rise rate. If the overcurrent condition remains, the part cycles between thermal shutdown and overcurrent.

Undervoltage Lockout

If the VX switch input voltage drops below 1.9V, the associated switch turns off and $\overline{\text{FAULT}}$ goes low. For example, if VY is 3.3V and VX is 0V, and if the interface controller selects VY, the VCC output will be 3.3V. If VX is selected, VCC changes to a high-impedance output and $\overline{\text{FAULT}}$ goes low.

When a voltage is initially applied to 12IN, it must be greater than 8V to allow the switch to operate. Operation continues until the voltage falls below 2V (the VPP output is high impedance).

When VY drops to less than 2.6V, all switches are turned off and the VCC and VPP outputs are high impedance.

Applications Information

Supply Bypassing

Bypass the VY, VX, and 12IN inputs with ceramic 0.1µF capacitors. Bypass the VCC and VPP outputs with a 0.1µF capacitor for noise reduction and ESD protection.

Single-Channel CardBus and PCMCIA VCC/VPP Power-Switching Network

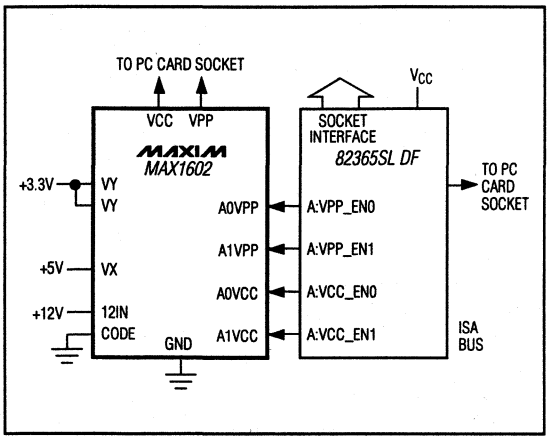


Figure 3. Application with Intel Interface

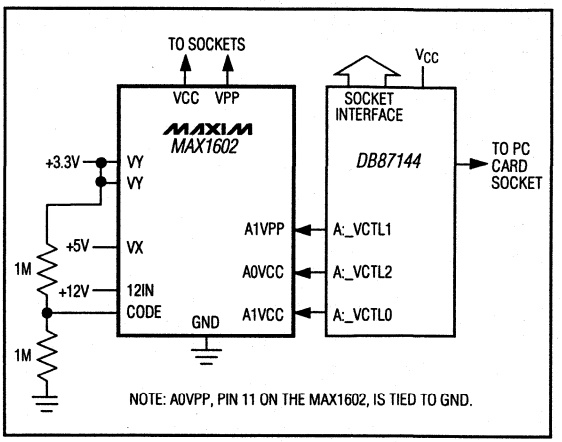
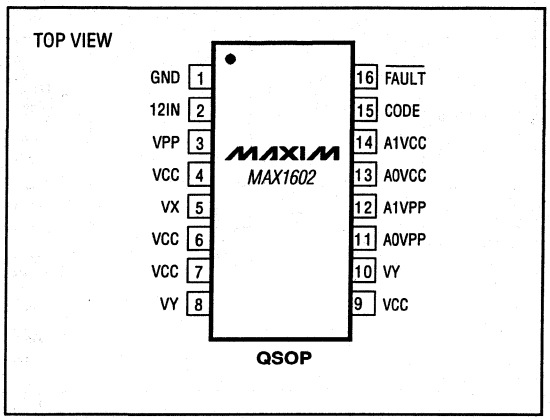


Figure 4. Block Diagram of the Databook DB87144 PCI to CardBus Controller Interface to the MAX1602

Single-Channel CardBus and PCMCIA VCC/VPP Power-Switching Network

Pin Configuration



Chip Information

TRANSISTOR COUNT: 1452

19-1128; Rev 0; 9/96

EVALUATION KIT AVAILABLE

MAXIM

Digitally Controlled CCFL Backlight Power Supplies

General Description

The MAX1610/MAX1611 are fully integrated, high-efficiency drivers for cold-cathode fluorescent lamps (CCFLs). They operate from a 4.5V to 26V power source. An on-board, high-switching-frequency power MOSFET reduces external component count and magnetics size. The MAX1610/MAX1611 protect against open or shorted lamps. The CCFL can be driven from an isolated transformer secondary winding to improve efficiency and avoid flicker at dim tube settings. Brightness is adjusted by scaling the lamp current, or by operating with a fixed lamp current and chopping the CCFL on and off at a rate faster than the eye can detect.

The MAX1610's digital inputs increment, decrement, or clear an internal, 5-bit up/down counter, which sets CCFL brightness. The MAX1611 uses a System Management Bus (SMBus) 2-wire serial interface to directly set CCFL brightness. Both devices include micropower shutdown and a linear regulator that eliminates the need for a separate logic supply. The digital interface remains active in shutdown, preserving the brightness setting.

Features

- ♦ **Direct Digital Control of CCFL Brightness**
- ♦ **Low Supply Current: 3mA Max Operating**
  20µA Max Shutdown
- ♦ **Low-Voltage Operation, Down to 4.5V**
- ♦ **Internal 26V, 0.7Ω Power Switch**
- ♦ **Protection Against Open or Shorted Lamps**
- ♦ **Supports Isolated Transformer Secondary Winding**
- ♦ **SMBus Serial Interface (MAX1611)**
- ♦ **No Flicker at Low Brightness (internal 280Hz current chopping)**
- ♦ **High Power-to-Light Efficiency**
- ♦ **Selectable 290kHz/145kHz Switching Frequency**
- ♦ **Oscillator SYNC Input**
- ♦ **16-Pin Narrow SO Package**

Applications

Notebook/Laptop Computers
Point-of-Sale Terminals
Portable Medical Equipment
Instrument Displays

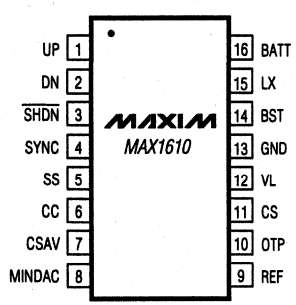
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1610CSE	0°C to +70°C	16 Narrow SO
MAX1611CSE	0°C to +70°C	16 Narrow SO

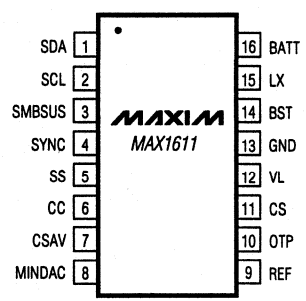
4

Pin Configurations

TOP VIEW



SO



SO

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Digitally Controlled CCFL Backlight Power Supplies

ABSOLUTE MAXIMUM RATINGS

BATT to GND .....-0.3V to 28V
BST to GND .....-0.3V to 30V
BST to LX .....-0.3V to 6V
LX to GND .....-0.6V to (BATT + 0.3V)
VL to GND .....-0.3V to 6V
CS, CSAV, CC, SYNC, REF, MINDAC, SS, OTP to GND .....-0.3V to (VL + 0.3V)
SHDN, UP, DN to GND .....-0.3V to 6V
SMBSUS, SDA, SCL to GND .....-0.3V to 6V

BATT, LX Current 1A
SDA Current 50mA
VL Current 50mA
Continuous Power Dissipation (T_A = +70°C)
SO (derate 8.70mW/°C above +70°C) 696mW
Operating Temperature Range
MAX1610CSE/MAX1611CSE .....0°C to +70°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functiona operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure tc absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = 0°C to +70°C, BATT = 8.2V, MINDAC = 0V, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY AND REFERENCE					
BATT Input Voltage Range		4.75		26	V
BATT Quiescent Supply Current, Operate Mode	BATT = 25V		1.5	3	mA
BATT Quiescent Supply Current, Shutdown Mode			10	20	µA
VL Output Voltage, Operate Mode	4.75V < BATT < 26V	4.25	4.5	4.75	V
VL Output Voltage, Shutdown Mode		3.0	3.6	4.75	V
REF Output Voltage	No load	1.92	2.0	2.08	V
REF Load Regulation	I_{SOURCE} = 100µA		6	20	mV
SWITCHING REGULATOR					
BATT-to-LX Switch On-Resistance	BST - LX = 4.1V		0.7	1.0	Ω
LX Switch Off-Leakage Current				10	µA
Oscillator Frequency	SYNC = REF	250	290	330	kHz
	SYNC = GND	125	145	165	
Oscillator SYNC Pin Synchronization Range		240		350	kHz
SYNC High Pulse Width		200			ns
SYNC Low Pulse Width		200			ns
SYNC Input Current	SYNC = GND or VL	-1		1	µA
SYNC Input Low Voltage				0.5	V
SYNC Input High Voltage		4.0			V
Power-Switch Maximum Duty Cycle	SYNC = REF	89	91		%
SS Source Current	SS = GND	2.5	4.0	5.5	µA
SS Sink Current	SS = 0.5V	2			mA

ELECTRICAL CHARACTERISTICS (continued)

(T_A = 0°C to +70°C, BATT = 8.2V, MINDAC = 0V, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DAC AND ERROR AMPLIFIER					
DAC Resolution	Guaranteed monotonic	5			Bits
MINDAC Input Voltage Range		0		1	V
MINDAC Input Bias Current		-1		1	µA
MINDAC Digital PWM Threshold			3		V
CSAV Input Voltage Range		0		1.0	V
CSAV Regulation Point	D/A at full scale	232	247	260	mV
	D/A at 1LSB		12		
CSAV Input Bias Current		-5		5	µA
CSAV to CC Voltage-to-Current Converter Transconductance	CC = 2V, CSAV = 1V, D/A at 1LSB		85		µmho
CC Sink Current	CC = 2V, CSAV = 1V, D/A at 1LSB		80		µA
CC Source Current	CC = 2V, CSAV = 0V, D/A at full scale		20		µA
OPEN AND SHORTED TUBE PROTECTION					
OTP Voltage Trip Point	Referred to REF, OTP rising	-20		20	mV
OTP Input Bias Current	GND < OTP < VL	-1		1	µA
CS Overcurrent Cutoff Threshold			500		mV
MAX1610 LOGIC LEVELS					
$\overline{SHDN}$, UP, DN Input Low Voltage				0.8	V
$\overline{SHDN}$, UP, DN Input High Voltage		2.4			V
$\overline{SHDN}$, UP, DN Input Bias Current		-1		1	µA
MAX1611 LOGIC LEVELS					
SMBSUS, SDA, SCL Input Low Voltage				0.8	V
SMBSUS, SDA, SCL Input High Voltage		2.2			V
SMBSUS, SDA, SCL Input Bias Current		-1		1	µA
SDA Output Low Sink Current	V_{SDA} = 0.6V	6			mA

Digitally Controlled CCFL Backlight Power Supplies

TIMING CHARACTERISTICS—MAX1610

(Figure 1, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
UP, DN Pulse Width High	t_1		1			µs
UP, DN Pulse Width Low	t_2		1			µs
UP, DN Pulse Separation	t_3		1			µs
Counter Reset Time	t_4		1			µs

TIMING CHARACTERISTICS—MAX1611

(Figures 2 and 3, T_A = +25°C, unless otherwise noted.)

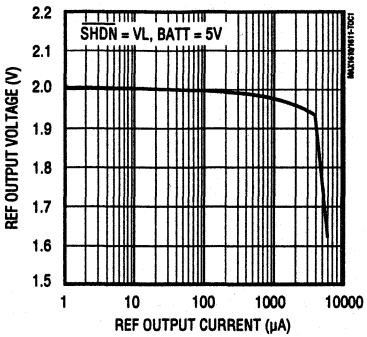
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Serial Clock High Period	t_{HIGH}		4			µs
SCL Serial Clock Low Period	t_{LOW}		4.7			µs
SCL, SCA Rise Time	t_R	(Note 1)			1	µs
SCL, SDA Fall Time	t_F	(Note 1)			0.3	µs
Start Condition Setup Time	$t_{SU:STA}$		4.7			µs
Start Condition Hold Time	$t_{HD:STA}$		4			µs
SDA Valid to SCL Rising Edge Setup Time, Slave Clocking in Data	$t_{SU:DAT}$		500			ns
SCL Falling Edge to SDA Transition	$t_{HD:DAT}$	(Note 1)	0			ns
SCL Falling Edge to SDA Valid, Reading Out Data	t_{DV}				1	µs

Note 1: Guaranteed by design.

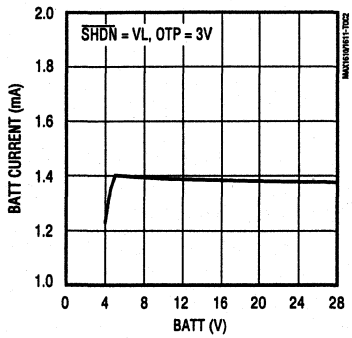
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

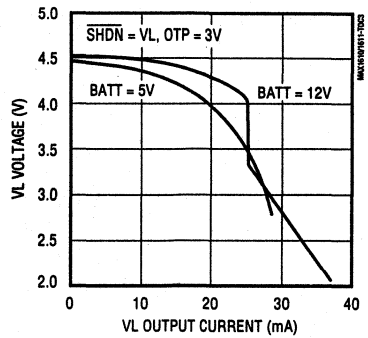
REF OUTPUT VOLTAGE vs. REF OUTPUT CURRENT



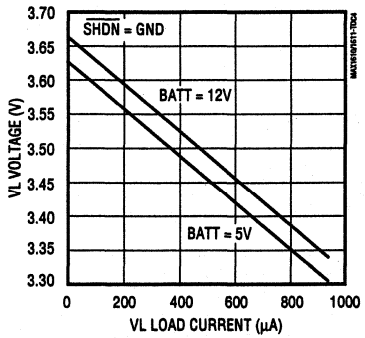
BATT SUPPLY CURRENT vs. BATT VOLTAGE (SHDN = VL)



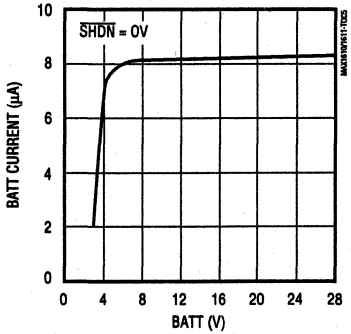
VL OUTPUT VOLTAGE vs. VL OUTPUT CURRENT



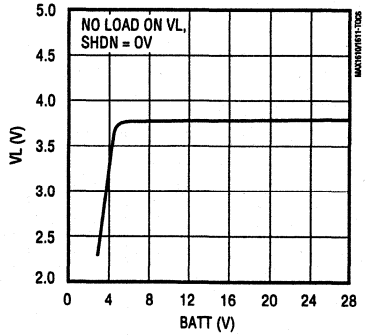
VL OUTPUT VOLTAGE vs. VL LOAD CURRENT



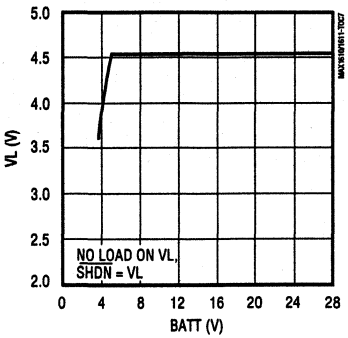
BATT SUPPLY CURRENT vs. BATT VOLTAGE (SHDN = 0V)



VL OUTPUT VOLTAGE vs. BATT VOLTAGE (SHDN = 0V)



VL OUTPUT VOLTAGE vs. BATT VOLTAGE (SHDN = VL)



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Pin Description

PIN		NAME	FUNCTION
MAX1610	MAX1611		
1	—	UP	Logic-Level Input. A rising edge on UP increments the 5-bit counter for the 5-bit DAC. UP = DN = 1 presets the counter to mid-scale.
—	1	SDA	System Management Bus Serial Data Input and Open-Drain Output
2	—	DN	Logic-Level Input. A rising edge on DN decrements the 5-bit counter for the 5-bit DAC. UP = DN = 1 presets the counter to mid-scale.
—	2	SCL	System Management Bus Serial Clock Input
3	—	$\overline{SHDN}$	Logic-Level Shutdown Input Pin. Applying a logic low to $\overline{SHDN}$ places the chip in a low-supply-current shutdown mode.
—	3	SMBSUS	System Management Bus Suspend Mode Input. SMBSUS Selects one of two chip-configuration settings, which are preprogrammed serially.
4	4	SYNC	Oscillator Synchronization Input. Tying SYNC to REF sets the oscillator frequency to 290kHz. Tying SYNC to GND or VL lowers the oscillator frequency to 145kHz.
5	5	SS	Soft-Start Pin. A 4µA current source feeds the capacitor placed on SS. The voltage on this pin limits the peak current in the switch. When the lamp is turned off, SS pulls to GND.
6	6	CC	Output of the Voltage-to-Current Converter; Input to the PWM Comparator, which sets the current limit. A capacitor placed at CC sets the current-regulator-loop bandwidth.
7	7	CSAV	Input to the Voltage-to-Current Converter, which averages the voltage on CSAV using the capacitor on CC.
8	8	MINDAC	The voltage at MINDAC sets the DAC's minimum-scale output voltage. Tying MINDAC to VL enables the internal 280Hz current-chopping mode.
9	9	REF	2.0V Reference Output. Bypass with 0.1µF to GND.
10	10	OTP	Open-Tube Protection Comparator. As long as OTP exceeds the reference voltage, the N-channel BATT-to-LX switch is forced off.
11	11	CS	Low-Side Current-Sense Input. The current-mode regulator terminates the switch cycle when the voltage at CS exceeds REF - CC.
12	12	VL	Output of the Internal Linear Regulator. VL can be overdriven by a voltage greater than 4.75V to operate the chip from +5V ± 5%, and to conserve power. Bypass with 0.1µF to GND.
13	13	GND	System Ground
14	14	BST	Power Input to the High-Side Gate Driver, which switches the internal N-channel MOSFET on and off.
15	15	LX	Ground Connection for the Internal High-Side Gate Driver; source-connection point for the internal N-channel MOSFET
16	16	BATT	4.5V to 25V Battery-Voltage Input Point. Connects to the internal N-channel power MOSFET's drain, and to the input of the internal linear regulator that powers the chip.

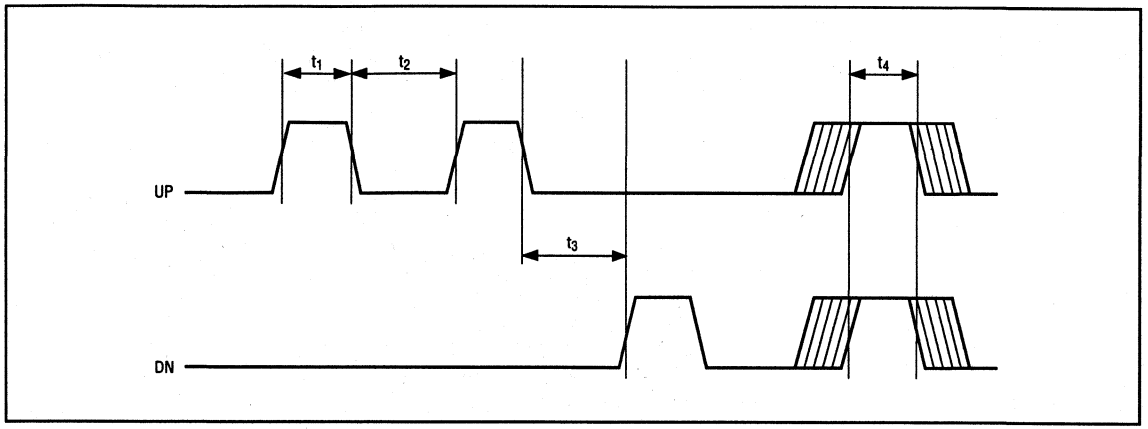


Figure 1. MAX1610 UP and DN Signal Timing

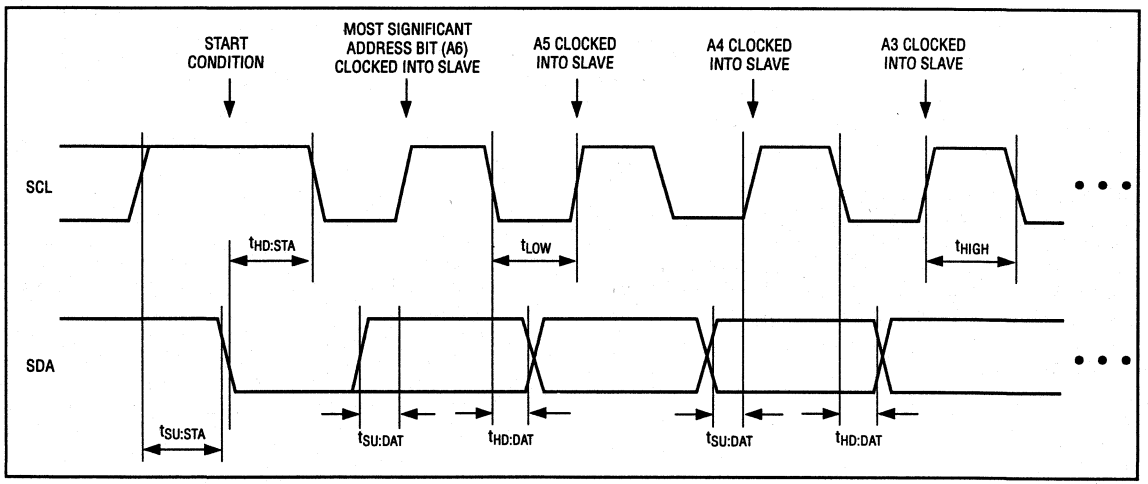


Figure 2. MAX1611 SMB Serial-Interface Timing—Address

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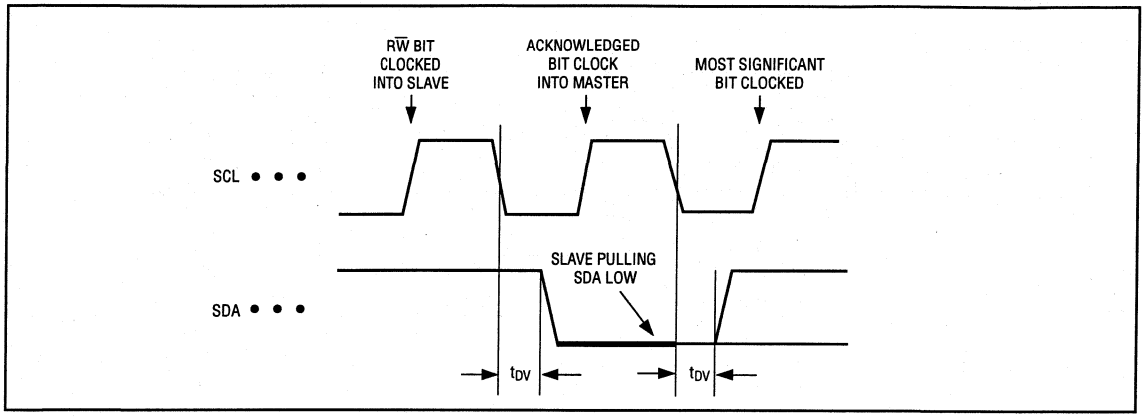


Figure 3. MAX1611 SMB Serial-Interface Timing—Acknowledge

Detailed Description

Getting Started

A cold-cathode fluorescent lamp (CCFL) has two terminals. For the CCFL to emit light, the two lamp terminals must be driven with a high-voltage (approximately 550V AC RMS) and high-frequency (approximately 45kHz) sine wave. The MAX1610/MAX1611 use a varying DC input voltage to create this high-voltage, high-frequency sine-wave drive. To select the correct component values for the MAX1610/MAX1611 circuit, several CCFL parameters and the minimum DC input voltage must be specified; these are listed in Table 1.

Table 3 shows the recommended component values to use with the circuit of Figure 4, depending on the particular CCFL parameters. The C2 values in Table 3 have been selected such that the normal operating voltage on the secondary of T1 is as close as possible to the CCFL strike voltage (where the strike voltage (V_S) is assumed to be approximately 1.8 times the CCFL operating voltage (V_L)).

Components T1, C1, R2, Q1, and Q2 form a Royer oscillator. A Royer oscillator is a resonant tank circuit that oscillates at a frequency dependent on C1, the primary magnetizing inductance of T1 (L_P), and the impedance seen by the T1 secondary. The MAX1610/MAX1611 regulate the current fed into the Royer oscillator by sensing the voltage on R1. For a given current through the Royer oscillator (I_{R1}), the power delivered to the CCFL depends on the Royer oscillator frequency. The R1 values in Table 3 have been selected to ensure that the power into the CCFL does not exceed its maximum rating, despite T1, C1, and C2 component-value variations. The Royer oscillator waveforms for the circuit of Figure 4 are shown in Figures 5 and 6.

Analog Circuitry

The MAX1610/MAX1611 maintain fixed CCFL brightness with varying input voltages on BATT by regulating the current fed into the Royer oscillator. This current is sensed via resistor R1 between CSAV and GND. An internal switch from BATT-to-LX pulse-width modulates at a fixed frequency to servo the CSAV pin to its regulation voltage. The CSAV regulation voltage can be adjusted via the digital interface to set CCFL brightness. The MAX1610 and MAX1611 differ only in the digital interface they use to adjust the internal 5-bit digital-to-analog converter (DAC) that sets the CSAV regulation voltage. The minimum-scale (min-scale) CSAV regulation voltage is resistor adjustable using the MINDAC pin, setting the minimum CCFL brightness. The D/A setting at MAX1610/MAX1611 power-up is preset to mid-scale (10000 binary) (Figure 7).

MINDAC Sets the Minimum Scale

The MINDAC pin sets the lowest CCFL brightness level. The voltage at MINDAC is divided by eight, and sets the minimum CSAV regulation voltage. For example, in the circuit of Figure 4, R5 (150kΩ) and R6 (51kΩ) form a resistor divider from REF, which sets MINDAC to 507mV (REF = 2.0V). This sets a minimum CSAV regulation voltage of 63mV with a full-scale CSAV regulation voltage of 247mV.

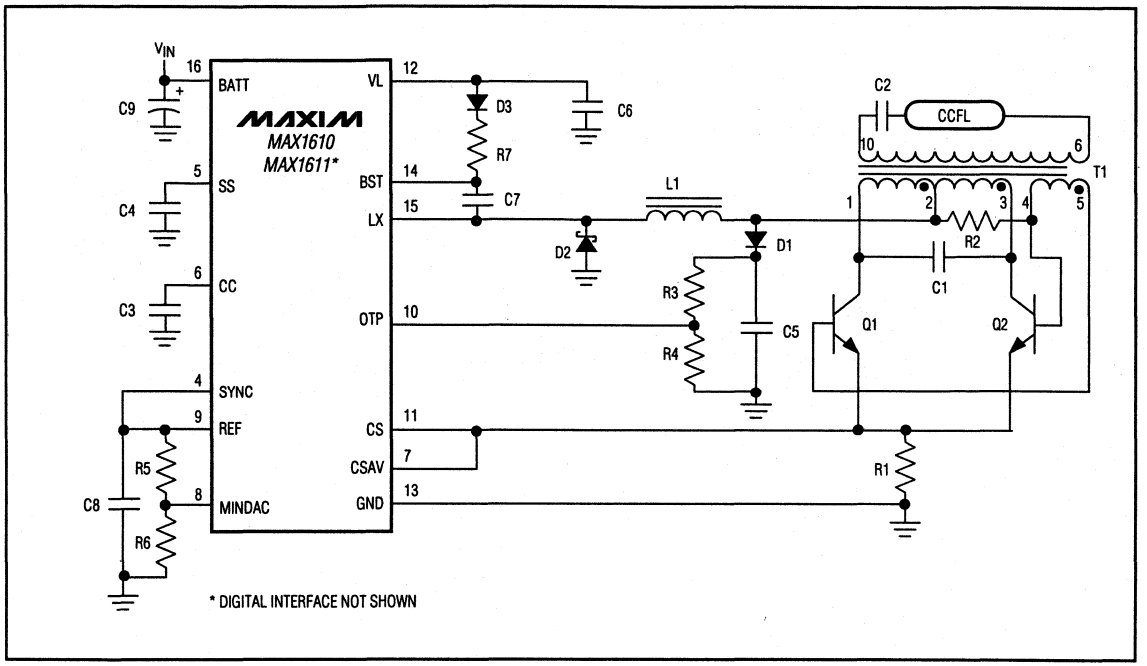


Figure 4. Typical Floating-Lamp Application Circuit

Table 1. Necessary CCFL Specifications

SPECIFICATION	UNITS	SYMBOL	DESCRIPTION
CCFL Minimum Strike Voltage ("Kick-Off Voltage")	V_{RMS}	V_S	Although CCFLs typically operate at $550V_{RMS}$, a higher voltage is required initially to light up the tube.
CCFL Typical Operating Voltage ("Lamp Voltage")	V_{RMS}	V_L	Once a CCFL has been struck, the voltage required to maintain light output falls to approximately $550V_{RMS}$. Small tubes may operate on as little as $250V_{RMS}$. The operating voltage of the CCFL stays relatively constant, even as the tube's brightness is varied.
CCFL Maximum Operating Current ("Lamp Current")	mA_{RMS}	I_L	The maximum root-mean-square AC current through a CCFL is almost always $5mA_{RMS}$. No DC current is allowed through any CCFL.
CCFL Maximum Frequency ("Lamp Frequency")	kHz	f_L	The maximum AC-lamp-current frequency.
DC Power Source Minimum Input Voltage	V	V_{MIN}	The minimum DC input voltage to the MAX1610/MAX1611 circuit determines the turns ratio required for the DC-AC conversion transformer. Decreasing the minimum input voltage increases the size of the transformer required for a given output power.

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Table 2. Typical Application Circuit Component Values

a) Resistors

SYMBOL	VALUE	TOLERANCE	POWER RATING
R1	(Note)	±1%	1/8W
R2	510Ω	±10%	1/8W
R3	51kΩ	±5%	1/16W
R4	8.2kΩ	±5%	1/16W
R5	150kΩ	±5%	1/16W
R6	51kΩ	±5%	1/16W
R7	20Ω	±10%	1/16W

b) Capacitors

SYMBOL	VALUE	TOLERANCE	WORKING VOLTAGE	NOTES
C1	0.1µF	±20%	±25V	δF ≤ 0.001 @ 1kHz
C2	(Note 1) (pF)	±10%	±3kV	High voltage
C3, C5	27nF	±20%	25V	
C4, C6, C7, C8	0.1µF	-20%	25V	Ceramic, larger values acceptable
C9	10µF	-50%	35V	Tantalum, low ESR

c) Other Components

SYMBOL	DESCRIPTION	GENERIC PART	SURFACE-MOUNT PART	MANUFACTURER
Q1, Q2	1A NPN switching transistor, $V_{CEO} \geq 50V$	2N2222A	FMMT619, SOT23	Zetex
D1, D3	50mA silicon diode, $V_{BR} \geq 40V$	1N4148	CMPD4448, SOT23	Central
D2	1A Schottky diode, $V_{BR} \geq 30V$	1N5818	EC10QS04	Nihon
L1	100µH, 1A inductor		CDR125-101	Sumida
T1	6W Royer oscillator transformer, turns ratio 67:1, secondary (pins 10 and 6) : primary (pins 1 and 3), primary magnetizing inductance (L_P) of 44µH ±20%		CTX110605	Coiltronics

Note: Component values depend on lamp characteristics. See Table 3 to select values.

Table 3. Selecting Circuit Values for Figure 4

V_L (V_{RMS})	I_L (mA_{RMS})	C2	R1	VCT (V_{MAX})	f_{ROY} (kHz)		
					MIN	TYP	MAX
250	3	22pF	1.21Ω	3.63V	50.3	58.6	71.8
250	5	43pF	0.715Ω	3.61V	43.3	49.7	60.3
300	3	18pF	1.18Ω	4.30V	52.1	61.0	75.1
300	5	36pF	0.681Ω	4.14V	45.6	52.8	64.7
450	5	20pF	0.732Ω	6.55V	51.1	59.7	73.3
500	5	18pF	0.715Ω	7.17V	52.1	61.0	75.1
550	5	18pF	0.665Ω	7.29V	52.5	61.8	76.7
600	5	15pF	0.698Ω	8.41V	53.6	63.1	78.1

Note: f_{ROY} = Royer oscillator damped resonant oscillation frequency. T1 primary magnetizing inductance (L_P) = 44µH ±20%.
VCT = average voltage from the T1 center tap to the emitters of Q1 and Q2 (ignoring Q1, Q2 $V_{CE,SAT}$).
C1 = 0.1µF ± 20%; C2 = ±10% tolerance; R1 = ±1% tolerance.

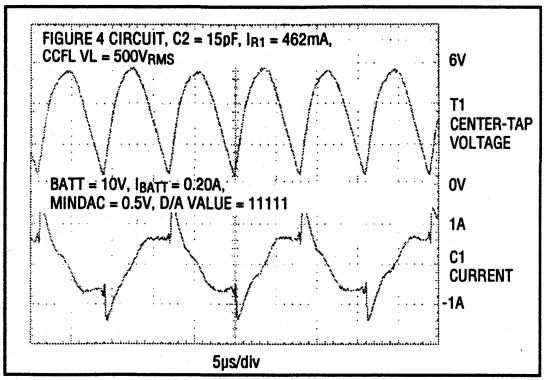


Figure 5. Royer Oscillator Typical Operating Waveforms for Circuit of Figure 4

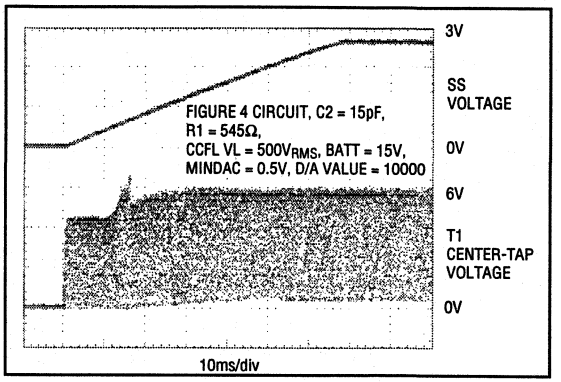


Figure 6. Start-Up Waveforms for Circuit of Figure 4

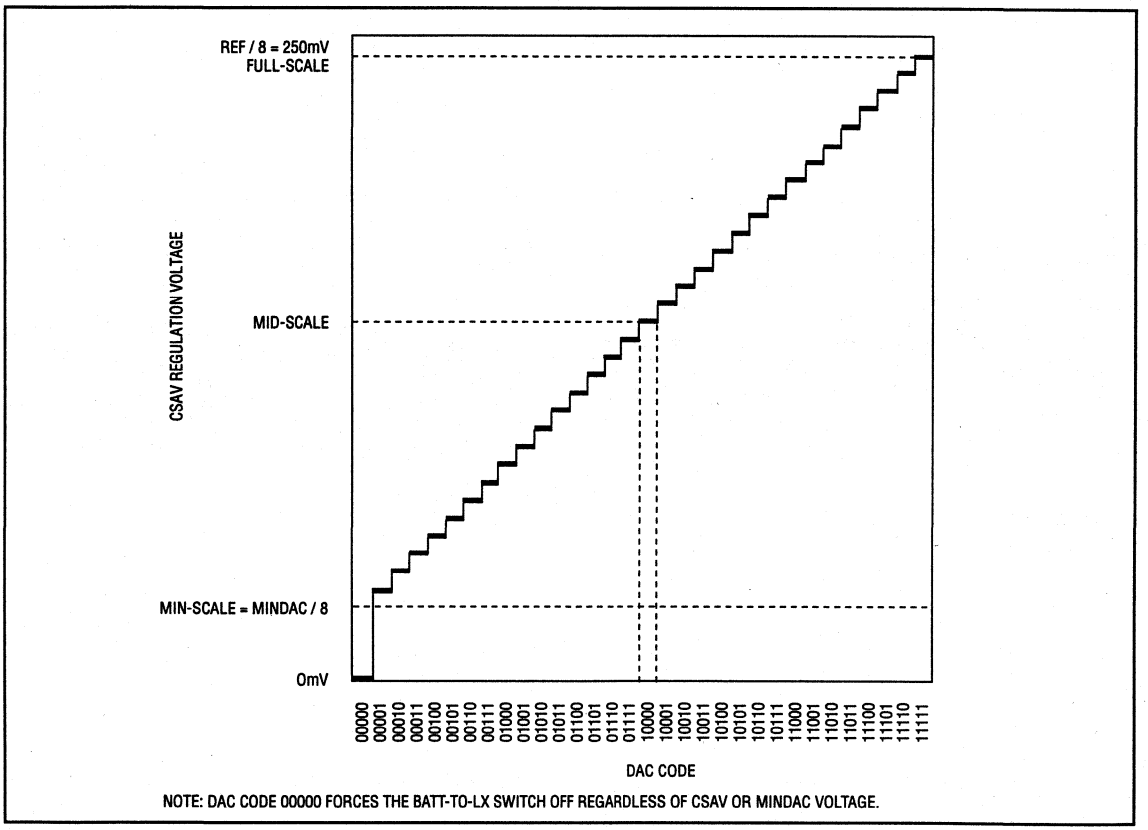


Figure 7. CSAV Regulation Voltage Range

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Open-Tube Protection (OTP)

Any real transformer used in a Royer oscillator will have a maximum-allowed secondary voltage. If the maximum-allowed secondary voltage is exceeded, the winding insulation can break down, leading to permanent transformer damage. The maximum-allowed secondary voltage can be exceeded either when the CCFL drive circuit is turned on without the CCFL being in place, or when the CCFL becomes disconnected during normal operation due to a mechanical failure. To protect against these fault conditions, use the OTP pin to sense the voltage on the transformer center tap (pin 2 of Figure 4). Whenever the voltage on OTP exceeds the REF reference voltage, the BATT-to-LX power switch is forced off.

For example, in Figure 4, the CTX110605 transformer has a maximum-allowed continuous secondary voltage of $1340V_{RMS}$. D1 and C5 detect the peak voltage on the center tap of T1. R3 and R4 determine the limit on the center tap peak voltage. The relationship between the voltage on the center tap of T1 and the secondary voltage is diagrammed in Figure 8. Neglecting the Q1/Q2 saturation voltage and the voltage on the R1 current-sense resistor yields Equation 1:

$$V_{CTPK} = \frac{V_{SEC}\sqrt{2}}{2N}$$

where V_{SEC} is the maximum root-mean-square voltage allowed on the secondary, N is the secondary-to-primary turns ratio, and V_{CTPK} is the peak voltage on the transformer center tap.

Block Diagram of the Analog Section

Figure 9 shows a functional diagram of the analog circuitry in the MAX1610/MAX1611. The chips have identical analog circuitry, and differ only in their digital interface.

Loop-Compensation Capacitor (CC)

The BATT-to-LX switch turns on at fixed frequency, and turns off when the current-sense voltage on the CS pin exceeds CC - REF. As the CC pin voltage rises, the CS current limit rises as well. A transconductance amplifier compares the voltage on CSAV to the desired regulation voltage and outputs a current proportional to this error to the CC pin. A capacitor from CC to GND sets the bandwidth of this regulation loop, as shown in Equation 2:

$$BW = \frac{85}{2\pi C3}$$

where BW is the bandwidth of the CSAV regulation loop in kHz, and C3 is the capacitance from CC to GND in nF.

Soft Start (SS)

Soft start prevents the triggering of OTP upon power-up. Placing a capacitor from SS to GND soft starts the Royer oscillator by slowly raising the CS current-limit voltage. Internal circuitry pulls SS to GND during power-on reset, or whenever the lamp is turned off (DAC = 00000, shutdown mode, ON-1 = 0, or ON-0 = 0) (Figures 10 and 11). When SS is not pulled to GND, an internal 4µA current sources into the capacitor at the SS pin. This pin is internally diode clamped to REF so that it rises to a maximum voltage of about 2.7V. Regardless of the voltage on CC, the CS current-sense voltage is never allowed to exceed the voltage on SS divided by 5.

Frequency Selection and Synchronization

The SYNC pin performs two functions: it sets the BATT-to-LX switching frequency, and it allows the BATT-to-LX switching frequency to be synchronized to an external oscillator. SYNC tied to GND or VL sets a 145kHz switching frequency; SYNC tied to REF sets a 290kHz

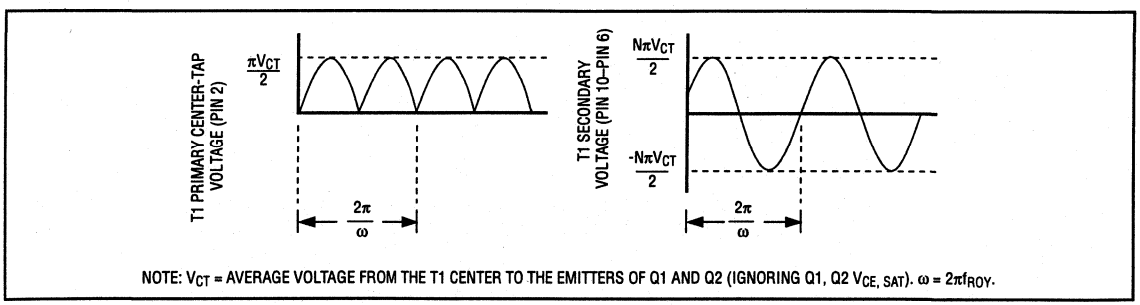
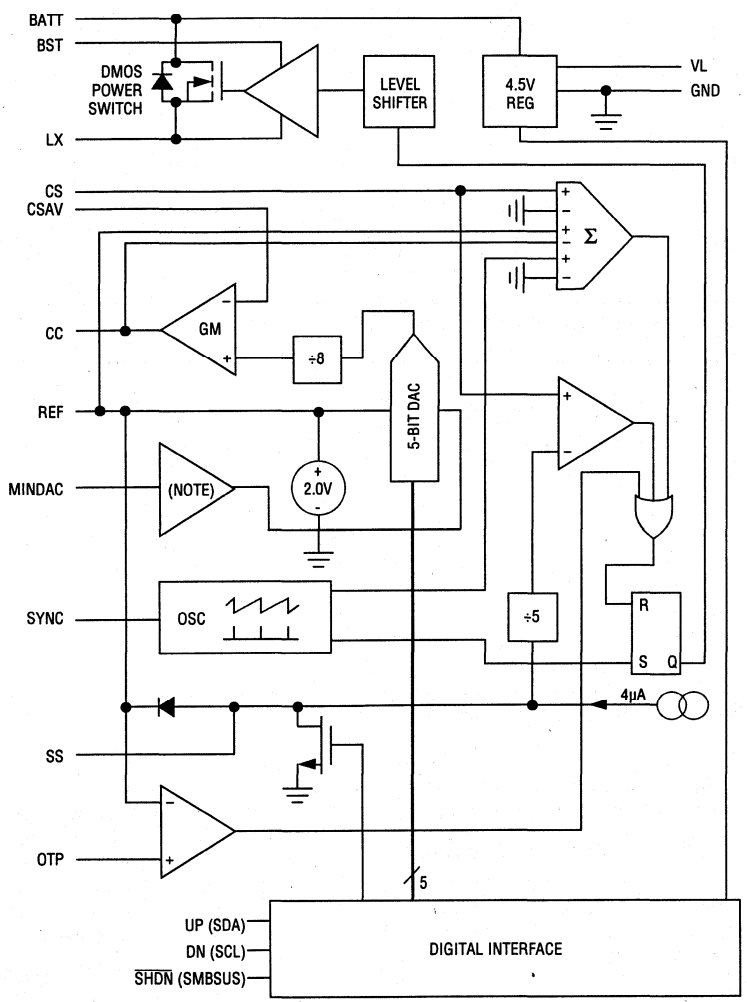


Figure 8. Transformer Primary/Secondary Voltage Relationship



( ) ARE FOR MAX1611

NOTE: CIRCUITRY TO DETECT MINDAC = VL NOT SHOWN. SEE *CHOPPING THE LAMP CURRENT* SECTION.

Figure 9. Functional Diagram

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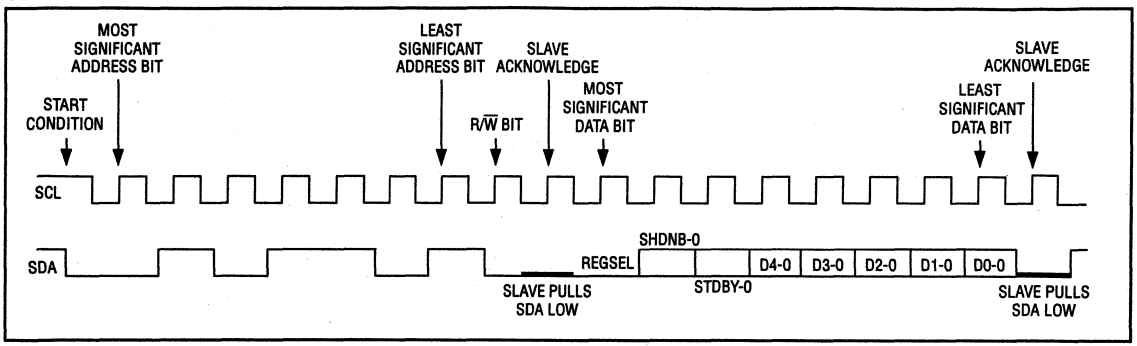


Figure 10. MAX1611 Serial-Interface Single-Byte Write Example (REGSEL = 0)

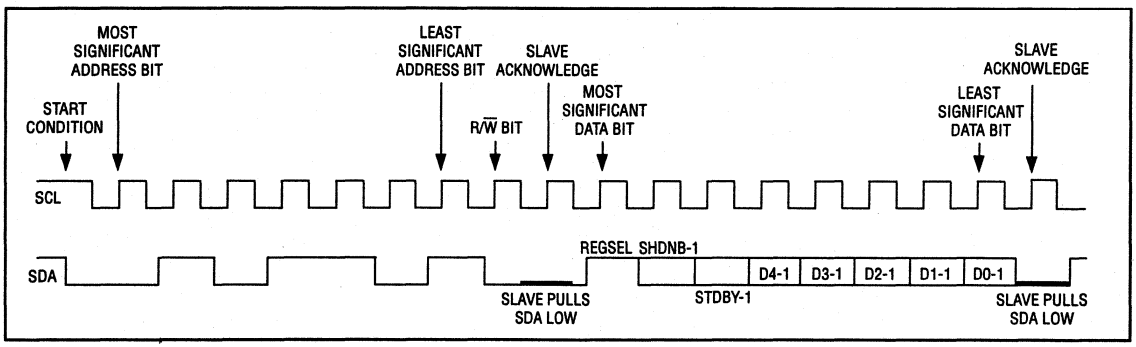


Figure 11. MAX1611 Serial-Interface Single-Byte Write Example (REGSEL = 1)

switching frequency. Any rising edge on SYNC restarts a BATT-to-LX switch cycle by forcing the switch on.

MAX1610 Digital Interface

The MAX1610 contains an internal 5-bit up/down counter that sets the value of the internal 5-bit DAC. At power-on, or when both the UP and DN pins are held high simultaneously, the 5-bit up/down counter is preset to 10000 binary, which corresponds to mid-scale. A rising edge on UP increments the 5-bit up/down counter. A rising edge on DN decrements the 5-bit up/down counter. The counter will not roll over on either underflow or overflow. For example, if the CCFL is at maximum intensity level, rising edges on UP will not change the output.

The $\overline{SHDN}$ pin provides a way to lower the MAX1610 supply current to 10µA without resetting the 5-bit up/down counter. With $\overline{SHDN}$ = 1, the MAX1610 operates normally with VL at 4.5V. When the BATT-to-LX power switch operates, an additional 3mA of current (other than the supply current) is consumed through the BST pin, requiring VL to source at least 4.5mA of current. With $\overline{SHDN}$ = 0, all analog circuitry turns off, except for a coarse regulator that can source up to 500µA from VL. The coarse regulator preserves the state of the internal logic and keeps the digital interface active during shutdown ($\overline{SHDN}$ = 0).

MAX1611 Digital Interface

A single byte of data written over the Intel System Management Bus (SMBus™) controls the MAX1611. Figures 10 and 11 show example single-byte writes. The MAX1611 contains two 7-bit latches for storing configuration data. Only one of the 7-bit latches is active at a time. The MAX1611 responds only to its own address, 0101101 binary. The SMBSUS pin selects which of the two sets of configuration data is used. Figure 12 shows a schematic diagram of the MAX1611's digital circuitry. Notice that the SMBSUS pin selects which one of the

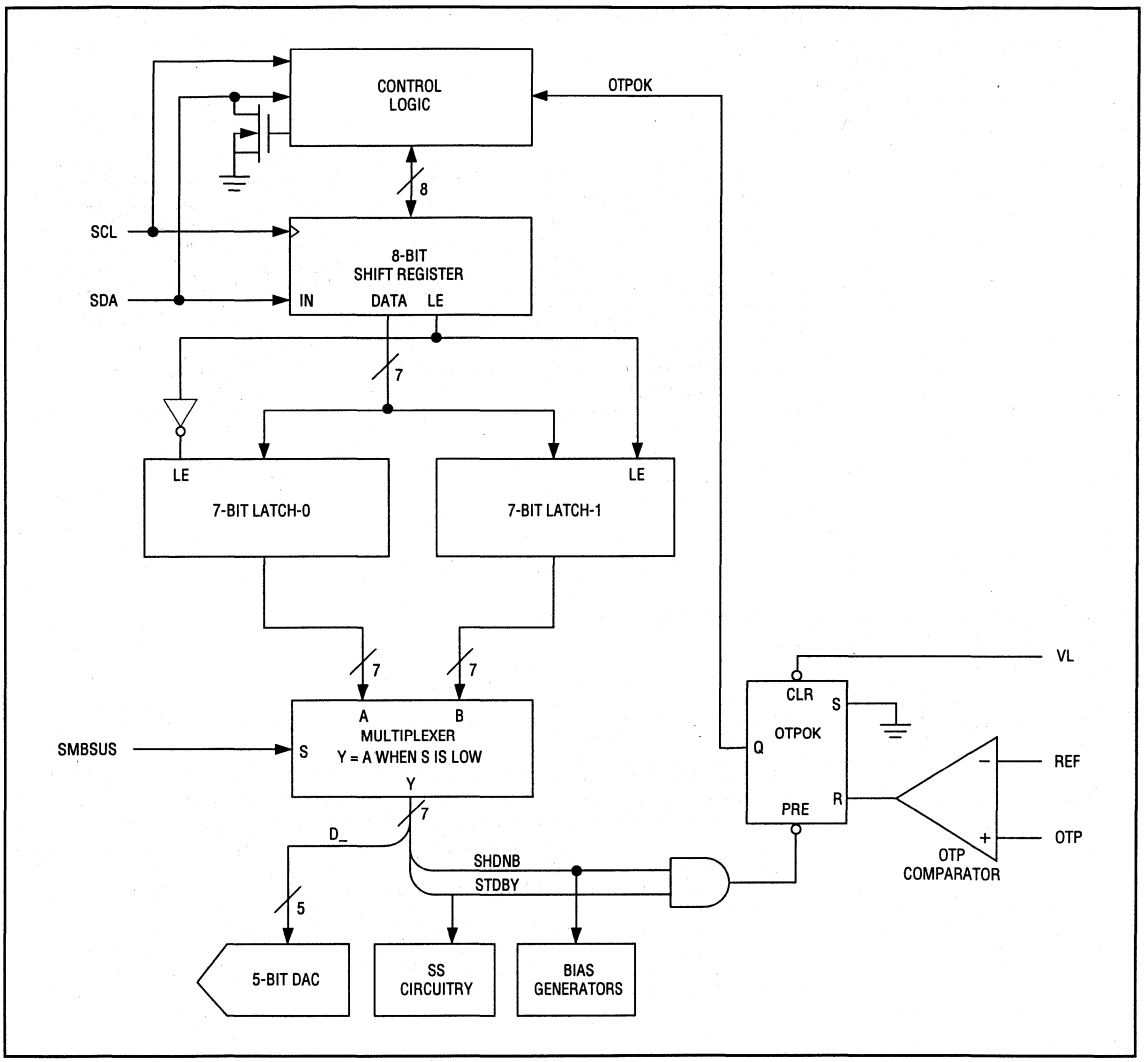


Figure 12. MAX1611 Serial-Interface Circuitry Block Diagram

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Table 4. MAX1611 Configuration Byte with REGSEL = 0

BIT	NAME	POR STATE*	DESCRIPTION
7	REGSEL	—	Register Select. A zero in this bit writes the remaining seven bits into the 7-bit latch-0 (Figure 13).
6	SHDNB-0	0	Complete Shutdown. Pulling SMBSUS low with SHDNB-0 = 0 places the MAX1611 into a low-quiescent-current shutdown mode, with the reference off and the VL linear-regulator output switched to a low-current, coarse regulation mode. Pulling SMBSUS low with SHDNB-0 = 1 puts the MAX1611 into its normal operational mode, with the reference and internal VL linear regulator fully on. SHDNB-0 supersedes STDBY-0. As long as SHDNB-0 = 0 and SMBSUS = 0, it doesn't matter what STDBY-0 is; the MAX1611 still shuts down.
5	STDBY-0	0	Standby, disables CCFL supply only. As long as SMBSUS stays low and STDBY-0 = 0, the internal power switch is kept off and SS is held shorted to GND; neither the internal reference nor the linear regulator is affected. With STDBY = 1 and SMBSUS low, the MAX1611 operates normally.
4 3 2 1 0	D4-0 D3-0 D2-0 D1-0 D0-0	1 0 0 0 0	DAC Input Data. With the SMBSUS pin low, bits D4-0 through D0-0 set the DAC.

** Initial register state after power-up.*

Table 5. MAX1611 Configuration Byte with REGSEL = 1

BIT	NAME	POR STATE*	DESCRIPTION
7	REGSEL	—	Register Select. A one in this bit writes the remaining seven bits into the 7-bit latch-1 (Figure 13).
6	SHDNB-1	1	Complete Shutdown. Pulling SMBSUS high with SHDNB-1 = 0 places the MAX1611 into a low-quiescent-current shutdown mode, with the reference off and the VL linear regulator output switched to a low-current coarse regulation mode. Pulling SMBSUS high with SHDNB-1 = 1 puts the MAX1611 into its normal operational mode, with the reference and internal VL linear regulator fully on. SHDNB-1 supersedes STDBY-1. As long as SHDNB-1 = 0 and SMBSUS = 0, it doesn't matter what STDBY-1 is; the MAX1611 still shuts down.
5	STDBY-1	1	Standby, disables CCFL supply only. As long as SMBSUS stays high and STDBY-1 = 0, the internal power switch is kept off and SS is held shorted to GND; neither the internal reference nor the linear regulator is affected. With STDBY-1 = 1 and SMBSUS high, the MAX1611 operates normally.
4 3 2 1 0	D4-1 D3-1 D2-1 D1-1 D0-1	1 0 0 0 0	DAC Input Data. With the SMBSUS pin high, bits D4-1 through D0-1 set the DAC.

** Initial register state after power-up.*

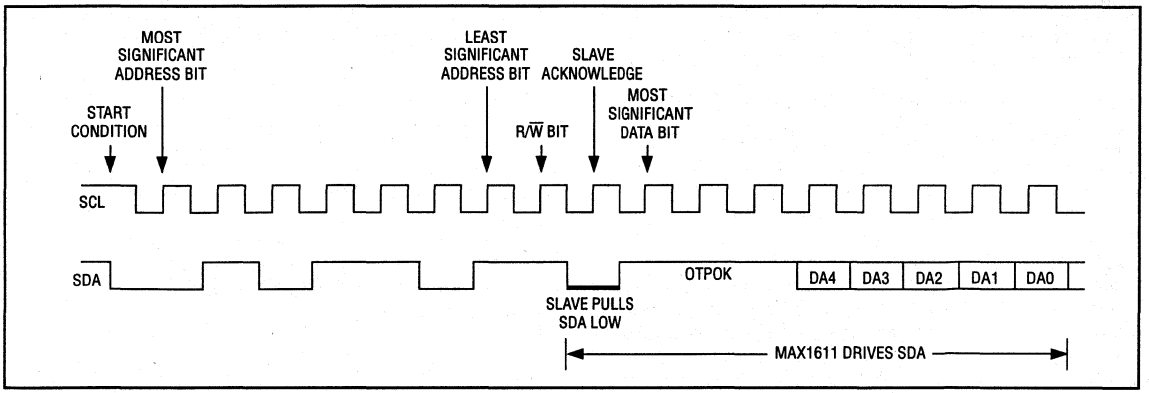


Figure 13. MAX1611 Serial-Interface Read Example

Table 6. MAX1611 Status Bits

BIT	NAME	POR STATE*	FUNCTION
7	OTPOK	1	Latched Open-Tube Detection. OTPOK = 0 indicates that open-tube detection has been triggered. As soon as the voltage on the OTP pin exceeds REF, the OTPOK bit is cleared. Reset the OTPOK pin by entering shutdown or standby.
6 5	— —	— —	Unused. These bits always return a logic one.
4 3 2 1 0	DA4 DA3 DA2 DA1 DA0		Displays the DAC setting selected by SMBSUS.

** Initial register state after power-up.*

two 7-bit registers is used. Tables 4 and 5 describe the data format for the configuration data.

Status information can be read from the MAX1611 using the SMBus read-byte protocol. Figure 13 shows an example status read. Table 6 describes the status information data format.

During shutdown (SMBSUS = 0 and SHDNB-0 = 0, or SMBSUS = 1 and SHDNB-1 = 0), the MAX1611 serial interface remains fully functional and can be used to set either the SHDNB-0 or SHDNB-1 bits in order to return the MAX1611 to its normal operational state.

Chopping the Lamp Current

Chopping the lamp current allows lower sustainable light levels without lamp flicker. Intensity is varied by controlling the on-time duty cycle. Tying MINDAC to VL activates a special mode, which allows the CCFL intensity to be varied by turning the lamp on and off at a frequency faster than the eye can detect. The SS pin pulls to GND during off time and rises to 2.7V during on time. During on time, the CSAV pin regulates to REF / 8 (250mV). During off time, the BATT-to-LX power switch is forced off and the CC compensation node goes high impedance. Omit R5, R6, and C4 of the circuit in Figure 4.

In this mode, leave SS floating and increase the CC capacitance to 0.1µF. Also, insert a 330Ω resistor in series with D1 (Figure 4) to prevent the open-lamp detection circuit from being tripped by the repeated striking of the lamp. The SS pin will oscillate at the switching frequency divided by 1024 (283Hz with SYNC = REF). The intensity can be varied with the duty cycle at the SS pin. The duty cycle is set by the DAC in 3% increments. Duty cycle will vary with intensity. Full-scale yields a 100% duty cycle. DAC codes 00001, 00010, and 00011 all yield the

Digitally Controlled CCFL Backlight Power Supplies

minimum 9% duty cycle. DAC code 00000 shuts off the lamp entirely (0% duty cycle). Figure 14 shows the chopped waveforms with the DAC set to mid-scale.

Applications Information

Directly Regulating the Lamp Current

The MAX1610/MAX1611 can directly regulate the CCFL current by tapping into the secondary of T1 (Figure 15). This allows more precise setting of the maximum lamp current (I_L). The disadvantage of this approach is that the secondary-to-ground voltage is twice that shown in Figure 4, increasing the likelihood of the thermometer effect, where one end of the lamp is brighter than the other. Figure 15 uses the same component values as Figure 4, except for R1, R40, D40, and D41. D40 and D41 are the same type of diode as D1. R1 should be 0.68Ω ±10% to set a peak current limit of about 735mA. Use a 107Ω ±1% resistor for R40 to set a lamp current of $5mA_{RMS}$. This circuit accepts a wide range of lamp types without component adjustments.

Component Suppliers

Table 7 lists three different sources for C1. C1 requires a low dissipation factor to prevent overheating as energy is cycled between C1 and the T1 magnetizing inductance in the Royer resonant tank. Table 8 lists suppliers for the high-voltage ballast capacitor, C2.

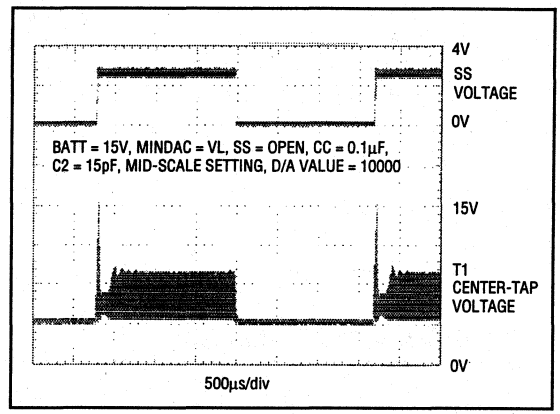


Figure 14. Chopped Waveforms

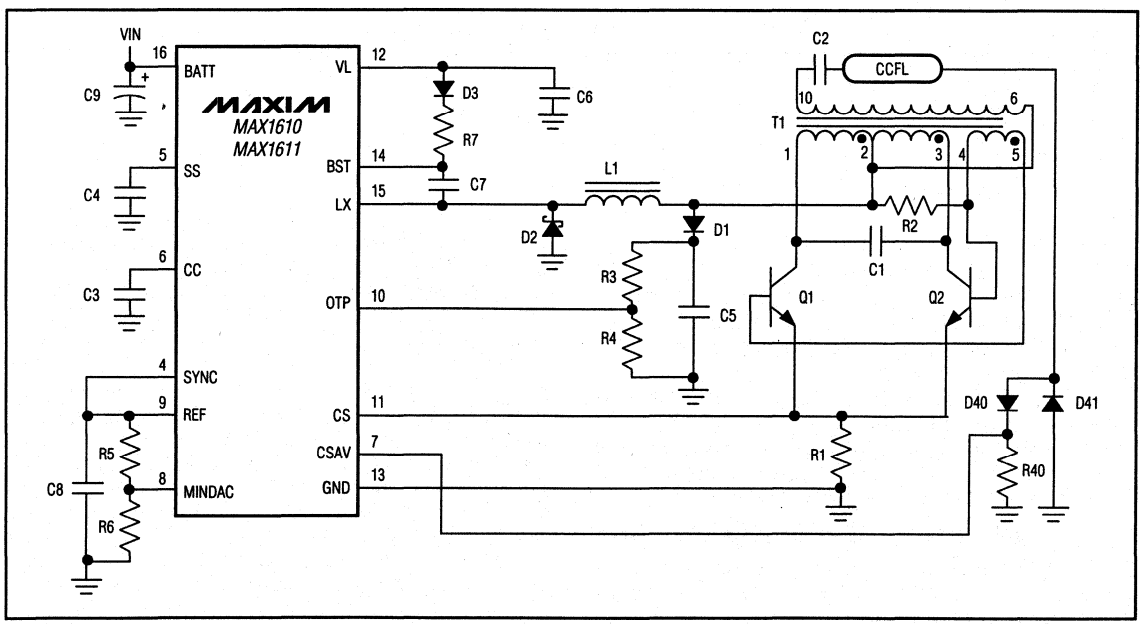


Figure 15. Directly Regulating the CCFL Current

Table 7. Capacitor C1 Supplier Information

PART	SUPPLIER	LOCATION	PHONE	FAX	NOTES/CONTACT
SMD7.3104	WIMA	Elmsford, NY	914-347-2474	914-347-7230	Dissipation factor (tan δ) at 1kHz and 20°C ≤ 0.008.
		Germany	(0621) 8785-0	(0621) 8710457158	
		Hong Kong	5-70-11-51	58-06-84-74	
CHEV0025J104	PACCOM Electronics	Redmond, WA	206-883-9200	206-881-6959	Dissipation factor (tan δ) at 1kHz ≤ 0.002.
4040N104M250	NOVACAP	Valencia, CA	805-295-5920	805-295-5928	Dissipation factor (tan δ) at 1kHz and 20°C ≤ 0.0015.

Table 8. Capacitor C2 Supplier Information

PART	SUPPLIER	LOCATION	PHONE	FAX
1808HA330KATMA	AVX/Kyocera	Olean, NY	716-372-6611	716-372-6316
		Vancouver, WA	206-696-2840	206-695-5836
		Germany	08131 9004-0	08131 9004-44
		Hong Kong	852-363-3303	852-765-8185
GHM1040SL330J3K	Murata	Smyrna, GA	404-436-1300	404-436-3030
		Germany	49-911-66870	49-911-6687193
		Taiwan	886-2-562-4218	886-2-536-6721
302C1812A330K	Metuchen Capacitors, Inc.	Old Bridge, NJ	908-679-3366	908-679-3222
302R29N330K	Johanson Dielectrics	Sylmar, CA	818-364-9800	818-364-6100

Chip Information

TRANSISTOR COUNT : 5457

ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
10/96

MAXIM

Digitally Adjustable LCD Bias Supply

General Description

The MAX1620/MAX1621 convert a 4V to 12V battery voltage to a positive or negative LCD backplane bias voltage. Backplane bias voltage is automatically disabled when the display logic voltage is removed, protecting the display. These devices use very little PC board area; they come in an ultra-small QSOP package and require only small, low-profile external components.

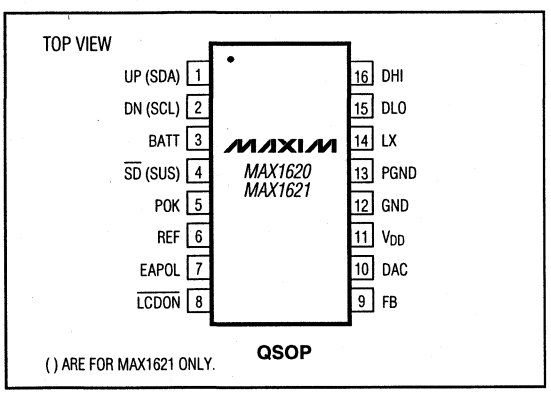
The output voltage can be preset to the desired positive or negative voltage range with external resistors, and adjusted over that range with the on-board DAC or with a potentiometer. The MAX1620/MAX1621 include a 5-bit DAC, allowing digital software control of the bias voltage. The MAX1620 uses up/down digital signaling to adjust the DAC, and the MAX1621 uses the System Management Bus (SMBus™) two-wire serial interface.

These devices use low-cost, external N-channel or NPN power switches, and can be configured for positive or negative output voltages. Operating power is a low 250µA, provided from the display logic supply of 3.0V to 5.5V. The MAX1620/MAX1621 are available in a 16-pin QSOP package.

Applications

Notebook Computers
Laptop Computers
Palmtop Computers
Personal Digital Assistants
Portable Data-Collection Terminals

Pin Configuration



SMBus is a trademark of Intel Corp.

Features

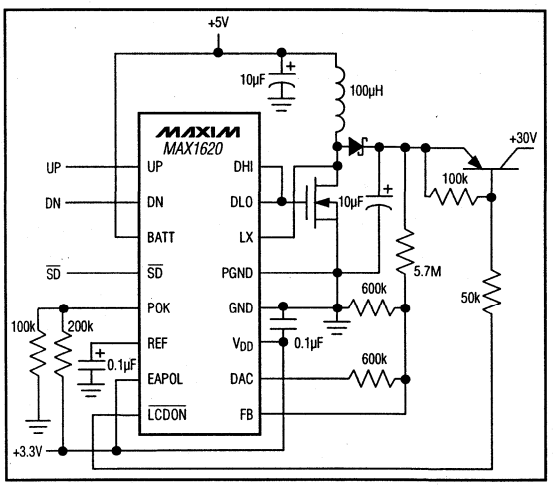
- ♦ **4V to 12V Battery Input Voltage**
- ♦ **Automatic Disable when Display Logic is Shut Down**
- ♦ **Extremely Small QSOP Package**
- ♦ **32-Level Internal DAC**
- ♦ **SMBus Serial Interface**
- ♦ **Positive or Negative Output Voltage**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1620CEE	0°C to +70°C	16 QSOP
MAX1620EEE	-40°C to +85°C	16 QSOP
MAX1621CEE	0°C to +70°C	16 QSOP
MAX1621EEE	-40°C to +85°C	16 QSOP

4

Typical Operating Circuit



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ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
11/96

MAXIM

High-Speed Step-Down Controllers with Synchronous Rectification for CPU Power

General Description

The MAX1624/MAX1625 are ultra-high-performance, step-down DC-DC controllers for CPU power in high-end computer systems. Designed for demanding applications where output voltage precision and good transient response are critical for proper operation (such as Intel's Pentium Pro CPU power modules), they deliver over 100W between 1.1V and 3.5V, with 1.5% initial accuracy from a +5V ±10% supply. Excellent dynamic response corrects output transients caused by the latest dynamic clocked CPUs. These controllers achieve over 90% efficiency using synchronous rectification. Unique bootstrap circuitry drives inexpensive external N-channel MOSFETs.

The switching frequency is resistor-programmable from 100kHz to 1MHz. This high switching frequency allows the use of a small surface-mount inductor and reduces output filter capacitor requirements, saving overall board area and system cost.

The MAX1624 is available in a 24-pin SSOP package and offers additional features such as a digitally programmable output (in 100mV increments), adjustable transient response, selectable 0.5%, 1%, or 2% load regulation, and gate drive for an optional load-side MOSFET half-H bridge used to correct load transients. The MAX1625 comes in a 16-pin narrow SO package. Other features in both controllers include internal digital soft-start, a power-good output, and a 3.5V ±2% reference output.

Applications

Pentium Pro®, PowerPC®, and DEC Alpha Systems

Desktop Computers

LAN Servers

Industrial Computers

GTL Bus Termination

Pentium Pro is a registered trademark of Intel Corp.
PowerPC is a registered trademark of IBM Corp.
GlitchCatcher is a trademark of Maxim Integrated Products.
** Patent pending*

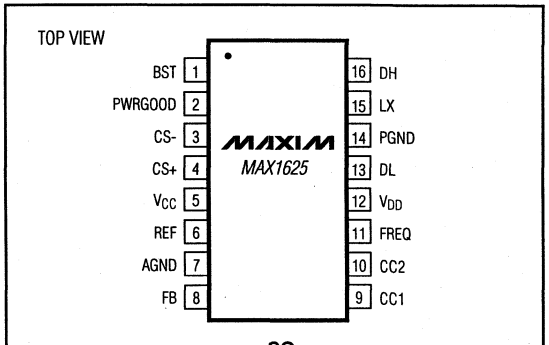
Features

- ♦ **Better than 1.5% Initial Output Accuracy**
- ♦ **Excellent Transient Response**
- ♦ **Resistor-Programmable Frequency from 100kHz to 1MHz**
- ♦ **Over 100W Output Power**
- ♦ **Digitally Programmable Output from 1.1V to 3.5V, in 100mV Increments (MAX1624)**
- ♦ **Adjustable Output (MAX1625)**
- ♦ **90% Efficiency**
- ♦ **Remote Output Voltage Sensing**
- ♦ **Adjustable Transient Response (MAX1624)**
- ♦ **GlitchCatcher™ Circuit for Excellent Load-Transient Response (MAX1624)**
- ♦ **Power-Good Output**
- ♦ **Current-Mode Feedback**
- ♦ **Digital Soft-Start**
- ♦ **Strong 2A Gate-Drive Outputs**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1624EAG	-40°C to +85°C	24 SSOP
MAX1625ESE	-40°C to +85°C	16 Narrow SO

Pin Configurations



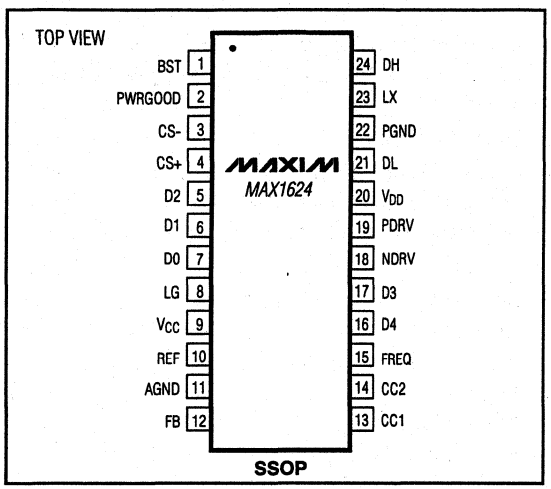
SO

MAX1624 appears on next page.

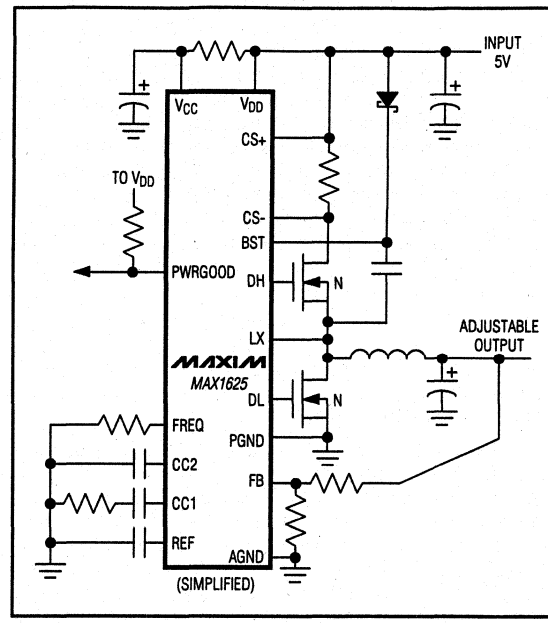
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High-Speed Step-Down Controllers with Synchronous Rectification for CPU Power

Pin Configurations (continued)



Typical Operating Circuit



19-1075; Rev 0; 6/96

EVALUATION KIT AVAILABLE

MAXIM

5V/3.3V or Adjustable, 100% Duty-Cycle, High-Efficiency, Step-Down DC-DC Controllers

General Description

The MAX1626/MAX1627 step-down DC-DC switching controllers provide high efficiency over loads ranging from 1mA to more than 2A. A unique current-limited, pulse-frequency-modulated (PFM) control scheme operates with up to a 100% duty cycle, resulting in very low dropout voltages. This control scheme eliminates minimum load requirements and reduces the supply current under light loads to 90µA (versus 2mA to 10mA for common pulse-width modulation controllers).

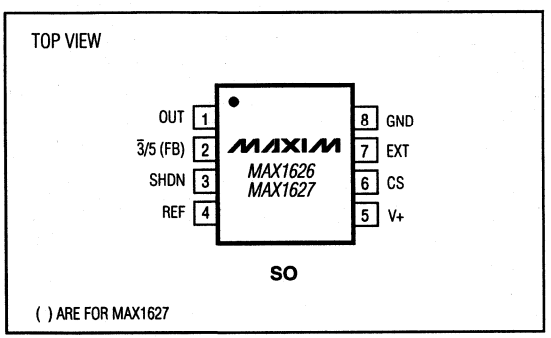
These step-down controllers drive an external P-channel MOSFET, allowing design flexibility for applications to 12W or higher. Soft-start reduces current surges during start-up. A high switching frequency (up to 300kHz) and operation in continuous-conduction mode allow the use of tiny surface-mount inductors. Output capacitor requirements are also reduced, minimizing PC board area and system costs.

The output voltage is preset at 5V or 3.3V for the MAX1626 and adjustable for the MAX1627. Input voltages can be up to 16.5V. The MAX1626/MAX1627 are functional upgrades for the MAX1649/MAX1651.

Applications

PCMCIA Power Supplies
Personal Digital Assistants
Hand-Held Computers
Portable Terminals
Low-Cost Notebook Computer Supplies
5V to 3.3V Green PC Applications
High-Efficiency Step-Down Regulation
Minimum-Component DC-DC Converters
Battery-Powered Applications

Pin Configuration



Features

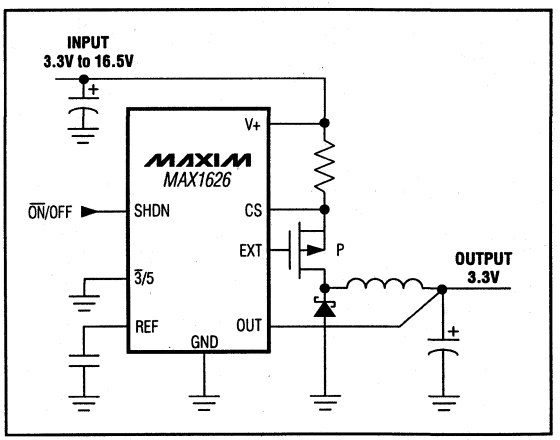
- ♦ Low Dropout Voltage
- ♦ 100% Maximum Duty Cycle
- ♦ Soft-Start Limits Start-Up Current
- ♦ Efficiency >90% (3mA to 2A Loads)
- ♦ Output Power >12.5W
- ♦ 90µA Max Quiescent Current
- ♦ 1µA Max Shutdown Current
- ♦ Up to 300kHz Switching Frequency
- ♦ 16.5V Max Input Voltage
- ♦ Output Voltage: 5V/3.3V (MAX1626)
  Adjustable (MAX1627)
- ♦ Current-Limited Control Scheme

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1626C/D	0°C to +70°C	Dice*
MAX1626ESA	-40°C to +85°C	8 SO
MAX1627C/D	0°C to +70°C	Dice*
MAX1627ESA	-40°C to +85°C	8 SO

** Dice are tested at T_A = +25°C.*

Typical Operating Circuit



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5V/3.3V or Adjustable, 100% Duty-Cycle, High-Efficiency, Step-Down DC-DC Controllers

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V+ to GND ..... -0.3V, +17V
OUT, FB, $\overline{3}/5$, SHDN, REF, CS, EXT to GND ... -0.3V, (V+ + 0.3V)
Maximum Current at REF (I_{REF}) 15mA
Maximum Current at EXT (I_{EXT}) 50mA
Continuous Power Dissipation (T_A = +70°C)
SO (derate 5.88mW/°C above +70°C) 471mW

Operating Temperature Range
MAX1626ESA/MAX1627ESA ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +3V to +16.5V, SHDN = $\overline{3}/5$ = 0V, T_A = 0°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V+		3.0		16.5	V
Supply Current into V+	I+	Operating, no load		70	90	µA
		V+ = SHDN = 16.5V (shutdown)			1	
Undervoltage Lockout				2.7	2.8	V
Output Voltage	V_{OUT}	Circuit of Figure 1, $\overline{3}/5$ = V+ (Note 1)	4.85	5.00	5.15	V
		Circuit of Figure 1, $\overline{3}/5$ = 0V (Note 1)	3.20	3.30	3.40	
OUT Input Current	I_{OUT}	MAX1626, $\overline{3}/5$ = V+, output forced to 5V	24	37	50	µA
FB Threshold Voltage		MAX1627, includes hysteresis	1.27	1.30	1.33	V
FB Leakage Current		MAX1627	0		35	nA
CS Input Current			0		10	µA
CS Threshold Voltage	V_{CS}		85	100	115	mV
SHDN Input Voltage High			1.6			V
SHDN Input Voltage Low					0.4	V
SHDN Input Current		SHDN = 0V or V+			±1	µA
$\overline{3}/5$ Input Voltage High			V+ - 0.5			V
$\overline{3}/5$ Input Voltage Low					0.5	V
$\overline{3}/5$ Leakage Current		$\overline{3}/5$ = 0V or V+			±1	µA
EXT Resistance		V+ = 5V		10		Ω
Minimum EXT Off Time		Output forced to 0V	8	10	12	µs
		Output in regulation	1.5	2.0	2.5	
EXT Duty-Cycle Limit			100			%
Line Regulation		6.0V < V+ < 12.0V, I_{LOAD} = 1A		5		mV/V
Load Regulation		30mA < I_{LOAD} < 2.0A, V+ = 8V		15		mV/A
Reference Voltage	V_{REF}	I_{LOAD} = 0µA	1.27	1.30	1.33	V
REF Load Regulation		0µA ≤ I_{REF} ≤ 100µA		4	10	mV
REF Line Regulation		V+ = 3V to 16.5V, I_{LOAD} = 0µA		10	100	µV/V

ELECTRICAL CHARACTERISTICS

(V+ = +3V to +16.5V, SHDN = $\overline{3}/5$ = 0V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

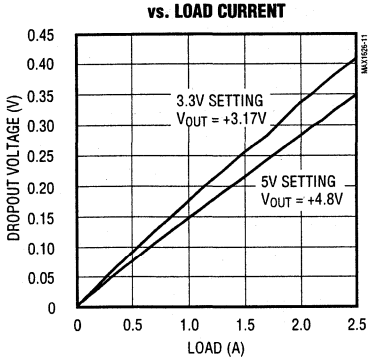
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage	V+		3.0		16.5	V
Supply Current into V+	I_{OUT}	Operating, no load			100	µA
		V+ = SHDN = 16.5V (shutdown)			2	
Undervoltage Lockout					2.9	V
Output Voltage	V_{OUT}	Circuit of Figure 1, $\overline{3}/5$ = V+	4.80		5.20	V
		Circuit of Figure 1, $\overline{3}/5$ = 0V	3.16		3.44	
OUT Input Current	I_{OUT}	MAX1626, $\overline{3}/5$ = V+, output forced to 5V	24		50	µA
FB Threshold Voltage		MAX1627, includes hysteresis	1.25		1.35	V
FB Leakage Current		MAX1627	0		50	nA
CS Threshold Voltage			80		120	mV
Reference		I_{LOAD} = 0µA	1.25		1.35	V

Note 1: V+ must exceed V_{OUT} to maintain regulation.
Note 2: Specifications from 0°C to -40°C are guaranteed by design, not production tested.

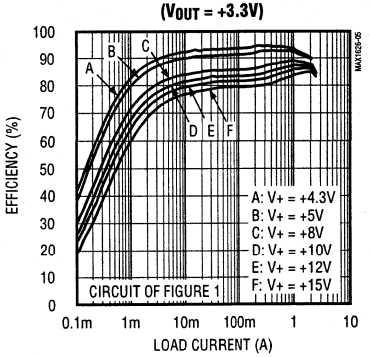
Typical Operating Characteristics

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

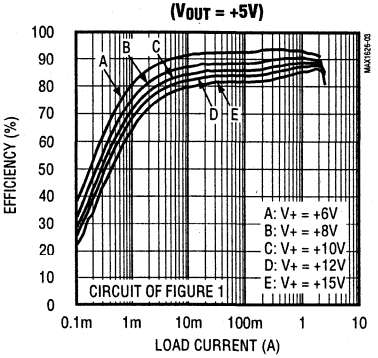
DROPOUT VOLTAGE vs. LOAD CURRENT



EFFICIENCY vs. LOAD CURRENT (V_{OUT} = +3.3V)



EFFICIENCY vs. LOAD CURRENT (V_{OUT} = +5V)

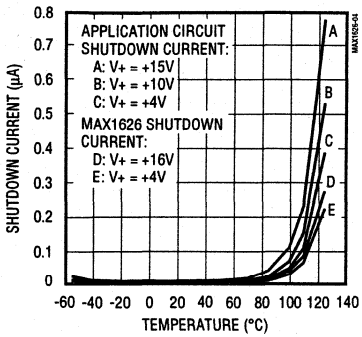


5V/3.3V or Adjustable, 100% Duty-Cycle, High-Efficiency, Step-Down DC-DC Controllers

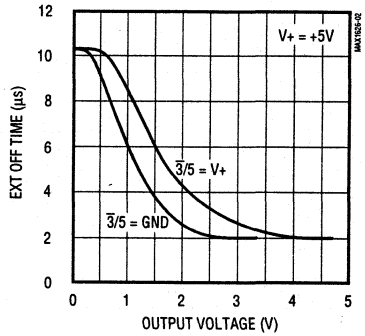
Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

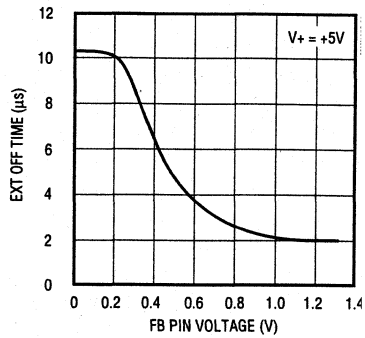
MAX1626 SHUTDOWN CURRENT vs. TEMPERATURE



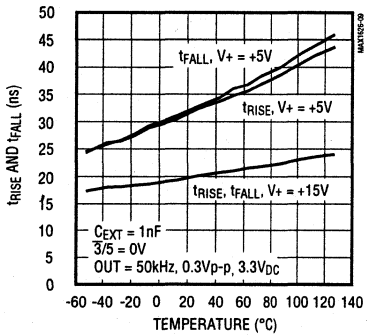
MAX1626 EXT OFF TIME vs. OUTPUT VOLTAGE



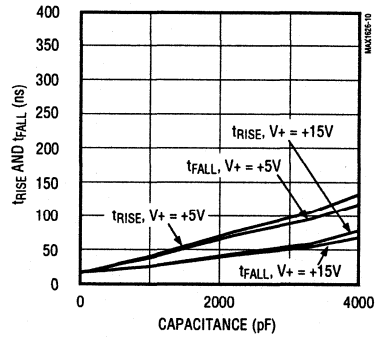
MAX1627 EXT OFF TIME vs. FB PIN VOLTAGE



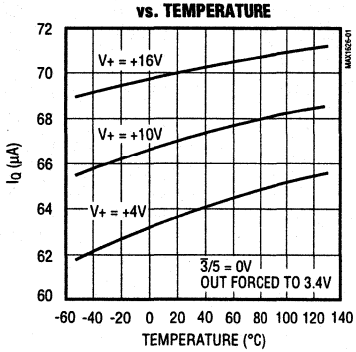
EXT RISE AND FALL TIMES vs. TEMPERATURE



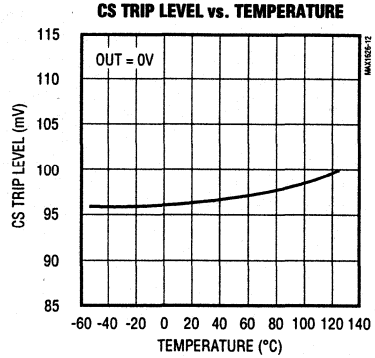
EXT RISE AND FALL TIMES vs. CAPACITANCE



MAX1626 V+ QUIESCENT CURRENT vs. TEMPERATURE



CS TRIP LEVEL vs. TEMPERATURE

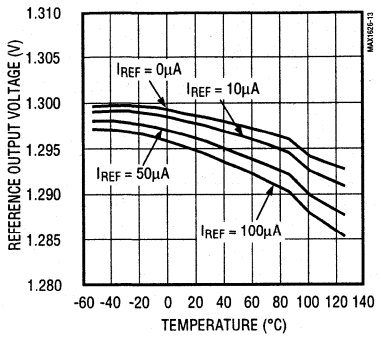


5V/3.3V or Adjustable, 100% Duty-Cycle, High-Efficiency, Step-Down DC-DC Controllers

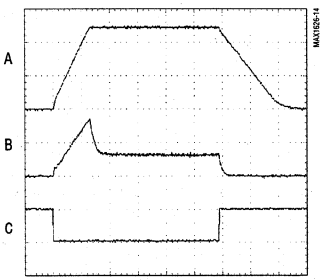
Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

REFERENCE OUTPUT VOLTAGE vs. TEMPERATURE



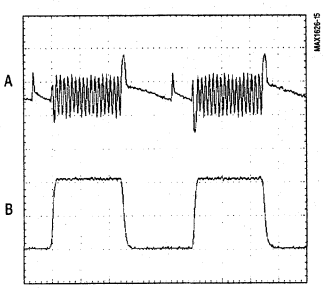
MAX1626 SHUTDOWN RESPONSE TIME AND SUPPLY CURRENT



500µs/div

V+ = 8V, V_{OUT} = 5V, LOAD = 1A
A: OUT, 2V/div
B: SUPPLY CURRENT, 1A/div
C: SHDN, 5V/div

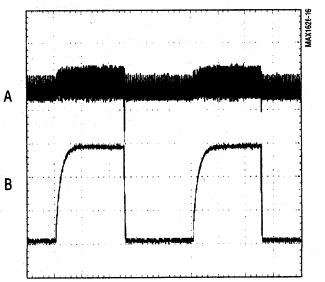
MAX1626 LOAD-TRANSIENT RESPONSE



100µs/div

V+ = 8V, V_{OUT} = 3.3V, LOAD = 30mA to 2A
A: OUT, 50mV/div, 3.3V DC OFFSET
B: LOAD CURRENT, 1A/div

MAX1626 LINE-TRANSIENT RESPONSE



5ms/div

V_{OUT} = 5V, LOAD = 1A, C_{IN} = 33µF
A: OUT, 100mV/div, 5V DC OFFSET
B: V+ 6V to 12V, 2V/div

LINE-TRANSIENT RESPONSE FROM 100% DUTY CYCLE



5ms/div

V_{OUT} = 3.3V, LOAD = 1A, C_{IN} = 47µF
A: OUT, 100mV/div, 3.3V DC OFFSET
B: V+ 3.3V to 15V, 5V/div

5V/3.3V or Adjustable, 100% Duty-Cycle, High-Efficiency, Step-Down DC-DC Controllers

Pin Description

PIN		NAME	FUNCTION
MAX1626	MAX1627		
1	1	OUT	Sense input for fixed 5V or 3.3V output operation. OUT is internally connected to an on-chip voltage divider (MAX1626). It does not supply current. Leave OUT unconnected during adjustable-output operation (MAX1627).
—	2	FB	Feedback Input for adjustable-output operation. Connect to an external voltage divider between the output and GND (see the *Setting the Output Voltage* section).
2	—	$\overline{3}/5$	3.3V or 5V Selection. Output voltage is set to 3.3V when this pin is low or 5V when it is high.
3	3	SHDN	Active-High Shutdown Input. Device is placed in shutdown when SHDN is driven high. In shutdown mode, the reference, output, and external MOSFET are turned off. Connect to GND for normal operation.
4	4	REF	1.3V Reference Output. Can source 100µA. Bypass with 0.1µF.
5	5	V+	Positive Supply Input. Bypass with 0.47µF.
6	6	CS	Current-Sense Input. Connect current-sense resistor between V+ and CS. External MOSFET is turned off when the voltage across the resistor equals the current-limit trip level (around 100mV).
7	7	EXT	Gate Drive for External P-Channel MOSFET. EXT swings between V+ and GND.
8	8	GND	Ground

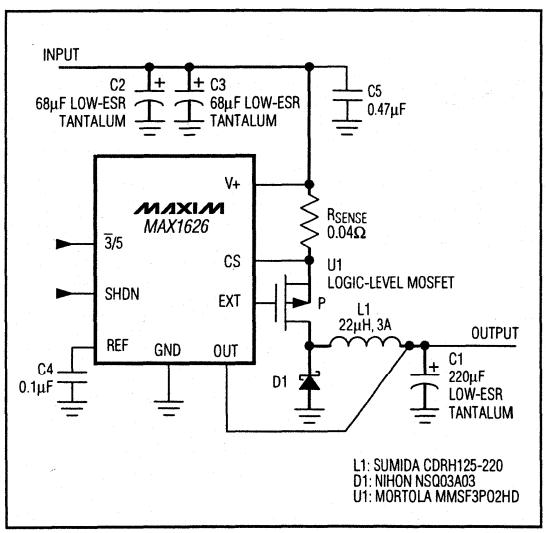


Figure 1. MAX1626 Typical Operating Circuit

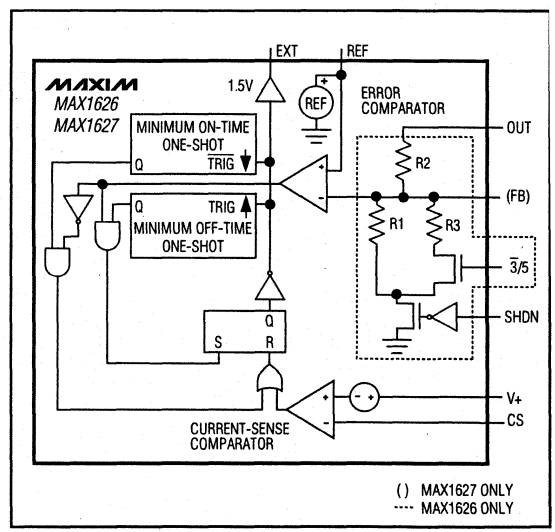


Figure 2. Simplified Functional Diagram

5V/3.3V or Adjustable, 100% Duty-Cycle, High-Efficiency, Step-Down DC-DC Controllers

Detailed Description

The MAX1626/MAX1627 are step-down DC-DC controllers designed primarily for use in portable computers and battery-powered devices. Using an external MOSFET and current-sense resistor allows design flexibility and the improved efficiencies associated with high-performance P-channel MOSFETs. A unique, current-limited, pulse-frequency-modulated (PFM) control scheme gives these devices excellent efficiency over load ranges up to three decades, while drawing around 90µA under no load. This wide dynamic range optimizes the MAX1626/MAX1627 for battery-powered applications, where load currents can vary considerably as individual circuit blocks are turned on and off to conserve energy. Operation to a 100% duty cycle allows the lowest possible dropout voltage, extending battery life. High switching frequencies and a simple circuit topology minimize PC board area and component costs. Figure 1 shows a typical operating circuit for the MAX1626.

PFM Control Scheme

The MAX1626/MAX1627 use a proprietary, third-generation, current-limited PFM control scheme. Improvements include a reduced current-sense threshold and operation to a 100% duty cycle. These devices pulse only as needed to maintain regulation, resulting in a variable switching frequency that increases with the load. This eliminates the current drain associated with constant-frequency pulse-width-modulation (PWM) controllers, caused by switching the MOSFET unnecessarily.

When the output voltage is too low, the error comparator sets a flip-flop, which turns on the external P-channel MOSFET and begins a switching cycle (Figures 1 and 2). As shown in Figure 3, current through the inductor ramps up linearly, storing energy in a magnetic field while dumping charge into an output capacitor and servicing the load. When the MOSFET is turned off, the magnetic field collapses, diode D1 turns on, and the current through the inductor ramps back down, transferring the stored energy to the output capacitor and load. The output capacitor stores energy when the inductor current is high and releases it when the inductor current is low.

The MAX1626/MAX1627 use a unique feedback and control system to govern each pulse. When the output voltage is too low, the error comparator sets a flip-flop, which turns on the external P-channel MOSFET. The MOSFET turns off when the current-sense threshold is exceeded or when the output voltage is in regulation. A one-shot enforces a 2µs minimum on-time, except in current limit. The flip-flop resets when the MOSFET turns off. Otherwise the MOSFET remains on, allowing a duty cycle of up to 100%. This feature ensures the lowest possible dropout. Once the MOSFET is turned off, the minimum off-time comparator keeps it off. The minimum off-time is normally 2µs, except when the output is significantly out of regulation. If the output is low by 30% or more, the minimum off-time increases, allowing soft-start. The error comparator has 0.5% hysteresis for improved noise immunity.

In the MAX1626, the $\overline{3}/5$ pin selects the output voltage (Figure 2). In the MAX1627, external feedback resistors at FB adjust the output.

Operating Modes

When delivering low and medium output currents, the MAX1626/MAX1627 operate in discontinuous-conduction mode. Current through the inductor starts at zero, rises as high as the peak current limit set by the current- sense resistor, then ramps down to zero during each cycle (Figure 3). Although efficiency is still excellent, output ripple increases and the switch waveform exhibits ringing. This ringing occurs at the resonant frequency of the inductor and stray capacitance, due to residual energy trapped in the core when the commutation diode (D1 in Figure 1) turns off. It is normal and poses no operational problems.

When delivering high output currents, the MAX1626/MAX1627 operate in continuous-conduction mode (Figure 4). In this mode, current always flows through the inductor and never ramps to zero. The control circuit adjusts the switch duty cycle to maintain regulation without exceeding the peak switching current set by the current-sense resistor. This provides reduced output ripple and high efficiency.

100% Duty Cycle and Dropout

The MAX1626/MAX1627 operate with a duty cycle up to 100%. This feature extends usable battery life by turning the MOSFET on continuously when the supply voltage approaches the output voltage. This services the load when conventional switching regulators with less than 100% duty cycle would fail. Dropout voltage is defined as the difference between the input and output voltages when the input is low enough for the output to drop out of regulation. Dropout depends on the MOSFET drain-to-source on-resistance, current-sense resistor, and inductor series resistance, and is proportional to the load current:

$$\text{Dropout Voltage} = I_{OUT} \times \left[R_{DS(ON)} + R_{SENSE} + R_{INDUCTOR}\right]$$

5V/3.3V or Adjustable, 100% Duty-Cycle, High-Efficiency, Step-Down DC-DC Controllers

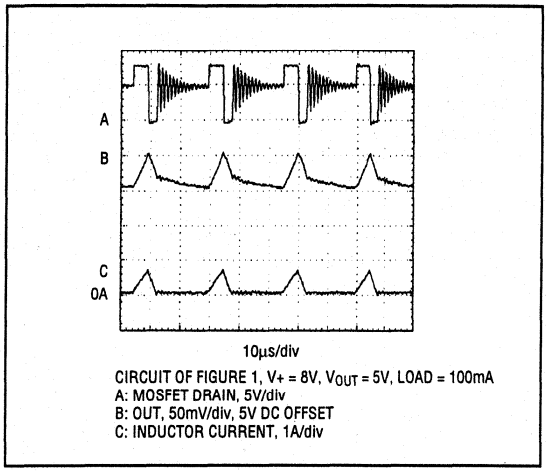


Figure 3. Discontinuous-Conduction Mode, Light-Load-Current Waveform

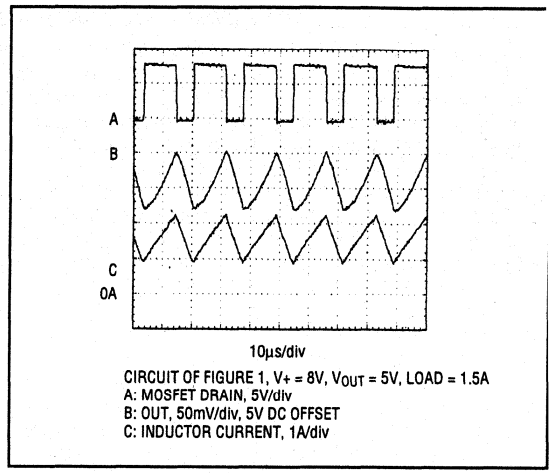


Figure 4. Continuous-Conduction Mode, Heavy-Load-Current Waveform

EXT Drive Voltage Range

EXT swings from V+ to GND and provides the gate drive for an external P-channel power MOSFET. A higher supply voltage increases the gate drive to the MOSFET and reduces on-resistance ($R_{DS(ON)}$). See *External Switching Transistor* section.

Quiescent Current

The device's typical quiescent current is 70µA. However, actual applications draw additional current to supply MOSFET switching currents, OUT pin current, or external feedback resistors (if used), and both the diode and capacitor leakage currents. For example, in the circuit of Figure 1, with V+ at 7V and V_{OUT} at 5V, typical no-load supply current for the entire circuit is 84µA. When designing a circuit for high-temperature operation, select a Schottky diode with low reverse leakage.

Shutdown Mode

When SHDN is high, the device enters shutdown mode. In this mode, the feedback and control circuit, reference, and internal biasing circuitry are turned off. EXT goes high, turning off the external MOSFET. The shutdown supply current drops to less than 1µA. SHDN is a logic-level input. Connect SHDN to GND for normal operation.

Reference

The 1.3V reference is suitable for driving external loads, such as an analog-to-digital converter. It has a guaranteed 10mV maximum load regulation while sourcing load currents up to 100µA. The reference is turned off during shutdown. Bypass the reference with 0.1µF for normal operation. Place the bypass capacitor within 0.2 inches (5mm) of REF, with a direct trace to GND (Figure 7).

Soft-Start

Soft-start reduces stress and transient voltage slumps on the power source. When the output voltage is near ground, the minimum off-time is lengthened to limit peak switching current. This compensates for reduced negative inductor current slope due to low output voltages.

Design Information

Setting the Output Voltage

The MAX1626's output voltage can be selected to 3.3V or 5V under logic control by using the $\overline{3}/5$ pin. The $\overline{3}/5$ pin requires less than 0.5V to ensure a 3.3V output, or more than (V+ - 0.5)V to guarantee a 5V output. The voltage sense pin (OUT) must be connected to the output for the MAX1626.

The MAX1627's output voltage is set using two resistors, R2 and R3 (Figure 5), which form a voltage divider between the output and GND. R2 is given by:

$$R2 = R3 \times \left(\frac{V_{OUT}}{V_{REF}} - 1 \right)$$

where V_{REF} = 1.3V. Since the input bias current at FB has a maximum value of 50nA, large values (10kΩ to 200kΩ) can be used for R3 with no significant accuracy loss. For 1% error, the current through R2 should be at

least 100 times FB's input bias current. Capacitor C_{R2} is used to compensate the MAX1627 for even switching. Values between 0pF and 330pF work for many applications. See the *Stability and MAX1627 Feedback Compensation* section for details.

Current-Sense-Resistor Selection

The current-sense comparator limits the peak switching current to V_{CS}/R_{SENSE}, where R_{SENSE} is the value of the current-sense resistor and V_{CS} is the current-sense threshold. V_{CS} is typically 100mV, but can range from 85mV to 115mV. Minimizing the peak switching current will increase efficiency and reduce the size and cost of external components. However, since available output current is a function of the peak switching current, the peak current limit must not be set too low.

Set the peak current limit above 1.3 times the maximum load current by setting the current-sense resistor to:

$$R_{CS} = \frac{V_{CS(MIN)}}{1.3 \times I_{OUT(MAX)}}$$

Alternatively, select the current-sense resistor for 5V and 3.3V output applications using the current-sense resistor graphs in Figures 6a and 6b. The current-sense resistor's power rating should be 20% higher than:

$$R_{POWER\ RATING\ (W)} = \frac{V^2_{CS(MAX)}}{R_{CS}}$$

Standard wire-wound resistors have an inductance high enough to degrade performance, and are not recommended. Surface-mount (chip) resistors have very little inductance and are well suited for use as current-sense resistors. Power metal-strip resistors feature 1/2W and 1W power dissipation, 1% tolerance, and inductance below 5nH. Resistance values between 10mΩ and 500mΩ are available.

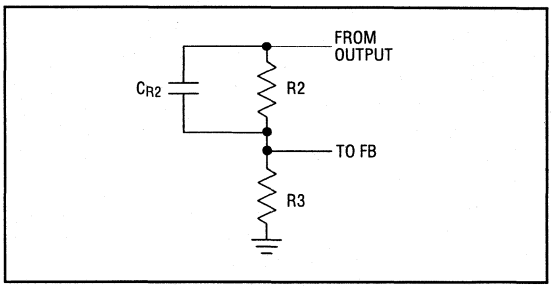


Figure 5. Adjustable-Output Operation Using the MAX1627

Inductor Selection

The essential parameters for inductor selection are inductance and current rating. The MAX1626/MAX1627 operate with a wide range of inductance values. In many applications, values between 10µH and 68µH take best advantage of the controller's high switching frequency.

Calculate the minimum inductance value as follows:

$$L_{(MIN)} = \frac{\left(V_{+(MAX)} - V_{OUT}\right) \times 2\mu s}{\frac{V_{CS(MIN)}}{R_{CS}}}$$

where 2µs is the minimum on-time. Inductor values between two and six times $L_{(MIN)}$ are recommended.

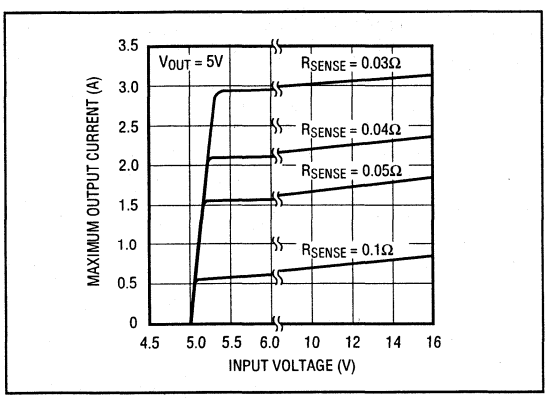


Figure 6a. MAX1626 5V-Operation Current-Sense Resistor Graph

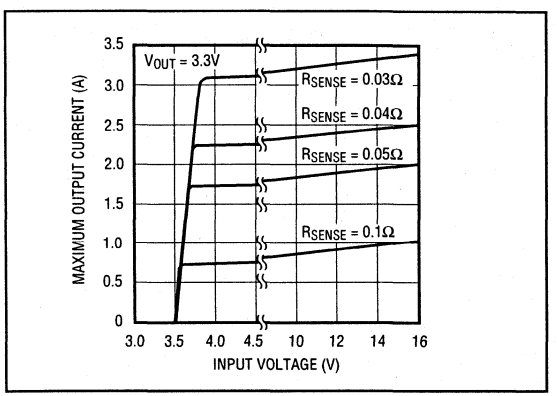


Figure 6b. MAX1626 3.3V-Operation Current-Sense Resistor Graph

5V/3.3V or Adjustable, 100% Duty-Cycle, High-Efficiency, Step-Down DC-DC Controllers

With high inductor values, the MAX1626/MAX1627 will begin continuous-conduction operation at a lower fraction of the full load (see *Detailed Description*). Low-value inductors may be smaller and less expensive, but they result in greater peak current overshoot due to current-sense comparator propagation delay. Peak-current overshoot reduces efficiency and could cause the external components' current ratings to be exceeded.

The inductor's saturation and heating current ratings must be greater than the peak switching current to prevent overheating and core saturation. Saturation occurs when the inductor's magnetic flux density reaches the maximum level the core can support, and inductance starts to fall. The heating current rating is the maximum DC current the inductor can sustain without overheating. The peak switching current is the sum of the current limit set by the current-sense resistor and overshoot during current-sense comparator propagation delay.

$$I_{PEAK} = \frac{V_{CS}}{R_{CS}} + \frac{(V+ - V_{OUT}) \times 1\mu s}{L}$$

1µs is the worst-case current-sense comparator propagation delay.

Inductors with a core of ferrite, Kool Mu™, METGLAS™, or equivalent, are recommended. Powder iron cores are not recommended for use with high switching frequencies. For optimum efficiency, the inductor windings' resistance should be on the order of the current-sense resistance. If necessary, use a toroid, pot-core, or shielded-core inductor to minimize radiated noise. Table 1 lists inductor types and suppliers for various applications.

KOOL Mu is a trademark of Magnetics.

METGLAS is a trademark of Allied Signal.

External Switching Transistor

The MAX1626/MAX1627 drive P-channel enhancement-mode MOSFETs. The EXT output swings from GND to the voltage at V+. To ensure the MOSFET is fully on, use logic-level or low-threshold MOSFETs when the input voltage is less than 8V. Tables 1 and 2 list recommended suppliers of switching transistors.

Four important parameters for selecting a P-channel MOSFET are drain-to-source breakdown voltage, current rating, total gate charge (Q_G), and $R_{DS(ON)}$. The drain-to-source breakdown voltage rating should be at least a few volts higher than V+. Choose a MOSFET with a maximum continuous drain current rating higher than the peak current limit:

$$I_{D(MAX)} \geq I_{LIM(MAX)} = \frac{V_{CS(MAX)}}{R_{SENSE}}$$

The Qg specification should be less than 100nC to ensure fast drain voltage rise and fall times, and reduce power losses during transition through the linear region. Q_G specifies all of the capacitances associated with charging the MOSFET gate. EXT pin rise and fall times vary with different capacitive loads, as shown in the *Typical Operating Characteristics*. $R_{DS(ON)}$ should be as low as practical to reduce power losses while the MOSFET is on. It should be equal to or less than the current-sense resistor.

Table 1. Component Selection Guide

PRODUCTION METHOD	INDUCTORS	CAPACITORS	DIODES	CURRENT-SENSE RESISTORS	MOSFETS
Surface Mount	Sumida CDRH125-470 (1.8A) CDRH125-220 (2.2A) Coilcraft DO3316-473 (1.6A) DO3340-473 (3.8A)	AVX TPS series Sprague 595D series	Motorola MBRS340T3 Nihon NSQ series	Dale WSL series IRC LRC series	Siliconix Little Foot series Motorola medium-power surface-mount products
Miniature Through-Hole	Sumida RCH875-470M (1.3A)	Sanyo OS-CON series low-ESR organic semiconductor		IRC OAR series	Motorola
Low-Cost Through-Hole	Coilcraft PCH-45-473 (3.4A)	Nichicon PL series low-ESR electrolytics United Chemi-Con LXF series	Motorola 1N5817 to 1N5823		Motorola TMOS power MOSFETs

Table 2. Component Suppliers

COMPANY		PHONE	FAX
AVX	USA	(803) 946-0690 or (800) 282-4975	(803) 626-3123
Coilcraft	USA	(847) 639-6400	(847) 639-1469
Coiltronics	USA	(516) 241-7876	(516) 241-9339
Dale	USA	(605) 668-4131	(605) 665-1627
International Rectifier	USA	(310) 322-3331	(310) 322-3332
IRC	USA	(512) 992-7900	(512) 992-3377
Motorola	USA	(602) 303-5454	(602) 994-6430
Nichicon	USA Japan	(847) 843-7500 81-7-5231-8461	(847) 843-2798 81-7-5256-4158
Nihon	USA Japan	(805) 867-2555 81-3-3494-7411	(805) 867-2698 81-3-3494-7414
Sanyo	USA Japan	(619) 661-6835 81-7-2070-6306	(619) 661-1055 81-7-2070-1174
Siliconix	USA	(408) 988-8000 or (800) 554-5565	(408) 970-3950
Sprague	USA	(603) 224-1961	(603) 224-1430
Sumida	USA Japan	(847) 956-0666 81-3-3607-5111	(847) 956-0702 81-3-3607-5144
United Chemi-Con	USA	(714) 255-9500	(714) 255-9400

Diode Selection

The MAX1626/MAX1627's high switching frequency demands a high-speed rectifier. Schottky diodes, such as the 1N5817–1N5822 family or surface-mount equivalents, are recommended. Ultra-high-speed rectifiers with reverse recovery times around 50ns or faster, such as the MUR series, are acceptable. Make sure that the diode's peak current rating exceeds the peak current limit set by R_{SENSE}, and that its breakdown voltage exceeds V+. Schottky diodes are preferred for heavy loads due to their low forward voltage, especially in low-voltage applications. For high-temperature applications, some Schottky diodes may be inadequate due to their high leakage currents. In such cases, ultra-high-speed rectifiers are recommended, although a Schottky diode with a higher reverse voltage rating can often provide acceptable performance.

Capacitor Selection

Choose filter capacitors to service input and output peak currents with acceptable voltage ripple. Equivalent series resistance (ESR) in the capacitor is a major contributor to output ripple, so low-ESR capacitors are recommended. Sanyo OS-CON capacitors are best, and low-ESR tantalum capacitors are second best. Low-ESR aluminum electrolytic capacitors are tolerable, but do not use standard aluminum electrolytic capacitors.

Voltage ripple is the sum of contributions from ESR and the capacitor value:

$$V_{RIPPLE} \approx V_{RIPPLE,ESR} + V_{RIPPLE,C}$$

To simplify selection, assume initially that two-thirds of the ripple results from ESR and one-third results from capacitor value. Voltage ripple as a consequence of ESR is approximated by:

$$V_{RIPPLE,ESR} \approx (R_{ESR})(I_{PEAK})$$

Estimate input and output capacitor values for given voltage ripple as follows:

$$C_{IN} = \frac{\frac{1}{2}LI_{\Delta L}^2}{V_{RIPPLE,CIN}V_{IN}}$$

$$C_{OUT} = \frac{\frac{1}{2}LI_{\Delta L}^2}{V_{RIPPLE,COUT}V_{OUT}} \left(\frac{V_{IN}}{V_{IN} - V_{OUT}}\right)$$

where $I_{\Delta L}$ is the change in inductor current (around $0.5I_{PEAK}$ under moderate loads).

These equations are suitable for initial capacitor selection; final values should be set by testing a prototype or evaluation kit. When using tantalum capacitors, use good soldering practices to prevent excessive heat from damaging the devices and increasing their ESR. Also, ensure that the tantalum capacitors' surge-current ratings exceed the start-up inrush and peak switching currents.

Pursuing output ripple lower than the error comparator's hysteresis (0.5% of the output voltage) is not practical, since the MAX1626/MAX1627 will switch as needed, until the output voltage crosses the hysteresis threshold. Choose an output capacitor with a working voltage rating higher than the output voltage.

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on V+ and CS, caused by the circuit's switching action. Use a low-ESR capacitor. Two smaller-value low-ESR capacitors can be connected in parallel for lower cost. Choose input capacitors with working voltage ratings higher than the maximum input voltage.

Place a surface-mount ceramic capacitor very close to V+ and GND, as shown in Figure 7. This capacitor bypasses the MAX1626/MAX1627, and prevents spikes and ringing on the power source from obscuring the

5V/3.3V or Adjustable, 100% Duty-Cycle, High-Efficiency, Step-Down DC-DC Controllers

current feedback signal and causing jitter. 0.47µF is recommended. Increase the value as necessary in high-power applications.

Bypass REF with 0.1µF. This capacitor should be placed within 0.2 inches (5mm) of the IC, next to REF, with a direct trace to GND (Figure 7).

Layout Considerations

High-frequency switching regulators are sensitive to PC board layout. Poor layout introduces switching noise into the current and voltage feedback signals, resulting in jitter, instability, or degraded performance. The current-sense resistor must be placed within 0.2 inches (5mm) of the controller IC, directly between V+ and CS. Place voltage feedback resistors (MAX1627) next to the FB pin (no more than 0.2") rather than near the output. Place the 0.47µF input and 0.1µF reference bypass capacitors within 0.2 inches (5mm) of V+ and REF, and route directly to GND. Figure 7 shows the recommended layout and routing for these components.

High-power traces, highlighted in the *Typical Operating Circuit* (Figure 1), should be as short and as wide as possible. The supply-current loop (formed by C2, C3, RSENSE, U1, L1, and C1) and commutation-current loop (D1, L1, and C1) should be as tight as possible to reduce radiated noise. Place the anode of the commutation diode (D1) and the ground pins of the input and output filter capacitors close together, and route them to a common "star-ground" point. Place components and route ground paths so as to prevent high currents from causing large voltage gradients between the ground pin of the output filter capacitor, the controller IC, and the reference bypass capacitor. Keep the extra copper on the component and solder sides of the PC board, rather than etching it away, and connect it to ground for use as a pseudo-ground plane. Refer to the MAX1626 Evaluation Kit manual for a two-layer PC board example.

Stability and MAX1627 Feedback Compensation

Use proper PC board layout and recommended external components to ensure stable operation. In one-shot, sequenced PFM DC-DC converters, instability is manifested as "Motorboat Instability." It is usually caused by excessive noise on the current or voltage feedback signals, ground, or reference, due to poor PC board design or external component selection. Motorboat instability is characterized by grouped switching pulses with large gaps and excessive low-frequency output ripple. It is normal to see some grouped switching pulses during the transition from discontinuous to continuous current mode. This effect is associated with small gaps between pulse groups and output ripple similar to or less than that seen during no-load conditions.

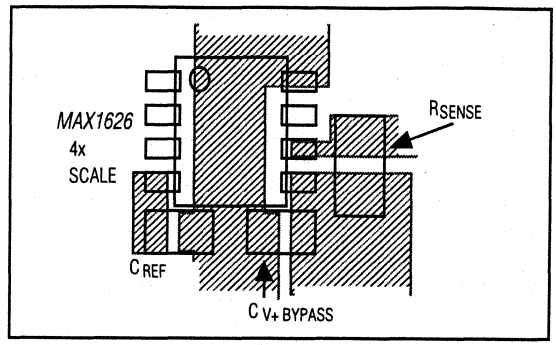


Figure 7. Recommended Placement and Routing of the Current-Sense Resistor, 0.1µF Reference, and 0.47µF Input Bypass Capacitors

Instability can also be caused by excessive stray capacitance on FB when using the MAX1627. Compensate for this by adding a 0pF to 330pF feed-forward capacitor across the upper feedback resistor (R2 in Figure 5).

MAX1626/MAX1627 vs. MAX1649/MAX1651 vs. MAX649/MAX651

The MAX1626/MAX1627 are specialized, third-generation upgrades to the MAX649/MAX651 step-down controllers. They feature improved efficiency, a reduced current-sense threshold (100mV), soft-start, and a 100% duty cycle for lowest dropout. The MAX649/MAX651 have a two-step (210mV/110mV) current-sense threshold. The MAX1649/MAX1651 are second-generation upgrades with a 96.5% maximum duty cycle for improved dropout performance and a reduced current-sense threshold (110mV) for higher efficiency, especially at low input voltages. The MAX1649/MAX1651 are preferable for special applications where a 100% duty cycle is undesirable, such as flyback and SEPIC circuits.

Since the MAX1626's pinout is similar to those of the MAX649 and MAX1649 family parts, the MAX1626 can be substituted (with minor external component value changes) into fixed-output mode applications, provided the PC board layout is adequate. The MAX1627 can also be substituted when MAX649 or MAX1649 family parts are used in adjustable mode, but the feedback resistor values must be changed, since the MAX1627 has a lower reference voltage (1.3V vs. 1.5V). Reduce the current-sense resistor value by 50% when substituting for the MAX649 or MAX651.

5V/3.3V or Adjustable, 100% Duty-Cycle, High-Efficiency, Step-Down DC-DC Controllers

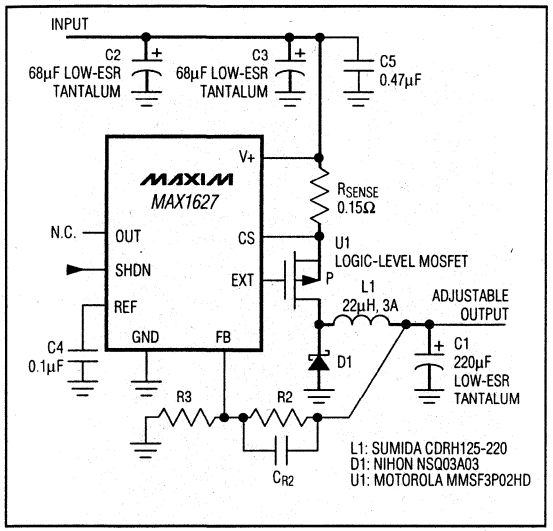


Figure 8. MAX1627 Typical Operating Circuit

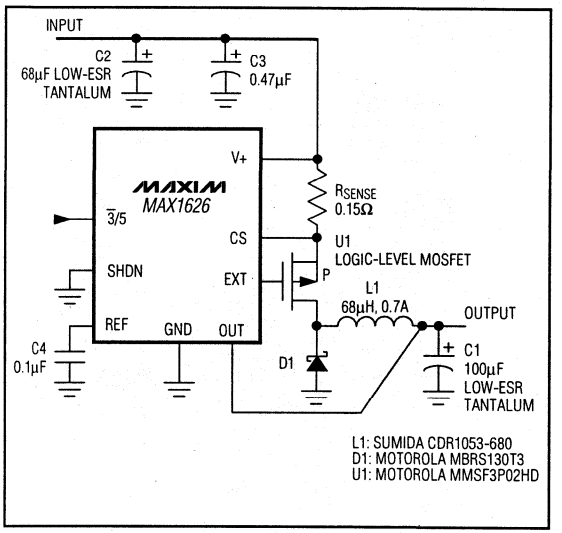


Figure 9. 0.5A Step-Down Converter

Applications

The MAX1626/MAX1627 typical operating circuits (Figures 1 and 8) are designed to output 2A at a 5V output voltage. The following circuits provide examples and guidance for other applications.

Micropower Step-Down Converter

When designing a low-power, battery-based application, choose an external MOSFET with low gate capacitance (to minimize switching losses), and use a low peak current limit to reduce I^2R losses. The circuit in Figure 9 is optimized for 0.5A.

High-Current Step-Down Converter

The circuit in Figure 10 outputs 6A at 2.5V from a 5V or 3.3V input. High-current design is difficult, and board layout is critical due to radiated noise, switching transients, and voltage gradients on the PC board traces. Figure 11 is a recommended PC board design. Choose the external MOSFET to minimize $R_{DS(ON)}$. Keep the gate-charge factor below the MAX1626/MAX1627's drive capability (see Ext Rise and Fall Times vs. Capacitance graph in the *Typical Operating Characteristics*). Otherwise, increased MOSFET rise and fall times will contribute to efficiency losses. For higher efficiencies, especially at low output voltages, the MAX796 family of step-down controllers with synchronous rectification is recommended.

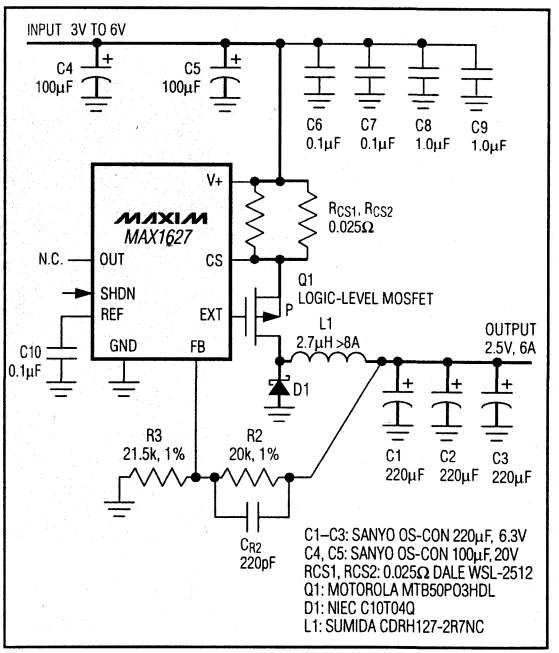
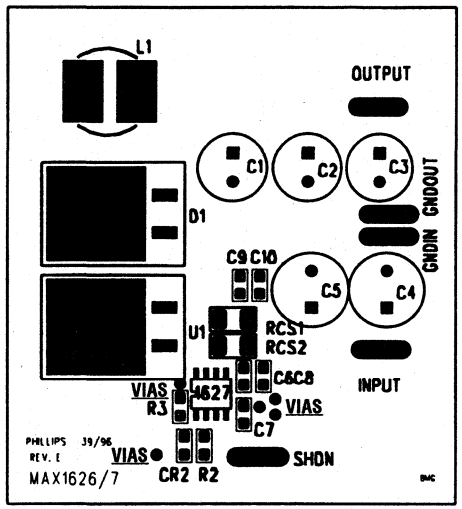
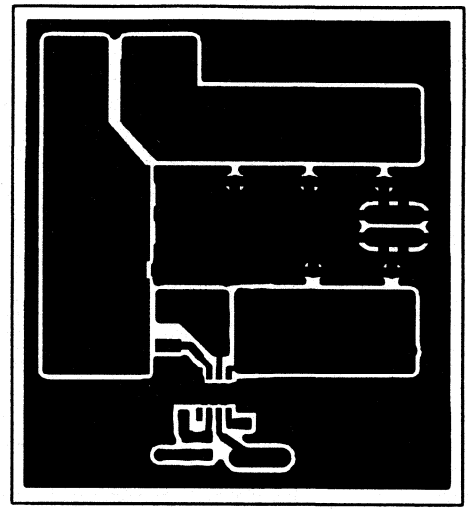


Figure 10. 6A Step-Down Converter

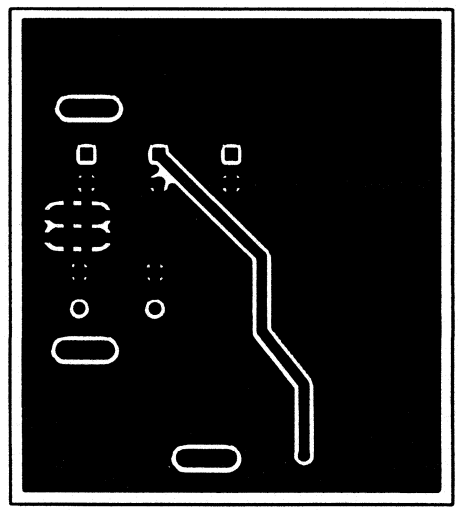
5V/3.3V or Adjustable, 100% Duty-Cycle, High-Efficiency, Step-Down DC-DC Controllers



COMPONENT PLACEMENT GUIDE—COMPONENT SIDE



COPPER ROUTING—FRONT SIDE

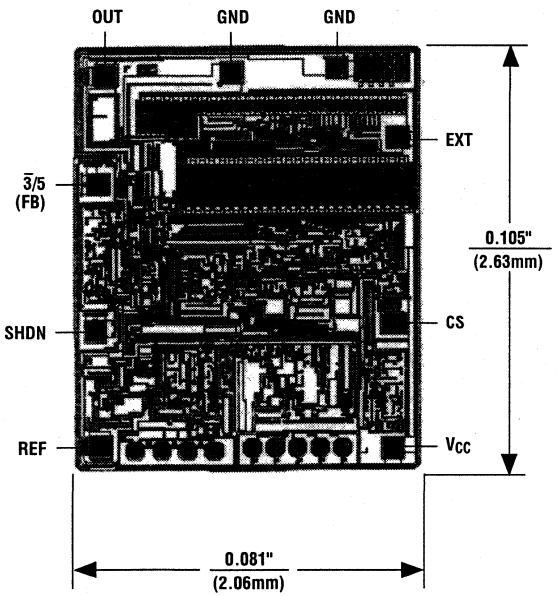


COPPER ROUTING—BACK SIDE

Figure 11. Recommended PC Board Design for 6A Step-Down Converter

5V/3.3V or Adjustable, 100% Duty-Cycle, High-Efficiency, Step-Down DC-DC Controllers

Chip Topography



( ) ARE FOR MAX1627

TRANSISTOR COUNT: 375

SUBSTRATE CONNECTED TO V+

19-0480; Rev 2; 12/96

EVALUATION KIT AVAILABLE

MAXIM

Multi-Output, Low-Noise Power-Supply Controllers for Notebook Computers

General Description

The MAX1630–MAX1635 are buck-topology, step-down, switch-mode, power-supply controllers that generate logic-supply voltages in battery-powered systems. These high-performance, dual/triple-output devices include on-board power-up sequencing, power-good signaling with delay, digital soft-start, secondary winding control, low-dropout circuitry, internal frequency-compensation networks, and automatic bootstrapping.

Up to 96% efficiency is achieved through synchronous rectification and Maxim's proprietary Idle Mode™ control scheme. Efficiency is greater than 80% over a 1000:1 load-current range, which extends battery life in system-suspend or standby mode. Excellent dynamic response corrects output load transients caused by the latest dynamic-clock CPUs within five 300kHz clock cycles. Strong 1A on-board gate drivers ensure fast external N-channel MOSFET switching.

These devices feature a logic-controlled and synchronizable, fixed-frequency, pulse-width-modulation (PWM) operating mode. This reduces noise and RF interference in sensitive mobile communications and pen-entry applications. Asserting the $\overline{SKIP}$ pin enables fixed-frequency mode, for lowest noise under all load conditions.

The MAX1630–MAX1635 include two PWM regulators, adjustable from 2.5V to 5.5V with fixed 5.0V and 3.3V modes. All these devices include secondary feedback regulation, and the MAX1630/MAX1632/MAX1633/MAX1635 each contain 12V/120mA linear regulators. The MAX1631/MAX1634 include a secondary feedback input (SECFB), plus a control pin (STEER) that selects which PWM (3.3V or 5V) receives the secondary feedback signal. SECFB provides a method for adjusting the secondary winding voltage regulation point with an external resistor divider, and is intended to aid in creating auxiliary voltages other than fixed 12V.

The MAX1630/MAX1631/MAX1632 contain internal output overvoltage and undervoltage protection features.

Applications

Notebook and Subnotebook Computers

PDAs and Mobile Communicators

Desktop CPU Local DC-DC Converters

Pin Configurations and Selector Guide appear at end of data sheet.

Idle Mode and Dual Mode are trademarks of Maxim Integrated Products.

Features

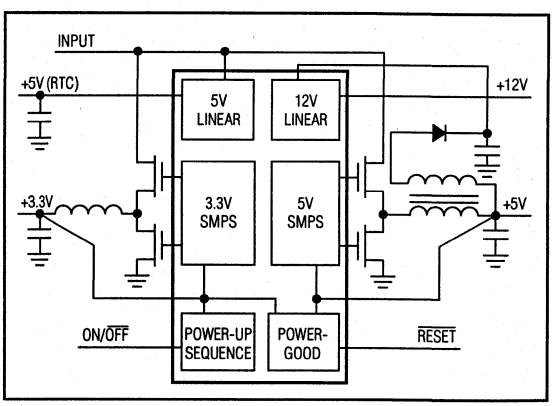
- ♦ **96% Efficiency**
- ♦ **+4.2V to +30V Input Range**
- ♦ **2.5V to 5.5V Dual Adjustable Outputs**
- ♦ **Selectable 3.3V and 5V Fixed or Adjustable Outputs (Dual Mode™)**
- ♦ **12V Linear Regulator**
- ♦ **Adjustable Secondary Feedback (MAX1631/MAX1634)**
- ♦ **5V/50mA Linear Regulator Output**
- ♦ **Precision 2.5V Reference Output**
- ♦ **Programmable Power-Up Sequencing**
- ♦ **Power-Good ($\overline{RESET}$) Output**
- ♦ **Output Overvoltage Protection (MAX1630/MAX1631/MAX1632)**
- ♦ **Output Undervoltage Shutdown (MAX1630/MAX1631/MAX1632)**
- ♦ **200kHz/300kHz Low-Noise, Fixed-Frequency Operation**
- ♦ **Low-Dropout, 99% Duty-Factor Operation**
- ♦ **2.5mW Typical Quiescent Power (+12V input, both SMPSs on)**
- ♦ **4µA Typical Shutdown Current**
- ♦ **28-Pin SSOP Package**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1630CAI	0°C to +70°C	28 SSOP
MAX1630EAI	-40°C to +85°C	28 SSOP

Ordering Information continued on last page.

Functional Diagram



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Multi-Output, Low-Noise Power-Supply Controllers for Notebook Computers

ABSOLUTE MAXIMUM RATINGS

V+ to GND .....-0.3V to +36V
PGND to GND .....±0.3V
VL to GND .....-0.3V to +6V
BST3, BST5 to GND .....-0.3V to +36V
LX3 to BST3 .....-6V to +0.3V
LX5 to BST5 .....-6V to +0.3V
REF, SYNC, SEQ, STEER, $\overline{SKIP}$, TIME/ON5, SECFB, $\overline{RESET}$ to GND .....-0.3V to +6V
V_{DD} to GND .....-0.3V to +20V
RUN/ON3, $\overline{SHDN}$ to GND .....-0.3V to (V+ + 0.3V)
12OUT to GND .....-0.3V to (V_{DD} + 0.3V)
DL3, DL5 to PGND .....-0.3V to (VL + 0.3V)
DH3 to LX3 .....-0.3V to (BST3 + 0.3V)
DH5 to LX5 .....-0.3V to (BST5 + 0.3V)

VL, REF Short to GND .....Momentai
12OUT Short to GND .....Continuou
REF Current .....+5mA to -1m
VL Current .....+50m
12OUT Current .....+200m
V_{DD} Shunt Current .....+15m
Operating Temperature Ranges
MAX163_CAI .....0°C to +70°
MAX163_EAI .....-40°C to +85°
Storage Temperature Range .....-65°C to +160°
Continuous Power Dissipation (T_A = +70°C)
SSOP (derate 9.52mW/°C above +70°C) 762mV
Lead Temperature (soldering, 10sec) .....+300°

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and function operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 15V, both PWMs on, SYNC = VL, VL load = 0mA, REF load = 0mA, $\overline{SKIP}$ = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
MAIN SMPS CONTROLLERS					
Input Voltage Range		4.2		30.0	V
3V Output Voltage in Adjustable Mode	V+ = 4.2V to 30V, CSH3–CSL3 = 0V, CSL3 tied to FB3	2.42	2.5	2.58	V
3V Output Voltage in Fixed Mode	V+ = 4.2V to 30V, 0mV < CSH3–CSL3 < 80mV, FB3 = 0V	3.20	3.39	3.47	V
5V Output Voltage in Adjustable Mode	V+ = 4.2V to 30V, CSH5–CSL5 = 0V, CSL5 tied to FB5	2.42	2.5	2.58	V
5V Output Voltage in Fixed Mode	V+ = 5.2V to 30V, 0mV < CSH–CSL5 < 80mV, FB5 = 0V	4.85	5.13	5.25	V
Output Voltage Adjust Range	Either SMPS	REF		5.5	V
Adjustable-Mode Threshold Voltage	Dual Mode comparator	0.5		1.1	V
Load Regulation	Either SMPS, 0V < CSH_–CSL_ < 80mV		-2		%
Line Regulation	Either SMPS, 5.2V < V+ < 30V		0.03		%/V
Current-Limit Threshold	CSH3–CSL3 or CSH5–CSL5	80	100	120	mV
	$\overline{SKIP}$ = VL or V_{DD} < 13V or SECFB < 2.44V	-50	-100	-150	
Idle Mode Threshold	$\overline{SKIP}$ = 0V, not tested	10	25	40	mV
Soft-Start Ramp Time	From enable to 95% full current limit with respect to f_{OSC} (Note 1)		512		clks
Oscillator Frequency	SYNC = VL	270	300	330	kHz
	SYNC = 0V	170	200	230	
Maximum Duty Factor	SYNC = VL	97	98		%
	SYNC = 0V (Note 2)	98	99		

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 15V, both PWMs on, SYNC = VL, VL load = 0mA, REF load = 0mA, $\overline{SKIP}$ = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SYNC Input High Pulse Width	Not tested		200			ns
SYNC Input Low Pulse Width	Not tested		200			ns
SYNC Rise/Fall Time	Not tested				200	ns
SYNC Input Frequency Range			240		350	kHz
Current-Sense Input Leakage Current	V+ = VL = 0V, CSL3 = CSH3 = CSL5 = CSH5 = 5.5V			0.01	10	µA
FLYBACK CONTROLLER						
V_{DD} Regulation Threshold	Falling edge (Note 3)		13		14	V
SECFB Regulation Threshold	Falling edge (MAX1631/MAX1634)		2.44		2.60	V
DL Pulse Width	V_{DD} < 13V or SECFB < 2.44V			1		µs
V_{DD} Shunt Threshold	Rising edge, hysteresis = 1% (Note 3)		18		20	V
V_{DD} Shunt Sink Current	V_{DD} = 20V (Note 3)		10			mA
V_{DD} Leakage Current	V_{DD} = 5V, off mode (Notes 3, 4)				30	µA
12V LINEAR REGULATOR (Note 3)						
12OUT Output Voltage	13V < V_{DD} < 18V, 0mA < IL < 120mA		11.65	12.1	12.50	V
12OUT Current Limit	12OUT forced to 11V, V_{DD} = 13V			150		mA
Quiescent V_{DD} Current	V_{DD} = 18V, run mode, no 12OUT load			50	100	µA
INTERNAL REGULATOR AND REFERENCE						
VL Output Voltage	$\overline{SHDN}$ = V+, RUN/ON3 = TIME/ON5 = 0V, 5.3V < V+ < 30V, 0mA < I_{LOAD} < 50mA		4.7		5.1	V
VL Undervoltage Lockout Fault Threshold	Falling edge, hysteresis = 1%		3.5	3.6	3.7	V
VL Switchover Threshold	Rising edge of CSL5, hysteresis = 1%		4.2	4.5	4.7	V
REF Output Voltage	No external load (Note 5)		2.45	2.5	2.55	V
REF Load Regulation	0µA < I_{LOAD} < 50µA				12.5	mV
	0mA < I_{LOAD} < 5mA				100.0	
REF Sink Current			10			µA
REF Fault Lockout Voltage	Falling edge		1.8		2.4	V
V+ Operating Supply Current	VL switched over to CSL5, 5V SMPS on			5	50	µA
V+ Standby Supply Current	V+ = 5.5V to 30V, both SMPSs off, includes current into $\overline{SHDN}$			30	60	µA
V+ Standby Supply Current in Dropout	V+ = 4.2V to 5.5V, both SMPSs off, includes current into $\overline{SHDN}$			50	200	µA
V+ Shutdown Supply Current	V+ = 4V to 24V, $\overline{SHDN}$ = 0V			4	10	µA
Quiescent Power Consumption	Both SMPSs enabled, FB3 = FB5 = 0V, CSL3 = CSH3 = 3.5V, CSL5 = CSH5 = 5.3V	(Note 3)		2.5	4	mW
		MAX1631/ MAX1634		1.5	4	

Multi-Output, Low-Noise Power-Supply Controllers for Notebook Computers

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 15V, both PWMs on, SYNC = VL, VL load = 0mA, REF load = 0mA, $\overline{SKIP}$ = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
FAULT DETECTION (MAX1630/MAX1631/MAX1632)					
Overvoltage Trip Threshold	With respect to unloaded output voltage	4	7	10	%
Overvoltage-Fault Propagation Delay	CSL_ driven 2% above overvoltage trip threshold		1.5		µs
Output Undervoltage Threshold	With respect to unloaded output voltage	60	70	80	%
Output Undervoltage Lockout Time	From each SMPS enabled, with respect to f_{OSC}	5000	6144	7000	clks
Thermal Shutdown Threshold	Typical hysteresis = +10°C		150		°C
$\overline{RESET}$					
$\overline{RESET}$ Trip Threshold	With respect to unloaded output voltage, falling edge; typical hysteresis = 1%	-7	-5.5	-4	%
$\overline{RESET}$ Propagation Delay	Falling edge, CSL_ driven 2% below $\overline{RESET}$ trip threshold		1.5		µs
$\overline{RESET}$ Delay Time	With respect to f_{OSC}	27,000	32,000	37,000	clks
INPUTS AND OUTPUTS					
Feedback Input Leakage Current	FB3, FB5, SECFB = 2.6V		1	50	nA
Logic Input Low Voltage	RUN/ON3, $\overline{SKIP}$, TIME/ON5 (SEQ = 0V or VL), $\overline{SHDN}$, STEER, SYNC			0.6	V
Logic Input High Voltage	RUN/ON3, $\overline{SKIP}$, TIME/ON5 (SEQ = 0V or VL), $\overline{SHDN}$, STEER, SYNC	2.4			V
Input Leakage Current	RUN/ON3, $\overline{SKIP}$, TIME/ON5 (SEQ = 0V or VL), $\overline{SHDN}$, STEER, SYNC, SEQ = 0V or 3.3V			±1	µA
Logic Output Low Voltage	$\overline{RESET}$, I_{SINK} = 4mA			0.4	V
Logic Output High Current	$\overline{RESET}$ = 3.5V	1			mA
TIME/ON5 Input Trip Level	TIME/ON5, SEQ = REF	2.4		2.6	V
TIME/ON5 Source Current	TIME/ON5 = 0V, SEQ = REF	2.5	3	3.5	µA
TIME/ON5 On-Resistance	TIME/ON5, RUN/ON3 = 0V, SEQ = REF		15	80	Ω
Gate Driver Sink/Source Current	DL3, DH3, DL5, DH5, forced to 2V		1		A
Gate Driver On-Resistance	High or low		1.5	7	Ω

Note 1: Each of the four digital soft-start levels is tested for functionality; the steps are typically in 20mV increments.

Note 2: High duty-factor operation supports low input-to-output differential voltages, and is achieved at a lowered operating frequency (see *Overload and Dropout Operation* section).

Note 3: MAX1630/MAX1632/MAX1633/MAX1635 only.

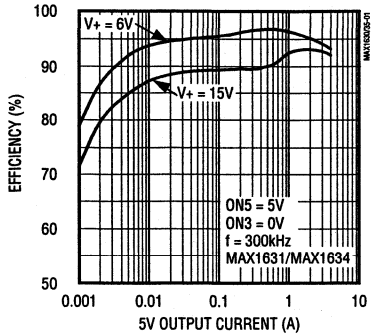
Note 4: Off mode for the 12V linear regulator occurs when the SMPS that has flyback feedback (V_{DD}) steered to it is disabled. In situations where the main outputs are being held up by external keep-alive supplies, turning off the 12OUT regulator prevents a leakage path from the output-referred flyback winding, through the rectifier, and into V_{DD}.

Note 5: Since the reference uses VL as its supply, the reference's V+ line-regulation error is insignificant.

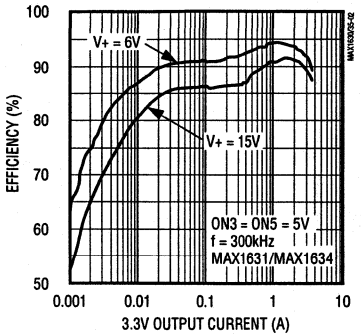
Typical Operating Characteristics

(Circuit of Figure 1, 3A Table 1 components, T_A = +25°C, unless otherwise noted.)

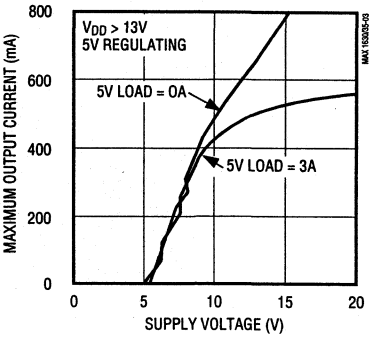
EFFICIENCY vs. 5V OUTPUT CURRENT



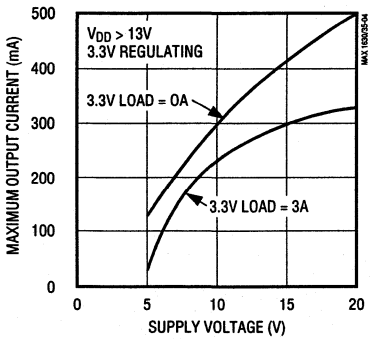
EFFICIENCY vs. 3.3V OUTPUT CURRENT



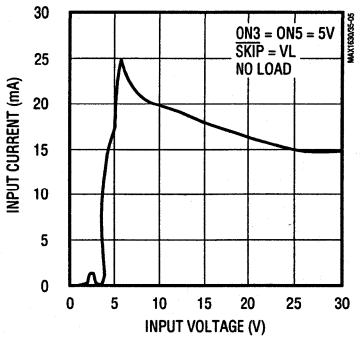
MAX1632/MAX1635 MAXIMUM 15V V_{DD} OUTPUT CURRENT vs. SUPPLY VOLTAGE



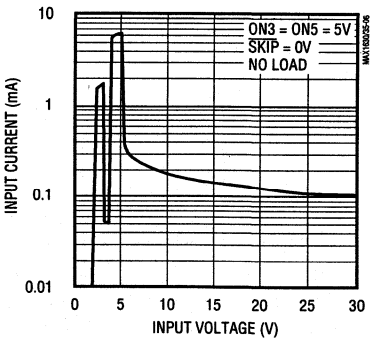
MAX1630/MAX1633 MAXIMUM 15V V_{DD} OUTPUT CURRENT vs. SUPPLY VOLTAGE



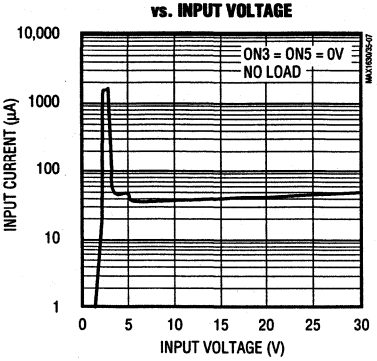
PWM MODE INPUT CURRENT vs. INPUT VOLTAGE



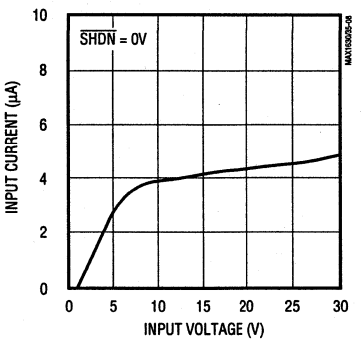
IDLE MODE INPUT CURRENT vs. INPUT VOLTAGE



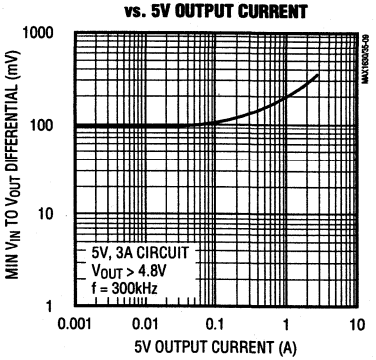
STANDBY INPUT CURRENT vs. INPUT VOLTAGE



SHUTDOWN INPUT CURRENT vs. INPUT VOLTAGE



MINIMUM V_{IN} TO V_{OUT} DIFFERENTIAL vs. 5V OUTPUT CURRENT

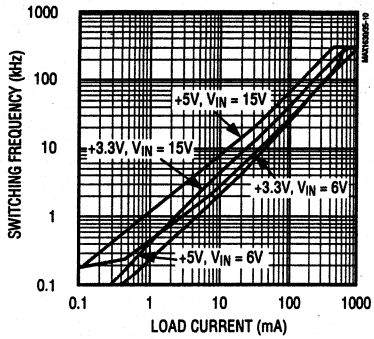


Multi-Output, Low-Noise Power-Supply Controllers for Notebook Computers

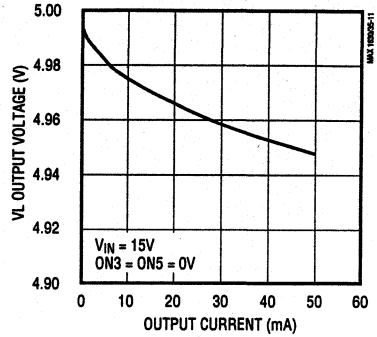
Typical Operating Characteristics (continued)

(Circuit of Figure 1, 3A Table 1 components, T_A = +25°C, unless otherwise noted.)

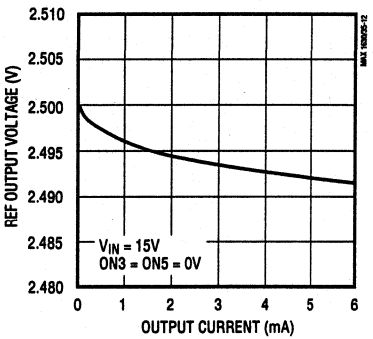
SWITCHING FREQUENCY vs. LOAD CURRENT



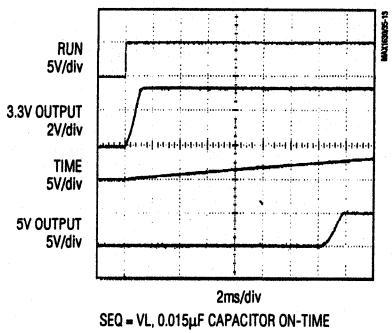
VL REGULATOR OUTPUT VOLTAGE vs. OUTPUT CURRENT



REF OUTPUT VOLTAGE vs. OUTPUT CURRENT



START-UP WAVEFORMS



Pin Description

PIN	NAME	FUNCTION
1	CSH3	Current-Sense Input for the 3.3V SMPS. Current-limit level is 100mV referred to CSL3.
2	CSL3	Current-Sense Input. Also serves as the feedback input in fixed-output mode.
3	FB3	Feedback Input for the 3.3V SMPS; regulates at FB3 = REF (approx. 2.5V) in adjustable mode. FB3 is a Dual Mode input that also selects the 3.3V fixed output voltage setting when tied to GND. Connect FB3 to a resistor divider for adjustable-output mode.
4	12OUT (MAX1630/ 32/33/35)	12V/120mA Linear Regulator Output. Input supply comes from V_{DD}. Bypass 12OUT to GND with 1µF minimum.
	STEER (MAX1631/ MAX1634)	Logic-Control Input for secondary feedback. Selects the PWM that uses a transformer and secondary feedback signal (SECFB): STEER = GND: 3.3V SMPS uses transformer STEER = VL: 5V SMPS uses transformer

Pin Description (continued)

PIN	NAME	FUNCTION
5	V_{DD} (MAX1630/32/33/35)	Supply Voltage Input for the 12OUT Linear Regulator. Also connects to an internal resistor divider for secondary winding feedback, and to an 18V overvoltage shunt regulator clamp.
	SECFB (MAX1631/MAX1634)	Secondary Winding Feedback Input. Normally connected to a resistor divider from an auxiliary output. SECFB regulates at V_{SECFB} = 2.5V (see *Secondary Feedback Regulation Loop* section). Tie to VL if not used.
6	SYNC	Oscillator Synchronization and Frequency Select. Tie to VL for 300kHz operation; tie to GND for 200kHz operation. Can be driven at 240kHz to 350kHz for external synchronization.
7	TIME/ON5	Dual-Purpose Timing Capacitor Pin and ON/$\overline{OFF}$ Control Input. See *Power-Up Sequencing and ON/$\overline{OFF}$ Controls* section.
8	GND	Low-Noise Analog Ground and Feedback Reference Point
9	REF	2.5V Reference Voltage Output. Bypass to GND with 1µF minimum.
10	$\overline{SKIP}$	Logic-Control Input that disables Idle Mode when high. Connect to GND for normal use.
11	$\overline{RESET}$	Active-Low Timed Reset Output. $\overline{RESET}$ swings GND to VL. Goes high after a fixed 32,000 clock-cycle delay following power-up.
12	FB5	Feedback Input for the 5V SMPS; regulates at FB5 = REF (approx. 2.5V) in adjustable mode. FB5 is a Dual Mode input that also selects the 5V fixed output voltage setting when tied to GND. Connect FB5 to a resistor divider for adjustable-output mode.
13	CSL5	Current-Sense Input for the 5V SMPS. Also serves as the feedback input in fixed-output mode, and as the bootstrap supply input when the voltage on CSL5/VL is > 4.5V.
14	CSH5	Current-Sense Input for the 5V SMPS. Current-limit level is 100mV referred to CSL5.
15	SEQ	Pin-Strap Input that selects the SMPS power-up sequence: SEQ = GND: 5V before 3.3V, $\overline{RESET}$ output determined by both outputs SEQ = REF: Separate ON3/ON5 controls, $\overline{RESET}$ output determined by 3.3V output SEQ = VL: 3.3V before 5V, $\overline{RESET}$ output determined by both outputs
16	DH5	Gate-Drive Output for the 5V, high-side N-channel switch. DH5 is a floating driver output that swings from LX5 to BST5, riding on the LX5 switching node voltage.
17	LX5	Switching Node (inductor) Connection. Can swing 2V below ground without hazard.
18	BST5	Boost capacitor connection for high-side gate drive (0.1µF)
19	DL5	Gate-Drive Output for the low-side synchronous-rectifier MOSFET. Swings 0V to VL.
20	PGND	Power Ground
21	VL	5V Internal Linear-Regulator Output. VL is also the supply voltage rail for the chip. After the 5V SMPS output has reached +4.5V (typical), VL automatically switches to the output voltage via CSL5 for boot-strapping. Bypass to GND with 4.7µF. VL supplies up to 25mA for external loads.
22	V+	Battery Voltage Input, +4.2V to +30V. Bypass V+ to PGND close to the IC with a 0.22µF capacitor. Connects to a linear regulator that powers VL.
23	$\overline{SHDN}$	Shutdown Control Input, active low. Logic threshold is set at approximately 1V. For automatic start-up, connect $\overline{SHDN}$ to V+ through a 220kΩ resistor and bypass $\overline{SHDN}$ to GND with a 0.01µF capacitor.
24	DL3	Gate-Drive Output for the low-side synchronous-rectifier MOSFET. Swings 0V to VL.
25	BST3	Boost Capacitor Connection for high-side gate drive (0.1µF)
26	LX3	Switching Node (inductor) Connection. Can swing 2V below ground without hazard.
27	DH3	Gate-Drive Output for the 3.3V, high-side N-channel switch. DH3 is a floating driver output that swings from LX3 to BST3, riding on the LX3 switching node voltage.
28	RUN/ON3	ON/$\overline{OFF}$ Control Input. See *Power-Up Sequencing and ON/$\overline{OFF}$ Controls* section.

Multi-Output, Low-Noise Power-Supply Controllers for Notebook Computers

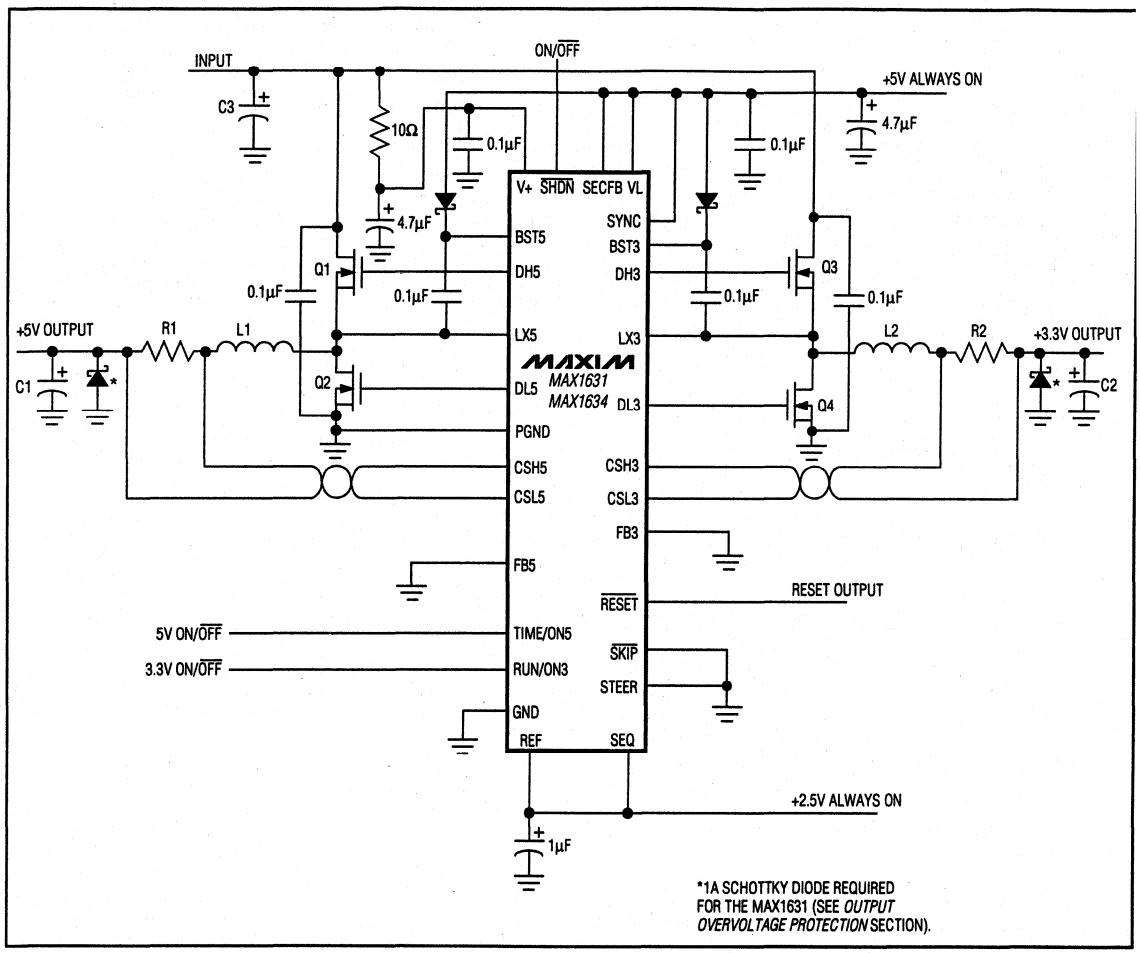


Figure 1. Standard 3.3V/5V Application Circuit (MAX1631/MAX1634)

Standard Application Circuit

The basic MAX1631/MAX1634 dual-output 3.3V/5V buck converter (Figure 1) is easily adapted to meet a wide range of applications with inputs up to 28V by substituting components from Table 1. These circuits represent a good set of tradeoffs between cost, size, and efficiency, while staying within the worst-case specification limits for stress-related parameters, such as capacitor ripple current. Don't change the frequency of these circuits without first recalculating component values (particularly inductance value at maximum battery voltage). Adding a Schottky rectifier across each synchronous rectifier improves the efficiency of these circuits by approximately 1%, but this rectifier is otherwise not needed because the MOSFETs required for these circuits typically incorporate a high-speed silicon diode from drain to source. Use a Schottky rectifier rated at a DC current equal to at least one-third of the load current.

Table 1. Component Selection for Standard 3.3V/5V Application

COMPONENT	LOAD CURRENT		
	2A	3A	4A
Input Range	4.75V to 18V	4.75V to 28V	4.75V to 24V
Application	PDA	Notebook	Workstation
Frequency	300kHz	300kHz	200kHz
Q1, Q3 High-Side MOSFETs	1/2 IR IRF7301; 1/2 Siliconix Si9925DQ; or 1/2 Motorola MMDF3N03HD or MMDF4N01HD (10V max)	IR IRF7403 or IRF7401 (18V max); Siliconix Si4412DY; or Motorola MMSF5N03HD or MMSF5N02HD (18V max)	IR IRF7413 or Siliconix Si4410DY
Q2, Q4 Low-Side MOSFETs	1/2 IR IRF7301; 1/2 Siliconix Si9925DQ; or 1/2 Motorola MMDF3N03HD or MMDF4N01HD (10V max)	IR IRF7403 or IRF7401 (18V max); Siliconix Si4412DY; or Motorola MMSF5N03HD or MMSF5N02HD (18V max)	IR IRF7413 or Siliconix Si4410DY
C1 Input Capacitor	10µF, 30V Sanyo OS-CON; 22µF, 35V AVX TPS; or Sprague 594D	2 x 10µF, 30V Sanyo OS-CON; 2 x 22µF, 35V AVX TPS; or Sprague 594D	3 x 10µF, 30V Sanyo OS-CON; 4 x 22µF, 35V AVX TPS; or Sprague 595D
C2 Output Capacitor	220µF, 10V AVX TPS or Sprague 595D	2 x 220µF, 10V AVX TPS or Sprague 595D	4 x 220µF, 10V AVX TPS or Sprague 595D
R1, R2 Resistors	0.033Ω IRC LR2010-01-R033 or Dale WSL2010-R033-F	0.02Ω IRC LR2010-01-R020 or Dale WSL2010-R020-F	0.012Ω Dale WSL2512-R012-F
L1 Inductor	15µH, 2.4A Ferrite Coilcraft DO3316P-153 or Sumida CDRH125-150	10µH, 4A Ferrite Coilcraft DO3316P-103 or Sumida CDRH125-100	4.7µH, 5.5A Ferrite Coilcraft DO3316-472 or 5.2µH, 6.5A Ferrite Sumida CDRH127-5R2MC

Table 2. Component Suppliers

COMPANY	FACTORY FAX (COUNTRY CODE)	USA PHONE
AVX	(1) 803-626-3123	(803) 946-0690
Central Semiconductor	(1) 516-435-1824	(516) 435-1110
Coilcraft	(1) 847-639-1469	(847) 639-6400
Coiltronics	(1) 561-241-9339	(561) 241-7876
Dale	(1) 605-665-1627	(605) 668-4131
International Rectifier (IR)	(1) 310-322-3332	(310) 322-3331
IRC	(1) (512) 992-3377	(512) 992-7900
Matsuo	(1) 714-960-6492	(714) 969-2491

COMPANY	FACTORY FAX (COUNTRY CODE)	USA PHONE
Motorola	(1) 602-994-6430	(602) 303-5454
Murata-Erie	(1) 814 238-0490	(814) 237-1431
NIEC	(81) 3-3494-7414	(805) 867-2555*
Sanyo	(81) 7-2070-1174	(619) 661-6835
Siliconix	(1) 408-970-3950	(408) 988-8000
Sprague	(1) (603) 224-1430	(603) 224-1961
Sumida	(81) 3-3607-5144	(847) 956-0666
TDK	(847) 390-4428	(847) 390-4373
Transpower Technologies	(1) 702-831-3521	(702) 831-0140

**Distributor*

Multi-Output, Low-Noise Power-Supply Controllers for Notebook Computers

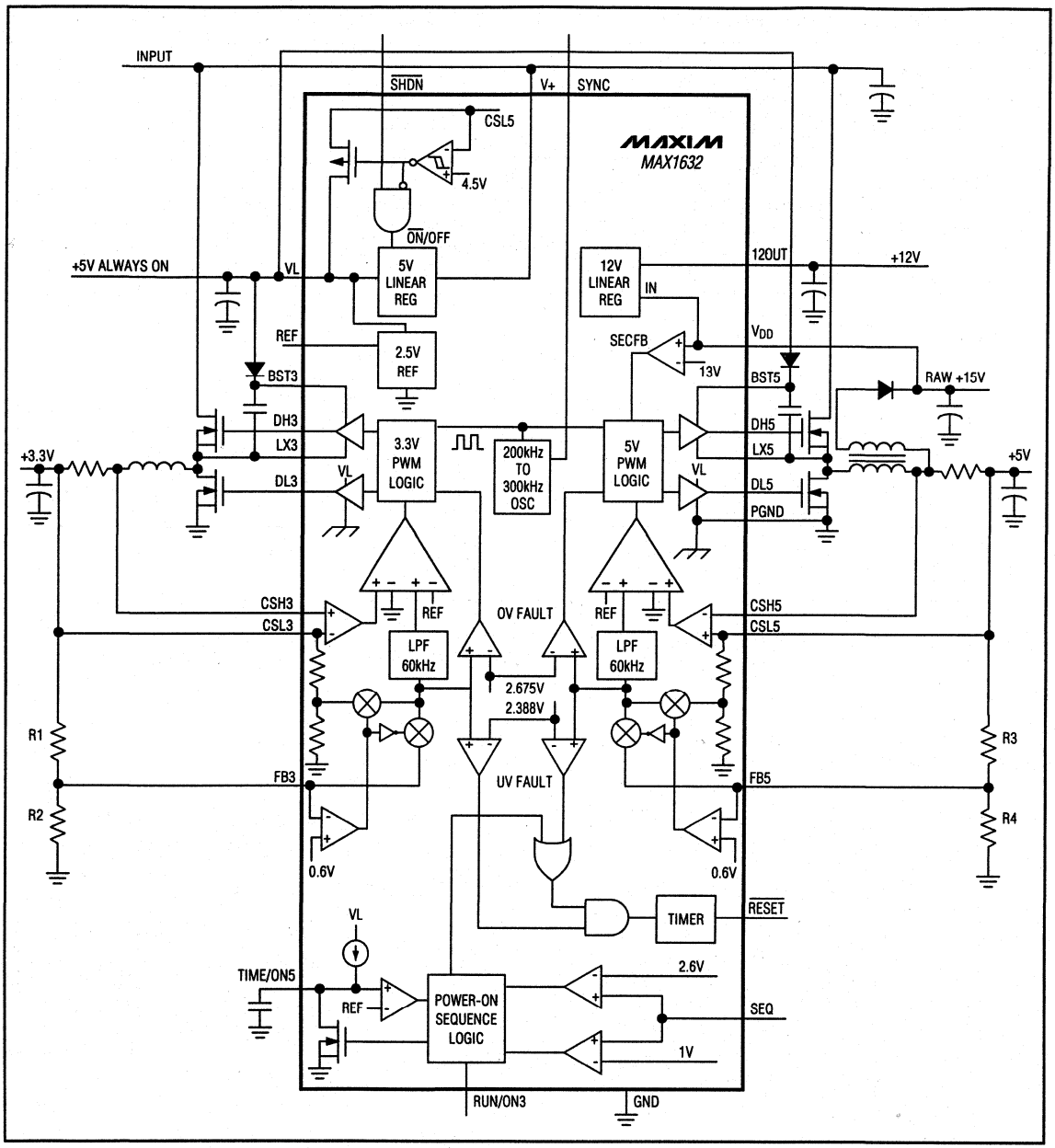


Figure 2. MAX1632 Block Diagram

Multi-Output, Low-Noise Power-Supply Controllers for Notebook Computers

Detailed Description

The MAX1630 is a dual, BiCMOS, switch-mode power-supply controller designed primarily for buck-topology regulators in battery-powered applications where high efficiency and low quiescent supply current are critical. Light-load efficiency is enhanced by automatic Idle Mode™ operation, a variable-frequency pulse-skipping mode that reduces transition and gate-charge losses. Each step-down, power-switching circuit consists of two N-channel MOSFETs, a rectifier, and an LC output filter. The output voltage is the average AC voltage at the switching node, which is regulated by changing the duty cycle of the MOSFET switches. The gate-drive signal to the N-channel high-side MOSFET must exceed the battery voltage, and is provided by a flying-capacitor boost circuit that uses a 100nF capacitor connected to BST_.

Devices in the MAX1630 family contain ten major circuit blocks (Figure 2).

The two pulse-width modulation (PWM) controllers each consist of a Dual Mode™ feedback network and multiplexer, a multi-input PWM comparator, high-side and low-side gate drivers, and logic. MAX1630/MAX1631/MAX1632 contain fault-protection circuits that monitor the main PWM outputs for undervoltage and overvoltage. A power-on sequence block controls the power-up timing of the main PWMs and determines whether one or both of the outputs are monitored for undervoltage faults. The MAX1630/MAX1632/MAX1633/MAX1635 include a secondary feedback network and 12V linear regulator to generate a 12V output from a coupled-inductor flyback winding. The MAX1631/MAX1634 have a secondary feedback input (SECFB) instead, which allows a quasi-regulated, adjustable-output, coupled-inductor flyback winding to be attached to either the 3.3V or the 5V main inductor. Bias generator blocks include the 5V IC internal rail (VL) linear regulator, 2.5V precision reference, and automatic bootstrap switchover circuit. The PWMs share a common 200kHz/300kHz synchronizable oscillator.

These internal IC blocks aren't powered directly from the battery. Instead, the 5V VL linear regulator steps down the battery voltage to supply both VL and the gate drivers. The synchronous-switch gate drivers are directly powered from VL, while the high-side switch gate drivers are indirectly powered from VL via an external diode-capacitor boost circuit. An automatic bootstrap circuit turns off the +5V linear regulator and powers the IC from the 5V PWM output voltage if the output is above 4.5V.

PWM Controller Block

The two PWM controllers are nearly identical. The only differences are fixed output settings (3.3V vs. 5V), the VL/CSL5 bootstrap switch connected to the +5V PWM, and SECFB. The heart of each current-mode PWM controller is a multi-input, open-loop comparator that sums three signals: the output voltage error signal with respect to the reference voltage, the current-sense signal, and the slope compensation ramp (Figure 3). The PWM controller is a direct-summing type, lacking a traditional error amplifier and the phase shift associated with it. This direct-summing configuration approaches ideal cycle-by-cycle control over the output voltage.

When $\overline{SKIP}$ = low, Idle Mode circuitry automatically optimizes efficiency throughout the load current range. Idle Mode dramatically improves light-load efficiency by reducing the effective frequency, which reduces switching losses. It keeps the peak inductor current above 25% of the full current limit in an active cycle, allowing subsequent cycles to be skipped. Idle Mode transitions seamlessly to fixed-frequency PWM operation as load current increases.

With $\overline{SKIP}$ = high, the controller always operates in fixed-frequency PWM mode for lowest noise. Each pulse from the oscillator sets the main PWM latch that turns on the high-side switch for a period determined by the duty factor (approximately V_{OUT}/V_{IN}). As the high-side switch turns off, the synchronous rectifier latch sets; 60ns later, the low-side switch turns on. The low-side switch stays on until the beginning of the next clock cycle.

Table 3. $\overline{SKIP}$ PWM Table

$\overline{SKIP}$	LOAD CURRENT	MODE	DESCRIPTION
Low	Light	Idle	Pulse-skipping, supply current = 250µA at V_{IN} = 12V, discontinuous inductor current
Low	Heavy	PWM	Constant-frequency PWM, continuous inductor current
High	Light	PWM	Constant-frequency PWM, continuous inductor current
High	Heavy	PWM	Constant-frequency PWM, continuous inductor current

Multi-Output, Low-Noise Power-Supply Controllers for Notebook Computers

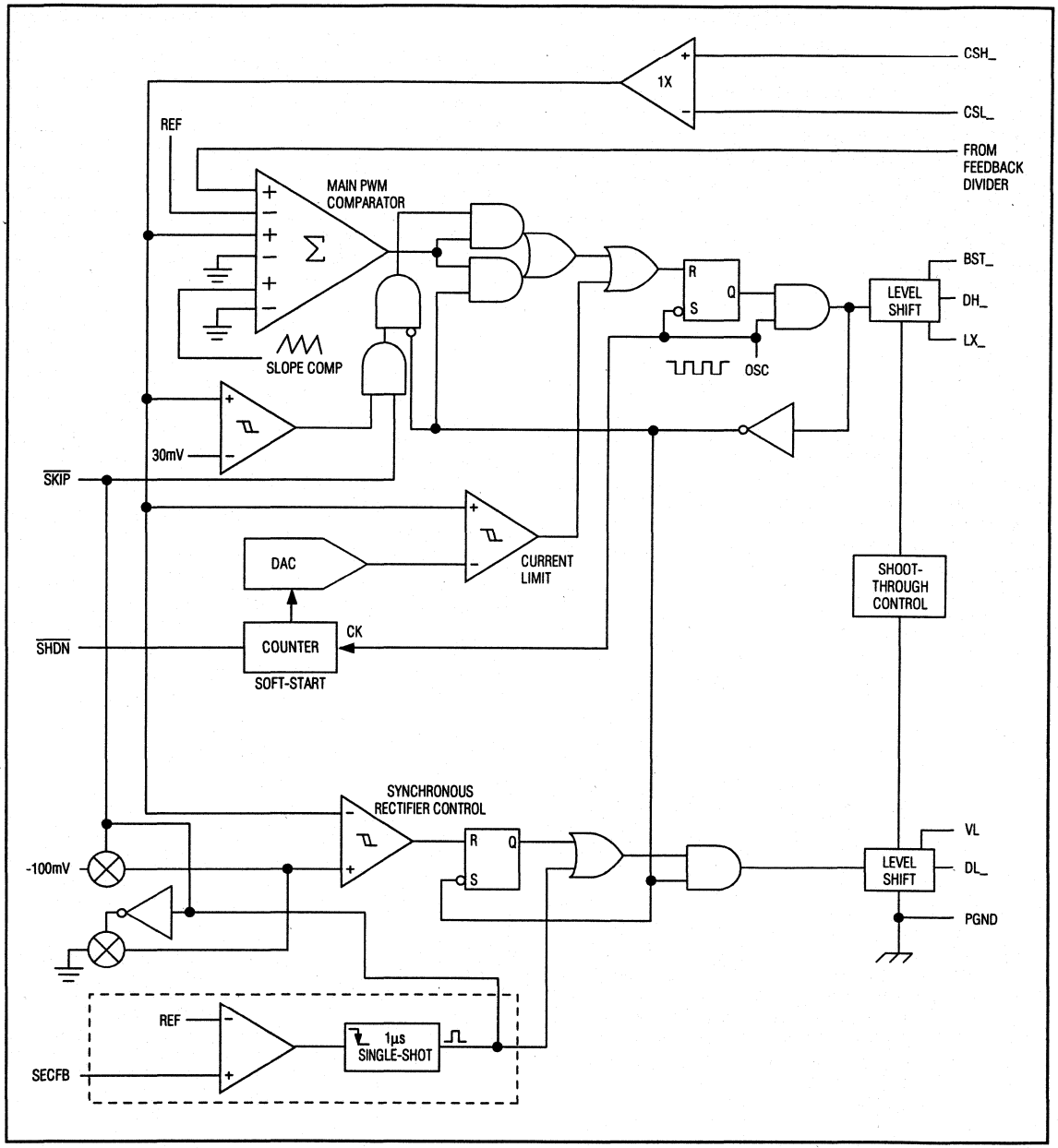


Figure 3. PWM Controller Detailed Block Diagram

In PWM mode, the controller operates as a fixed-frequency current-mode controller where the duty ratio is set by the input/output voltage ratio. The current-mode feedback system regulates the peak inductor current value as a function of the output-voltage error signal. In continuous-conduction mode, the average inductor current is nearly the same as the peak current, so the circuit acts as a switch-mode transconductance amplifier. This pushes the second output LC filter pole, normally found in a duty-factor-controlled (voltage-mode) PWM, to a higher frequency. To preserve inner-loop stability and eliminate regenerative inductor current "staircasing," a slope compensation ramp is summed into the main PWM comparator to make the apparent duty factor less than 50%.

The MAX1630 family uses a relatively low loop gain, allowing the use of lower-cost output capacitors. The relative gains of the voltage-sense and current-sense inputs are weighted by the values of current sources that bias three differential input stages in the main PWM comparator (Figure 4). The relative gain of the voltage comparator to the current comparator is internally fixed at K = 2:1. The low loop gain results in the 2% typical load-regulation error. The low value of loop gain helps reduce output filter capacitor size and cost by shifting the unity-gain crossover frequency to a lower level.

The output filter capacitors (C1 and C2) set a dominant pole in the feedback loop that must roll off the loop gain to unity before encountering the zero introduced by the output capacitor's parasitic resistance (ESR) (see *Design Procedure* section). A 60kHz pole-zero cancellation filter provides additional rolloff above the unity-gain crossover. This internal 60kHz lowpass compensation filter cancels the zero due to filter capacitor ESR. The 60kHz filter is included in the loop in both fixed-output and adjustable-output modes.

Synchronous Rectifier Driver (DL)

Synchronous rectification reduces conduction losses in the rectifier by shunting the normal Schottky catch diode with a low-resistance MOSFET switch. Also, the synchronous rectifier ensures proper start-up of the boost gate-driver circuit. If the synchronous power MOSFETs are omitted for cost or other reasons, replace them with a small-signal MOSFET, such as a 2N7002.

If the circuit is operating in continuous-conduction mode, the DL drive waveform is simply the complement of the DH high-side drive waveform (with controlled dead time to prevent cross-conduction or "shoot-through"). In discontinuous (light-load) mode, the synchronous switch is turned off as the inductor current falls through zero. The synchronous rectifier works

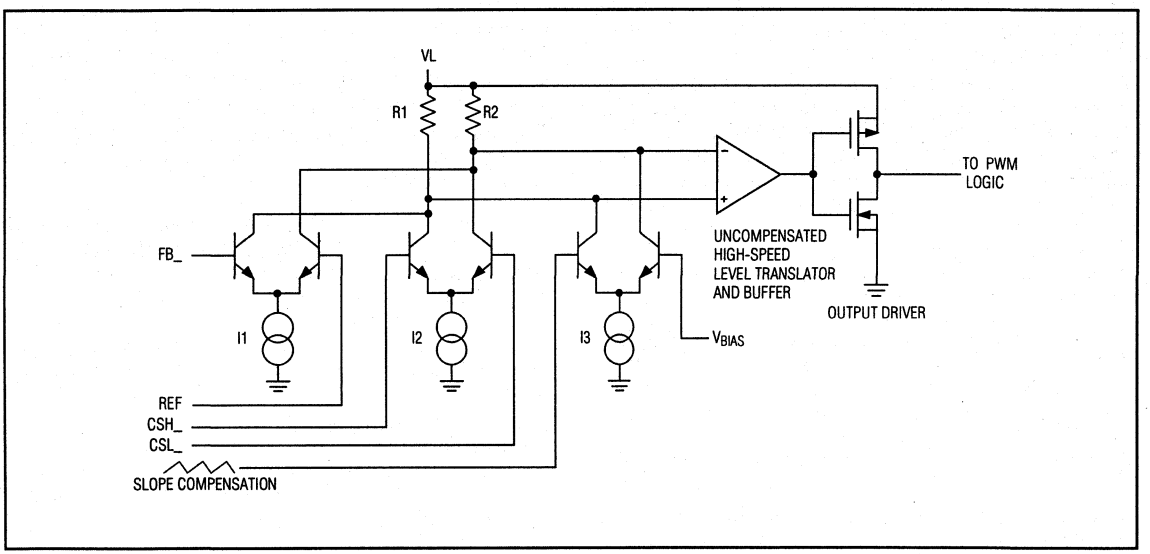


Figure 4. Main PWM Comparator Block Diagram

Multi-Output, Low-Noise Power-Supply Controllers for Notebook Computers

under all operating conditions, including Idle Mode. The SECFB signal further controls the synchronous switch timing in order to improve multiple-output cross-regulation (see *Secondary Feedback Regulation Loop* section).

Internal VL and REF Supplies

An internal regulator produces the +5V supply (VL) that powers the PWM controller, logic, reference, and other blocks within the IC. This 5V low-dropout linear regulator supplies up to 25mA for external loads, with a reserve of 25mA for supplying gate-drive power. Bypass VL to GND with 4.7µF.

Important: Ensure that VL does not exceed 6V. Measure VL with the main output fully loaded. If it is pumped above 5.5V, either excessive boost diode capacitance or excessive ripple at V+ is the probable cause. Use only small-signal diodes for the boost circuit (10mA to 100mA Schottky or 1N4148 are preferred), and bypass V+ to PGND with 4.7µF directly at the package pins.

The 2.5V reference (REF) is accurate to ±2% over temperature, making REF useful as a precision system reference. Bypass REF to GND with 1µF minimum. REF can supply up to 5mA for external loads. (Bypass REF with a minimum 1µF/mA reference load current.) However, if extremely accurate specifications for both the main output voltages and REF are essential, avoid loading REF more than 100µA. Loading REF reduces the main output voltage slightly, because of the reference load-regulation error.

When the 5V main output voltage is above 4.5V, an internal P-channel MOSFET switch connects CSL5 to VL, while simultaneously shutting down the VL linear regulator. This action bootstraps the IC, powering the internal circuitry from the output voltage, rather than through a linear regulator from the battery. Bootstrapping reduces power dissipation due to gate charge and quiescent losses by providing that power from a 90%-efficient switch-mode source, rather than from a much less efficient linear regulator.

Boost High-Side Gate-Drive Supply (BST3 and BST5)

Gate-drive voltage for the high-side N-channel switches is generated by a flying-capacitor boost circuit (Figure 2). The capacitor between BST_ and LX_ is alternately charged from the VL supply and placed parallel to the high-side MOSFET's gate-source terminals.

On start-up, the synchronous rectifier (low-side MOSFET) forces LX_ to 0V and charges the boost capacitors to 5V. On the second half-cycle, the SMPS turns on the high-side MOSFET by closing an internal switch between BST_ and DH_. This provides the necessary enhancement voltage to turn on the high-side switch, an action that "boosts" the 5V gate-drive signal above the battery voltage.

Ringing at the high-side MOSFET gate (DH3 and DH5) in discontinuous-conduction mode (light loads) is a natural operating condition. It is caused by residual energy in the tank circuit, formed by the inductor and stray capacitance at the switching node, LX. The gate-drive negative rail is referred to LX, so any ringing there is directly coupled to the gate-drive output.

Current-Limiting and Current-Sense Inputs (CSH and CSL)

The current-limit circuit resets the main PWM latch and turns off the high-side MOSFET switch whenever the voltage difference between CSH and CSL exceeds 100mV. This limiting is effective for both current flow directions, putting the threshold limit at ±100mV. The tolerance on the positive current limit is ±20%, so the external low-value sense resistor (R1) must be sized for 80mV/I_{PEAK}, where I_{PEAK} is the required peak inductor current to support the full load current, while components must be designed to withstand continuous current stresses of 120mV/R1.

For breadboarding or for very-high-current applications, it may be useful to wire the current-sense inputs with a twisted pair, rather than PC traces. (This twisted pair needn't be anything special; two pieces of wire-wrap wire twisted together are sufficient.) This reduces the possible noise picked up at CSH_ and CSL_, which can cause unstable switching and reduced output current.

The CSL5 input also serves as the IC's bootstrap supply input. Whenever V_{CSL5} > 4.5V, an internal switch connects CSL5 to VL.

Oscillator Frequency and Synchronization (SYNC)

The SYNC input controls the oscillator frequency. Low selects 200kHz; high selects 300kHz. SYNC can also be used to synchronize with an external 5V CMOS or TTL clock generator. SYNC has a guaranteed 240kHz to 350kHz capture range. A high-to-low transition on SYNC initiates a new cycle.

300kHz operation optimizes the application circuit for component size and cost. 200kHz operation provides increased efficiency, lower dropout, and improved load-transient response at low input-output voltage differences (see *Low-Voltage Operation* section).

Multi-Output, Low-Noise Power-Supply Controllers for Notebook Computers

Shutdown Mode

Holding $\overline{SHDN}$ low puts the IC into its 4µA shutdown mode. $\overline{SHDN}$ is logic input with a threshold of about 1V (the V_{TH} of an internal N-channel MOSFET). For automatic start-up, bypass $\overline{SHDN}$ to GND with a 0.01µF capacitor and connect it to V+ through a 220kΩ resistor.

Power-Up Sequencing and ON/OFF Controls

Start-up is controlled by RUN/ON3 and TIME/ON5 in conjunction with SEQ. With SEQ tied to REF, the two control inputs act as separate ON/$\overline{OFF}$ controls for each supply. With SEQ tied to VL or GND, RUN/ON3 becomes the master ON/$\overline{OFF}$ control input and TIME/ON5 becomes a timing pin, with the delay between the two supplies determined by an external capacitor. The delay is approximately 800µs/nF. The +3.3V supply powers-up first if SEQ is tied to VL, and the +5V supply is first if SEQ is tied to GND. When driving TIME/ON5 as a control input with external logic, always place a resistor (>1kΩ) in series with the input. This prevents possible crowbar current due to the internal discharge pull-down transistor, which turns on in standby mode and momentarily at the first power-up or in shutdown mode.

$\overline{RESET}$ Power-Good Voltage Monitor

The power-good monitor generates a system $\overline{RESET}$ signal. At first power-up, $\overline{RESET}$ is held low until both the 3.3V and 5V SMPS outputs are in regulation. At this point, an internal timer begins counting oscillator pulses, and $\overline{RESET}$ continues to be held low until 32,000 cycles have elapsed. After this timeout period (107ms at 300kHz or 160ms at 200kHz), $\overline{RESET}$ is actively pulled up to VL. If SEQ is tied to REF (for separate ON3/ON5 controls), only the 3.3V SMPS is monitored—the 5V SMPS is ignored.

Output Undervoltage Shutdown Protection (MAX1630/MAX1631/MAX1632)

The output undervoltage lockout circuit is similar to foldback current limiting, but employs a timer rather than a variable current limit. Each SMPS has an undervoltage protection circuit that is activated 6144 clock cycles after the SMPS is enabled. If either SMPS output is under 70% of the nominal value, both SMPSs are latched off and won't restart until $\overline{SHDN}$ or RUN/ON3 is toggled, or until V+ power is cycled below 1V. Note that undervoltage protection can make prototype troubleshooting difficult, since you have only 20ms or 30ms to figure out what might be wrong with the circuit before both SMPSs are latched off. In extreme cases, it may be useful to substitute the MAX1633/MAX1634/MAX1635 into the prototype breadboard until the prototype is working properly.

Output Overvoltage Protection (MAX1630/MAX1631/MAX1632)

Both SMPS outputs are monitored for overvoltage. If either output is more than 7% above the nominal regulation point, both low-side gate drivers (DL_) are latched high until $\overline{SHDN}$ or RUN/ON3 is toggled, or until V+ power is cycled below 1V. This action turns on the synchronous rectifiers with 100% duty, in turn rapidly discharging the output capacitors and forcing both SMPS outputs to ground. The DL outputs are also kept high whenever the corresponding SMPS is disabled, and in shutdown if VL is sustained.

Table 4. Operating Modes

$\overline{SHDN}$	SEQ	RUN/ON3	TIME/ON5	MODE	DESCRIPTION
Low	X	X	X	Shutdown	All circuit blocks turned off. Supply current = 4µA.
High	Ref	Low	Low	Standby	Both SMPSs off. Supply current = 30µA.
High	Ref	High	Low	Run	3.3V SMPS enabled/5V off
High	Ref	Low	High	Run	5V SMPS enabled/3.3V off
High	Ref	High	High	Run	Both SMPSs enabled
High	GND	Low	Timing capacitor	Standby	Both SMPSs off. Supply current = 30µA.
High	GND	High	Timing capacitor	Run	Both SMPSs enabled. 5V enabled before 3.3V.
High	VL	Low	Timing capacitor	Standby	Both SMPSs off. Supply current = 30µA.
High	VL	High	Timing capacitor	Run	Both SMPSs enabled. 3.3V enabled before 5V.

X = Don't Care

Multi-Output, Low-Noise Power-Supply Controllers for Notebook Computers

Discharging the output capacitor through the main inductor causes the output to momentarily go below GND. Clamp this negative pulse with a back-biased 1A Schottky diode across the output capacitor (Figure 1).

To ensure overvoltage protection on initial power-up, connect signal diodes from both output voltages to VL (cathodes to VL) to eliminate the VL power-up delay. This circuitry protects the load from accidental overvoltage caused by a short-circuit across the high-side power MOSFETs. This scheme relies on the presence of a fuse, in series with the battery, which is blown by the resulting crowbar current. Note that the overvoltage circuitry will interfere with external keep-alive supplies that hold up the outputs (such as lithium backup or hot-swap power supplies); in such cases, the MAX1633, MAX1634, or MAX1635 should be used.

Low-Noise Operation (PWM Mode)

PWM mode ($\overline{SKIP}$ = high) minimizes RF and audio interference in noise-sensitive applications (such as hi-fi multimedia-equipped systems), cellular phones, RF communicating computers, and electromagnetic pen-entry systems. See the summary of operating modes in Table 2. $\overline{SKIP}$ can be driven from an external logic signal.

Interference due to switching noise is reduced in PWM mode by ensuring a constant switching frequency, thus concentrating the emissions at a known frequency outside the system audio or IF bands. Choose an oscillator frequency for which switching frequency harmonics don't overlap a sensitive frequency band. If necessary, synchronize the oscillator to a tight-tolerance external clock generator. To extend the output-voltage-regulation range, constant operating frequency is not maintained under overload or dropout conditions (see *Overload and Dropout Operation* section.)

PWM mode ($\overline{SKIP}$ = high) forces two changes upon the PWM controllers. First, it disables the minimum-current comparator, ensuring fixed-frequency operation. Second, it changes the detection threshold for reverse-current limit from 0mV to -100mV, allowing the inductor current to reverse at light loads. This results in fixed-frequency operation and continuous inductor-current flow. This eliminates discontinuous-mode inductor ringing and improves cross regulation of transformer-coupled multiple-output supplies, particularly in circuits that don't use additional secondary regulation via SECFB or V_{DD}.

In most applications, tie $\overline{SKIP}$ to GND to minimize quiescent supply current. VL supply current with $\overline{SKIP}$ high is typically 20mA, depending on external MOSFET gate capacitance and switching losses.

Internal Digital Soft-Start Circuit

Soft-start allows a gradual increase of the internal current-limit level at start-up to reduce input surge currents. Both SMPSs contain internal digital soft-start circuits, each controlled by a counter, a digital-to-analog converter (DAC), and a current-limit comparator. In shutdown or standby mode, the soft-start counter is reset to zero. When an SMPS is enabled, its counter starts counting oscillator pulses, and the DAC begins incrementing the comparison voltage applied to the current-limit comparator. The DAC output increases from 0mV to 100mV in five equal steps as the count increases to 512 clocks. As a result, the main output capacitor charges up relatively slowly. The exact time of the output rise depends on output capacitance and load current, and is typically 1ms with a 300kHz oscillator.

Dropout Operation

Dropout (low input-output differential operation) is enhanced by stretching the clock pulse width to increase the maximum duty factor. The algorithm follows: If the output voltage (V_{OUT}) drops out of regulation without the current limit having been reached, the SMPS skips an off-time period (extending the on-time). At the end of the cycle, if the output is still out of regulation, the SMPS skips another off-time period. This action can continue until three off-time periods are skipped, effectively dividing the clock frequency by as much as four.

The typical PWM minimum off-time is 300ns, regardless of the operating frequency. Lowering the operating frequency raises the maximum duty factor above 98%.

Adjustable-Output Feedback (Dual Mode FB)

Fixed, preset output voltages are selected when FB_ is connected to ground. Adjusting the main output voltage with external resistors is simple for any of the MAX1630 family ICs, through resistor dividers connected to FB3 and FB5 (Figure 2). Calculate the output voltage with the following formula:

$$V_{OUT} = V_{REF} (1 + R1 / R2)$$

where V_{REF} = 2.5V nominal.

The nominal output should be set approximately 1% or 2% high to make up for the MAX1630's -2% typical load-regulation error. For example, if designing for a 3.0V output, use a resistor ratio that results in a nominal output voltage of 3.05V. This slight offsetting gives the best possible accuracy. Recommended normal values for R2 range from 5kΩ to 100kΩ. To achieve a 2.5V nominal output, simply connect FB_ directly to CSL_.

Remote output-voltage sensing, while not possible in fixed-output mode due to the combined nature of the voltage-sense and current-sense inputs (CSL3 and CSL5), is easy to do in adjustable mode by using the top of the external resistor divider as the remote sense point.

When using adjustable mode, it is a good idea to always set the "3.3V output" to a lower voltage than the "5V output." The 3.3V output must always be less than VL, so that the voltage on CSH3 and CSL3 is within the common-mode range of the current-sense inputs. While VL is nominally 5V, it can be as low as 4.7V when linearly regulating, and as low as 4.2V when automatically bootstrapped to CSH5.

Secondary Feedback Regulation Loop (SECFB or VDD)

A flyback-winding control loop regulates a secondary winding output, improving cross-regulation when the primary output is lightly loaded or when there is a low input-output differential voltage. If VDD or SECFB falls below its regulation threshold, the low-side switch is turned on for an extra 1µs. This reverses the inductor (primary) current, pulling current from the output filter capacitor and causing the flyback transformer to operate in forward mode. The low impedance presented by the transformer secondary in forward mode dumps current into the secondary output, charging up the secondary capacitor and bringing VDD or SECFB back into regulation. The secondary feedback loop does not improve secondary output accuracy in normal flyback mode, where the main (primary) output is heavily loaded. In this condition, secondary output accuracy is determined by the secondary rectifier drop, transformer turns ratio, and accuracy of the main output voltage. A linear post-regulator may still be needed to meet strict output-accuracy specifications.

Devices with a 12OUT linear regulator have a VDD pin that regulates at a fixed 13.5V, set by an internal resistor divider. The MAX1631/MAX1634 have an adjustable secondary output voltage set by an external resistor divider on SECFB (Figure 5). Ordinarily, the secondary regulation point is set 5% to 10% below the voltage normally produced by the flyback effect. For example, if the output voltage as determined by turns ratio is 15V, set the feedback resistor ratio to produce 13.5V. Otherwise, the SECFB one-shot might be triggered unintentionally, unnecessarily increasing supply current and output noise.

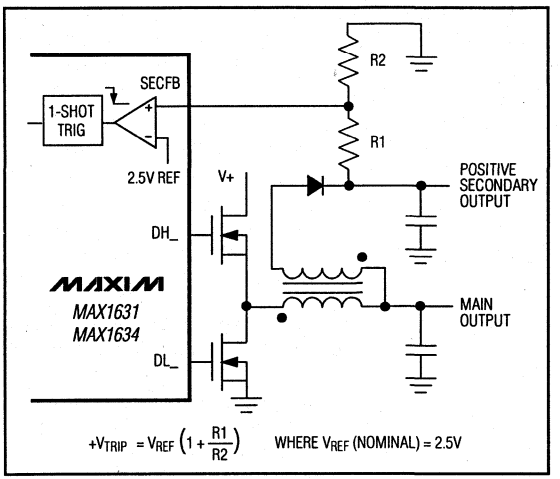


Figure 5. Adjusting the Secondary Output Voltage with SECFB

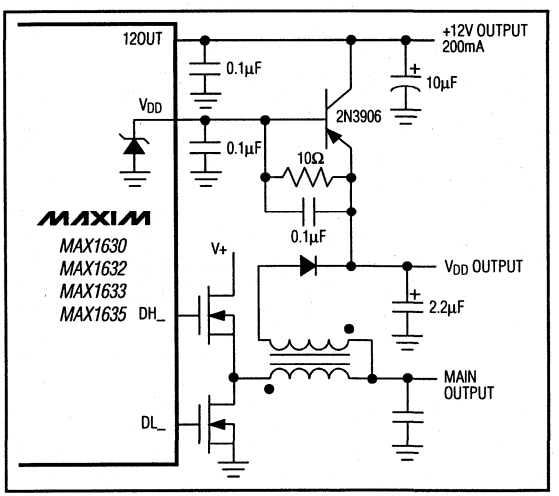


Figure 6. Increased 12V Linear Regulator Output Current

12V Linear Regulator Output (MAX1630/MAX1632/MAX1633/MAX1635)

The MAX1630/MAX1632/MAX1633/MAX1635 include a 12V linear regulator output capable of delivering 120mA of output current. Typically, greater current is available at the expense of output accuracy. If an accurate output of more than 120mA is needed, an external pass tran-

Multi-Output, Low-Noise Power-Supply Controllers for Notebook Computers

sistor can be added. Figure 6's circuit delivers more than 200mA. Total output current is constrained by the V+ input voltage and the transformer primary load (see Maximum 15V V_{DD} Output Current vs. Supply Voltage graphs in the *Typical Operating Characteristics*).

Design Procedure

The three predesigned 3V/5V standard application circuits (Figure 1 and Table 1) contain ready-to-use solutions for common application needs. Also, two standard flyback transformer circuits support the 12OUT linear regulator in the *Applications Information* section. Use the following design procedure to optimize these basic schematics for different voltage or current requirements. But before beginning a design, firmly establish the following:

Maximum input (battery) voltage, $V_{IN(MAX)}$. This value should include the worst-case conditions, such as no-load operation when a battery charger or AC adapter is connected but no battery is installed. $V_{IN(MAX)}$ must not exceed 30V.

Minimum input (battery) voltage, $V_{IN(MIN)}$. This should be taken at full load under the lowest battery conditions. If $V_{IN(MIN)}$ is less than 4.2V, use an external circuit to externally hold VL above the VL undervoltage lockout threshold. If the minimum input-output difference is less than 1.5V, the filter capacitance required to maintain good AC load regulation increases (see *Low-Voltage Operation* section).

Inductor Value

The exact inductor value isn't critical and can be freely adjusted to make trade-offs between size, cost, and efficiency. Lower inductor values minimize size and cost, but reduce efficiency due to higher peak-current levels. The smallest inductor is achieved by lowering the inductance until the circuit operates at the border between continuous and discontinuous mode. Further reducing the inductor value below this crossover point results in discontinuous-conduction operation even at full load. This helps lower output filter capacitance requirements, but efficiency suffers due to high I^2R losses. On the other hand, higher inductor values mean greater efficiency, but resistive losses due to extra wire turns will eventually exceed the benefit gained from lower peak-current levels. Also, high inductor values can affect load-transient response (see the V_{SAG} equation in the *Low-Voltage Operation* section). The equations that follow are for continuous-conduction operation, since the MAX1630 family is intended mainly for high-efficiency, battery-powered applications. See Appendix A in Maxim's *Battery Management and DC-DC Converter Circuit Collection* for crossover-point and discontinuous-mode equations. Discontinuous conduction doesn't affect normal Idle Mode operation.

Three key inductor parameters must be specified: inductance value (L), peak current (I_{PEAK}), and DC resistance (R_{DC}). The following equation includes a constant, LIR, which is the ratio of inductor peak-to-peak AC current to DC load current. A higher LIR value allows smaller inductance, but results in higher losses and higher ripple. A good compromise between size and losses is found at a 30% ripple-current to load-current ratio (LIR = 0.3), which corresponds to a peak inductor current 1.15 times higher than the DC load current.

$$L = \frac{V_{OUT}(V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f \times I_{OUT} \times LIR}$$

where: f = switching frequency, normally 200kHz or 300kHz

I_{OUT} = maximum DC load current

LIR = ratio of AC to DC inductor current, typically 0.3; should be selected for >0.15

The nominal peak inductor current at full load is 1.15 x I_{OUT} if the above equation is used; otherwise, the peak current can be calculated by:

$$I_{PEAK} = I_{LOAD} + \frac{V_{OUT}(V_{IN(MAX)} - V_{OUT})}{2 \times f \times L \times V_{IN(MAX)}}$$

The inductor's DC resistance should be low enough that $R_{DC} \times I_{PEAK} < 100mV$, as it is a key parameter for efficiency performance. If a standard off-the-shelf inductor is not available, choose a core with an LI^2 rating greater than $L \times I_{PEAK}2$ and wind it with the largest-diameter wire that fits the winding area. For 300kHz applications, ferrite core material is strongly preferred; for 200kHz applications, Kool-Mu® (aluminum alloy) or even powdered iron is acceptable. If light-load efficiency is unimportant (in desktop PC applications, for example), then low-permeability iron-powder cores, such as the Micrometals type found in Pulse Engineering's 2.1µH PE-53680, may be acceptable even at 300kHz. For high-current applications, shielded-core geometries, such as toroidal or pot core, help keep noise, EMI, and switching-waveform jitter low.

Kool-Mu is a registered trademark of Magnetics Div., Spang & Co.

Current-Sense Resistor Value

The current-sense resistor value is calculated according to the worst-case, low-current-limit threshold voltage (from the *Electrical Characteristics* table) and the peak inductor current:

$$R_{SENSE} = \frac{80mV}{I_{PEAK}}$$

Use I_{PEAK} from the second equation in the *Inductor Value* section

Use the calculated value of R_{SENSE} to size the MOSFET switches and specify inductor saturation-current ratings according to the worst-case high-current-limit threshold voltage:

$$I_{PEAK(MAX)} = \frac{120mV}{R_{SENSE}}$$

Low-inductance resistors, such as surface-mount metal-film, are recommended.

Input Capacitor Value

Connect low-ESR bulk capacitors and small ceramic capacitors (0.1µF) directly to the drains on the high-side MOSFETs. The bulk input filter capacitor is usually selected according to input ripple current requirements and voltage rating, rather than capacitor value. Electrolytic capacitors with low enough effective series resistance (ESR) to meet the ripple current requirement invariably have sufficient capacitance values. Aluminum electrolytic capacitors, such as Sanyo OS-CON or Nichicon PL, are superior to tantalum types, which carry the risk of power-up surge-current failure, especially when connecting to robust AC adapters or low-impedance batteries. RMS input ripple current (I_{RMS}) is determined by the input voltage and load current, with the worst case occurring at $V_{IN} = 2 \times V_{OUT}$:

$$I_{RMS} = I_{LOAD} \times \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

Therefore, when V_{IN} is $2 \times V_{OUT}$:

$$I_{RMS} = \frac{I_{LOAD}}{2}$$

Bypassing V+

Bypass the V+ input with a 4.7µF tantalum capacitor paralleled with a 0.1µF ceramic capacitor, close to the IC. A 10Ω series resistor to V_{IN} is also recommended.

Bypassing VL

Bypass the VL output with a 4.7µF tantalum capacitor paralleled with a 0.1µF ceramic capacitor, close to the device.

Output Filter Capacitor Value

The output filter capacitor values are generally determined by the ESR and voltage rating requirements, rather than actual capacitance requirements for loop stability. In other words, the low-ESR electrolytic capacitor that meets the ESR requirement usually has more output capacitance than is required for AC stability. Use only specialized low-ESR capacitors intended for switching-regulator applications, such as AVX TPS, Sprague 595D, Sanyo OS-CON, or Nichicon PL series. To ensure stability, the capacitor must meet *both* minimum capacitance and maximum ESR values as given in the following equations:

$$C_{OUT} > \frac{V_{REF}(1 + V_{OUT} / V_{IN(MIN)})}{V_{OUT} \times R_{SENSE} \times f}$$

$$R_{ESR} < \frac{R_{SENSE} \times V_{OUT}}{V_{REF}}$$

(can be multiplied by 1.5; see text below)

These equations are worst case, with 45 degrees of phase margin to ensure jitter-free, fixed-frequency operation and provide a nicely damped output response for zero to full-load step changes. Some cost-conscious designers may wish to bend these rules with less-expensive capacitors, particularly if the load lacks large step changes. This practice is tolerable if some bench testing over temperature is done to verify acceptable noise and transient response.

No well-defined boundary exists between stable and unstable operation. As phase margin is reduced, the first symptom is a bit of timing jitter, which shows up as blurred edges in the switching waveforms where the scope won't quite sync up. Technically speaking, this jitter (usually harmless) is unstable operation, since the duty factor varies slightly. As capacitors with higher ESRs are used, the jitter becomes more pronounced, and the load-transient output voltage waveform starts looking ragged at the edges. Eventually, the load-transient waveform has enough ringing on it that the peak noise levels exceed the allowable output voltage tolerance. Note that even with zero phase margin and gross instability present, the output voltage noise never gets much worse than $I_{PEAK} \times R_{ESR}$ (under constant loads).

Designers of RF communicators or other noise-sensitive analog equipment should be conservative and stay within the guidelines. Designers of notebook computers and similar commercial-temperature-range digital sys-

Multi-Output, Low-Noise Power-Supply Controllers for Notebook Computers

tems can multiply the R_{ESR} value by a factor of 1.5 without hurting stability or transient response.

The output voltage ripple is usually dominated by the filter capacitor's ESR, and can be approximated as $I_{RIPPLE} \times R_{ESR}$. There is also a capacitive term, so the full equation for ripple in continuous-conduction mode is $V_{NOISE\ (p-p)} = I_{RIPPLE} \times [R_{ESR} + 1/(2 \times \pi \times f \times C_{OUT})]$. In Idle Mode, the inductor current becomes discontinuous, with high peaks and widely spaced pulses, so the noise can actually be higher at light load (compared to full load). In Idle Mode, calculate the output ripple as follows:

$$V_{NOISE(p-p)} = \frac{0.02 \times R_{ESR}}{R_{SENSE}} + \frac{0.0003 \times L \times [1 / V_{OUT} + 1 / (V_{IN} - V_{OUT})]}{(R_{SENSE})^2 \times C_{OUT}}$$

Transformer Design (for Auxiliary Outputs Only)

Buck-plus-flyback applications, sometimes called "coupled-inductor" topologies, need a transformer to generate multiple output voltages. Performing the basic electrical design is a simple task of calculating turns ratios and adding the power delivered to the secondary to calculate the current-sense resistor and primary inductance. However, extremes of low input-output differentials, widely different output loading levels, and high turns ratios can complicate the design due to parasitic transformer parameters such as interwinding capacitance, secondary resistance, and leakage inductance. For examples of what is possible with real-world transformers, see the Maximum Secondary Current vs. Input Voltage graph in the *Typical Operating Characteristics* section.

Power from the main and secondary outputs is combined to get an equivalent current referred to the main output voltage (see the *Inductor Value* section for parameter definitions). Set the current-sense resistor resistor value at 80mV / I_{TOTAL}.

P_{TOTAL} = The sum of the output power from all outputs

$I_{TOTAL} = P_{TOTAL} / V_{OUT}$ = The equivalent output current referred to V_{OUT}

$$L(primary) = \frac{V_{OUT}(V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f \times I_{TOTAL} \times LIR}$$

$$\text{Turns Ratio } N = \frac{V_{SEC} + V_{FWD}}{V_{OUT(MIN)} + V_{RECT} + V_{SENSE}}$$

where: V_{SEC} = the minimum required rectified secondary output voltage

V_{FWD} = the forward drop across the secondary rectifier

$V_{OUT(MIN)}$ = the *minimum* value of the main output voltage (from the *Electrical Characteristics*)

V_{RECT} = the on-state voltage drop across the synchronous rectifier MOSFET

V_{SENSE} = the voltage drop across the sense resistor

In positive-output applications, the transformer secondary return is often referred to the main output voltage, rather than to ground, to reduce the needed turns ratio. In this case, the main output voltage must first be subtracted from the secondary voltage to obtain V_{SEC}.

Selecting Other Components

MOSFET Switches

The high-current N-channel MOSFETs must be logic-level types with guaranteed on-resistance specifications at V_{GS} = 4.5V. Lower gate threshold specifications are better (i.e., 2V max rather than 3V max). Drain-source breakdown voltage ratings must at least equal the maximum input voltage, preferably with a 20% derating factor. The best MOSFETs will have the lowest on-resistance per nanocoulomb of gate charge. Multiplying $R_{DS(ON)} \times Q_G$ provides a good figure for comparing various MOSFETs. Newer MOSFET process technologies with dense cell structures generally perform best. The internal gate drivers tolerate >100nC total gate charge, but 70nC is a more practical upper limit to maintain best switching times.

In high-current applications, MOSFET package power dissipation often becomes a dominant design factor. I^2R power losses are the greatest heat contributor for both high-side and low-side MOSFETs. I^2R losses are distributed between Q1 and Q2 according to duty factor (see the following equations). Generally, switching losses affect only the upper MOSFET, since the Schottky rectifier clamps the switching node in most cases before the synchronous rectifier turns on. Gate-charge losses are dissipated by the driver and don't heat the MOSFET. Calculate the temperature rise according to package thermal-resistance specifications to ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature. The worst-case dissipation for the high-side MOSFET occurs at both extremes of input voltage, and the worst-case dissipation for the low-side MOSFET occurs at maximum input voltage.

$$PD(\text{upper FET}) = (I_{LOAD})^2 \times R_{DS(ON)} \times DUTY + V_{IN} \times I_{LOAD} \times f \times \left(\frac{V_{IN} \times C_{RSS}}{I_{GATE}} + 20ns \right)$$

$$PD(\text{lower FET}) = (I_{LOAD})^2 \times R_{DS(ON)} \times (1 - DUTY)$$

$$DUTY = (V_{OUT} + V_{Q2}) / (V_{IN} - V_{Q1})$$

where: on-state voltage drop $V_{Q_} = I_{LOAD} \times R_{DS(ON)}$

C_{RSS} = MOSFET reverse transfer capacitance

I_{GATE} = DH driver peak output current capability (1A typical)

20ns = DH driver inherent rise/fall time

Under output short-circuit, the MAX1633/MAX1634/MAX1635's synchronous rectifier MOSFET suffers extra stress because its duty factor can increase to greater than 0.9. It may need to be oversized to tolerate a continuous DC short circuit. During short circuit, the MAX1630/MAX1631/MAX1632's output undervoltage shutdown protects the synchronous rectifier under output short-circuit conditions.

To reduce EMI, add a 0.1µF ceramic capacitor from the high-side switch drain to the low-side switch source.

Rectifier Clamp Diode

The rectifier is a clamp across the low-side MOSFET that catches the negative inductor swing during the 60ns dead time between turning one MOSFET off and each low-side MOSFET on. The latest generations of MOSFETs incorporate a high-speed silicon body diode, which serves as an adequate clamp diode if efficiency is not of primary importance. A Schottky diode can be placed in parallel with the body diode to reduce the forward voltage drop, typically improving efficiency 1% to 2%. Use a diode with a DC current rating equal to one-third of the load current; for example, use an MBR0530 (500mA-rated) type for loads up to 1.5A, a 1N5819 type for loads up to 3A, or a 1N5822 type for loads up to 10A. The rectifier's rated reverse breakdown voltage must be at least equal to the maximum input voltage, preferably with a 20% derating factor.

Boost-Supply Diode D2

A signal diode such as a 1N4148 works well in most applications. If the input voltage can go below +6V, use a small (20mA) Schottky diode for slightly improved efficiency and dropout characteristics. Don't use large power diodes, such as 1N5817 or 1N4001, since high junction capacitance can pump up VL to excessive voltages.

Rectifier Diode D3 (Transformer Secondary Diode)

The secondary diode in coupled-inductor applications must withstand flyback voltages greater than 60V, which usually rules out most Schottky rectifiers. Common silicon rectifiers, such as the 1N4001, are also prohibited because they are too slow. This often makes fast silicon rectifiers such as the MURS120 the only choice. The flyback voltage across the rectifier is related to the V_{IN} - V_{OUT} difference, according to the transformer turns ratio:

$$V_{FLYBACK} = V_{SEC} + (V_{IN} - V_{OUT}) \times N$$

where: N = the transformer turns ratio SEC/PRI

V_{SEC} = the maximum secondary DC output voltage

V_{OUT} = the primary (main) output voltage

Subtract the main output voltage (V_{OUT}) from $V_{FLYBACK}$ in this equation if the secondary winding is returned to V_{OUT} and not to ground. The diode reverse breakdown rating must also accommodate any ringing due to leakage inductance. D3's current rating should be at least twice the DC load current on the secondary output.

Low-Voltage Operation

Low input voltages and low input-output differential voltages each require extra care in their design. Low absolute input voltages can cause the VL linear regulator to enter dropout and eventually shut itself off. Low input voltages relative to the output (low V_{IN}-V_{OUT} differential) can cause bad load regulation in multi-output flyback applications (see the design equations in the *Transformer Design* section). Also, low V_{IN}-V_{OUT} differentials can also cause the output voltage to sag when the load current changes abruptly. The amplitude of the sag is a function of inductor value and maximum duty factor (an *Electrical Characteristics* parameter, 98% guaranteed over temperature at f = 200kHz), as follows:

$$V_{SAG} = \frac{(I_{STEP})^2 \times L}{2 \times C_{OUT} \times (V_{IN(MAX)} \times D_{MAX} - V_{OUT})}$$

The cure for low-voltage sag is to increase the output capacitor's value. For example, at V_{IN} = +5.5V, V_{OUT} = +5V, L = 10µH, f = 200kHz, I_{STEP} = 3A, a total capacitance of 660µF keeps the sag less than 200mV. Note that only the capacitance requirement increases, and the ESR requirements don't change. Therefore, the added capacitance can be supplied by a low-cost bulk capacitor in parallel with the normal low-ESR capacitor.

Multi-Output, Low-Noise Power-Supply Controllers for Notebook Computers

Table 5. Low-Voltage Troubleshooting Chart

SYMPTOM	CONDITION	ROOT CAUSE	SOLUTION
Sag or droop in V_{OUT} under step-load change	Low V_{IN}-V_{OUT} differential, <1.5V	Limited inductor-current slew rate per cycle.	Increase bulk output capacitance per formula (see *Low-Voltage Operation* section). Reduce inductor value.
Dropout voltage is too high (V_{OUT} follows V_{IN} as V_{IN} decreases)	Low V_{IN}-V_{OUT} differential, <1V	Maximum duty-cycle limits exceeded.	Reduce operation to 200kHz. Reduce MOSFET on-resistance and coil DCR.
Unstable—jitters between different duty factors and frequencies	Low V_{IN}-V_{OUT} differential, <0.5V	Normal function of internal low-dropout circuitry.	Increase the minimum input voltage or ignore.
Secondary output won't support a load	Low V_{IN}-V_{OUT} differential, V_{IN} < 1.3 x V_{OUT} (main)	Not enough duty cycle left to initiate forward-mode operation. Small AC current in primary can't store energy for flyback operation.	Reduce operation to 200kHz. Reduce secondary impedances; use a Schottky diode, if possible. Stack secondary winding on the main output.
Poor efficiency	Low input voltage, <5V	VL linear regulator is going into dropout and isn't providing good gate-drive levels.	Use a small 20mA Schottky diode for boost diode D2. Supply VL from an external source.
Won't start under load or quits before battery is completely dead	Low input voltage, <4.5V	VL output is so low that it hits the VL UVLO threshold.	Supply VL from an external source other than V_{IN}, such as the system +5V supply.

Applications Information

Heavy-Load Efficiency Considerations

The major efficiency-loss mechanisms under loads are, in the usual order of importance:

- P(I^2R) = I^2R losses
- P(tran) = transition losses
- P(gate) = gate-charge losses
- P(diode) = diode-conduction losses
- P(cap) = capacitor ESR losses
- P(IC) = losses due to the IC's operating supply supply current

Inductor core losses are fairly low at heavy loads because the inductor's AC current component is small. Therefore, they aren't accounted for in this analysis. Ferrite cores are preferred, especially at 300kHz, but powdered cores, such as Kool-Mu, can work well.

$$\text{Efficiency} = P_{OUT} / P_{IN} \times 100\%$$
$$= P_{OUT} / (P_{OUT} + P_{TOTAL}) \times 100\%$$

$$P_{TOTAL} = P(I^2R) + P(\text{tran}) + P(\text{gate}) + P(\text{diode}) + P(\text{cap}) + P(\text{IC})$$

$$P = (I^2R) = (I_{LOAD})^2 \times (R_{DC} + R_{DS(ON)} + R_{SENSE})$$

where R_{DC} is the DC resistance of the coil, $R_{DS(ON)}$ is the MOSFET on-resistance, and R_{SENSE} is the current-sense resistor value. The $R_{DS(ON)}$ term assumes identical MOSFETs for the high-side and low-side switches, because they time-share the inductor current. If the MOSFETs aren't identical, their losses can be estimated by averaging the losses according to duty factor.

$$PD(\text{tran}) = \text{transition loss} = V_{IN} \times I_{LOAD} \times f \times \frac{3}{2} \times [(V_{IN} \times C_{RSS} / I_{GATE}) + 20\text{ns}]$$

where C_{RSS} is the reverse transfer capacitance of the high-side MOSFET (a data-sheet parameter), I_{GATE} is the DH gate-driver peak output current (1.5A typical), and 20ns is the rise/fall time of the DH driver (20ns typical).

$$P(\text{gate}) = qG \times f \times VL$$

where VL is the internal-logic-supply voltage (+5V), and qG is the sum of the gate-charge values for low-side and high-side switches. For matched MOSFETs, qG is twice the data-sheet value of an individual MOSFET. If V_{OUT} is set to less than 4.5V, replace VL in this equation with V_{BATT}. In this case, efficiency can be improved by connecting VL to an efficient 5V source, such as the system +5V supply.

$$P(\text{diode}) = \text{diode-conduction losses} = I_{LOAD} \times V_{FWD} \times t_D \times f$$

where t_D is the diode-conduction time (120ns typical) and V_{FWD} is the forward voltage of the diode.

This power is dissipated in the MOSFET body diode if no external Schottky diode is used.

$$P(cap) = \text{input capacitor ESR loss} = (I_{RMS})^2 \times R_{ESR}$$

where I_{RMS} is the input ripple current as calculated in the *Design Procedure* and *Input Capacitor Value* sections.

Light-Load Efficiency Considerations

Under light loads, the PWM operates in discontinuous mode, where the inductor current discharges to zero at some point during the switching cycle. This makes the inductor current's AC component high compared to the load current, which increases core losses and I^2R losses in the output filter capacitors. For best light-load efficiency, use MOSFETs with moderate gate-charge levels, and use ferrite, MPP, or other low-loss core material. Avoid powdered-iron cores; even Kool-Mu (aluminum alloy) is not as good as ferrite.

PC Board Layout Considerations

Good PC board layout is *required* in order to achieve specified noise, efficiency, and stability performance. The PC board layout artist must be given explicit instructions, preferably a pencil sketch showing the placement of power-switching components and high-current routing. See the PC board layout in the MAX1630 Evaluation Kit manual for examples. A ground plane is essential for optimum performance. In most applications, the circuit will be located on a multilayer board, and full use of the four or more copper layers is recommended. Use the top layer for high-current connections, the bottom layer for quiet connections (REF, SS, GND), and the inner layers for an uninterrupted ground plane. Use the following step-by-step guide:

1) Place the high-power components (C1, C2, Q1, Q2, D1, L1, and R1) first, with their grounds adjacent.

   Priority 1: **Minimize current-sense resistor trace lengths** and ensure accurate current sensing with Kelvin connections (Figure 7).

   Priority 2: **Minimize ground trace lengths** in the high-current paths (discussed below).

   Priority 3: Minimize other trace lengths in the high-current paths.

   Use >5mm-wide traces

   C_{IN} to high-side MOSFET drain: 10mm max length

   Rectifier diode cathode to low-side MOSFET: 5mm max length

   LX node (MOSFETs, rectifier cathode, inductor): 15mm max length

Ideally, surface-mount power components are butted up to one another with their ground terminals almost touching. These high-current grounds are then connected to each other with a wide filled zone of top-layer copper so they don't go through vias. The resulting top-layer "sub-ground-plane" is connected to the normal inner-layer ground plane at the output ground terminals, which ensures that the IC's analog ground is sensing at the supply's output terminals without interference from IR drops and ground noise. Other high-current paths should also be minimized, but **focusing primarily on short ground and current-sense connections eliminates about 90% of all PC board layout problems** (see the PC board layouts in the MAX1630 Evaluation Kit manual for examples).

2) Place the IC and signal components. Keep the main switching nodes (LX nodes) away from sensitive analog components (current-sense traces and REF capacitor). Place the IC and analog components on the opposite side of the board from the power-switching node. **Important:** the IC must be no farther than 10mm from the current-sense resistors. Keep the gate-drive traces (DH_, DL_, and BST_) shorter than 20mm and route them away from CSH_, CSL_, and REF.

3) Use a single-point star ground where the input ground trace, power ground (sub-ground-plane), and normal ground plane meet at the supply's output ground terminal. Connect both IC ground pins and all IC bypass capacitors to the normal ground plane.

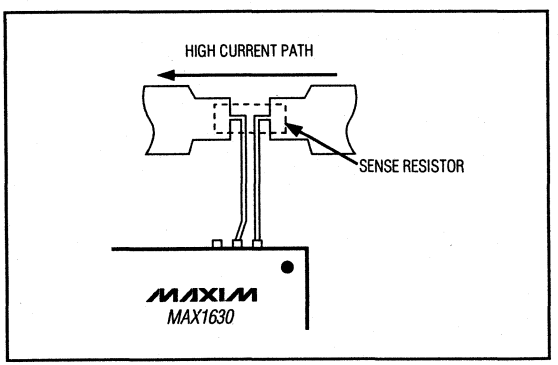


Figure 7. Kelvin Connections for the Current-Sense Resistors

Multi-Output, Low-Noise Power-Supply Controllers for Notebook Computers

Application Circuits

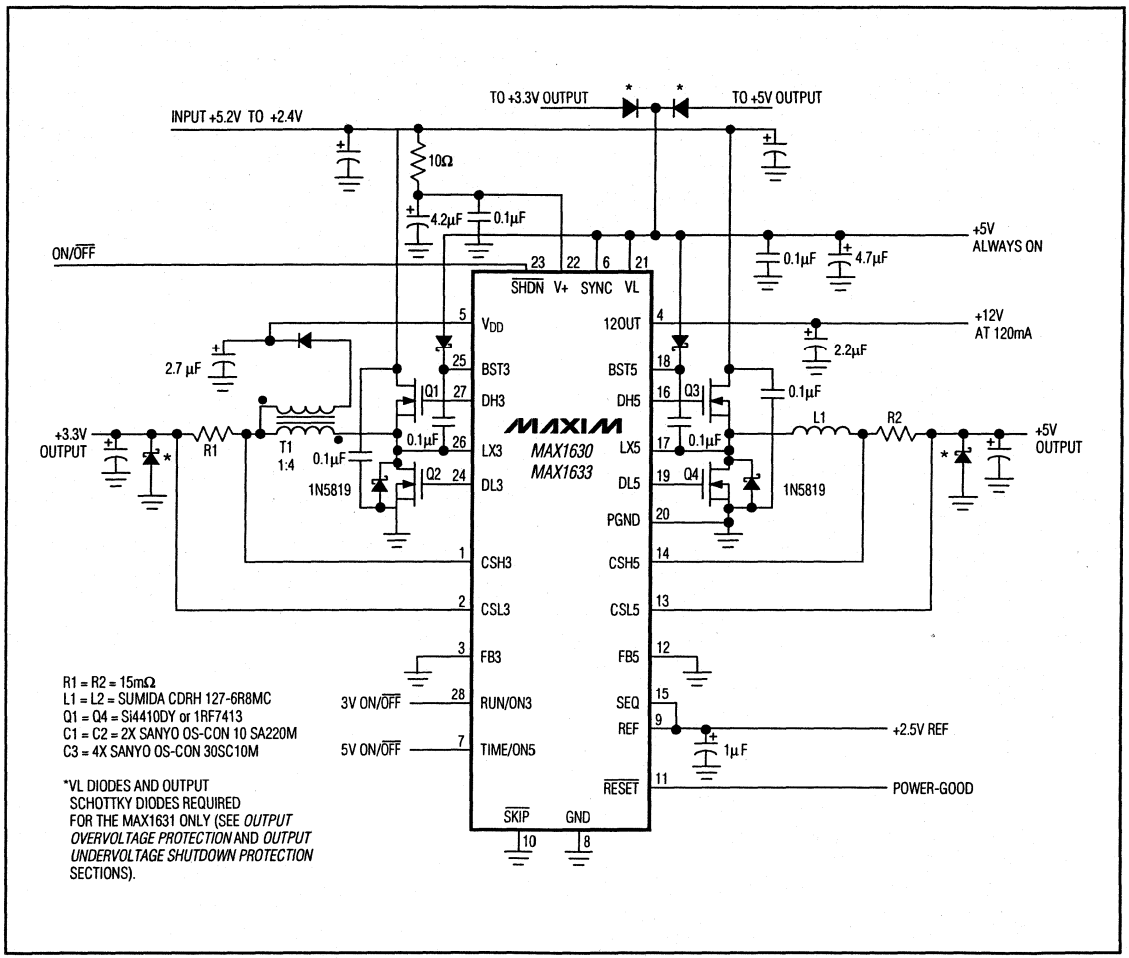


Figure 8. Triple-Output Application for Low-Voltage Batteries (MAX1630/MAX1633)

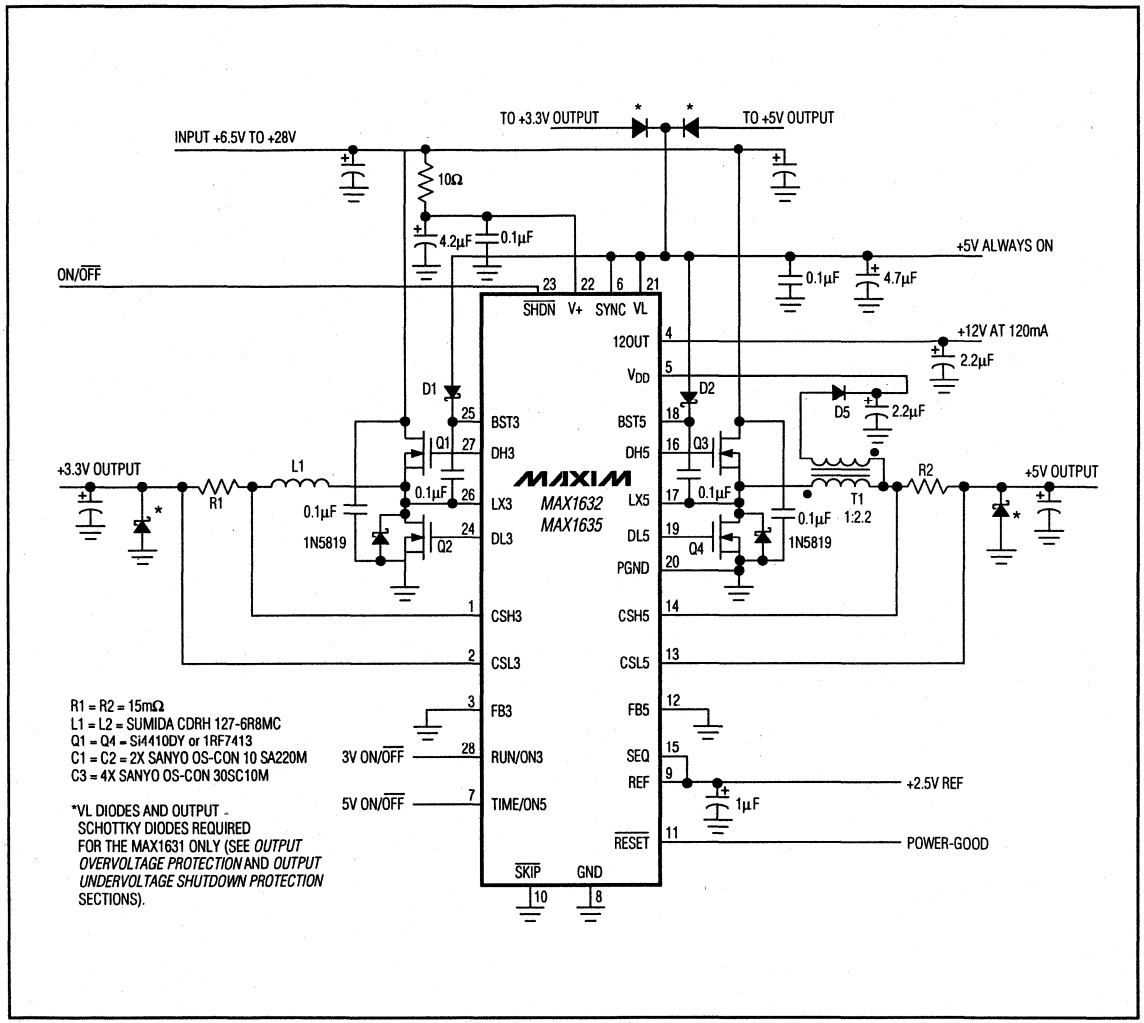


Figure 9. Triple-Output Application for High-Voltage Batteries (MAX1632/MAX1635)

Multi-Output, Low-Noise Power-Supply Controllers for Notebook Computers

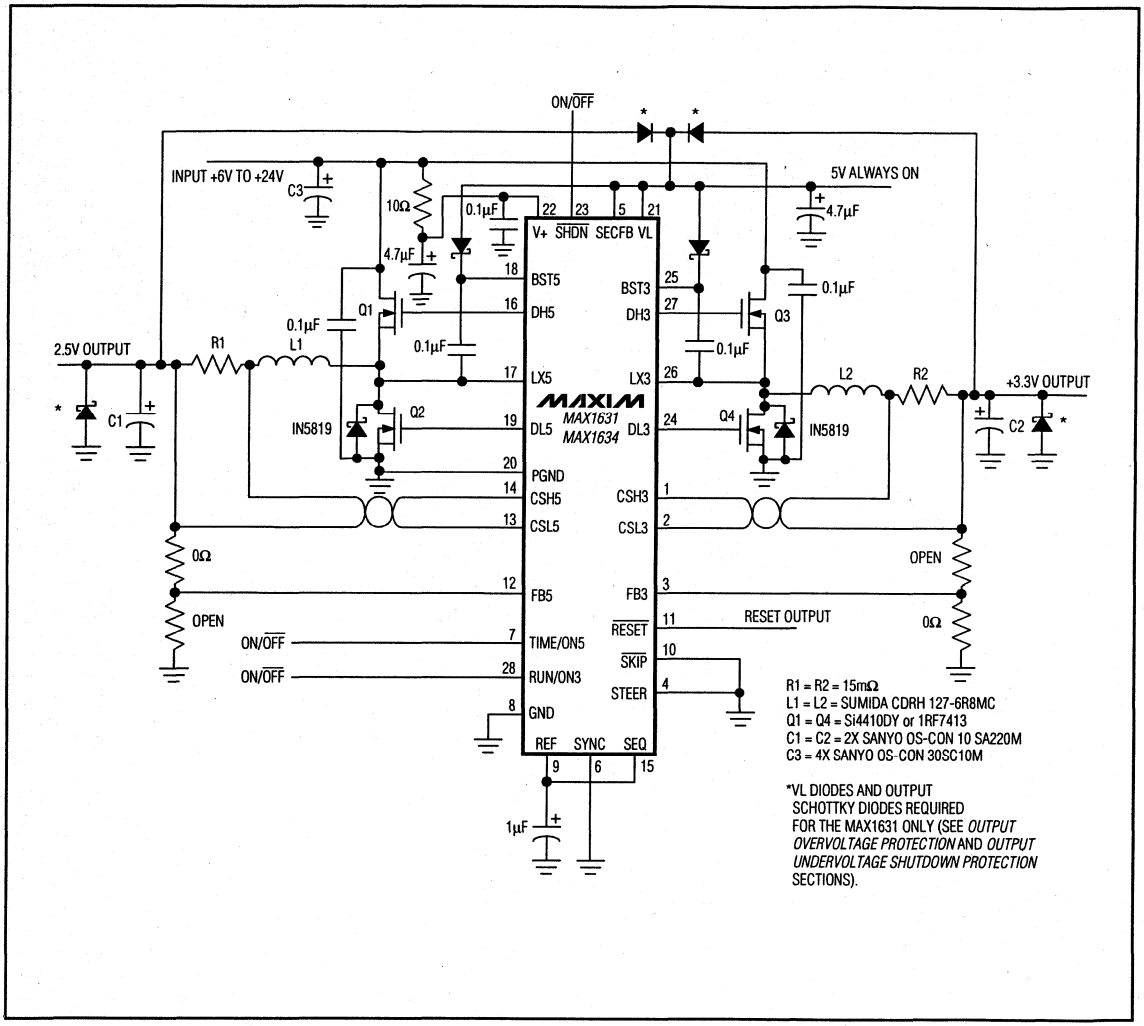
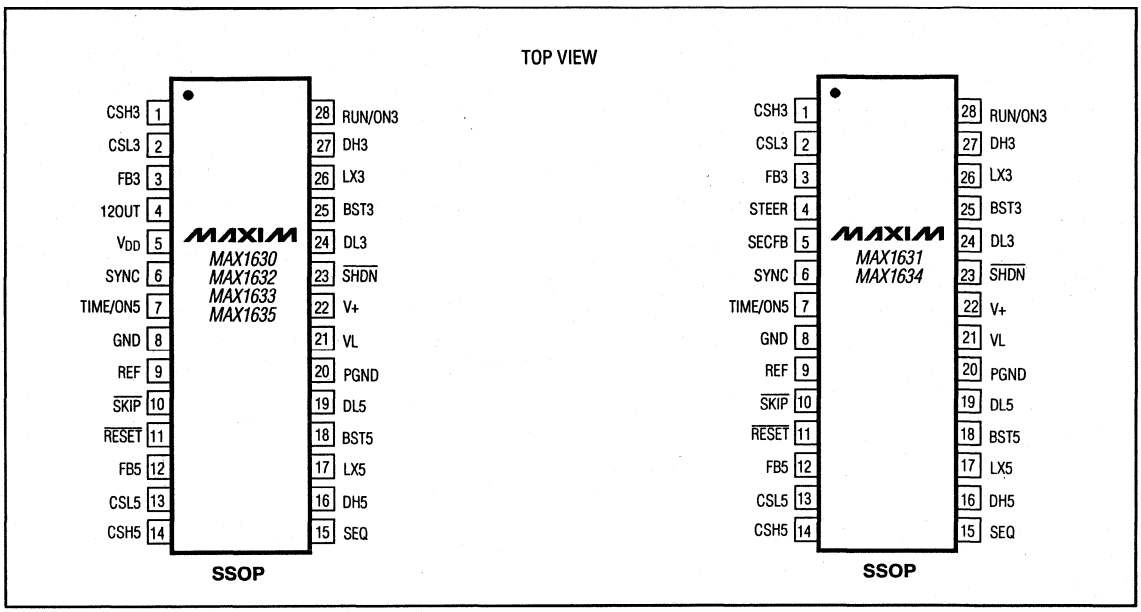


Figure 10. Dual, 4A, Notebook Computer Power Supply

Multi-Output, Low-Noise Power-Supply Controllers for Notebook Computers

Pin Configurations



Selector Guide

DEVICE	AUXILIARY OUTPUT	SECONDARY FEEDBACK	OVER/UNDERVOLTAGE PROTECTION
MAX1630	12V Linear Regulator	Feeds into the 3.3V SMPS	Yes
MAX1631	None (SECFB input)	Selectable (STEER pin)	Yes
MAX1632	12V Linear Regulator	Feeds into the 5V SMPS	Yes
MAX1633	12V Linear Regulator	Feeds into the 3.3V SMPS	No
MAX1634	None (SECFB input)	Selectable (STEER pin)	No
MAX1635	12V Linear Regulator	Feeds into the 5V SMPS	No

Multi-Output, Low-Noise Power-Supply Controllers for Notebook Computers

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX1631CAI	0°C to +70°C	28 SSOP
MAX1631EAI	-40°C to +85°C	28 SSOP
MAX1632CAI	0°C to +70°C	28 SSOP
MAX1632EAI	-40°C to +85°C	28 SSOP
MAX1633CAI	0°C to +70°C	28 SSOP
MAX1633EAI	-40°C to +85°C	28 SSOP
MAX1634CAI	0°C to +70°C	28 SSOP
MAX1634EAI	-40°C to +85°C	28 SSOP
MAX1635CAI	0°C to +70°C	28 SSOP
MAX1635EAI	-40°C to +85°C	28 SSOP

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

10/96

MAXIM

High-Efficiency, Switch-Mode Current Source

General Description

The MAX1640/MAX1641 are high-efficiency switch-mode current sources intended for microprocessor-controlled battery chargers and variable-load applications. The charging current, output voltage limit, and pulse-trickle-charge level are programmable with external resistors or DAC outputs. They operate from 5.5V to 30V inputs and deliver loads up to 3A.

The MAX1640 senses current on the high side of the battery, which allows the load to connect directly to ground and eliminates ground-potential errors. The MAX1641 senses current on the low side of the battery, bypassing the offset voltage of the error amplifier and improving current-regulation accuracy.

These devices use an external P-channel MOSFET switch and an optional external N-channel MOSFET synchronous rectifier to improve efficiency and reduce power dissipation, permitting use in small spaces.

Features

- **95% Efficiency**
- **Simple Current Regulation**
- **5%-Accurate Current Regulation**
- **Permits DAC-Controlled Current Adjustment**
- **Optional Synchronous Rectifier for Higher Efficiency**
- **5.5V to 30V Input Range**
- **Adjustable Voltage Limit**
- **High-Side or Low-Side Current Sensing**
- **Pulse-Trickle Charging**

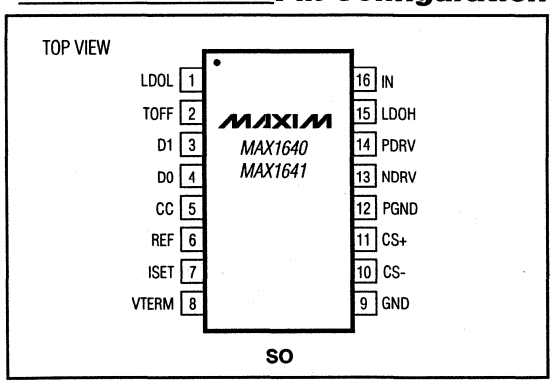
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1640C/D	0°C to +70°C	Dice
MAX1640ESE	-40°C to +85°C	16 Narrow SO
MAX1641C/D	0°C to +70°C	Dice
MAX1641ESE	-40°C to +85°C	16 Narrow SO

Applications

Notebook Computers
Hand-Held Terminals
Cellular Phone Chargers
Portable Stereos
Battery Backup Applications

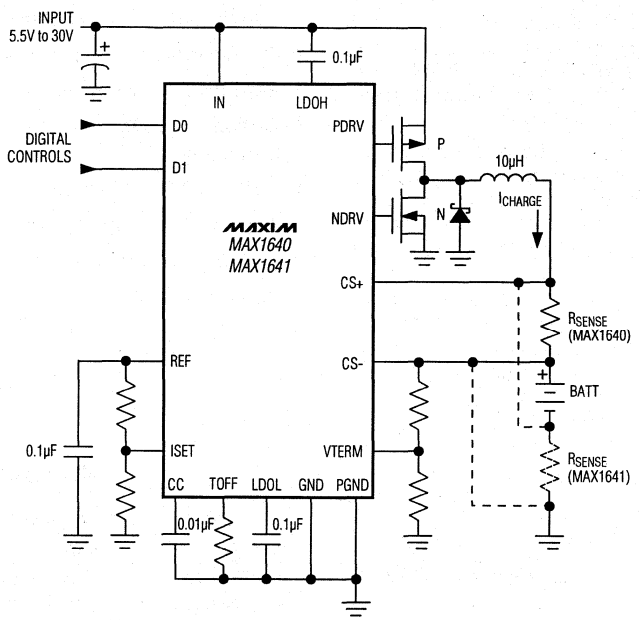
Pin Configuration



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High-Efficiency, Switch-Mode Current Source

Typical Operating Circuit



ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

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MAXIM

High-Efficiency, Step-Up DC-DC Converters for 1V Inputs

General Description

The MAX1642/MAX1643 are high-efficiency, low-voltage, step-up DC-DC converters intended for devices powered by a single alkaline cell. They feature low quiescent supply currents, and come packaged in the ultra-small µMAX, which is only 1.1mm high. The guaranteed start-up voltage is 0.85V.

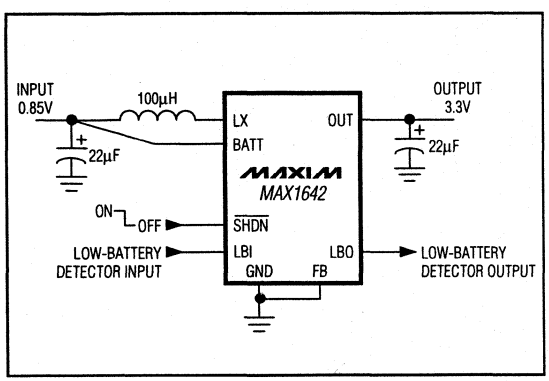
Each device consists of the following: an internal 1Ω, N-channel MOSFET power switch; a built-in synchronous rectifier which acts as the catch diode; an oscillator; a reference; and pulse-frequency modulation (PFM) control circuitry. The MAX1642 also includes a voltage detector and a 1µA logic-controlled shutdown mode. The MAX1643 offers a voltage detector and a dedicated low-battery voltage detector.

The output range for each device is preset to 3.3V ±4%, or can be adjusted from +2V to +5.5V using only two resistors. Typical output current is 20mA. When the MAX1642 is in shutdown, the input and output are disconnected.

Applications

Pagers
Remote Controls
Pointing Devices
Personal Medical Monitors
Single-Cell Battery-Powered Devices

Functional Diagram



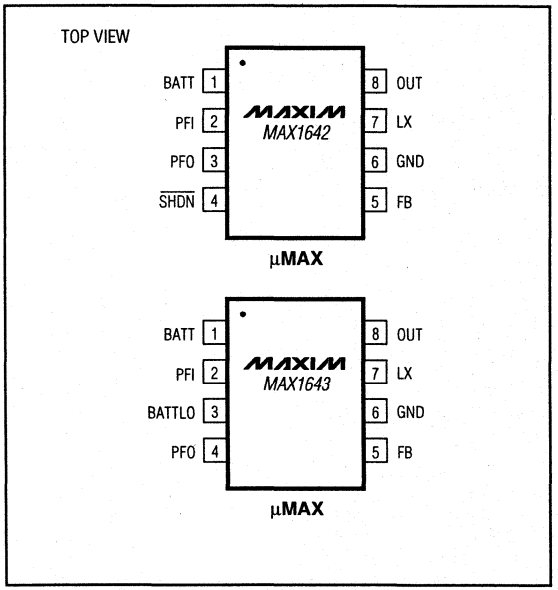
Features

- ♦ **Built-In Synchronous Rectifier**
- ♦ **0.85V Guaranteed Start-Up**
- ♦ **Ultra-Small µMAX Package; 1.1mm High**
- ♦ **85% Efficiency**
- ♦ **10µA Quiescent Supply Current**
- ♦ **1µA Logic-Controlled Shutdown (MAX1642)**
- ♦ **Two Voltage Detectors (MAX1643)**
- ♦ **2V to 5.5V Output Range**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1642C/D	0°C to +70°C	Dice
MAX1642EUA	-40°C to +85°C	8 µMAX
MAX1643C/D	0°C to +70°C	Dice
MAX1643EUA	-40°C to +85°C	8 µMAX

Pin Configurations



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ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

11/96

MAXIM

Chemistry-Independent Battery Chargers

General Description

The MAX1647/MAX1648 provide the power control necessary to charge batteries of any chemistry. In the MAX1647, all charging functions are controlled via an Intel System Management Bus (SMBus™) interface. The SMBus 2-wire serial interface sets the charge voltage and current, and provides thermal status information. The MAX1647 functions as a level 2 charger, compliant with the Duracell/Intel Smart Battery Charger Specification. The MAX1648 omits the SMBus serial interface, and instead sets the charge voltage and current proportional to the voltage applied to external control pins.

In addition to the feature set required for a level 2 charger, the MAX1647 generates interrupts to signal the host when power is applied to the charger or a battery is installed or removed. Additional status bits allow the host to check whether the charger has enough input voltage, and whether the voltage on or current into the battery is being regulated. This allows the host to determine when lithium-ion batteries have completed charge without interrogating the battery.

The MAX1647 is available in a 20-pin SSOP package with a profile height of only 2mm. The MAX1648 is available in a 16-pin SO package.

Applications

Notebook Computers

Personal Digital Assistants

Charger Base Stations

Phones

Features

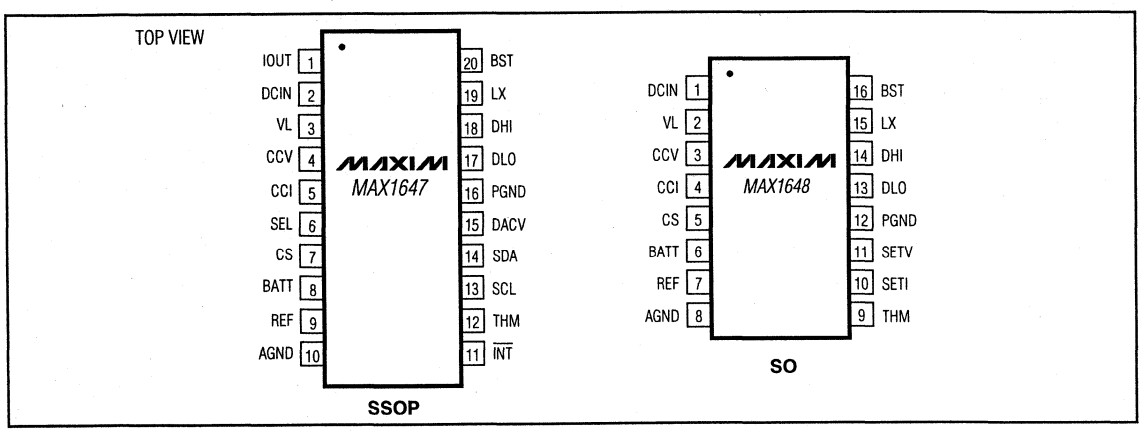
- ♦ **Charges Any Battery Chemistry: Li-Ion, NiCd, NiMH, etc.**
- ♦ **Intel SMBus 2-Wire Serial Interface (MAX1647)**
- ♦ **Intel/Duracell Level 2 Smart Battery Compliant (MAX1647)**
- ♦ **4A, 2A, or 1A Maximum Battery Charge Current**
- ♦ **11-Bit Control of Charge Current**
- ♦ **Up to 18V Battery Compliance Voltage**
- ♦ **10-Bit Control of Compliance Voltage**
- ♦ **±0.75% Compliance Voltage Accuracy with External ±0.1% Reference**
- ♦ **Input Voltage Up to 28V**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1647EAP	-40°C to +85°C	20 SSOP
MAX1648ESE	-40°C to +85°C	16 Narrow SO

4

Pin Configurations

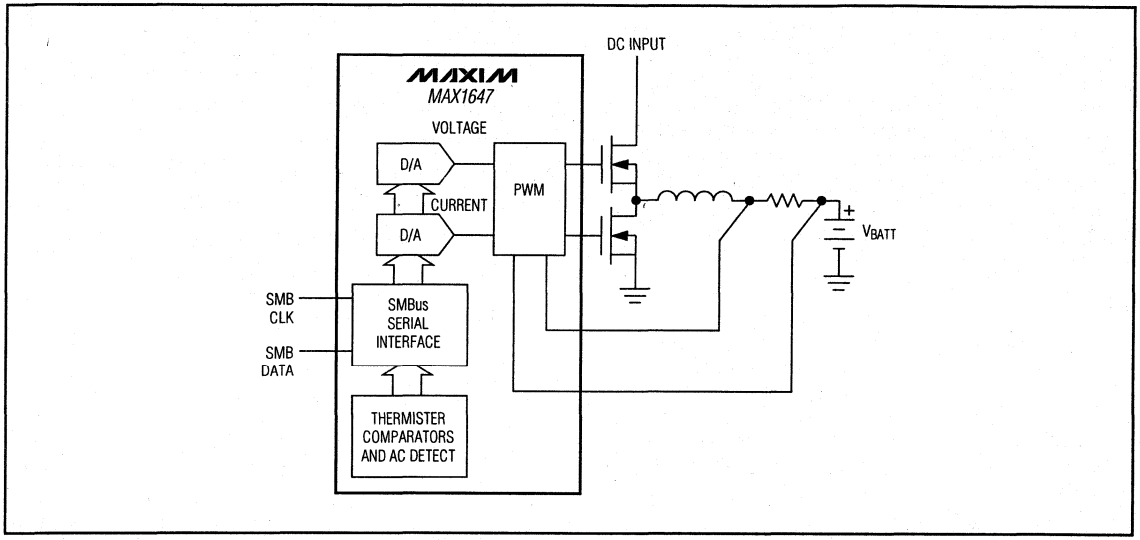


SMBus is a trademark of Intel Corp.

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Chemistry-Independent Battery Chargers

Functional Diagram



19-1117; Rev 0; 8/96

MAXIM

Low-Cost, Low-Dropout, Dual Linear Regulator

General Description

The MAX8862 low-cost, low-dropout, dual linear voltage regulator is ideal for battery-powered and portable applications. The regulators have independent supply inputs and provide 250mA and 100mA, respectively, with a full-load dropout voltage of 160mV. Both regulators use P-channel MOSFET pass transistors and maintain low quiescent current independent of load current. In dropout, the MOSFET does not suffer from excessive base currents, as do saturated PNP transistors.

The MAX8862 output voltage is preset to 4.95V (L), 3.175V (T), or 2.85V (R). This device employs Dual Mode™ operation, allowing user-adjustable outputs from +2V to +11V with external resistors. The input supply-voltage range is 2.5V to 11.5V. Other features include independent shutdown, power-good indicator, short-circuit and reverse-battery protection, and thermal shutdown.

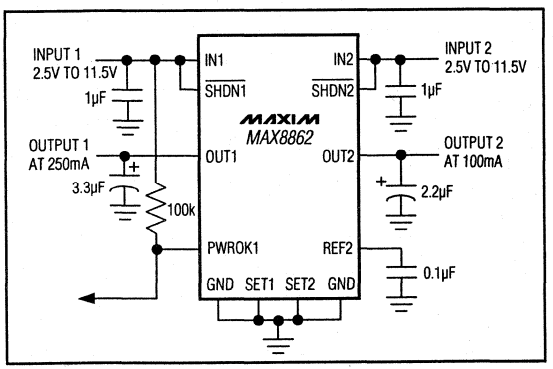
The MAX8862's regulators are ideal power supplies for the radio and the microcontroller (µC) used in digital, cordless, and PCS phones. The main regulator is optimized for superior transient and dynamic response, while the secondary regulator exhibits low-output, wideband noise.

The MAX8862 comes in a 16-pin SO package with a lead frame that uses multiple GND pins as a heat sink for additional thermal dissipation.

Applications

Cellular Phones
Cordless Phones
PCS Phones
PCMCIA Cards
Modems
Hand-Held Instruments
Electronic Planners

Typical Operating Circuit



Dual Mode is a trademark of Maxim Integrated Products.

Features

- ♦ **Low Cost**
- ♦ **Guaranteed 250mA and 100mA Output Currents, with Current Limiting**
- ♦ **Dual Mode Operation:**
  Fixed or Adjustable Output from +2V to +11V
- ♦ **+2.5V to +11.5V Input Range**
- ♦ **160mV Dropout Voltage at 200mA Output Current**
- ♦ **Low Supply Current—Even in Dropout**
  200µA Operating
  <1µA Shutdown
- ♦ **Power-Good Indicator**
- ♦ **Reverse-Battery Protection**
- ♦ **Thermal Overload Protection**

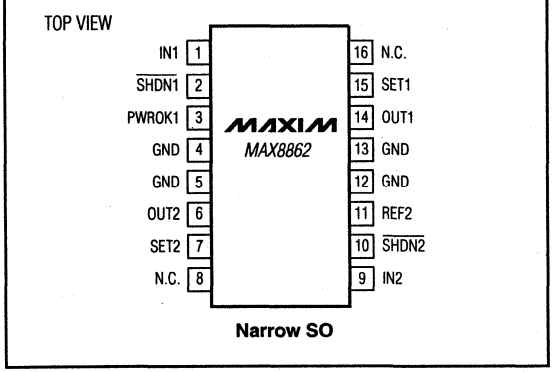
Ordering Information

PART*	TEMP. RANGE	PIN-PACKAGE
MAX8862_ESE	-40°C to +85°C	16 Narrow SO

**Insert the desired suffix letter (from the table below) into the blank to complete the part number.*

SUFFIX	FIXED OUTPUT VOLTAGE (V)
L	4.95
T	3.175
R	2.85

Pin Configuration



Narrow SO

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Low-Cost, Low-Dropout, Dual Linear Regulator

ABSOLUTE MAXIMUM RATINGS

IN1, IN2 to GND (Note 1) ..... ±12V
SET1, $\overline{SHDN1}$, PWROK1 to GND ..... -0.3V to (V_{IN1} + 0.3V)
SET2, $\overline{SHDN2}$, REF2 to GND ..... -0.3V, (V_{IN2} + 0.3V)
Output Short-Circuit Duration ..... Infinite
Continuous Power Dissipation (T_A = +70°C)
16-Pin Narrow SO (derate 20mW/°C above +70°C) 1W

Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: Connect $\overline{SHDN1}$ to IN1 and $\overline{SHDN2}$ to IN2 through 20kΩ resistors to limit current flow in case a battery is reversed.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Notes 2, 3)

($V_{IN_}$ = $V_{OUT_(TYP)}$ + 1V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range			2.5		11.5	V
Output Voltage	0mA < I_{OUT1} ≤ 250mA, 0mA < I_{OUT2} ≤ 100mA	MAX8862L	4.80	4.95	5.15	V
		MAX8862T	3.050	3.175	3.300	
		MAX8862R	2.75	2.85	2.95	
Output Voltage Range			2		11	V
Maximum Output Current	V_{IN1} = 2.5V min, V_{OUT1} = 2V		250			mA
	V_{IN2} = 2.5V min, V_{OUT2} = 2V		100			
Current Limit	I_{OUT1}			580		mA
	I_{OUT2}			250		
Quiescent Current				200	330	µA
Shutdown Supply Current	V_{IN1} = V_{IN2} = 11.5V			0.01	1	µA
Dropout Voltage (Note 4)	I_{OUT1} = I_{OUT2} = 1mA			1.5		mV
	I_{OUT1} = 200mA, MAX8862L/T			160	330	
	I_{OUT2} = 100mA, MAX8862L/T			160	350	
	I_{OUT1} = 200mA, MAX8862R			165	350	
	I_{OUT2} = 100mA, MAX8862R			180	400	
Line Regulation	I_{OUT1} = I_{OUT2} = 15mA	V_{IN1} = ($V_{OUT1\ (TYP)}$ + 1V) to 11.5V		0.03	0.1	%/V
		V_{IN2} = ($V_{OUT2\ (TYP)}$ + 1V) to 11.5V		0.02	0.08	
Load Regulation	I_{OUT1} = 0mA to 250mA, C_{OUT1} = 3.3µF			0.015		%/mA
	I_{OUT2} = 0mA to 100mA, C_{OUT2} = 2.2µF			0.02		
OUT2 Voltage Noise	C_{OUT2} = 2.2µF, Z_{OUT2} = 10mA	10Hz < f < 100kHz		277		mV_{RMS}
		10Hz < f < 1MHz		875		
	C_{OUT2} = 100µF, Z_{OUT2} = 10mA	10Hz < f < 100kHz		211		
		10Hz < f < 1MHz		667		
REFERENCE						
REF2 Output Voltage	C_{REF2} = 0.1µF		1.230	1.250	1.270	V
REF2 Line Regulation	V_{IN2} = 2.5V to 11.5V			1		mV
REF2 Load Regulation	I_{REF2} = 0µA to 10µA			6		mV

ELECTRICAL CHARACTERISTICS (Notes 2, 3)

($V_{IN_}$ = $V_{OUT_(TYP)}$ + 1V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PWROK1 OUTPUT					
PWROK1 Trip Voltage	Falling edge at SET1	1.175	1.200	1.225	V
PWROK1 Hysteresis	Rising edge at SET1		15		mV
PWROK1 Leakage Current	V_{PWROK1} = 11.5V		0.01	1	µA
PWROK1 Low Voltage	I_{SINK} = 0.5mA		25	200	mV
$\overline{SHDN}$					
$\overline{SHDN}$_ Logic Low	Shutdown mode, $V_{IN_}$ = $V_{OUT_(TYP)}$ + 1V to 11.5V			0.45	V
$\overline{SHDN}$_ Logic High	Active mode, $V_{IN_}$ = 11.5V	1.8			V
$\overline{SHDN}$_ Leakage Current	$V_{\overline{SHDN}_}$ = 11.5V		0.01	1	µA
SET_ INPUT					
SET_ Reference Voltage	SET_ = OUT_, I_{OUT1} = I_{OUT2} = 15mA	1.23	1.25	1.28	V
SET_ Input Bias Current	$V_{SET_}$ = 1.30V		0.01	0.1	µA
SET_ Threshold	Internal feedback			40	mV
	External feedback	250			
THERMAL PROTECTION					
Thermal Shutdown Temperature			160		°C
Thermal Shutdown Hysteresis			20		

4

ELECTRICAL CHARACTERISTICS (Notes 2, 3)

($V_{IN_}$ = $V_{OUT_(TYP)}$ + 1V, **T_A = -40°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range			2.5		11.5	V
Output Voltage	0mA < I_{OUT1} ≤ 250mA, 0mA < I_{OUT2} ≤ 100mA	MAX8862L	4.80	4.95	5.15	V
		MAX8862T	3.050	3.175	3.300	
		MAX8862R	2.740	2.85	2.960	
Output Voltage Range			2		11	V
Maximum Output Current	V_{IN1} = 2.5V min, V_{OUT1} = 2V		250			mA
	V_{IN2} = 2.5V min, V_{OUT2} = 2V		100			
Current Limit	I_{OUT1}			580		mA
	I_{OUT2}			250		
Quiescent Current				200	330	µA
Shutdown Supply Current	V_{IN1} = V_{IN2} = 11.5V			0.01	1	µA
Dropout Voltage (Note 4)	I_{OUT1} = I_{OUT2} = 1mA			1.5		mV
	I_{OUT1} = 200mA, MAX8862L/T			160	330	
	I_{OUT2} = 100mA, MAX8862L/T			160	350	
	I_{OUT1} = 200mA, MAX8862R			165	350	
	I_{OUT2} = 100mA, MAX8862R			180	400	

ELECTRICAL CHARACTERISTICS (Notes 2, 3) (continued)

($V_{IN_}$ = $V_{OUT_(TYP)}$ + 1V, **T_A = -40°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Line Regulation	I_{OUT1} = I_{OUT2} = 15mA	V_{IN1} = ($V_{OUT1\ (TYP)}$ + 1V) to 11.5V		0.03	0.12	%/V
		V_{IN2} = ($V_{OUT2\ (TYP)}$ + 1V) to 11.5V		0.02	0.10	
Load Regulation	I_{OUT1} = 0 to 250mA, C_{OUT1} = 3.3µF			0.015		%/mA
	C_{OUT2} = 2.2µF, 10Hz < f < 1MHz, I_{OUT2} = 10mA			0.02		
OUT2 Voltage Noise	C = 2.2µF, Z_{OUT2} = 10mA	10Hz < f < 100kHz	-	277	-	μV_{RMS}
		10Hz < f < 1MHz	-	875	-	
	C = 100µF, Z_{OUT2} = 10mA	10Hz < f < 100kHz	-	211	-	
		10Hz < f < 1MHz	-	667	-	
REFERENCE						
REF2 Output Voltage	C_{REF2} = 0.1µF		1.217	1.250	1.277	V
REF2 Line Regulation	V_{IN2} = 2.5V to 11.5V			1		mV
REF2 Load Regulation	I_{REF2} = 0µA to 10µA			6		mV
PWROK1 OUTPUT						
PWROK1 Trip Voltage	Falling edge at SET1		1.165	1.200	1.235	V
PWROK1 Hysteresis	Rising edge at SET1			15		mV
PWROK1 Leakage Current	V_{PWROK1} = 11.5V			0.01	1	µA
PWROK1 Low Voltage	I_{SINK} = 0.5mA			25	200	mV
$\overline{SHDN}$						
$\overline{SHDN}$_ Logic Low	Shutdown mode, $V_{IN_}$ = $V_{OUT_(TYP)}$ + 1V to 11.5V				0.45	V
$\overline{SHDN}$_ Logic High	Active mode, $V_{IN_}$ = 11.5V		2.0			V
$\overline{SHDN}$_ Leakage Current	$V_{\overline{SHDN}_}$ = 11.5V			0.02	1	µA
SET_ INPUT						
SET_ Reference Voltage	SET_ = OUT_, I_{OUT1} = I_{OUT2} = 15mA		1.220	1.250	1.290	V
SET_ Input Bias Current	$V_{SET_}$ = 1.30V			0.01	0.1	µA
SET_ Threshold	Internal feedback				30	mV
	External feedback		250			
THERMAL PROTECTION						
Thermal Shutdown Temperature				160		°C
Thermal Shutdown Hysteresis				10		

Note 2: Guaranteed by design for T_A = -40°C.

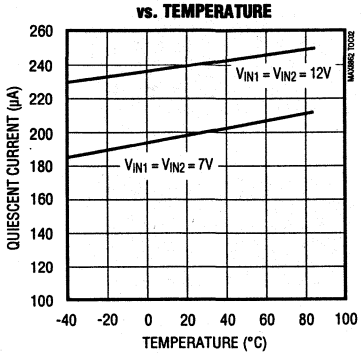
Note 3: Guaranteed for a junction temperature (T_J) equal to the operating temperature range. E-grade parts are guaranteed by design to operate up to T_J = +125°C. For T_J above +125°C, specifications exceed the operating limits.

Note 4: Dropout voltage is ($V_{IN_}$ - $V_{OUT_}$) when $V_{OUT_}$ falls to 100mV below its nominal value at $V_{IN_}$ = ($V_{OUT_}$ + 1V). For example, the MAX8862 is tested by measuring the $V_{OUT_}$ at ($V_{IN_}$ = 5.95V for the MAX8862L, $V_{IN_}$ = 4.175V for the MAX8862T, and $V_{IN_}$ = 3.85V for the MAX8862R) then $V_{IN_}$ is lowered until $V_{OUT_}$ falls 100mV below the measured value.

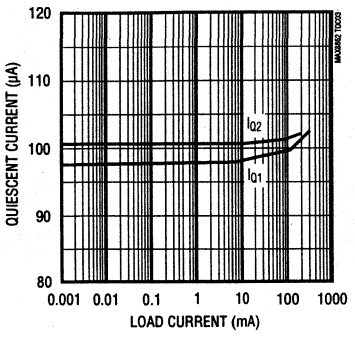
Typical Operating Characteristics

(V_{IN1} = V_{IN2} = 5.3V, C_{IN1} = C_{IN2} = 1µF, C_{OUT1} = 3.3µF, C_{OUT2} = 2.2µF, $\overline{SHDN1}$ = IN1, $\overline{SHDN2}$ = IN2. T_A = +25°C, unless otherwise noted.)

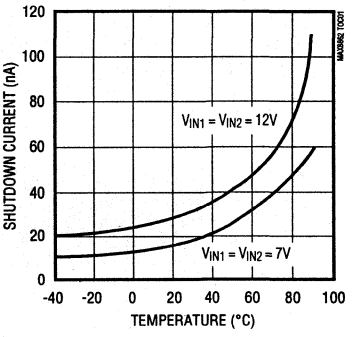
QUIESCENT CURRENT vs. TEMPERATURE



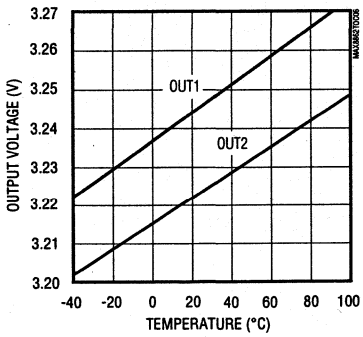
QUIESCENT CURRENT vs. LOAD CURRENT



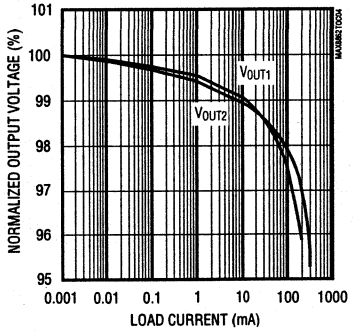
SHUTDOWN CURRENT vs. TEMPERATURE



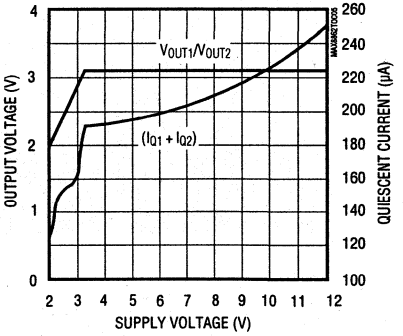
OUTPUT VOLTAGE vs. TEMPERATURE



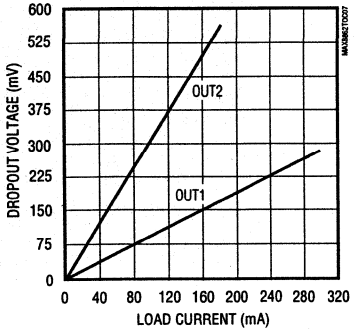
OUTPUT VOLTAGE vs. LOAD CURRENT



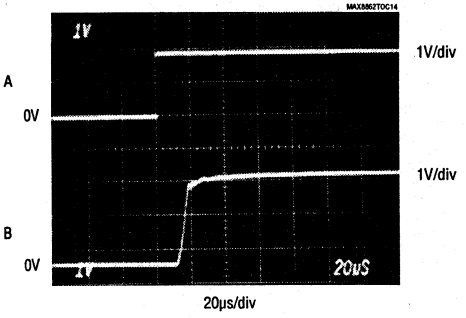
MAX8862T OUTPUT VOLTAGE & QUIESCENT CURRENT vs. SUPPLY VOLTAGE



DROPOUT VOLTAGE vs. LOAD CURRENT



OVERSHOOT AND TIME EXITING SHUTDOWN MODE



20µs/div

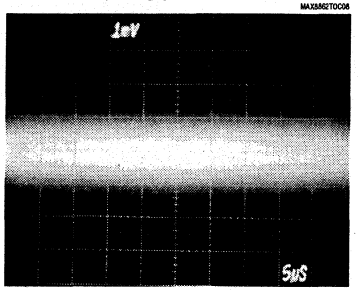
V_{IN1} = 5.3V, I_{OUT1} = 5mA
A = $\overline{SHDN1}$, 0.8V TO 2.4V, 1V/div
B = OUT1, 1V/div

Low-Cost, Low-Dropout, Dual Linear Regulator

Typical Operating Characteristics (continued)

(V_{IN1} = V_{IN2} = 5.3V, C_{IN1} = C_{IN2} = 1µF, C_{OUT1} = 3.3µF, C_{OUT2} = 2.2µF, $\overline{SHDN1}$ = IN1, $\overline{SHDN2}$ = IN2. T_A = +25°C, unless otherwise noted.)

OUT1 NOISE AND RIPPLE

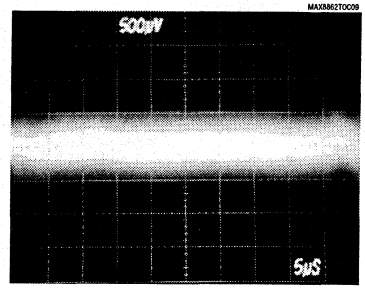


V_{OUT}
1mV/div

5µs/div

I_{OUT1} = 250mA, AC COUPLED

OUT2 NOISE AND RIPPLE

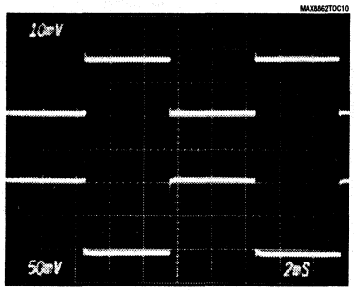


V_{OUT}
500µV/div

5µs/div

I_{OUT2} = 100mA, AC COUPLED

OUT1 LOAD-TRANSIENT RESPONSE

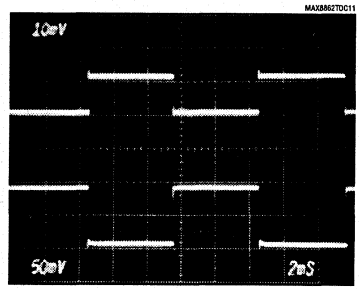


A
300mA
0mA
B
50mV/div

2ms/div

V_{IN1} = 7V, V_{OUT1} = 3.2V
A = LOAD CURRENT, 0mA TO 300mA, 0.2A/div
B = V_{OUT1} RIPPLE, 50mV/div, AC COUPLED

OUT2 LOAD-TRANSIENT RESPONSE

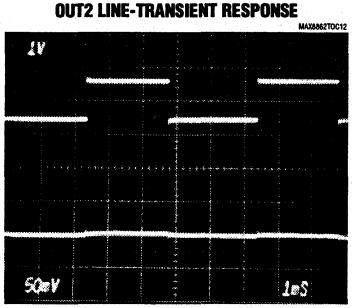


A
200mA
0mA
B
50mV/div

2ms/div

V_{IN2} = 7V, V_{OUT2} = 3.2V
A = LOAD CURRENT, 0mA TO 200mA, 0.2A/div
B = V_{OUT2} RIPPLE, 50mV/div, AC COUPLED

OUT2 LINE-TRANSIENT RESPONSE

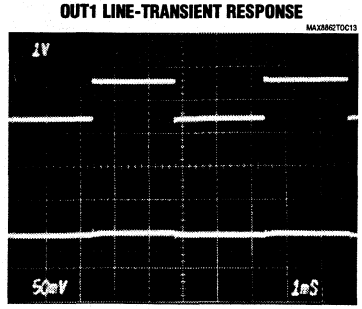


A
6.5V
5.5V
B
50mV/div

1ms/div

I_{OUT2} = 200mA, V_{OUT2} = 3.2V
A = V_{IN2}, 5.5V TO 6.5V, 1V/div
B = V_{OUT2} RIPPLE, 50mV/div, AC COUPLED

OUT1 LINE-TRANSIENT RESPONSE



A
6.5V
5.5V
B
50mV/div

1ms/div

I_{OUT1} = 300mA, V_{OUT1} = 3.2V
A = V_{IN1} = 5.5V TO 6.5V, 1V/div
B = V_{OUT1} RIPPLE, 50mV/div, AC COUPLED

Pin Description

PIN	NAME	FUNCTION
1	IN1	Main Regulator Supply Input (2.5V to 11.5V). Bypass with a 1µF, low-ESR capacitor to GND.
2	$\overline{SHDN1}$	Main Regulator Shutdown Input. A logic low turns off the main regulator and power-good comparator.
3	PWROK1	Power-Good Output. This open-drain output is low when V_{OUT1} is out of regulation (V_{OUT1} is 4% lower than its nominal value).
4, 5, 12, 13	GND	Ground. Connect to a ground plane to maximize thermal dissipation.
6	OUT2	Secondary Regulator Output. Bypass with a 2.2µF low-ESR (< 0.5Ω) capacitor to GND. To improve load-transient response and noise performance, use a higher-value, lower-ESR capacitor.
7	SET2	OUT2 Voltage-Set Input. Connect to GND for the factory-preset output voltage. Connect to a resistive divider from OUT2 to GND for adjustable output voltage.
8, 16	N.C.	No connect. There is no internal connection to this pin.
9	IN2	Secondary Regulator Supply Input (2.5V to 11.5V). Bypass with a 1µF, low-ESR capacitor to GND.
10	$\overline{SHDN2}$	Secondary Regulator Shutdown Input. A logic-low input turns off the secondary regulator and the reference.
11	REF2	Secondary Reference Output. Bypass with a 0.1µF capacitor to GND.
14	OUT1	Main Regulator Output. Bypass with a 3.3µF, low-ESR (< 0.5Ω) capacitor to GND. To improve load-transient response and noise performance, use a higher-value, lower-ESR capacitor.
15	SET1	OUT1 Voltage Set Input. Connect to GND for the factory-preset output voltage. Connect to a resistive divider from OUT1 to GND for adjustable output voltage.

Detailed Description

The MAX8862 features Dual Mode™ operation, allowing a fixed output of 4.95V (L), 3.175V (T), or 2.85V (R), or an adjustable output from 2V to 11V. The regulator's outputs, OUT1 and OUT2, supply 250mA and 100mA, respectively.

The block diagram (Figure 1) shows the contents of each regulator. Note that the main regulator provides a power-good indicator, and the secondary regulator's reference output voltage is available at REF2.

The 1.25V bandgap reference is connected to the error amplifier's inverting input. The error amplifier compares this reference with the selected feedback voltage and amplifies the difference. The MOSFET driver reads the error signal and applies the appropriate drive to the P-channel transistor. If the feedback voltage is lower than the reference, the pass transistor's gate is pulled lower, allowing more current to pass and increase the output voltage. If the feedback voltage is too high, the pass transistor's gate is pulled up, allowing less current to pass to the output.

The output voltage is fed back through either an internal resistor voltage divider connected to OUT1/OUT2, or an external resistor network connected to SET1/SET2. The Dual Mode comparator examines V_{SET1}/V_{SET2} and selects the feedback path. If this voltage is below 40mV, internal feedback is used and the output voltage is regulated to the factory-preset voltage.

Internal P-Channel Pass Transistor

The MAX8862's P-channel pass transistor provides several advantages over similar designs using PNP pass transistors, including longer battery life.

The P-channel MOSFET requires no continuous base current, thereby reducing quiescent current considerably. PNP regulators normally waste a considerable amount of current in dropout when the pass transistor saturates; they also use high base-drive currents under large loads. The MAX8862 does not suffer from these problems: it consumes only 200µA of quiescent current for both regulators under light and heavy loads, as well as in dropout.

Low-Cost, Low-Dropout, Dual Linear Regulator

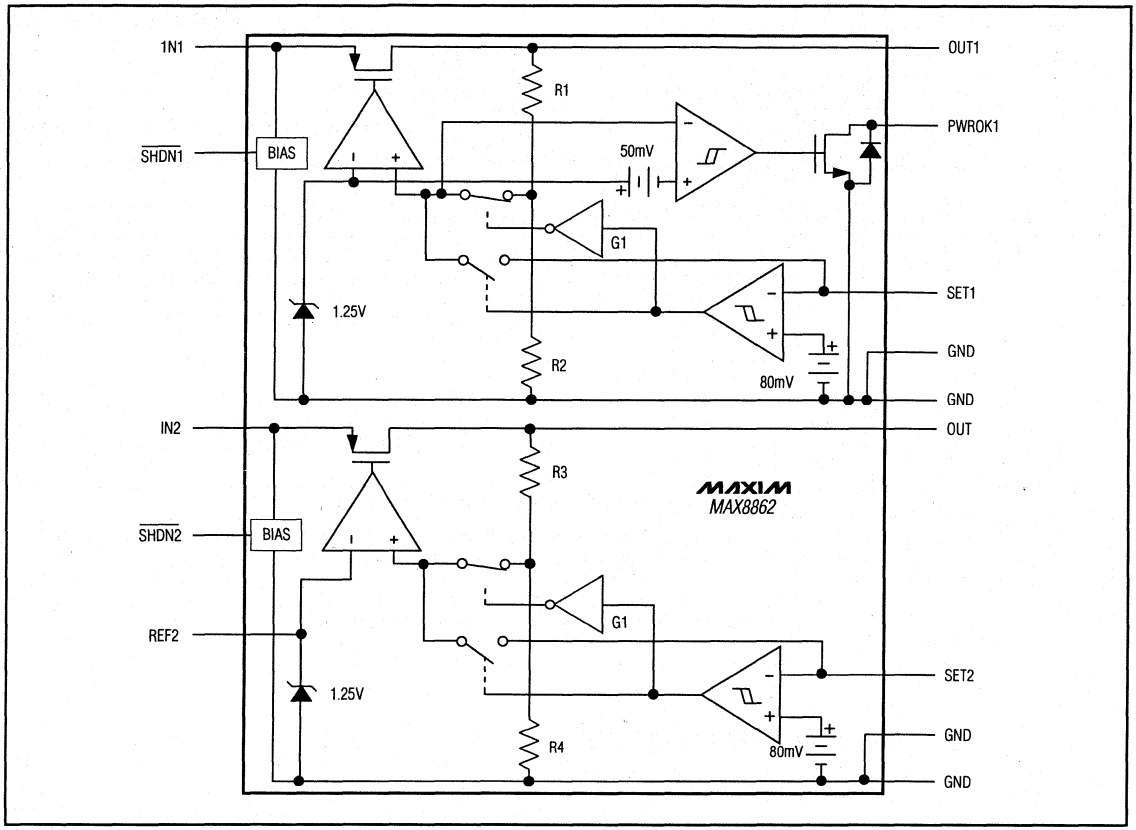


Figure 1. Functional Diagram

Output Voltage Selection

The MAX8862's Dual Mode operation allows a fixed or adjustable output voltage. In preset/internal-feedback mode (SET1/SET2 = GND), output voltages are factory preset to 4.95V (L), 3.175V (T), or 2.85V (R).

In adjustable/external feedback mode, output voltage is adjusted between 2V and 11V with two external resistors connected as a voltage divider to SET1/SET2 (Figure 2). Since the input bias current at SET1/SET2 is <0.1µA, large resistance values can be used for R1 and R2 to minimize power consumption without losing accuracy. Select R2 in the 10kΩ to 400kΩ range. R1 is given by:

$$R1 = R2 (V_{OUT} / V_{SET} - 1)$$

where V_{SET} = 1.25V.

Power-Good Comparator

The MAX8862's main regulator features a power-good indicator that asserts when the output voltage falls out of regulation. In internal-feedback mode, the open-drain PWROK1 output goes low when OUT1 falls 4% below its nominal value. When used in external feedback mode, PWROK1 goes low when V_{SET1} falls below 1.2V. A 100kΩ pull-up resistor from PWROK1 to V_{IN1} provides a logic-control signal. This resistor also minimizes current flow to the input in case the battery is reversed. PWROK1 can be used to reset a microcontroller or to drive an external LED for indicating a power failure.

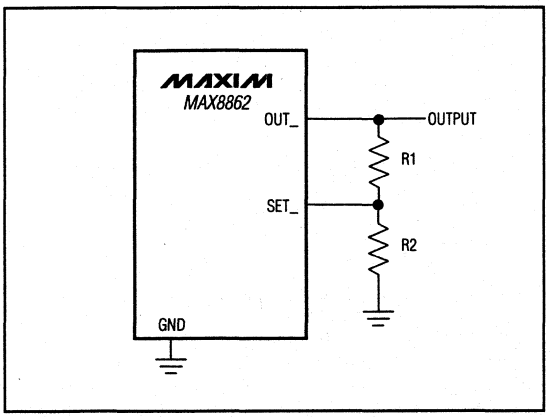


Figure 2. Adjustable Output Voltage

Reference

The MAX8862 provides a precision 1.25V reference at REF2. Bypass REF2 with a 0.1µF capacitor to ground. Larger bypassing capacitors will further reduce the secondary regulator's wideband noise.

Shutdown

The MAX8862's regulators have individual shutdown controls. A logic low on either $\overline{SHDN1}$ or $\overline{SHDN2}$ turns off the corresponding internal reference, error comparator, and pass transistors' control logic, reducing quiescent current to less than 1µA.

Current Limiting

The MAX8862 features a current limit for each regulator. It monitors and controls the pass transistor's gate voltage, limiting the output current to 580mA for the main regulator and 250mA for the secondary regulator. The current limits apply to all input and output voltage conditions. The outputs can be shorted to ground for an indefinite period of time if the package can dissipate ($V_{IN1} \times I_{LIM1} + V_{IN2} \times I_{LIM2}$) without exceeding T_J = +150°C (see the *Power Dissipation and Operating Region* section).

Thermal Overload Protection

Thermal overload protection limits the MAX8862's total power dissipation. When the junction temperature exceeds T_J = +160°C, the thermal sensor sends a signal to the shutdown logic, turning off the pass transistors and allowing the device to cool down. The thermal sensor turns the pass transistors on again after the IC's junction temperature decreases by 20°C. If the thermal overload condition persists, OUT1 and OUT2 pulse on and off.

Thermal overload protection is designed to protect the MAX8862 during fault conditions. For continuous operation, the absolute maximum junction temperature rating of T_J = +150°C should not be exceeded.

Reverse-Battery Protection

This feature protects the MAX8862 against polarity reversal at the supply inputs. The inputs can handle negative voltages up to -12V without suffering any ill effects. When the input polarity is reversed, the output will be at the same potential as ground, and no current will flow from the output back to the input. This feature protects both the device and the supply-voltage source. The reverse currents that flow back to the input are due to R_{PWROK1}, R_{SHDN1}, and R_{SHDN2}. These currents are approximately: $I_{REV1} = |V_{IN1}| / (R_{SHDN1} + R_{PWROK1})$ and $I_{REV2} = |V_{IN2}| / R_{SHDN2}$. When operating the MAX8862 in continuous mode ($V_{\overline{SHDN1}} = V_{IN1}$ and $V_{\overline{SHDN2}} = V_{IN2}$) place a resistor (>20kΩ) between shutdown and supply inputs to limit the current flow in case the battery is reversed.

Low-Cost, Low-Dropout, Dual Linear Regulator

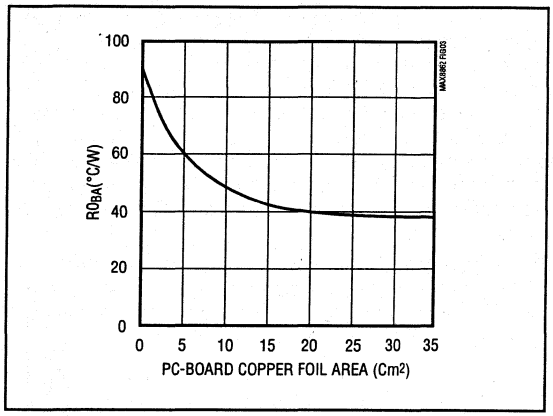


Figure 3. Typical Copper Thermal Resistance vs. Copper Ground Pad Area

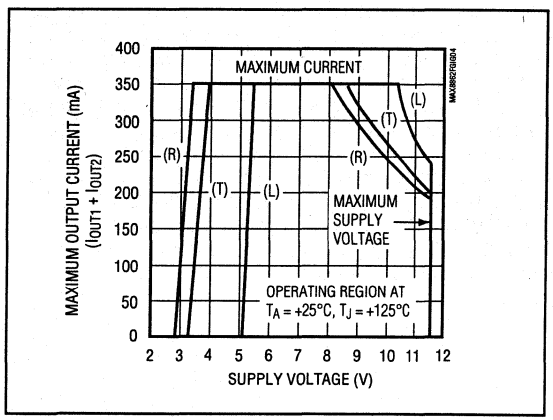


Figure 4. Safe Operating Regions: Main and Secondary Regulators Maximum Output Current vs. Supply Voltage

Applications Information

Power Dissipation and Operating Region

The MAX8862's maximum power dissipation depends on the thermal resistance of the case and circuit board, the temperature difference between the die junction and ambient air, and the rate of air flow.

The GND pins of the MAX8862 SO package perform the dual function of providing an electrical connection to ground and channeling heat away. Connect all GND pins to ground using a large pad or ground plane. Where this is impossible, place a copper plane on an adjacent layer. For a given power dissipation, the pad should exceed the associated dimensions in Figure 3. This figure shows a typical thermal resistance for a 35µm-thick copper foil as a function of its area[1].

The power dissipation across the device is given by:

$$P = I_{OUT1} (V_{IN1} - V_{OUT1}) + I_{OUT2} (V_{IN2} - V_{OUT2}).$$

The resulting power dissipation is as follows:

$$P = (T_J - T_A) / (\theta_{JB} + \theta_{BA})$$

where $(T_J - T_A)$ is the temperature difference between the MAX8862 die junction and the surrounding air, θ_{JB} (or θ_{JC}) is the thermal resistance of the package, and θ_{BA} is the thermal resistance through the printed circuit board, copper traces, and other materials to the surrounding air. The MAX8862's narrow SO package has a thermal resistance of θ_{JB} = +50°C/W.

The MAX8862 regulators deliver the rated output currents and operate with input voltages up to 11.5V, but not simultaneously. High output currents can only be sustained when input-output differential voltages are small, as shown in Figure 4.

Capacitor Selection and Regulator Stability

Filter capacitors are required at the MAX8862's inputs and outputs. 1µF ceramic capacitors are required at the inputs. The minimum output capacitance required for stability is 3.3µF for OUT1 and 2.2µF for OUT2. The capacitor values depend primarily on the desired power-up time and load-transient response. Load-transient response is improved by using larger capacitor values. Input and output filter capacitors should be soldered directly to pins to minimize lead inductance of PC board traces.

The output capacitor's equivalent series resistance (ESR) affects stability and output noise. Surface-mount ceramic capacitors have a very low ESR and are available up to 10µF. Otherwise, other low-ESR (<0.5Ω) capacitors should be used. If the selected capacitor's ESR is higher than the recommended value, the capacitor value should be increased proportionally to maintain minimum output noise under all input voltage and output load conditions. Paralleling two or more capacitors also results in lower ESR.

[1]This graph was generated by Mr. Kieran O'Malley of Cherry Semiconductor Corp. and was published in the October 26, 1995, issue of EDN magazine.

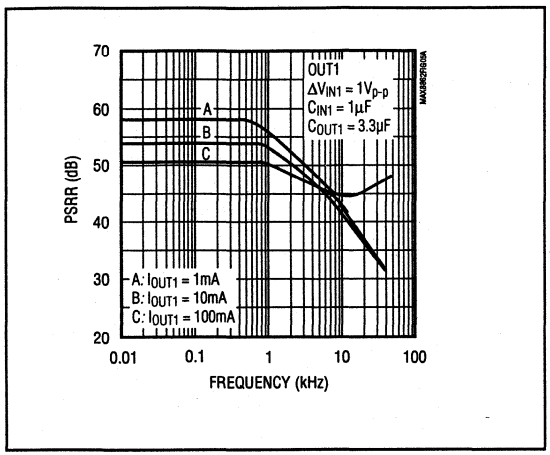


Figure 5a. Power-Supply Rejection Ratio vs. Ripple Frequency for Light and Heavy Loads

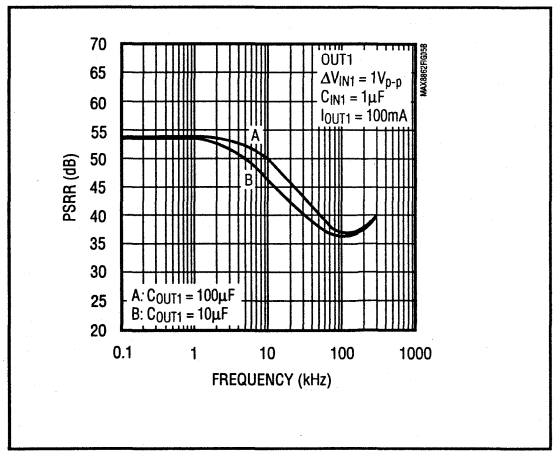


Figure 5b. Power-Supply Rejection Ratio vs. Ripple Frequency for Various Output Capacitors

Noise

The MAX8862's OUT1 exhibits about 2.5mVp-p, and OUT2 exhibits 1mVp-p of noise under full-load conditions. When using the MAX8862 for applications that include analog-to-digital converters (ADCs) with resolutions greater than 12 bits, consider the ADC's power-supply-rejection specifications.

PSRR and Operation from Sources Other than Batteries

The MAX8862 is designed to achieve low dropout voltages and low quiescent currents in battery-powered systems. However, to gain these benefits; the device must trade away power-supply noise rejection, as well as swift response to supply variations and load transients. For a 1mA load current, power-supply rejection typically changes from 58dB to 43dB when the input frequency is changed from 1Hz to 10kHz. At higher frequencies, the circuit depends primarily on the output capacitor's characteristics, and the PSRR increases (Figure 5).

When operating from sources other than batteries, supply-noise rejection and transient response can be improved by increasing the value of the input and output capacitors and employing passive filtering techniques. Do not use power supplies with ripple voltages exceeding 200mV at 100kHz.

Overshoot and Transient Considerations

The *Typical Operating Characteristics* section shows power-up, line, and load-transient response graphs. Typical transients for step changes in the load current from 0mA to 300mA are 100mVp-p. During recovery from shutdown, overshoot is minimized by the 1µF input, and output capacitors (3.3µF for OUT1, and 2.2µF for OUT2).

Input-Output (Dropout) Voltage

A regulator's minimum input-to-output voltage differential (or dropout voltage) determines the lowest usable supply voltage. In battery-powered systems, this determines the useful end-of-life battery voltage. Since P-channel MOSFETs are used as pass transistors, the dropout voltage is the product of the $R_{DS(ON)}$ and the load current (see the *Electrical Characteristics*).

Chip Information

TRANSISTOR COUNT: 457

19-0466; Rev 0; 3/96

MAXIM

Low-Dropout, 100mA Linear Regulators

General Description

The MAX8863T/S/R and MAX8864T/S/R low-dropout linear regulators operate from a +2.5V to +5.5V input range and deliver up to 100mA. A PMOS pass transistor allows the low, 80µA supply current to remain independent of load, making these devices ideal for battery-operated portable equipment such as cellular phones, cordless phones, and modems.

The devices feature Dual Mode™ operation: their output voltage is preset (at 3.15V for the T versions, 2.84V for the S versions, or 2.80V for the R versions) or can be adjusted with an external resistor divider. Other features include low-power shutdown, short-circuit protection, thermal shutdown protection, and reverse battery protection. The MAX8864 also includes an auto-discharge function, which actively discharges the output voltage to ground when the device is placed in shutdown mode. Both devices come in a miniature 5-pin SOT23-5 package.

Features

- ♦ **Low Cost**
- ♦ **Low, 55mV Dropout Voltage @ 50mA I_{OUT}**
- ♦ **Low, 68µA No-Load Supply Current**
  Low, 80µA Operating Supply Current (even in dropout)
- ♦ **Low, 350µV_{RMS} Output Noise**
- ♦ **Miniature External Components**
- ♦ **Thermal Overload Protection**
- ♦ **Output Current Limit**
- ♦ **Reverse Battery Protection**
- ♦ **Dual Mode™ Operation: Fixed or Adjustable (1.25V to 5.5V) Output**
- ♦ **Low-Power Shutdown**

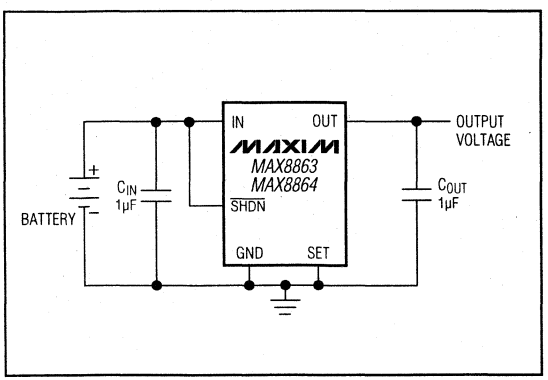
Applications

Cordless Telephones	Modems
PCS Telephones	Hand-Held Instruments
Cellular Telephones	Palmtop Computers
PCMCIA Cards	Electronic Planners

Ordering Information

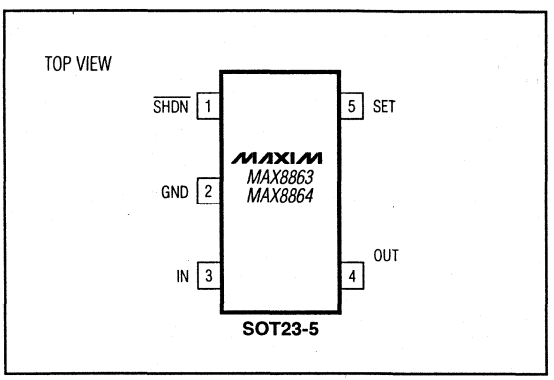
PART	TEMP. RANGE	PIN-PACKAGE	PRESET V_{OUT} (V)
MAX8863TEUK-T	-40°C to +85°C	5 SOT23-5	3.15
MAX8863SEUK-T	-40°C to +85°C	5 SOT23-5	2.84
MAX8863REUK-T	-40°C to +85°C	5 SOT23-5	2.80
MAX8864TEUK-T	-40°C to +85°C	5 SOT23-5	3.15
MAX8864SEUK-T	-40°C to +85°C	5 SOT23-5	2.84
MAX8864REUK-T	-40°C to +85°C	5 SOT23-5	2.80

Typical Operating Circuit



Dual Mode is a trademark of Maxim Integrated Products.

Pin Configuration



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Low-Dropout, 100mA Linear Regulators

ABSOLUTE MAXIMUM RATINGS

V_{IN} to GND .....-6V to +6V
Output Short-Circuit Duration .....Infinite
SET to GND .....-0.3V to +6V
$\overline{SHDN}$ to GND.....-6V to +6V
$\overline{SHDN}$ to IN .....-6V to +0.3V
OUT to GND .....-0.3V to (V_{IN} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
SOT23-5 (derate 7.1mW/°C above +70°C).....571mW

Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
θ_{JA}.....140°C/Watt
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = +3.6V, GND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage (Note 2)	V_{IN}			2.5		5.5	V
Output Voltage	V_{OUT}	0mA ≤ I_{OUT} ≤ 50mA, SET = GND	MAX886_T	3.05	3.15	3.25	V
			MAX886_S	2.75	2.84	2.93	
			MAX886_R	2.70	2.80	2.88	
Adjustable Output Voltage Range (Note 3)	V_{OUT}			V_{SET}		5.5	V
Maximum Output Current				100			mA
Current Limit (Note 4)	I_{LIM}				220		mA
Ground Pin Current	I_Q	SET = GND	I_{LOAD} = 0mA		68	150	µA
			I_{LOAD} = 50mA		80		
Dropout Voltage (Note 5)		I_{OUT} = 1mA			1.1		mV
		I_{OUT} = 50mA			55	120	
Line Regulation	ΔV_{LNR}	V_{IN} = 2.5V to 5.5V, SET tied to OUT, I_{OUT} = 1mA		-0.10	0	0.10	%/V
Load Regulation	ΔV_{LDR}	I_{OUT} = 0mA to 50mA	SET = GND		0.011	0.040	%/mA
			SET tied to OUT		0.006		
Output Voltage Noise		10Hz to 1MHz	C_{OUT} = 1µF		350		μV_{RMS}
			C_{OUT} = 100µF		220		
SHUTDOWN							
$\overline{SHDN}$ Input Threshold	V_{IH}			2.0			V
	V_{IL}					0.4	
$\overline{SHDN}$ Input Bias Current	$I_{\overline{SHDN}}$	$V_{\overline{SHDN}}$ = V_{IN}	T_A = +25°C		0	2.5	nA
			T_A = T_{MAX}		0.05		
Shutdown Supply Current	I_{QSHDN}	V_{OUT} = 0V	T_A = +25°C		0.08	50	nA
			T_A = T_{MAX}		20		
Shutdown to Output Discharge Delay (MAX8864)		C_{OUT} = 1µF, no load			1		ms

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +3.6V, GND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

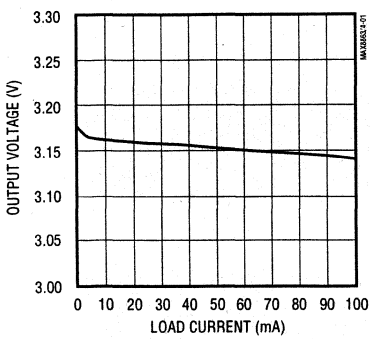
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SET INPUT							
SET Reference Voltage (Note 3)	V_{SET}	V_{IN} = 2.5V to 5.5V, I_{OUT} = 1mA	T_A = +25°C	1.225	1.25	1.275	V
			T_A = T_{MIN} to T_{MAX}	1.215	1.25	1.285	
SET Input Leakage Current (Note 3)	I_{SET}	V_{SET} = 1.3V	T_A = +25°C		0.015	2.5	nA
			T_A = T_{MAX}		0.5		
THERMAL PROTECTION							
Thermal Shutdown Temperature	T_{SHDN}				170		°C
Thermal Shutdown Hysteresis	ΔT_{SHDN}				20		°C

Note 1: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) Methods.
Note 2: Guaranteed by line regulation test.
Note 3: Adjustable mode only.
Note 4: Not tested. For design purposes, the current limit should be considered 120mA minimum to 320mA maximum.
Note 5: The dropout voltage is defined as (V_{IN} - V_{OUT}) when V_{OUT} is 100mV below the value of V_{OUT} for V_{IN} = V_{OUT} +2V.

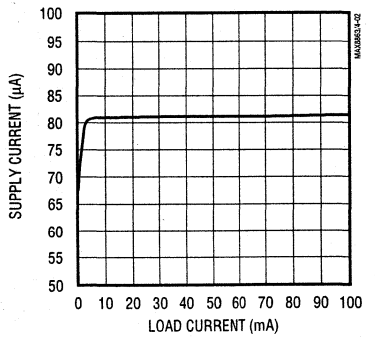
Typical Operating Characteristics

(V_{IN} = +3.6V, C_{IN} = 1µF, C_{OUT} = 1µF, T_A = +25°C, MAX886_T, unless otherwise noted.)

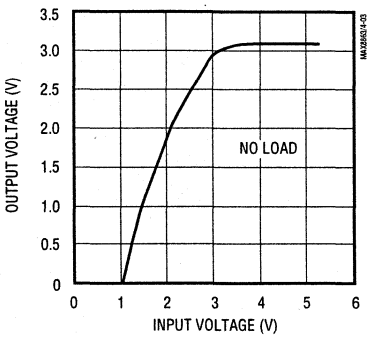
OUTPUT VOLTAGE vs. LOAD CURRENT



SUPPLY CURRENT vs. LOAD CURRENT



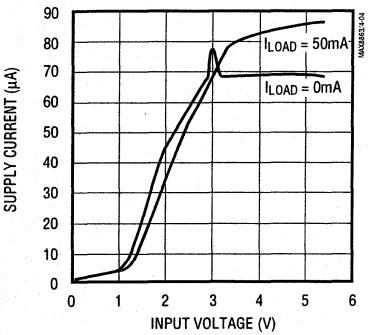
OUTPUT VOLTAGE vs. INPUT VOLTAGE



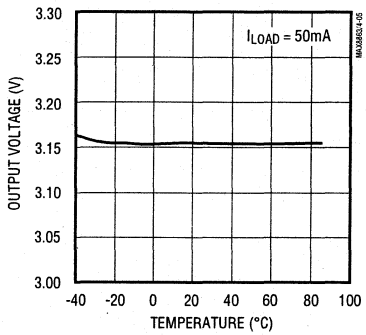
Typical Operating Characteristics (continued)

(V_{IN} = +3.6V, C_{IN} = 1µF, C_{OUT} = 1µF, MAX886_T, T_A = +25°C, unless otherwise noted.)

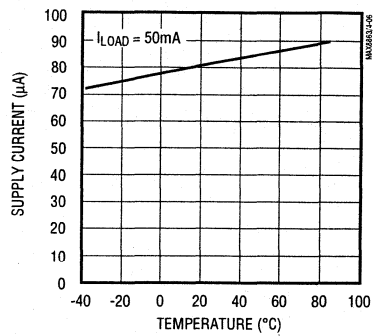
SUPPLY CURRENT vs. INPUT VOLTAGE



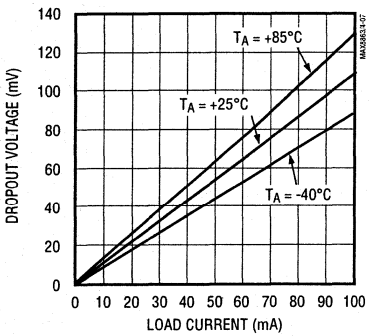
OUTPUT VOLTAGE vs. TEMPERATURE



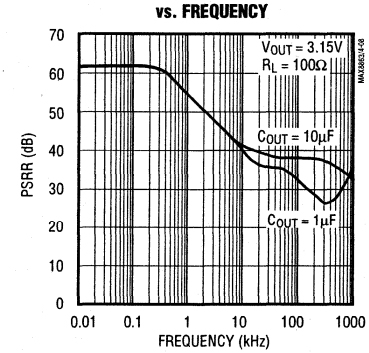
SUPPLY CURRENT vs. TEMPERATURE



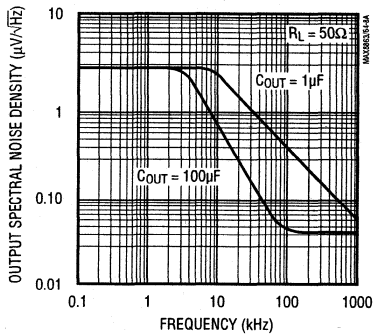
DROPOUT VOLTAGE vs. LOAD CURRENT



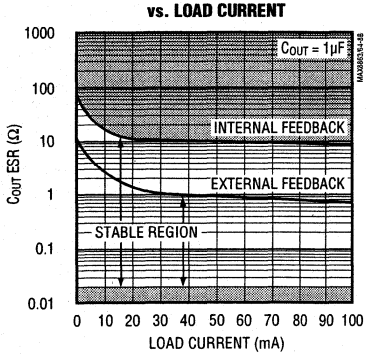
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



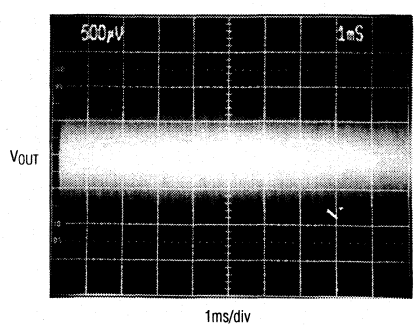
OUTPUT SPECTRAL NOISE DENSITY vs. FREQUENCY



REGION OF STABLE COUT ESR vs. LOAD CURRENT



OUTPUT NOISE DC TO 1MHz

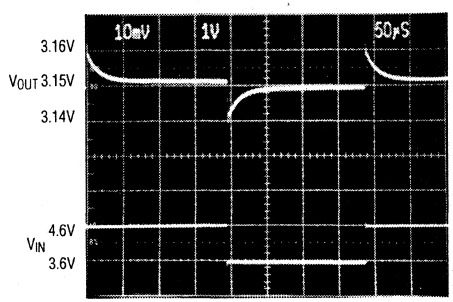


ILOAD = 50mA, VOUT IS AC COUPLED

Typical Operating Characteristics (continued)

(V_{IN} = +3.6V, C_{IN} = 1µF, C_{OUT} = 1µF, MAX886_T, T_A = +25°C, unless otherwise noted.)

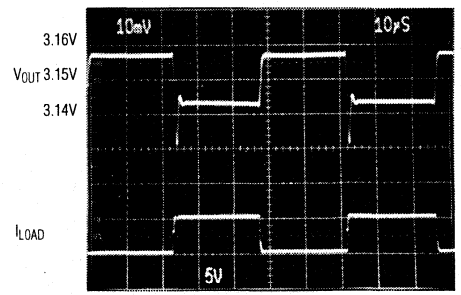
LINE TRANSIENT



50µs/div

I_{LOAD} = 50mA, V_{OUT} IS AC COUPLED

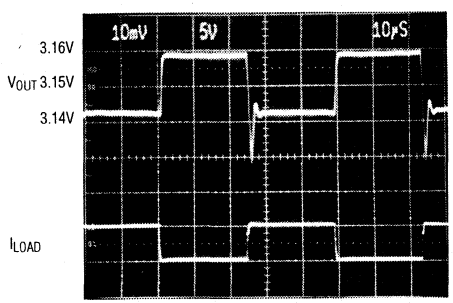
LOAD TRANSIENT



10µs/div

I_{LOAD} = 0mA to 50mA, C_{IN} = 10µF, V_{OUT} IS AC COUPLED

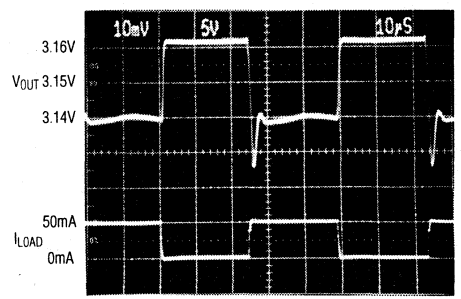
LOAD TRANSIENT



10µs/div

V_{IN} = V_{OUT} + 0.2V, I_{LOAD} = 0mA to 50mA, C_{IN} = 10µF, V_{OUT} IS AC COUPLED

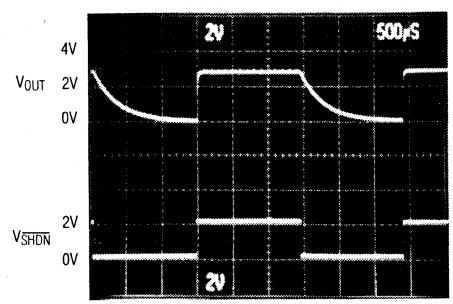
LOAD TRANSIENT



10µs/div

V_{IN} = V_{OUT} + 0.1V, I_{LOAD} = 0mA to 50mA, C_{IN} = 10µF, V_{OUT} IS AC COUPLED

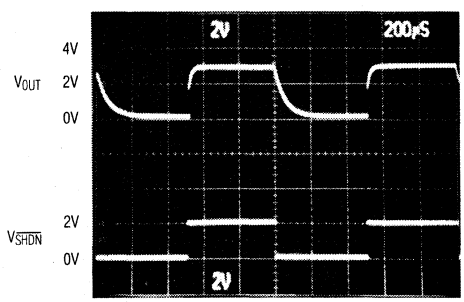
MAX8864 SHUTDOWN (NO LOAD)



500µs/div

NO LOAD

MAX8864 SHUTDOWN



200µs/div

I_{LOAD} = 50mA

Low-Dropout, 100mA Linear Regulators

Pin Description

PIN	NAME	FUNCTION
1	$\overline{SHDN}$	Active-Low Shutdown Input. A logic low reduces the supply current to 0.08nA. On the MAX8864, a logic low also causes the output voltage to discharge to GND. Connect to IN for normal operation.
2	GND	Ground. This pin also functions as a heatsink. Solder to large pads or the circuit board ground plane to maximize thermal dissipation.
3	IN	Regulator Input. Supply voltage can range from +2.5V to +5.5V. Bypass with 1µF to GND (see *Capacitor Selection and Regulator Stability*).
4	OUT	Regulator Output. Fixed or adjustable from 1.25V to 5.5V. Sources up to 100mA. Bypass with a 1µF, <0.2Ω typical ESR capacitor to GND.
5	SET	Feedback Input for Setting the Output Voltage. Connect to GND to set the output voltage to the preset 2.80V (MAX886_R), 2.84V (MAX886_S), or 3.15V (MAX886_T). Connect to an external resistor divider for adjustable-output operation.

Detailed Description

The MAX8863/MAX8864 are low-dropout, low-quiescent-current linear regulators designed primarily for battery-powered applications. They supply an adjustable 1.25V to 5.5V output or a preselected 2.80V (MAX886_R), 2.84V (MAX886_S), or 3.15V (MAX886_T) output for load currents up to 100mA. As illustrated in Figure 1, these devices consist of a 1.25V reference, error amplifier, MOSFET driver, P-channel pass transistor, Dual Mode™ comparator, and internal feedback voltage divider.

The 1.25V bandgap reference is connected to the error amplifier's inverting input. The error amplifier compares this reference with the selected feedback voltage and amplifies the difference. The MOSFET driver reads the error signal and applies the appropriate drive to the P-channel pass transistor. If the feedback voltage is lower than the reference, the pass-transistor gate is pulled lower, allowing more current to pass and increasing the output voltage. If the feedback voltage is too high, the pass-transistor gate is pulled up, allowing less current to pass to the output.

The output voltage is fed back through either an internal resistor voltage divider connected to the OUT pin, or an external resistor network connected to the SET pin. The Dual Mode comparator examines the SET voltage and selects the feedback path. If SET is below 60mV, internal feedback is used and the output voltage is regulated to the preset output voltage. Additional blocks include a current limiter, reverse battery protection, thermal sensor, and shutdown logic.

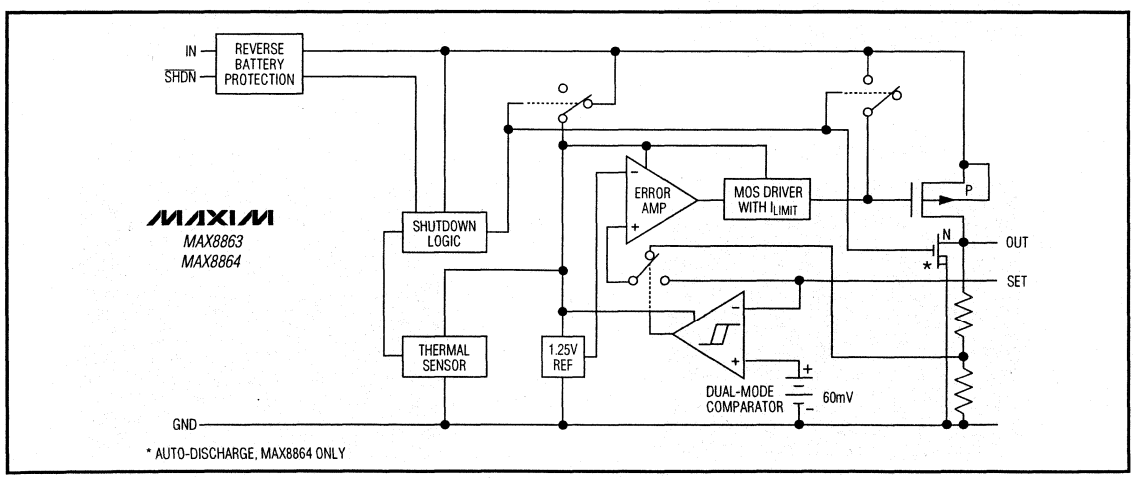


Figure 1. Functional Diagram

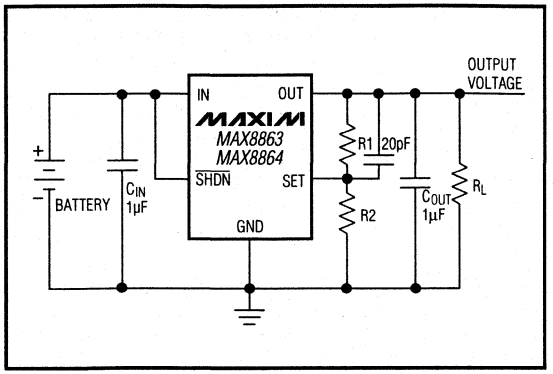


Figure 2. Adjustable Output Using External Feedback Resistors

Internal P-Channel Pass Transistor

The MAX8863/MAX8864 feature a 1.1Ω typical P-channel MOSFET pass transistor. This provides several advantages over similar designs using PNP pass transistors, including longer battery life.

The P-channel MOSFET requires no base drive current, which reduces quiescent current considerably. PNP-based regulators waste considerable amounts of current in dropout when the pass transistor saturates. They also use high base-drive currents under large loads. The MAX8863/MAX8864 do not suffer from these problems, and consume only 80µA of quiescent current, whether in dropout, light load, or heavy load applications (see *Typical Operating Characteristics*).

Output Voltage Selection

The MAX8863/MAX8864 feature Dual Mode operation: they operate in either a preset voltage mode or an adjustable mode.

In preset voltage mode, internal, trimmed feedback resistors set the MAX886_R output to 2.80V, the MAX886_S output to 2.84V, and the MAX886_T output to 3.15V. Select this mode by connecting SET to ground.

In adjustable mode, select an output between 1.25V and 5.5V using two external resistors connected as a voltage divider to SET (Figure 2). The output voltage is set by the following equation:

$$V_{OUT} = V_{SET} (1 + R1 / R2)$$

where V_{SET} = 1.25V. To simplify resistor selection:

$$R1 = R2 \left(\frac{V_{OUT}}{V_{SET}} - 1 \right)$$

Choose R2 = 100kΩ to optimize power consumption, accuracy, and high-frequency power-supply rejection. The total current through the external resistive feedback and load resistors should not be less than 10µA. Since the V_{SET} tolerance is typically less than ±25mV, the output can be set using fixed resistors instead of trim pots. Connect a 10pF to 25pF capacitor across R1 to compensate for layout-induced parasitic capacitances.

In preset voltage mode, impedances between SET and ground should be less than 100kΩ. Otherwise, spurious conditions could cause the voltage at SET to exceed the 60mV Dual Mode threshold.

Shutdown

A low input on the $\overline{SHDN}$ pin shuts down the MAX8863/MAX8864. In shutdown mode, the pass transistor, control circuit, reference, and all biases are turned off, reducing the supply current to typically 0.08nA. Connect $\overline{SHDN}$ to IN for normal operation. The MAX8864 output voltage is actively discharged to ground when the part is placed in shutdown (see *Typical Operating Characteristics*).

Current Limit

The MAX8863/MAX8864 include a current limiter that monitors and controls the pass transistor's gate voltage, estimating the output current and limiting it to about 220mA. For design purposes, the current limit should be considered 120mA (min) to 320mA (max). The output can be shorted to ground for an indefinite time period without damaging the part.

Thermal Overload Protection

Thermal overload protection limits total power dissipation in the MAX8863/MAX8864. When the junction temperature exceeds T_J = +170°C, the thermal sensor sends a signal to the shutdown logic, turning off the pass transistor and allowing the IC to cool. The thermal sensor will turn the pass transistor on again after the IC's junction temperature typically cools by 20°C, resulting in a pulsed output during continuous thermal overload conditions.

Thermal overload protection is designed to protect the MAX8863/MAX8864 in the event of fault conditions. Stressing the device with high load currents and high input-output differential voltages (which result in die temperatures above +125°C) may cause a momentary overshoot (2% to 8% for 200ms) when the load is completely removed. This can be remedied by raising the minimum load current from 0µA (+125°C) to 100µA (+150°C). For continuous operation, do not exceed the absolute maximum junction temperature rating of T_J = +150°C.

Operating Region and Power Dissipation

Maximum power dissipation of the MAX8863/MAX8864 depends on the thermal resistance of the case and circuit board, the temperature difference between the die junction and ambient air, and the rate of air flow. The power dissipation across the device is $P = I_{OUT} (V_{IN} - V_{OUT})$. The resulting maximum power dissipation is:

$$P_{MAX} = (T_J - T_A) / \theta_{JA}$$

where $(T_J - T_A)$ is the temperature difference between the MAX8863/MAX8864 die junction and the surrounding air, and θ_{JA} is the thermal resistance of the chosen package to the surrounding air.

The GND pin of the MAX8863/MAX8864 performs the dual function of providing an electrical connection to ground and channeling heat away. Connect the GND pin to ground using a large pad or ground plane.

Reverse Battery Protection

The MAX8863/MAX8864 have a unique protection scheme that limits the reverse supply current to less than 1mA when either V_{IN} or $V_{\overline{SHDN}}$ falls below ground. The circuitry monitors the polarity of these two pins, disconnecting the internal circuitry and parasitic diodes when the battery is reversed. This feature prevents the device from overheating and damaging the battery.

Applications Information

Capacitor Selection and Regulator Stability

Normally, use a 1µF capacitor on the input and a 1µF capacitor on the output of the MAX8863/MAX8864. Larger input capacitor values and lower ESR provide better supply-noise rejection and transient response. A higher-value input capacitor (10µF) may be necessary if large, fast transients are anticipated and the device is located several inches from the power source. Improve load-transient response, stability, and power-supply rejection by using large output capacitors. For stable operation over the full temperature range, with load currents up to 100mA, a minimum of 1µF is recommended.

Noise

The MAX8863/MAX8864 exhibit $350\mu V_{RMS}$ noise during normal operation. When using the MAX8863/MAX8864 in applications that include analog-to-digital converters of greater than 12 bits, consider the ADC's power-supply rejection specifications (see the Output Noise DC to 1MHz photo in the *Typical Operating Characteristics*).

Power-Supply Rejection and Operation from Sources Other than Batteries

The MAX8863/MAX8864 are designed to deliver low dropout voltages and low quiescent currents in battery-powered systems. Power-supply rejection is 62dB at low frequencies and rolls off above 300Hz. As the frequency increases above 20kHz, the output capacitor is the major contributor to the rejection of power-supply noise (see the Power-Supply Rejection Ratio vs. Ripple Frequency graph in the *Typical Operating Characteristics*).

When operating from sources other than batteries, improve supply-noise rejection and transient response by increasing the values of the input and output capacitors, and using passive filtering techniques (see the supply and load-transient responses in the *Typical Operating Characteristics*).

Load Transient Considerations

The MAX8863/MAX8864 load-transient response graphs (see *Typical Operating Characteristics*) show two components of the output response: a DC shift of the output voltage due to the different load currents, and the transient response. Typical overshoot for step changes in the load current from 0mA to 50mA is 12mV. Increasing the output capacitor's value and decreasing its ESR attenuates transient spikes.

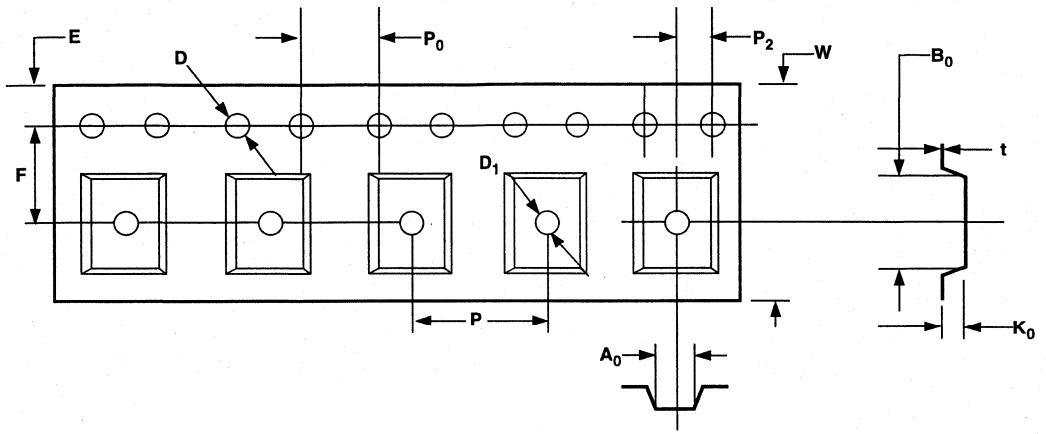
Input-Output (Dropout) Voltage

A regulator's minimum input-output voltage differential (or dropout voltage) determines the lowest usable supply voltage. In battery-powered systems, this will determine the useful end-of-life battery voltage. Because the MAX8863/MAX8864 use a P-channel MOSFET pass transistor, their dropout voltage is a function of $R_{DS(ON)}$ multiplied by the load current (see *Electrical Characteristics*).

Chip Information

TRANSISTOR COUNT: 148

Ordering Information (continued)



A_0	3.200	±0.102
B_0	3.099	±0.102
D	1.499	+0.102 +0.000
D_1	0.991	+0.254 +0.000
E	1.753	±0.102
F	3.505	±0.051
K_0	1.397	±0.102

NOTE: DIMENSIONS ARE IN MM.
AND FOLLOW EIA481-1 STANDARD.

P	3.988	±0.102
P_0	3.988	±0.102
$P_0$10	40.005	±0.203
P_2	2.007	±0.051
t	0.254	±0.127
W	8.001	+0.305 -0.102

19-0485; Rev 0; 4/96

MAXIM

Dual, Low-Dropout, 100mA Linear Regulators

General Description

The MAX8865 and MAX8866 dual, low-dropout linear regulators operate from a +2.5V to +5.5V input range and deliver up to 100mA. At 200mA total load, the PMOS pass transistors keep the supply current at 145µA, making these devices ideal for battery-operated portable equipment such as cellular phones, cordless phones, and modems.

The devices feature Dual Mode™ operation: their output voltages are preset (at 3.15V for the "T" versions, 2.84V for the "S" versions, or 2.80V for the "R" versions) or can be adjusted with external resistor dividers. Other features include independent low-power shutdown, short-circuit protection, thermal shutdown protection, and reverse battery protection. The MAX8866 also includes an auto-discharge function, which actively discharges the selected output voltage to ground when the device is placed in shutdown mode. Both devices come in a miniature 8-pin µMAX package.

Features

- ♦ **Low Cost**
- ♦ **Low, 55mV Dropout Voltage @ 50mA I_{OUT}**
- ♦ **Low, 105µA No-Load Supply Current**
- ♦ **Low, 145µA Operating Supply Current (even in dropout)**
- ♦ **Low, 350µV_{RMS} Output Noise**
- ♦ **Independent, Low-Current Shutdown Control**
- ♦ **Thermal Overload Protection**
- ♦ **Output Current Limit**
- ♦ **Reverse Battery Protection**
- ♦ **Dual Mode Operation: Fixed or Adjustable (1.25V to 5.5V) Outputs**

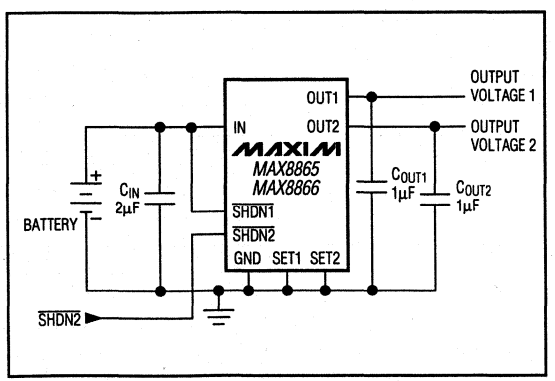
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	PRESET V_{OUT} (V)
MAX8865TEUA	-40°C to +85°C	8 µMAX	3.15
MAX8865SEUA	-40°C to +85°C	8 µMAX	2.84
MAX8865REUA	-40°C to +85°C	8 µMAX	2.80
MAX8866TEUA	-40°C to +85°C	8 µMAX	3.15
MAX8866SEUA	-40°C to +85°C	8 µMAX	2.84
MAX8866REUA	-40°C to +85°C	8 µMAX	2.80

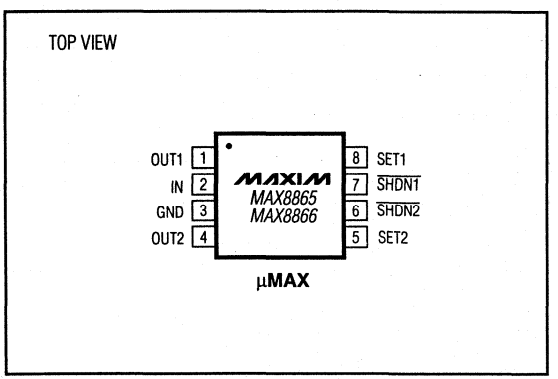
Applications

Cordless Telephones	Modems
PCS Telephones	Hand-Held Instruments
Cellular Telephones	Palmtop Computers
PCMCIA Cards	Electronic Planners

Typical Operating Circuit



Pin Configuration



Dual Mode is a trademark of Maxim Integrated Products.

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Dual, Low-Dropout, 100mA Linear Regulators

ABSOLUTE MAXIMUM RATINGS

V_{IN} to GND .....-6V to +6V
Output Short-Circuit Duration .....Infinite
SET_ to GND .....-0.3V to +6V
$\overline{SHDN}$_ to GND .....-6V to +6V
$\overline{SHDN}$_ to IN .....-6V to +0.3V
OUT_ to GND.....-0.3V to (V_{IN} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
μMAX (derate 4.1mW/°C above +70°C).....330mW

Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Thermal Resistance (θ_{JA}).....244°C/W
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = +3.6V, GND = 0V, T_A = 0°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage (Note 1)	V_{IN}			2.5		5.5	V
Output Voltage	$V_{OUT_}$	0mA ≤ I_{OUT} ≤ 50mA, SET_ = GND	MAX886_T	3.08	3.15	3.24	V
			MAX886_S	2.77	2.84	2.91	
			MAX886_R	2.73	2.80	2.87	
Adjustable Output Voltage Range (Note 2)	$V_{OUT_}$			$V_{SET_}$		5.5	V
Maximum Output Current				100			mA
Current Limit (Note 3)	I_{LIM}				220		mA
Ground Pin Current	I_Q	SET_ = GND	$I_{OUT_}$ = 0mA		105	270	μA
			$I_{OUT_}$ = 50mA		145		
Dropout Voltage (Note 4)		I_{OUT} = 1mA			1.1		mV
		I_{OUT} = 50mA			55	120	
Line Regulation	ΔV_{LNR}	V_{IN} = 2.5V to 5.5V, SET_ tied to OUT_, $I_{OUT_}$ = 1mA		-0.10	0	0.10	%/V
Load Regulation	ΔV_{LDR}	$I_{OUT_}$ = 0mA to 50mA	SET_ = GND		0.012	0.03	%/mA
			SET_ tied to OUT_		0.006		
Output Voltage Noise		10Hz to 1MHz	C_{OUT} = 1μF		350		μV_{RMS}
			C_{OUT} = 100μF		220		
SHUTDOWN							
$\overline{SHDN}$ Input Threshold	V_{IH}			2.0			V
	V_{IL}					0.4	
$\overline{SHDN}$ Input Bias Current	$I_{\overline{SHDN}_}$	$V_{\overline{SHDN}_}$ = V_{IN}			0	1000	nA
Shutdown Supply Current	I_Q SHDN	$V_{OUT_}$ = 0V			0.16	3000	nA
Shutdown to Output Discharge Delay (MAX8866)		C_{OUT} = 1μF, no load			1		ms
SET INPUT							
SET Reference Voltage (Note 2)	$V_{SET_}$	V_{IN} = 2.5V to 5.5V, $I_{OUT_}$ = 1mA		1.222	1.25	1.276	V
SET Input Leakage Current (Note 2)	$I_{SET_}$	$V_{SET_}$ = 1.3V			0.015	50	nA
THERMAL PROTECTION							
Thermal Shutdown Temperature	T_{SHDN}				170		°C
Thermal Shutdown Hysteresis	ΔT_{SHDN}				20		°C

ELECTRICAL CHARACTERISTICS

(V_{IN} = +3.6V, GND = 0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage (Note 1)	V_{IN}			2.5		5.5	V
Output Voltage	$V_{OUT_}$	0mA ≤ I_{OUT} ≤ 50mA, SET_ = GND	MAX886_T	3.05	3.15	3.26	V
			MAX886_S	2.74	2.84	2.93	
			MAX886_R	2.70	2.80	2.89	
Adjustable Output Voltage Range (Note 2)	$V_{OUT_}$			$V_{SET_}$		5.5	V
Maximum Output Current				80			mA
Current Limit (Note 3)	I_{LIM}				220		mA
Ground Pin Current	I_Q	SET_ = GND	$I_{OUT_}$ = 0mA		105	270	µA
			$I_{OUT_}$ = 50mA		145		
Dropout Voltage (Note 4)		I_{OUT} = 1mA			1.1		mV
		I_{OUT} = 50mA			55	120	
Line Regulation	ΔV_{LNR}	V_{IN} = 2.5V to 5.5V, SET_ tied to OUT_, $I_{OUT_}$ = 1mA		-0.11	0	0.11	%/V
Load Regulation	ΔV_{LDR}	$I_{OUT_}$ = 0mA to 50mA	SET_ = GND		0.012	0.03	%/mA
			SET_ tied to OUT_		0.006		
Output Voltage Noise		10Hz to 1MHz	C_{OUT} = 1µF		350		μV_{RMS}
			C_{OUT} = 100µF		220		
SHUTDOWN							
$\overline{SHDN}$ Input Threshold	V_{IH}			2.0			V
	V_{IL}					0.4	
$\overline{SHDN}$ Input Bias Current	$I_{\overline{SHDN}_}$	$V_{\overline{SHDN}_}$ = V_{IN}			0	1000	nA
Shutdown Supply Current	I_Q SHDN	$V_{OUT_}$ = 0V			0.16	3000	nA
Shutdown to Output Discharge Delay (MAX8866)		C_{OUT} = 1µF			1		ms
SET INPUT							
SET Reference Voltage (Note 2)	$V_{SET_}$	V_{IN} = 2.5V to 5.5V, $I_{OUT_}$ = 1mA		1.207	1.25	1.288	V
SET Input Leakage Current (Note 2)	$I_{SET_}$	$V_{SET_}$ = 1.3V			0.015	50	nA
THERMAL PROTECTION							
Thermal Shutdown Temperature	T_{SHDN}				170		°C
Thermal Shutdown Hysteresis	ΔT_{SHDN}				20		°C

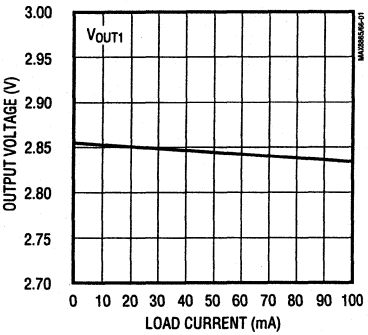
Note 1: Guaranteed by line regulation test.
Note 2: Adjustable mode only.
Note 3: Not tested. For design purposes, the current limit should be considered 120mA minimum to 320mA maximum.
Note 4: The dropout voltage is defined as ($V_{IN_}$ - $V_{OUT_}$) when $V_{OUT_}$ is 100mV below the value of $V_{OUT_}$ for $V_{IN_}$ = $V_{OUT_}$ +2V.
Note 5: Specifications to -40°C are guaranteed by design and not production tested.

Dual, Low-Dropout, 100mA Linear Regulators

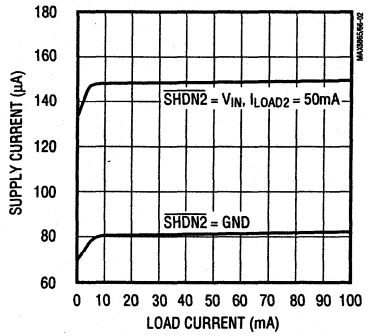
Typical Operating Characteristics

(V_{IN} = +3.6V, C_{IN} = 2µF, C_{OUT} = 1µF, $\overline{SHDN2}$ = GND, MAX886_S, T_A = +25°C, unless otherwise noted.)

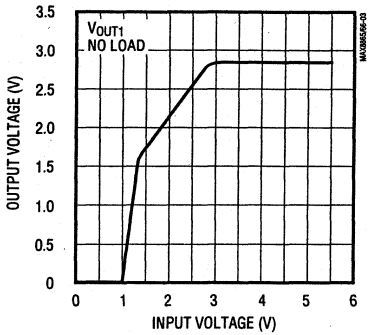
OUTPUT VOLTAGE vs. LOAD CURRENT



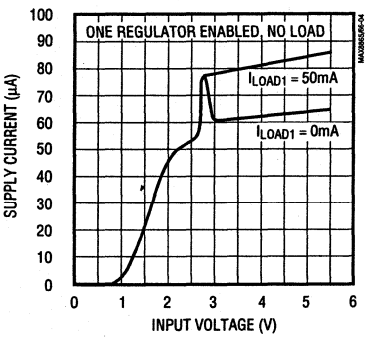
SUPPLY CURRENT vs. LOAD CURRENT



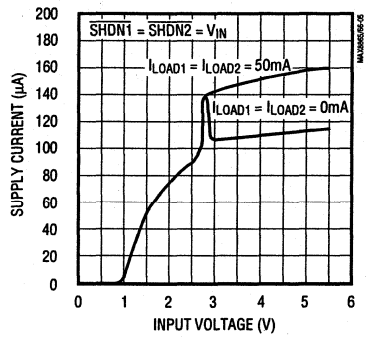
OUTPUT VOLTAGE vs. INPUT VOLTAGE



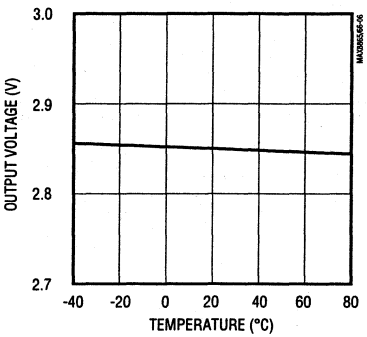
SUPPLY CURRENT vs. INPUT VOLTAGE



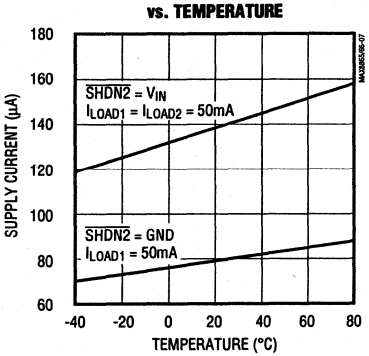
TOTAL SUPPLY CURRENT vs. INPUT VOLTAGE



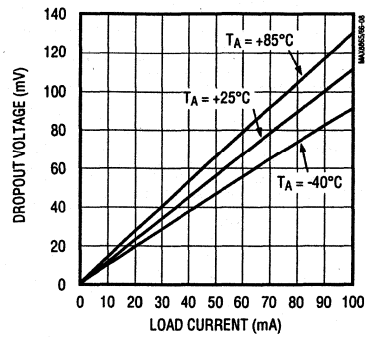
OUTPUT VOLTAGE vs. TEMPERATURE



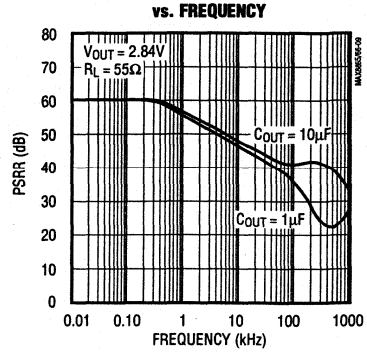
SUPPLY CURRENT vs. TEMPERATURE



DROPOUT VOLTAGE vs. LOAD CURRENT



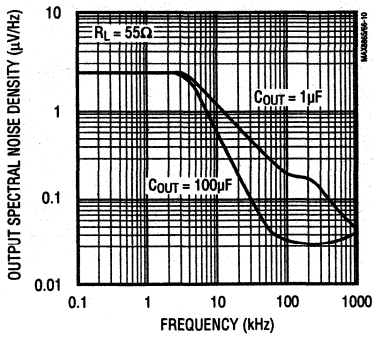
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



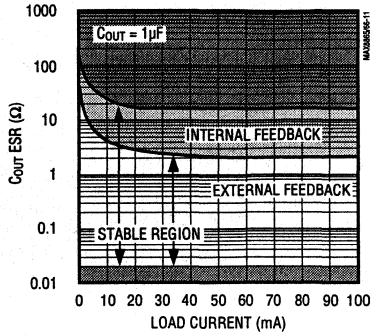
Typical Operating Characteristics (continued)

(V_{IN} = +3.6V, C_{IN} = 2µF, C_{OUT} = 1µF, $\overline{SHDN2}$ = GND, MAX886_S, T_A = +25°C, unless otherwise noted.)

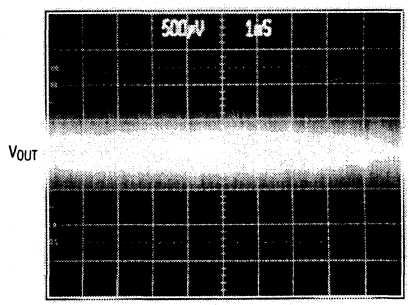
OUTPUT SPECTRAL NOISE DENSITY vs. FREQUENCY



REGION OF STABLE C_{OUT} ESR vs. LOAD CURRENT



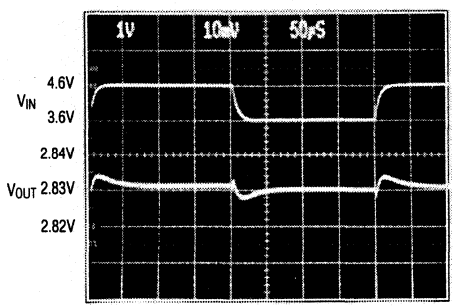
OUTPUT NOISE DC TO 1MHz



1ms/div

I_{LOAD} = 50mA, V_{OUT} IS AC COUPLED

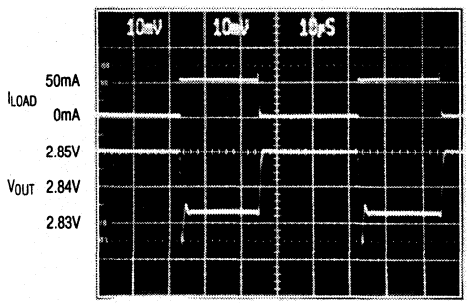
LINE-TRANSIENT RESPONSE



50µs/div

I_{LOAD} = 50mA, V_{OUT} IS AC COUPLED

LOAD-TRANSIENT RESPONSE



10µs/div

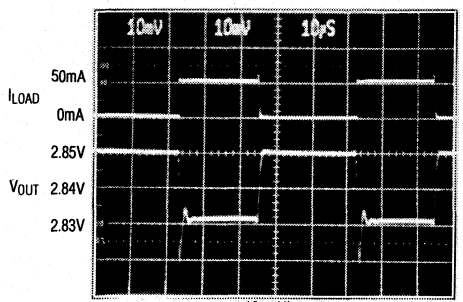
V_{IN} = 3.60V, I_{LOAD} = 0mA to 50mA, C_{IN} = 10µF, V_{OUT} IS AC COUPLED

Dual, Low-Dropout, 100mA Linear Regulators

Typical Operating Characteristics (continued)

(V_{IN} = +3.6V, C_{IN} = 2µF, C_{OUT} = 1µF, $\overline{SHDN2}$ = GND, MAX886_S, T_A = +25°C, unless otherwise noted.)

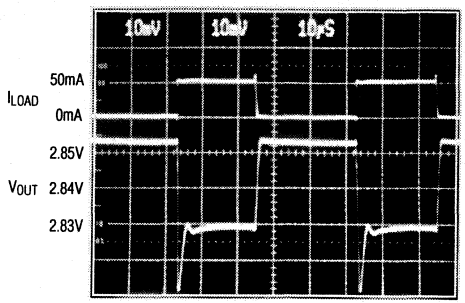
LOAD-TRANSIENT RESPONSE



10µs/div

V_{IN} = V_{OUT} + 0.2V, I_{LOAD} = 0mA to 50mA, C_{IN} = 10µF, V_{OUT} IS AC COUPLED

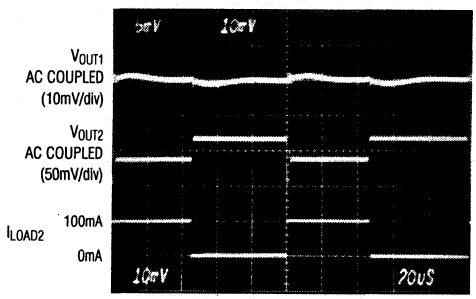
LOAD-TRANSIENT RESPONSE



10µs/div

V_{IN} = V_{OUT} + 0.1V, I_{LOAD} = 0mA to 50mA, C_{IN} = 10µF, V_{OUT} IS AC COUPLED

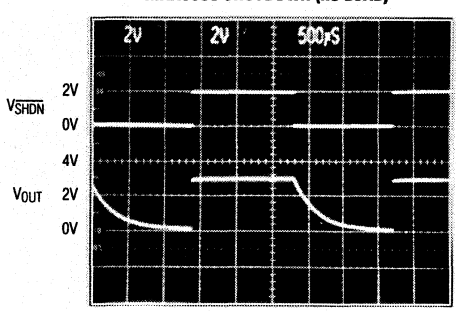
CROSSTALK DUE TO LOAD TRANSIENT



20µs/div

C_{IN} = 10µF, I_{OUT1} = 100mA, $\overline{SHDN2}$ = V_{IN}

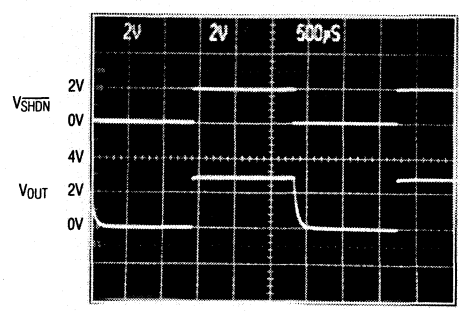
MAX8866 SHUTDOWN (NO LOAD)



500µs/div

NO LOAD

MAX8866 SHUTDOWN (50mA LOAD)



500µs/div

I_{LOAD} = 50mA

Pin Description

PIN	NAME	FUNCTION
1	OUT1	Regulator 1 Output. Fixed or adjustable from 1.25V to 5.5V. Sources up to 100mA. Bypass with a 1µF capacitor to GND.
2	IN	Regulator Input. Supply voltage can range from +2.5V to +5.5V. Bypass with 2µF to GND.
3	GND	Ground. Solder to large pads or the circuit board ground plane to maximize thermal dissipation.
4	OUT2	Regulator 2 Output. Fixed or adjustable from 1.25V to 5.5V. Sources up to 100mA. Bypass with a 1µF capacitor to GND.
5	SET2	Feedback Input for Setting the Output 2 Voltage. Connect to GND to set the output voltage to the preset 2.80V (MAX886_R), 2.84V (MAX886_S), or 3.15V (MAX886_T). Connect to an external resistor divider for adjustable-output operation.
6	$\overline{SHDN2}$	Active-Low Shutdown 2 Input. A logic low turns off regulator 2. On the MAX8866, a logic low also causes the output voltage to discharge to GND. Connect to IN for normal operation.
7	$\overline{SHDN1}$	Active-Low Shutdown 1 Input. A logic low turns off regulator 1. On the MAX8866, a logic low also causes the output voltage to discharge to GND. Connect to IN for normal operation.
8	SET1	Feedback Input for Setting the Output 1 Voltage. Connect to GND to set the output voltage to the preset 2.80V (MAX886_R), 2.84V (MAX886_S), or 3.15V (MAX886_T). Connect to an external resistor divider for adjustable-output operation.

Detailed Description

The MAX8865/MAX8866 are dual, low-dropout, low-quiescent-current linear regulators designed primarily for battery-powered applications. They supply adjustable 1.25V to 5.5V outputs or preselected 2.80V (MAX886_R), 2.84V (MAX886_S), or 3.15V (MAX886_T) outputs for load currents up to 100mA. As illustrated in Figure 1, these devices have a 1.25V reference and two independent linear regulators. Each linear regulator consists of an error amplifier, MOSFET driver, P-channel pass transistor, Dual Mode™ comparator, and internal feedback voltage divider.

The 1.25V bandgap reference is connected to the error amplifiers' inverting inputs. Each error amplifier compares this reference with the selected feedback voltage and amplifies the difference. The MOSFET driver reads the error signal and applies the appropriate drive to the P-channel pass transistor. If the feedback voltage is lower than the reference, the pass-transistor gate is pulled lower, allowing more current to pass and increasing the output voltage. If the feedback voltage is too high, the pass-transistor gate is pulled up, allowing less current to pass to the output.

The output voltage is fed back through either an internal resistor voltage divider connected to the OUT_ pin, or an external resistor network connected to the SET_ pin. The Dual Mode comparator examines the SET_ voltage and selects the feedback path. If SET_ is below 60mV, internal feedback is used and the output voltage is regulated to 2.80V for the MAX886_R, 2.84V for the MAX886_S, or 3.15V for the MAX886_T. Both regulators are preset for the same voltage. The reference and the thermal sensor are shared between the regulators. Duplicate blocks exist for current limiters, reverse battery protection, and shutdown logic.

Internal P-Channel Pass Transistor

The MAX8865/MAX8866 feature 1.1Ω typical P-channel MOSFET pass transistors. This provides several advantages over similar designs using PNP pass transistors, including longer battery life.

The P-channel MOSFET requires no base-drive current, which reduces quiescent current significantly. PNP-based regulators waste considerable amounts of current in dropout when the pass transistor saturates. They also use high base-drive currents under large loads. The MAX8865/MAX8866 do not suffer from these problems, and consume only 145µA of quiescent current, whether in dropout, light load, or heavy load applications (see *Typical Operating Characteristics*).

Output Voltage Selection

The MAX8865/MAX8866 feature Dual Mode operation: they operate in either a preset voltage mode or an adjustable mode.

Dual, Low-Dropout, 100mA Linear Regulators

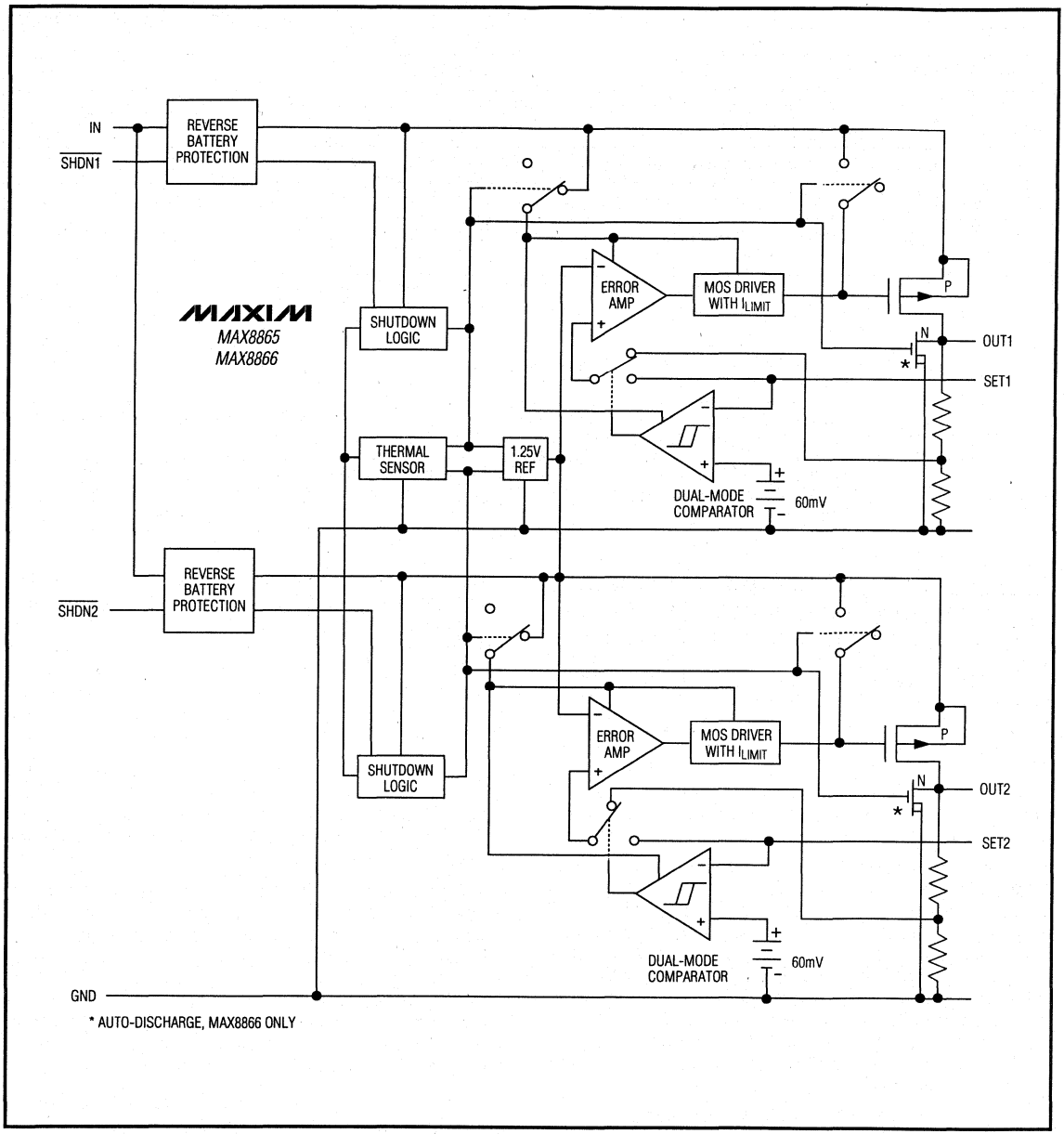


Figure 1. Functional Diagram

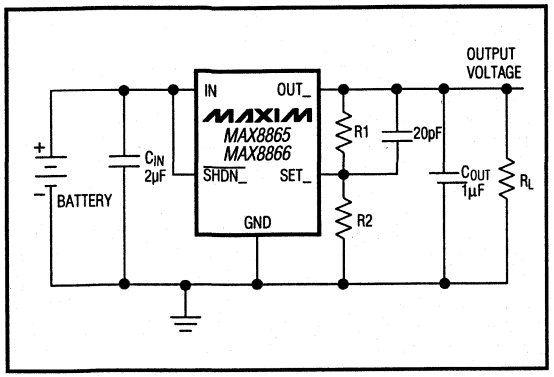


Figure 2. Adjustable Output Using External Feedback Resistors

In preset voltage mode, internal, trimmed feedback resistors set the MAX886_R outputs to 2.80V, the MAX886_S outputs to 2.84V, and the MAX886_T outputs to 3.15V. Select this mode by connecting SET_ to ground. If SET_ can't be grounded in preset voltage mode, limit impedances between SET_ and ground to less than 100kΩ. Otherwise, spurious conditions could cause the voltage at SET_ to exceed the 60mV Dual Mode threshold.

In adjustable mode, select an output between 1.25V and 5.5V using two external resistors connected as a voltage divider to SET_ (Figure 2). The output voltage is set by the following equation:

$$V_{OUT_} = V_{SET_}(1 + R1 / R2)$$

where $V_{SET_}$ = 1.25V. To simplify resistor selection:

$$R1 = R2\left(\frac{V_{OUT_}}{V_{SET_}} - 1\right)$$

Choose R2 = 100kΩ to optimize power consumption, accuracy, and high-frequency power-supply rejection. The total current through the external resistive feedback and load resistors should not be less than 10µA. Since the $V_{SET_}$ tolerance is typically less than ±25mV, the output can be set using fixed resistors instead of trim pots. Connect a 10pF to 25pF capacitor across R1 to compensate for layout-induced parasitic capacitances.

Shutdown

A low input on a $\overline{SHDN_}$ pin individually shuts down one of the two outputs. In shutdown mode, the selected pass transistor, control circuit, and all biases are turned off. When both sections are turned off, the reference and thermal shutdown are also turned off and the supply current is typically reduced to 0.16nA. Connect $\overline{SHDN_}$ to IN for normal operation. The MAX8866 output voltages are actively discharged to ground when individual regulators are shut down (see *Typical Operating Characteristics*).

Current Limit

The MAX8865/MAX8866 include a current limiter for each output section that monitors and controls the pass transistor's gate voltage, estimating the output current and limiting it to about 220mA. For design purposes, the current limit should be considered 120mA (min) to 320mA (max). The outputs can be shorted to ground for an indefinite time period without damaging the part.

Thermal Overload Protection

Thermal overload protection limits total power dissipation in the MAX8865/MAX8866. When the junction temperature exceeds T_J = +170°C, the thermal sensor sends a signal to the shutdown logic, turning off the pass transistors and allowing the IC to cool. The thermal sensor will turn the pass transistors on again after the IC's junction temperature typically cools by 20°C, resulting in a pulsed output during continuous thermal overload conditions.

Thermal overload protection is designed to protect the MAX8865/MAX8866 in the event of fault conditions. Stressing the device with high load currents and high input-output differential voltages (which result in elevated die temperatures above +125°C) may cause a momentary overshoot (2% to 8% for 200ms) when the load is completely removed. This can be remedied by raising the minimum load current from 0µA (+125°C) to 100µA (+150°C). For continuous operation, do not exceed the absolute maximum junction temperature rating of T_J = +150°C.

Operating Region and Power Dissipation

Maximum power dissipation of the MAX8865/MAX8866 depends on the thermal resistance of the case and circuit board, the temperature difference between the die junction and ambient air, and the rate of air flow. The power dissipation across the device is $P = I_{OUT}(V_{IN} - V_{OUT})$. The resulting maximum power dissipation is:

$$P_{MAX} = (T_J - T_A) / \theta_{JA}$$

where $(T_J - T_A)$ is the temperature difference between the MAX8865/MAX8866 die junction and the surrounding air, and θ_{JA} is the thermal resistance of the package to the surrounding air (244°C/W).

Dual, Low-Dropout, 100mA Linear Regulators

Reverse Battery Protection

The MAX8865/MAX8866 have a unique protection scheme that limits the reverse supply current to less than 1mA when either V_{IN} or $V_{\overline{SHDN}}$ falls below ground. The circuitry monitors the polarity of these pins, disconnecting the internal circuitry and parasitic diodes when the battery is reversed. This feature prevents the device from overheating and damaging the battery.

Applications Information

Capacitor Selection and Regulator Stability

Normally, use two 1µF surface-mount ceramic capacitors on the input and a 1µF surface-mount ceramic capacitor on each output of the MAX8865/MAX8866. Larger input capacitor values and lower ESR provide better supply-noise rejection and transient response. A higher-value input capacitor (10µF) may be necessary if large, fast transients are anticipated and the device is located several inches from the power source. Improve load-transient response, stability, and power-supply rejection by using large output capacitors. For stable operation over the full temperature range, with load currents of 100mA, a minimum of 1µF is recommended (see the Region of Stable C_{OUT} ESR vs. Load Current graph in the *Typical Operating Characteristics*).

Noise

The MAX8865/MAX8866 exhibit 350μV_{RMS} noise during normal operation. When using the MAX8865/MAX8866 in applications that include analog-to-digital converters of greater than 12 bits, consider the ADC's power-supply rejection specifications (see the Output Noise DC to 1MHz photo in the *Typical Operating Characteristics*).

Power-Supply Rejection and Operation from Sources Other than Batteries

The MAX8865/MAX8866 are designed to deliver low dropout voltages and low quiescent currents in battery-powered systems. Power-supply rejection is 60dB at low frequencies and rolls off above 400Hz. As the frequency increases above 100kHz, the output capacitor is the major contributor to the rejection of power-supply noise (see the Power-Supply Rejection Ratio vs. Frequency graph in the *Typical Operating Characteristics*.

When operating from sources other than batteries, improve supply-noise rejection and transient response by increasing the values of the input and output capacitors, and using passive filtering techniques (see the supply and load-transient responses in the *Typical Operating Characteristics*).

Load-Transient Considerations

The MAX8865/MAX8866 load-transient response graphs (see *Typical Operating Characteristics*) show two components of the output response: a DC shift of the output voltage due to the different load currents, and the transient response. Typical overshoot for step changes in the load current from 0mA to 50mA is 12mV. Increasing the output capacitor's value and decreasing its ESR attenuates transient spikes.

Cross-Regulation

Cross-regulation refers to the change in one output voltage when the load changes on the other output. For the MAX8865/MAX8866, cross-regulation for a 0mA to 50mA load change on one side results in less than 1mV change of output voltage. If the power dissipation on one output causes the junction temperature to exceed 125°C, ensure regulation of the other output with a minimum load current of 100µA.

Input-Output (Dropout) Voltage

A regulator's minimum input-output voltage differential (or dropout voltage) determines the lowest usable supply voltage. In battery-powered systems, this will determine the useful end-of-life battery voltage. Because the MAX8865/MAX8866 use P-channel MOSFET pass transistors, their dropout voltages are a function of $R_{DS(ON)}$ multiplied by the load currents (see *Electrical Characteristics*).

Chip Information

TRANSISTOR COUNT: 259

MAXIM

µP Supervisory Circuits

µP Supervisory Circuits, Product Tables and Trees 5-2

MAX801L/M/N — 8-Pin µP Supervisory Circuit with ±1.5% Accuracy and Watchdog Timer 5-5

MAX808L/M/N — 8-Pin µP Supervisory Circuit with ±1.5% Reset Accuracy and On-Board Gating of Chip Enable 5-5

MAX817L/M — 5V µP Supervisory Circuit 5-17

MAX818L/M — 5V µP Supervisory Circuit in a µMAX Package 5-17

MAX819L/M — 5V µP Supervisory Circuit with Manual Reset Input 5-17

MAX821L/M/R/S/T — 4-Pin µP Supervisory Circuit with Active-Low Reset 5-33

MAX822L/M/R/S/T — 4-Pin µP Supervisory Circuit with Active-High Reset 5-33

MAX823L/M/R/S/T — 5-Pin µP Supervisory Circuit with Watchdog Input and Manual-Reset Input 5-41

MAX824L/M/R/S/T — 5-Pin µP Supervisory Circuit with Watchdog Input and Active-High Reset 5-41

MAX825L/M/R/S/T — 5-Pin µP Supervisory Circuit with Manual-Reset Input and Active-High Reset 5-41

MAX6301 — 5V, Low-Power µP Supervisory Circuit with Active-Low, Adjustable Reset 5-49

MAX6302 — 5V, Low-Power µP Supervisory Circuit with Active-High, Adjustable Reset 5-49

MAX6303 — 5V, Low-Power µP Supervisory Circuit with Push/Pull Reset Output 5-49

MAX6304 — 5V, Low-Power µP Supervisory Circuit with Active-High, Push/Pull Reset Output 5-49

MAX6305 — 5-Pin, Multiple-Input, Programmable Reset IC 5-61

MAX6306 — 5-Pin, Multiple-Input, Programmable Reset IC 5-61

MAX6307 — 5-Pin, Multiple-Input, Programmable Reset IC 5-61

MAX6308 — 5-Pin, Multiple-Input, Programmable Reset IC 5-61

MAX6309 — 5-Pin, Multiple-Input, Programmable Reset IC 5-61

MAX6310 — 5-Pin, Multiple-Input, Programmable Reset IC 5-61

MAX6311 — 5-Pin, Multiple-Input, Programmable Reset IC 5-61

MAX6312 — 5-Pin, Multiple-Input, Programmable Reset IC 5-61

MAX6313 — 5-Pin, Multiple-Input, Programmable Reset IC 5-61

MAX6314 — 68HC11/Bidirectional-Compatible µP Reset Circuit 5-75

MAX6315 — Open-Drain SOT µP Reset Circuit 5-85

µP Supervisory Circuits

±1% Reset-Threshold Accuracy (Over Temp.)

MAX814K/L/N/T
MAX816
(adj. reset threshold)

With Watchdog

MAX815K/L/N/T

~±1.5% Reset-Threshold Accuracy (Over Temp.)

With Backup-Battery Switchover

★ MAX801L/N/M

With Chip-Enable Gating

★ MAX808L/N/M

With Watchdog

MAX807L/N/M
(with low-line)

> ±2.5% Reset-Threshold Accuracy (Over Temp.)

★ MAX6314
★ MAX6315
MAX707
MAX708
MAX708R/S/T
MAX809L/M/R/S/T
MAX810L/M/R/S/T
MAX811L/M/R/S/T
MAX812L/M/R/S/T
★ MAX821L/M/R/S/T
★ MAX822L/M/R/S/T
★ MAX825L/M/R/S/T

With Backup-Battery Switchover

MAX703
MAX704
MAX704R/S/T
MAX806R/S/T
(±2% power fail)
★ MAX819L/M

With Watchdog

Reset Active High

MAX804R/S/T
(±2% power fail)
MAX805L/R/S/T

Reset Active Low

MAX690A
MAX690R/S/T
MAX692A
MAX802L/M/R/S/T (±2% power fail)
★ MAX817L/M

With Chip-Enable Gating

MAX1691
(module: MAX691A + lithium)
MAX691A
MAX693A
MAX793R/S/T
MAX794 (adj. reset threshold)
MAX818L/M

With Chip-Enable Gating

MAX795R/S/T

With Watchdog

Reset Active High

★ MAX6301-4
MAX706P
MAX813L
★ MAX824L/M/R/S/T

Reset Active Low

MAX705
MAX706
MAX706R/S/T
★ MAX823L/M/R/S/T
★ MAX824L/M/R/S/T

With Chip-Enable Gating

MAX792L/M/R/S/T
MAX820L/M/R/S/T
(±2% power fail)

★ New product

RESET TRIP THRESHOLDS

SUFFIX*	ACCURACY					
	±1%		~±1.5%		>±2.5%	
	Min	Max	Min	Max	Min	Max
K	4.75	4.85	—	—	—	—
L	4.65	4.75	4.60	4.75	4.50	4.75
N	4.50	4.60	4.50	4.65	—	—
M	4.35	4.50	4.35	4.50	4.25	4.50
T	3.00	3.06	—	—	3.00	3.15
S	—	—	—	—	2.85	3.00
R	—	—	—	—	2.55	2.70

* Not all parts have suffix indicator for trip thresholds.
See *µP Supervisory Circuits* table for specific information.

Part Number	Nominal Reset Threshold (V)	Minimum Reset Pulse Width (ms)	Active-Low Reset	Active-High Reset	RESET Valid to V_{CC} = 1V	Nominal Watchdog Timeout Period (sec), if Available	Separate Watchdog Output	Backup-Battery Switch	V_{CC}-to-V_{OUT} On-Resistance Max (Ω)	V_{BATT}-to-V_{OUT} On-Resistance Max (Ω)	$\overline{CE}$ Write Protect	Power-Fail Comparator	Manual Reset Input	Low-Line Output	Battery-On Output	I_{SUPPLY} Operating Mode (µA) max (typ)	I_{SUPPLY} Backup Mode (µA) max (typ)	Pins	Price† 1000-up ($)
MAX1232	4.37/4.62	250	✔	✔	✔	0.15/0.6/ 1.2							✔			200(50)		8	1.71
MAX6301–6304	Adj.	Adj.	✔	✔	✔	Adj.										7(4)		8	1.51
MAX6305–6313	Dual reset with both adj. and preset trip thresholds												✔			16(8)		5	1.20
MAX6314/6315	2.5 to 5.0 preset	1 to 1000	✔	✔	✔								✔			12(5)		4	0.99**
MAX690A/692A	4.65/4.40	140	✔		✔	1.6		✔	10	400		✔				350(200)	5(0.05)	8	3.26
MAX690R/S/T	2.63/2.93/3.08	140	✔		✔	1.6		✔	6	400		✔				500(400)	1(0.4)	8	3.23
MAX691A/693A	4.65/4.40	140/adj.	✔	✔	✔	1.6/adj.	✔	✔	1.2	25	✔/10ns	✔			✔	100(35)	5(0.04)	16	3.61
MAX1691	The MAX1691 is a module with the MAX691A and a 125mAh lithium battery																	16	7.32
MAX696	Adj.	35/adj.	✔	✔		1.6/adj.	✔	✔				✔			✔			16	3.55
MAX697	Adj.	35/adj.	✔	✔		1.6/adj.	✔				✔	✔						16	3.58
MAX700	4.65/adj.	200	✔	✔									✔			200(100)		8	2.17
MAX703/704	4.65/4.40	140	✔		✔			✔	10	400		✔	✔			350(200)	5(0.05)	8	1.38*
MAX704R/S/T	2.63/2.93/3.08	140	✔		✔			✔	6	400		✔	✔			500(400)	1(0.4)	8	2.93
MAX705/706	4.65/4.40	140	✔		✔	1.6	✔					✔	✔			350(200)		8	1.02*
MAX706P	2.63	140		✔	✔	1.6	✔					✔	✔			350(200)		8	1.71
MAX706R/S/T	2.63/2.93/3.08	140	✔		✔	1.6	✔					✔	✔			350(200)		8	1.71
MAX707/708	4.65/4.40	140	✔	✔	✔							✔	✔			350(200)		8	0.88*
MAX708R/S/T	2.63/2.93/3.08	140	✔	✔	✔							✔	✔			350(200)		8	1.63
MAX792L/M/R/S/T	4.65/4.40/ 2.63/2.93/3.08	140	✔	✔	✔	1	✔				✔/10ns	✔	✔	✔		150(70)		16	3.42
MAX793R/S/T	2.63/2.93/3.08	140	✔	✔	✔	1.6	✔	✔	0.4	400	✔	✔	✔	✔		60(46)	1	16	3.48
MAX794	Adj.	140	✔	✔	✔	1.6	✔	✔	0.4	400	✔	✔	✔	✔		60(46)	1	16	3.48
MAX795R/S/T	2.63/2.93/3.08	140	✔		✔			✔	0.4	400	✔			✔		60(46)	1	8	3.41
MAX801L/N/M	4.68/4.58/4.43	140	✔	✔	✔	1.6		✔	1.5	25				✔		110(68)	5(0.4)	8	3.17
MAX802L/M/R/S/T	4.60/4.40/2.63 2.93/3.08	140	✔		✔	1.6		✔	10	400		✔/±2%				0.35(0.2)	5(0.05)	8	3.59
MAX804R/S/T	2.63/2.93/3.08	140		✔	✔	1.6		✔	6	400		✔/±2%				500(400)	1(0.4)	8	3.66
MAX805L/R/S/T	4.65/2.63/2.93/3.08	140		✔	✔	1.6		✔	10	400		✔				350(200)	5(0.05)	8	3.26
MAX806R/S/T	2.63/2.93/3.08	140	✔	✔	✔			✔	6	400		✔/±2%	✔			500(400)	1(0.4)	8	3.90
MAX807L/N/M	4.68/4.58/4.43	140	✔/±1.5%	✔/±1.5%	✔	1.6	✔	✔	1.4	25	✔/8ns	✔	✔	✔	✔	110(70)	5(0.5)	8	3.29
MAX808L/N/M	4.68/4.58/4.43	140	✔		✔			✔	1.5	25	✔/8ns			✔		90(48)	5(0.4)	8	3.17
MAX809L/M/R/S/T	4.65/4.40/ 2.63/2.93/3.08	140	✔		✔											60(24)		3	0.80**
MAX810L/M/R/S/T	4.65/4.40/ 2.63/2.93/3.08	140		✔	✔											60(24)		3	0.80**

† Prices provided are for design guidance and are FOB USA (unless otherwise noted). International prices will differ due to local duties, taxes, and exchange rates.

* 25,000 pc. price, factory direct.

** 2500 pc. price, factory direct. Only factory-direct orders in multiples of 2500 pieces accepted (smaller quantities are available from distributors).

Part Number	Nominal Reset Threshold (V)	Minimum Reset Pulse Width (ms)	Active-Low Reset	Active-High Reset	RESET Valid to V_{CC} = 1V	Nominal Watchdog Timeout Period (sec), if Available	Separate Watchdog Output	Backup-Battery Switch	V_{CC}-to-V_{OUT} On-Resistance Max (Ω)	V_{BATT}-to-V_{OUT} On-Resistance Max (Ω)	CE Write Protect	Power-Fail Comparator	Manual Reset Input	Low-Line Output	Battery-On Output	I_{SUPPLY} Operating Mode (µA) max (typ)	I_{SUPPLY} Backup Mode (µA) max (typ)	Pins	Price† 1000-up ($)
MAX811L/M/R/S/T	4.65/4.40/ 2.63/2.93/3.08	140	✔		✔								✔			15(6) 10(3)		4	0.94**
MAX812L/M/R/S/T	4.65/4.40/ 2.63/2.93/3.08	140		✔	✔								✔			15(6) 10(3)		4	0.94**
MAX813L	4.65	140		✔	✔	1.6	✔					✔/±2%	✔			350(200)		8	1.02*
MAX814K/L/N/T	4.80/4.70/4.55/3.03	140	✔/±1%	✔/±1%	✔							✔/±2%	✔	✔		75		8	4.39
MAX815K/L/N/T	4.80/4.70/4.55/3.03	140	✔/±1%		✔	1.6	✔					✔/±2%	✔			75		8	4.74
MAX816	Adj./±1%	140	✔	✔	✔							✔/±2%	✔			75		8	4.39
MAX817L/M	4.65/4.40	140	✔		✔	1		✔	10	400		✔				45(11)	5(0.05)	8	2.44
MAX818L/M	4.65/4.40	140	✔		✔	1		✔	10	400	✔/8ns					45(11)	5(0.05)	8	2.74
MAX819L/M	4.65/4.40	140	✔		✔			✔	10	400		✔	✔			45(11)	5(0.05)	8	2.07
MAX820L/M/R/S/T	4.65/4.40/2.63 2.93/3.08	140	✔	✔	✔	1	✔				✔/10ns	✔/±2%	✔	✔		0.15(0.07)		16	3.82
MAX821L/M/R/S/T	4.65/4.40/ 2.63/2.93/3.08	0.5 to 100	✔		✔											7(2.5) 5.5(1.8)		4	0.90
MAX822L/M/R/S/T	4.65/4.40/ 2.63/2.93/3.08	0.5 to 100		✔	✔											7(2.5) 5.5(1.8)		4	0.90
MAX823L/M/R/S/T	4.65/4.40/ 2.63/2.93/3.08	140	✔		✔	1.1							✔			24(10) 12(5)		5	1.20
MAX824L/M/R/S/T	4.65/4.40/ 2.63/2.93/3.08	140	✔	✔	✔	1.1										24(10) 12(5)		5	1.20
MAX825L/M/R/S/T	4.65/4.40/ 2.63/2.93/3.08	140	✔	✔	✔								✔			24(10) 12(5)		5	1.15
MXD1210	4.37/4.62							✔	2.5	667	✔					500(230)	0.1(0.002)	8	2.44

RESET TRIP THRESHOLDS

SUFFIX‡	ACCURACY					
	±1%		~±1.5%		>±2.5%	
	Min	Max	Min	Max	Min	Max
K	4.75	4.85	—	—	—	—
L	4.65	4.75	4.60	4.75	4.50	4.75
N	4.50	4.60	4.50	4.65	—	—
M	4.35	4.50	4.35	4.50	4.25	4.50
T	3.00	3.06	—	—	3.00	3.15
S	—	—	—	—	2.85	3.00
R	—	—	—	—	2.55	2.70

RESET TRIP THRESHOLD	RESET			WATCHDOG		
	CODE	TIMEOUT DELAY (sec)		CODE	TIMEOUT DELAY (sec)	
		Min	Max		Min	Max
2.5V to 5.0V in 0.1V Increments	D1	1m	2m	W1	4.3m	9.3m
	D2	20m	40m	W2	7.1m	15.3m
	D3	140m	280m	W3	1.12	2.4
	D4	1.12	2.24	W4	17.9	38.4

† Prices provided are for design guidance and are FOB USA (unless otherwise noted). International prices will differ due to local duties, taxes, and exchange rates.
* 25,000 pc. price, factory direct.

19-1086; Rev 0; 6/96

MAXIM

8-Pin µP Supervisory Circuits with ±1.5% Reset Accuracy

General Description

The MAX801/MAX808 microprocessor (µP) supervisory circuits monitor and control the activities of +5V µPs by providing backup-battery switchover, low-line indication, and µP reset. Additional features include a watchdog for the MAX801 and CMOS RAM write protection for the MAX808.

The MAX801/MAX808 offer a choice of reset-threshold voltage (denoted by suffix letter): 4.675V (L), 4.575V (N), and 4.425V (M). These devices are available in 8-pin DIP and SO packages.

Applications

Computers

Controllers

Intelligent Instruments

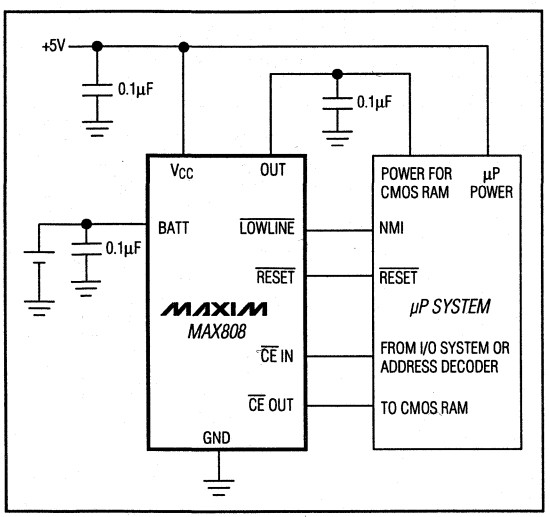
Critical µP Power Monitoring

Portable/Battery-Powered Equipment

Embedded Systems

Pin Configurations appear at end of data sheet.

Typical Operating Circuit



Features

- **Precision Voltage Monitoring, ±1.5% Reset Accuracy**
- **200ms Power-OK/Reset Time Delay**
- **$\overline{\text{RESET}}$ Output (MAX808)**
  RESET and $\overline{\text{RESET}}$ Outputs (MAX801)
- **Watchdog Timer (MAX801)**
- **On-Board Gating of Chip-Enable Signals (MAX808):**
  Memory Write-Cycle Completion
  3ns CE Gate Propagation Delay
- **1µA Standby Current**
- **Power Switching:**
  250mA in VCC Mode
  20mA in Battery-Backup Mode
- **MaxCap™/SuperCap™ Compatible**
- **$\overline{\text{RESET}}$ Guaranteed Valid to VCC = 1V**
- **Low-Line Threshold 52mV Above Reset Threshold**

MaxCap is a trademark of The Carborundum Corp.
SuperCap is a trademark of Baknor Industries.

Ordering Information

PART*	TEMP. RANGE	PIN-PACKAGE
MAX801_CPA	0°C to +70°C	8 Plastic DIP
MAX801_CSA	0°C to +70°C	8 SO
MAX801_EPA	-40°C to +85°C	8 Plastic DIP
MAX801_ESA	-40°C to +85°C	8 SO
MAX801_MJA	-55°C to +125°C	8 CERDIP**
MAX808_CPA	0°C to +70°C	8 Plastic DIP
MAX808_CSA	0°C to +70°C	8 SO
MAX808_EPA	-40°C to +85°C	8 Plastic DIP
MAX808_ESA	-40°C to +85°C	8 SO
MAX808_MJA	-55°C to +125°C	8 CERDIP**

** These parts offer a choice of reset threshold voltage. From the table below, select the suffix corresponding to the desired threshold and insert it into the blank to complete the part number.*
***Contact factory for availability and processing to MIL-STD-883.*

SUFFIX	RESET THRESHOLD (V)		
	MIN	TYP	MAX
L	4.60	4.675	4.75
N	4.50	4.575	4.65
M	4.35	4.425	4.50

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

8-Pin µP Supervisory Circuits with ±1.5% Reset Accuracy

ABSOLUTE MAXIMUM RATINGS

Input Voltage (with respect to GND)
- V_{CC} ..... -0.3V to +6V
- V_{BATT} ..... -0.3V to +6V
- All Other Pins ..... -0.3V to (V_{OUT} + 0.3V)

Input Current
- V_{CC} Peak 1.0A
- V_{CC} Continuous 500mA
- I_{BATT} Peak 250mA
- I_{BATT} Continuous 50mA
- GND 50mA
- All Other Inputs 50mA

Output Current
- OUT Peak 1.0A
- OUT Continuous 500mA
- All Other Outputs 50mA

Continuous Power Dissipation (T_A = +70°C)
- Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
- SO (derate 5.88mW/°C above +70°C) 471mW
- CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges
- MAX801_C_A/MAX808_C_A ..... 0°C to +70°C
- MAX801_E_A/MAX808_E_A ..... -40°C to +85°C
- MAX801_MJA/MAX808_MJA ..... -55°C to +125°C

Storage Temperature Range ..... -65°C to +160°C

Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.6V to 5.5V for the MAX80_L, V_{CC} = 4.5V to 5.5V for the MAX80_N, V_{CC} = 4.35V to 5.5V for the MAX80_M; V_{BATT} = 2.8V; T_A = T_{MIN} to T_{MAX}. Typical values are at V_{CC} = 5V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Operating Voltage Range V_{CC}, BATT (Note 1)					0	X	5.5	V
V_{OUT} in Normal Operating Mode		V_{CC} = 4.5V	I_{OUT} = 25mA			V_{CC} - 0.02		V
			I_{OUT} = 250mA, MAX80_C/E		V_{CC} - 0.38	V_{CC} - 0.25		
			I_{OUT} = 250mA, MAX80_M		V_{CC} - 0.45			
		V_{CC} = 3V, V_{BATT} = 2.8V, I_{OUT} = 100mA			V_{CC} - 0.25	V_{CC} - 0.12		
V_{CC} to OUT On-Resistance		V_{CC} = 4.5V, I_{OUT} = 250mA	MAX80_C/E			1.0	1.5	Ω
			MAX80_M				1.8	
		V_{CC} = 3V, I_{OUT} = 100mA				1.2	2.5	
V_{OUT} in Battery-Backup Mode		V_{CC} = 0V	V_{BATT} = 4.5V, I_{OUT} = 20mA			V_{BATT} - 0.16		V
			V_{BATT} = 2.8V, I_{OUT} = 10mA		V_{BATT} - 0.25	V_{BATT} - 0.12		
			V_{BATT} = 2.0V, I_{OUT} = 5mA		V_{BATT} - 0.20	V_{BATT} - 0.08		
BATT to OUT On-Resistance		V_{CC} = 0V	V_{BATT} = 4.5V, I_{OUT} = 20mA			8		Ω
			V_{BATT} = 2.8V, I_{OUT} = 10mA			12	25	
			V_{BATT} = 2.0V, I_{OUT} = 5mA			16	40	
Supply Current in Normal Operating Mode (excludes I_{OUT})		MAX801				68	110	µA
		MAX808				48	90	
Supply Current in Battery-Backup Mode (excludes I_{OUT}) (Note 2)		V_{CC} = 0V, V_{BATT} = 2.8V	T_A = +25°C			0.4	1	µA
			T_A = T_{MIN} to T_{MAX}	MAX80_C/E			5	
				MAX80_M			50	
BATT Standby Current (Note 3)		V_{BATT} + 0.2V ≤ V_{CC}	T_A = +25°C		-0.1		0.1	µA
			T_A = T_{MIN} to T_{MAX}		-1.0		1.0	
Battery-Switchover Threshold		V_{BATT} = 2.8V	Power-up			V_{BATT} + 0.05		V
			Power-down			V_{BATT}		
Battery-Switchover Hysteresis						50		mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4.6V to 5.5V for the MAX80_L, V_{CC} = 4.5V to 5.5V for the MAX80_N, V_{CC} = 4.35V to 5.5V for the MAX80_M; V_{BATT} = 2.8V; T_A = T_{MIN} to T_{MAX}. Typical values are at V_{CC} = 5V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
RESET AND LOW-LINE							
Reset Threshold	V_{RST}	V_{CC} rising and falling	MAX80_L	4.600	4.675	4.750	V
			MAX80_N	4.500	4.575	4.650	
			MAX80_M	4.350	4.425	4.500	
Reset-Threshold Hysteresis					13		mV
$\overline{LOWLINE}$ to $\overline{RESET}$ Threshold Voltage	V_{LR}	V_{CC} falling		30	52	70	mV
$\overline{LOWLINE}$ Threshold, V_{CC} Rising	V_{LL}	MAX80_L			4.73	4.81	V
		MAX80_N			4.63	4.71	
		MAX80_M			4.48	4.56	
V_{CC} to $\overline{RESET}$ Delay	t_{RD}	V_{CC} falling at 1mV/µs			17		µs
V_{CC} to $\overline{LOWLINE}$ Delay	t_{LL}	V_{CC} falling at 1mV/µs			17		µs
$\overline{RESET}$ Active Timeout Period	t_{RP}	V_{CC} rising		140	200	280	ms
$\overline{RESET}$ Output Voltage		I_{SINK} = 50µA, V_{BATT} = 0V, V_{CC} falling	V_{CC} = 1.0V, MAX80_C			0.3	V
			V_{CC} = 1.2V, MAX80_E/M			0.3	
		I_{SINK} = 3.2mA, V_{CC} = 4.25V			0.1	0.4	
		I_{SOURCE} = 0.1mA		V_{CC} - 1.5	V_{CC} - 0.1		
$\overline{RESET}$ Output Short-Circuit Current	I_{SC}	Output sink current, V_{CC} = 4.25V			40		mA
		Output source current			1.6		
RESET Output Voltage (MAX801)		I_{SINK} = 3.2mA				0.4	V
		I_{SOURCE} = 5mA, V_{CC} = 4.25V		V_{CC} - 1.5			
RESET Output Short-Circuit Current (MAX801)	I_{SC}	Output sink current			55		mA
		Output source current, V_{CC} = 4.25V			15		
$\overline{LOWLINE}$ Output Voltage		I_{SINK} = 3.2mA, V_{CC} = 4.25V				0.4	V
		I_{SOURCE} = 5mA, V_{CC} = 4.25V		V_{CC} - 1.5			
$\overline{LOWLINE}$ Output Short-Circuit Current	I_{SC}	Output sink current, V_{CC} = 4.25V			40		mA
		Output source current			20		
WATCHDOG TIMER (MAX801)							
Watchdog Timeout Period	t_{WD}			1.12	1.6	2.24	sec
Minimum Watchdog Input Pulse Width		V_{IL} = 0.8V, V_{IH} = 0.75V x V_{CC}		100			ns
WDI Threshold Voltage (Note 4)	V_{IH}			0.75 x V_{CC}			V
	V_{IL}					0.8	
WDI Input Current		RESET deasserted, WDI = 0V		-50	-10		µA
		RESET deasserted, WDI = V_{CC}			16	50	

8-Pin µP Supervisory Circuits with ±1.5% Reset Accuracy

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4.6V to 5.5V for the MAX80_L, V_{CC} = 4.5V to 5.5V for the MAX80_N, V_{CC} = 4.35V to 5.5V for the MAX80_M; V_{BATT} = 2.8V; T_A = T_{MIN} to T_{MAX}. Typical values are at V_{CC} = 5V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CHIP-ENABLE GATING (MAX808)						
$\overline{CE}$ IN Leakage Current		V_{CC} = 4.25V		±0.00002	±1	µA
$\overline{CE}$ IN to $\overline{CE}$ OUT Resistance (Note 5)		Enabled mode, V_{CC} = V_{RST}(max)		75	150	Ω
$\overline{CE}$ OUT Short-Circuit Current ($\overline{RESET}$ Active)		V_{CC} = 4.25V, $\overline{CE}$ OUT = 0V		15		mA
$\overline{CE}$ IN to $\overline{CE}$ OUT Propagation Delay (Note 6)		V_{CC} = 5V, C_{LOAD} = 50pF, 50Ω source-impedance driver		3	8	ns
$\overline{CE}$ OUT Output Voltage High ($\overline{RESET}$ Active)		V_{CC} = 4.25V, I_{OUT} = 2mA	3.5			V
		V_{CC} = 0V, I_{OUT} = 10µA	V_{BATT} - 0.1	V_{BATT}		
$\overline{RESET}$ to $\overline{CE}$ OUT Delay (Note 7)		V_{CC} falling, $\overline{CE}$ IN = 0V		18		µs

Note 1: Either V_{CC} or V_{BATT} can go to 0V if the other is greater than 2V.

Note 2: The supply current drawn by the MAX80_ from the battery (excluding I_{OUT}) typically goes to 15µA when (V_{BATT} - 0.1V) < V_{CC} < V_{BATT}. In most applications, this is a brief period as V_{CC} falls through this region (see *Typical Operating Characteristics*).

Note 3: "+" = battery-discharging current, "-" = battery-charging current.

Note 4: WDI is internally connected to a voltage divider between V_{CC} and GND. If unconnected, WDI is typically driven to 1.8V, disabling the watchdog function.

Note 5: The chip-enable resistance is tested with $V_{\overline{CE}\ IN}$ = V_{CC} / 2 and $I_{\overline{CE}\ IN}$ = 1mA.

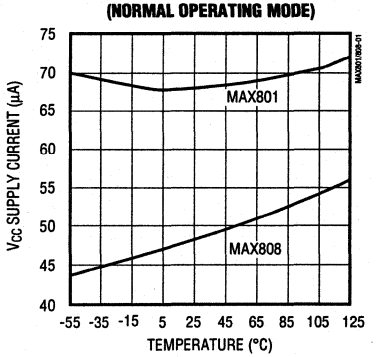
Note 6: The chip-enable propagation delay is measured from the 50% point at $\overline{CE}$ IN to the 50% point at $\overline{CE}$ OUT.

Note 7: If $\overline{CE}$ IN goes high, $\overline{CE}$ OUT goes high immediately and stays high until reset is deasserted and $\overline{CE}$ IN is low.

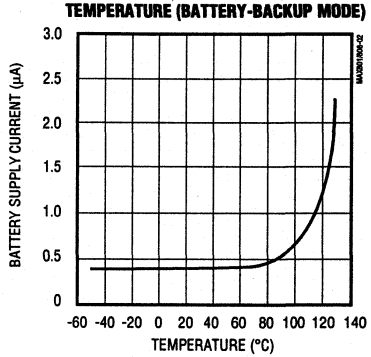
Typical Operating Characteristics

(V_{CC} = 5V, V_{BATT} = 2.8V, no load, T_A = +25°C, unless otherwise noted.)

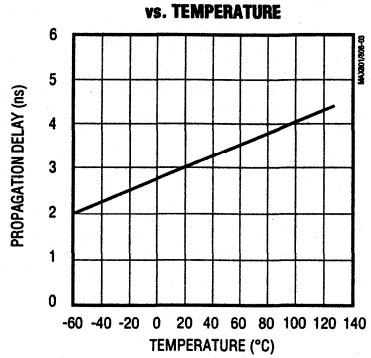
V_{CC} SUPPLY CURRENT vs. TEMPERATURE (NORMAL OPERATING MODE)



BATTERY SUPPLY CURRENT vs. TEMPERATURE (BATTERY-BACKUP MODE)



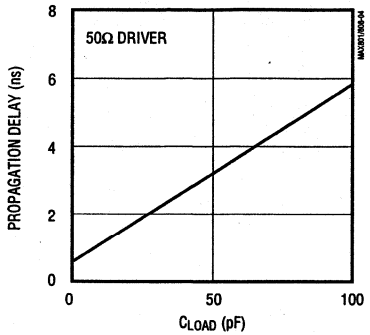
MAX808 CHIP-ENABLE PROPAGATION DELAY vs. TEMPERATURE



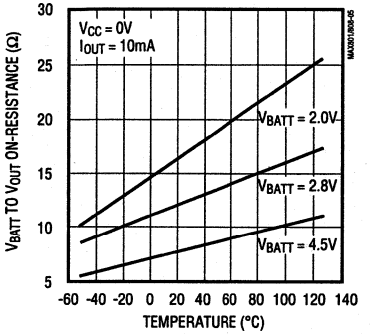
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{BATT} = 2.8V, no load, T_A = +25°C, unless otherwise noted.)

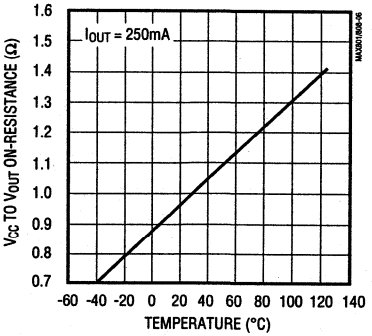
MAX808
CHIP-ENABLE PROPAGATION DELAY vs. $\overline{CE}$ OUT LOAD CAPACITANCE



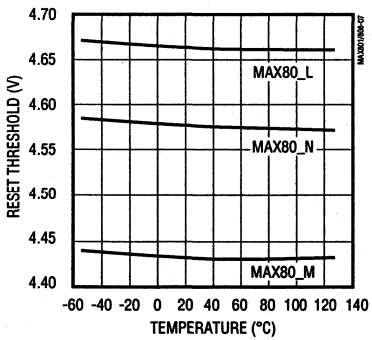
BATT to OUT ON-RESISTANCE vs. TEMPERATURE



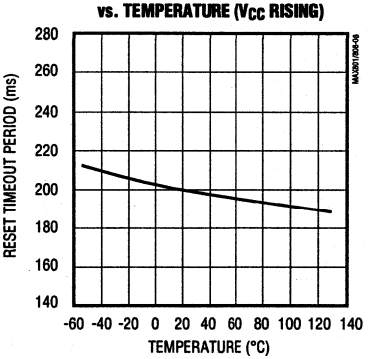
V_{CC} to OUT ON-RESISTANCE vs. TEMPERATURE



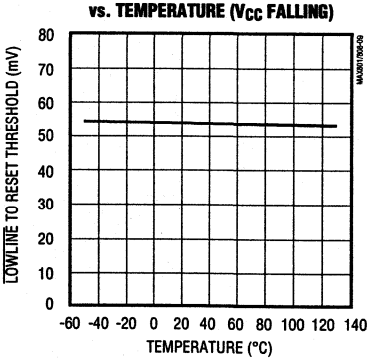
RESET THRESHOLD vs. TEMPERATURE



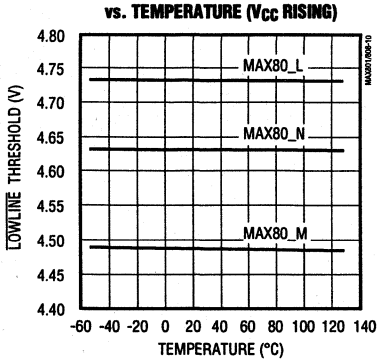
RESET TIMEOUT PERIOD vs. TEMPERATURE (V_{CC} RISING)



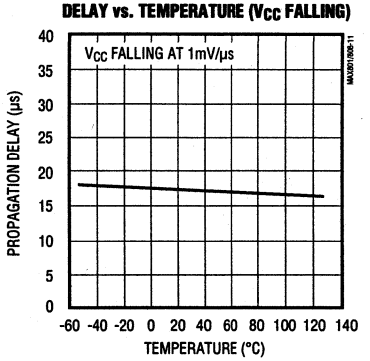
$\overline{LOWLINE}$ to RESET THRESHOLD vs. TEMPERATURE (V_{CC} FALLING)



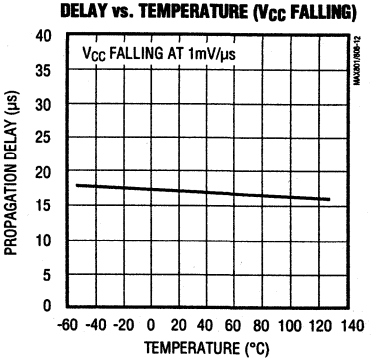
$\overline{LOWLINE}$ THRESHOLD vs. TEMPERATURE (V_{CC} RISING)



$\overline{LOWLINE}$ COMPARATOR PROPAGATION DELAY vs. TEMPERATURE (V_{CC} FALLING)



RESET COMPARATOR PROPAGATION DELAY vs. TEMPERATURE (V_{CC} FALLING)

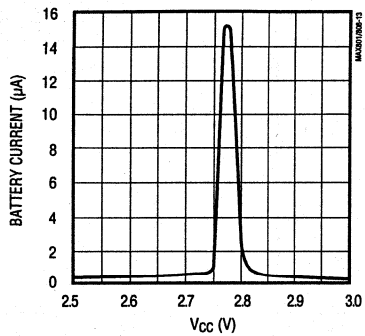


8-Pin µP Supervisory Circuits with ±1.5% Reset Accuracy

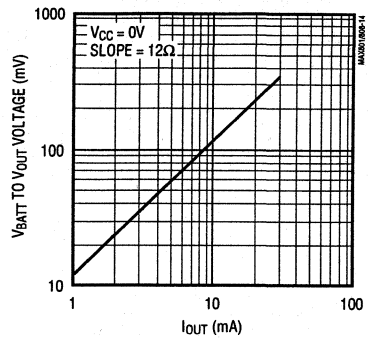
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{BATT} = 2.8V, no load, T_A = +25°C, unless otherwise noted.)

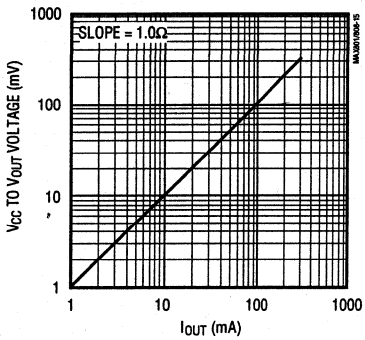
BATTERY CURRENT vs. INPUT SUPPLY VOLTAGE



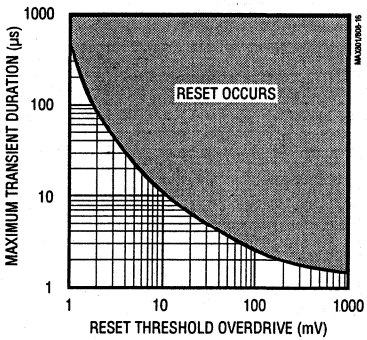
BATT to OUT VOLTAGE vs. OUTPUT CURRENT



VCC to OUT VOLTAGE vs. OUTPUT CURRENT



MAXIMUM TRANSIENT DURATION vs. RESET THRESHOLD OVERDRIVE



Pin Description

PIN		NAME	FUNCTION
MAX801	MAX808		
1	1	V_{CC}	Input Supply Voltage, nominally +5V. Bypass with a 0.1µF capacitor to GND.
2	2	$\overline{LOWLINE}$	Low-Line Comparator Output. This CMOS-logic output goes low when V_{CC} falls to 52mV above the reset threshold. Use $\overline{LOWLINE}$ to generate an NMI, initiating an orderly shutdown routine when V_{CC} is falling. $\overline{LOWLINE}$ swings between V_{CC} and GND.
3	3	$\overline{RESET}$	Active-Low Reset Output. $\overline{RESET}$ is triggered and stays low when V_{CC} is below the reset threshold (or during a watchdog timeout for the MAX801). It remains low 200ms after V_{CC} rises above the reset threshold (or 200ms after the watchdog timeout occurs). $\overline{RESET}$ has a strong pull-down but a relatively weak pull-up, and can be wire-OR connected to logic gates. Valid for $V_{CC} \geq 1V$. $\overline{RESET}$ swings between V_{CC} and GND.
4	4	GND	Ground

Pin Description (continued)

PIN		NAME	FUNCTION
MAX801	MAX808		
5	—	RESET	Active-High Reset Output. RESET is the inverse of $\overline{\text{RESET}}$. It is a CMOS output that sources and sinks current. RESET swings between V_{CC} and GND.
—	5	$\overline{\text{CE}}$ OUT	Chip-Enable Output. Output to the chip-enable gating circuit. $\overline{\text{CE}}$ OUT is pulled up to the higher of V_{CC} or V_{BATT} when the chip-enable gate is disabled.
6	—	WDI	Watchdog Input. If WDI remains high or low longer than the watchdog timeout period (typically 1.6sec), $\overline{\text{RESET}}$ will be asserted for 200ms. Leave unconnected to disable the watchdog function.
—	6	$\overline{\text{CE}}$ IN	Chip-Enable Input
7	7	BATT	Backup-Battery Input. When V_{CC} falls below the reset threshold and V_{BATT}, OUT switches from V_{CC} to BATT. V_{BATT} may exceed V_{CC}. The battery can be removed while the MAX801/MAX808 is powered up, provided BATT is bypassed with a 0.1µF capacitor to GND. If no battery is used, connect BATT to ground and V_{CC} to OUT.
8	8	OUT	Output Supply Voltage to CMOS RAM. When V_{CC} exceeds the reset threshold or V_{BATT}, OUT connects to V_{CC}. When V_{CC} falls below the reset threshold and V_{BATT}, OUT connects to BATT. Bypass OUT with a 0.1µF capacitor to GND.

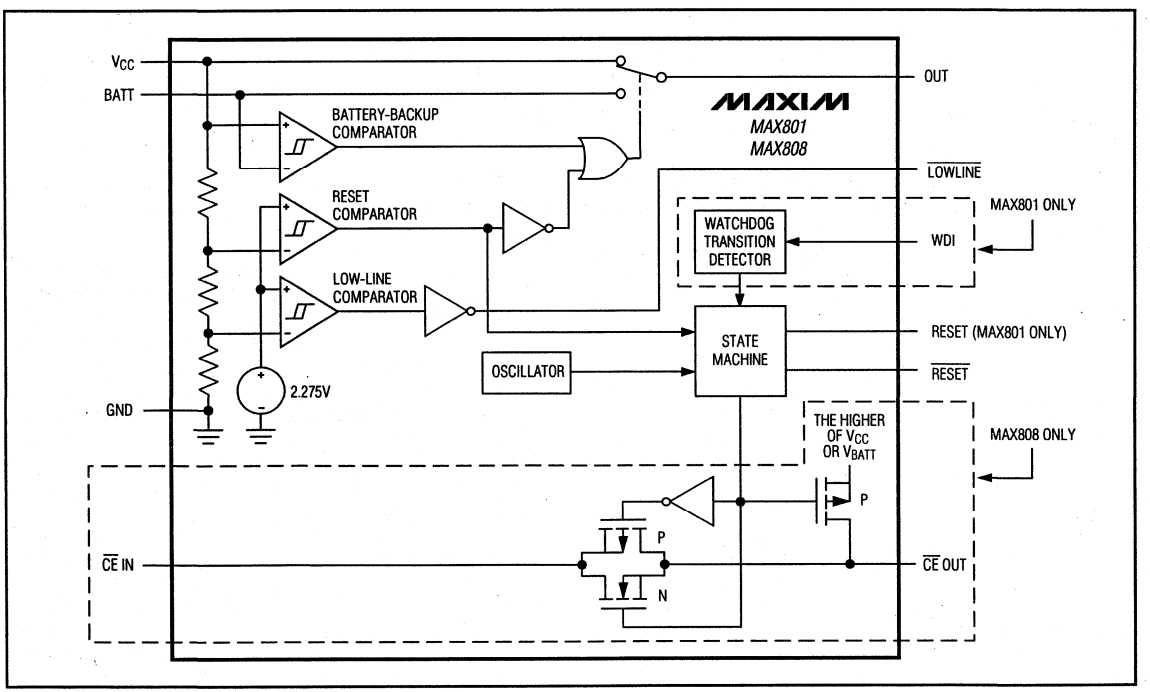


Figure 1. Functional Diagram

8-Pin µP Supervisory Circuits with ±1.5% Reset Accuracy

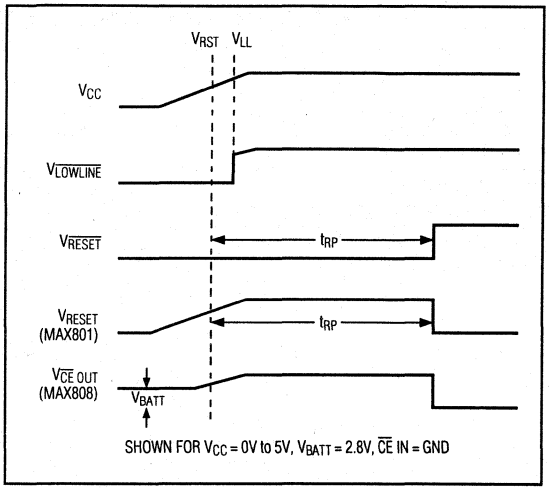


Figure 2a. Timing Diagram, VCC Rising

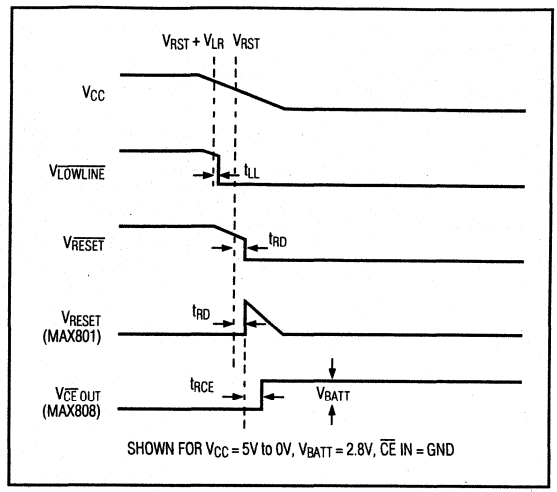


Figure 2b. Timing Diagram, VCC Falling

Detailed Description

The MAX801/MAX808 microprocessor (µP) supervisory circuits provide power-supply monitoring and backup-battery switchover in µP systems. The MAX801 also provides program-execution watchdog functions (Figure 1). Use of BiCMOS technology results in an improved, 1.5% reset-threshold precision while keeping supply currents typically at 68µA (48µA for the MAX808). The MAX801/MAX808 are intended for battery-powered applications that require high reset-threshold precision, allowing a wide power-supply operating range while preventing the system from operating below its specified voltage range.

RESET and RESET Outputs

The MAX801/MAX808's RESET output ensures that the µP powers up in a known state, and prevents code-execution errors during power-down and brownout conditions. It does this by resetting the µP, terminating program execution when VCC dips below the reset threshold. Each time RESET is asserted, it stays low for at least the 200ms reset timeout period (set by an internal timer) to ensure the µP has adequate time to return to an initial state. The internal timer restarts any time VCC goes below the reset threshold (VRST) before the reset timeout period is completed. The watchdog timer on the MAX801 can also initiate a reset (see the *MAX801 Watchdog Timer* section).

The RESET output is active low, and is implemented with a strong pull-down/relatively weak pull-up structure. It is guaranteed to be a logic low for 0V < VCC < VRST, provided VBATT is greater than 2V. Without a backup battery, RESET is guaranteed valid for VCC ≥ 1V.

The RESET output is the inverse of the RESET output; it both sources and sinks current and cannot be wire-OR connected.

Low-Line Comparator

The low-line comparator monitors VCC with a threshold voltage typically 52mV above the reset threshold, with 13mV of hysteresis. Use LOWLINE to provide a non-maskable interrupt (NMI) to the µP when power begins to fall, initiating an orderly software shutdown routine. In most battery-operated portable systems, reserve energy in the battery provides ample time to complete the shutdown routine once the low-line warning is encountered and before reset asserts. If the system must contend with a more rapid VCC fall time (such as when the main battery is disconnected, when a DC-DC converter shuts down, or when a high-side switch is opened during normal operation), use capacitance on the VCC line to provide time to execute the shutdown routine (Figure 3). First calculate the worst-case time required for the system to perform its shutdown routine. Then, with worst-case shutdown time, worst-case load current, and minimum low-line to reset threshold (VLR(min)),

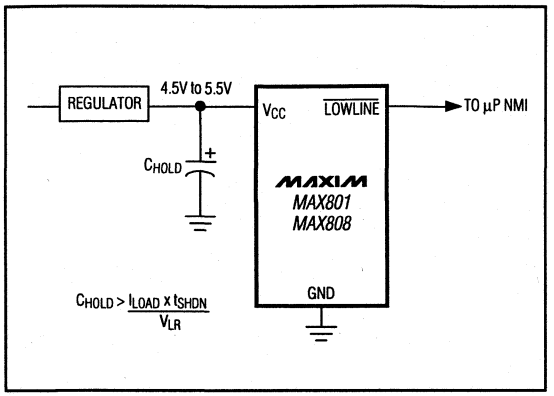


Figure 3. Using LOWLINE to Provide a Power-Fail Warning to the µP

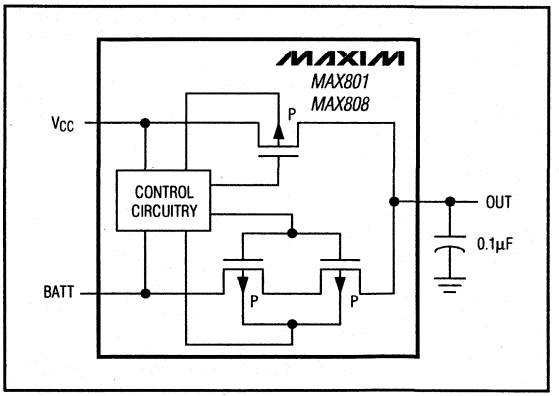


Figure 4. VCC and BATT to OUT Switch

calculate the amount of capacitance required to allow the shutdown routine to complete before reset is asserted:

$$C_{HOLD} = (I_{LOAD} \times t_{SHDN}) / (V_{LR(min)})$$

where t_{SHDN} is the time required for the system to complete the shutdown routine (including the VCC to low-line propagation delay), I_{LOAD} is the current being drained from the capacitor, and V_{LR} is the low-line to reset threshold.

Output Supply Voltage

The output supply (OUT) transfers power from VCC or BATT to the µP, RAM, and other external circuitry. At the maximum source current of 250mA, VOUT will typically be 220mV below VCC. Decouple OUT with a 0.1µF capacitor to ground.

Battery-Backup Mode

Battery-backup mode preserves the contents of RAM in the event of a brownout or power failure. With a backup battery installed at BATT, the MAX801/MAX808 automatically switches RAM to backup power when VCC falls. Two conditions are required for switchover to battery-backup mode: 1) VCC must be below the reset threshold; 2) VCC must be below VBATT. Table 1 lists the status of inputs and outputs during battery-backup mode.

BATT is designed to conduct up to 20mA to OUT during battery backup. The PMOS switch on-resistance is approximately 12Ω. Figure 4 shows the two series pass elements (between the BATT input and OUT) that facilitate UL recognition. VBATT can exceed VCC during normal operation without causing a reset.

Table 1. Input and Output Status in Battery-Backup Mode

PIN		NAME	STATUS
MAX801	MAX808		
1	1	VCC	Battery switchover comparator monitors VCC for active switchover.
2	2	$\overline{\text{LOWLINE}}$	Logic low
3	3	$\overline{\text{RESET}}$	Logic low
4	4	GND	Ground—0V reference for all signals
5	—	RESET	Logic high; the open-circuit voltage is equal to VCC.
—	5	$\overline{\text{CE}}$ OUT	Logic high. The open-circuit output voltage is equal to VBATT (MAX808).
6	—	WDI	WDI is ignored and goes high impedance.
—	6	$\overline{\text{CE}}$ IN	High impedance (MAX808)
7	7	BATT	Supply current is 1µA max for VBATT ≤ 2.8V.
8	8	OUT	OUT is connected to BATT through two internal PMOS switches in series.

8-Pin µP Supervisory Circuits with ±1.5% Reset Accuracy

MAX801 Watchdog Timer

The watchdog monitors the µP's activity. If the µP does not toggle the watchdog input (WDI) within 1.6sec, reset asserts for the reset timeout period. The internal 1.6sec timer is cleared when reset asserts or when a transition (low-to-high or high-to-low) occurs at WDI while reset is not asserted. The timer remains cleared and does not count as long as reset is asserted. It starts counting as soon as reset is released (Figure 5). Supply current is typically reduced by 10µA when WDI is at a valid logic level. To disable the watchdog function, leave WDI unconnected. An internal voltage divider sets WDI to about mid-supply, disabling the watchdog timer/counter.

MAX808 Chip-Enable Gating

The MAX808 provides internal gating of chip-enable (CE) signals to prevent erroneous data from corrupting CMOS RAM in the event of a power failure. During normal operation, the CE gate is enabled and passes all CE transitions. When reset is asserted, this path becomes disabled, preventing erroneous data from corrupting the CMOS RAM. The MAX808 uses a series transmission gate from the chip-enable input ($\overline{CE}$ IN) to the chip-enable output ($\overline{CE}$ OUT) (Figure 1). The 8ns max chip-enable propagation from $\overline{CE}$ IN to $\overline{CE}$ OUT enables the MAX808 to be used with most µPs.

The MAX808 also features write-cycle-completion circuitry. If V_{CC} falls below the reset threshold while the µP is writing to RAM, the MAX808 holds the CE gate enabled for 18µs to allow the µP to complete the write instruction. If the write cycle has not completed by the end of the 18µs period, the CE transmission gate turns off and $\overline{CE}$ OUT goes high. If the µP completes the write instruction during the 18µs period, the CE gate turns off (high impedance) and $\overline{CE}$ OUT goes high as soon as the µP pulls $\overline{CE}$ IN high. $\overline{CE}$ OUT remains high, even if $\overline{CE}$ IN falls low for any reason (Figure 6).

Chip-Enable Input

$\overline{CE}$ IN is high impedance (disabled mode) while reset is asserted. During a power-down sequence when V_{CC} passes the reset threshold, the CE transmission gate disables. $\overline{CE}$ IN becomes high impedance 18µs after reset asserts, provided $\overline{CE}$ IN is still low. If the µP completes the write instruction during the 18µs period, the CE gate turns off. $\overline{CE}$ IN becomes high impedance as soon as the µP pulls $\overline{CE}$ IN high. $\overline{CE}$ IN remains high impedance even if the signal at $\overline{CE}$ IN falls low (Figure 6). During a power-up sequence, $\overline{CE}$ IN remains high impedance (regardless of $\overline{CE}$ IN activity) until reset is deasserted following the reset timeout period.

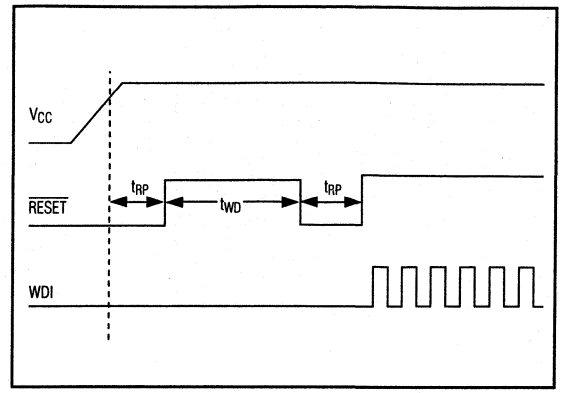


Figure 5. Watchdog Timing

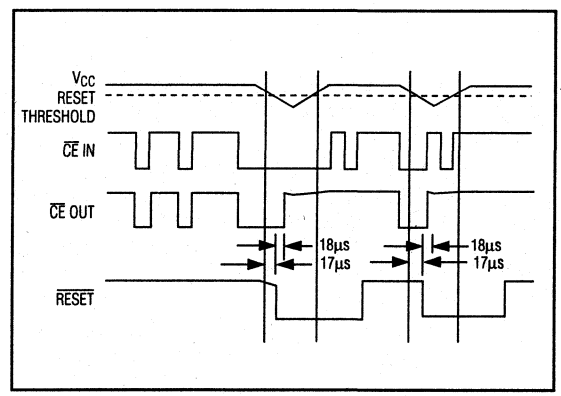


Figure 6. Chip-Enable Timing

In high-impedance mode, the leakage currents into this input are ±1µA max over temperature. In low-impedance mode, the impedance of $\overline{CE}$ IN appears as a 75Ω resistor in series with the load at $\overline{CE}$ OUT.

The propagation delay through the CE transmission gate depends on both the source impedance of the drive to $\overline{CE}$ IN and the capacitive loading on $\overline{CE}$ OUT (see the Chip-Enable Propagation Delay vs. $\overline{CE}$ OUT Load Capacitance graph in the *Typical Operating Characteristics*). The CE propagation delay is production tested from the 50% point on $\overline{CE}$ IN to the 50% point on $\overline{CE}$ OUT using a 50Ω driver and 50pF of load capacitance (Figure 7). For minimum propagation delay, minimize the capacitive load at $\overline{CE}$ OUT and use a low-output-impedance driver.

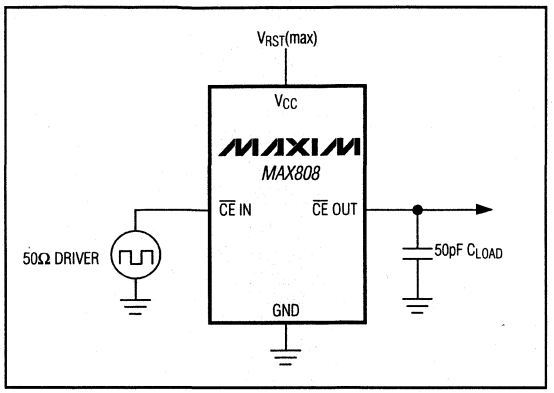


Figure 7. MAX808 CE Gate Test Circuit

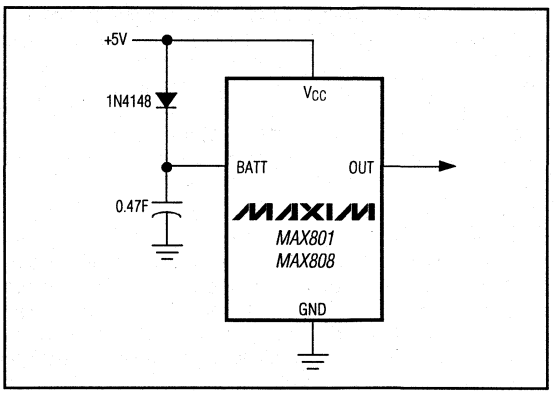


Figure 8. Using the MAX801/MAX808 with a SuperCap

Chip-Enable Output

In enabled mode, $\overline{CE}$ OUT's impedance is equivalent to 75Ω in series with the source driving $\overline{CE}$ IN. In disabled mode, the 75Ω transmission gate is off and $\overline{CE}$ OUT is actively pulled to the higher of V_{CC} or V_{BATT}. The source turns off when the transmission gate is enabled.

Applications Information

The MAX801/MAX808 are not short-circuit protected. Shorting OUT to ground, other than power-up transients such as charging a decoupling capacitor, may destroy the device. If long leads connect to the IC's inputs, ensure that these lines are free from ringing and other conditions that would forward bias the IC's protection diodes. Bypass OUT, V_{CC}, and BATT with 0.1µF capacitors to GND.

The MAX801/MAX808 operate in two distinct modes:

1) Normal Operating Mode, with all circuitry powered up. Typical supply current from V_{CC} is 68µA (48µA for the MAX808), while only leakage currents flow from the battery.
2) Battery-Backup Mode, where V_{CC} is below V_{BATT} and V_{RST}. The supply current from the battery is typically less than 1µA.

Using SuperCaps™ or MaxCaps™ with the MAX801/MAX808

BATT has the same operating voltage range as V_{CC}, and the battery-switchover threshold voltage is typically V_{BATT} when V_{CC} is decreasing or V_{BATT} + 0.05V when V_{CC} is increasing. This hysteresis allows use of a SuperCap (e.g., around 0.47F) and a simple charging circuit as a backup source (Figure 8). Since V_{BATT} can exceed V_{CC} while V_{CC} is above the reset threshold, no special precautions are needed when using these µP supervisors with a SuperCap.

Backup-Battery Replacement

The backup battery can be disconnected while V_{CC} is above the reset threshold, provided BATT is bypassed with a 0.1µF capacitor to ground. No precautions are necessary to avoid spurious reset pulses.

Negative-Going V_{CC} Transients

While issuing resets to the µP during power-up, power-down, and brownout conditions, these supervisors are relatively immune to short-duration, negative-going V_{CC} transients (glitches). It is usually undesirable to reset the µP when V_{CC} experiences only small glitches.

The *Typical Operating Characteristics* show a graph of Maximum Transient Duration vs. Reset Threshold Overdrive, for which reset pulses are not generated. The graph was produced using negative-going V_{CC} pulses, starting at 5V and ending below the reset threshold by the magnitude indicated (reset comparator overdrive). The graph shows the maximum pulse width that a negative-going V_{CC} transient may typically have without causing a reset pulse to be issued. As the amplitude of the transient increases (i.e., goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a V_{CC} transient that goes 40mV below the reset threshold and lasts for 3µs or less will not cause a reset pulse to be issued. A 0.1µF bypass capacitor mounted close to the V_{CC} pin provides additional transient immunity.

8-Pin µP Supervisory Circuits with ±1.5% Reset Accuracy

Watchdog Software Considerations

To help the watchdog timer keep a closer watch on software execution, you can set and reset the watchdog input at different points in the program, rather than "pulsing" the watchdog input high-low-high or low-high-low. This technique avoids a "stuck" loop, where the watchdog timer continues to be reset within the loop, keeping the watchdog from timing out.

Figure 9 shows a sample flow diagram where the I/O driving the watchdog input is set high at the beginning of the program, low at the beginning of every subroutine or loop, then high again when the program returns to the beginning. If the program should "hang" in any subroutine, the I/O would be continually set low and the watchdog timer would be allowed to time out, causing a reset or interrupt to be issued.

Maximum V_{CC} Fall Time

The V_{CC} fall time is limited by the propagation delay of the battery switchover comparator and should not exceed 0.03V/µs. A standard rule for filter capacitance on most regulators is around 100µF per Ampere of current. When the power supply is shut off or the main battery is disconnected, the associated initial V_{CC} fall rate is just the inverse, or 1A/100µF = 0.01V/µs.

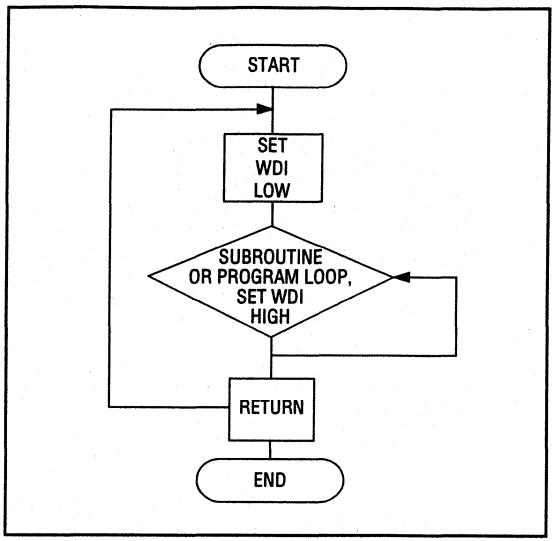
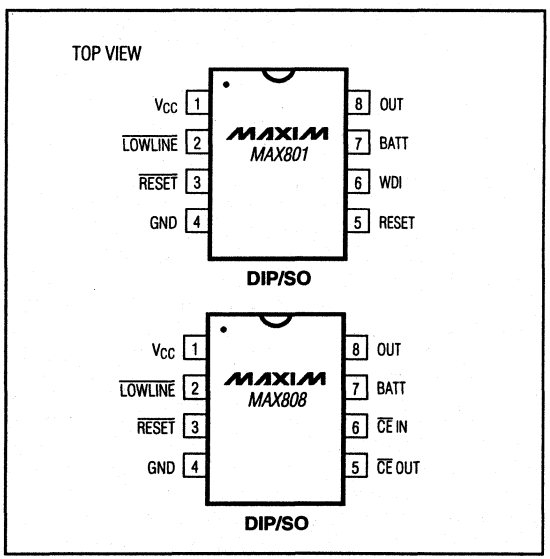


Figure 9. Watchdog Flow Diagram

Pin Configurations



Chip Information

TRANSISTOR COUNT: 922

19-0494; Rev 1; 3/96

MAXIM

+5V Microprocessor Supervisory Circuits

General Description

The MAX817/MAX818/MAX819 microprocessor (µP) supervisory circuits simplify power-supply monitoring, battery control, and chip-enable gating in µP systems by reducing the number of components required. These devices are designed for use in +5V-powered systems. Low supply current (11µA typical) and small package size make these devices ideal for portable applications. The MAX817/MAX818/MAX819 are specifically designed to ignore fast transients on V_{CC}. Other supervisory functions include active-low reset, backup-battery switchover, watchdog input, battery freshness seal, and chip-enable gating. The *Selector Guide* below lists the specific functions available from each device.

These devices offer two pretrimmed reset threshold voltages for ±5% or ±10% power supplies: 4.65V for the L versions and 4.40V for the M versions. The MAX817/MAX818/MAX819 are available in space-saving µMAX packages, as well as 8-pin DIP/SO.

Selector Guide

FEATURE	MAX817 L/M	MAX818 L/M	MAX819 L/M
Active-Low Reset	✔	✔	✔
Backup-Battery Switchover	✔	✔	✔
Power-Fail Comparator	✔	—	✔
Watchdog Input	✔	✔	—
Battery Freshness Seal	✔	✔	✔
Manual Reset Input	—	—	✔
Chip-Enable Gating	—	✔	—
Pin-Package	8-DIP/SO/ µMAX	8-DIP/SO/ µMAX	8-DIP/SO/ µMAX
Low-Power, Pin-Compatible Upgrades for:	MAX690A/ MAX692A	—	MAX703/ MAX704

Applications

Battery-Powered Computers and Controllers
Embedded Controllers
Intelligent Instruments
Critical µP Monitoring
Portable Equipment

Typical Operating Circuit appears at end of data sheet.

**Patents Pending*

Features

- ♦ **Precision Supply-Voltage Monitor:**
  4.65V (MAX81_L)
  4.40V (MAX81_M)
- ♦ **11µA Quiescent Supply Current**
- ♦ **200ms Reset Time Delay**
- ♦ **Watchdog Timer with 1.6sec Timeout (MAX817/MAX818)**
- ♦ **Battery-Backup Power Switching; Battery Voltage Can Exceed V_{CC}**
- ♦ **Battery Freshness Seal**
- ♦ **On-Board, 3ns Gating of Chip-Enable Signals (MAX818)**
- ♦ **Uncommitted Voltage Monitor for Power-Fail or Low-Battery Warning (MAX817/MAX819)**
- ♦ **Manual Reset Input (MAX819)**

Ordering Information

PART†	TEMP. RANGE	PIN-PACKAGE
MAX817_CPA	0°C to +70°C	8 Plastic DIP
MAX817_CSA	0°C to +70°C	8 SO
MAX817_CUA	0°C to +70°C	8 µMAX

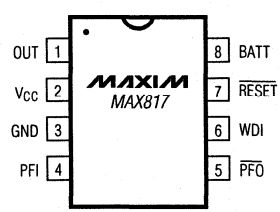
Ordering Information continued on last page.

†These parts offer a choice of reset threshold voltage. From the table below, select the suffix corresponding to the desired threshold and insert it into the blank to complete the part number.

SUFFIX	RESET THRESHOLD (V)
L	4.65
M	4.40

Pin Configurations

TOP VIEW



DIP/SO/µMAX

Pin Configurations continued at end of data sheet.

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

+5V Microprocessor Supervisory Circuits

ABSOLUTE MAXIMUM RATINGS

Input Voltage
- V_{CC}, BATT ..... -0.3V to +6.0V
- All Other Pins (Note 1) ..... -0.3V to (V_{CC} + 0.3V)

Input Current
- V_{CC} Peak 1A
- V_{CC} Continuous 250mA
- BATT Peak 250mA
- BATT Continuous 50mA
- GND 25mA

Output Current
- OUT 250mA
- All Other Outputs 25mA

OUT Short-Circuit Duration 10sec

Continuous Power Dissipation (T_A = +70°C)
- Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
- SO (derate 5.88mW/°C above +70°C) 471mW
- µMAX (derate 4.10mW/°C above +70°C) 330mW

Operating Temperature Ranges
- MAX81_ _C_A ..... 0°C to +70°C
- MAX81_ _E_A ..... -40°C to +85°C

Storage Temperature Range ..... -65°C to +160°C

Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: The input voltage limits on PFI and WDI may be exceeded (up to 12V V_{IN}) if the current into these pins is limited to less than 10mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.75V to +5.5V for MAX81_L, V_{CC} = +4.5V to +5.5V for MAX81_M, V_{BATT} = 2.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range, V_{CC}, V_{BATT} (Note 2)				0		5.5	V
Supply Current (excluding I_{OUT})	I_{SUPPLY}	As applicable; $\overline{CE}$ IN = 0V, WDI and $\overline{MR}$ unconnected	MAX81_ _C		11	45	µA
			MAX81_ _E		11	60	
Supply Current in Battery-Backup Mode (excluding I_{OUT})		V_{CC} = 0V	T_A = +25°C		0.05	1.0	µA
			T_A = T_{MIN} to T_{MAX}			5.0	
BATT Standby Current (Note 3)		5.5V > V_{CC} > (V_{BATT} + 0.2V)	T_A = +25°C	-0.10		0.02	µA
			T_A = T_{MIN} to T_{MAX}	-1.00		0.02	
BATT Leakage Current, Freshness Seal Enabled		V_{CC} = 0V, V_{OUT} = 0V				1	µA
V_{OUT} Output		I_{OUT} = 5mA		V_{CC} - 0.05	V_{CC} - 0.025		V
		I_{OUT} = 50mA		V_{CC} - 0.5	V_{CC} - 0.25		
V_{CC} to OUT On-Resistance					5	10	Ω
BATT to OUT On-Resistance					100		Ω
V_{OUT} in Battery-Backup Mode		I_{OUT} = 250µA, V_{CC} < (V_{BATT} - 0.2V)		V_{BATT} - 0.1	V_{BATT} - 0.02		V
Battery Switch Threshold (V_{CC} - V_{BATT})		V_{CC} < V_{RST}	Power-up		20		mV
			Power-down		-20		
Battery Switchover Hysteresis					40		mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +4.75V to +5.5V for MAX81_L, V_{CC} = +4.5V to +5.5V for MAX81_M, V_{BATT} = 2.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RESET AND WATCHDOG TIMER						
Reset Threshold	V_{RST}	MAX81_L	4.50	4.65	4.75	V
		MAX81_M	4.25	4.40	4.50	
Reset Threshold Hysteresis				25		mV
Reset Timeout Period	t_{RP}		140	200	280	ms
$\overline{RESET}$ Output Voltage	V_{OH}	V_{CC} > $V_{RST(MAX)}$, I_{SOURCE} = 800µA	V_{CC} - 1.5			V
	V_{OL}	V_{CC} < $V_{RST(MIN)}$, I_{SINK} = 3.2mA			0.4	
		MAX81_ _C, V_{CC} = 1V, V_{CC} falling, V_{BATT} = 0V, I_{SINK} = 50µA			0.3	
		MAX81_ _E, V_{CC} = 1.2V, V_{CC} falling, V_{BATT} = 0V, I_{SINK} = 100µA			0.3	
V_{CC} to $\overline{RESET}$ Delay		From V_{RST}, V_{CC} falling at 10V/ms		100		µs
Watchdog Timeout Period	t_{WD}		1.00	1.60	2.25	sec
WDI Pulse Width	t_{WDI}	V_{IL} = 0.4V, V_{IH} = 0.8V_{CC}	50			ns
WDI Input Threshold (Note 4)	V_{IL}	V_{CC} = 5V			0.8	V
	V_{IH}		3.5			
WDI Input Current (Note 5)		WDI = V_{CC}, time average		120	160	µA
		WDI = GND, time average	-20	-15		
POWER-FAIL COMPARATOR (MAX817/MAX819 only)						
PFI Input Threshold	V_{PFT}		1.20	1.25	1.30	V
PFI Input Hysteresis				4		mV
PFI Input Current	I_{PFI}		-25	0.01	25	nA
$\overline{PFO}$ Output Voltage	V_{OL}	V_{PFI} < 1.20V, I_{SINK} = 3.2mA, V_{CC} > 4.50V			0.4	V
	V_{OH}	V_{PFI} > 1.30V, I_{SOURCE} = 40µA, V_{CC} > 4.5V	V_{CC} - 1.5			
$\overline{PFO}$ Short-Circuit Current		$V_{\overline{PFO}}$ = 0V		250	500	µA
MANUAL RESET INPUT (MAX819 only)						
$\overline{MR}$ Input Threshold	V_{IL}		0.8			V
	V_{IH}				2.0	
$\overline{MR}$ Pulse Width			1			µs
$\overline{MR}$ Pulse that Would Not Cause a Reset				100		ns
$\overline{MR}$ to Reset Delay				120		ns
$\overline{MR}$ Pull-Up Resistance			45	63	85	kΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +4.75V to +5.5V for MAX81_L, V_{CC} = +4.5V to +5.5V for MAX81_M, V_{BATT} = 2.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CHIP-ENABLE GATING (MAX818 only)						
$\overline{CE}$ IN Leakage Current		Disable mode		±0.005	±1	µA
$\overline{CE}$ IN to $\overline{CE}$ OUT Resistance (Note 6)		Enable mode		40	150	Ω
$\overline{CE}$ OUT Short-Circuit Current (Reset Active)		Disable mode, $\overline{CE}$ OUT = 0V	0.1	0.75	2.0	mA
$\overline{CE}$ IN to $\overline{CE}$ OUT Propagation Delay (Note 7)		50Ω source impedance driver, C_{LOAD} = 50pF		3	8	ns
$\overline{CE}$ OUT Output	V_{OH}	I_{OUT} = -100µA, V_{CC} = 0V	V_{CC} - 1V			V
		I_{OUT} = -1µA, V_{CC} = 0V, V_{BATT} = 2.8V	2.7			
$\overline{CE}$ OUT Input Threshold	V_{IH}	V_{CC} = 5V			0.8	V
	V_{IL}		3.5			
$\overline{RESET}$ to $\overline{CE}$ OUT Delay		Power-down		15		µs

Note 2: Either V_{CC} or V_{BATT} can go to 0V if the other is greater than 2.0V.

Note 3: "-" = battery-charging current, "+" = battery-discharging current.

Note 4: WDI is internally serviced within the watchdog timeout period if WDI is left unconnected.

Note 5: WDI input is designed to be driven by a three-stated output device. To float WDI, the "high-impedance mode" of the output device must have a maximum leakage current of 10µA and a maximum output capacitance of 200pF. The output device must also be able to source and sink at least 200µA when active.

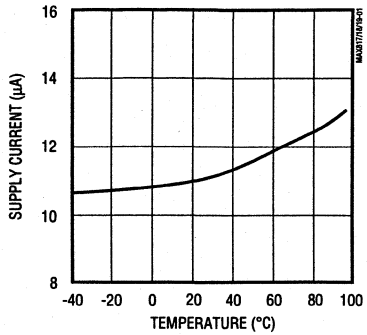
Note 6: The chip-enable resistance is tested with V_{CC} = +4.75V for the MAX818L and V_{CC} = +4.5V for the MAX818M. $V_{\overline{CE}\ IN}$ = $V_{\overline{CE}\ OUT}$ = V_{CC}/2.

Note 7: The chip-enable propagation delay is measured from the 50% point at $\overline{CE}$ IN to the 50% point at $\overline{CE}$ OUT.

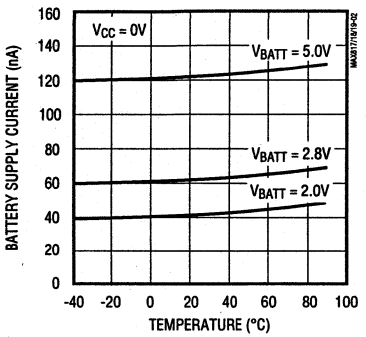
Typical Operating Characteristics

(V_{CC} = +5V, V_{BATT} = 3.0V, T_A = +25°C, unless otherwise noted.)

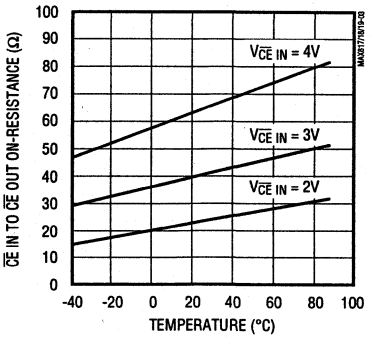
SUPPLY CURRENT vs. TEMPERATURE (NO LOAD)



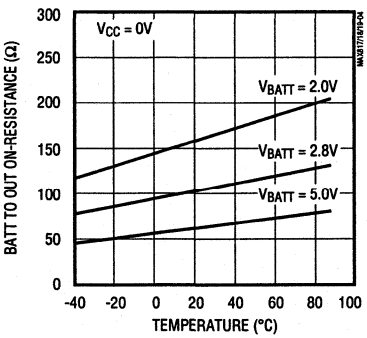
BATTERY SUPPLY CURRENT (BACKUP MODE) vs. TEMPERATURE



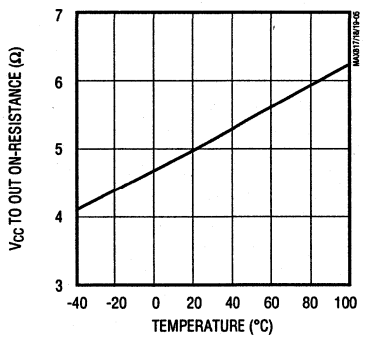
$\overline{CE}$ IN TO $\overline{CE}$ OUT ON-RESISTANCE vs. TEMPERATURE



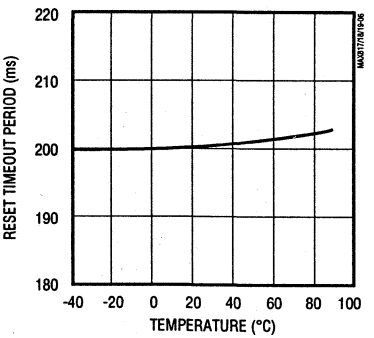
BATT TO OUT ON-RESISTANCE vs. TEMPERATURE



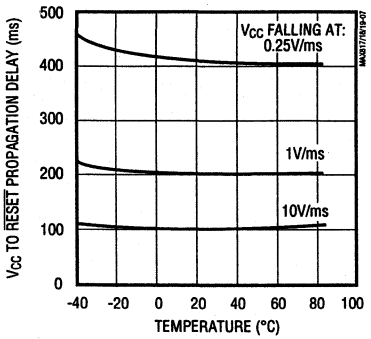
V_{CC} TO OUT ON-RESISTANCE vs. TEMPERATURE



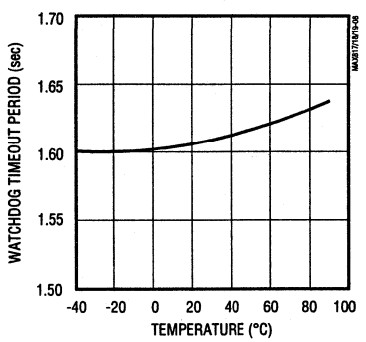
RESET TIMEOUT PERIOD vs. TEMPERATURE



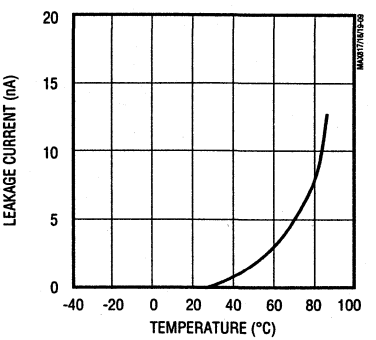
V_{CC} TO $\overline{RESET}$ PROPAGATION DELAY vs. TEMPERATURE



WATCHDOG TIMEOUT PERIOD vs. TEMPERATURE



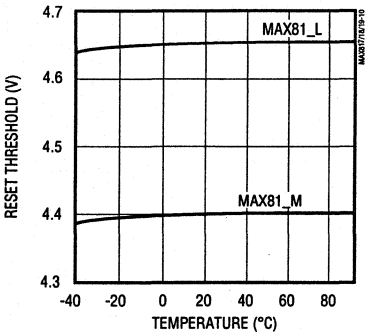
BATTERY FRESHNESS SEAL LEAKAGE CURRENT vs. TEMPERATURE



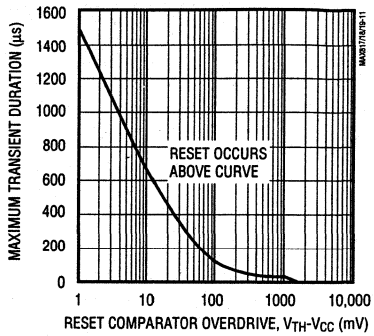
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{BATT} = 3.0V, T_A = +25°C, unless otherwise noted.)

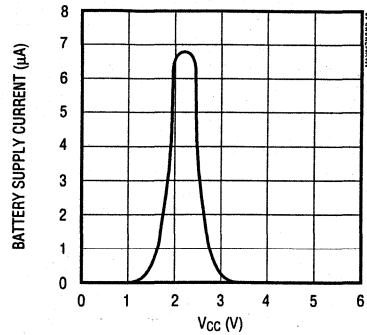
RESET THRESHOLD vs. TEMPERATURE



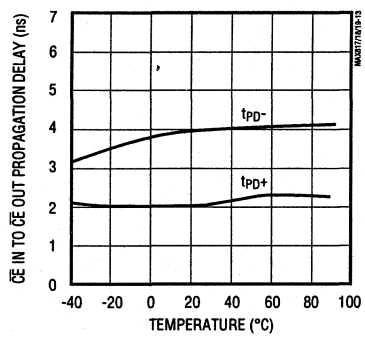
MAXIMUM TRANSIENT DURATION vs. RESET THRESHOLD OVERDRIVE



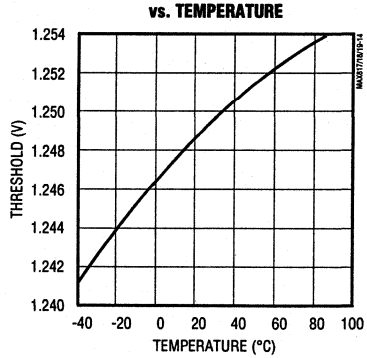
BATTERY SUPPLY CURRENT vs. SUPPLY VOLTAGE



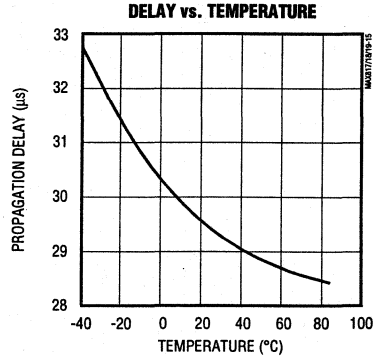
$\overline{CE}$ IN TO $\overline{CE}$ OUT PROPAGATION DELAY vs. TEMPERATURE



MAX817/MAX819 PFI THRESHOLD vs. TEMPERATURE



MAX817/MAX819 PFI TO $\overline{PFO}$ PROPAGATION DELAY vs. TEMPERATURE



Pin Description

PIN			NAME	FUNCTION
MAX817	MAX818	MAX819		
1	1	1	OUT	Supply Output for CMOS RAM. When V_{CC} rises above the reset threshold or above V_{BATT}, OUT is connected to V_{CC} through an internal P-channel MOSFET switch. When V_{CC} falls below V_{BATT}, BATT connects to OUT.
2	2	2	V_{CC}	Input Supply Voltage, +5V input.
3	3	3	GND	Ground. 0V reference for all signals.
4	—	4	PFI	Power-Fail Comparator Input. When V_{PFI} is below V_{PFT} or when V_{CC} is below V_{BATT}, $\overline{PFO}$ goes low; otherwise, $\overline{PFO}$ remains high (see *Power-Fail Comparator* section). Connect to ground if unused.
—	4	—	$\overline{CE}$ IN	Chip-Enable Input. The input to the chip-enable gating circuit. Connect to ground if unused.
5	—	5	$\overline{PFO}$	Power-Fail Comparator Output. When PFI is less than V_{PFT} or when V_{CC} is below V_{BATT}, $\overline{PFO}$ goes low; otherwise $\overline{PFO}$ remains high. $\overline{PFO}$ is also used to enable the battery freshness seal (see *Battery Freshness Seal* and *Power-Fail Comparator* sections).
—	5	—	$\overline{CE}$ OUT	Chip-Enable Output. $\overline{CE}$ OUT goes low only if $\overline{CE}$ IN is low while reset is not asserted. If $\overline{CE}$ IN is low when reset is asserted, $\overline{CE}$ OUT will remain low for 15µs or until $\overline{CE}$ IN goes high, whichever occurs first. $\overline{CE}$ OUT is pulled up to OUT in battery-backup mode. $\overline{CE}$ OUT is also used to enable the battery freshness seal (see *Battery Freshness Seal* section).
6	6	—	WDI	Watchdog Input. If WDI remains either high or low for longer than the watchdog timeout period, the internal watchdog timer runs out and a reset is triggered. If WDI is left unconnected or is connected to a high-impedance three-state buffer, the watchdog feature is disabled. The internal watchdog timer clears whenever reset is asserted, WDI is three-stated, or WDI sees a rising or falling edge. The WDI input is designed to be driven by a three-stated-output device with a maximum high-impedance leakage current of 10µA and a maximum output capacitance of 200pF. The output device must also be capable of sinking and sourcing 200µA when active.
—	—	6	$\overline{MR}$	Manual Reset Input. A logic low on $\overline{MR}$ asserts reset. Reset remains asserted for as long as $\overline{MR}$ is held low and for 200ms after $\overline{MR}$ returns high. The active-low input has an internal 63kΩ pull-up resistor. It can be driven from a TTL- or CMOS-logic line or shorted to ground with a switch. Leave open, or connect to V_{CC} if unused.
7	7	7	$\overline{RESET}$	Active-Low Reset Output. Pulses low for 200ms when triggered and remains low whenever V_{CC} is below the reset threshold or when $\overline{MR}$ is a logic low. It remains low for 200ms after V_{CC} rises above the reset threshold, the watchdog triggers a reset, or $\overline{MR}$ goes low to high.
8	8	8	BATT	Backup-Battery Input. When V_{CC} falls below V_{BATT}, OUT switches from V_{CC} to BATT. When V_{CC} rises above V_{BATT}, OUT reconnects to V_{CC}.

+5V Microprocessor Supervisory Circuits

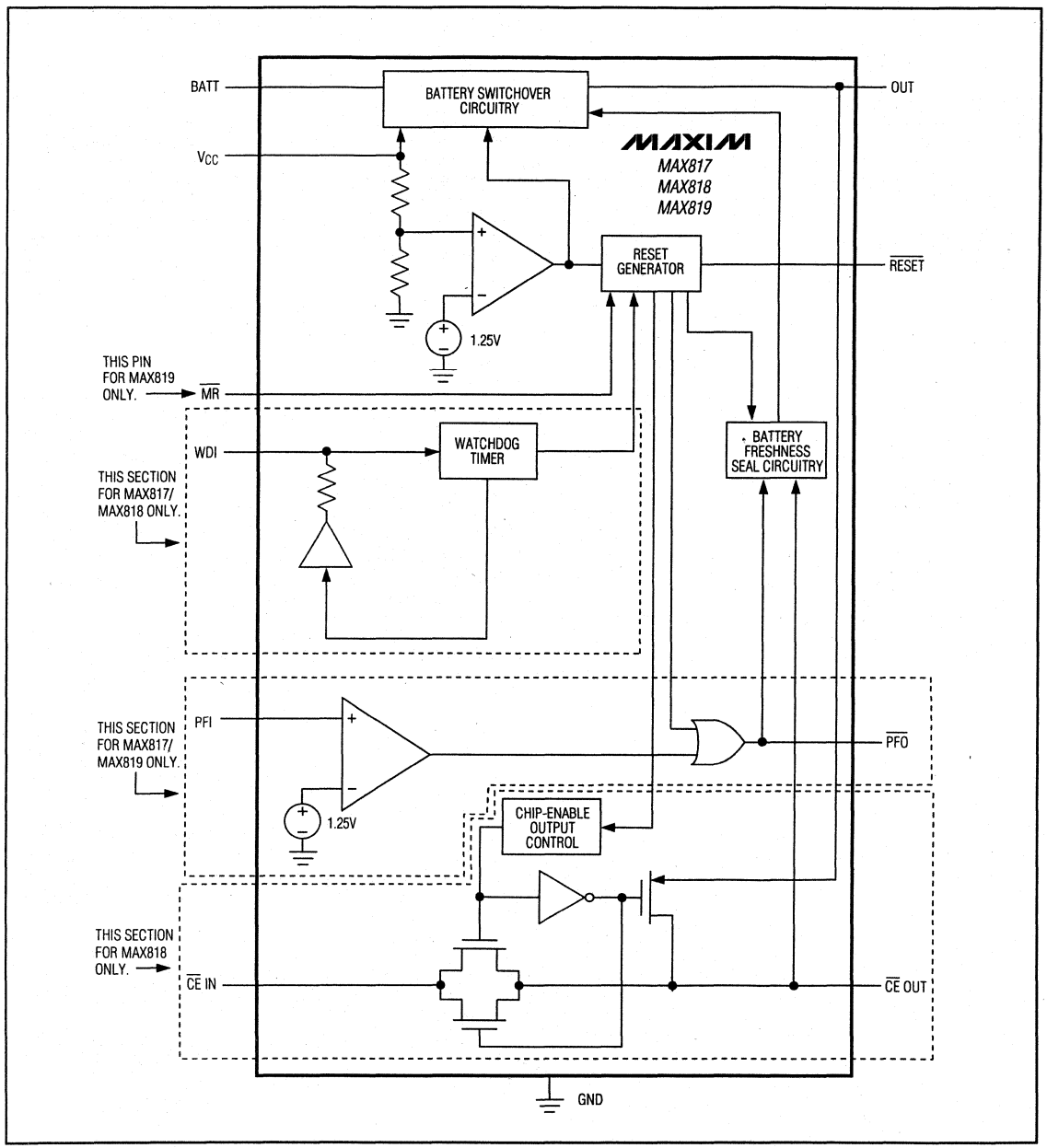


Figure 1. Functional Diagram

Detailed Description

General Timing Characteristics

Designed for 5V systems, the MAX817/MAX818/MAX819 provide a number of microprocessor (µP) supervisory functions (see the *Selector Guide* on the first page). Figure 2 shows the typical timing relationships of the various outputs during power-up and power-down with typical V_{CC} rise and fall times.

RESET Output

A µP's reset input starts the µP in a known state. The MAX817/MAX818/MAX819 µP supervisory circuits assert a reset to prevent code-execution errors during power-up, power-down, and brownout conditions. $\overline{RESET}$ is guaranteed to be a logic low for $0V < V_{CC} < V_{RST}$ if V_{BATT} is greater than 1V. Without a backup battery (V_{BATT} = GND) $\overline{RESET}$ is guaranteed valid for $V_{CC} \geq 1V$. Once V_{CC} exceeds the reset threshold an internal timer keeps $\overline{RESET}$ low for the reset timeout period, t_{RP}. After this interval $\overline{RESET}$ returns high (Figure 2).

If a brownout condition occurs (V_{CC} drops below the reset threshold), $\overline{RESET}$ goes low. Each time $\overline{RESET}$ is asserted it stays low for at least the reset timeout period. Any time V_{CC} goes below the reset threshold the internal timer clears. The reset timer starts when V_{CC} returns above the reset threshold. $\overline{RESET}$ both sources and sinks current.

Manual Reset Input (MAX819)

Many µP-based products require manual reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. On the MAX819, a logic low on $\overline{MR}$ asserts reset. Reset remains asserted while $\overline{MR}$ is low, and for t_{RP} (200ms) after it returns high.

During the reset timeout period (t_{RP}), $\overline{MR}$'s state is ignored if the battery freshness seal is enabled. $\overline{MR}$ has an internal 63kΩ pull-up resistor, so it can be left open if not used. This input can be driven with TTL/CMOS-logic levels or with open-drain/collector outputs. Connect a normally open momentary switch from $\overline{MR}$ to GND to create a manual reset function; external debounce circuitry is not required. If $\overline{MR}$ is driven from long cables or the device is used in a noisy environment, connect a 0.1µF capacitor from $\overline{MR}$ to GND to provide additional noise immunity.

Note that $\overline{MR}$ must be high or open to enable the battery freshness seal. Once the battery freshness seal is enabled its operation is unaffected by $\overline{MR}$.

Battery Freshness Seal

The MAX817/MAX818/MAX819 battery freshness seal disconnects the backup battery from internal circuitry and OUT until it is needed. This allows an OEM to ensure that the backup battery connected to BATT will be fresh when the final product is put to use. To enable the freshness seal on the MAX817 and MAX819:

1) Connect a battery to BATT.
2) Ground $\overline{PFO}$.
3) Bring V_{CC} above the reset threshold and hold it there until reset is deasserted following the reset timeout period.
4) Bring V_{CC} down again (Figure 3).

Use the same procedure for the MAX818, but ground $\overline{CE}$ OUT instead of $\overline{PFO}$. Once the battery freshness seal is enabled (disconnecting the backup battery from internal circuitry and anything connected to OUT), it remains enabled until V_{CC} is brought above V_{RST}.

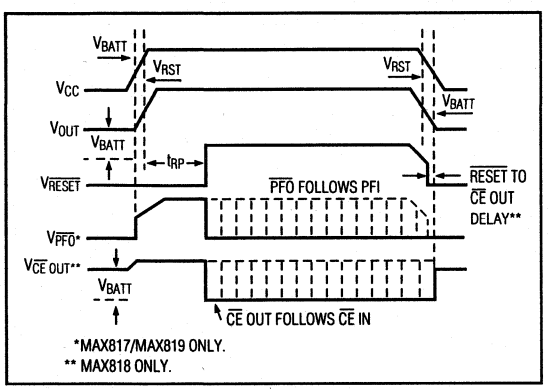


Figure 2. Power-Up and Power-Down Timing

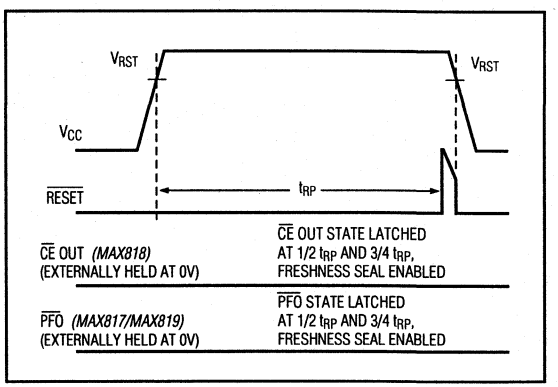


Figure 3. Battery Freshness Seal Timing

On the MAX819, $\overline{MR}$ must be high or open to enable the battery freshness seal. Once the battery freshness seal is enabled its operation is unaffected by $\overline{MR}$.

Watchdog Input (MAX817/MAX818)

In the MAX817/MAX818, the watchdog circuit monitors the µP's activity. If the µP does not toggle the watchdog input (WDI) within t_{WD} (1.6sec), reset asserts. The internal 1.6sec timer is cleared by either a reset pulse or by toggling WDI, which can detect pulses as short as 50ns. The timer remains cleared and does not count for as long as reset is asserted. As soon as reset is released, the timer starts counting (Figure 4).

To disable the watchdog function, leave WDI unconnected or three-state the driver connected to WDI. The watchdog input is internally driven low during the first 7/8 of the watchdog timeout period, then momentarily pulses high, resetting the watchdog counter. When WDI is left open-circuited, this internal driver clears the 1.6sec timer every 1.4sec. When WDI is three-stated or left unconnected, the maximum allowable leakage current is 10µA and the maximum allowable load capacitance is 200pF.

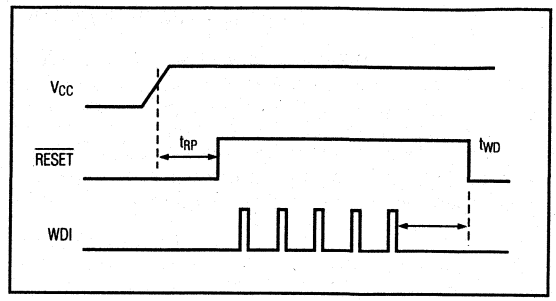


Figure 4. Watchdog Timing

Chip-Enable Gating (MAX818)

Internal gating of the chip-enable (CE) signal prevents erroneous data from corrupting CMOS RAM in the event of an undervoltage condition. The MAX818 uses a series transmission gate from $\overline{CE}$ IN to $\overline{CE}$ OUT (Figure 5). During normal operation (reset not asserted), the CE transmission gate is enabled and passes all CE transitions. When reset is asserted, this path becomes disabled, preventing erroneous data from corrupting the CMOS RAM. The short CE propagation delay from $\overline{CE}$ IN to $\overline{CE}$ OUT enables the MAX818 to be used with most µPs. If $\overline{CE}$ IN is low when reset asserts, $\overline{CE}$ OUT remains low for typically 15µs to permit the current write cycle to complete.

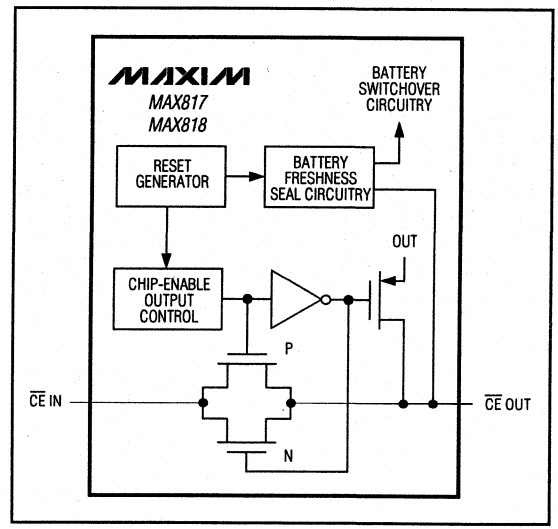


Figure 5. Chip-Enable Transmission Gate

Chip-Enable Input (MAX818)

The CE transmission gate is disabled and $\overline{CE}$ IN is high impedance (disabled mode) while reset is asserted. During a power-down sequence when V_{CC} passes the reset threshold, the CE transmission gate disables and $\overline{CE}$ IN immediately becomes high impedance if the voltage at $\overline{CE}$ IN is high. If $\overline{CE}$ IN is low when reset asserts, the CE transmission gate will disable 15µs after reset asserts (Figure 6). This permits the current write cycle to complete during power-down.

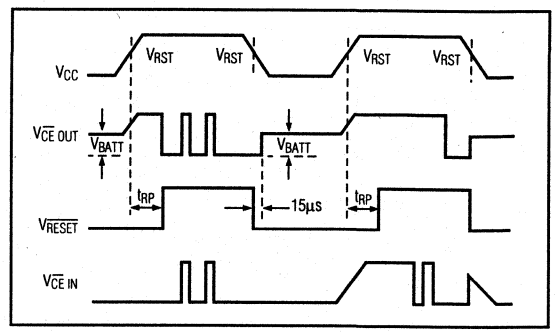


Figure 6. Chip-Enable Timing

Any time a reset is generated, the CE transmission gate remains disabled and $\overline{CE}$ IN remains high impedance (regardless of $\overline{CE}$ IN activity) for the reset timeout period. When the CE transmission gate is enabled, the impedance of $\overline{CE}$ IN appears as a 40Ω resistor in series with the load at $\overline{CE}$ OUT. The propagation delay through the CE transmission gate depends on V_{CC}, the source impedance of the drive connected to $\overline{CE}$ IN, and the loading on $\overline{CE}$ OUT (see *Typical Operating Characteristics*). The CE propagation delay is production tested from the 50% point on $\overline{CE}$ IN to the 50% point on $\overline{CE}$ OUT using a 50Ω driver and a 50pF load capacitance (Figure 7). For minimum propagation delay, minimize the capacitive load at $\overline{CE}$ OUT and use a low-output-impedance driver.

Chip-Enable Output (MAX818)

When the CE transmission gate is enabled, the impedance of $\overline{CE}$ OUT is equivalent to a 40Ω resistor in series with the source driving $\overline{CE}$ IN. In the disabled mode, the transmission gate is off and an active pull-up connects $\overline{CE}$ OUT to OUT (Figure 5). This pull-up turns off when the transmission gate is enabled.

Power-Fail Comparator (MAX817/MAX819)

The MAX817/MAX819 PFI input is compared to an internal reference. If PFI is less than the power-fail threshold (V_{PFT}), $\overline{PFO}$ goes low. The power-fail comparator is intended for use as an undervoltage detector to signal a failing power supply (Figure 8). However, the comparator does not need to be dedicated to this function because it is completely separate from the rest of the circuitry.

The power-fail comparator turns off and $\overline{PFO}$ goes low when V_{CC} falls below V_{BATT}. During the reset timeout period (t_{RP}), $\overline{PFO}$ is forced high, regardless of the state of V_{PFI} (see *Battery Freshness Seal* section). If the comparator is unused, connect PFI to ground and leave $\overline{PFO}$ unconnected. $\overline{PFO}$ can be connected to $\overline{MR}$ on the MAX819 so that a low voltage on PFI will generate a reset (Figure 9). In this configuration, when the monitored voltage causes PFI to fall below V_{PFT}, $\overline{PFO}$ pulls $\overline{MR}$ low, causing a reset to be asserted. Reset remains asserted as long as $\overline{PFO}$ holds $\overline{MR}$ low, and for t_{RP} (200ms) after $\overline{PFO}$ pulls $\overline{MR}$ high when the monitored supply is above the programmed threshold. When $\overline{PFO}$ is connected to $\overline{MR}$, it is not possible to enable the battery freshness seal. Enabling the battery freshness seal requires $\overline{MR}$ to be high or open. Once the battery freshness seal is enabled, it is no longer affected by $\overline{PFO}$'s connection to $\overline{MR}$.

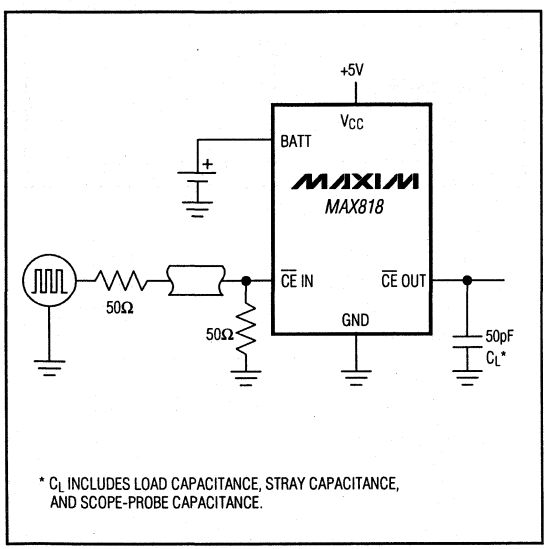


Figure 7. CE Propagation Delay Test Circuit

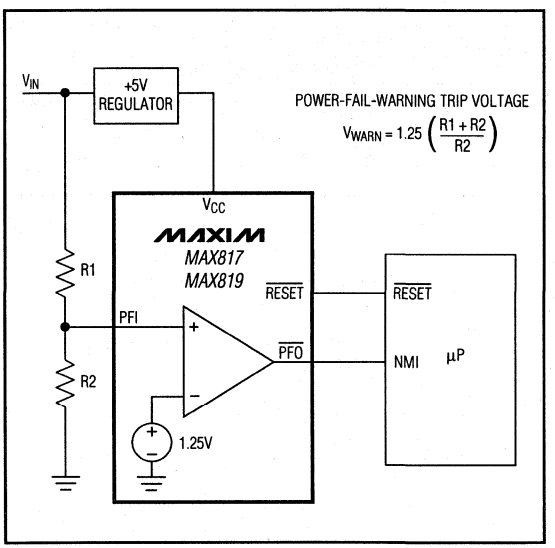


Figure 8. Using the Power-Fail Comparator to Generate a Power-Fail Warning

Backup-Battery Switchover

In a brownout or power failure, it may be necessary to preserve the contents of RAM. With a backup battery installed at BATT, the MAX817/MAX818/MAX819 automatically switch RAM to backup power when V_{CC} falls. These devices require two conditions before switching to battery-backup mode: 1) V_{CC} must be below the reset threshold, and 2) V_{CC} must be below V_{BATT}. Table 1 lists the status of the inputs and outputs in battery-backup mode.

As long as V_{CC} exceeds the reset threshold, OUT connects to V_{CC} through a 5Ω PMOS power switch. Once V_{CC} falls below the reset threshold, V_{CC} or V_{BATT} (whichever is higher) switches to OUT. When V_{CC} falls below V_{RST} and V_{BATT}, BATT switches to OUT through an 80Ω switch.

Table 1. Input and Output Status in Battery-Backup Mode

SIGNAL	STATUS
V_{CC}	Disconnected from V_{OUT}.
V_{OUT}	Connected to V_{BATT} through an internal 80Ω PMOS switch.
V_{BATT}	Connected to V_{OUT}. Current drawn from the battery is less than 1µA, as long as $V_{CC} < V_{BATT} - 0.2V$.
$V_{\overline{RESET}}$	Logic low
V_{WDI}	Watchdog timer is disabled.
$V_{\overline{CE}OUT}$	Logic high. The open-circuit voltage is equal to V_{OUT}.
$V_{\overline{CE}IN}$	High impedance

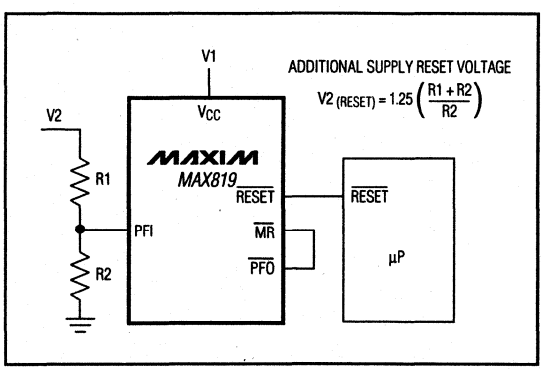
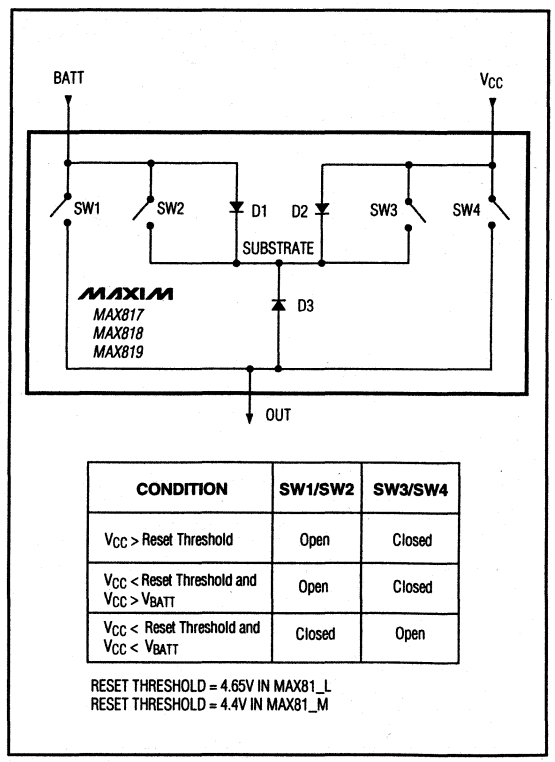


Figure 9. Monitoring an Additional Supply by Connecting $\overline{PFO}$ to $\overline{MR}$.

When V_{CC} exceeds the reset threshold, it is connected to the substrate, regardless of the voltage applied to BATT (Figure 10). During this time, the diode (D1) between BATT and the substrate will conduct current from BATT to V_{CC} if V_{BATT} is 0.6V greater than V_{CC}. When BATT connects to OUT, backup mode is activated and the internal circuitry is powered from the battery (Table 1). When V_{CC} is just below V_{BATT}, the current draw from BATT is typically 6µA. When V_{CC} drops to more than 1V below V_{BATT}, the internal switchover comparator shuts off and the supply current falls to less than 1µA.

Applications Information

The MAX817/MAX818/MAX819 are protected for typical short-circuit conditions of 10sec or less. Shorting OUT to ground for longer than 10sec destroys the device. Decouple V_{CC}, OUT, and BATT to ground by placing 0.1µF capacitors as close to the device as possible.



CONDITION	SW1/SW2	SW3/SW4
V_{CC} > Reset Threshold	Open	Closed
V_{CC} < Reset Threshold and $V_{CC} > V_{BATT}$	Open	Closed
V_{CC} < Reset Threshold and $V_{CC} < V_{BATT}$	Closed	Open

RESET THRESHOLD = 4.65V IN MAX81_L
RESET THRESHOLD = 4.4V IN MAX81_M

Figure 10. Backup-Battery-Switchover Block Diagram

Watchdog Input Current

The MAX817/MAX818 WDI inputs are internally driven through a buffer and series resistor from the watchdog counter (Figure 1). When WDI is left unconnected, the watchdog timer is serviced within the watchdog timeout period by a low-high-low pulse from the counter chain. For minimum watchdog input current (minimum overall power consumption), leave WDI low for the majority of the watchdog timeout period, pulsing it low-high-low once within 7/8 of the watchdog timeout period to reset the watchdog timer. If instead WDI is externally driven high for the majority of the timeout period, up to 150µA can flow into WDI.

Using a SuperCap™ as a Backup Power Source

SuperCaps are capacitors with extremely high capacitance values (on the order of 0.47F) for their size. Since BATT has the same operating voltage range as V_{CC}, and the battery switchover threshold voltages are typically ±30mV centered at V_{BATT}, a SuperCap and simple charging circuit can be used as a backup power source. Figure 11 shows a SuperCap used as a backup source.

If V_{CC} is above the reset threshold and V_{BATT} is 0.5V above V_{CC}, current flows to OUT and V_{CC} from BATT until the voltage at BATT is less than 0.5V above V_{CC}. For example, if a SuperCap is connected to BATT through a diode to V_{CC}, and V_{CC} quickly changes from 5.4V to 4.9V, the capacitor discharges through OUT and V_{CC} until V_{BATT} reaches 5.1V typical. Leakage current through the SuperCap charging diode and the internal power diode eventually discharges the SuperCap to V_{CC}. Also, if V_{CC} and V_{BATT} start from 0.1V above the reset threshold and power is lost at V_{CC}, the SuperCap on BATT discharges through V_{CC} until V_{BATT} reaches the reset threshold. Battery-backup mode is then initiated and the current through V_{CC} goes to zero.

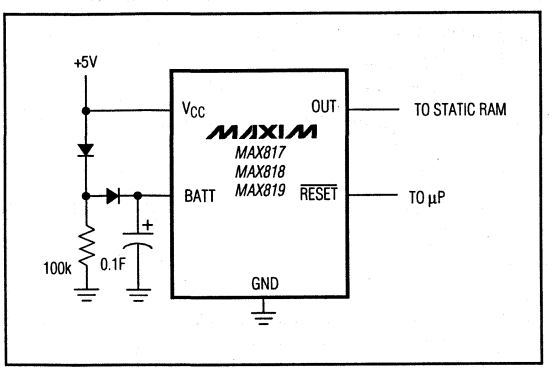


Figure 11. Using a SuperCap™ as a Backup Power Source with a +5V ±10% Supply

SuperCap is a trademark of Baknor Industries.

Operation Without a Backup Power Source

The MAX817/MAX818/MAX819 were designed for battery-backed applications. If a backup battery is not used, connect V_{CC} to OUT, and connect BATT to ground.

Replacing the Backup Battery

The backup power source can be removed while V_{CC} remains valid, without danger of triggering a reset pulse, if BATT is decoupled with a 0.1µF capacitor to ground. As long as V_{CC} stays above the reset threshold, battery-backup mode cannot be entered.

Adding Hysteresis to the Power-Fail Comparator (MAX817/MAX819)

The power-fail comparator has a typical input hysteresis of 4mV. This is sufficient for most applications where a power-supply line is being monitored through an external voltage divider (see *Monitoring an Additional Supply*).

For additional noise margin, connect a resistor between $\overline{PFO}$ and PFI, as shown in Figure 12. Select the ratio of R1 and R2 such that PFI sees V_{PFT} when V_{IN} falls to the

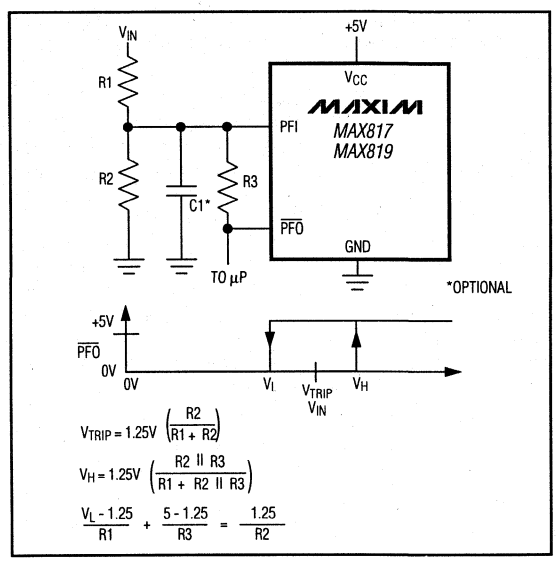


Figure 12. Adding Hysteresis to the Power-Fail Comparator

desired trip point (V_{TRIP}). Resistor R3 adds hysteresis. It will typically be an order of magnitude greater than R1 or R2. The current through R1 and R2 should be at least 1µA to ensure that the 25nA (max) PFI input leakage current does not shift the trip point. R3 should be larger than 200kΩ to prevent it from loading down the $\overline{PFO}$ pin. Capacitor C1 adds additional noise rejection.

Monitoring an Additional Supply (MAX817/MAX819)

The MAX817/MAX819 µP supervisors can monitor either positive or negative supplies using a resistor voltage divider to PFI. $\overline{PFO}$ can be used to generate an interrupt to the µP or to trigger a reset (Figures 9 and 13).

Interfacing to µPs with Bidirectional Reset Pins

µPs with bidirectional reset pins, such as the Motorola 68HC11 series, can contend with the MAX817/MAX818/MAX819 $\overline{RESET}$ output. If, for example, the $\overline{RESET}$ output is driven high and the µP wants to pull it low, indeterminate logic levels may result. To correct this, connect a 4.7kΩ resistor between the $\overline{RESET}$ output and the µP reset I/O, as in Figure 14. Buffer the $\overline{RESET}$ output to other system components.

Negative-Going V_{CC} Transients

These supervisors are relatively immune to short-duration, negative-going V_{CC} transients (glitches) while issuing a reset to the µP during power-up, power-down, and brownout conditions. Therefore, resetting the µP when V_{CC} experiences only small glitches is usually not desirable.

The *Typical Operating Characteristics* show a graph of Maximum Transient Duration vs. Reset Threshold Overdrive for which reset pulses are **not** generated. The graph was produced using negative-going V_{CC} pulses, starting at 3.3V and ending below the reset threshold by the magnitude indicated (reset threshold overdrive). The graph shows the maximum pulse width that a negative-going V_{CC} transient can typically have without triggering a reset pulse. As the amplitude of the transient increases (i.e., goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a V_{CC} transient that goes 100mV below the reset threshold and lasts for 135µs will not trigger a reset pulse.

A 0.1µF bypass capacitor mounted close to the V_{CC} pin provides additional transient immunity.

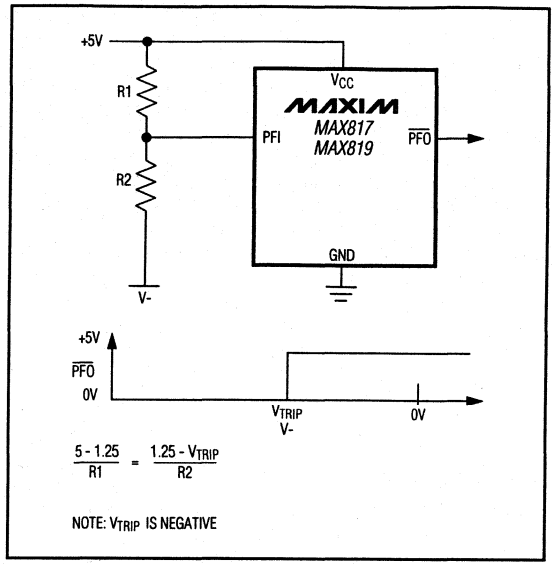


Figure 13. Monitoring a Negative Voltage

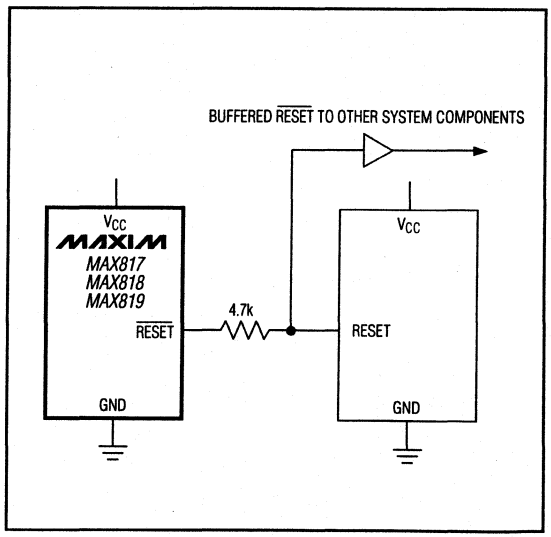


Figure 14. Interfacing to µPs with Bidirectional Reset I/O

Watchdog Software Considerations (MAX817/MAX818)

To help the watchdog timer monitor software execution more closely, set and reset the watchdog input at different points in the program, rather than "pulsing" the watchdog input high-low-high or low-high-low. This technique avoids a "stuck" loop, in which the watchdog timer would continue to be reset within the loop, keeping the watchdog from timing out. Figure 15 shows an example of a flow diagram where the I/O driving the watchdog input is set high at the beginning of the program, set low at the beginning of every subroutine or loop, then set high again when the program returns to the beginning. If the program should "hang" in any subroutine, the problem would quickly be corrected, since the I/O is continually set low and the watchdog timer is allowed to time out, triggering a reset or an interrupt. As described in the *Watchdog Input Current* section, this scheme results in higher average WDI input current than does the method of leaving WDI low for the majority of the timeout period and periodically pulsing it low-high-low.

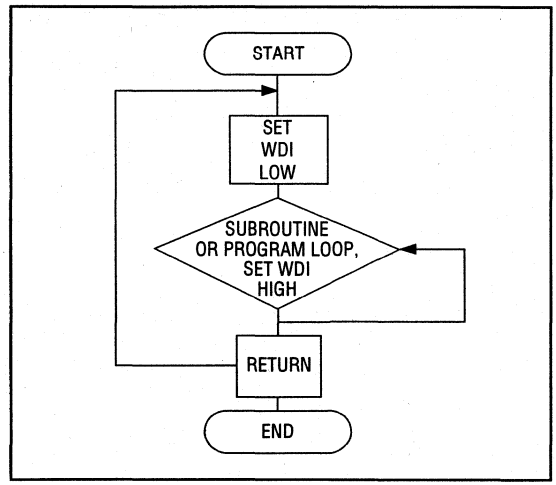
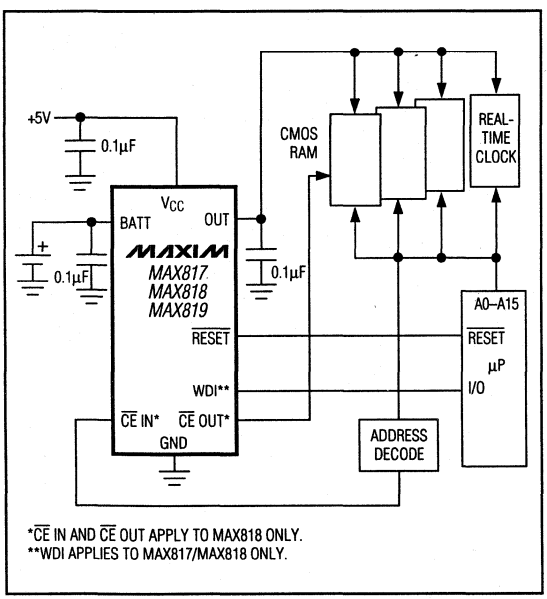


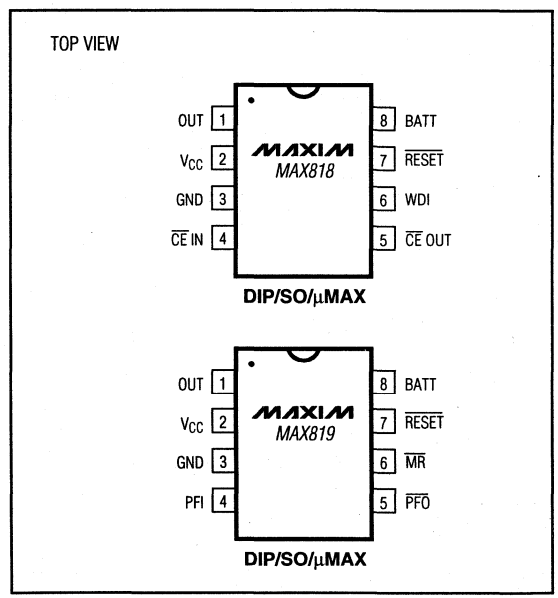
Figure 15. Watchdog Flow Diagram

Typical Operating Circuit



*CE IN AND CE OUT APPLY TO MAX818 ONLY.
**WDI APPLIES TO MAX817/MAX818 ONLY.

Pin Configurations (continued)



_Ordering Information (continued)

PART†	TEMP. RANGE	PIN-PACKAGE
MAX817_EPA	-40°C to +85°C	8 Plastic DIP
MAX817_ESA	-40°C to +85°C	8 SO
MAX818_CPA	0°C to +70°C	8 Plastic DIP
MAX818_CSA	0°C to +70°C	8 SO
MAX818_CUA	0°C to +70°C	8 µMAX
MAX818_EPA	-40°C to +85°C	8 Plastic DIP
MAX818_ESA	-40°C to +85°C	8 SO
MAX819_CPA	0°C to +70°C	8 Plastic DIP
MAX819_CSA	0°C to +70°C	8 SO
MAX819_CUA	0°C to +70°C	8 µMAX
MAX819_EPA	-40°C to +85°C	8 Plastic DIP
MAX819_ESA	-40°C to +85°C	8 SO

†*These parts offer a choice of reset threshold voltage. From the table below, select the suffix corresponding to the desired threshold and insert it into the blank to complete the part number.*

SUFFIX	RESET THRESHOLD (V)
L	4.65
M	4.40

_____Chip Information

TRANSISTOR COUNT: 719

19-1122; Rev 0; 9/96

MAXIM

4-Pin µP Voltage Monitors with Pin-Selectable Power-On Reset Timeout Delay

General Description

The MAX821/MAX822 microprocessor (µP) supervisory circuits monitor power supplies in µP and digital systems. They provide excellent circuit reliability and low cost by eliminating external components and adjustments when used with 5V-powered or 3V-powered circuits. The MAX821/MAX822 also provide a power-on reset timeout delay that is pin selectable to 1ms (max), 20ms (min), or 100ms (min).

These devices perform a single function: they assert a reset signal whenever the V_{CC} supply voltage falls below a preset threshold, and they keep reset asserted for the pin-selected reset timeout delay after V_{CC} has risen above the reset threshold. The only difference between the two devices is that the MAX821 has an active-low $\overline{RESET}$ output (which is guaranteed to be in the correct state for V_{CC} down to 1V), while the MAX822 has an active-high RESET output. The reset comparator is designed to ignore fast transients on V_{CC}. Reset thresholds suitable for operation with a variety of supply voltages are available.

Low supply current makes the MAX821/MAX822 ideal for use in portable equipment. These devices come in a 4-pin SOT143 package.

Applications

Bar-Code Scanners

Computers

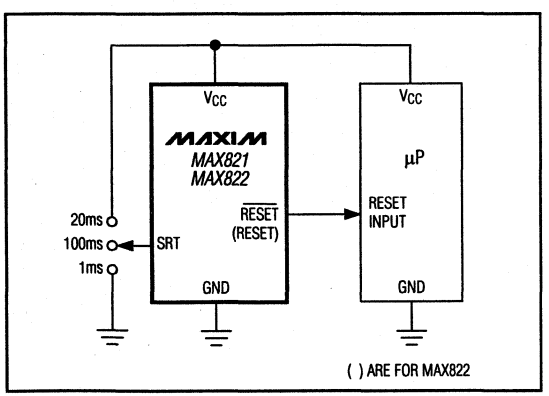
Controllers

Intelligent Instruments

Critical µP and µC Power Monitoring

Portable/Battery-Powered Equipment

Typical Operating Circuit



Features

- **Pin-Selectable, Precision Power-On Reset Delay: 1ms (max), 20ms (min), or 100ms (min)**
- **Precision Monitoring of +3V to +5V Power-Supply Voltages**
- **2.5µA Supply Current**
- **Guaranteed Over Temperature**
- **Guaranteed $\overline{RESET}$ Valid to V_{CC} = 1V (MAX821)**
- **Power-Supply Transient Immunity**
- **No External Components**
- **SOT143 Package**

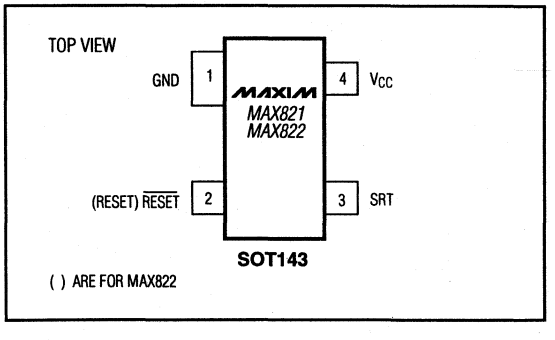
Ordering Information

PART	NOMINAL V_{TH} (V)	PKG. TOP MARK*
MAX821LUS-T	4.63	AZ_ _
MAX821MUS-T	4.38	BA_ _
MAX821PUS-T	4.00	BM_ _
MAX821TUS-T	3.08	BB_ _
MAX821SUS-T	2.93	BC_ _
MAX821UUS-T	2.78	BL_ _
MAX821RUS-T	2.63	BD_ _
MAX822LUS-T	4.63	BF_ _
MAX822MUS-T	4.38	BG_ _
MAX822TUS-T	3.08	BH_ _
MAX822SUS-T	2.93	BJ_ _
MAX822RUS-T	2.63	BK_ _

** The first two letters in the package top mark identify the part, while the remaining two letters are the lot-tracking code.*

NOTE: These parts are offered in the SOT143-4 package, in the extended temperature range (-40°C to +85°C).

Pin Configuration



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

4-Pin µP Voltage Monitors with Pin-Selectable Power-On Reset Timeout Delay

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)
- V_{CC} ..... -0.3V to 6.0V
- All Other Inputs..... -0.3V to (V_{CC} + 0.3V)

Input Current, V_{CC}, SRT..... 20mA
Output Current, RESET or $\overline{RESET}$..... 20mA

Continuous Power Dissipation (T_A = +70°C)
- SOT143-4 (derate 4mW/°C above +70°C)..... 320mW

Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = full range, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC} Range		T_A = 0°C to +70°C		1.0		5.5	V
		T_A = -40°C to +85°C		1.2		5.5	
Supply Current	I_{CC}	MAX82_L/M/P, V_{CC} = 5.5V, I_{OUT} = 0A	T_A = +25°C		2.5	7.0	µA
			T_A = T_{MIN} to T_{MAX}			12	
		MAX82_R/S/T/U, V_{CC} = 3.6V, I_{OUT} = 0A	T_A = +25°C		1.8	5.5	
			T_A = T_{MIN} to T_{MAX}			9	
Reset Threshold (Note 1)	V_{TH}	MAX82_L	T_A = +25°C	4.56	4.63	4.70	V
			T_A = 0°C to +70°C	4.50		4.75	
		MAX82_M	T_A = +25°C	4.31	4.38	4.45	
			T_A = 0°C to +70°C	4.25		4.50	
		MAX82_P	T_A = +25°C	3.97	4.00	4.04	
			T_A = 0°C to +70°C	3.91		4.09	
		MAX82_T	T_A = +25°C	3.04	3.08	3.11	
			T_A = 0°C to +70°C	3.00		3.15	
		MAX82_S	T_A = +25°C	2.89	2.93	2.96	
			T_A = 0°C to +70°C	2.85		3.00	
		MAX82_U	T_A = +25°C	2.74	2.78	2.81	
			T_A = 0°C to +70°C	2.70		2.85	
		MAX82_R	T_A = +25°C	2.59	2.63	2.66	
			T_A = 0°C to +70°C	2.55		2.70	
Reset Threshold Tempco					30		ppm/°C
V_{CC} to Reset Delay (Note 1)		V_{CC} falling at 1mV/µs			50		µs
Reset Active Timeout Period	t_{RP}	SRT = GND		0.5	0.8	1	ms
		SRT = V_{CC}		20	32	40	
		SRT = unconnected		100	160	200	
SRT Input Current (Note 2)		$\overline{RESET}$ = low for MAX821, RESET = high for MAX822	SRT = GND	-100			µA
			SRT = V_{CC}			100	
			SRT = unconnected	-1		1	
SRT Input Threshold	V_{IL}	$\overline{RESET}$ = low for MAX821, RESET = high for MAX822				0.07V_{CC}	V
	V_{IH}			0.9V_{CC}			
	V_{OPEN}				0.5V_{CC}		

4-Pin µP Voltage Monitors with Pin-Selectable Power-On Reset Timeout Delay

ELECTRICAL CHARACTERISTICS (continued)

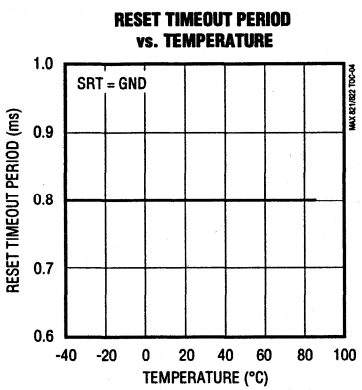
(V_{CC} = full range, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

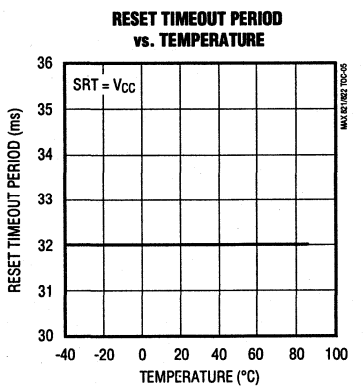
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SRT Input Capacitance (Note 3) (see *Setting the Reset Timeout Delay* section)		Internal				20	pF
$\overline{RESET}$ Output Voltage (MAX821)	V_{OL}	MAX821L/M/P only, I_{SINK} = 3.2mA, V_{CC} = $V_{TH(MIN)}$				0.4	V
		MAX821R/S/T/U only, I_{SINK} = 1.2mA, V_{CC} = $V_{TH(MIN)}$				0.3	
		I_{SINK} = 50µA	T_A = 0°C to +70°C, V_{CC} ≥ 1V			0.3	
			T_A = -40°C to +85°C, V_{CC} ≥ 1.2V			0.3	
	V_{OH}	MAX821L/M/P only, I_{SOURCE} = 800µA, V_{CC} ≥ $V_{TH(MAX)}$		V_{CC} -1.5			
		MAX821R/S/T/U only, I_{SOURCE} = 500µA, V_{CC} ≥ $V_{TH(MAX)}$		0.8V_{CC}			
RESET Output Voltage (MAX822)	V_{OL}	MAX822L/M only, I_{SINK} = 3.2mA, V_{CC} = $V_{TH(MAX)}$				0.4	V
		MAX822R/S/T only, I_{SINK} = 1.2mA, V_{CC} = $V_{TH(MAX)}$				0.3	
	V_{OH}	I_{SOURCE} = 150µA, 1.4V ≤ V_{CC} ≤ $V_{TH(MIN)}$		0.8V_{CC}			

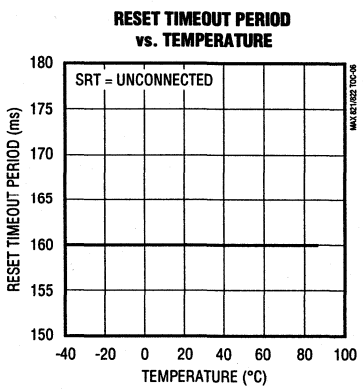
Note 1: $\overline{RESET}$ output for MAX821; RESET output for MAX822.
Note 2: During reset active timeout period only.
Note 3: Guaranteed by design.

Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)





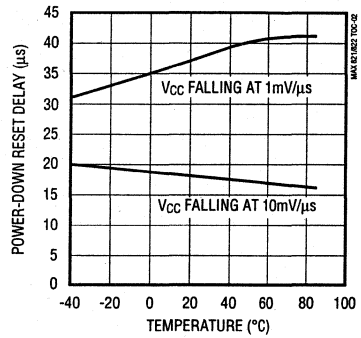


4-Pin µP Voltage Monitors with Pin-Selectable Power-On Reset Timeout Delay

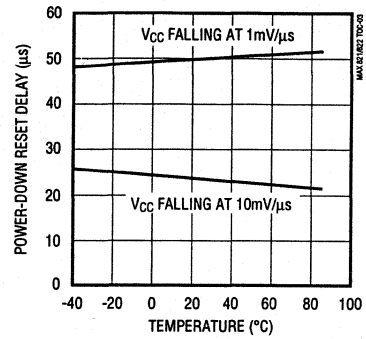
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

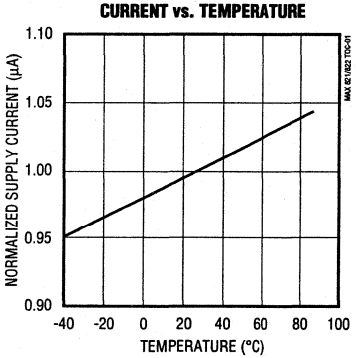
MAX82_R/S/T POWER-DOWN RESET DELAY vs. TEMPERATURE



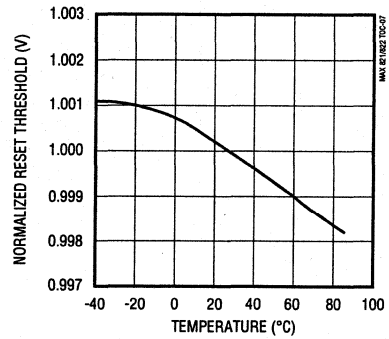
MAX82_L/M POWER-DOWN RESET DELAY vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED RESET THRESHOLD vs. TEMPERATURE



Pin Description

PIN		NAME	FUNCTION
MAX821	MAX822		
1	1	GND	Ground
2	–	$\overline{\text{RESET}}$	Active-Low Reset Output. $\overline{\text{RESET}}$ is low while V_{CC} is below the reset threshold. It remains low for the reset timeout period after the reset condition is terminated. The reset timeout period is determined by the SRT input.
–	2	RESET	Active-High Reset Output. RESET is high while V_{CC} is below the reset threshold. It remains high for the reset timeout period after the reset condition is terminated. The reset timeout period is determined by the SRT input.
3	3	SRT	Set Reset Timeout Input. Connect to GND for 1ms (max) delay; connect to V_{CC} for 20ms (min) delay; leave unconnected for 100ms (min) delay.
4	4	V_{CC}	Supply Voltage

4-Pin µP Voltage Monitors with Pin-Selectable Power-On Reset Timeout Delay

Detailed Description

Reset Output

A microprocessor's (µP's) reset input starts the µP in a known state. These µP supervisory circuits assert reset to prevent code-execution errors during power-up, power-down, or brownout conditions. They also provide a reset timeout delay that is pin programmable to 1ms (max), 20ms (min), or 100ms (min). This feature allows flexibility in designing bar-code scanners, hand-held devices, and other applications that require quick or nonstandard power-up times.

The MAX821's $\overline{RESET}$ output is guaranteed to be a logic low for V_{CC} > 1V. Once V_{CC} exceeds the reset threshold, an internal timer keeps $\overline{RESET}$ low for the reset timeout period, as determined by the Set Reset Timeout (SRT) input. See the *Setting the Reset Timeout Delay* section.

If a brownout condition occurs (V_{CC} dips below the reset threshold), $\overline{RESET}$ goes low. Any time V_{CC} goes below the reset threshold, the internal timer resets to zero, and $\overline{RESET}$ goes low. The internal timer begins counting after V_{CC} returns above the reset threshold, and $\overline{RESET}$ remains low for the reset timeout period.

The MAX822 has an active-high RESET output that is the inverse of the MAX821's $\overline{RESET}$ output.

Setting the Reset Timeout Delay

Use the three-level Set Reset Timeout (SRT) input to set the reset timeout delay. Connect SRT to GND for a 1ms (max) delay; connect it to V_{CC} for a 20ms (min) delay; or leave it unconnected for a 100ms (min) delay.

If you choose to drive the SRT pin with an external signal, make sure the signal source can charge/discharge the capacitance on SRT quickly enough (<500µs) to avert an unintended reset timeout delay.

To ensure proper operation when selecting the 100ms timeout (SRT = unconnected), minimize capacitive loading on the SRT pin (< 200pF). Excessive capacitive loading can select an unintended faster timeout mode.

Reset Threshold Accuracy

The MAX821/MAX822 are designed to meet their worst-case specifications over their entire operating temperature range. Choose a reset threshold guaranteed to assert at a voltage below the power supply's regulation range and above the minimum specified operating voltage range for the system's ICs.

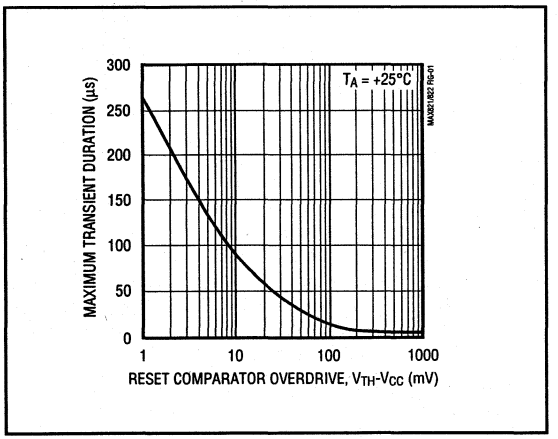


Figure 1. Maximum Transient Duration Without Causing a Reset Pulse vs. Comparator Overdrive

Applications Information

Negative-Going V_{CC} Transients

While designed to issue a reset to the microprocessor (µP) during power-up, power-down, and brownout conditions, the MAX821/MAX822 are relatively immune to short-duration, negative-going V_{CC} transients (glitches).

Figure 1 shows the maximum transient duration vs. reset comparator overdrive for which the MAX821/MAX822 typically do not generate a reset pulse. This graph was generated using a negative-going pulse applied to V_{CC}, starting above the actual reset threshold and ending below it by the magnitude indicated (reset comparator overdrive). The graph indicates the typical maximum pulse width a negative-going V_{CC} transient may have without causing a reset pulse to be issued. As the magnitude of the transient increases (goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, for the MAX821/MAX822, a V_{CC} transient that goes 100mV below the reset threshold and lasts 12µs or less will not cause a reset pulse to be issued. A 0.1µF capacitor mounted as close as possible to V_{CC} can provide additional transient immunity, if desired.

4-Pin µP Voltage Monitors with Pin-Selectable Power-On Reset Timeout Delay

Ensuring a Valid $\overline{RESET}$ Output Down to V_{CC} = 0V

When V_{CC} falls below 1V, the MAX821 $\overline{RESET}$ output no longer sinks current—it becomes an open circuit. Therefore, high-impedance CMOS logic inputs connected to the $\overline{RESET}$ output can drift to undetermined voltages. This presents no problem in most applications, since most µP and other circuitry is inoperative with V_{CC} below 1V. However, in applications where the $\overline{RESET}$ output must be valid down to 0V, adding a pull-down resistor to the $\overline{RESET}$ pin will cause any stray leakage currents to flow to ground, holding $\overline{RESET}$ low (Figure 2a). R1's value is not critical; 100kΩ is large enough not to load $\overline{RESET}$, and small enough to pull $\overline{RESET}$ to ground.

A 100kΩ pull-up resistor to V_{CC} is also recommended for the MAX822 if RESET is required to remain valid for V_{CC} < 1V (Figure 2b).

Interfacing to µPs with Bidirectional Reset Pins

µPs with bidirectional reset pins (such as the Motorola 68HC11 series) can contend with the MAX821 reset output. For example, if the MAX821 $\overline{RESET}$ output is asserted high and the µP wants to pull it low, indeterminate logic levels may result. To correct such cases, connect a 4.7kΩ resistor between the MAX821 $\overline{RESET}$ output and the µP reset I/O (Figure 3). Buffer the reset output to other system components.

Chip Information

TRANSISTOR COUNT: 492

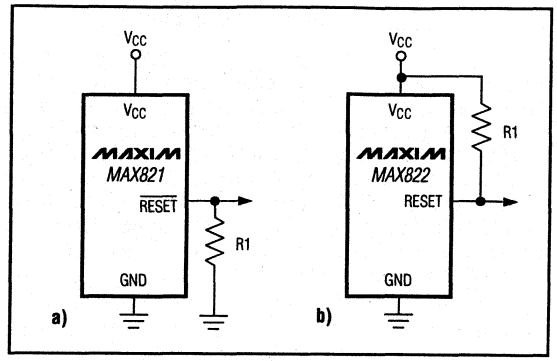


Figure 2. $\overline{RESET}$/RESET Valid to V_{CC} = Ground Circuit

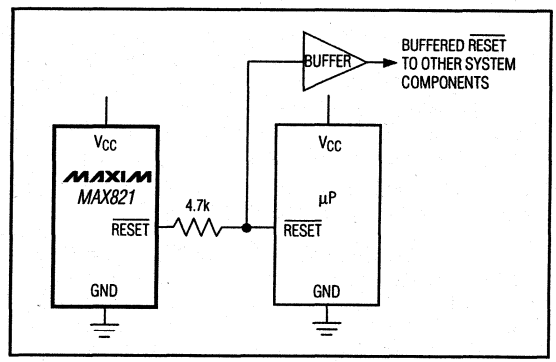
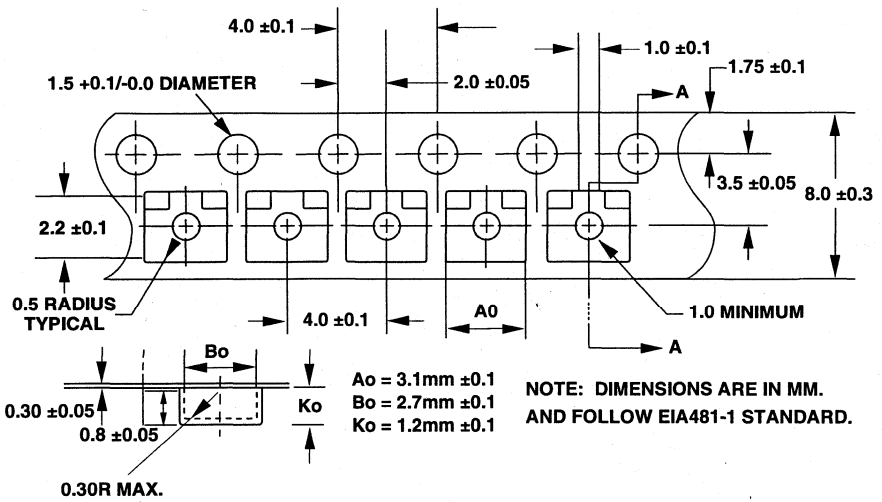


Figure 3. Interfacing to µPs with Bidirectional Reset I/O

4-Pin µP Voltage Monitors with Pin-Selectable Power-On Reset Timeout Delay

Tape-and-Reel Information



5

19-0487; Rev 0; 3/96

MAXIM

5-Pin Microprocessor Supervisory Circuits

General Description

The MAX823/MAX824/MAX825* microprocessor (µP) supervisory circuits combine reset output, watchdog, and manual-reset input functions in a 5-pin SOT23-5 package. They significantly improve system reliability and accuracy compared to separate ICs or discrete components. The MAX823/MAX824/MAX825 are specifically designed to ignore fast transients on V_{CC}.

Five preprogrammed reset threshold voltages are available, designated by the following package suffixes: L = 4.63V, M = 4.38V, T = 3.08V, S = 2.93V, and R = 2.63V. All three devices have an active-low reset output, which is guaranteed to be in the correct state for V_{CC} down to 1V. The MAX824/MAX825 also have an active-high reset output. The following *Selector Guide* explains the functions offered in this series of parts.

Applications

Battery-Powered Computers and Controllers
Embedded Controllers
Intelligent Instruments
Automotive Systems
Critical µP Monitoring
Portable/Battery-Powered Equipment

Selector Guide

FUNCTION	MAX823	MAX824	MAX825
Active-Low Reset	✔	✔	✔
Active-High Reset	—	✔	✔
Watchdog Input	✔	✔	—
Manual-Reset Input	✔	—	✔

Typical Operating Circuit appears at end of data sheet.
Marking Information appears at end of data sheet.

Features

- ♦ **Precision Monitoring of +3V, +3.3V, and +5V Power Supplies**
- ♦ **Operating Current: 10µA (MAX823L/M) 3µA (MAX825T/S/R)**
- ♦ **Fully Specified Over Temperature**
- ♦ **140ms Min Power-On Reset**
- ♦ **Guaranteed $\overline{RESET}$ Valid to V_{CC} = 1V**
- ♦ **Power-Supply Transient Immunity**
- ♦ **Watchdog Timer with 1.6sec Timeout (MAX823/MAX824)**
- ♦ **Manual-Reset Input (MAX823/MAX825)**
- ♦ **No External Components**

Ordering Information

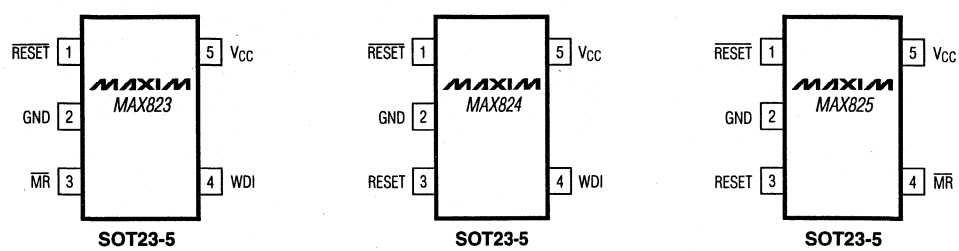
PART†	TEMP. RANGE	PIN-PACKAGE
MAX823_EUK	-40°C to +85°C	5 SOT23-5
MAX824_EUK‡	-40°C to +85°C	5 SOT23-5
MAX825_EUK‡	-40°C to +85°C	5 SOT23-5

†*Insert the desired suffix letter (from the table below) into the blank to complete the part number.*
‡*Future product—contact factory for availability.*

SUFFIX	RESET THRESHOLD (V)
L	4.63
M	4.38
T	3.08
S	2.93
R	2.63

Pin Configurations

TOP VIEW



*Patents Pending

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

5-Pin Microprocessor Supervisory Circuits

ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... -0.3V to +6.0V
All Other Pins ..... -0.3V to (V_{CC} + 0.3V)
Input Current, All Pins Except RESET and $\overline{RESET}$ 20mA
Output Current, RESET, $\overline{RESET}$ 20mA
Rate of Rise, V_{CC} 100V/µs
Continuous Power Dissipation (T_A = +70°C)
SOT23-5 (derate 7.1mW/°C above +70°C) 571mW

Operating Temperature Range
MAX82_EUK ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.75V to +5.5V for MAX82_L, V_{CC} = +4.5V to +5.5V for MAX82_M, V_{CC} = +3.15V to +3.6V for MAX82_T, V_{CC} = +3V to +3.6V for MAX82_S, V_{CC} = +2.7V to +3.6V for MAX82_R, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}	T_A = 0°C to +70°C		1.0		5.5	V
		T_A = -40°C to +85°C		1.2			
Supply Current	I_{SUPPLY}	WDI and $\overline{MR}$ unconnected	MAX823L/M, MAX824L/M		10	24	µA
			MAX823T/S/R, MAX824T/S/R		5	12	
		$\overline{MR}$ unconnected	MAX825L/M		4.5	12	
			MAX825T/S/R		3	8	
Reset Threshold	V_{RST}	MAX82_L	T_A = +25°C	4.56	4.63	4.70	V
			T_A = 0°C to +70°C	4.50		4.75	
		MAX82_M	T_A = +25°C	4.31	4.38	4.45	
			T_A = 0°C to +70°C	4.25		4.50	
		MAX82_T	T_A = +25°C	3.04	3.08	3.11	
			T_A = 0°C to +70°C	3.00		3.15	
		MAX82_S	T_A = +25°C	2.89	2.93	2.96	
			T_A = 0°C to +70°C	2.85		3.00	
		MAX82_R	T_A = +25°C	2.59	2.63	2.66	
			T_A = 0°C to +70°C	2.55		2.70	
Reset Threshold Hysteresis		MAX82_L/M			10		mV
		MAX82_T/S/R			5		
Reset Threshold Temperature Coefficient					40		ppm/°C
Reset Timeout Period	t_{RP}	MAX82_L/M		140	200	280	ms
		MAX82_T/S/R		140	200	280	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +4.75V to +5.5V for MAX82_L, V_{CC} = +4.5V to +5.5V for MAX82_M, V_{CC} = +3.15V to +3.6V for MAX82_T, V_{CC} = +3V to +3.6V for MAX82_S, V_{CC} = +2.7V to +3.6V for MAX82_R, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{RESET}$ Output Voltage	V_{OH}	MAX82_L/M, V_{CC} = V_{RST} max, I_{SOURCE} = 120µA	V_{CC} - 1.5			V
		MAX82_T/S/R, V_{CC} = V_{RST} max, I_{SOURCE} = 30µA	0.8V_{CC}			
	V_{OL}	MAX82_L/M, V_{CC} = V_{RST} min, I_{SINK} = 3.2mA			0.4	
		MAX82_T/S/R, V_{CC} = V_{RST} min, I_{SINK} = 1.2mA			0.3	
		T_A = 0°C to +70°C, V_{CC} = 1V, V_{CC} falling, I_{SINK} = 50µA			0.3	
		T_A = 0°C to +70°C, V_{CC} = 1.2V, V_{CC} falling, V_{BATT} = 0V, I_{SINK} = 100µA			0.3	
$\overline{RESET}$ Output Short-Circuit Current (Note 2)	I_{SOURCE}	MAX82_L/M, $\overline{RESET}$ = 0V, V_{CC} = 5.5V			800	µA
		MAX82_T/S/R, $\overline{RESET}$ = 0V, V_{CC} = 3.6V			400	
RESET Output Voltage	V_{OH}	V_{CC} > 1.8V, I_{SOURCE} = 150µA	0.8V_{CC}			V
	V_{OL}	MAX824L/M, MAX825L/M, V_{CC} = V_{RST} max, I_{SINK} = 3.2mA			0.4	
		MAX824T/S/R, MAX825T/S/R, V_{CC} = V_{RST} max, I_{SINK} = 1.2mA			0.3	
V_{CC} to $\overline{RESET}$ Delay		V_{RST} - V_{CC} = 100mV		20		µs
WATCHDOG INPUT (MAX823/MAX824)						
Watchdog Timeout Period	t_{WD}		1.12	1.60	2.40	sec
WDI Pulse Width	t_{WDI}	V_{IL} = 0.4V, V_{IH} = 0.8V_{CC}	50			ns
WDI Input Threshold (Note 3)	V_{IL}	V_{CC} = 5V			0.3V_{CC}	V
	V_{IH}		0.7V_{CC}			
WDI Input Current (Note 4)		WDI = V_{CC}, time average		120	160	µA
		WDI = 0V, time average	-20	-15		
MANUAL-RESET INPUT (MAX823/MAX825)						
$\overline{MR}$ Input Threshold	V_{IL}		0.3V_{CC}			V
	V_{IH}				0.7V_{CC}	
$\overline{MR}$ Pulse Width			1.0			µs
$\overline{MR}$ Noise Immunity (pulse width with no reset)				100		ns
$\overline{MR}$ to Reset Delay				500		ns
$\overline{MR}$ Pull-Up Resistance (internal)			35	52	75	kΩ

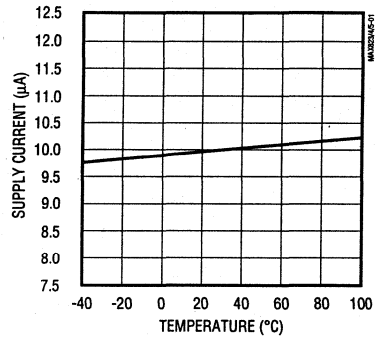
Note 1: Over-temperature limits are guaranteed by design and not production tested.
Note 2: The $\overline{RESET}$ short-circuit current is the maximum pull-up current when $\overline{RESET}$ is driven low by a µP bidirectional reset pin.
Note 3: WDI is internally serviced within the watchdog period if WDI is left unconnected.
Note 4: The WDI input current is specified as the average input current when the WDI input is driven high or low. The WDI input is designed to drive a three-stated-output device with a 10µA maximum leakage current and a maximum capacitive load of 200pF. This output device must be able to source and sink at least 200µA when active.

5-Pin Microprocessor Supervisory Circuits

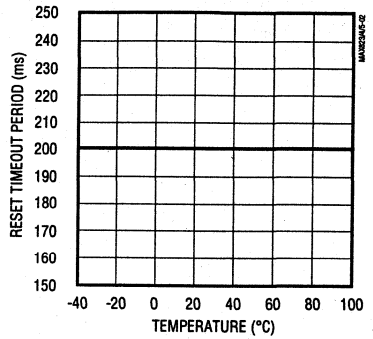
Typical Operating Characteristics

(MAX823L, V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

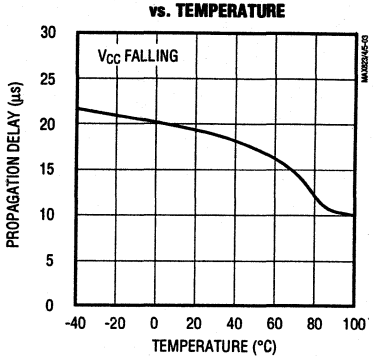
V_{CC} SUPPLY CURRENT vs. TEMPERATURE



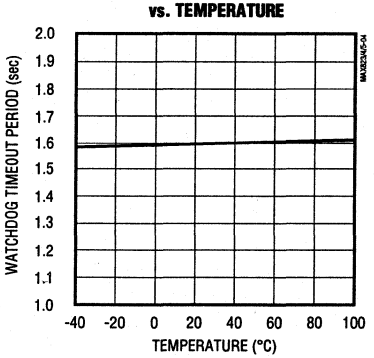
RESET TIMEOUT PERIOD vs. TEMPERATURE



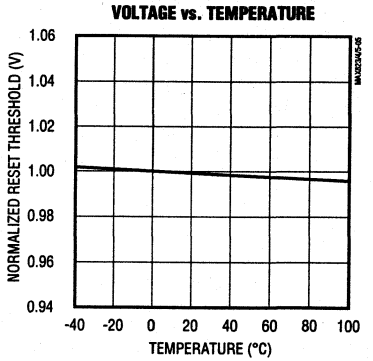
RESET COMPARATOR PROPAGATION DELAY vs. TEMPERATURE



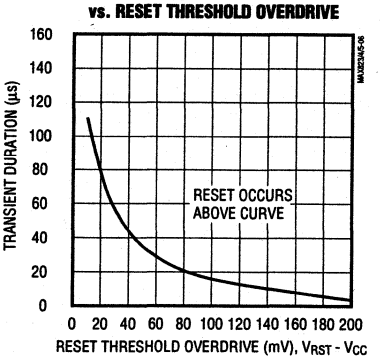
WATCHDOG TIMEOUT PERIOD vs. TEMPERATURE



NORMALIZED RESET THRESHOLD VOLTAGE vs. TEMPERATURE



MAXIMUM V_{CC} TRANSIENT DURATION vs. RESET THRESHOLD OVERDRIVE



5-Pin Microprocessor Supervisory Circuits

Pin Description

PIN			NAME	FUNCTION
MAX823	MAX824	MAX825		
1	1	1	$\overline{\text{RESET}}$	Active-Low Reset Output. Pulses low for 200ms when triggered, and remains low whenever V_{CC} is below the reset threshold or when $\overline{MR}$ is a logic low. It remains low for 200ms after one of the following occurs: V_{CC} rises above the reset threshold, the watchdog triggers a reset, or $\overline{MR}$ goes low to high.
2	2	2	GND	Ground. 0V reference for all signals.
3	—	4	$\overline{MR}$	Manual-Reset Input. A logic low on $\overline{MR}$ asserts reset. Reset remains asserted as long as $\overline{MR}$ is held low and for 200ms after $\overline{MR}$ returns high. The active-low input has an internal 52kΩ pull-up resistor. It can be driven from a CMOS-logic line or shorted to ground with a switch. Leave open or connect to V_{CC} if unused.
—	3	3	RESET	Active-High Reset Output. Inverse of $\overline{\text{RESET}}$.
4	4	—	WDI	Watchdog Input. If WDI remains either high or low for longer than the watchdog timeout period, the internal watchdog timer runs out and a reset is triggered. The internal watchdog timer clears whenever reset is asserted, or whenever WDI sees a rising or falling edge. If WDI is left unconnected or is connected to a three-stated buffer output, the watchdog feature is disabled.
5	5	5	V_{CC}	Supply Voltage

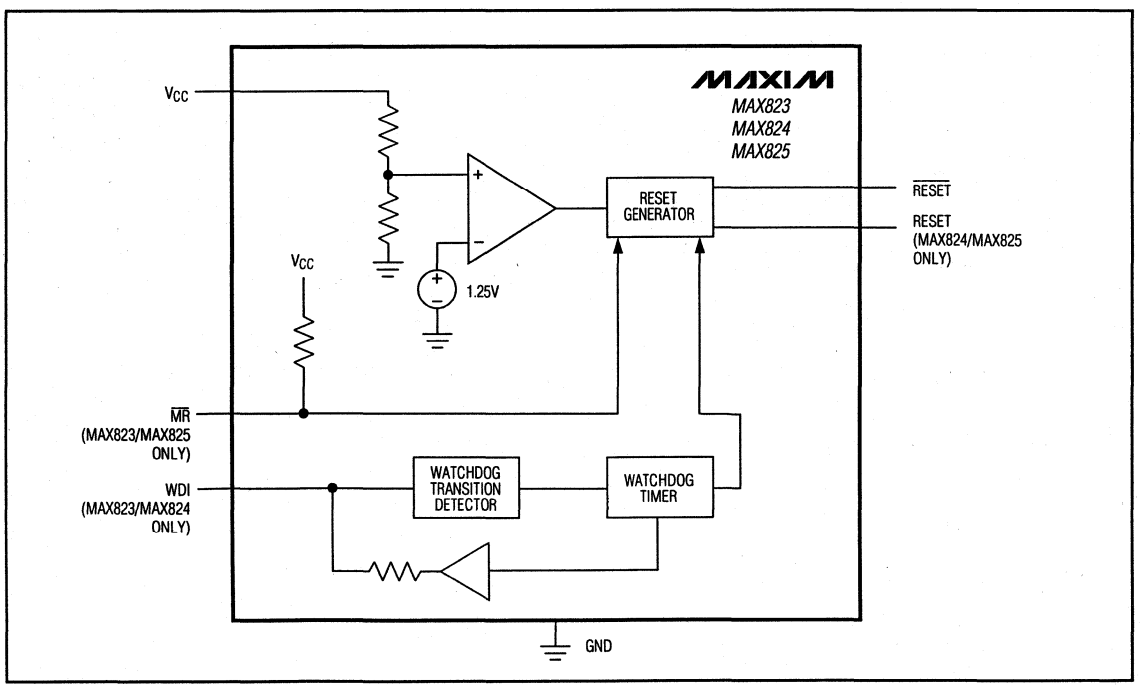


Figure 1. Functional Diagram

5-Pin Microprocessor Supervisory Circuits

Detailed Description

RESET Output

A microprocessor's (µP's) reset input starts the µP in a known state. The MAX823/MAX824/MAX825 µP supervisory circuits assert a reset to prevent code-execution errors during power-up, power-down, and brownout conditions. $\overline{RESET}$ is guaranteed to be a logic low for V_{CC} down to 1V. Once V_{CC} exceeds the reset threshold, an internal timer keeps $\overline{RESET}$ low for the specified reset timeout period (t_{RP}); after this interval, $\overline{RESET}$ returns high (Figure 2).

If a brownout condition occurs (V_{CC} dips below the reset threshold), $\overline{RESET}$ goes low. Each time $\overline{RESET}$ is asserted it stays low for the reset timeout period. Any time V_{CC} goes below the reset threshold the internal timer restarts. $\overline{RESET}$ both sources and sinks current. RESET on the MAX824/MAX825 is the inverse of $\overline{RESET}$.

Manual-Reset Input (MAX823/MAX825)

Many µP-based products require manual-reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. On the MAX823/MAX825, a logic low on $\overline{MR}$ asserts reset. Reset remains asserted while $\overline{MR}$ is low, and for t_{RP} (200ms nominal) after it returns high. $\overline{MR}$ has an internal 52kΩ pull-up resistor, so it can be left open if not used. This input can be driven with CMOS-logic levels or with open-drain/collector outputs. Connect a normally open momentary switch from $\overline{MR}$ to GND to create a manual-reset function; external debounce circuitry is not required. If $\overline{MR}$ is driven from long cables or the device is used in a noisy environment, connect a 0.1µF capacitor from $\overline{MR}$ to GND to provide additional noise immunity.

Watchdog Input (MAX823/MAX824)

In the MAX823/MAX824, the watchdog circuit monitors the µP's activity. If the µP does not toggle the watchdog input (WDI) within t_{WD} (1.6sec), reset asserts. The internal 1.6sec timer is cleared by either a reset pulse or by toggling WDI, which detects pulses as short as 50ns. While reset is asserted, the timer remains cleared and does not count. As soon as reset is released, the timer starts counting (Figure 3).

Disable the watchdog function by leaving WDI unconnected or by three-stating the driver connected to WDI. The watchdog input is internally driven low during the first 7/8 of the watchdog timeout period and high for the last 1/8 of the watchdog timeout period. When WDI is left unconnected, this internal driver clears the 1.6sec timer every 1.4sec. When WDI is three-stated or unconnected, the maximum allowable leakage current is 10µA and the maximum allowable load capacitance is 200pF.

Applications Information

Watchdog Input Current

The MAX823/MAX824 WDI inputs are internally driven through a buffer and series resistor from the watchdog counter (Figure 1). When WDI is left unconnected, the watchdog timer is serviced within the watchdog timeout period by a low-high-low pulse from the counter chain. For minimum watchdog input current (minimum overall power consumption), leave WDI low for the majority of the watchdog timeout period, pulsing it low-high-low once within the first 7/8 of the watchdog timeout period to reset the watchdog timer. If WDI is externally driven high for the majority of the timeout period, up to 160µA can flow into WDI.

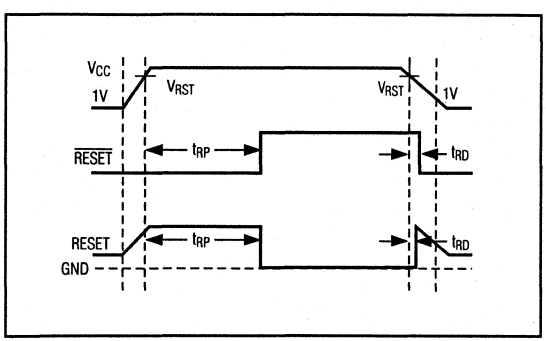


Figure 2. Reset Timing Diagram

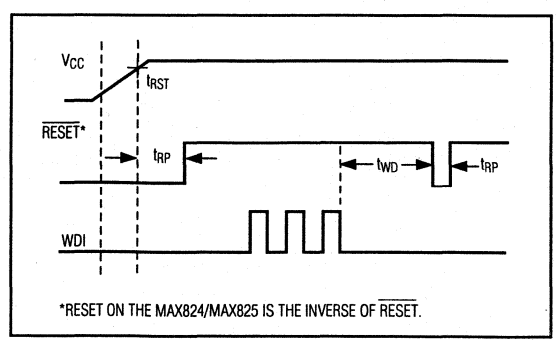


Figure 3. MAX823/MAX824 Watchdog Timing Relationship

Interfacing to µPs with Bidirectional Reset Pins

The $\overline{\text{RESET}}$ output maximum pull-up current is 800µA for L/M versions (400µA for T/S/R versions). This allows µPs with bidirectional resets, such as the 68HC11, to force $\overline{\text{RESET}}$ low when the MAX823/MAX824/MAX825 are pulling $\overline{\text{RESET}}$ high (Figure 4).

Negative-Going V_{CC} Transients

These supervisors are relatively immune to short-duration, negative-going V_{CC} transients (glitches), which usually do not require the entire system to shut down. Resets are issued to the µP during power-up, power-down, and brownout conditions.

The *Typical Operating Characteristics* show a graph of the MAX823L's Maximum V_{CC} Transient Duration vs. Reset Threshold Overdrive, for which reset pulses are **not** generated. The graph was produced using negative-going V_{CC} pulses, starting at 5V and ending below the reset threshold by the magnitude indicated (reset threshold overdrive). The graph shows the maximum pulse width that a negative-going V_{CC} transient can typically have without triggering a reset pulse. As the amplitude of the transient increases (i.e., goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a V_{CC} transient that goes 100mV below the reset threshold and lasts for 15µs or less will not trigger a reset pulse.

An optional 0.1µF bypass capacitor mounted close to V_{CC} provides additional transient immunity.

Watchdog Software Considerations (MAX823/MAX824)

One way to help the watchdog timer monitor software execution more closely is to set and reset the watchdog input at different points in the program, rather than pulsing the watchdog input high-low-high or low-high-low. This technique avoids a stuck loop, in which the watchdog timer would continue to be reset inside the loop, keeping the watchdog from timing out.

Figure 5 shows an example of a flow diagram where the I/O driving the watchdog input is set high at the beginning of the program, set low at the beginning of every subroutine or loop, then set high again when the program returns to the beginning. If the program should hang in any subroutine, the problem would quickly be corrected, since the I/O is continually set low and the watchdog timer is allowed to time out, causing a reset or interrupt to be issued. As described in the *Watchdog Input Current* section, this scheme results in higher time average WDI input current than does leaving WDI low for the majority of the timeout period and periodically pulsing it low-high-low.

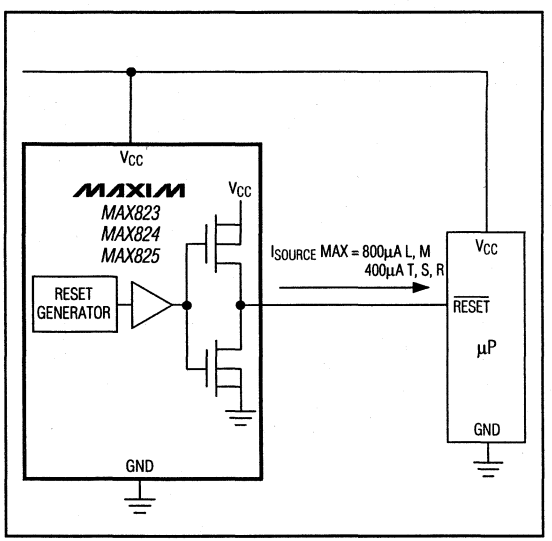


Figure 4. Interfacing to µPs with Bidirectional Resets

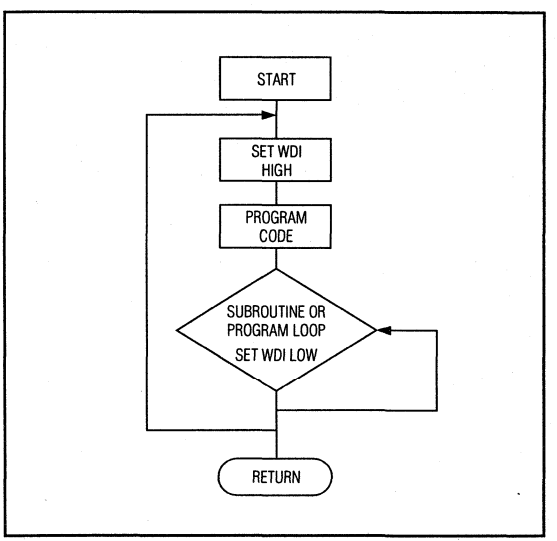
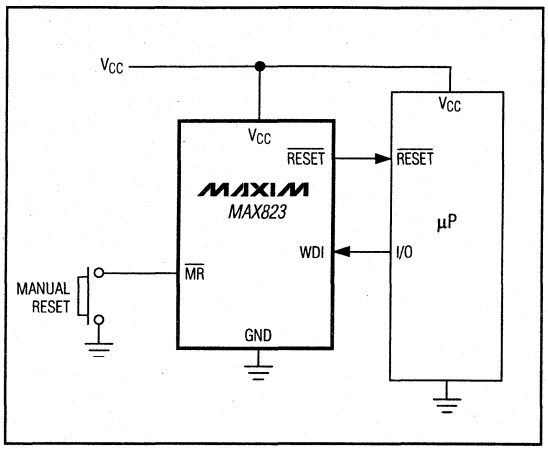


Figure 5. Watchdog Flow Diagram

5-Pin Microprocessor Supervisory Circuits

Typical Operating Circuit



Chip Information

TRANSISTOR COUNT: 607

19-1078; Rev 0; 6/96

MAXIM

+5V, Low-Power µP Supervisory Circuits with Adjustable Reset/Watchdog

General Description

The MAX6301/MAX6302/MAX6303/MAX6304* low-power microprocessor (µP) supervisory circuits provide maximum adjustability for reset and watchdog functions. The reset threshold can be adjusted to any voltage above 1.22V, using external resistors. In addition, the reset and watchdog timeout periods are adjustable using external capacitors. A watchdog select pin extends the watchdog timeout period to 500x. The reset function features immunity to power-supply transients.

These four devices differ only in the structure of their reset outputs (see *Selector Guide*). The MAX6301–MAX6304 are available in the space-saving 8-pin µMAX package, as well as 8-pin DIP/SO.

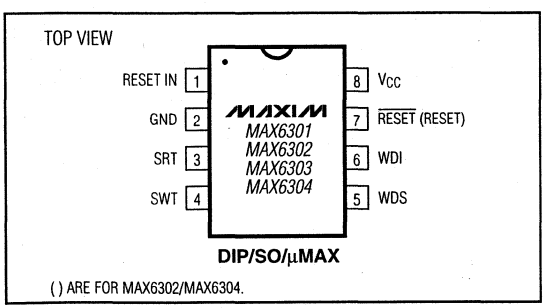
Applications

Medical Equipment	Embedded Controllers
Intelligent Instruments	Critical µP Monitoring
Portable Equipment	Set-Top Boxes
Battery-Powered Computers/Controllers	Computers

Selector Guide

FEATURE	MAX6301	MAX6302	MAX6303	MAX6304
Active-Low Reset	✓	—	✓	—
Active-High Reset	—	✓	—	✓
Open-Drain Reset Output	✓	✓	—	—
Push/Pull Reset Output	—	—	✓	✓
Pins-Package	8-DIP/SO/ µMAX	8-DIP/SO/ µMAX	8-DIP/SO/ µMAX	8-DIP/SO/ µMAX

Pin Configuration



* Patents pending

Features

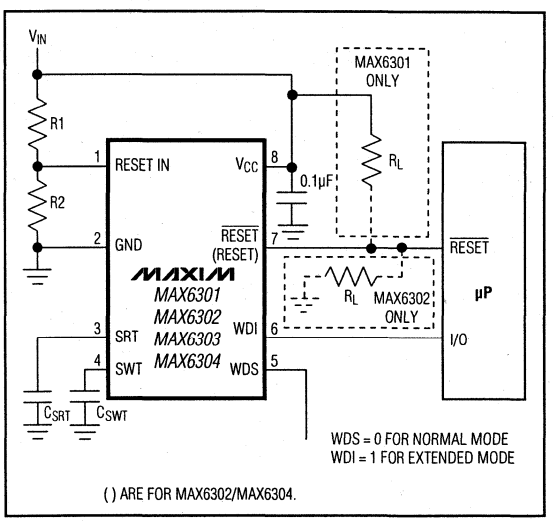
- ♦ **Adjustable Reset Threshold**
- ♦ **Adjustable Reset Timeout**
- ♦ **Adjustable Watchdog Timeout**
- ♦ **500x Watchdog Timeout Multiplier**
- ♦ **4µA Supply Current**
- ♦ **RESET or $\overline{\text{RESET}}$ Output Options**
- ♦ **Push/Pull or Open-Drain Output Options**
- ♦ **Guaranteed $\overline{\text{RESET}}$ Asserted At or Above V_{CC} = 1V (MAX6301/MAX6303)**
- ♦ **Power-Supply Transient Immunity**
- ♦ **Watchdog Function Can Be Disabled**
- ♦ **DIP/SO/µMAX Packages Available**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX6301CPA	0°C to +70°C	8 Plastic DIP
MAX6301CSA	0°C to +70°C	8 SO
MAX6301CUA	0°C to +70°C	8 µMAX
MAX6301EPA	-40°C to +85°C	8 Plastic DIP
MAX6301ESA	-40°C to +85°C	8 SO

Ordering Information continued at end of data sheet.

Typical Operating Circuit



5

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+5V, Low-Power µP Supervisory Circuits with Adjustable Reset/Watchdog

ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... -0.3V to +7.0V
RESET IN, SWT, SRT ..... -0.3V to (V_{CC} + 0.3V)
WDI, WDS ..... -0.3V to (V_{CC} + 0.3V)
RESET, $\overline{RESET}$
  MAX6301 ..... -0.3V to +7.0V
  MAX6302/6303/6304 ..... -0.3V to (V_{CC} + 0.3V)
Input Current
  V_{CC} ..... ±20mA
  GND ..... ±20mA
Output Current
  RESET, $\overline{RESET}$ ..... ±20mA

Continuous Power Dissipation (T_A = +70°C)
  Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
  SO (derate 5.88mW/°C above +70°C) 471mW
  µMAX (derate 4.10mW/°C above +70°C) 330mW
Operating Temperature Ranges
  MAX630_C_A ..... 0°C to +70°C
  MAX630_E_A ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range (Note 1)	V_{CC}	MAX6301C/MAX6303C	1.00		5.50	V
		MAX6301E/MAX6303E	1.20		5.50	
		MAX6302/MAX6304	1.31		5.50	
Supply Current (Note 2)	I_{CC}	No load		4.0	7.0	µA
RESET TIMER						
Reset Input Threshold Voltage	V_{TH}	$V_{RESET\ IN}$ falling, V_{CC} = 5.0V	1.195	1.220	1.245	V
		$V_{RESET\ IN}$ rising, V_{CC} = 5.0V		1.240	1.265	
Reset Input Hysteresis	V_{HYST}			20		mV
Reset Input Leakage Current	$I_{RESET\ IN}$			±0.01	±1	nA
Reset Output Voltage High (MAX6302/MAX6303/MAX6304)	V_{OH}	V_{CC} ≥ 4.5V, I_{SOURCE} = 0.8mA	V_{CC} - 0.4			V
		V_{CC} = 2V, I_{SOURCE} = 0.4mA	VCC - 0.4			
		MAX6302/MAX6304, V_{CC} = 1.31V, R_L = 10kΩ	V_{CC} - 0.3			
Reset Output Voltage Low (MAX6301/MAX6303/MAX6304)	V_{OL}	V_{CC} ≥ 4.5V, I_{SINK} = 3.2mA			0.4	V
		V_{CC} = 2V, I_{SINK} = 1.6mA			0.4	
		MAX6301/MAX6303: V_{CC} = 1V, I_{SINK} = 50µA, T_A = 0°C to +70°C			0.3	
		MAX6301/MAX6303: V_{CC} = 1.2V, I_{SINK} = 100µA, T_A = -40°C to +85°C			0.3	
V_{CC} to Reset Delay	t_{RD}	V_{CC} falling at 1mV/µs		63		µs
Reset Input Pulse Width	t_{RI}	Comparator overdrive = 50mV		26		µs
Reset Timeout Period (Note 3)	t_{RP}	C_{SRT} = 1500pF	2.8	4.0	5.2	ms
Reset Output Leakage Current		MAX6301, $V_{\overline{RESET}}$ = V_{CC}			±1	µA
		MAX6302, V_{RESET} = GND			±1	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V and T_A = +25°C.)

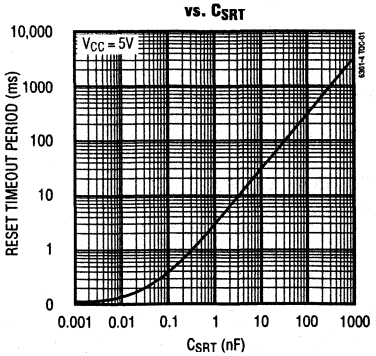
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
WATCHDOG TIMER						
WDI, WDS Input Threshold	V_{IH}		0.7V_{CC}			V
	V_{IL}				0.3V_{CC}	
WDI Pulse Width	t_{WP}	V_{CC} = 4.5V to 5.5V	30			ns
		V_{CC} = 2V to 4.5V	60			
WDI, WDS Leakage Current		Extended mode disabled			±1	µA
WDI Sink/Source Current (Note 4)		Extended mode enabled		±70		µA
Watchdog Timeout Period (Note 3)	t_{WD}	WDS = GND, C_{SWT} = 1500pF	2.8	4.0	5.2	ms
		WDS = V_{CC}, C_{SWT} = 1500pF	1.4	2.0	2.6	sec

Note 1: Reset is guaranteed valid from the selected reset threshold voltage down to the minimum V_{CC}.
Note 2: VDS = V_{CC}, WDI unconnected.
Note 3: Precision timing currents of 500nA are present at both the SRT and SWT pins. Timing capacitors connected to these nodes must have low leakage consistent with these currents to prevent timing errors.
Note 4: The sink/source is supplied through a resistor, and is proportional to V_{CC} (Figure 8). At V_{CC} = 2V, it is typically ±24µA.

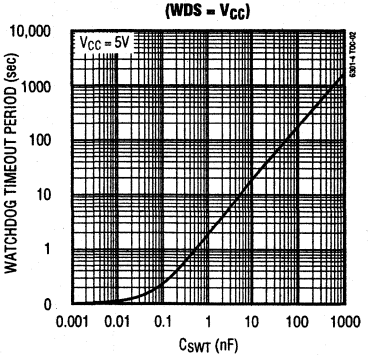
Typical Operating Characteristics

(C_{SWT} = C_{SRT} = 1500pF, T_A = +25°C, unless otherwise noted.)

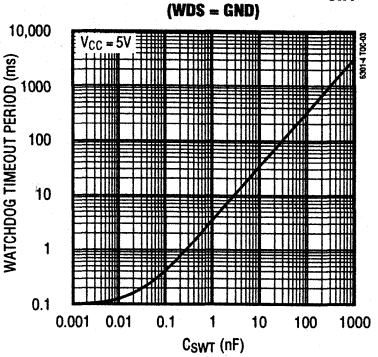
RESET TIMEOUT PERIOD vs. C_{SRT}



EXTENDED-MODE WATCHDOG TIMEOUT PERIOD vs. C_{SWT} (WDS = V_{CC})



NORMAL-MODE WATCHDOG TIMEOUT PERIOD vs. C_{SWT} (WDS = GND)

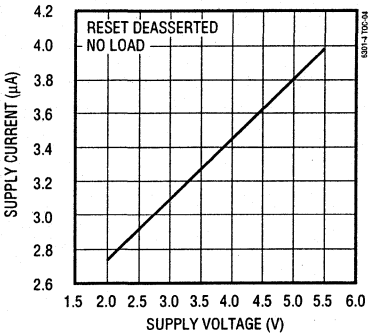


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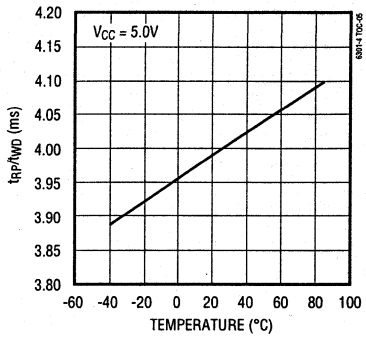
Typical Operating Characteristics (continued)

(C_{SWT} = C_{SRT} = 1500pF, T_A = +25°C, unless otherwise noted.)

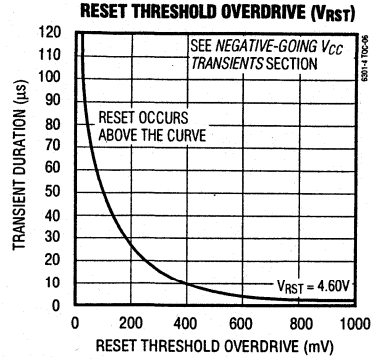
SUPPLY CURRENT vs. SUPPLY VOLTAGE



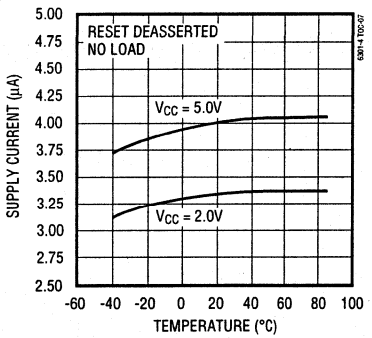
RESET AND NORMAL-MODE WATCHDOG TIMEOUT PERIOD vs. TEMPERATURE



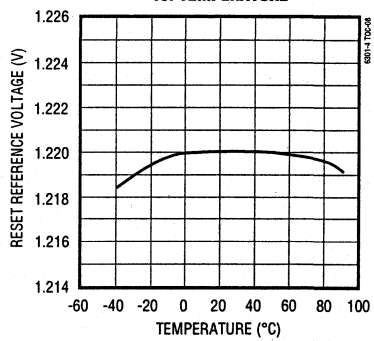
MAXIMUM TRANSIENT DURATION vs. RESET THRESHOLD OVERDRIVE (V_{RST})



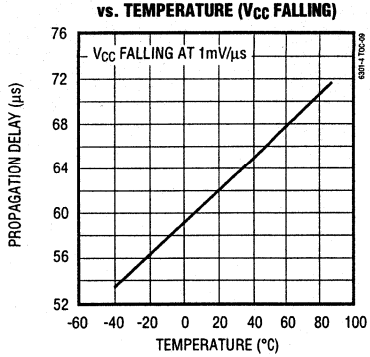
SUPPLY CURRENT vs. TEMPERATURE



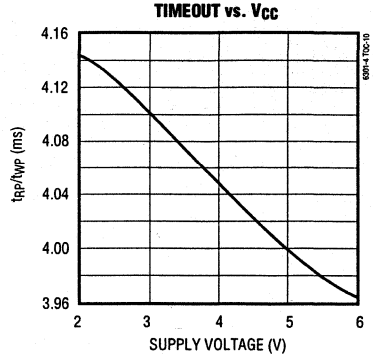
RESET IN THRESHOLD VOLTAGE vs. TEMPERATURE



V_{CC} TO RESET DELAY vs. TEMPERATURE (V_{CC} FALLING)



RESET AND WATCHDOG TIMEOUT vs. V_{CC}



Pin Description

PIN	NAME	FUNCTION	
1	RESET IN	Reset Input. High-impedance input to the reset comparator. Connect this pin to the center point of an external resistor voltage-divider network to set the reset threshold voltage. The reset threshold voltage is calculated as follows: V_{RST} = 1.22 x (R1 + R2) / R2 (see *Typical Operating Circuit*).	
2	GND	Ground	
3	SRT	Set Reset-Timeout Input. Connect a capacitor between this input and ground to select the reset timeout period (t_{RS}). Determine the period as follows: t_{RP} = 2.67 x C_{SRT}, with C_{SRT} in pF and t_{RP} in µs (see *Typical Operating Circuit*).	
4	SWT	Set Watchdog-Timeout Input. Connect a capacitor between this input and ground to select the basic watchdog timeout period (t_{WD}). Determine the period as follows: t_{WD} = 2.67 x C_{SWT}, with C_{SWT} in pF and t_{WD} in µs. The watchdog function can be disabled by connecting this pin to ground.	
5	WDS	Watchdog-Select Input. This input selects the watchdog mode. Connect to ground to select normal mode and the basic watchdog timeout period. Connect to V_{CC} to select extended mode, multiplying the basic timeout period by a factor of 500. A change in the state of this pin resets the watchdog timer to zero.	
6	WDI	Watchdog Input. A rising or falling transition must occur on this input within the selected watchdog timeout period, or a reset pulse will occur. The capacitor value selected for SWT and the state of WDS determine the watchdog timeout period. The watchdog timer clears and restarts when a transition occurs on WDI or WDS. The watchdog timer is cleared when reset is asserted and restarted after reset deasserts. In the extended watchdog mode (WDS = V_{CC}), the watchdog function can be disabled by driving WDI with a three-stated driver or by leaving WDI unconnected.	
7	$\overline{\text{RESET}}$ (MAX6301/3)	Open-Drain, Active-Low Reset Output (MAX6301)	$\overline{\text{RESET}}$ changes from high to low whenever the monitored voltage (V_{IN}) drops below the selected reset threshold (V_{RST}). $\overline{\text{RESET}}$ remains low as long as V_{IN} is below V_{RST}. Once V_{IN} exceeds V_{RST}, $\overline{\text{RESET}}$ remains low for the reset timeout period and then goes high. The watchdog timer triggers a reset pulse (t_{RP}) whenever the watchdog timeout period (t_{WD}) is exceeded.
		Push/Pull, Active-Low Reset Output (MAX6303)	
	RESET (MAX6302/4)	Open-Drain, Active-High Reset Output (MAX6302)	RESET changes from low to high whenever the monitored voltage (V_{IN}) drops below the selected reset threshold (V_{RST}). RESET remains high as long as V_{IN} is below V_{RST}. Once V_{IN} exceeds V_{RST}, RESET remains high for the reset timeout period and then goes low. The watchdog timer triggers a reset pulse (t_{RP}) whenever the watchdog timeout period (t_{WD}) is exceeded.
		Push/Pull, Active-High Reset Output (MAX6304)	
8	V_{CC}	Supply Voltage	

+5V, Low-Power µP Supervisory Circuits with Adjustable Reset/Watchdog

Detailed Description

Reset Function/Output

The reset output is typically connected to the reset input of a microprocessor (µP). A µP's reset input starts or restarts the µP in a known state. The MAX6301–MAX6304 µP supervisory circuits provide the reset logic to prevent code-execution errors during power-up, power-down, and brownout conditions (see *Typical Operating Circuit*).

For the MAX6301/MAX6303, $\overline{RESET}$ changes from high to low whenever the monitored voltage (V_{IN}) drops below the reset threshold voltage (V_{RST}). $\overline{RESET}$ remains low as long as V_{IN} is below V_{RST}. Once V_{IN} exceeds V_{RST}, $\overline{RESET}$ remains low for the reset timeout period, then goes high. When a reset is asserted due to a watchdog timeout condition, $\overline{RESET}$ stays low for the reset timeout period. Anytime reset asserts, the watchdog timer clears. At the end of the reset timeout period, $\overline{RESET}$ goes high and the watchdog timer is restarted from zero. If the watchdog timeout period is exceeded again, then $\overline{RESET}$ goes low again. This cycle continues unless WDI receives a transition.

On power-up, once V_{CC} reaches 1V, $\overline{RESET}$ is guaranteed to be a logic low. For information about applications where V_{CC} is less than 1V, see the section *Ensuring a Valid $\overline{RESET}$/RESET Output Down to V_{CC} = 0V (MAX6303/MAX6304)*. As V_{CC} rises, $\overline{RESET}$ remains low. When V_{IN} rises above V_{RST}, the reset timer starts and $\overline{RESET}$ remains low. When the reset timeout period ends, $\overline{RESET}$ goes high.

On power-down, once V_{IN} goes below V_{RST}, $\overline{RESET}$ goes low and is guaranteed to be low until V_{CC} droops below 1V. For information about applications where V_{CC} is less than 1V, see the section *Ensuring a Valid $\overline{RESET}$/RESET Output Down to V_{CC} = 0V (MAX6303/MAX6304)*.

The MAX6302/MAX6304 active-high RESET output is the inverse of the MAX6301/MAX6303 active-low $\overline{RESET}$ output, and is guaranteed valid for V_{CC} > 1.31V.

Reset Threshold

These supervisors monitor the voltage on RESET IN. The MAX6301–MAX6304 have an adjustable reset threshold voltage (V_{RST}) set with an external resistor voltage divider (Figure 1). Use the following formula to calculate V_{RST} (the point at which the monitored voltage triggers a reset):

$$V_{RST} = \frac{V_{TH} \times (R1 + R2)}{R2} \ (V)$$

where V_{RST} is the desired reset threshold voltage and V_{TH} is the reset input threshold (1.22V). Resistors R1 and R2 can have very high values to minimize current consumption. Set R2 to some conveniently high value (1MΩ, for example) and calculate R1 based on the desired reset threshold voltage, using the following formula:

$$R1 = R2 \times \left(\frac{V_{RST}}{V_{TH}} - 1 \right) \ (\Omega)$$

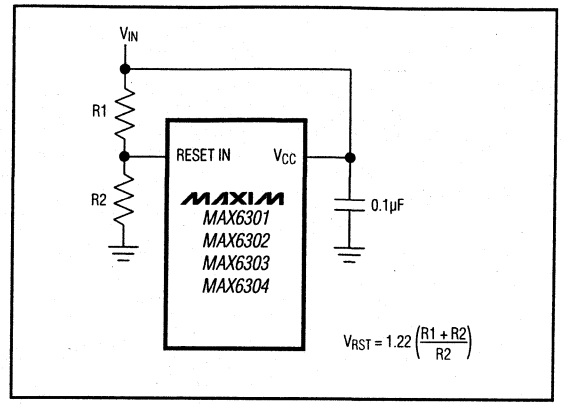


Figure 1. Calculating the Reset Threshold Voltage (V_{RST})

Watchdog Timer

The watchdog circuit monitors the µP's activity. If the µP does not toggle the watchdog input (WDI) within t_{WD} (user selected), reset asserts. The internal watchdog timer is cleared by reset, by a transition at WDI (which can detect pulses as short as 30ns), or by a transition at WDS. The watchdog timer remains cleared while reset is asserted; as soon as reset is released, the timer starts counting (Figure 2).

The MAX6301–MAX6304 feature two modes of watchdog timer operation: normal mode and extended mode. In normal mode (WDS = GND), the watchdog timeout period is determined by the value of the capacitor connected between SWT and ground (see the section *Selecting the Reset and Watchdog Timeout Capacitor*). In extended mode (WDS = V_{CC}), the watchdog timeout period is multiplied by 500. For example, in the extended mode, a 1µF capacitor gives a watchdog timeout period of 22 minutes (see the graph Extended-Mode Watchdog Timeout Period vs. C_{SWT} in the *Typical Operating Characteristics*).

In extended mode, the watchdog function can be disabled by leaving WDI unconnected or by three-stating the driver connected to WDI. In this mode, the watchdog input is internally driven low during the watchdog

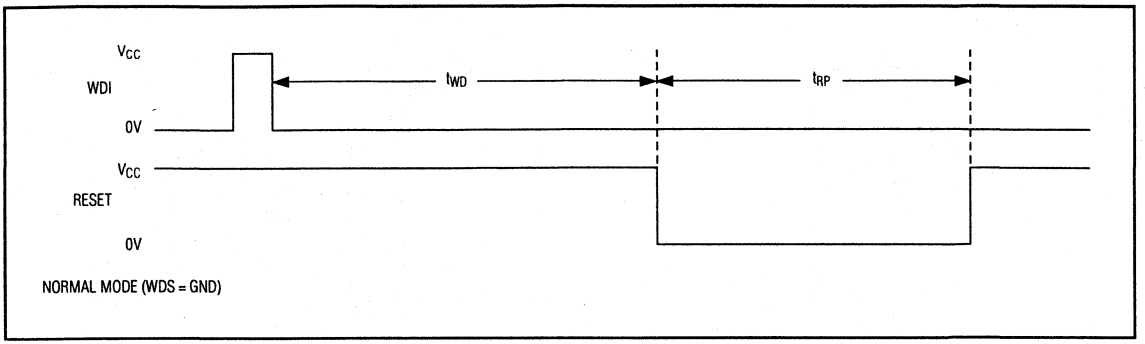


Figure 2a. Watchdog Timing Diagram, WDS = GND

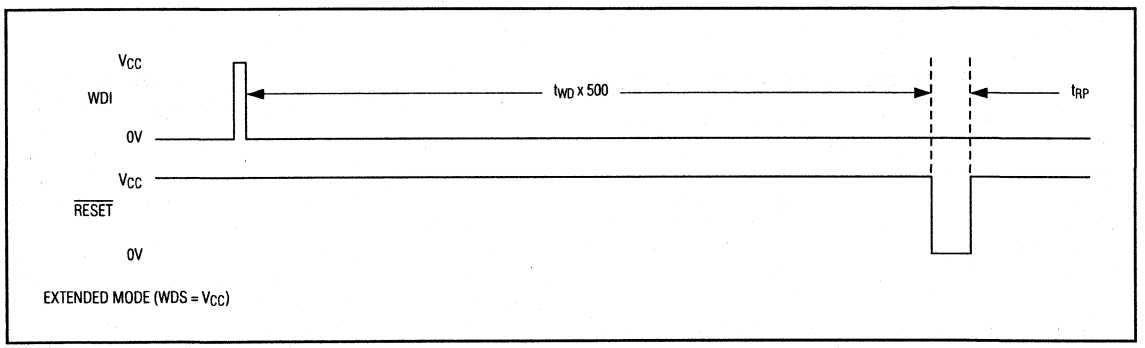


Figure 2b. Watchdog Timing Diagram, WDS = V_{CC}

timeout period, then momentarily pulses high, resetting the watchdog counter. When WDI is left unconnected, the watchdog timer is cleared by this internal driver just before the timeout period is reached (the internal driver pulls WDI high at about 94% of t_{WD}). When WDI is three-stated, the maximum allowable leakage current of the device driving WDI is 10µA.

In normal mode (WDS = GND), the watchdog timer cannot be disabled by three-stating WDI. WDI is a high-impedance input in this mode. Do not leave WDI unconnected in normal mode.

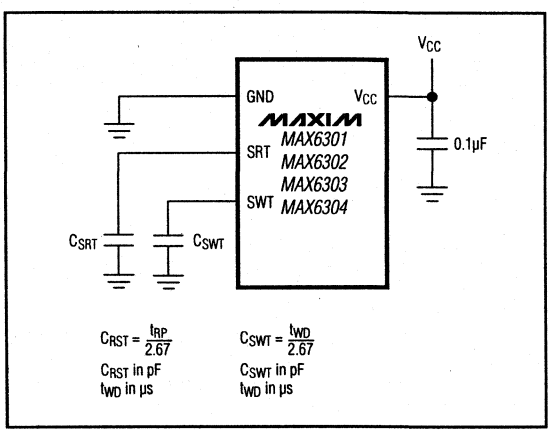


Figure 3. Calculating the Reset (C_{SRT}) and Watchdog (C_{SWT}) Timeout Capacitor Values

+5V, Low-Power µP Supervisory Circuits with Adjustable Reset/Watchdog

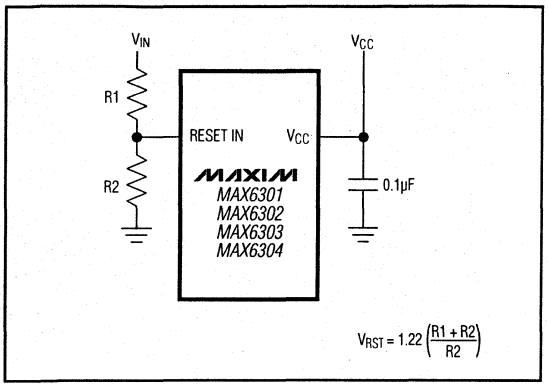


Figure 4. Monitoring a Voltage Other than VCC

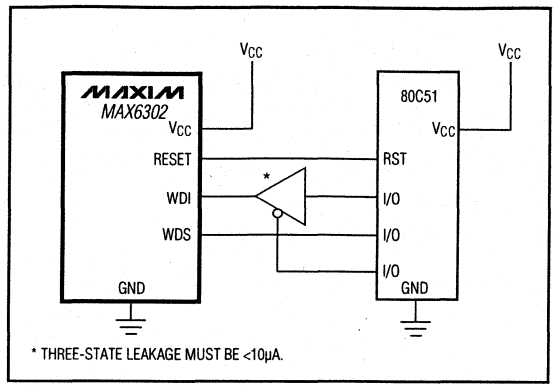


Figure 5. Wake-Up Timer

Applications Information

Selecting the Reset and Watchdog Timeout Capacitor

The reset timeout period is adjustable to accommodate a variety of µP applications. Adjust the reset timeout period (t_{RS}) by connecting a specific value capacitor (C_{SRT}) between SRT and ground (Figure 3). Calculate the reset timeout capacitor as follows:

$$C_{SRT} = t_{RP} / 2.67$$

with C_{SRT} in pF and t_{RP} in µs. C_{SRT} must be a low-leakage (<10nA) type capacitor. Ceramic is recommended.

The watchdog timeout period is adjustable to accommodate a variety of µP applications. With this feature, the watchdog timeout can be optimized for software execution. The programmer can determine how often the watchdog timer should be serviced. Adjust the watchdog timeout period (t_{WD}) by connecting a specific value capacitor (C_{SWT}) between SWT and ground (Figure 3). For normal-mode operation, calculate the watchdog timeout capacitor as follows:

$$C_{SWT} = t_{WD} / 2.67$$

where C_{SWT} is in pF and t_{WD} is in µs. C_{SRT} must be a low leakage (<10nA) type capacitor. Ceramic is recommended.

Monitoring Voltages Other than VCC

The *Typical Operating Circuit* monitors V_{CC}. However, monitoring other voltages is simple, and Figure 4 shows a circuit that accomplishes this. Calculate V_{RST} as shown in the *Reset Threshold* section.

Wake-Up Timer

In some applications, it is advantageous to put a µP into sleep mode, periodically "wake it up" to perform checks and/or tasks, then put it back into sleep mode. The MAX6301 family supervisors can easily accommodate this technique. Figure 5 illustrates an example using the MAX6302 and an 80C51.

In Figure 5, just before the µC puts itself into sleep mode, it pulls WDS high. The µC's I/O pins maintain their logic levels while in sleep mode and WDS remains high. This places the MAX6302 in extended mode, increasing the watchdog timeout 500 times. When the watchdog timeout period ends, a reset is applied on the 80C51, "waking it up" to perform tasks. While the µP is performing tasks, the 80C51 pulls WDS low (selecting normal mode), and the MAX6302 monitors the µP for hang-ups. When the µP finishes its tasks, it puts itself back into sleep mode, drives WDS high, and starts the cycle over again. This is a power-saving technique, since the µP is operating only part of the time and the MAX6302 has very low quiescent current.

Adding a Manual Reset Function

A manual reset option can easily be implemented by connecting a normally open momentary switch in parallel with R2 (Figure 6). When the switch is closed, the voltage on RESET IN goes to zero, initiating a reset. When the switch is released, reset remains asserted for the reset timeout period and then is cleared. The pushbutton switch is effectively debounced by the reset timer.

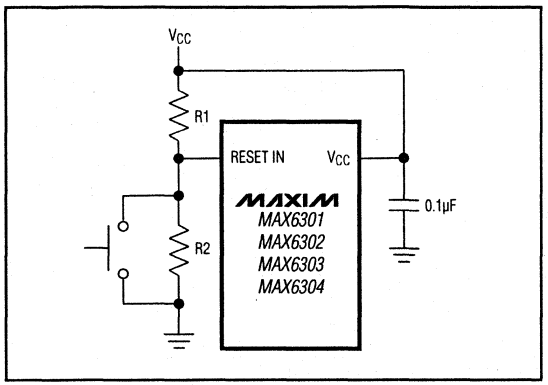


Figure 6. Adding a Manual Reset Function

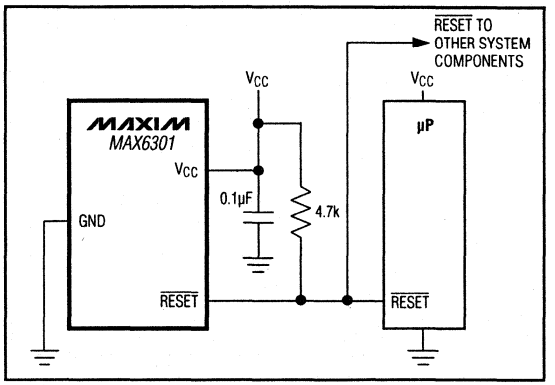


Figure 7. Interfacing to µPs with Bidirectional Reset I/O Pins

Interfacing to µPs with Bidirectional Reset Pins

Since $\overline{\text{RESET}}$ is open-drain, the MAX6301 interfaces easily with µPs that have bidirectional reset pins, such as the Motorola 68HC11 (Figure 7). Connecting $\overline{\text{RESET}}$ directly to the µP's reset pin with a single pull-up allows either device to assert reset.

Negative-Going V_{CC} Transients

In addition to issuing a reset to the µP during power-up, power-down, and brownout conditions, these supervisors are relatively immune to short-duration negative-going transients (glitches). The graph Maximum Transient Duration vs. Reset Threshold Overdrive in the *Typical Operating Characteristics* shows this relationship.

The area below the curves of the graph is the region in which these devices typically do not generate a reset pulse. This graph was generated using a negative-going pulse applied to V_{IN}, starting above the actual reset threshold (V_{RST}) and ending below it by the magnitude indicated (reset-threshold overdrive). As the magnitude of the transient increases (farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a V_{CC} transient that goes 100mV below the reset threshold and lasts 50µs or less will not cause a reset pulse to be issued.

Watchdog Input Current

Extended Mode

In extended mode (WDS = V_{CC}), the WDI input is internally driven through a buffer and series resistor from the watchdog counter (Figure 8). When WDI is left unconnected, the watchdog timer is serviced within the watchdog timeout period by a very brief low-high-low pulse from the counter chain. For minimum watchdog input current (minimum overall power consumption), leave WDI low for the majority of the watchdog timeout period, pulsing it low-high-low (>30ns) once within the period to reset the watchdog timer. If instead WDI is externally driven high for the majority of the timeout period, typically 70µA can flow into WDI.

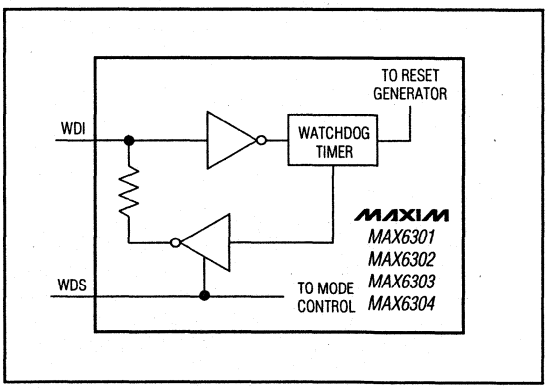


Figure 8. Watchdog Input Structure

Normal Mode

In normal mode (WDS = GND), the internal buffer that drives WDI is disabled. In this mode, WDI is a standard CMOS input and leakage current is typically 100pA, regardless of whether WDI is high or low.

+5V, Low-Power µP Supervisory Circuits with Adjustable Reset/Watchdog

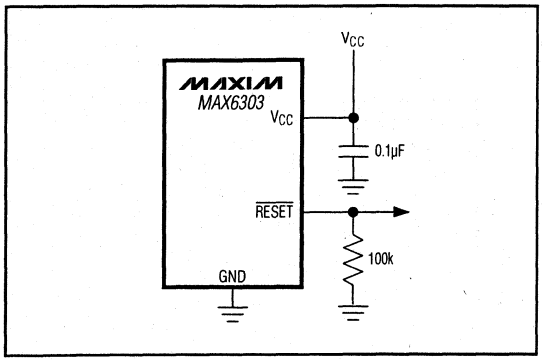


Figure 9. Ensuring $\overline{RESET}$ Valid to V_{CC} = 0V

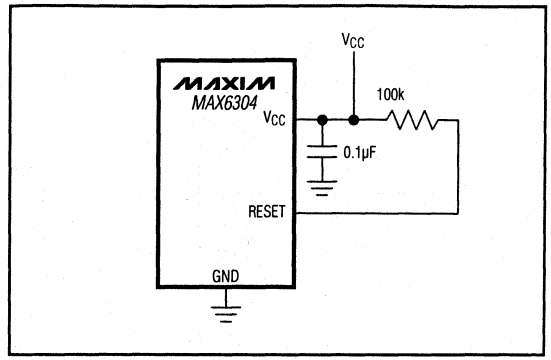


Figure 10. Ensuring RESET Valid to V_{CC} = 0V

Ensuring a Valid $\overline{RESET}$/RESET Output Down to V_{CC} = 0V (MAX6303/MAX6304)

When V_{CC} falls below 1V, $\overline{RESET}$/RESET current sinking (sourcing) capabilities decline drastically. In the case of the MAX6303, high-impedance CMOS-logic inputs connected to $\overline{RESET}$ can drift to undetermined voltages. This presents no problem in most applications, since most µPs and other circuitry do not operate with V_{CC} below 1V.

In those applications where $\overline{RESET}$ must be valid down to 0V, adding a pull-down resistor between $\overline{RESET}$ and ground sinks any stray leakage currents, holding $\overline{RESET}$ low (Figure 9). The value of the pull-down resistor is not critical; 100kΩ is large enough not to load $\overline{RESET}$ and small enough to pull $\overline{RESET}$ to ground. For applications using the MAX6304, a 100kΩ pull-up resistor between RESET and V_{CC} will hold RESET high when V_{CC} falls below 1V (Figure 10).

Watchdog-Software Considerations

To help the watchdog timer monitor software execution more closely, set and reset the watchdog input at different points in the program, rather than "pulsing" the watchdog input high-low-high or low-high-low. This technique avoids a "stuck" loop in which the watchdog timer would continue to be reset within the loop, keeping the watchdog from timing out.

Figure 11 shows an example of a flow diagram where the I/O driving the watchdog input is set high at the beginning of the program, set low at the beginning of every subroutine or loop, then set high again when the program returns to the beginning. If the program should "hang" in any subroutine the problem would quickly be corrected, since the I/O is continually set low and the watchdog timer is allowed to time out, causing a reset or interrupt to be issued. When using extended mode, as described in the *Watchdog Input Current* section, this scheme does result in higher average WDI input current than does the method of leaving WDI low for the majority of the timeout period and periodically pulsing it low-high-low.

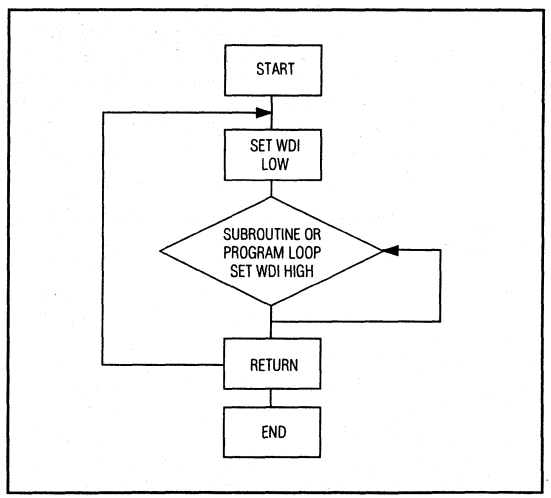


Figure 11. Watchdog Flow Diagram

Layout Considerations

SRT and SWT are precision current sources. When developing the layout for the application, be careful to minimize board capacitance and leakage currents around these pins. Traces connected to these pins should be kept as short as possible. Traces carrying high-speed digital signals and traces with large voltage potentials should be routed as far from these pins as possible. Leakage currents and stray capacitance (e.g., a scope probe) at these pins could cause errors in the reset and/or watchdog timeout period. When evaluating these parts, use clean prototype boards to ensure accurate reset and watchdog timeout periods.

RESET IN is a high-impedance input which is typically driven by a high-impedance resistor-divider network (e.g., 1MΩ to 10MΩ). Minimize coupling to transient signals by keeping the connections to this input short. Any DC leakage current at RESET IN (e.g., a scope probe) causes errors in the programmed reset threshold. Note that sensitive pins are located on the GND side of the device, away from the digital I/O, to simplify board layout.

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX6302CPA	0°C to +70°C	8 Plastic DIP
MAX6302CSA	0°C to +70°C	8 SO
MAX6302CUA	0°C to +70°C	8 µMAX
MAX6302EPA	-40°C to +85°C	8 Plastic DIP
MAX6302ESA	-40°C to +85°C	8 SO
MAX6303CPA	0°C to +70°C	8 Plastic DIP
MAX6303CSA	0°C to +70°C	8 SO
MAX6303CUA	0°C to +70°C	8 µMAX
MAX6303EPA	-40°C to +85°C	8 Plastic DIP
MAX6303ESA	-40°C to +85°C	8 SO
MAX6304CPA	0°C to +70°C	8 Plastic DIP
MAX6304CSA	0°C to +70°C	8 SO
MAX6304CUA	0°C to +70°C	8 µMAX
MAX6304EPA	-40°C to +85°C	8 Plastic DIP
MAX6304ESA	-40°C to +85°C	8 SO

Chip Information

TRANSISTOR COUNT: 580

19-1145; Rev 0; 9/96

MAXIM

5-Pin, Multiple-Input, Programmable Reset ICs

General Description

The MAX6305–MAX6313 CMOS microprocessor (µP) supervisory circuits are designed to monitor more than one power supply. Ideal for monitoring both 5V and 3.3V in personal computer systems, these devices assert a system reset if any of the monitored supplies falls outside the programmed threshold. Low supply current (15µA) and a small package suit them for portable applications. The MAX6305–MAX6313 are specifically designed to ignore fast transients on any monitored supply.

These devices are available in a SOT23-5 package, have factory-programmed reset thresholds from 2.5V to 5.0V (in 100mV increments), and feature four power-on reset timeout periods.

Applications

Portable Computers

Computers

Controllers

Intelligent Instruments

Portable/Battery-Powered Equipment

Multivoltage Systems: 3V/5V, 5V/12V, 5V/24V

Embedded Control Systems

Pin Configurations and Typical Operating Circuit appear at end of data sheet.

Features

- ♦ **Small 5-Pin SOT23 Package**
- ♦ **Precision Factory-Set V_{CC} Reset Thresholds; Available in 0.1V Increments from 2.5V to 5V**
- ♦ **Immune to Short V_{CC} Transients**
- ♦ **Guaranteed $\overline{RESET}$ Valid to V_{CC} = 1V**
- ♦ **Guaranteed Over Temperature**
- ♦ **8µA Supply Current**
- ♦ **Factory-Set Reset Timeout Delay from 1ms (min) to 1120ms (min)**
- ♦ **No External Components**
- ♦ **Manual Reset Input**
- ♦ **Under/Overvoltage Supply Monitoring**

Ordering Information

PART†	TEMP. RANGE	PIN-PACKAGE
MAX6305UK00D_-T	0°C to +70°C	5 SOT23-5
MAX6306UK_ _D_-T	0°C to +70°C	5 SOT23-5
MAX6307UK_ _D_-T	0°C to +70°C	5 SOT23-5

† *The MAX6306/MAX6307/MAX6309/MAX6310/MAX6312/MAX6313 are available with factory-set V_{CC} reset thresholds from 2.5V to 5V, in 0.1V increments. Insert the desired nominal reset threshold (from Table 1) into the blanks following the letters UK. All parts also offer factory-programmed reset timeout periods. Insert the number corresponding to the desired nominal timeout period index following the "D" in the part number (D1 = 1ms min, D2 = 20ms min, D3 = 140ms min, and D4 = 1120ms min). Contact factory for availability and minimum order sizes.*

Ordering Information continued at end of data sheet.

Selector Table

PART	OPEN-DRAIN $\overline{RESET}$ OUTPUT	PUSH/PULL $\overline{RESET}$ OUTPUT	PUSH/PULL RESET OUTPUT	FACTORY-SET RESET THRESHOLD ON V_{CC}	ADDITIONAL UNDERVOLTAGE RESET INPUTS	NEGATIVE/ OVERVOLTAGE RESET INPUT	MANUAL-RESET INPUT
MAX6305	✔	—	—	—	2	—	—
MAX6306	✔	—	—	✔	1	—	✔
MAX6307	✔	—	—	✔	1	✔	—
MAX6308	—	✔	—	—	2	—	—
MAX6309	—	✔	—	✔	1	—	✔
MAX6310	—	✔	—	✔	1	✔	—
MAX6311	—	—	✔	—	2	—	—
MAX6312	—	—	✔	✔	1	—	✔
MAX6313	—	—	✔	✔	1	✔	—

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5-Pin, Multiple-Input, Programmable Reset ICs

ABSOLUTE MAXIMUM RATINGS

V_{CC} .....-0.3V to +6V
All Other Pins.....-0.3V to (V_{CC} + 0.3V)
Input/Output Current, All Pins 20mA
Rate of Rise, V_{CC} 100V/µs

Continuous Power Dissipation (T_A = +70°C)
SOT23-5 (derate 7.1mW/°C above +70°C).....571mW
Operating Temperature Range.....0°C to +70°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.5V to +5.5V for the MAX6305/MAX6308/MAX6311, V_{CC} = (V_{TH} + 2.5%) to +5.5V for the MAX6306/MAX6307/MAX6309/MAX6310/MAX6312/MAX6313; T_A = 0°C to +70°C; unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC} Range		T_A = 0°C to +70°C (Note 1)		1.0		5.5	V
Supply Current	I_{CC}	V_{CC} = 5.5V			8	16	µA
Reset Threshold (Note 2)	V_{TH}	MAX6306/MAX6307/ MAX6309/MAX6310/ MAX6312/MAX6313	T_A = +25°C	V_{TH} - 1.5%	V_{TH}	V_{TH} + 1.5%	V
			T_A = 0°C to +70°C	V_{TH} - 2.5%		V_{TH} + 2.5%	
Reset Threshold Tempco	ΔV_{TH}/°C				40		ppm/°C
Reset Threshold Hysteresis	V_{TH} HYST				2 x V_{TH}		mV
Reset Timeout Period	t_{RP}	D1		1	1.4	2	ms
		D2		20	28	40	
		D3		140	200	280	
		D4		1120	1570	2240	
$\overline{RESET}$ Output Voltage	V_{OL}	MAX6305–MAX6310	V_{CC} > 4.25V, I_{SINK} = 3.2mA			0.4	V
			V_{CC} > 2.5V, I_{SINK} = 1.2mA			0.3	
			T_A = 0°C to +70°C, V_{CC} > 1.2V, I_{SINK} = 500µA			0.3	
			T_A = 0°C to +70°C, V_{CC} > 1.0V, I_{SINK} = 50µA			0.3	
	V_{OH}	MAX6308/MAX6309/ MAX6310	V_{CC} > 4.25V, I_{SOURCE} = 800µA	VCC - 1.5			
			V_{CC} > 2.5V, I_{SOURCE} = 500µA	0.8 x VCC			
RESET Output Voltage	V_{OL}	MAX6311/MAX6312/ MAX6313	V_{CC} > 4.25V, I_{SINK} = 3.2mA			0.4	V
			V_{CC} > 2.5V, I_{SINK} = 1.2mA			0.3	
	V_{OH}		V_{CC} > 1.8V, I_{SOURCE} = 150µA	0.8 x VCC			
			T_A = 0°C to +70°C, V_{CC} > 1.0V, I_{SOURCE} = 10µA	0.8 x VCC			

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.5V to +5.5V for the MAX6305/MAX6308/MAX6311, V_{CC} = (V_{TH} + 2.5%) to +5.5V for the MAX6306/MAX6307/MAX6309/MAX6310/MAX6312/MAX6313; T_A = 0°C to +70°C; unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MANUAL-RESET INPUT (MAX6308/MAX6309/MAX6310)						
$\overline{MR}$ Input	V_{IL}	V_{TH} > 4.0V	0.8			V
	V_{IH}				2.4	
	V_{IL}	V_{TH} < 4.0V	0.3 x V_{CC}			
	V_{IH}				0.7 x V_{CC}	
$\overline{MR}$ Minimum Input Pulse			1			µs
$\overline{MR}$ Glitch Rejection				0.1		µs
$\overline{MR}$ to Reset Delay				500		nsV
$\overline{MR}$ Pull-Up Resistance			32	63.5	100	kΩ
ADJUSTABLE RESET COMPARATOR INPUTS						
RST IN Input Threshold	V_{RSTH}	T_A = +25°C	1.21	1.23	1.25	V
		T_A = 0°C to +70°C	1.20		1.26	
RST IN Input Current	$I_{RST\ IN_}$	0V < $V_{RST\ IN_}$ < V_{CC} - 0.3V	-25		25	nA
RST IN Hysteresis				2.5		mV

Note 1: The MAX6305/MAX6308/MAX6311 switch from undervoltage reset to normal operation between 1.5V < V_{CC} < 2.5V.

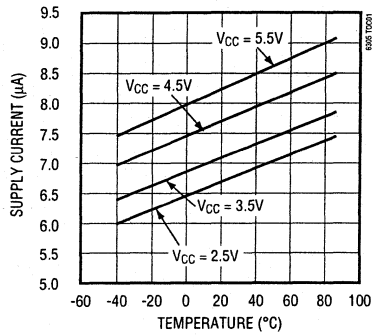
Note 2: The MAX6306/MAX6307/MAX6309/MAX6310/MAX6312/MAX6313 monitor V_{CC} through an internal factory-trimmed voltage divider, which programs the nominal reset threshold. Factory-trimmed reset thresholds are available in approximately 100mV increments from 2.5V to 5V (Table 1).

5-Pin, Multiple-Input, Programmable Reset ICs

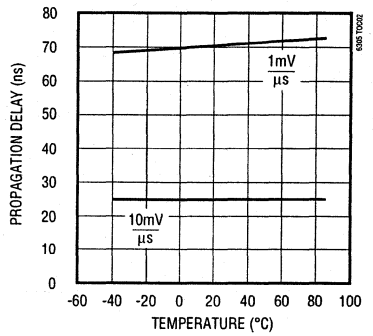
Typical Operating Characteristics

(V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

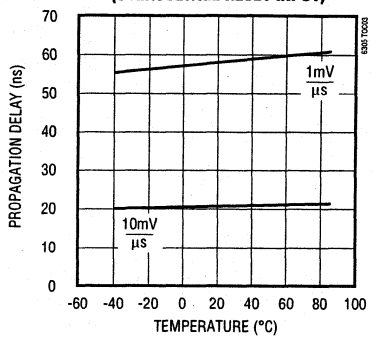
SUPPLY CURRENT vs. TEMPERATURE



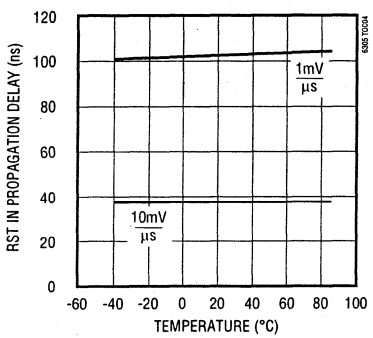
VCC FALLING PROPAGATION DELAY vs. TEMPERATURE



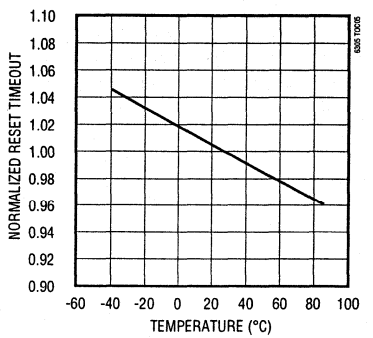
OVRST IN RISING PROPAGATION DELAY vs. TEMPERATURE (OVERVOLTAGE RESET INPUT)



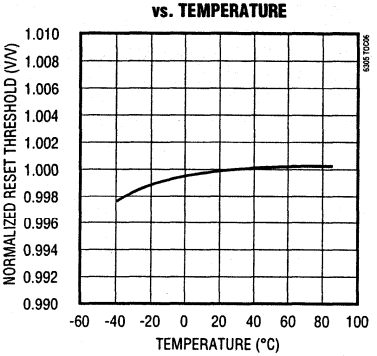
RST IN_ FALLING PROPAGATION DELAY vs. TEMPERATURE



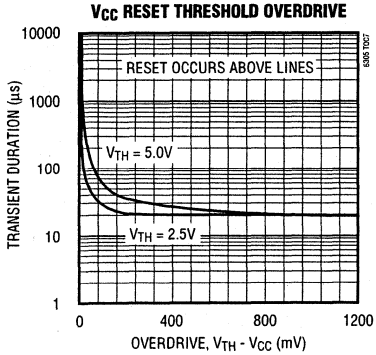
RESET TIMEOUT vs. TEMPERATURE



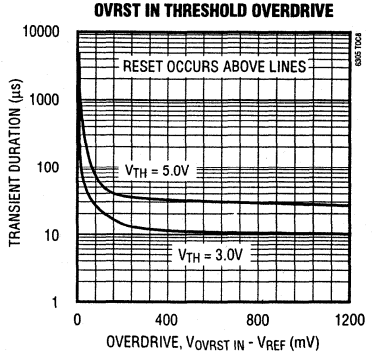
RESET THRESHOLD vs. TEMPERATURE



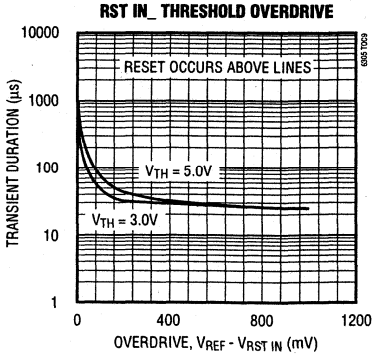
MAXIMUM TRANSIENT DURATION vs. VCC RESET THRESHOLD OVERDRIVE



MAXIMUM TRANSIENT DURATION vs. OVRST IN THRESHOLD OVERDRIVE



MAXIMUM TRANSIENT DURATION vs. RST IN_ THRESHOLD OVERDRIVE



5-Pin, Multiple-Input, Programmable Reset ICs

Pin Description

PIN			NAME	FUNCTION
MAX6305 MAX6308 MAX6311	MAX6306 MAX6309 MAX6312	MAX6307 MAX6310 MAX6313		
1	1	1	$\overline{\text{RESET}}$	Active-Low, Open-Drain Reset Output for the MAX6305/MAX6306/MAX6307. Active-Low, Push/Pull Reset Output (sources and sinks current) for the MAX6308/MAX6309/MAX6310.
			RESET	Active-High, Push/Pull Reset Output for the MAX6311/MAX6312/MAX6313
2	2	2	GND	System Ground
—	3	—	$\overline{\text{MR}}$	Manual-Reset Input. Pull low to force a reset. $\overline{\text{RESET}}$/RESET remains active as long as $\overline{\text{MR}}$ is low and for the timeout period after $\overline{\text{MR}}$ goes high. Leave unconnected or connect to V_{CC} if unused.
3, 4	—	—	RST IN1, RST IN2	Undervoltage Reset Comparator Input. Asserts reset when the monitored voltage falls below the programmed threshold. Set the reset threshold with an external resistor divider. Connect to V_{CC} if unused.
—	4	3	RST IN	
—	—	4	OVRST IN	Overvoltage Reset Comparator Input. Asserts reset when the monitored voltage exceeds the programmed threshold. Set the reset threshold with an external resistor divider. Connect to GND if unused.
5	5	5	V_{CC}	System Supply. The MAX6306/MAX6307/MAX6309/MAX6310/MAX6312/MAX6313 also monitor V_{CC} through an internal factory-trimmed resistor divider to the reset comparator.

Detailed Description

The MAX6305–MAX6313 CMOS microprocessor (µP) supervisory circuits are designed to monitor more than one power supply and issue a system reset when any monitored supply falls out of regulation. The MAX6305/MAX6308/MAX6311 have two adjustable undervoltage reset inputs (RST IN1 and RST IN2). The MAX6306/MAX6307/MAX6309/MAX6310/MAX6312/MAX6313 monitor V_{CC} through an internal, factory-trimmed voltage divider. The MAX6306/ MAX6309/ MAX6312 have, in addition, an adjustable undervoltage reset input and a manual-reset input. The internal voltage divider sets the reset threshold as specified in the device part number (Table 1). The MAX6307/MAX6310/ MAX6313 feature an adjustable undervoltage reset input (RST IN) and an adjustable overvoltage reset input (OVRST IN) in addition to the factory-trimmed reset threshold on the V_{CC} monitor. Program the adjustable reset inputs with an external resistor divider (see *Adjustable Reset Inputs* section).

Reset Outputs

A µP's reset input starts the µP in a known state. These µP supervisory circuits assert reset to prevent code-execution errors during power-up, power-down, or brownout conditions.

$\overline{\text{RESET}}$ (MAX6305–MAX6310) and RESET (MAX6311/ MAX6312/MAX6313) are guaranteed to be asserted at a valid logic level for V_{CC} > 1V (see *Electrical Characteristics*). Once all monitored voltages exceed their programmed reset thresholds, an internal timer keeps reset asserted for the reset timeout period (t_{RP}); after this interval, reset deasserts.

If a brownout condition occurs (any or all monitored voltages dip outside their programmed reset threshold), reset asserts (RESET goes high; $\overline{\text{RESET}}$ goes low). Any time any of the monitored voltages dip below their reset threshold, the internal timer resets to zero and reset asserts. The internal timer starts when all of the monitored voltages return above their reset thresholds, and reset remains asserted for a reset timeout period. The MAX6305/MAX6306/MAX6307 feature an active-low,

5-Pin, Multiple-Input, Programmable Reset ICs

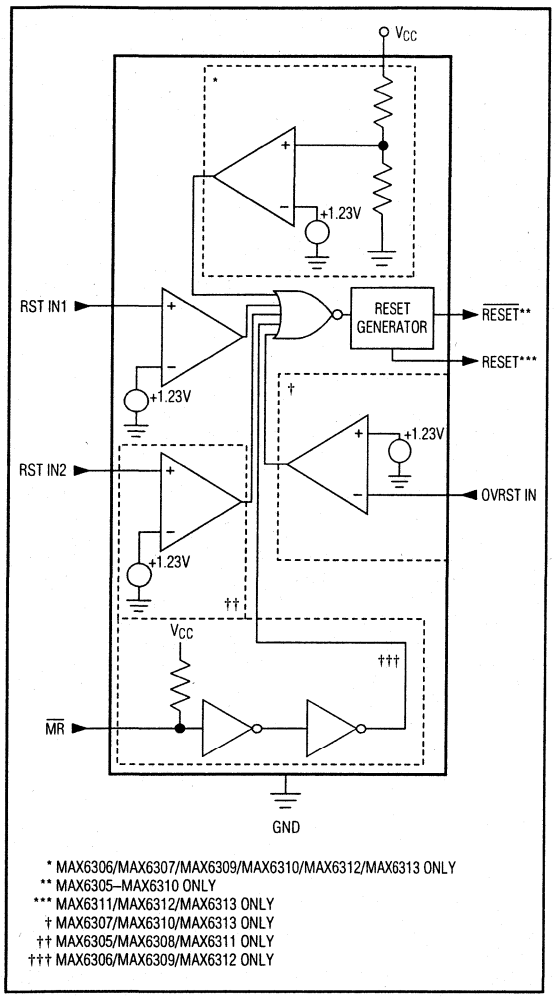


Figure 1. Functional Diagram

open-drain, N-channel output. The MAX6308/MAX6309/MAX6310 feature an active-low, complementary output structure that both sinks and sources current, and the MAX6311/MAX6312/MAX6313 have an active-high complementary reset output.

The MAX6305/MAX6308/MAX6311 switch from undervoltage lockout operation to normal operation between 1.5V < V_{CC} < 2.5V. Below 1.5V, V_{CC} undervoltage-lockout mode asserts $\overline{RESET}$. Above 2.5V, V_{CC} normal-operation mode asserts reset if RST IN_ falls below the RST IN_ threshold.

Manual-Reset Input (MAX6303/MAX6309/MAX6312)

Many µP-based products require manual-reset capability, allowing an operator or external logic circuitry to initiate a reset. A logic low on $\overline{MR}$ asserts reset. Reset remains asserted while $\overline{MR}$ is low, and for a reset active timeout period (t_{RP}) after $\overline{MR}$ returns high. This input has an internal 63.5kΩ pull-up resistor, so it can be left open if it is not used. $\overline{MR}$ can be driven with TTL-logic levels in 5V systems, with CMOS-logic levels in 3V systems, or with open-drain/collector output devices. Connect a normally open momentary switch from $\overline{MR}$ to GND to create a manual-reset function; external debounce circuitry is not required. If $\overline{MR}$ is driven from long cables or if the device is used in a noisy environment, connecting a 0.1µF capacitor from $\overline{MR}$ to ground provides additional noise immunity.

The $\overline{MR}$ pin has internal ESD-protection circuitry that may be forward biased under certain conditions, drawing excessive current. For example, assume the circuitry driving $\overline{MR}$ uses a +5V supply other than V_{CC}. If V_{CC} drops or browns out lower than +4.7V, $\overline{MR}$'s absolute maximum rating is violated (-0.3V to (V_{CC} + 0.3V)), and undesirable current flows through the ESD structure from $\overline{MR}$ to V_{CC}. To avoid this, it is recommended that the supply for the $\overline{MR}$ pin be the same as the supply monitored by V_{CC}. In this way, the voltage at $\overline{MR}$ will not exceed V_{CC}.

Adjustable Reset Inputs

The MAX6305–MAX6313 each have one or more reset inputs (RST IN_ /OVRST IN). These inputs are compared to the internal reference voltage (Figure 1). Connect a resistor voltage divider to RST IN_ such that $V_{RST\ IN_}$ falls below V_{RSTH} (1.23V) when the monitored voltage (V_{IN}) falls below the desired reset threshold (V_{TH}) (Figure 2). Calculate the desired reset voltage with the following formula:

$$V_{TH} = \frac{R1 + R2}{R2} \times V_{RSTH}$$

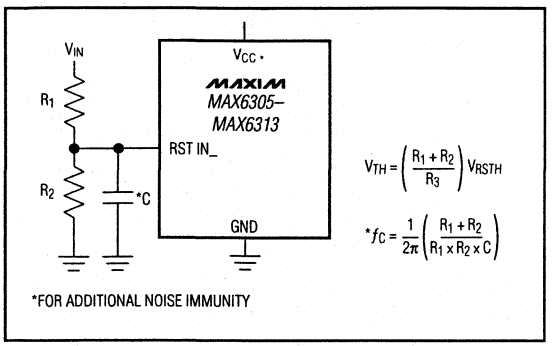


Figure 2. Increasing Noise Immunity

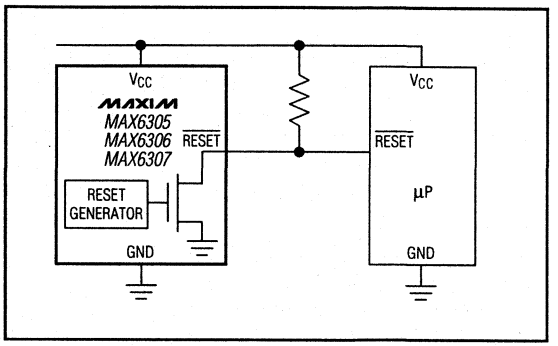


Figure 3. Interfacing to µPs with Bidirectional Reset I/O

The ±25nA max input leakage current allows resistors on the order of megohms. Choose the pull-up resistor in the divider to minimize the error due to the input leakage current. The error term in the calculated threshold is simply:

$$\pm 25nA \times R1$$

If you choose R1 to be 1MΩ, the resulting error is $\pm 25 \times 10^{-9} \times 1 \times 10^{6} = \pm 25mV$.

Like the V_{CC} voltage monitors on the MAX6306/MAX6307/MAX6309/MAX6310/MAX6312/MAX6313, the RST IN_ inputs (when used with a voltage divider) are designed to ignore fast voltage transients. Increase the noise immunity by connecting a capacitor on the order of 0.1µF between RST IN and GND (Figure 2). This creates a single-pole lowpass filter with a corner frequency given by:

$$f = (1/2\pi) / (R1 + R2)(R1 \times R2 \times C)$$

For example, if R1 = 1MΩ and R2 = 1.6MΩ, adding a 0.1µF capacitor from RST IN_ to ground results in a lowpass corner frequency of f = 2.59Hz. Note that adding capacitance to RST IN slows the circuit's overall response time.

Applications Information

Interfacing to µPs with Bidirectional Reset Pins

Since the $\overline{RESET}$ output on the MAX6305/MAX6306/MAX6307 is open drain, these devices interface easily with µPs that have bidirectional reset pins, such as the Motorola 68HC11. Connecting the µP supervisor's $\overline{RESET}$ output directly to the microcontroller's $\overline{RESET}$ pin with a single pull-up resistor allows either device to assert reset (Figure 3).

Negative-Going V_{CC} Transients

In addition to issuing a reset to the µP during power-up, power-down, and brownout conditions, these devices are relatively immune to short-duration, negative-going V_{CC} transients (glitches).

The *Typical Operating Characteristics* show the Maximum Transient Duration vs. Reset Threshold Overdrive, for which reset pulses are not generated. The graph was produced using negative-going pulses, starting at V_{TH} max, and ending below the programmed reset threshold by the magnitude indicated (reset threshold overdrive). The graph shows the maximum pulse width that a negative-going V_{CC} transient may typically have without causing a reset pulse to be issued. As the amplitude of the transient increases (i.e., goes farther below the reset threshold), the maximum allowable pulse width decreases.

RST IN_/OVRST IN are also immune to negative/positive-going transients (see *Typical Operating Characteristics*). A 0.1µF bypass capacitor mounted close to the RST IN_, OVRST IN, and/or the V_{CC} pin provides additional transient immunity.

Ensuring a Valid $\overline{RESET}$/RESET Output Down to V_{CC} = 0V

When V_{CC} falls below 1V, push/pull structured $\overline{RESET}$/RESET current sinking (or sourcing) capabilities decrease drastically. High-impedance CMOS-logic inputs connected to $\overline{RESET}$ can drift to undetermined voltages. This presents no problem in most applications, since most µPs and other circuitry do not operate with V_{CC} below 1V. In those applications where $\overline{RESET}$ must be valid down to 0V, adding a pull-down resistor between $\overline{RESET}$ and ground sinks any stray leakage

currents, holding $\overline{RESET}$ low (Figure 4). The pull-down resistor's value is not critical; 100kΩ is large enough not to load $\overline{RESET}$ and small enough to pull $\overline{RESET}$ to ground. For applications where RESET must be valid to V_{CC}, a 100kΩ pull-up resistor between RESET and V_{CC} will hold RESET high when V_{CC} falls below 1V (Figure 5).

Since the MAX6305/MAX6306/MAX6307 have open-drain, active-low outputs, they typically use a pull-up resistor. With these devices and under these conditions (V_{CC} < 1V), $\overline{RESET}$ will most likely not maintain an active condition, but will drift toward a nonactive level due to the pull-up resistor and the $\overline{RESET}$ output's reduction in sinking capability. These devices are not recommended for applications that require a valid $\overline{RESET}$ output below 1V.

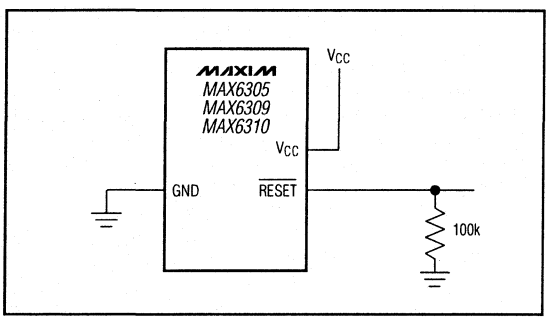


Figure 4. Ensuring $\overline{RESET}$ Valid to V_{CC} = 0V

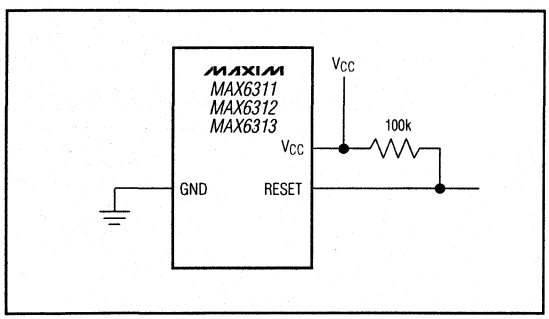


Figure 5. Ensuring RESET Valid to V_{CC} = 0V

Table 1. Factory-Trimmed Reset Thresholds*

SUFFIX	T_A = +25°C			T_A = 0°C to +70°C	
	MIN	TYP	MAX	MIN	MAX
UK00	Preprogrammed Threshold Not Available			Preprogrammed Threshold Not Available	
UK50	4.925	5.000	5.075	4.875	5.125
UK49	4.827	4.900	4.974	4.778	5.023
UK48	4.728	4.800	4.872	4.680	4.920
UK47	4.630	4.700	4.771	4.583	4.818
UK46	4.561	4.630	4.699	4.514	4.746
UK45	4.433	4.500	4.568	4.388	4.613
UK44	4.314	4.380	4.446	4.270	4.490
UK43	4.236	4.300	4.365	4.193	4.408
UK42	4.137	4.200	4.263	4.095	4.305
UK41	4.039	4.100	4.162	3.998	4.203
UK40	3.940	4.000	4.060	3.900	4.100
UK39	3.842	3.900	3.959	3.803	3.998
UK38	3.743	3.800	3.857	3.705	3.895
UK37	3.645	3.700	3.756	3.608	3.793
UK36	3.546	3.600	3.654	3.510	3.690
UK35	3.448	3.500	3.553	3.413	3.588
UK34	3.349	3.400	3.451	3.315	3.485
UK33	3.251	3.300	3.350	3.218	3.383
UK32	3.152	3.200	3.248	3.120	3.280
UK31	3.034	3.080	3.126	3.003	3.157
UK30	2.955	3.000	3.045	2.925	3.075
UK29	2.886	2.930	2.974	2.857	3.000
UK28	2.758	2.800	2.842	2.730	2.870
UK27	2.660	2.700	2.741	2.633	2.768
UK26	2.591	2.630	2.669	2.564	2.696
UK25	2.463	2.500	2.538	2.438	2.563

** Factory-trimmed reset thresholds are available in approximately 100mV increments with a ±1.5% room-temperature variance.*

Table 2. Device Marking Codes

DEVICE	CODE	DEVICE	CODE	DEVICE	CODE	DEVICE	CODE
MAX6305UK00D1-T	ABAK	MAX6306UK41D3-T	ABCA	MAX6306UK30D1-T	ABDQ	MAX6307UK46D3-T	ABFG
MAX6305UK00D2-T	ABAL	MAX6306UK41D4-T	ABCB	MAX6306UK30D2-T	ABDR	MAX6307UK46D4-T	ABFH
MAX6305UK00D3-T	ABAM	MAX6306UK40D1-T	ABCC	MAX6306UK30D3-T	ABDS	MAX6307UK45D1-T	ABFI
MAX6305UK00D4-T	ABAN	MAX6306UK40D2-T	ABCD	MAX6306UK30D4-T	ABDT	MAX6307UK45D2-T	ABFJ
MAX6306UK50D1-T	ABAO	MAX6306UK40D3-T	ABCE	MAX6306UK29D1-T	ABDU	MAX6307UK45D3-T	ABFK
MAX6306UK50D2-T	ABAP	MAX6306UK40D4-T	ABCF	MAX6306UK29D2-T	ABDV	MAX6307UK45D4-T	ABFL
MAX6306UK50D3-T	ABAQ	MAX6306UK39D1-T	ABCG	MAX6306UK29D3-T	ABDW	MAX6307UK44D1-T	ABFM
MAX6306UK50D4-T	ABAR	MAX6306UK39D2-T	ABCH	MAX6306UK29D4-T	ABDX	MAX6307UK44D2-T	ABFN
MAX6306UK49D1-T	ABAS	MAX6306UK39D3-T	ABCI	MAX6306UK28D1-T	ABDY	MAX6307UK44D3-T	ABFO
MAX6306UK49D2-T	ABAT	MAX6306UK39D4-T	ABCJ	MAX6306UK28D2-T	ABDZ	MAX6307UK44D4-T	ABFP
MAX6306UK49D3-T	ABAU	MAX6306UK38D1-T	ABCK	MAX6306UK28D3-T	ABEA	MAX6307UK43D1-T	ABFQ
MAX6306UK49D4-T	ABAV	MAX6306UK38D2-T	ABCL	MAX6306UK28D4-T	ABEB	MAX6307UK43D2-T	ABFR
MAX6306UK48D1-T	ABAW	MAX6306UK38D3-T	ABCM	MAX6306UK27D1-T	ABEC	MAX6307UK43D3-T	ABFS
MAX6306UK48D2-T	ABAX	MAX6306UK38D4-T	ABCN	MAX6306UK27D2-T	ABED	MAX6307UK43D4-T	ABFT
MAX6306UK48D3-T	ABAY	MAX6306UK37D1-T	ABCO	MAX6306UK27D3-T	ABEE	MAX6307UK42D1-T	ABFU
MAX6306UK48D4-T	ABAZ	MAX6306UK37D2-T	ABCP	MAX6306UK27D4-T	ABEF	MAX6307UK42D2-T	ABFV
MAX6306UK47D1-T	ABBA	MAX6306UK37D3-T	ABCQ	MAX6306UK26D1-T	ABEG	MAX6307UK42D3-T	ABFW
MAX6306UK47D2-T	ABBB	MAX6306UK37D4-T	ABCR	MAX6306UK26D2-T	ABEH	MAX6307UK42D4-T	ABFX
MAX6306UK47D3-T	ABBC	MAX6306UK36D1-T	ABCS	MAX6306UK26D3-T	ABEI	MAX6307UK41D1-T	ABFY
MAX6306UK47D4-T	ABBD	MAX6306UK36D2-T	ABCT	MAX6306UK26D4-T	ABEJ	MAX6307UK41D2-T	ABFZ
MAX6306UK46D1-T	ABBE	MAX6306UK36D3-T	ABCU	MAX6306UK25D1-T	ABEK	MAX6307UK41D3-T	ABGA
MAX6306UK46D2-T	ABBF	MAX6306UK36D4-T	ABCV	MAX6306UK25D2-T	ABEL	MAX6307UK41D4-T	ABGB
MAX6306UK46D3-T	ABBG	MAX6306UK35D1-T	ABCW	MAX6306UK25D3-T	ABEM	MAX6307UK40D1-T	ABGC
MAX6306UK46D4-T	ABBH	MAX6306UK35D2-T	ABCX	MAX6306UK25D4-T	ABEN	MAX6307UK40D2-T	ABGD
MAX6306UK45D1-T	ABBI	MAX6306UK35D3-T	ABCY	MAX6307UK50D1-T	ABEO	MAX6307UK40D3-T	ABGE
MAX6306UK45D2-T	ABBJ	MAX6306UK35D4-T	ABCZ	MAX6307UK50D2-T	ABEP	MAX6307UK40D4-T	ABGF
MAX6306UK45D3-T	ABBK	MAX6306UK34D1-T	ABDA	MAX6307UK50D3-T	ABEQ	MAX6307UK39D1-T	ABGG
MAX6306UK45D4-T	ABBL	MAX6306UK34D2-T	ABDB	MAX6307UK50D4-T	ABER	MAX6307UK39D2-T	ABGH
MAX6306UK44D1-T	ABBM	MAX6306UK34D3-T	ABDC	MAX6307UK49D1-T	ABES	MAX6307UK39D3-T	ABGI
MAX6306UK44D2-T	ABBN	MAX6306UK34D4-T	ABDD	MAX6307UK49D2-T	ABET	MAX6307UK39D4-T	ABGJ
MAX6306UK44D3-T	ABBO	MAX6306UK33D1-T	ABDE	MAX6307UK49D3-T	ABEU	MAX6307UK38D1-T	ABGK
MAX6306UK44D4-T	ABBP	MAX6306UK33D2-T	ABDF	MAX6307UK49D4-T	ABEV	MAX6307UK38D2-T	ABGL
MAX6306UK43D1-T	ABBQ	MAX6306UK33D3-T	ABDG	MAX6307UK48D1-T	ABEW	MAX6307UK38D3-T	ABGM
MAX6306UK43D2-T	ABBR	MAX6306UK33D4-T	ABDH	MAX6307UK48D2-T	ABEX	MAX6307UK38D4-T	ABGN
MAX6306UK43D3-T	ABBS	MAX6306UK32D1-T	ABDI	MAX6307UK48D3-T	ABEY	MAX6307UK37D1-T	ABGO
MAX6306UK43D4-T	ABBT	MAX6306UK32D2-T	ABDJ	MAX6307UK48D4-T	ABEZ	MAX6307UK37D2-T	ABGP
MAX6306UK42D1-T	ABBU	MAX6306UK32D3-T	ABDK	MAX6307UK47D1-T	ABFA	MAX6307UK37D3-T	ABGQ
MAX6306UK42D2-T	ABBV	MAX6306UK32D4-T	ABDL	MAX6307UK47D2-T	ABFB	MAX6307UK37D4-T	ABGR
MAX6306UK42D3-T	ABBW	MAX6306UK31D1-T	ABDM	MAX6307UK47D3-T	ABFC	MAX6307UK36D1-T	ABGS
MAX6306UK42D4-T	ABBX	MAX6306UK31D2-T	ABDN	MAX6307UK47D4-T	ABFD	MAX6307UK36D2-T	ABGT
MAX6306UK41D1-T	ABBY	MAX6306UK31D3-T	ABDO	MAX6307UK46D1-T	ABFE	MAX6307UK36D3-T	ABGU
MAX6306UK41D2-T	ABBZ	MAX6306UK31D4-T	ABDP	MAX6307UK46D2-T	ABFF	MAX6307UK36D4-T	ABGV

5-Pin, Multiple-Input, Programmable Reset ICs

Table 2. Device Marking Codes (continued)

DEVICE	CODE	DEVICE	CODE	DEVICE	CODE	DEVICE	CODE
MAX6307UK35D1-T	ABGW	MAX6307UK25D3-T	ABIM	MAX6309UK41D1-T	ABKC	MAX6309UK31D3-T	ABLS
MAX6307UK35D2-T	ABGX	MAX6307UK25D4-T	ABIN	MAX6309UK41D2-T	ABKD	MAX6309UK31D4-T	ABLT
MAX6307UK35D3-T	ABGY	MAX6308UK00D1-T	ABIO	MAX6309UK41D3-T	ABKE	MAX6309UK30D1-T	ABLU
MAX6307UK35D4-T	ABGZ	MAX6308UK00D2-T	ABIP	MAX6309UK41D4-T	ABKF	MAX6309UK30D2-T	ABLV
MAX6307UK34D1-T	ABHA	MAX6308UK00D3-T	ABIQ	MAX6309UK40D1-T	ABKG	MAX6309UK30D3-T	ABLW
MAX6307UK34D2-T	ABHB	MAX6308UK00D4-T	ABIR	MAX6309UK40D2-T	ABKH	MAX6309UK30D4-T	ABLX
MAX6307UK34D3-T	ABHC	MAX6309UK50D1-T	ABIS	MAX6309UK40D3-T	ABKI	MAX6309UK29D1-T	ABLY
MAX6307UK34D4-T	ABHD	MAX6309UK50D2-T	ABIT	MAX6309UK40D4-T	ABKJ	MAX6309UK29D2-T	ABLZ
MAX6307UK33D1-T	ABHE	MAX6309UK50D3-T	ABIU	MAX6309UK39D1-T	ABKK	MAX6309UK29D3-T	ABMA
MAX6307UK33D2-T	ABHF	MAX6309UK50D4-T	ABIV	MAX6309UK39D2-T	ABKL	MAX6309UK29D4-T	ABMB
MAX6307UK33D3-T	ABHG	MAX6309UK49D1-T	ABIW	MAX6309UK39D3-T	ABKM	MAX6309UK28D1-T	ABMC
MAX6307UK33D4-T	ABHH	MAX6309UK49D2-T	ABIX	MAX6309UK39D4-T	ABKN	MAX6309UK28D2-T	ABMD
MAX6307UK32D1-T	ABHI	MAX6309UK49D3-T	ABIY	MAX6309UK38D1-T	ABKO	MAX6309UK28D3-T	ABME
MAX6307UK32D2-T	ABHJ	MAX6309UK49D4-T	ABIZ	MAX6309UK38D2-T	ABKP	MAX6309UK28D4-T	ABMF
MAX6307UK32D3-T	ABHK	MAX6309UK48D1-T	ABJA	MAX6309UK38D3-T	ABKQ	MAX6309UK27D1-T	ABMG
MAX6307UK32D4-T	ABHL	MAX6309UK48D2-T	ABJB	MAX6309UK38D4-T	ABKR	MAX6309UK27D2-T	ABMH
MAX6307UK31D1-T	ABHM	MAX6309UK48D3-T	ABJC	MAX6309UK37D1-T	ABKS	MAX6309UK27D3-T	ABMI
MAX6307UK31D2-T	ABHN	MAX6309UK48D4-T	ABJD	MAX6309UK37D2-T	ABKT	MAX6309UK27D4-T	ABMJ
MAX6307UK31D3-T	ABHO	MAX6309UK47D1-T	ABJE	MAX6309UK37D3-T	ABKU	MAX6309UK26D1-T	ABMK
MAX6307UK31D4-T	ABHP	MAX6309UK47D2-T	ABJF	MAX6309UK37D4-T	ABKV	MAX6309UK26D2-T	ABML
MAX6307UK30D1-T	ABHQ	MAX6309UK47D3-T	ABJG	MAX6309UK36D1-T	ABKW	MAX6309UK26D3-T	ABMM
MAX6307UK30D2-T	ABHR	MAX6309UK47D4-T	ABJH	MAX6309UK36D2-T	ABKX	MAX6309UK26D4-T	ABMN
MAX6307UK30D3-T	ABHS	MAX6309UK46D1-T	ABJI	MAX6309UK36D3-T	ABKY	MAX6309UK25D1-T	ABMO
MAX6307UK30D4-T	ABHT	MAX6309UK46D2-T	ABJJ	MAX6309UK36D4-T	ABKZ	MAX6309UK25D2-T	ABMP
MAX6307UK29D1-T	ABHU	MAX6309UK46D3-T	ABJK	MAX6309UK35D1-T	ABLA	MAX6309UK25D3-T	ABMQ
MAX6307UK29D2-T	ABHV	MAX6309UK46D4-T	ABJL	MAX6309UK35D2-T	ABLB	MAX6309UK25D4-T	ABMR
MAX6307UK29D3-T	ABHW	MAX6309UK45D1-T	ABJM	MAX6309UK35D3-T	ABLC	MAX6310UK50D1-T	ABMS
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MAX6307UK28D1-T	ABHY	MAX6309UK45D3-T	ABJO	MAX6309UK34D1-T	ABLE	MAX6310UK50D3-T	ABMU
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MAX6307UK27D1-T	ABIC	MAX6309UK44D3-T	ABJS	MAX6309UK33D1-T	ABLI	MAX6310UK49D3-T	ABMY
MAX6307UK27D2-T	ABID	MAX6309UK44D4-T	ABJT	MAX6309UK33D2-T	ABLJ	MAX6310UK49D4-T	ABMZ
MAX6307UK27D3-T	ABIE	MAX6309UK43D1-T	ABJU	MAX6309UK33D3-T	ABLK	MAX6310UK48D1-T	ABNA
MAX6307UK27D4-T	ABIF	MAX6309UK43D2-T	ABJV	MAX6309UK33D4-T	ABLL	MAX6310UK48D2-T	ABNB
MAX6307UK26D1-T	ABIG	MAX6309UK43D3-T	ABJW	MAX6309UK32D1-T	ABLM	MAX6310UK48D3-T	ABNC
MAX6307UK26D2-T	ABIH	MAX6309UK43D4-T	ABJX	MAX6309UK32D2-T	ABLN	MAX6310UK48D4-T	ABND
MAX6307UK26D3-T	ABII	MAX6309UK42D1-T	ABJY	MAX6309UK32D3-T	ABLO	MAX6310UK47D1-T	ABNE
MAX6307UK26D4-T	ABIJ	MAX6309UK42D2-T	ABJZ	MAX6309UK32D4-T	ABLP	MAX6310UK47D2-T	ABNF
MAX6307UK25D1-T	ABIK	MAX6309UK42D3-T	ABKA	MAX6309UK31D1-T	ABLQ	MAX6310UK47D3-T	ABNG
MAX6307UK25D2-T	ABIL	MAX6309UK42D4-T	ABKB	MAX6309UK31D2-T	ABLR	MAX6310UK47D4-T	ABNH

Table 2. Device Marking Codes (continued)

DEVICE	CODE	DEVICE	CODE	DEVICE	CODE	DEVICE	CODE
MAX6310UK46D1-T	ABNI	MAX6310UK36D3-T	ABOY	MAX6310UK25D1-T	ABQO	MAX6312UK42D3-T	ABSE
MAX6310UK46D2-T	ABNJ	MAX6310UK36D4-T	ABOZ	MAX6310UK25D2-T	ABQP	MAX6312UK42D4-T	ABSF
MAX6310UK46D3-T	ABNK	MAX6310UK35D1-T	ABPA	MAX6310UK25D3-T	ABQQ	MAX6312UK41D1-T	ABSG
MAX6310UK46D4-T	ABNL	MAX6310UK35D2-T	ABPB	MAX6310UK25D4-T	ABQR	MAX6312UK41D2-T	ABSH
MAX6310UK45D1-T	ABNM	MAX6310UK35D3-T	ABPC	MAX6311UK00D1-T	ABQS	MAX6312UK41D3-T	ABSI
MAX6310UK45D2-T	ABNN	MAX6310UK35D4-T	ABPD	MAX6311UK00D2-T	ABQT	MAX6312UK41D4-T	ABSJ
MAX6310UK45D3-T	ABNO	MAX6310UK34D1-T	ABPE	MAX6311UK00D3-T	ABQU	MAX6312UK40D1-T	ABSK
MAX6310UK45D4-T	ABNP	MAX6310UK34D2-T	ABPF	MAX6311UK00D4-T	ABQV	MAX6312UK40D2-T	ABSL
MAX6310UK44D1-T	ABNQ	MAX6310UK34D3-T	ABPG	MAX6311UK50D1-T	ABQW	MAX6312UK40D3-T	ABSM
MAX6310UK44D2-T	ABNR	MAX6310UK34D4-T	ABPH	MAX6312UK50D2-T	ABQX	MAX6312UK40D4-T	ABSN
MAX6310UK44D3-T	ABNS	MAX6310UK33D1-T	ABPI	MAX6312UK50D3-T	ABQY	MAX6312UK39D1-T	ABSO
MAX6310UK44D4-T	ABNT	MAX6310UK33D2-T	ABPJ	MAX6312UK50D4-T	ABQZ	MAX6312UK39D2-T	ABSP
MAX6310UK43D1-T	ABNU	MAX6310UK33D3-T	ABPK	MAX6312UK49D1-T	ABRA	MAX6312UK39D3-T	ABSQ
MAX6310UK43D2-T	ABNV	MAX6310UK33D4-T	ABPL	MAX6312UK49D2-T	ABRB	MAX6312UK39D4-T	ABSR
MAX6310UK43D3-T	ABNW	MAX6310UK32D1-T	ABPM	MAX6312UK49D3-T	ABRC	MAX6312UK38D1-T	ABSS
MAX6310UK43D4-T	ABNX	MAX6310UK32D2-T	ABPN	MAX6312UK49D4-T	ABRD	MAX6312UK38D2-T	ABST
MAX6310UK42D1-T	ABNY	MAX6310UK32D3-T	ABPO	MAX6312UK48D1-T	ABRE	MAX6312UK38D3-T	ABSU
MAX6310UK42D2-T	ABNZ	MAX6310UK32D4-T	ABPP	MAX6312UK48D2-T	ABRF	MAX6312UK38D4-T	ABSV
MAX6310UK42D3-T	ABOA	MAX6310UK31D1-T	ABPQ	MAX6312UK48D3-T	ABRG	MAX6312UK37D1-T	ABSW
MAX6310UK42D4-T	ABOB	MAX6310UK31D2-T	ABPR	MAX6312UK48D4-T	ABRH	MAX6312UK37D2-T	ABSX
MAX6310UK41D1-T	ABOC	MAX6310UK31D3-T	ABPS	MAX6312UK47D1-T	ABRI	MAX6312UK37D3-T	ABSY
MAX6310UK41D2-T	ABOD	MAX6310UK31D4-T	ABPT	MAX6312UK47D2-T	ABRJ	MAX6312UK37D4-T	ABSZ
MAX6310UK41D3-T	ABOE	MAX6310UK30D1-T	ABPU	MAX6312UK47D3-T	ABRK	MAX6312UK36D1-T	ABTA
MAX6310UK41D4-T	ABOF	MAX6310UK30D2-T	ABPV	MAX6312UK47D4-T	ABRL	MAX6312UK36D2-T	ABTB
MAX6310UK40D1-T	ABOG	MAX6310UK30D3-T	ABPW	MAX6312UK46D1-T	ABRM	MAX6312UK36D3-T	ABTC
MAX6310UK40D2-T	ABOH	MAX6310UK30D4-T	ABPX	MAX6312UK46D2-T	ABRN	MAX6312UK36D4-T	ABTD
MAX6310UK40D3-T	ABOI	MAX6310UK29D1-T	ABPY	MAX6312UK46D3-T	ABRO	MAX6312UK35D1-T	ABTE
MAX6310UK40D4-T	ABOJ	MAX6310UK29D2-T	ABPZ	MAX6312UK46D4-T	ABRP	MAX6312UK35D2-T	ABTF
MAX6310UK39D1-T	ABOK	MAX6310UK29D3-T	ABQA	MAX6312UK45D1-T	ABRQ	MAX6312UK35D3-T	ABTG
MAX6310UK39D2-T	ABOL	MAX6310UK29D4-T	ABQB	MAX6312UK45D2-T	ABRR	MAX6312UK35D4-T	ABTH
MAX6310UK39D3-T	ABOM	MAX6310UK28D1-T	ABQC	MAX6312UK45D3-T	ABRS	MAX6312UK34D1-T	ABTI
MAX6310UK39D4-T	ABON	MAX6310UK28D2-T	ABQD	MAX6312UK45D4-T	ABRT	MAX6312UK34D2-T	ABTJ
MAX6310UK38D1-T	ABOO	MAX6310UK28D3-T	ABQE	MAX6312UK44D1-T	ABRU	MAX6312UK34D3-T	ABTK
MAX6310UK38D2-T	ABOP	MAX6310UK28D4-T	ABQF	MAX6312UK44D2-T	ABRV	MAX6312UK34D4-T	ABTL
MAX6310UK38D3-T	ABOQ	MAX6310UK27D1-T	ABQG	MAX6312UK44D3-T	ABRW	MAX6312UK33D1-T	ABTM
MAX6310UK38D4-T	ABOR	MAX6310UK27D2-T	ABQH	MAX6312UK44D4-T	ABRX	MAX6312UK33D2-T	ABTN
MAX6310UK37D1-T	ABOS	MAX6310UK27D3-T	ABQI	MAX6312UK43D1-T	ABRY	MAX6312UK33D3-T	ABTO
MAX6310UK37D2-T	ABOT	MAX6310UK27D4-T	ABQJ	MAX6312UK43D2-T	ABRZ	MAX6312UK33D4-T	ABTP
MAX6310UK37D3-T	ABOU	MAX6310UK26D1-T	ABQK	MAX6312UK43D3-T	ABSA	MAX6312UK32D1-T	ABTQ
MAX6310UK37D4-T	ABOV	MAX6310UK26D2-T	ABQL	MAX6312UK43D4-T	ABSB	MAX6312UK32D2-T	ABTR
MAX6310UK36D1-T	ABOW	MAX6310UK26D3-T	ABQM	MAX6312UK42D1-T	ABSC	MAX6312UK32D3-T	ABTS
MAX6310UK36D2-T	ABOX	MAX6310UK26D4-T	ABQN	MAX6312UK42D2-T	ABSD	MAX6312UK32D4-T	ABTT

5-Pin, Multiple-Input, Programmable Reset ICs

Table 2. Device Marking Codes (continued)

DEVICE	CODE	DEVICE	CODE	DEVICE	CODE	DEVICE	CODE
MAX6312UK31D1-T	ABTU	MAX6313UK49D2-T	ABVB	MAX6313UK41D3-T	ABWI	MAX6313UK33D4-T	ABXP
MAX6312UK31D2-T	ABTV	MAX6313UK49D3-T	ABVC	MAX6313UK41D4-T	ABWJ	MAX6313UK32D1-T	ABXQ
MAX6312UK31D3-T	ABTW	MAX6313UK49D4-T	ABVD	MAX6313UK40D1-T	ABWK	MAX6313UK32D2-T	ABXR
MAX6312UK31D4-T	ABTX	MAX6313UK48D1-T	ABVE	MAX6313UK40D2-T	ABWL	MAX6313UK32D3-T	ABXS
MAX6312UK30D1-T	ABTY	MAX6313UK48D2-T	ABVF	MAX6313UK40D3-T	ABWM	MAX6313UK32D4-T	ABXT
MAX6312UK30D2-T	ABTZ	MAX6313UK48D3-T	ABVG	MAX6313UK40D4-T	ABWN	MAX6313UK31D1-T	ABXU
MAX6312UK30D3-T	ABUA	MAX6313UK48D4-T	ABVH	MAX6313UK39D1-T	ABWO	MAX6313UK31D2-T	ABXV
MAX6312UK30D4-T	ABUB	MAX6313UK47D1-T	ABVI	MAX6313UK39D2-T	ABWP	MAX6313UK31D3-T	ABXW
MAX6312UK29D1-T	ABUC	MAX6313UK47D2-T	ABVJ	MAX6313UK39D3-T	ABWQ	MAX6313UK31D4-T	ABXX
MAX6312UK29D2-T	ABUD	MAX6313UK47D3-T	ABVK	MAX6313UK39D4-T	ABWR	MAX6313UK30D1-T	ABXY
MAX6312UK29D3-T	ABUE	MAX6313UK47D4-T	ABVL	MAX6313UK38D1-T	ABWS	MAX6313UK30D2-T	ABXZ
MAX6312UK29D4-T	ABUF	MAX6313UK46D1-T	ABVM	MAX6313UK38D2-T	ABWT	MAX6313UK30D3-T	ABYA
MAX6312UK28D1-T	ABUG	MAX6313UK46D2-T	ABVN	MAX6313UK38D3-T	ABWU	MAX6313UK30D4-T	ABYB
MAX6312UK28D2-T	ABUH	MAX6313UK46D3-T	ABVO	MAX6313UK38D4-T	ABWV	MAX6313UK29D1-T	ABYC
MAX6312UK28D3-T	ABUI	MAX6313UK46D4-T	ABVP	MAX6313UK37D1-T	ABWW	MAX6313UK29D2-T	ABYD
MAX6312UK28D4-T	ABUJ	MAX6313UK45D1-T	ABVQ	MAX6313UK37D2-T	ABWX	MAX6313UK29D3-T	ABYE
MAX6312UK27D1-T	ABUK	MAX6313UK45D2-T	ABVR	MAX6313UK37D3-T	ABWY	MAX6313UK29D4-T	ABYF
MAX6312UK27D2-T	ABUL	MAX6313UK45D3-T	ABVS	MAX6313UK37D4-T	ABWZ	MAX6313UK28D1-T	ABYG
MAX6312UK27D3-T	ABUM	MAX6313UK45D4-T	ABVT	MAX6313UK36D1-T	ABXA	MAX6313UK28D2-T	ABYH
MAX6312UK27D4-T	ABUN	MAX6313UK44D1-T	ABVU	MAX6313UK36D2-T	ABXB	MAX6313UK28D3-T	ABYI
MAX6312UK26D1-T	ABUO	MAX6313UK44D2-T	ABVV	MAX6313UK36D3-T	ABXC	MAX6313UK28D4-T	ABYJ
MAX6312UK26D2-T	ABUP	MAX6313UK44D3-T	ABVW	MAX6313UK36D4-T	ABXD	MAX6313UK27D1-T	ABYK
MAX6312UK26D3-T	ABUQ	MAX6313UK44D4-T	ABVX	MAX6313UK35D1-T	ABXE	MAX6313UK27D2-T	ABYL
MAX6312UK26D4-T	ABUR	MAX6313UK43D1-T	ABVY	MAX6313UK35D2-T	ABXF	MAX6313UK27D3-T	ABYM
MAX6312UK25D1-T	ABUS	MAX6313UK43D2-T	ABVZ	MAX6313UK35D3-T	ABXG	MAX6313UK27D4-T	ABYN
MAX6312UK25D2-T	ABUT	MAX6313UK43D3-T	ABWA	MAX6313UK35D4-T	ABXH	MAX6313UK26D1-T	ABYO
MAX6312UK25D3-T	ABUU	MAX6313UK43D4-T	ABWB	MAX6313UK34D1-T	ABXI	MAX6313UK26D2-T	ABYP
MAX6312UK25D4-T	ABUV	MAX6313UK42D1-T	ABWC	MAX6313UK34D2-T	ABXJ	MAX6313UK26D3-T	ABYQ
MAX6313UK50D1-T	ABUW	MAX6313UK42D2-T	ABWD	MAX6313UK34D3-T	ABXK	MAX6313UK26D4-T	ABYR
MAX6313UK50D2-T	ABUX	MAX6313UK42D3-T	ABWE	MAX6313UK34D4-T	ABXL	MAX6313UK25D1-T	ABYS
MAX6313UK50D3-T	ABUY	MAX6313UK42D4-T	ABWF	MAX6313UK33D1-T	ABXM	MAX6313UK25D2-T	ABYT
MAX6313UK50D4-T	ABUZ	MAX6313UK41D1-T	ABWG	MAX6313UK33D2-T	ABXN	MAX6313UK25D3-T	ABYU
MAX6313UK49D1-T	ABVA	MAX6313UK41D2-T	ABWH	MAX6313UK33D3-T	ABXO	MAX6313UK25D4-T	ABYV

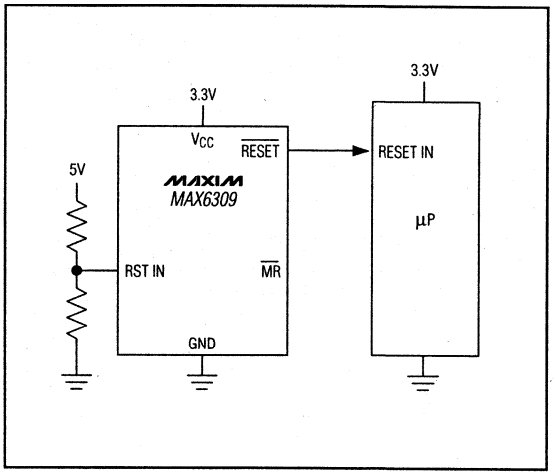
5-Pin, Multiple-Input, Programmable Reset ICs

Ordering Information (continued)

PART†	TEMP. RANGE	PIN-PACKAGE
MAX6308UK00D_-T	0°C to +70°C	5 SOT23-5
MAX6309UK_ _D_-T	0°C to +70°C	5 SOT23-5
MAX6310UK_ _D_-T	0°C to +70°C	5 SOT23-5
MAX6311UK00D_-T	0°C to +70°C	5 SOT23-5
MAX6312UK_ _D_-T	0°C to +70°C	5 SOT23-5
MAX6313UK_ _D_-T	0°C to +70°C	5 SOT23-5

† *The MAX6306/MAX6307/MAX6309/MAX6310/MAX6312/MAX6313 are available with factory-set V_{CC} reset thresholds from 2.5V to 5V, in 0.1V increments. Insert the desired nominal reset threshold (from Table 1) into the blanks following the letters UK. All parts also offer factory-programmed reset timeout periods. Insert the number corresponding to the desired nominal timeout period index following the "D" in the part number (D1 = 1ms min, D2 = 20ms min, D3 = 140ms min, and D4 = 1120ms min). Contact factory for availability and minimum order sizes.*

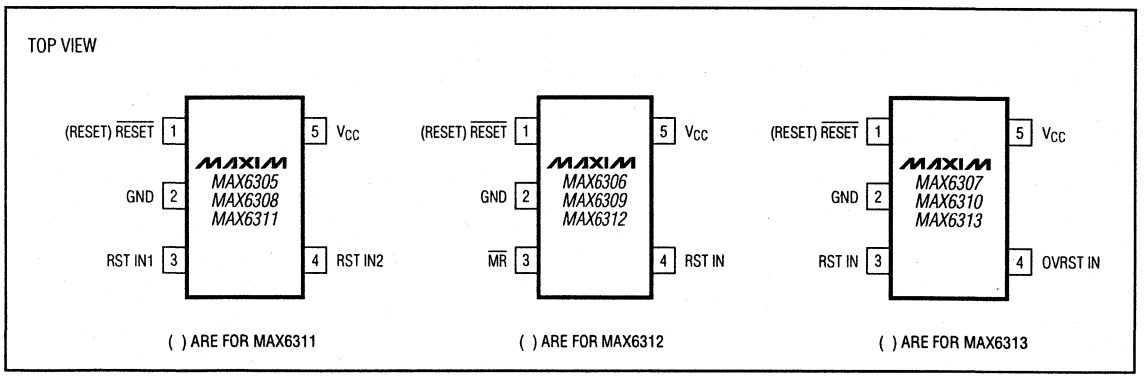
Typical Operating Circuit



Chip Information

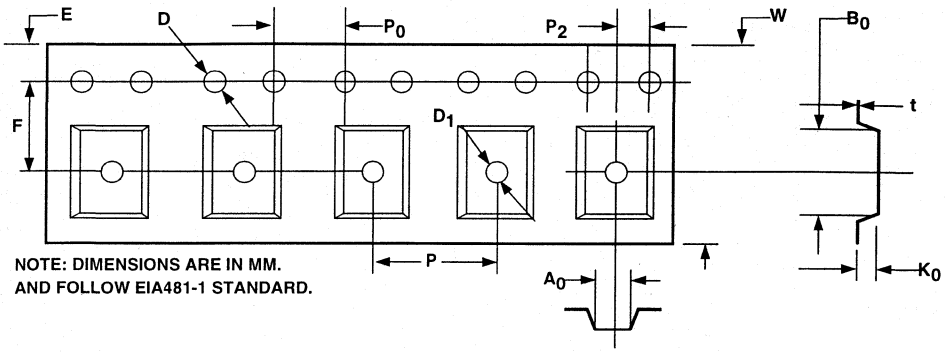
TRANSISTOR COUNT: 800

Pin Configurations



5-Pin, Multiple-Input, Programmable Reset ICs

Tape-and-Reel Information



NOTE: DIMENSIONS ARE IN MM.
AND FOLLOW EIA481-1 STANDARD.

A_0	3.200	±0.102
B_0	3.099	±0.102
D	1.499	+0.102 +0.000
D_1	0.991	+0.254 +0.000

E	1.753	±0.102
F	3.505	±0.051
K_0	1.397	±0.102
P	3.988	±0.102

P_0	3.988	±0.102
$P_0$10	40.005	±0.203
P_2	2.007	±0.051
t	0.254	±0.127
W	8.001	+0.305 -0.102

5 SOT23-5

19-1090; Rev 0; 6/96

MAXIM

68HC11/Bidirectional-Compatible µP Reset Circuit

General Description

The MAX6314 low-power CMOS microprocessor (µP) supervisory circuit is designed to monitor power supplies in µP and digital systems. The MAX6314's $\overline{\text{RESET}}$ output is bidirectional, allowing it to be directly connected to µPs with bidirectional reset inputs, such as the 68HC11. It provides excellent circuit reliability and low cost by eliminating external components and adjustments. The MAX6314 also provides a debounced manual reset input.

This device performs a single function: it asserts a reset signal whenever the V_{CC} supply voltage falls below a preset threshold or whenever manual reset is asserted. Reset remains asserted for an internally programmed interval (reset timeout period) after V_{CC} has risen above the reset threshold or manual reset is deasserted.

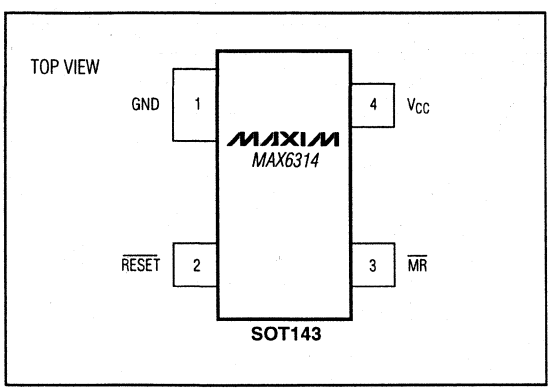
The MAX6314 comes with factory-trimmed reset threshold voltages in 100mV increments from 2.5V to 5V. Preset timeout periods of 1ms, 20ms, 140ms, and 1120ms (minimum) are also available. The device comes in a SOT143 package.

For a µP supervisor with an open-drain reset pin, see the MAX6315 data sheet.

Applications

Computers
Controllers
Intelligent Instruments
Critical µP and µC Power Monitoring
Portable/Battery-Powered Equipment

Pin Configuration



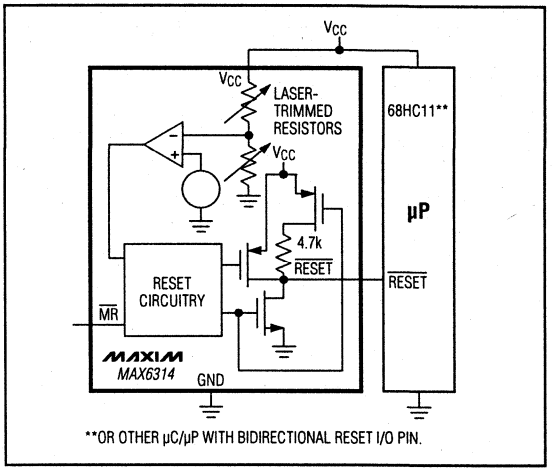
* Patents Pending

Features

- **Small SOT143 Package**
- **$\overline{\text{RESET}}$ Output Simplifies Interface to Bidirectional Reset I/Os**
- **Precision Factory-Set V_{CC} Reset Thresholds: 100mV Increments from 2.5V to 5V**
- **±1.8% Reset Threshold Accuracy at T_A = +25°C**
- **±2.5% Reset Threshold Accuracy Over Temp.**
- **Four Reset Timeout Periods Available: 1ms, 20ms, 140ms, or 1120ms (minimum)**
- **Immune to Short V_{CC} Transients**
- **5µA Supply Current**
- **Pin Compatible with MAX811**

Ordering and Marking Information appear at end of data sheet.

Typical Operating Circuit



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

68HC11/Bidirectional-Compatible µP Reset Circuit

ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... -0.3V to +6.0V
All Other Pins ..... -0.3V to (V_{CC} + 0.3V)
Input Current (V_{CC}) 20mA
Output Current ($\overline{RESET}$) 20mA
Rate of Rise (V_{CC}) 100V/µs

Continuous Power Dissipation (T_A = +70°C)
SOT143 (derate 4mW/°C above +70°C) 320mW
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.5V to +5.5V, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}	T_A = 0°C to +70°C	1.0		5.5	V
V_{CC} Supply Current	I_{CC}	V_{CC} = 5.5V, no load		5	12	µA
		V_{CC} = 3.6V, no load		4	10	
Reset Threshold (Note 1)	V_{TH}	T_A = +25°C	V_{TH} - 1.8%	V_{TH}	V_{TH} + 1.8%	V
		T_A = 0°C to +70°C	V_{TH} - 2.5%		V_{TH} + 2.5%	
Reset Threshold Tempco	ΔV_{TH}/°C			60		ppm/°C
V_{CC} to Reset Delay		V_{CC} = falling at 1mV/µs		35		µs
Reset Timeout Period	t_{RP}	MAX6314US_ _D1-T	1	1.4	2	ms
		MAX6314US_ _D2-T	20	28	40	
		MAX6314US_ _D3-T	140	200	280	
		MAX6314US_ _D4-T	1120	1570	2240	
MANUAL RESET INPUT						
$\overline{MR}$ Input Threshold	V_{IL}	V_{TH} > 4.0V	0.8			V
	V_{IH}				2.4	
	V_{IL}	V_{TH} < 4.0V	0.3 x V_{CC}			
	V_{IH}				0.7 x V_{CC}	
$\overline{MR}$ Minimum Input Pulse			1			µs
$\overline{MR}$ Glitch Rejection				100		ns
$\overline{MR}$ to Reset Delay				500		ns
$\overline{MR}$ Pull-Up Resistance			32	63	100	kΩ
$\overline{RESET}$ Output Voltage	V_{OL}	V_{CC} > 4.25V, I_{SINK} = 3.2mA			0.4	V
		V_{CC} > 2.5V, I_{SINK} = 1.2mA			0.3	
		V_{CC} > 1.2V, I_{SINK} = 0.5mA			0.3	
		V_{CC} > 1.0V, I_{SINK} = 80µA			0.3	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.5V to +5.5V, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{RESET}$ INTERNAL PULL-UP							
Transition Flip-Flop Setup Time (Note 2)	t_S				400		ns
Active Pull-Up Enable Threshold		V_{CC} = 5V		0.4		0.9	V
$\overline{RESET}$ Active Pull-Up Current		V_{CC} = 5V			20		mA
$\overline{RESET}$ Pull-Up Resistance				4.2	4.7	5.2	kΩ
$\overline{RESET}$ Output Rise Time (Note 3)	t_R	V_{CC} = 3V	C_{LOAD} = 120pF			333	ns
			C_{LOAD} = 250pF			666	
		V_{CC} = 5V	C_{LOAD} = 200pF			333	
			C_{LOAD} = 400pF			666	

Note 1: The MAX6314 monitors V_{CC} through an internal, factory-trimmed voltage divider that programs the nominal reset threshold. Factory-trimmed reset thresholds are available in 100mV increments from 2.5V to 5V (see *Ordering and Marking Information*).

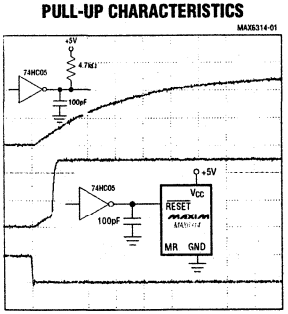
Note 2: This is the minimum time $\overline{RESET}$ must be held low by an external pull-down source to set the active pull-up flip-flop.

Note 3: Measured from $\overline{RESET}$ V_{OL} to (0.8 x V_{CC}), R_{LOAD} = ∞.

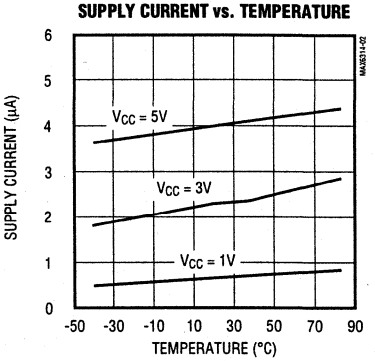
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

PULL-UP CHARACTERISTICS



SUPPLY CURRENT vs. TEMPERATURE

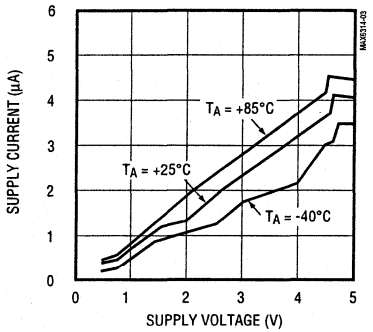


68HC11/Bidirectional-Compatible µP Reset Circuit

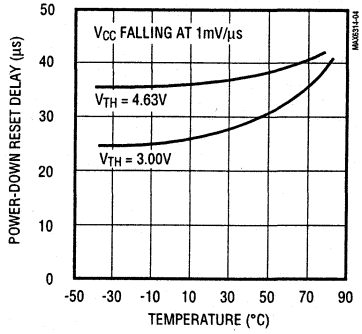
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

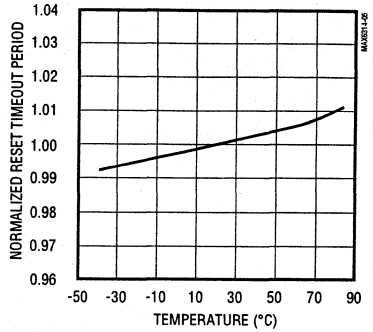
SUPPLY CURRENT vs. SUPPLY VOLTAGE



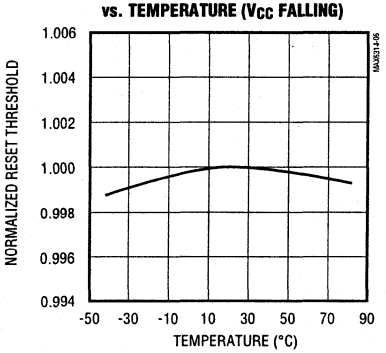
POWER-DOWN RESET DELAY vs. TEMPERATURE



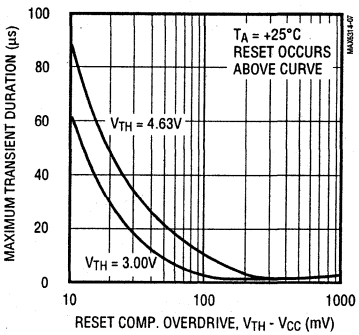
NORMALIZED RESET TIMEOUT PERIOD vs. TEMPERATURE (V_{CC} RISING)



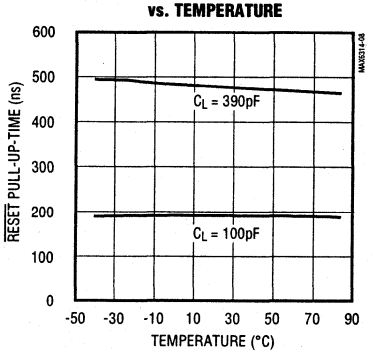
NORMALIZED RESET THRESHOLD vs. TEMPERATURE (V_{CC} FALLING)



MAXIMUM TRANSIENT DURATION vs. RESET COMPARATOR OVERDRIVE



$\overline{\text{RESET}}$ PULL-UP TIME vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1	GND	Ground
2	$\overline{\text{RESET}}$	Active-Low Complementary Output. In addition to the normal N-channel pull-down, $\overline{\text{RESET}}$ has a P-channel pull-up transistor in parallel with a 4.7kΩ resistor to facilitate connection to µPs with bidirectional resets. See the *Reset Output* section.
3	$\overline{\text{MR}}$	Manual Reset Input. A logic low on $\overline{\text{MR}}$ asserts reset. Reset remains asserted as long as $\overline{\text{MR}}$ is low, and for the reset timeout period (t_{RP}) after the reset conditions are terminated. Connect to V_{CC} if not used.
4	V_{CC}	Supply Voltage and Reset Threshold Monitor Input

68HC11/Bidirectional-Compatible µP Reset Circuit

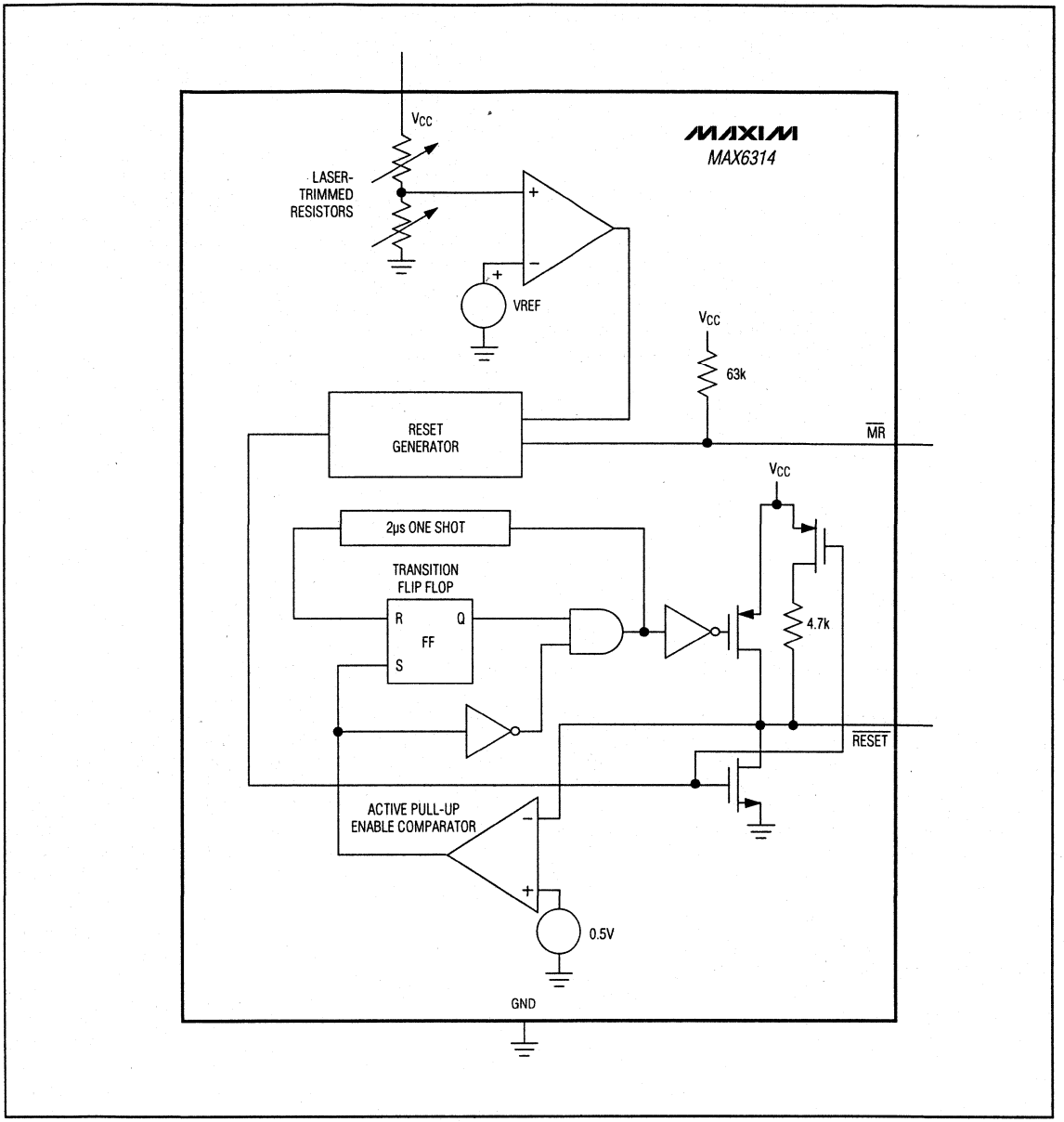


Figure 1. Functional Diagram

68HC11/Bidirectional-Compatible µP Reset Circuit

Detailed Description

The MAX6314 has a reset output consisting of a 4.7kΩ pull-up resistor in parallel with a P-channel transistor and an N-channel pull down (Figure 1), allowing this IC to directly interface with microprocessors (µPs) that have bidirectional reset pins (see the *Reset Output* section).

Reset Output

A µP's reset input starts the µP in a known state. The MAX6314 asserts reset to prevent code-execution errors during power-up, power-down, or brownout conditions. $\overline{RESET}$ is guaranteed to be a logic low for V_{CC} > 1V (see the *Electrical Characteristics*). Once V_{CC} exceeds the reset threshold, the internal timer keeps reset asserted for the reset timeout period (t_{RP}); after this interval $\overline{RESET}$ goes high. If a brownout condition occurs (monitored voltage dips below its programmed reset threshold), $\overline{RESET}$ goes low. Any time V_{CC} dips below the reset threshold, the internal timer resets to zero and $\overline{RESET}$ goes low. The internal timer starts when V_{CC} returns above the reset threshold, and $\overline{RESET}$ remains low for the reset timeout period.

The MAX6314's $\overline{RESET}$ output is designed to interface with µPs that have bidirectional reset pins, such as the Motorola 68HC11. Like an open-drain output, the MAX6314 allows the µP or other devices to pull $\overline{RESET}$ low and assert a reset condition. However, unlike a standard open-drain output, it includes the commonly specified 4.7kΩ pull-up resistor with a P-channel active pull-up in parallel.

This configuration allows the MAX6314 to solve a problem associated with µPs that have bidirectional reset pins in systems where several devices connect to $\overline{RESET}$. These µPs can often determine if a reset was asserted by an external device (i.e., the supervisor IC) or by the µP itself (due to a watchdog fault, clock error, or other source), and then jump to a vector appropriate for the source of the reset. However, if the µP does assert reset, it does not retain the information, but must determine the cause after the reset has occurred.

The following procedure describes how this is done with the Motorola 68HC11. In all cases of reset, the µP pulls $\overline{RESET}$ low for about four E-clock cycles. It then releases $\overline{RESET}$, waits for two E-clock cycles, then checks $\overline{RESET}$'s state. If $\overline{RESET}$ is still low, the µP concludes that the source of the reset was external and, when $\overline{RESET}$ eventually reaches the high state, jumps to the normal reset vector. In this case, stored state information is erased and processing begins from scratch. If, on the other hand, $\overline{RESET}$ is high after the two E-clock cycle delay, the processor knows that it caused the reset itself and can jump to a different vector and use stored state information to determine what caused the reset.

The problem occurs with faster µPs; two E-clock cycles is only 500ns at 4MHz. When there are several devices on the reset line, the input capacitance and stray capacitance can prevent $\overline{RESET}$ from reaching the logic-high state (0.8 x V_{CC}) in the allowed time if only a passive pull-up resistor is used. In this case, all resets will be interpreted as external. The µP is guaranteed to sink only 1.6mA, so the rise time cannot be much reduced by decreasing the recommended 4.7kΩ pull-up resistance.

The MAX6314 solves this problem by including a pull-up transistor in parallel with the recommended 4.7kΩ resistor (Figure 1). The pull-up resistor holds the output high until $\overline{RESET}$ is forced low by the µP reset I/O, or by the MAX6314 itself. Once $\overline{RESET}$ goes below 0.5V, a comparator sets the transition edge flip-flop, indicating that the next transition for $\overline{RESET}$ will be low to high. As soon as $\overline{RESET}$ is released, the 4.7kΩ resistor pulls $\overline{RESET}$ up toward V_{CC}. When $\overline{RESET}$ rises above 0.5V, the active P-channel pull-up turns on for the 2µs duration of the one-shot. The parallel combination of the 4.7kΩ pull-up and the P-channel transistor on-resistance quickly charges stray capacitance on the reset line, allowing $\overline{RESET}$ to transition low to high within the required two E-clock period, even with several devices on the reset line (Figure 2). Once the one-shot times out, the P-channel transistor turns off. This process occurs regardless of whether the reset was caused by V_{CC} dipping below the reset threshold, $\overline{MR}$ being asserted, or the µP or other device asserting $\overline{RESET}$. Because the MAX6314 includes the standard 4.7kΩ pull-up resistor, no external pull-up resistor is required. To minimize current consumption, the internal pull-up resistor is disconnected whenever the MAX6314 asserts $\overline{RESET}$.

Manual Reset Input

Many µP-based products require manual reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. A logic low on $\overline{MR}$ asserts reset. Reset remains asserted while $\overline{MR}$ is low, and for the reset active timeout period after $\overline{MR}$ returns high. To minimize current consumption, the internal 4.7kΩ pull-up resistor on $\overline{RESET}$ is disconnected whenever $\overline{RESET}$ is asserted.

68HC11/Bidirectional-Compatible µP Reset Circuit

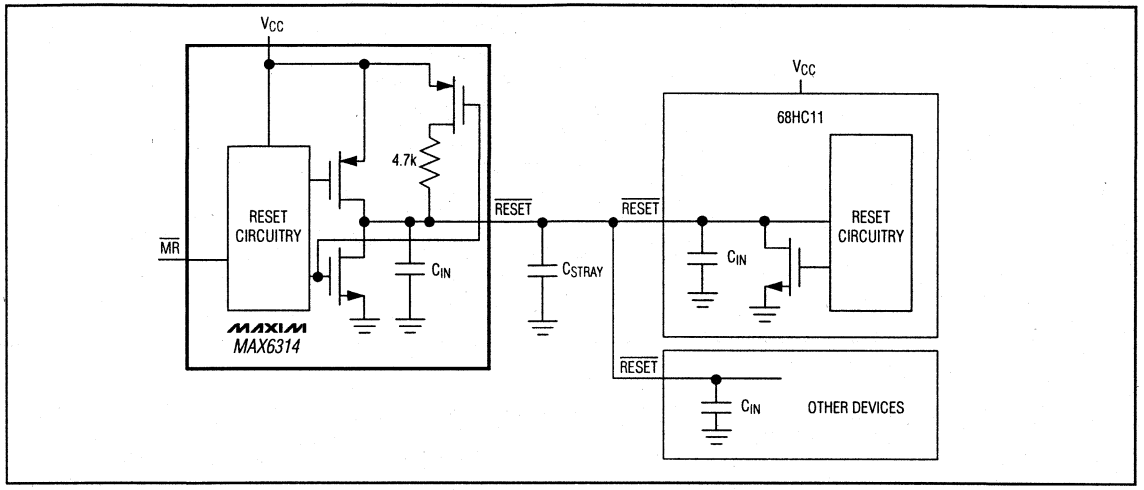


Figure 2. MAX6314 Supports Additional Devices on the Reset Bus

$\overline{MR}$ has an internal 63kΩ pull-up resistor, so it can be left open if not used. Connect a normally open momentary switch from $\overline{MR}$ to GND to create a manual reset function; external debounce circuitry is not required. If $\overline{MR}$ is driven from long cables or if the device is used in a noisy environment, connecting a 0.1µF capacitor from $\overline{MR}$ to ground provides additional noise immunity.

Applications Information

Negative-Going VCC Transients

In addition to issuing a reset to the µP during power-up, power-down, and brownout conditions, these devices are relatively immune to short-duration negative-going transients (glitches). *The Typical Operating Characteristics* show the Maximum Transient Duration vs. Reset Threshold Overdrive, for which reset pulses are not generated. The graph was produced using negative-going pulses, starting at V_{RST} max and ending below the programmed reset threshold by the magnitude indicated (reset threshold overdrive). The graph shows the maximum pulse width that a negative-going V_{CC} transient may typically have without causing a reset pulse to be issued. As the amplitude of the transient increases (i.e., goes farther below the reset threshold), the maximum allowable pulse width decreases. A 0.1µF bypass capacitor mounted close to V_{CC} provides additional transient immunity.

Ensuring a Valid $\overline{RESET}$ Output Down to VCC = 0V

When V_{CC} falls below 1V, $\overline{RESET}$ no longer sinks current—it becomes an open circuit. Therefore, high-impedance CMOS-logic inputs connected to $\overline{RESET}$ can drift to undetermined voltages. This presents no problem in most applications, since most µP and other circuitry is inoperative with V_{CC} below 1V. However, in applications where $\overline{RESET}$ must be valid down to V_{CC} = 0V, adding a pull-down resistor to $\overline{RESET}$ will cause any stray leakage currents to flow to ground, holding $\overline{RESET}$ low (Figure 3). R1's value is not critical; 100kΩ is large enough not to load $\overline{RESET}$ and small enough to pull $\overline{RESET}$ to ground.

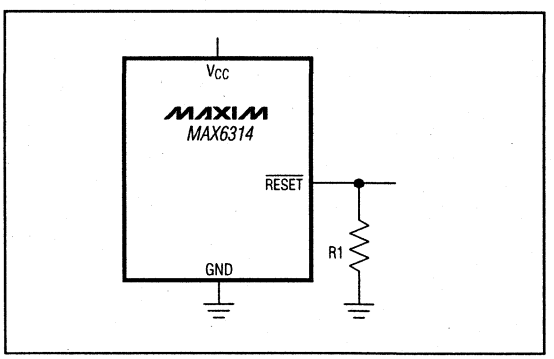


Figure 3. $\overline{RESET}$ Valid to V_{CC} = Ground Circuit

68HC11/Bidirectional-Compatible µP Reset Circuit

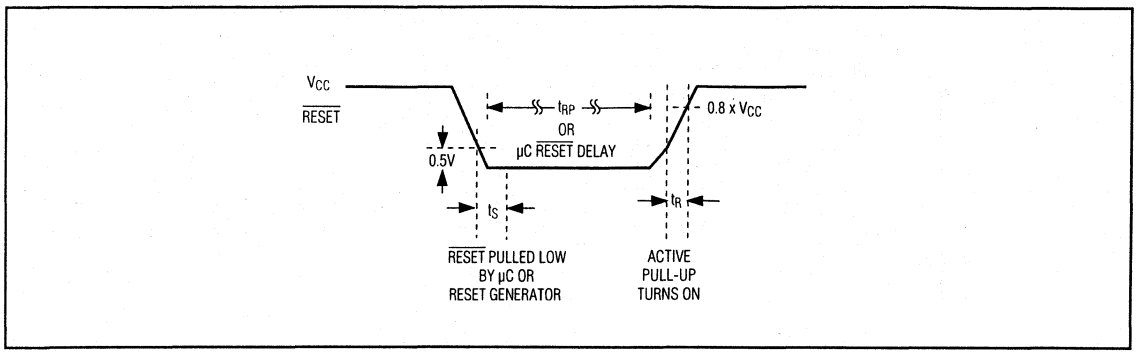


Figure 4. RESET Timing Diagram

Ordering and Marking Information

PART†	NOMINAL V_{TH} (V)	MIN t_{RP} (ms)	PKG. TOP MARK††
MAX6314US50D1-T	5.00	1	AA_ _
MAX6314US49D1-T	4.90	1	AB_ _
MAX6314US48D1-T	4.80	1	AC_ _
MAX6314US47D1-T	4.70	1	AD_ _
MAX6314US46D1-T	4.63	1	AE_ _
MAX6314US45D1-T	4.50	1	AF_ _
MAX6314US44D1-T†††	4.39	1	AG_ _
MAX6314US43D1-T	4.30	1	AH_ _
MAX6314US42D1-T	4.20	1	AI_ _
MAX6314US41D1-T	4.10	1	AJ_ _
MAX6314US40D1-T	4.00	1	AK_ _
MAX6314US39D1-T	3.90	1	AL_ _
MAX6314US38D1-T	3.80	1	CA_ _
MAX6314US37D1-T	3.70	1	CB_ _
MAX6314US36D1-T	3.60	1	CC_ _
MAX6314US35D1-T	3.50	1	CD_ _
MAX6314US34D1-T	3.40	1	CE_ _
MAX6314US33D1-T	3.30	1	CF_ _
MAX6314US32D1-T	3.20	1	CG_ _
MAX6314US31D1-T	3.08	1	CH_ _
MAX6314US30D1-T	3.00	1	CI_ _
MAX6314US29D1-T	2.93	1	CJ_ _

PART†	NOMINAL V_{TH} (V)	MIN t_{RP} (ms)	PKG. TOP MARK††
MAX6314US28D1-T	2.80	1	CK_ _
MAX6314US27D1-T	2.70	1	CL_ _
MAX6314US26D1-T†††	2.63	1	CM_ _
MAX6314US25D1-T	2.50	1	CN_ _
MAX6314US50D2-T	5.00	20	CO_ _
MAX6314US49D2-T	4.90	20	CP_ _
MAX6314US48D2-T	4.80	20	CQ_ _
MAX6314US47D2-T	4.70	20	CR_ _
MAX6314US46D2-T	4.63	20	CS_ _
MAX6314US45D2-T	4.50	20	CT_ _
MAX6314US44D2-T†††	4.39	20	CU_ _
MAX6314US43D2-T	4.30	20	CV_ _
MAX6314US42D2-T	4.20	20	CW_ _
MAX6314US41D2-T	4.10	20	CX_ _
MAX6314US40D2-T	4.00	20	CY_ _
MAX6314US39D2-T	3.90	20	CZ_ _
MAX6314US38D2-T	3.80	20	DA_ _
MAX6314US37D2-T	3.70	20	DB_ _
MAX6314US36D2-T	3.60	20	DC_ _
MAX6314US35D2-T	3.50	20	DD_ _
MAX6314US34D2-T	3.40	20	DE_ _
MAX6314US33D2-T	3.30	20	DJ_ _

†*The MAX6314 is available in a SOT143 package, 0°C to +70°C temperature range.*
††*The first two letters in the package top mark identify the part, while the remaining two letters are the lot tracking code.*
†††*Sample stocks generally held on the bolded products; also, the bolded products have lower minimum-order quantities. Contact factory for details.*

NOTE: All devices available in tape-and-reel only. Contact factory for availability.

68HC11/Bidirectional-Compatible µP Reset Circuit

Ordering and Marking Information (continued)

PART†	NOMINAL V_{TH} (V)	MIN t_{RP} (ms)	PKG. TOP MARK††
MAX6314US32D2-T	3.20	20	DK_ _
MAX6314US31D2-T	3.08	20	DL_ _
MAX6314US30D2-T	3.00	20	DM_ _
MAX6314US29D2-T	2.93	20	DN_ _
MAX6314US28D2-T	2.80	20	DO_ _
MAX6314US27D2-T	2.70	20	DP_ _
MAX6314US26D2-T†††	2.63	20	DQ_ _
MAX6314US25D2-T	2.50	20	DR_ _
MAX6314US50D3-T	5.00	140	DS_ _
MAX6314US49D3-T	4.90	140	DT_ _
MAX6314US48D3-T	4.80	140	DU_ _
MAX6314US47D3-T	4.70	140	DV_ _
MAX6314US46D3-T†††	4.63	140	DW_ _
MAX6314US45D3-T	4.50	140	DX_ _
MAX6314US44D3-T†††	4.39	140	DY_ _
MAX6314US43D3-T	4.30	140	DZ_ _
MAX6314US42D3-T	4.20	140	EA_ _
MAX6314US41D3-T	4.10	140	EB_ _
MAX6314US40D3-T	4.00	140	EC_ _
MAX6314US39D3-T	3.90	140	EG_ _
MAX6314US38D3-T	3.80	140	EH_ _
MAX6314US37D3-T	3.70	140	EI_ _
MAX6314US36D3-T	3.60	140	EJ_ _
MAX6314US35D3-T	3.50	140	EK_ _
MAX6314US34D3-T	3.40	140	EL_ _
MAX6314US33D3-T	3.30	140	EM_ _
MAX6314US32D3-T	3.20	140	EN_ _
MAX6314US31D3-T†††	3.08	140	EO_ _
MAX6314US30D3-T	3.00	140	EP_ _
MAX6314US29D3-T†††	2.93	140	ES_ _

PART†	NOMINAL V_{TH} (V)	MIN t_{RP} (ms)	PKG. TOP MARK††
MAX6314US28D3-T	2.80	140	ET_ _
MAX6314US27D3-T	2.70	140	EU_ _
MAX6314US26D3-T†††	2.63	140	EV_ _
MAX6314US25D3-T	2.50	140	EW_ _
MAX6314US50D4-T	5.00	1120	EX_ _
MAX6314US49D4-T	4.90	1120	EY_ _
MAX6314US48D4-T	4.80	1120	EZ_ _
MAX6314US47D4-T	4.70	1120	FA_ _
MAX6314US46D4-T	4.63	1120	FB_ _
MAX6314US45D4-T	4.50	1120	FC_ _
MAX6314US44D4-T†††	4.39	1120	FD_ _
MAX6314US43D4-T	4.30	1120	FE_ _
MAX6314US42D4-T	4.20	1120	FF_ _
MAX6314US41D4-T	4.10	1120	FG_ _
MAX6314US40D4-T	4.00	1120	FH_ _
MAX6314US39D4-T	3.90	1120	FI_ _
MAX6314US38D4-T	3.80	1120	FJ_ _
MAX6314US37D4-T	3.70	1120	FK_ _
MAX6314US36D4-T	3.60	1120	FL_ _
MAX6314US35D4-T	3.50	1120	FM_ _
MAX6314US34D4-T	3.40	1120	FN_ _
MAX6314US33D4-T	3.30	1120	FO_ _
MAX6314US32D4-T	3.20	1120	FP_ _
MAX6314US31D4-T	3.08	1120	FQ_ _
MAX6314US30D4-T	3.00	1120	FR_ _
MAX6314US29D4-T	2.93	1120	FS_ _
MAX6314US28D4-T	2.80	1120	FT_ _
MAX6314US27D4-T	2.70	1120	FU_ _
MAX6314US26D4-T†††	2.63	1120	FV_ _
MAX6314US25D4-T	2.50	1120	FW_ _

†The MAX6314 is available in a SOT143 package, 0°C to +70°C temperature range.
††The first two letters in the package top mark identify the part, while the remaining two letters are the lot tracking code.
†††Sample stocks generally held on the bolded products; also, the bolded products have lower minimum-order quantities. Contact factory for details.

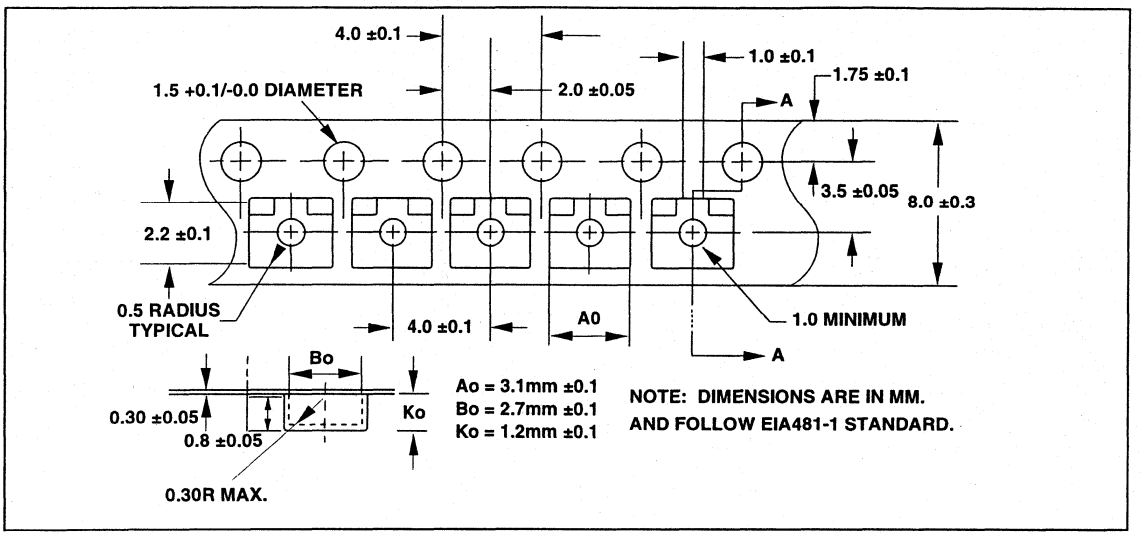
NOTE: All devices available in tape-and-reel only. Contact factory for availability.

68HC11/Bidirectional-Compatible µP Reset Circuit

Chip Information

TRANSISTOR COUNT: 519

Tape-and-Reel Information



19-2000; Rev 0; 6/96

Open-Drain SOT µP Reset Circuit

General Description

The MAX6315 low-power CMOS microprocessor (µP) supervisory circuit is designed to monitor power supplies in µP and digital systems. It provides excellent circuit reliability and low cost by eliminating external components and adjustments. The MAX6315 also provides a debounced manual reset input.

This device performs a single function: it asserts a reset signal whenever the V_{CC} supply voltage falls below a preset threshold or whenever manual reset is asserted. Reset remains asserted for an internally programmed interval (reset timeout period) after V_{CC} has risen above the reset threshold or manual reset is deasserted. The MAX6315's open-drain $\overline{RESET}$ output can be pulled up to a voltage higher than V_{CC}.

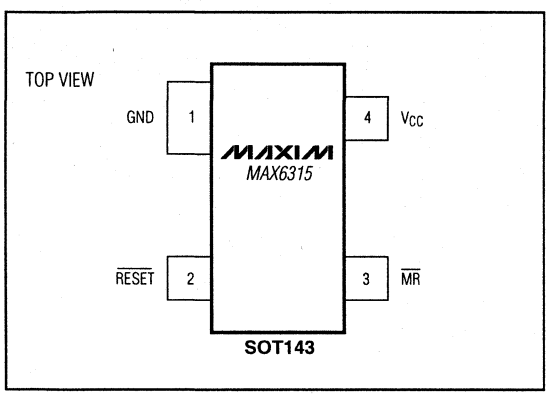
The MAX6315 comes with factory-trimmed reset threshold voltages in 100mV increments from 2.5V to 5V. Preset timeout periods of 1ms, 20ms, 140ms, and 1120ms (minimum) are also available. The device comes in a SOT143 package.

For microcontrollers (µCs) and µPs with bidirectional reset pins, see the MAX6314 data sheet.

Applications

Computers
Controllers
Intelligent Instruments
Critical µP and µC Power Monitoring
Portable/Battery-Powered Equipment

Pin Configuration

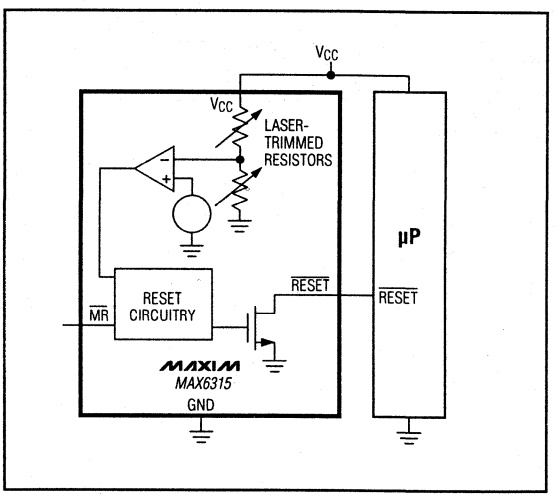


Features

- **Small SOT143 Package**
- **Open-Drain $\overline{RESET}$ Output Can Exceed V_{CC}**
- **Precision, Factory-Set V_{CC} Reset Thresholds: 100mV Increments from 2.5V to 5V**
- **±1.8% Reset Threshold Accuracy at T_A = +25°C**
- **±2.5% Reset Threshold Accuracy Over Temp.**
- **Four Reset Timeout Periods Available: 1ms, 20ms, 140ms, or 1120ms (minimum)**
- **Immune to Short V_{CC} Transients**
- **5µA Supply Current**
- **Pin Compatible with MAX811**

Ordering and Marking Information appear at end of data sheet.

Typical Operating Circuit



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Open-Drain SOT µP Reset Circuit

ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... -0.3V to +6.0V
$\overline{RESET}$ ..... -0.3V to +6.0V
All Other Pins ..... -0.3V to (V_{CC} + 0.3V)
Input Current (V_{CC}) 20mA
Output Current ($\overline{RESET}$) 20mA
Rate of Rise (V_{CC}) 100V/µs

Continuous Power Dissipation (T_A = +70°C)
SOT143 (derate 4mW/°C above +70°C) 320mW
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.5V to +5.5V, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}	T_A = 0°C to +70°C	1.0		5.5	V
V_{CC} Supply Current	I_{CC}	V_{CC} = 5.5V, no load		5	12	µA
		V_{CC} = 3.6V, no load		4	10	
Reset Threshold (Note 1)	V_{TH}	T_A = +25°C	V_{TH} - 1.8%	V_{TH}	V_{TH} + 1.8%	V
		T_A = 0°C to +70°C	V_{TH} - 2.5%		V_{TH} + 2.5%	
Reset Threshold Tempco	ΔV_{TH}/°C			60		ppm/°C
V_{CC} to Reset Delay		V_{CC} = falling at 1mV/µs		35		µs
Reset Timeout Period	t_{RP}	MAX6315US_ _D1-T	1	1.4	2	ms
		MAX6315US_ _D2-T	20	28	40	
		MAX6315US_ _D3-T	140	200	280	
		MAX6315US_ _D4-T	1120	1570	2240	
MANUAL RESET INPUT						
$\overline{MR}$ Input Threshold	V_{IL}	V_{TH} > 4.0V	0.8			V
	V_{IH}				2.4	
	V_{IL}	V_{TH} < 4.0V	0.3 x V_{CC}			
	V_{IH}				0.7 x V_{CC}	
$\overline{MR}$ Minimum Input Pulse			1			µs
$\overline{MR}$ Glitch Rejection				100		ns
$\overline{MR}$ to Reset Delay				500		ns
$\overline{MR}$ Pull-Up Resistance			32	63	100	kΩ
$\overline{RESET}$ Output Voltage	V_{OL}	V_{CC} > 4.25V, I_{SINK} = 3.2mA			0.4	V
		V_{CC} > 2.5V, I_{SINK} = 1.2mA			0.3	
		V_{CC} > 1.2V, I_{SINK} = 0.5mA				
		V_{CC} > 1.0V, I_{SINK} = 80mA			0.3	
$\overline{RESET}$ Output Leakage Current		V_{CC} > V_{TH}, $\overline{RESET}$ deasserted			1	µA

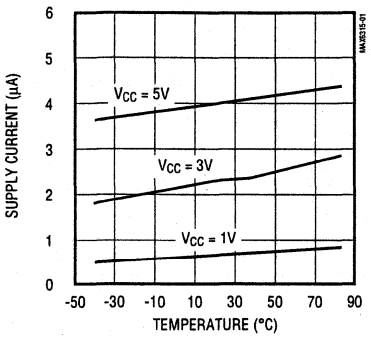
Note 1: The MAX6315 monitors V_{CC} through an internal factory-trimmed voltage divider that programs the nominal reset threshold. Factory-trimmed reset thresholds are available in 100mV increments from 2.5V to 5V (see *Ordering and Marking Information*).

Open-Drain SOT µP Reset Circuit

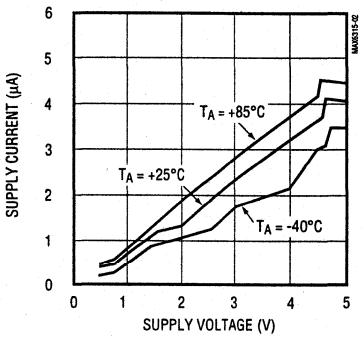
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

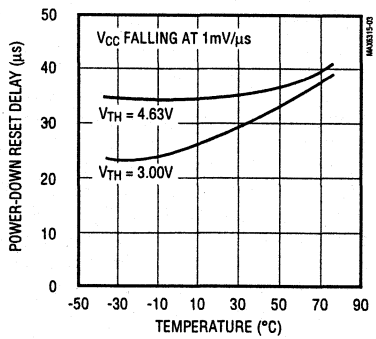
SUPPLY CURRENT vs. TEMPERATURE



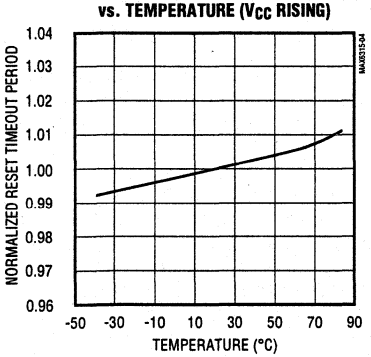
SUPPLY CURRENT vs. SUPPLY VOLTAGE



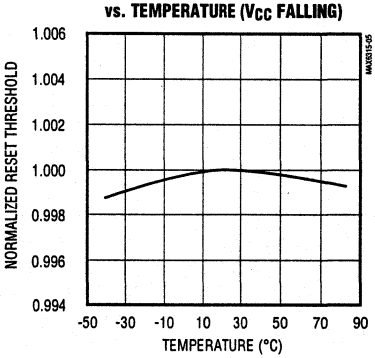
POWER-DOWN RESET DELAY vs. TEMPERATURE



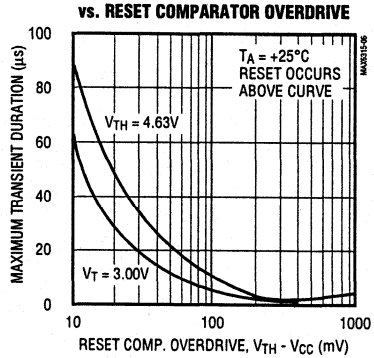
NORMALIZED RESET TIMEOUT PERIOD vs. TEMPERATURE (V_{CC} RISING)



NORMALIZED RESET THRESHOLD vs. TEMPERATURE (V_{CC} FALLING)



MAXIMUM TRANSIENT DURATION vs. RESET COMPARATOR OVERDRIVE



Pin Description

PIN	NAME	FUNCTION
1	GND	Ground
2	$\overline{RESET}$	Active-Low Open-Drain Output. Connect to an external pull-up resistor. Can be pulled up to a voltage higher than V_{CC}, but less than 6V.
3	$\overline{MR}$	Manual Reset Input. A logic low on $\overline{MR}$ asserts reset. Reset remains asserted as long as $\overline{MR}$ is low, and for the reset timeout period (t_{RP}) after the reset conditions are terminated. Connect to V_{CC} if not used.
4	V_{CC}	Supply Voltage and Reset Threshold Monitor Input

Open-Drain SOT µP Reset Circuit

Detailed Description

Reset Output

A microprocessor's (µP's) reset input starts the µP in a known state. The MAX6315 asserts reset to prevent code-execution errors during power-up, power-down, or brownout conditions. $\overline{RESET}$ is guaranteed to be a logic low for V_{CC} > 1V (see *Electrical Characteristics*). Once V_{CC} exceeds the reset threshold, the internal timer keeps reset asserted for the reset timeout period (t_{RP}); after this interval $\overline{RESET}$ goes high. If a brownout condition occurs (monitored voltage dips below its programmed reset threshold), $\overline{RESET}$ goes low. Any time V_{CC} dips below the reset threshold, the internal timer resets to zero and $\overline{RESET}$ goes low. The internal timer starts when V_{CC} returns above the reset threshold, and $\overline{RESET}$ remains low for the reset timeout period.

The MAX6315's $\overline{RESET}$ output structure is a simple open-drain N-channel MOSFET switch. Connect a pull-up resistor to any supply in the 0V to +6V range. Select a resistor value large enough to register a logic low when $\overline{RESET}$ is asserted (see *Electrical Characteristics*), and small enough to register a logic high while supplying all input current and leakage paths connected to the $\overline{RESET}$ line. A 10kΩ pull-up is sufficient in most applications.

Often, the pull-up connected to the MAX6315's $\overline{RESET}$ output will connect to the supply voltage monitored at the IC's V_{CC} pin. However, some systems may use the open-drain output to level-shift from the monitored supply to reset circuitry powered by some other supply (Figure 1). This is one useful feature of an open-drain output. Keep in mind that as the MAX6315's V_{CC} decreases below 1V, so does the IC's ability to sink current at $\overline{RESET}$. Finally, with any pull-up, $\overline{RESET}$ will be pulled high as V_{CC} decays toward 0V. The voltage where this occurs depends on the pull-up resistor value and the voltage to which it connects (see *Electrical Characteristics*).

Manual-Reset Input

Many µP-based products require manual-reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. A logic low on $\overline{MR}$ asserts reset. Reset remains asserted while $\overline{MR}$ is low, and for the reset active timeout period after $\overline{MR}$ returns high.

$\overline{MR}$ has an internal 63kΩ pull-up resistor, so it can be left open if not used. Connect a normally open momentary switch from $\overline{MR}$ to GND to create a manual reset function; external debounce circuitry is not required.

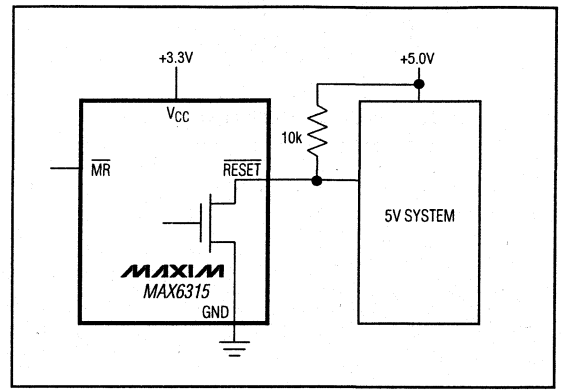


Figure 1. MAX6315 Open-Drain $\overline{RESET}$ Output Allows Use with Multiple Supplies

If $\overline{MR}$ is driven from long cables or if the device is used in a noisy environment, connecting a 0.1µF capacitor from $\overline{MR}$ to ground provides additional noise immunity.

Applications Information

Negative-Going V_{CC} Transients

In addition to issuing a reset to the µP during power-up, power-down, and brownout conditions, these devices are relatively immune to short-duration negative-going transients (glitches). The *Typical Operating Characteristics* show the Maximum Transient Duration vs. Reset Threshold Overdrive, for which reset pulses are not generated. The graph was produced using negative-going pulses, starting at V_{RST} max and ending below the programmed reset threshold by the magnitude indicated (reset threshold overdrive). The graph shows the maximum pulse width that a negative-going V_{CC} transient may typically have without causing a reset pulse to be issued. As the transient amplitude increases (i.e., goes farther below the reset threshold), the maximum allowable pulse width decreases. A 0.1µF bypass capacitor mounted close to V_{CC} provides additional transient immunity.

Open-Drain SOT µP Reset Circuit

Ordering Information

PART†	NOMINAL V_{TH} (V)	MIN t_{RP} (ms)	PKG. TOP MARK††
MAX6315US50D1-T	5.00	1	FX_ _
MAX6315US49D1-T	4.90	1	FY_ _
MAX6315US48D1-T	4.80	1	FZ_ _
MAX6315US47D1-T	4.70	1	GA_ _
MAX6315US46D1-T	4.63	1	GB_ _
MAX6315US45D1-T	4.50	1	GC_ _
MAX6315US44D1-T†††	4.39	1	GD_ _
MAX6315US43D1-T	4.30	1	GE_ _
MAX6315US42D1-T	4.20	1	GF_ _
MAX6315US41D1-T	4.10	1	GG_ _
MAX6315US40D1-T	4.00	1	GH_ _
MAX6315US39D1-T	3.90	1	GI_ _
MAX6315US38D1-T	3.80	1	GJ_ _
MAX6315US37D1-T	3.70	1	GK_ _
MAX6315US36D1-T	3.60	1	GL_ _
MAX6315US35D1-T	3.50	1	GM_ _
MAX6315US34D1-T	3.40	1	GN_ _
MAX6315US33D1-T	3.30	1	GO_ _
MAX6315US32D1-T	3.20	1	GP_ _
MAX6315US31D1-T	3.08	1	GQ_ _
MAX6315US30D1-T	3.00	1	GR_ _
MAX6315US29D1-T	2.93	1	GS_ _
MAX6315US28D1-T	2.80	1	GT_ _
MAX6315US27D1-T	2.70	1	GU_ _
MAX6315US26D1-T†††	2.63	1	GV_ _
MAX6315US25D1-T	2.50	1	GW_ _

PART†	NOMINAL V_{TH} (V)	MIN t_{RP} (ms)	PKG. TOP MARK††
MAX6315US50D2-T	5.00	20	GX_ _
MAX6315US49D2-T	4.90	20	GY_ _
MAX6315US48D2-T	4.80	20	GZ_ _
MAX6315US47D2-T	4.70	20	HA_ _
MAX6315US46D2-T	4.63	20	HB_ _
MAX6315US45D2-T	4.50	20	HC_ _
MAX6315US44D2-T†††	4.39	20	HD_ _
MAX6315US43D2-T	4.30	20	HE_ _
MAX6315US42D2-T	4.20	20	HF_ _
MAX6315US41D2-T	4.10	20	HG_ _
MAX6315US40D2-T	4.00	20	HH_ _
MAX6315US39D2-T	3.90	20	HI_ _
MAX6315US38D2-T	3.80	20	HJ_ _
MAX6315US37D2-T	3.70	20	HK_ _
MAX6315US36D2-T	3.60	20	HL_ _
MAX6315US35D2-T	3.50	20	HM_ _
MAX6315US34D2-T	3.40	20	HN_ _
MAX6315US33D2-T	3.30	20	HO_ _
MAX6315US32D2-T	4.20	20	HP_ _
MAX6315US31D2-T	3.08	20	HQ_ _
MAX6315US30D2-T	3.00	20	HR_ _
MAX6315US29D2-T	2.93	20	HS_ _
MAX6315US28D2-T	2.80	20	HT_ _
MAX6315US27D2-T	2.70	20	HU_ _
MAX6315US26D2-T†††	2.63	20	HV_ _
MAX6315US25D2-T	2.50	20	HW_ _

†The MAX6315 is available in a SOT143 package, 0°C to +70°C temperature range.
††The first two letters in the package top mark identify the part, while the remaining two letters are the lot tracking code.
†††Sample stocks generally held on the bolded products; also, the bolded products have lower minimum-order quantities. Contact factory for details.

NOTE: All devices available in tape-and-reel only. Contact factory for availability.

Open-Drain SOT µP Reset Circuit

Ordering Information (continued)

PART†	NOMINAL V_{TH} (V)	MIN t_{RP} (ms)	PKG. TOP MARK††
MAX6315US50D3-T	5.00	140	HX_ _
MAX6315US49D3-T	4.90	140	HY_ _
MAX6315US48D3-T	4.80	140	HZ_ _
MAX6315US47D3-T	4.70	140	IA_ _
MAX6315US46D3-T†††	4.63	140	IB_ _
MAX6315US45D3-T	4.50	140	IC_ _
MAX6315US44D3-T†††	4.39	140	ID_ _
MAX6315US43D3-T	4.30	140	IE_ _
MAX6315US42D3-T	4.20	140	IF_ _
MAX6315US41D3-T	4.10	140	IG_ _
MAX6315US40D3-T	4.00	140	IH_ _
MAX6315US39D3-T	3.90	140	II_ _
MAX6315US38D3-T	3.80	140	IJ_ _
MAX6315US37D3-T	3.70	140	IK_ _
MAX6315US36D3-T	3.60	140	IL_ _
MAX6315US35D3-T	3.50	140	IM_ _
MAX6315US34D3-T	3.40	140	IN_ _
MAX6315US33D3-T	3.30	140	IO_ _
MAX6315US32D3-T	3.20	140	IP_ _
MAX6315US31D3-T†††	3.08	140	IQ_ _
MAX6315US30D3-T	3.00	140	IR_ _
MAX6315US29D3-T†††	2.93	140	IS_ _
MAX6315US28D3-T	2.80	140	IT_ _
MAX6315US27D3-T	2.70	140	IU_ _
MAX6315US26D3-T†††	2.63	140	IV_ _
MAX6315US25D3-T	2.50	140	IW_ _

PART†	NOMINAL V_{TH} (V)	MIN t_{RP} (ms)	PKG. TOP MARK††
MAX6315US50D4-T	5.00	1120	IX_ _
MAX6315US49D4-T	4.90	1120	IY_ _
MAX6315US48D4-T	4.80	1120	IZ_ _
MAX6315US47D4-T	4.70	1120	JA_ _
MAX6315US46D4-T	4.63	1120	JB_ _
MAX6315US45D4-T	4.50	1120	JC_ _
MAX6315US44D4-T†††	4.39	1120	JD_ _
MAX6315US43D4-T	4.30	1120	JE_ _
MAX6315US42D4-T	4.20	1120	JF_ _
MAX6315US41D4-T	4.10	1120	JG_ _
MAX6315US40D4-T	4.00	1120	JH_ _
MAX6315US39D4-T	3.90	1120	JI_ _
MAX6315US38D4-T	3.80	1120	JJ_ _
MAX6315US37D4-T	3.70	1120	JK_ _
MAX6315US36D4-T	3.60	1120	JL_ _
MAX6315US35D4-T	3.50	1120	JM_ _
MAX6315US34D4-T	3.40	1120	JN_ _
MAX6315US33D4-T	3.30	1120	JO_ _
MAX6315US32D4-T	3.20	1120	JP_ _
MAX6315US31D4-T	3.08	1120	JQ_ _
MAX6315US30D4-T	3.00	1120	JR_ _
MAX6315US29D4-T	2.93	1120	JS_ _
MAX6315US28D4-T	2.80	1120	JT_ _
MAX6315US27D4-T	2.70	1120	JU_ _
MAX6315US26D4-T†††	2.63	1120	JV_ _
MAX6315US25D4-T	2.50	1120	JW_ _

†The MAX6315 is available in a SOT143 package, 0°C to +70°C temperature range.

††The first two letters in the package top mark identify the part, while the remaining two letters are the lot tracking code.

†††Sample stocks generally held on the bolded products; also, the bolded products have lower minimum-order quantities. Contact factory for details.

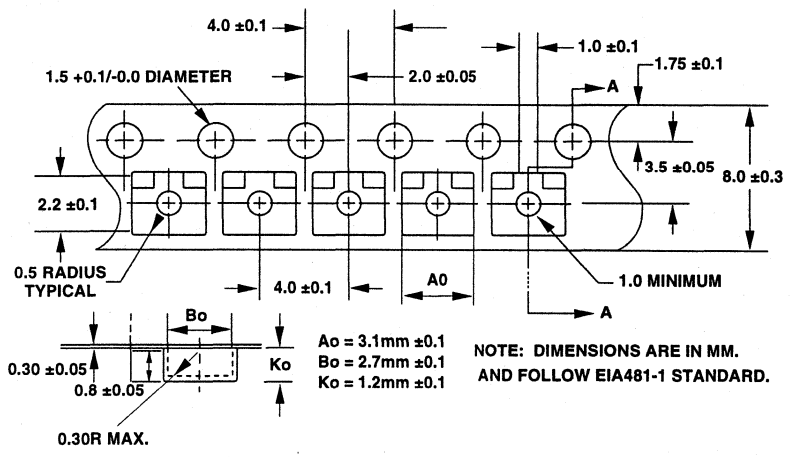
NOTE: All devices available in tape-and-reel only. Contact factory for availability.

Open-Drain SOT µP Reset Circuit

Chip Information

TRANSISTOR COUNT: 519

Tape-and-Reel Information



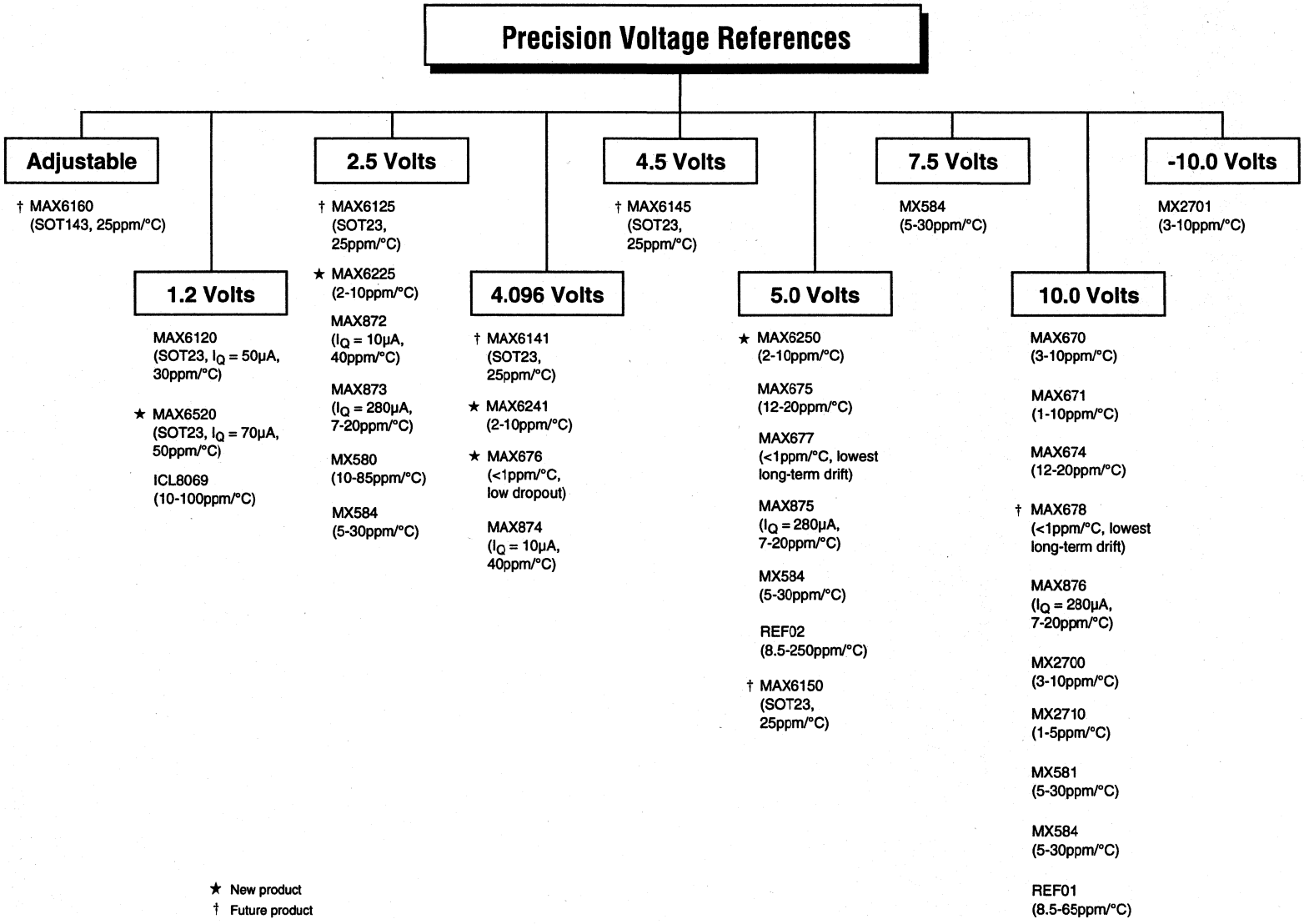
Voltage References

Voltage References, Product Tables and Trees 6-2

MAX6120	Low-Cost, Micropower, Precision 3-Terminal, 1.2V Voltage Reference	6-5
MAX6125	2.5V-Output, Low-Dropout, Micropower, Precision 3-Terminal Voltage Reference	6-11*
MAX6141	4.096V-Output, Low-Dropout, Micropower, Precision 3-Terminal Voltage Reference	6-11*
MAX6145	4.5V-Output, Low-Dropout, Micropower, Precision 3-Terminal Voltage Reference	6-11*
MAX6150	5V-Output, Low-Dropput, Micropower, Precision 3-Terminal Voltage Reference	6-11*
MAX6160	Adjustable-Output, Low-Dropout, Micropower, Precision 3-Terminal Voltage Reference	6-11*
MAX6225	Low-Drift, Low-Noise, 2.5V Precision Voltage Reference	6-13
MAX6241	Low-Drift, Low-Noise, 4.096V Precision Voltage Reference	6-13
MAX6250	Low-Drift, Low-Noise, 5.0V Precision Voltage Reference	6-13
MAX6520	Low-Cost, Micropower, Precision 3-Terminal, 1.2V Voltage Reference	6-23

*Advance Information–first page of data sheet in preparation.

Precision Voltage References



★ New product
† Future product

Part Number	Voltage (V)	Temp. Drift (ppm/°C max)	Initial Accuracy T_A = +25°C (%F.S. max)	Quiescent Current (mA max)	Noise 0.1Hz-10Hz (μV_{p-p}), max(typ)	Package Options[1]	Temp. Ranges[2]	Features	Price† 1000-up ($)
MAX6160	Adj.	50	1	110	TBD	SOT143, SO	E	Low-cost, low-dropout 3-terminal adjustable reference	††
MAX6120	1.2	100 (30 typ)	1	58µA	(10)	SOT23, SO	E	Low-cost, micropower 3-terminal reference	0.80
MAX6520	1.2	50	1	70µA	(10)	SOT23, SO	E	Low-cost, micropower 3-terminal reference; low drift	1.25
ICL8069	1.2	10 to 100	2	0.05	5 (10Hz to 10kHz)	TO-52, TO-92, SO*	C,E,M	Micropower 2-terminal reference	0.65
MAX6125	2.5	50	1	110	TBD	SOT23, SO	E	Low-cost, low-dropout 3-terminal reference	††
MAX6225	2.5	2 to 10	0.04 to 0.2	3	(1.5)	DIP, SO, CERDIP	C,E,M	Low drift, less than 1ppm p-p output noise	2.25
MAX872	2.5	40	0.2	10µA	(60)	DIP, SO	C,E	Lowest power, lowest dropout precision reference. $V_{CC} = V_{OUT} + 200mV$	2.12
MAX873	2.5	7 to 20	0.06 to 0.1	0.28	(16)	DIP, SO	C,E,M	Low power/drift, REF43 upgrade	2.95
MX580	2.5	10 to 85	0.4 to 3	1.5	(60)	TO-52, SO**	C,M	Low-drift bandgap reference	2.33
MX584	2.5	5 to 30	0.05 to 0.3	1	(50)	TO-99, DIP, SO, CERDIP	C,M	Low-drift programmable reference	3.09
MAX6141	4.096	50	1	110	TBD	SOT23, SO	E	Low-cost, low-dropout 3-terminal reference	††
MAX6241	4.096	2 to 10	0.02 to 0.1	3	(2.4)	DIP, SO, CERDIP	C,E,M	Low drift, less than 1ppm p-p output noise	2.25
MAX676	4.096	1 to 3	0.02	10	(1.2)	DIP, SO, CERDIP	C,E,M	Lowest temperature drift in SO package, lowest long-term drift, low dropout	9.03
MAX874	4.096	40	0.2	10µA	(60)	DIP, SO	C,E	Lowest power, lowest dropout precision reference. $V_{CC} = V_{OUT} + 200mV$	2.12
MAX6145	4.5	50	1	120	TBD	SOT23, SO	E	Low-cost, low-dropout 3-terminal reference	††
MAX6150	5.0	50	1	125	TBD	SOT23, SO	E	Low-cost, low-dropout 3-terminal reference	††
MAX6250	5.0	2 to 10	0.02 to 0.1	3	(3)	DIP, SO, CERDIP	C,E,M	Low drift, less than 1ppm p-p output noise	2.25
MAX675	5.0	12 to 20	0.15	1.4	15	TO-99, DIP, SO, CERDIP	C,E,M	Low-drift, low-noise bandgap reference	3.08
MAX677	5.0	1 to 3	0.02	10	(1.5)	DIP, SO, CERDIP	C,E,M	Lowest temperature drift in SO package, lowest long-term drift	9.03
MAX875	5.0	7 to 20	0.06 to 0.1	0.28	(32)	DIP, SO	C,E,M	Low power/drift, REF02 upgrade	2.95
MX584	5.0	5 to 30	0.05 to 0.3	1	(50)	TO-99, DIP, SO, CERDIP	C,M	Low-drift programmable reference	3.09
REF02	5.0	8.5 to 250	0.3 to 2	1.4	15	TO-99, DIP, SO, CERDIP	C,M	Low-drift bandgap reference	1.80
MX584	7.5	5 to 30	0.05 to 0.3	1	(50)	TO-99, DIP, SO, CERDIP	C,M	Low-drift programmable reference	3.09
MAX670	10.0	3 to 10	0.025	14	50	SB Ceramic	E,M	Kelvin connected, ultra-low-drift reference	38.51
MAX671	10.0	1 to 10	0.01	14	50	SB Ceramic	C,E,M	Kelvin connected, ultra-low-drift reference	37.41
MAX674	10.0	12 to 20	0.15	1.4	30	TO-99, DIP, SO, CERDIP	C,E,M	Low-drift, low-noise bandgap reference	3.08
MAX678	10.0	1 to 3	0.02	10	(3)	DIP, SO, CERDIP	C,E,M	Lowest temperature drift in SO package, lowest long-term drift	††
MAX876	10.0	7 to 20	0.06 to 0.1	0.28	(64)	DIP, SO	C,E,M	Low power/drift, REF01 upgrade	2.95
MX2700	10.0	3 to 10	0.025 to 0.05	14	(50)	SB Ceramic	I,M	Ultra-low-drift voltage reference	19.61
MX2710	10.0	1 to 5	0.01	14	(30)	SB Ceramic	C	Ultra-low-drift voltage reference	24.74
MX581	10.0	5 to 30	0.05 to 0.3	1	(50)	TO-39, SO***	C,M	Low-drift bandgap reference	2.90
MX584	10.0	5 to 30	0.05 to 0.3	1	(50)	TO-99, DIP, SO, CERDIP	C,M	Low-drift programmable reference	3.09
REF01	10.0	8.5 to 65	0.3 to 1	1.4	30	TO-99, DIP, SO, CERDIP	C,M	Low-drift bandgap reference	2.05
MX2701	-10.0	3 to 10	0.025 to 0.05	14	(50)	SB Ceramic	I,M	Ultra-low-drift voltage reference	24.02

* The ICL8069 is available in 2-pin TO-52, 2-pin TO-92, and 8-pin SO packages.
** The MX580 is available in 3-pin TO-52 and 8-pin SO packages.
*** The MX581 is available in 3-pin TO-39 and 8-pin SO packages.
1 Package Options: DIP = Dual-In-Line Package, PLCC = Plastic Leadless Chip Carrier (quad pack), FP = Flat Pack
2 Temp Ranges: C = 0°C to +70°C, I = -25°C to +85°C, E = -40°C to +85°C, M = -55°C to +125°C
† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future product—contact factory for pricing and availability. Specifications are preliminary.

19-0458; Rev 1; 9/96

MAXIM

Low-Cost, Micropower, Precision, 3-Terminal, 1.2V Voltage Reference

General Description

The MAX6120 is the lowest-power 1.2V, precision, three-terminal voltage reference offered in a SOT23 package. Ideal for 3V battery-powered equipment where power conservation is critical, the MAX6120 is a low-power alternative to existing two-terminal shunt references. Unlike two-terminal references that throw away battery current and require an external series resistor, the MAX6120 has a 70µA maximum supply current (typically only 50µA) that is independent of the input voltage. This feature translates to maximum efficiency at all battery voltages.

The MAX6120 operates from a supply voltage as low as 2.4V, and initial accuracy is ±1% for the SOT23 package. Output voltage temperature coefficient is typically only 30ppm/°C, and is guaranteed to be less than 100ppm/°C in the SOT23 package. For a guaranteed output voltage temperature coefficient of less than 50ppm/°C, see the MAX6520 data sheet.

Applications

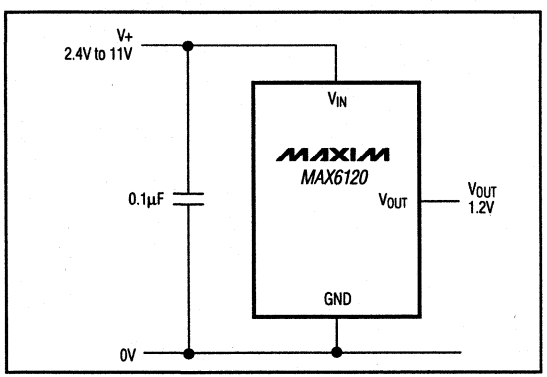
Battery-Powered Systems

Portable and Hand-Held Equipment

Data-Acquisition Systems

Instrumentation and Process Control

Typical Operating Circuit



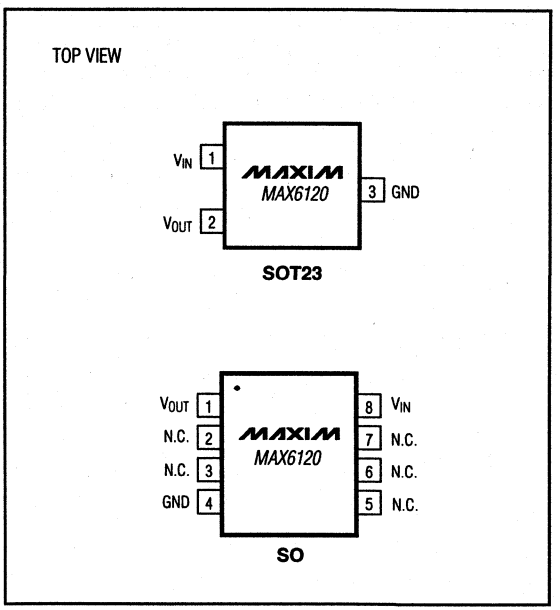
Features

- ♦ **3-Pin SOT23 Package**
- ♦ **Supply Current Independent of Input Voltage Over Temperature**
- ♦ **50µA Supply Current**
- ♦ **2.4V to 11V Input Voltage Range**
- ♦ **30ppm/°C Typical Tempco (SOT23)**
- ♦ **±1% Initial Accuracy (SOT23)**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX6120ESA	-40°C to +85°C	8 SO
MAX6120EUR	-40°C to +85°C	3 SOT23-3

Pin Configurations



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Low-Cost, Micropower, Precision, 3-Terminal, 1.2V Voltage Reference

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{IN}) .....-0.3V to +12V
V_{OUT} .....-0.3V to (V_{IN} + 0.3V)
Output Short-Circuit Duration .....Continuous to Either Supply
Continuous Power Dissipation (T_A = +70°C)
SOT23 (derate 4mW/°C above +70°C) 320mW

Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{IN} = 2.4V, I_{LOAD} = 0mA, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage	V_{OUT}	MAX6120EUR (SOT23)	T_A = +25°C	1.188	1.200	1.212	V
			T_A = T_{MIN} to T_{MAX} (Note 2)	1.176		1.224	V
Output Voltage Temperature Coefficient	TCV_{OUT}	MAX6120EUR (SOT23), T_A = T_{MIN} to T_{MAX} (Note 2)			30	100	ppm/°C
Output Voltage Noise	e_n	0.1Hz to 10Hz			10		µVp-p
		10Hz to 10kHz			400		
Line Regulation	V_{OUT}/V_{IN}	V_{IN} = 2.4V to 11V, T_A = T_{MIN} to T_{MAX} (Note 1)			2	30	µV/V
Load Regulation	V_{OUT}/I_{OUT}	I_{LOAD} = -50µA to 400µA (Note 1)			0.1	1	µV/µA
Quiescent Supply Current	I_Q	T_A = +25°C			50	58	µA
		T_A = T_{MIN} to T_{MAX} (Note 1)				70	
Change in Supply Current vs. Input Voltage	I_Q/V_{IN}	V_{IN} = 2.4V to 11V			1.5	5	µA/V
Short-Circuit Output Current	I_{SC}	V_{OUT} shorted to GND			4.3		mA
		V_{OUT} shorted to V_{IN}			400		µA

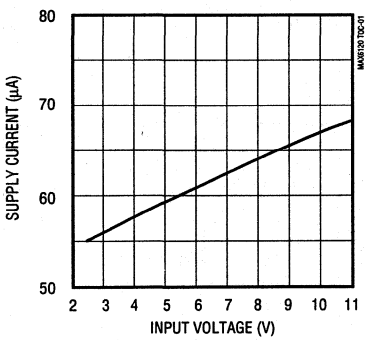
Note 1: Production testing done at T_A = +25°C, over temperature limits guaranteed by parametric correlation data.

Note 2: Contact factory for availability of a higher-grade, lower-TC option in a SOT23 package.

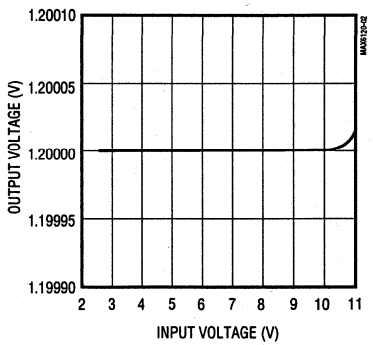
Typical Operating Characteristics

(V_{IN} = 3V, I_{LOAD} = 0mA, T_A = +25°C, unless otherwise noted.)

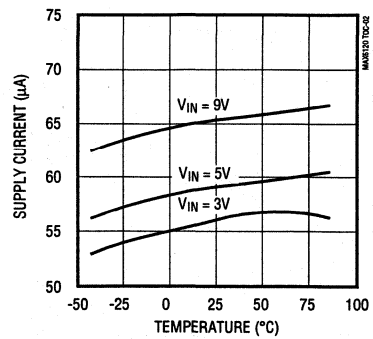
SUPPLY CURRENT vs. INPUT VOLTAGE



OUTPUT VOLTAGE vs. INPUT VOLTAGE



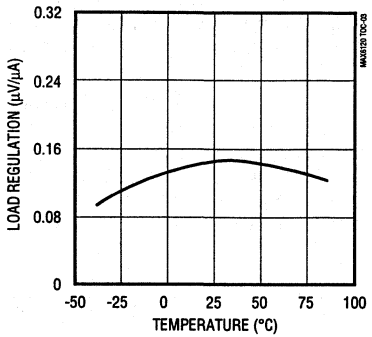
SUPPLY CURRENT vs. TEMPERATURE



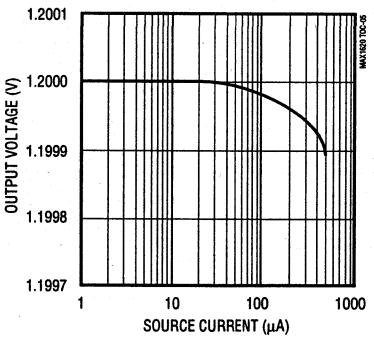
Typical Operating Characteristics (continued)

(V_{IN} = 3V, I_{LOAD} = 0mA, T_A = +25°C, unless otherwise noted.)

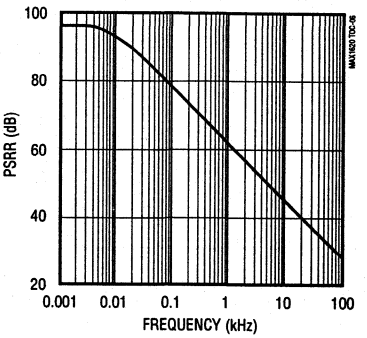
LOAD REGULATION vs. TEMPERATURE



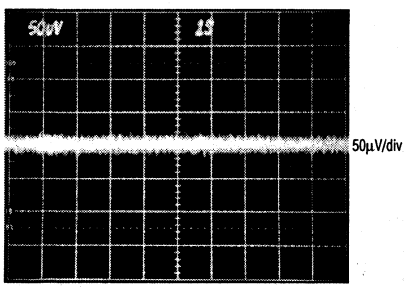
OUTPUT VOLTAGE vs. SOURCE CURRENT



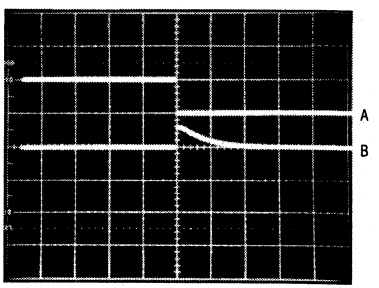
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



0.1Hz TO 100Hz NOISE

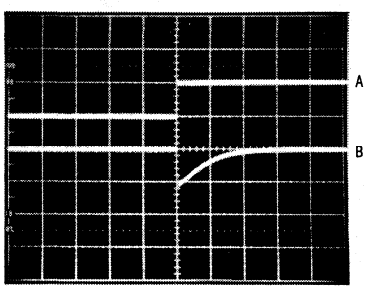


LOAD-TRANSIENT RESPONSE



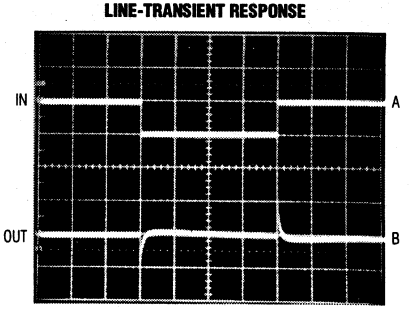
A = OUTPUT CURRENT, 50µA/div, I_{LOAD} = 0µA TO -50µA
B = OUTPUT VOLTAGE, 100mV/div

LOAD-TRANSIENT RESPONSE



A = OUTPUT CURRENT, 500µA/div, I_{LOAD} = 0µA TO 500µA
B = OUTPUT VOLTAGE, 100mV/div

LINE-TRANSIENT RESPONSE



A = INPUT VOLTAGE, 100mV/div, V_{IN} = 3V ± 50mV
B = OUTPUT VOLTAGE, 10mV/div

Low-Cost, Micropower, Precision, 3-Terminal, 1.2V Voltage Reference

Pin Description

PIN		NAME	FUNCTION
SOT23	SO		
1	8	V_{IN}	Input Voltage
2	1	V_{OUT}	Reference Output
3	4	GND	Ground
—	2, 3, 5, 6, 7	N.C.	No Connect—not internally connected

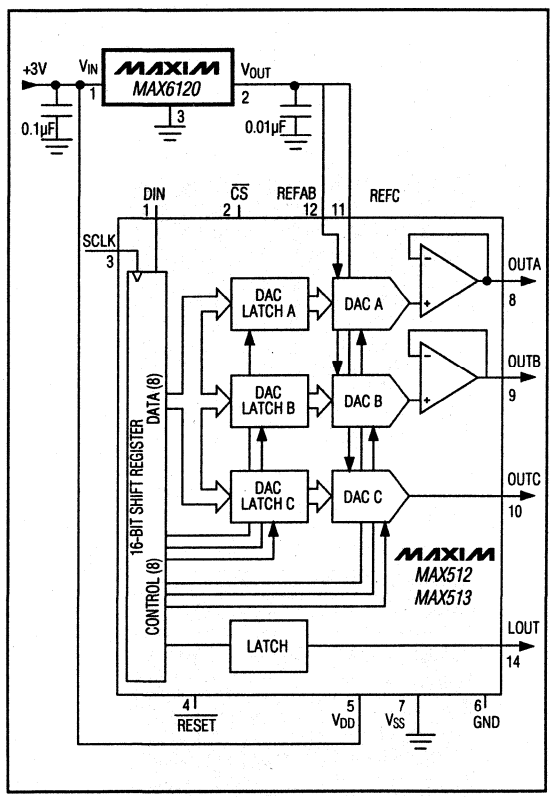


Figure 1. 3V, Triple, 8-Bit Serial DAC

Applications Information

Input Bypassing

For the best line-transient performance, decouple the input with a 0.1µF ceramic capacitor as shown in the *Typical Operating Circuit*. Locate the capacitor as close to the device pin as possible. Where transient performance is less important, no capacitor is necessary.

Output Bypass

The MAX6120 performs well without an output decoupling capacitor. If your application requires an output charge reservoir (e.g., to decouple the reference from the input of a DAC), then make sure that the total output capacitive load does not exceed 10nF.

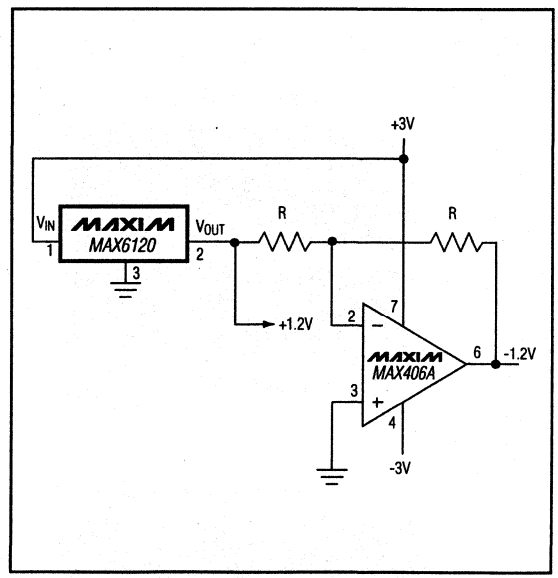
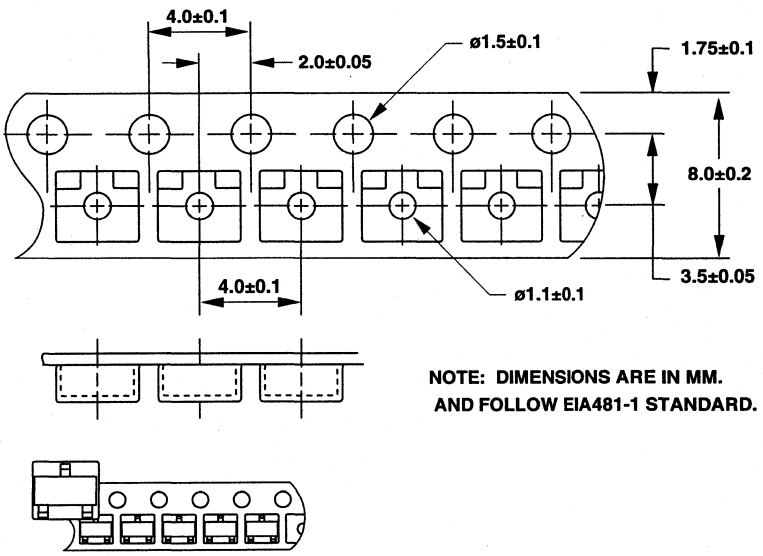


Figure 2. Low-Power ±1.2V Reference

Chip Information

TRANSISTOR COUNT: 39

Tape-and-Reel Information



NOTE: DIMENSIONS ARE IN MM.
AND FOLLOW EIA481-1 STANDARD.

MARKING INFORMATION†
LOT SPECIFIC CODE
AY XX = MAX6120

†ICs MAY ALSO BE MARKED WITH FULL PART NAME: MAX6120

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

10/96

MAXIM

Miniature, Low-Cost, Low-Dropout 3-Terminal References

General Description

The MAX6125/MAX6141/MAX6145/MAX6150/MAX6160 low-dropout, micropower, three-terminal voltage references offer 2.5V, 4.096V, 4.5V, 5.0V, and adjustable (1.23V to 12.4V) output voltages, respectively. Low, 200mV dropout, three-terminal architecture, and miniature SOT packages make these devices ideal for 3V and 5V battery-powered systems. Unlike two-terminal references that waste battery current and require an external resistor, the MAX61xx family's supply current is virtually independent of input voltage variations, which translates to longer battery life.

Initial accuracy for these devices is ±1%. The output temperature coefficient is typically 15ppm/°C, and guaranteed to be less than 50ppm°C. The MAX6125/MAX6141/MAX6145/MAX6150 are available in 3-pin SOT23 and 8-pin SO packages. The MAX6160 is available in 4-pin SOT143 and 8-pin SO packages.

Features

- **3-Pin SOT23 Package (MAX6125/41/45/50)**
  4-Pin SOT143 Package (MAX6160)
- **Low, 200mV Dropout Voltage**
- **70µA Supply Current, Independent of Input Voltage (MAX6125)**
- **15ppm/°C Tempco**
- **Adjustable Output Voltage from 1.23V to (V_{IN} - 0.2V) (MAX6160)**
- **Optimized for 3V/5V Operation**

Applications

3V/5V Systems
Battery-Powered Systems
Portable and Hand-Held Equipment
Data Acquisition Systems
Instrumentation and Process Control

Selector Guide

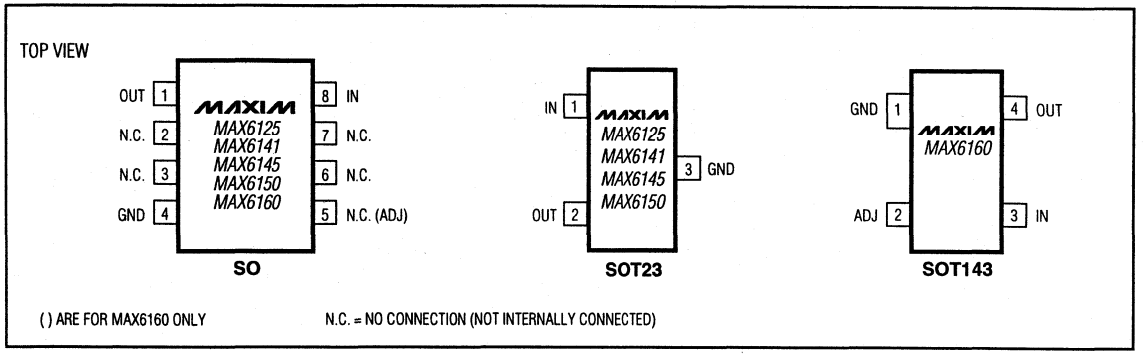
PART	PRESET OUTPUT VOLTAGE (V)	PACKAGE
MAX6125	2.5	8-SO/3-SOT23
MAX6141	4.096	8-SO/3-SOT23
MAX6145	4.5	8-SO/3-SOT23
MAX6150	5	8-SO/3-SOT23
MAX6160	Adjustable	8-SO/4-SOT143

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
MAX6125ESA	-40°C to +85°C	8 SO	—
MAX6125EUR	-40°C to +85°C	3 SOT23-3	EB
MAX6141ESA	-40°C to +85°C	8 SO	—
MAX6141EUR	-40°C to +85°C	3 SOT23-3	EC

Ordering Information continued on next page.

Pin Configurations



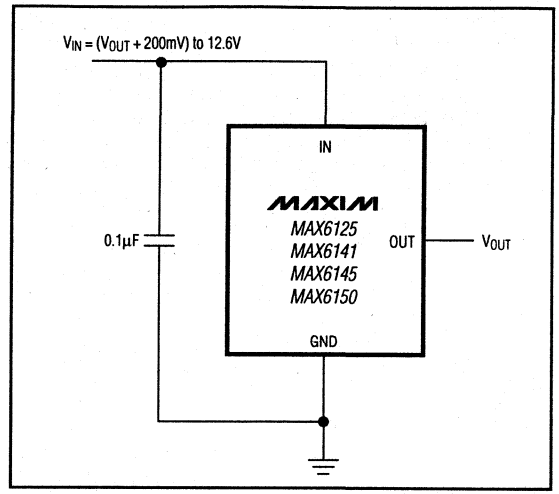
For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Miniature, Low-Cost, Low-Dropout 3-Terminal References

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
MAX6145ESA	-40°C to +85°C	8 SO	—
MAX6145EUR	-40°C to +85°C	3 SOT23-3	ED
MAX6150ESA	-40°C to +85°C	8 SO	—
MAX6150EUR	-40°C to +85°C	3 SOT23-3	EE
MAX6160ESA	-40°C to +85°C	8 SO	—
MAX6160EUS	-40°C to +85°C	4 SOT143	JX

_____Typical Operating Circuit



19-1139; Rev 0; 9/96

MAXIM

Low-Noise, Precision, +2.5V/+4.096V/+5V Voltage References

General Description

The MAX6225/MAX6241/MAX6250 are low-noise, precision voltage references with extremely low temperature coefficients normally associated with heated voltage references, but with low power consumption. These devices feature buried Zener technology for low-noise performance. Load-regulation specifications are guaranteed for source and sink currents up to 15mA. Excellent line and load regulation and low output impedance at high frequency make them ideal for high-resolution data-conversion systems up to 16 bits.

The MAX6225 is set for 2.500V output, the MAX6241 is set for 4.096V output, and the MAX6250 is set for 5.000V output. All three provide for the option of external trimming and noise reduction.

Applications

High-Resolution Analog-to-Digital and Digital-to-Analog Converters

High-Accuracy Reference Standard

High-Accuracy Industrial and Process Control

Digital Voltmeters

ATE Equipment

Precision Current Sources

Features

- ♦ **Low 2.5ppm/°C Temperature Coefficient**
- ♦ **Very Low 1.5µVp-p Noise (0.1Hz to 10Hz)**
- ♦ **±0.1% Initial Accuracy**
- ♦ **±15mA Output Source and Sink Current**
- ♦ **Industry-Standard Pinout**
- ♦ **Optional Noise Reduction and Voltage Trim**
- ♦ **Excellent Transient Response**
- ♦ **8-Pin SO Package**
- ♦ **Low 20ppm/1000h Long-Term Stability**
- ♦ **Stable for All Capacitive Loads**

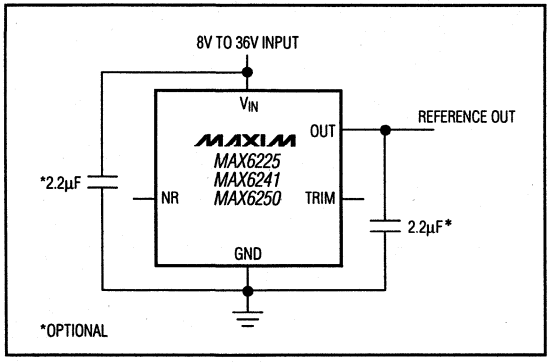
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	MAX TEMPCO (ppm/°C)
MAX6225ACPA*	0°C to +70°C	8 Plastic DIP	*
MAX6225ACSA*	0°C to +70°C	8 SO	*
MAX6225AEPA*	-40°C to +85°C	8 Plastic DIP	*
MAX6225AESA*	-40°C to +85°C	8 SO	*
MAX6225AMJA*	-55°C to +125°C	8 CERDIP	*
MAX6225BCPA	0°C to +70°C	8 Plastic DIP	5
MAX6225BCSA	0°C to +70°C	8 SO	5
MAX6225BEPA	-40°C to +85°C	8 Plastic DIP	7
MAX6225BESA	-40°C to +85°C	8 SO	7
MAX6225BMJA*	-55°C to +125°C	8 CERDIP	*

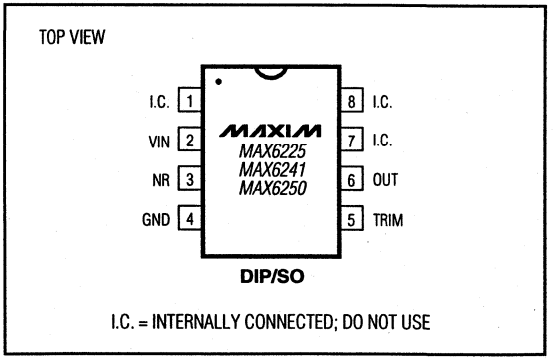
Ordering Information continued at end of data sheet.

**Contact factory for availability. The "A" grade max tempco specifications will be <5ppm/°C.*

Typical Operating Circuit



Pin Configuration



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Low-Noise, Precision, +2.5V/+4.096V/+5V Voltage References

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to GND
V_{IN} .....-0.3V to +40V
V_{OUT}, V_{TRIM} .....-0.3V to +12V
V_{NR} .....-0.3V to +6V
V_{OUT} Short Circuit to GND Duration ($V_{IN} \le 12V$).....Continuous
V_{OUT} Short Circuit to GND Duration ($V_{IN} \le 40V$) 5sec
V_{OUT} Short Circuit to V+ Duration ($V_{IN} \le 12V$) .....Continuous
Continuous Power Dissipation (T_A = +70°C)
Narrow Plastic DIP (derate 9.09mW/°C above +70°C)...727mW
Narrow SO (derate 5.88mW/°C above +70°C).....471mW
CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges
MAX62_ _ _C_ A.....0°C to +70°C
MAX62_ _ _E_ A.....-40°C to +85°C
MAX62_ _ _MJA.....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX6225

(V_{IN} = 10V, I_{OUT} = 0mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		T_A (Note 1)	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}			C, E	8		36	V
Output Voltage	V_{OUT}	MAX6225B_ _ _		+25°C	2.497	2.500	2.503	V
Output Voltage Temperature Coefficient (Note 2)	TCV_{OUT}	MAX6225BC_A		C		2.5	5.0	ppm/°C
		MAX6225BE_A		E		2.5	7.0	
Line Regulation (Note 3)		8V ≤ V_{IN} ≤ 10V		+25°C		10	18	ppm/V
				C			30	
				E			35	
		10V ≤ V_{IN} ≤ 36V		+25°C		2	5	
				C			7	
				E			8	
Load Regulation (Note 3)		Sourcing	0mA ≤ I_{OUT} ≤ 15mA	+25°C		1	5	ppm/mA
				C			6	
				E			7	
		Sinking	-15mA ≤ I_{OUT} ≤ 0mA	+25°C		1	5	
				C			6	
				E			7	
Turn-On Settling Time to ±0.01% of Final Value	t_{ON}			+25°C		5		µs
Supply Current	I_{IN}			+25°C		1.8	2.7	mA
				C, E			3.0	
Trim-Adjustment Range	ΔV_{OUT}			C, E	±15	±25		mV
Output Noise Voltage (Note 4)	e_n	0.1Hz ≤ f ≤ 10Hz		+25°C		1.5		μV_{P-P}
		10Hz ≤ f ≤ 1kHz				1.3	2.8	μV_{RMS}
Temperature Hysteresis		(Note 5)		+25°C		20		ppm
Long-Term Stability				+25°C		20		ppm/1000h

ELECTRICAL CHARACTERISTICS—MAX6241

(V_{IN} = 10V, I_{OUT} = 0mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		T_A	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}			C, E	8		36	V
Output Voltage	V_{OUT}	MAX6241B_ _ _		+25°C	4.092	4.096	4.100	V
Output Voltage Temperature Coefficient (Note 2)	TCV_{OUT}	MAX6241BC_A		C		2.5	5.0	ppm/°C
		MAX6241BE_A		E		2.5	7.0	
Line Regulation (Note 3)		8V ≤ V_{IN} ≤ 10V		+25°C		10	18	ppm/V
				C			30	
				E			35	
		10V ≤ V_{IN} ≤ 36V		+25°C		2	5	
				C			7	
				E			8	
Load Regulation (Note 3)		Sourcing	0mA ≤ I_{OUT} ≤ 15mA	+25°C		1	5	ppm/mA
				C			6	
				E			7	
		Sinking	-15mA ≤ I_{OUT} ≤ 0mA	+25°C		1	5	
				C			6	
				E			7	
Turn-On Settling Time to ±0.01% of Final Value	t_{ON}			+25°C		8		µs
Supply Current	I_{IN}			+25°C		1.9	2.9	mA
				C, E			3.2	
Trim-Adjustment Range	ΔV_{OUT}			C, E	±24	±40		mV
Output Noise Voltage (Note 4)	e_n	0.1Hz ≤ f ≤ 10Hz		+25°C		2.4		μV_{P-P}
		10Hz ≤ f ≤ 1kHz				2.0	4.0	μV_{RMS}
Temperature Hysteresis		(Note 5)		+25°C		20		ppm
Long-Term Stability				+25°C		20		ppm/1000h

Low-Noise, Precision, +2.5V/+4.096V/+5V Voltage References

ELECTRICAL CHARACTERISTICS—MAX6250

(V_{IN} = 10V, I_{OUT} = 0mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		T_A	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}			C, E	8		36	V
Output Voltage	V_{OUT}	MAX6250B_ _ _		+25°C	4.995	5.000	5.005	V
Output Voltage Temperature Coefficient (Note 2)	TCV_{OUT}	MAX6250BC_A		C		2.5	5.0	ppm/°C
		MAX6250BE_A		E		2.5	7.0	
Line Regulation (Note 3)		8V ≤ V_{IN} ≤ 10V		+25°C		10	18	ppm/V
				C			30	
				E			35	
		10V ≤ V_{IN} ≤ 36V		+25°C		2	5	
				C			7	
				E			8	
Load Regulation (Note 3)		Sourcing	0mA ≤ I_{OUT} ≤ 15mA	+25°C		1	5	ppm/mA
				C			6	
				E			7	
		Sinking	-15mA ≤ I_{OUT} ≤ 0mA	+25°C		1	5	
				C			6	
				E			7	
Turn-On Settling Time to ±0.01% of Final Value	t_{ON}			+25°C		10		µs
Supply Current	I_{IN}			+25°C		2.0	3.0	mA
				C, E			3.3	
Trim-Adjustment Range	ΔV_{OUT}			C, E	±30	±50		mV
Output Noise Voltage (Note 5)	e_n	0.1Hz ≤ f ≤ 10Hz		+25°C		3		μV_{P-P}
		10Hz ≤ f ≤ 1kHz				2.5	5.0	μV_{RMS}
Temperature Hysteresis		(Note 5)		+25°C		20		ppm
Long-Term Stability				+25°C		20		ppm/1000h

Note 1: Operating temperature range: C = 0°C to +70°C, E = -40°C to +85°C, M = -55°C to +125°C.

Note 2: Temperature coefficient is measured by the box method, i.e., the maximum ΔV_{OUT} is divided by $\Delta T \times V_{OUT}$.

Note 3: Line, $\Delta V_{OUT} / (V_{OUT} \times \Delta V_{IN})$, and load, $\Delta V_{OUT} / (V_{OUT} \times \Delta I_{OUT})$, regulation are measured with pulses and do not include output voltage changes due to die temperature changes.

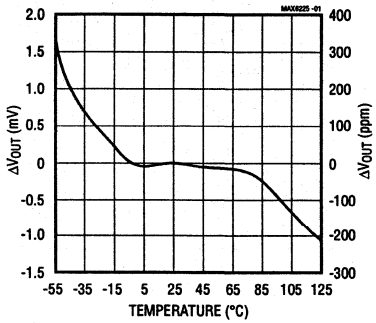
Note 4: Noise specifications are 100% tested for 10Hz to 1kHz bandwidth. Contact factory for 100% noise testing in the 0.1Hz to 10Hz bandwidth.

Note 5: Temperature hysteresis is specified at T_A = +25°C by measuring V_{OUT} before and after changing temperature by +25°C using the PDIP package.

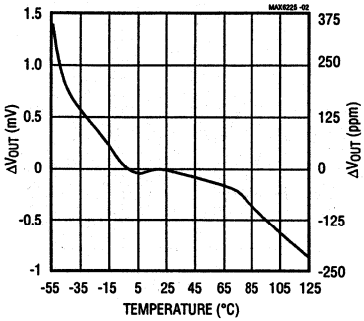
Typical Operating Characteristics

(V_{IN} = 10V, I_{OUT} = 0mA, T_A = +25°C, unless otherwise noted.)

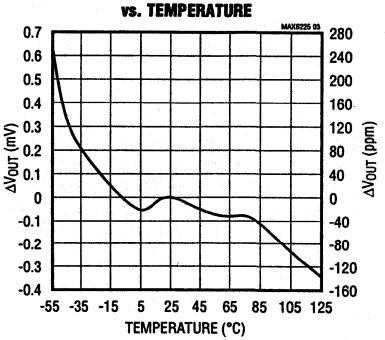
MAX6250
NORMALIZED OUTPUT VOLTAGE vs. TEMPERATURE



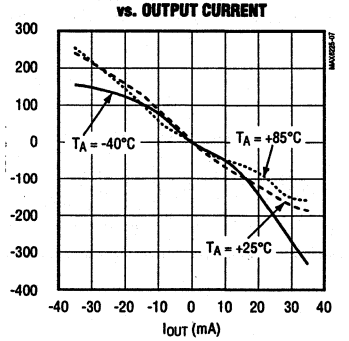
MAX6241
NORMALIZED OUTPUT VOLTAGE vs. TEMPERATURE



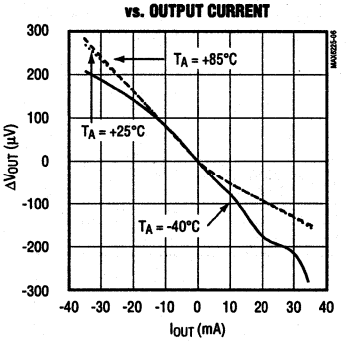
MAX6225
NORMALIZED OUTPUT VOLTAGE vs. TEMPERATURE



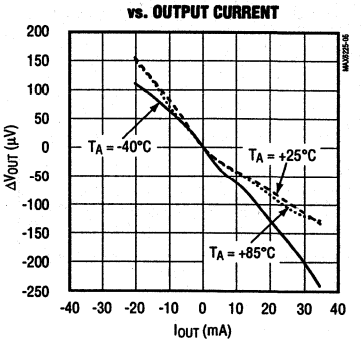
MAX6250
CHANGE IN OUTPUT VOLTAGE vs. OUTPUT CURRENT



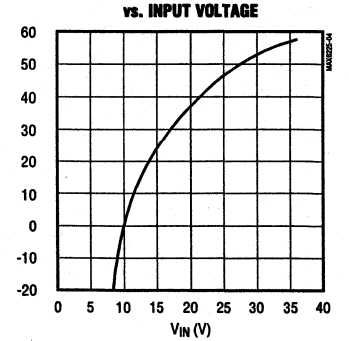
MAX6241
CHANGE IN OUTPUT VOLTAGE vs. OUTPUT CURRENT



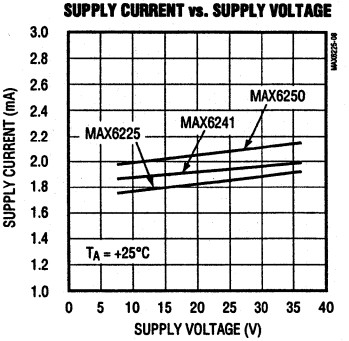
MAX6225
CHANGE IN OUTPUT VOLTAGE vs. OUTPUT CURRENT



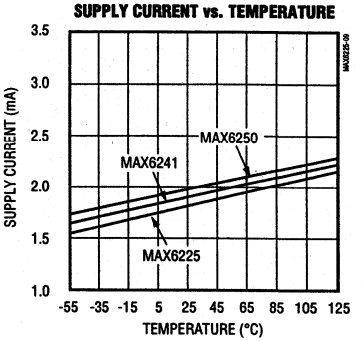
CHANGE IN OUTPUT VOLTAGE vs. INPUT VOLTAGE



SUPPLY CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



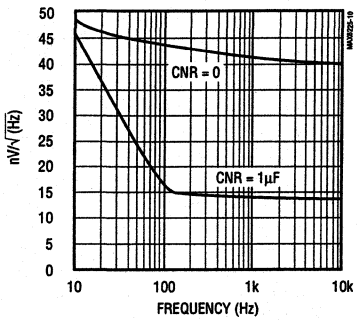
Low-Noise, Precision, +2.5V/+4.096V/+5V Voltage References

Typical Operating Characteristics (continued)

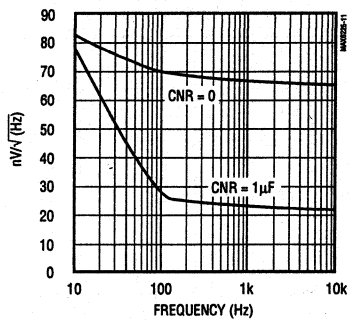
(VIN = 10V, IOUT = 0mA, TA = +25°C, unless otherwise noted.)

5°C

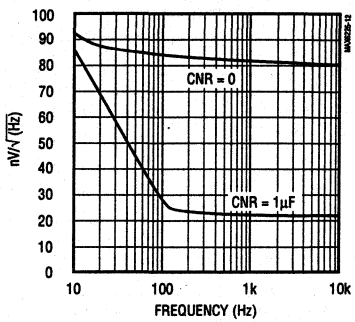
MAX6225
OUTPUT NOISE-VOLTAGE DENSITY



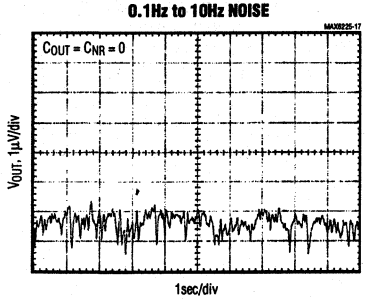
MAX6241
OUTPUT NOISE-VOLTAGE DENSITY



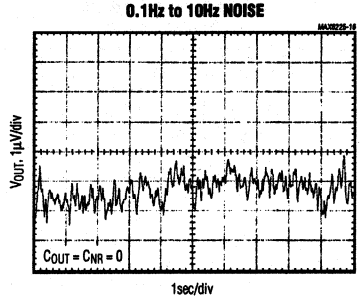
MAX6250
OUTPUT NOISE-VOLTAGE DENSITY



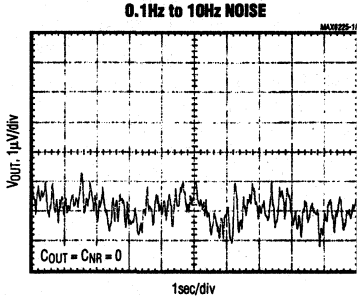
MAX6225B
0.1Hz to 10Hz NOISE



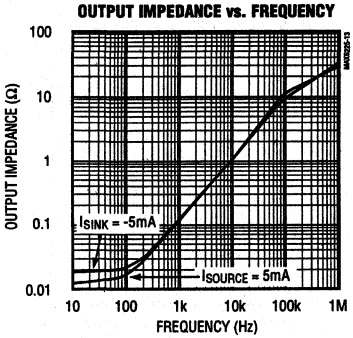
MAX6241
0.1Hz to 10Hz NOISE



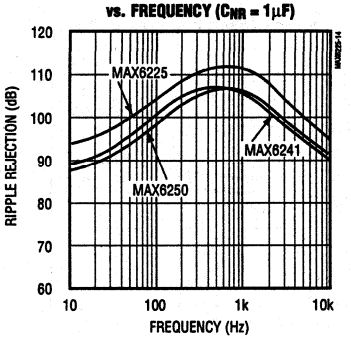
MAX6250
0.1Hz to 10Hz NOISE



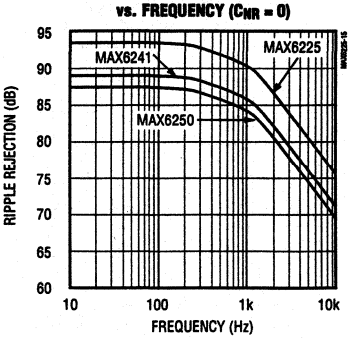
OUTPUT IMPEDANCE vs. FREQUENCY



RIPPLE REJECTION
vs. FREQUENCY (CNR = 1µF)



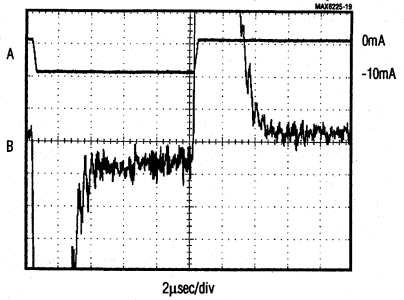
RIPPLE REJECTION
vs. FREQUENCY (CNR = 0)



Typical Operating Characteristics (continued)

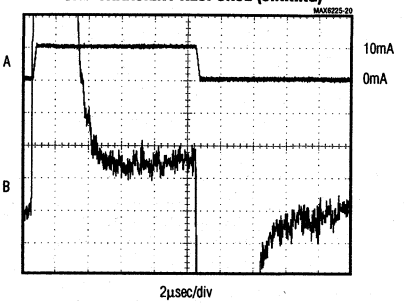
(V_{IN} = 10V, I_{OUT} = 0mA, T_A = +25°C, unless otherwise noted.)

LOAD-TRANSIENT RESPONSE (SOURCING)



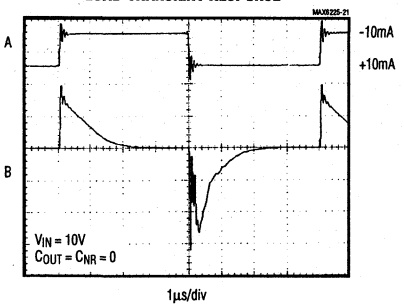
A: I_{OUT}, 10mA/div (SOURCING)
B: V_{OUT}, 500µV/div

LOAD-TRANSIENT RESPONSE (SINKING)



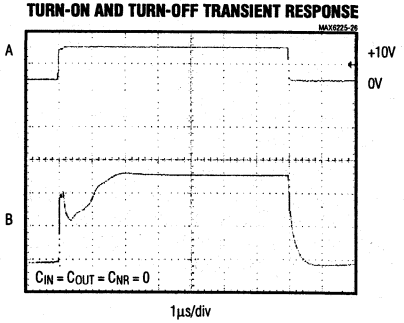
A: I_{OUT}, 10mA/div (SINKING)
B: V_{OUT}, 500µV/div

LOAD-TRANSIENT RESPONSE



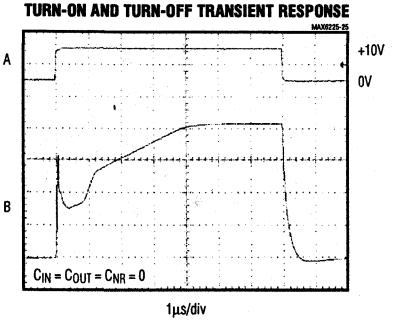
A: I_{OUT} (±10mA SOURCE AND SINK), 20mA/div, AC COUPLED
B: V_{OUT}, 20mV/div, AC COUPLED

MAX6225
TURN-ON AND TURN-OFF TRANSIENT RESPONSE



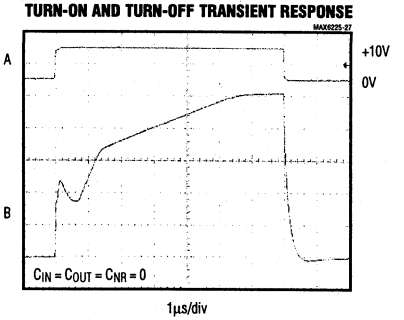
A: V_{IN}, 10V/div
B: V_{OUT}, 1V/div

MAX6241
TURN-ON AND TURN-OFF TRANSIENT RESPONSE



A: V_{IN}, 10V/div
B: V_{OUT}, 1V/div

MAX6250
TURN-ON AND TURN-OFF TRANSIENT RESPONSE



A: V_{IN}, 10V/div
B: V_{OUT}, 1V/div

Low-Noise, Precision, +2.5V/+4.096V/+5V Voltage References

Pin Description

PIN	NAME	FUNCTION
1, 7, 8	I.C.	Internally Connected. **Do not use.**
2	VIN	Positive Power-Supply Input
3	NR	Noise Reduction. Optional capacitor connection for wideband noise reduction. Leave open if not used (Figure 2).
4	GND	Ground
5	TRIM	External Trim Input. Allows ±1% output adjustment (Figure 1). Leave open if not used.
6	OUT	Voltage Reference Output

Detailed Description

Temperature Stability

The MAX6225/MAX6241/MAX6250 are highly stable, low-noise voltage references that use a low-power temperature-compensation scheme to achieve laboratory-standard temperature stability. This produces a nearly flat temperature curve, yet does not require the power associated with heated references.

The output voltage can be trimmed a minimum of 0.6% by connecting a 10kΩ potentiometer between OUT and GND, and connecting its tap to the TRIM pin, as shown in Figure 1. The external trimming does not affect temperature stability.

Noise Reduction

To augment wideband noise reduction, add a 1µF capacitor to the NR pin (Figure 2). Larger values do not improve noise appreciably (*see Typical Operating Characteristics*).

Noise in the power-supply input can affect output noise, but can be reduced by adding an optional bypass capacitor to the VIN pin and GND.

Bypassing

The MAX6225/MAX6241/MAX6250 are stable with all values of capacitive load from zero to 100µF, for all values of load current. Adding an output bypass capacitor can help reduce noise and output glitching caused by load transients.

Applications Information

Negative Regulator

Figure 3 shows how both a +5V and -5V precision reference can be obtained from a single unregulated +5V supply. A MAX681 generates approximately ±9V to operate the MAX6250 reference and MAX432 inverting amplifier. The +5V is inverted by the MAX432 chopper-stabilized amplifier. Resistor R1 is optional, and may be used to trim the ±5V references. R2 and R4 should be matched, both in absolute resistance and temperature coefficient. R3 is optional, and is adjusted to set the -5V reference.

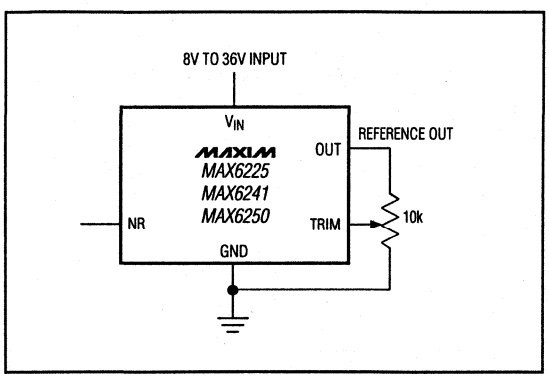


Figure 1. Output Voltage Adjustment

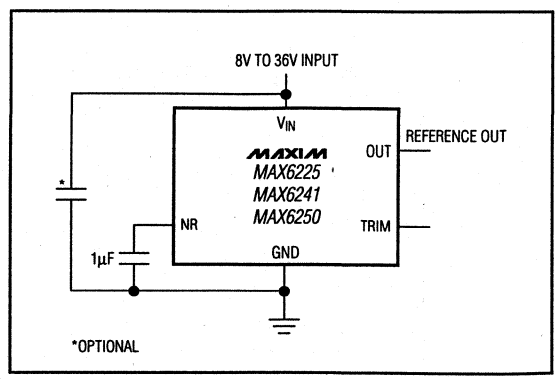


Figure 2. Noise-Reduction Capacitor

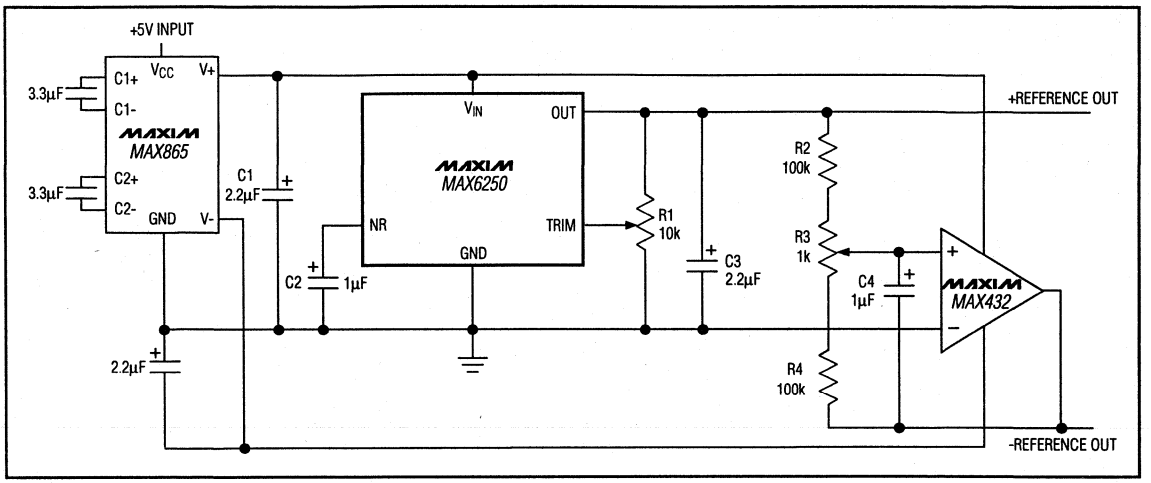


Figure 3. +5V and -5V References from a Single +5V Supply

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	MAX. TEMPCO (ppm/°C)
MAX6241ACPA*	0°C to +70°C	8 Plastic DIP	
MAX6241ACSA*	0°C to +70°C	8 SO	
MAX6241AEPA*	-40°C to +85°C	8 Plastic DIP	
MAX6241AESA*	-40°C to +85°C	8 SO	
MAX6241AMJA*	-55°C to +125°C	8 CERDIP	
MAX6241BCPA	0°C to +70°C	8 Plastic DIP	5
MAX6241BCSA	0°C to +70°C	8 SO	5
MAX6241BEPA	-40°C to +85°C	8 Plastic DIP	7
MAX6241BESA	-40°C to +85°C	8 SO	7
MAX6241BMJA*	-55°C to +125°C	8 CERDIP	
MAX6250ACPA*	0°C to +70°C	8 Plastic DIP	
MAX6250ACSA*	0°C to +70°C	8 SO	
MAX6250AEPA*	-40°C to +85°C	8 Plastic DIP	
MAX6250AESA*	-40°C to +85°C	8 SO	
MAX6250AMJA*	-55°C to +125°C	8 CERDIP	
MAX6250BCPA	0°C to +70°C	8 Plastic DIP	5
MAX6250BCSA	0°C to +70°C	8 SO	5
MAX6250BEPA	-40°C to +85°C	8 Plastic DIP	7
MAX6250BESA	-40°C to +85°C	8 SO	7
MAX6250BMJA*	-55°C to +125°C	8 CERDIP	

**Contact factory for availability.*

_Chip Information

TRANSISTOR COUNT: 435

SUBSTRATE CONNECTED TO GROUND.

19-1130; Rev 0; 9/96

MAXIM

50ppm/°C, SOT23, 3-Terminal, 1.2V Voltage Reference

General Description

The MAX6520 is the lowest-power 1.2V, precision, three-terminal voltage reference offered in a SOT23-3 package. Ideal for 3V battery-powered equipment where power conservation is critical, the MAX6520 is a low-power alternative to existing two-terminal shunt references. Unlike two-terminal references that throw away battery current and require an external series resistor, the MAX6520 has a 70µA maximum supply current (typically only 50µA) that is independent of the input voltage. This feature translates to maximum efficiency at all battery voltages.

The MAX6520 operates from a supply voltage as low as 2.4V, and initial accuracy is ±1% for the SOT23 package. **Output voltage temperature coefficient is typically only 25ppm/°C, and is guaranteed to be less than 50ppm/°C in the SOT23 package.**

Features

- **3-Pin SOT23 Package**
- **50ppm/°C max Tempco**
- **Supply Current Independent of Input Voltage Over Temperature**
- **50µA Supply Current**
- **2.4V to 11V Input Voltage Range**
- **±1% Initial Accuracy**

Applications

Battery-Powered Systems

Portable and Hand-Held Equipment

Data-Acquisition Systems

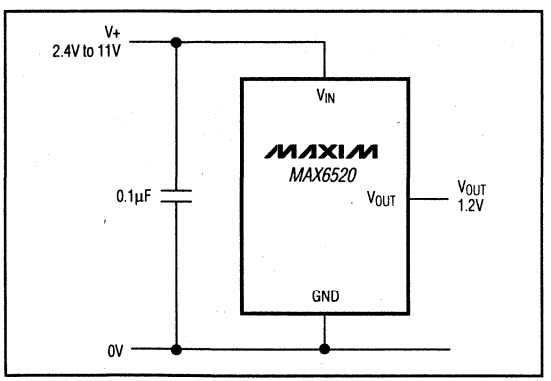
Instrumentation and Process Control

Ordering Information

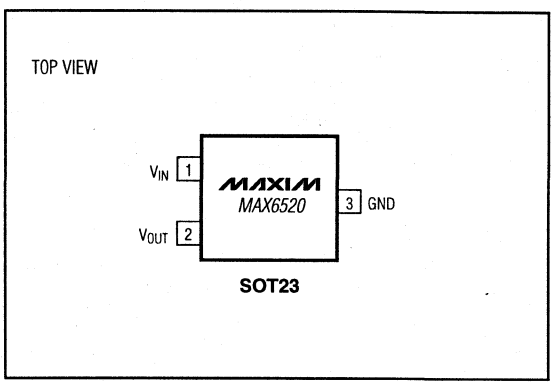
PART	TEMP. RANGE	PIN-PACKAGE
MAX6520EUR-T	-40°C to +85°C	3 SOT23-3

** Contact factory for availability.*

Typical Operating Circuit



Pin Configuration



6

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

50ppm/°C, SOT23, 3-Terminal, 1.2V Voltage Reference

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{IN}) .....-0.3V to +12V
V_{OUT} .....-0.3V to (V_{IN} + 0.3V)
Output Short-Circuit Duration .....Continuous to Either Supply
Continuous Power Dissipation (T_A = +70°C)
SOT23 (derate 4mW/°C above +70°C) 320mW

Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

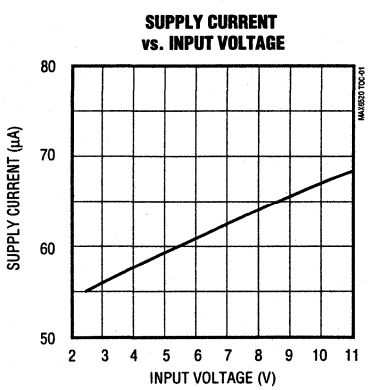
(V_{IN} = 2.4V, I_{LOAD} = 0mA, T_A = +25°C, unless otherwise noted.)

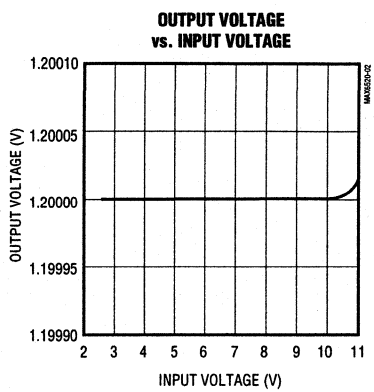
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage	V_{OUT}	MAX6520EUR	T_A = +25°C	1.188	1.200	1.212	V
			T_A = T_{MIN} to T_{MAX}	1.176		1.224	V
Output Voltage Temperature Coefficient	TCV_{OUT}	MAX6520EUR, T_A = T_{MIN} to T_{MAX}			25	50	ppm/°C
Output Voltage Noise	e_n	0.1Hz to 10Hz			10		µVp-p
		10Hz to 10kHz			400		
Line Regulation	V_{OUT}/V_{IN}	V_{IN} = 2.4V to 11V, T_A = T_{MIN} to T_{MAX} (Note 1)			2	30	µV/V
Load Regulation	V_{OUT}/I_{OUT}	I_{LOAD} = -50µA to 400µA (Note 1)			0.1	1	µV/µA
Quiescent Supply Current	I_Q	T_A = +25°C			50	58	µA
		T_A = T_{MIN} to T_{MAX} (Note 1)				70	
Change in Supply Current vs. Input Voltage	I_Q/V_{IN}	V_{IN} = 2.4V to 11V			1.5	5	µA/V
Short-Circuit Output Current	I_{SC}	V_{OUT} shorted to GND			4.3		mA
		V_{OUT} shorted to V_{IN}			400		µA

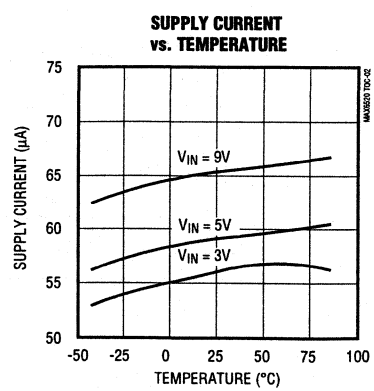
Note 1: Production testing done at T_A = +25°C, over temperature limits guaranteed by parametric correlation data.

Typical Operating Characteristics

(V_{IN} = 3V, I_{LOAD} = 0mA, T_A = +25°C, unless otherwise noted.)





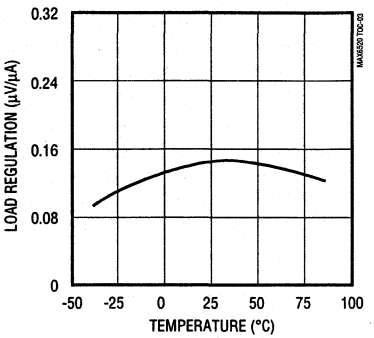


50ppm/°C, SOT23, 3-Terminal, 1.2V Voltage Reference

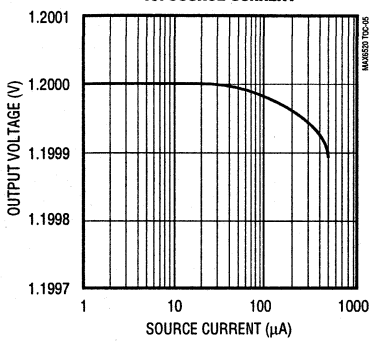
Typical Operating Characteristics (continued)

(V_{IN} = 3V, I_{LOAD} = 0mA, T_A = +25°C, unless otherwise noted.)

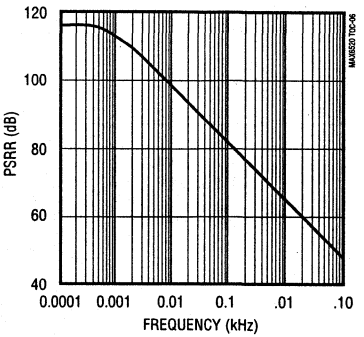
LOAD REGULATION vs. TEMPERATURE



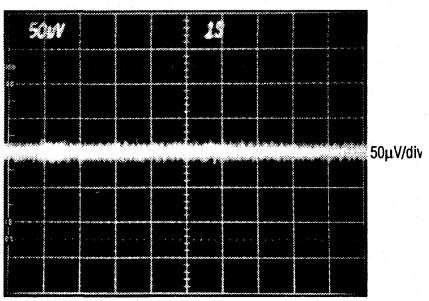
OUTPUT VOLTAGE vs. SOURCE CURRENT



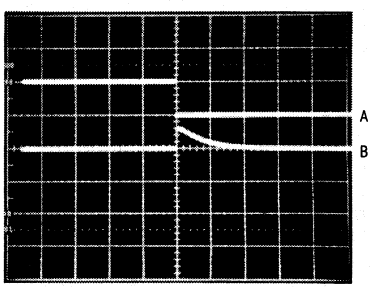
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



0.1Hz TO 100Hz NOISE

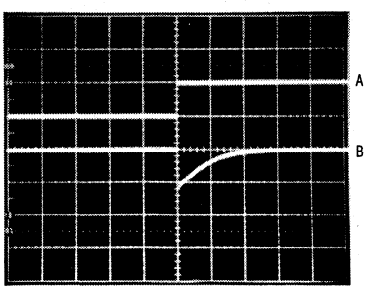


LOAD-TRANSIENT RESPONSE



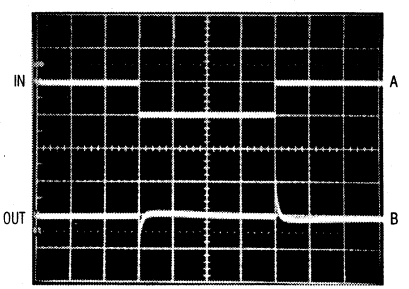
A = OUTPUT CURRENT, 50µA/div, I_{LOAD} = 0µA TO -50µA
B = OUTPUT VOLTAGE, 100mV/div

LOAD-TRANSIENT RESPONSE



A = OUTPUT CURRENT, 500µA/div, I_{LOAD} = 0µA TO 500µA
B = OUTPUT VOLTAGE, 100mV/div

LINE-TRANSIENT RESPONSE



A = INPUT VOLTAGE, 100mV/div, V_{IN} = 3V ± 50mV
B = OUTPUT VOLTAGE, 10mV/div

50ppm/°C, SOT23, 3-Terminal, 1.2V Voltage Reference

Pin Description

PIN	NAME	FUNCTION
1	V_{IN}	Input Voltage
2	V_{OUT}	Reference Output
3	GND	Ground

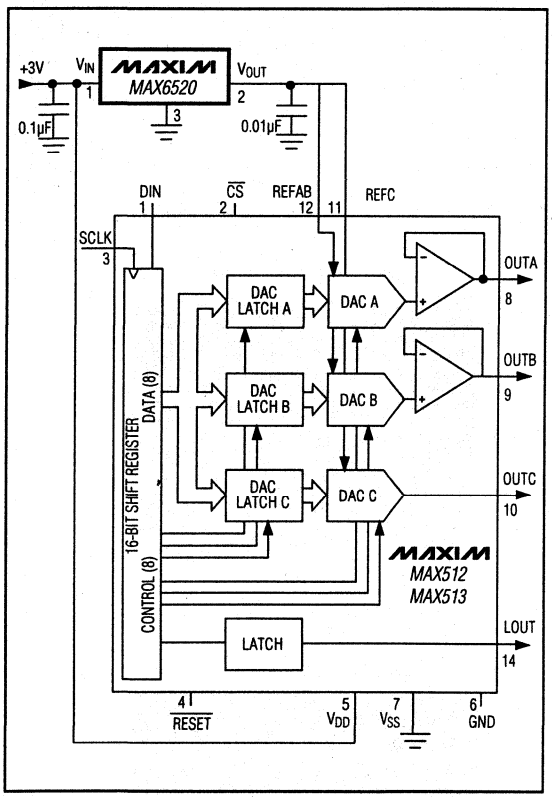


Figure 1. 3V, Triple, 8-Bit Serial DAC

Applications Information

Input Bypassing

For the best line-transient performance, decouple the input with a 0.1µF ceramic capacitor as shown in the *Typical Operating Circuit*. Locate the capacitor as close to the device pin as possible. Where transient performance is less important, no capacitor is necessary.

Output Bypass

The MAX6520 performs well without an output decoupling capacitor. If your application requires an output charge reservoir (e.g., to decouple the reference from the input of a DAC), then make sure that the total output capacitive load does not exceed 10nF.

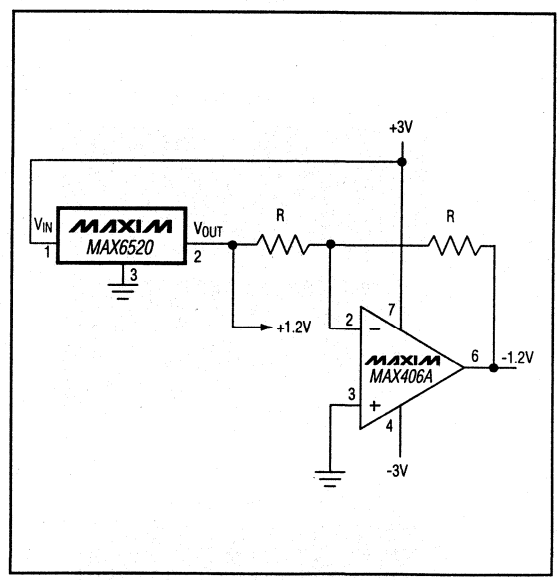
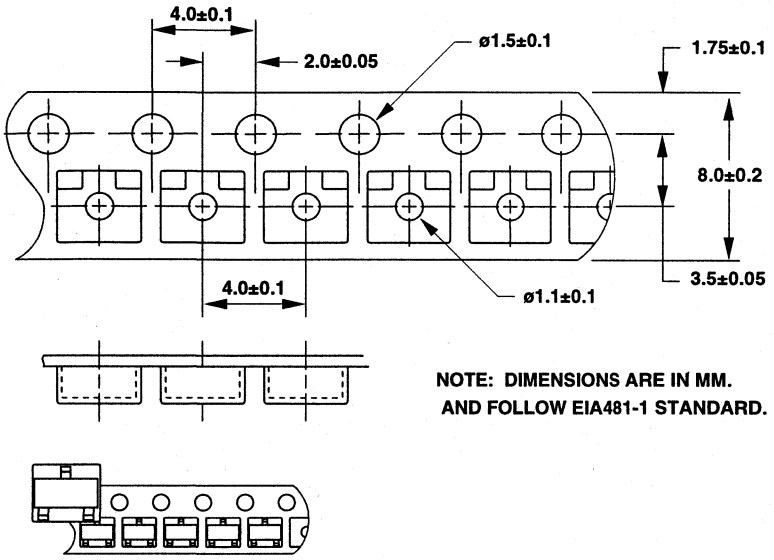


Figure 2. Low-Power ±1.2V Reference

Chip Information

TRANSISTOR COUNT: 39

Tape-and-Reel Information



NOTE: DIMENSIONS ARE IN MM.
AND FOLLOW EIA481-1 STANDARD.

MARKING INFORMATION†

LOT SPECIFIC CODE

AY [XX] = MAX6520

†ICs MAY ALSO BE MARKED WITH FULL PART NAME: MAX6520

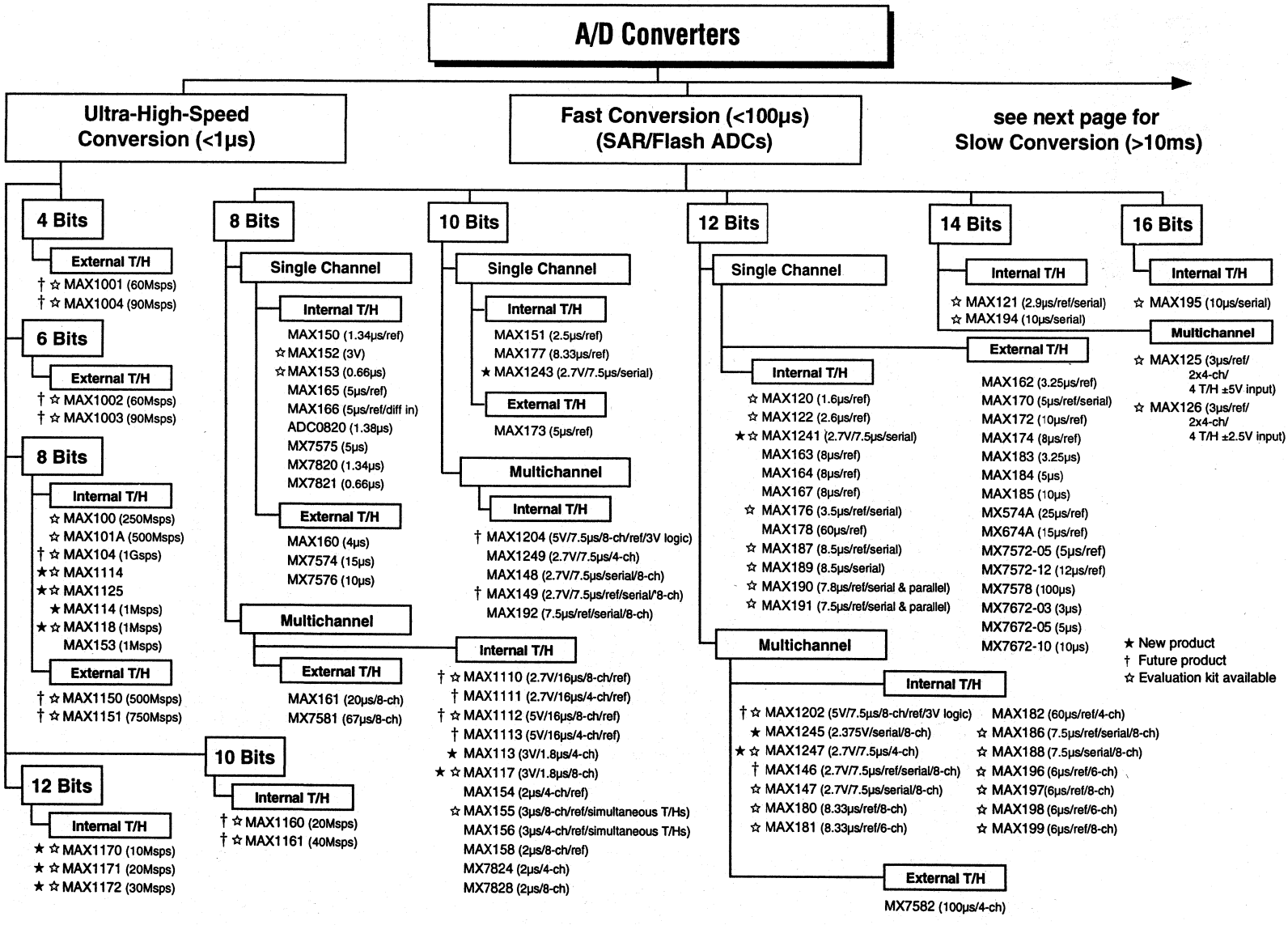
MAXIM

A/D Converters

A/D Converters, Product Tables and Trees 7-2

MAX104	1Gsps, 8-Bit ADC with Track/Hold	7-9*
MAX113	3V, 8-Bit, 4-Channel, Low-Power ADC	7-11
MAX114	5V, 8-Bit, 4-Channel, Low-Power ADC	7-23
MAX117	3V, 8-Bit, 8-Channel, Low-Power ADC	7-11
MAX118	5V, 8-Bit, 8-Channel, Low-Power ADC	7-23
MAX125	2x4-Channel, Simultaneous-Sampling 14-Bit DAS with ±5V Input Range	7-35*
MAX126	2x4-Channel, Simultaneous-Sampling 14-Bit DAS with ±2.5V Input Range	7-35*
MAX146	2.7V, Low-Power, 8-Channel, Serial 12-Bit ADC with Internal Reference	7-37*
MAX147	2.7V, Low-Power, 8-Channel, Serial 12-Bit ADC	7-39
MAX148	2.7V, Low-Power, 8-Channel, Serial 10-Bit ADC	7-59
MAX149	2.7V, Low-Power, 8-Channel, Serial 10-Bit ADC with Internal Reference	7-79*
MAX196	6-Channel, Multi-Range, 5V, 12-Bit DAS with 12-Bit Bus Interface and Fault Protection	7-81
MAX197	8-Channel, Multi-Range, 5V, 12-Bit DAS with 8+4 Bus Interface and Fault Protection	7-97
MAX198	6-Channel, Multi-Range, 5V, 12-Bit DAS with 12-Bit Bus Interface and Fault Protection	7-81
MAX1002	Dual, 6-Bit, 60Msps ADC	7-113*
MAX1003	Dual, 6-Bit, 90Msps ADC	7-113*
MAX1110	+2.7V, 8-Channel, 8-Bit ADC with Serial Interface	7-115*
MAX1111	+2.7V, 4-Channel, 8-Bit ADC with Serial Interface	7-115*
MAX1112	+5V, 8-Channel, 8-Bit ADC with Serial Interface	7-117*
MAX1113	+5V, 4-Channel, 8-Bit ADC with Serial Interface	7-117*
MAX1114	8-Bit, 150Msps ADC	7-119
MAX1125	8-Bit, 300Msps ADC	7-131
MAX1150	8-Bit, 500Msps ADC	7-143
MAX1151	8-Bit, 750Msps ADC	7-151
MAX1160	10-Bit, 20Msps ADC	7-159*
MAX1161	10-Bit, 40Msps ADC	7-161*
MAX1170	12-Bit, 10Msps ADC	7-163
MAX1171	12-Bit, 20Msps ADC	7-175
MAX1172	12-Bit, 30Msps ADC	7-187
MAX1202	Low-Power, 8-Channel, Serial 12-Bit ADC with Programmable Output Logic Level	7-199*
MAX1204	Low-Power, 8-Channel, Serial 10-Bit ADC with Programmable Output Logic Level	7-201*
MAX1241	2.7V, 1-Channel, Serial 12-Bit ADC	7-203
MAX1243	2.7V, 1-Channel, Serial 10-Bit ADC	7-215
MAX1245	2.375V, 8-Channel, Serial 12-Bit ADC	7-227
MAX1247	2.7V, Low-Power, 4-Channel, Serial 12-Bit ADC	7-247
MAX1249	2.7V, Low-Power, 4-Channel, Serial 10-Bit ADC	7-267

*Advance Information–first page of data sheet in preparation.


A/D Converters
Ultra-High-Speed Conversion (<1µs)
Fast Conversion (<100µs) (SAR/Flash ADCs)
see next page for Slow Conversion (>10ms)
4 Bits
External T/H
† ☆ MAX1001 (60Msps)
† ☆ MAX1004 (90Msps)
6 Bits
External T/H
† ☆ MAX1002 (60Msps)
† ☆ MAX1003 (90Msps)
8 Bits
Internal T/H
☆ MAX100 (250Msps)
☆ MAX101A (500Msps)
† ☆ MAX104 (1Gsps)
★☆ MAX1114
★☆ MAX1125
★ MAX114 (1Msps)
★☆ MAX118 (1Msps)
MAX153 (1Msps)
External T/H
† ☆ MAX1150 (500Msps)
† ☆ MAX1151 (750Msps)
12 Bits
Internal T/H
★☆ MAX1170 (10Msps)
★☆ MAX1171 (20Msps)
★☆ MAX1172 (30Msps)
8 Bits
Single Channel
Internal T/H
MAX150 (1.34µs/ref)
☆ MAX152 (3V)
☆ MAX153 (0.66µs)
MAX165 (5µs/ref)
MAX166 (5µs/ref/diff in)
ADC0820 (1.38µs)
MX7575 (5µs)
MX7820 (1.34µs)
MX7821 (0.66µs)
External T/H
MAX160 (4µs)
MX7574 (15µs)
MX7576 (10µs)
Multichannel
External T/H
MAX161 (20µs/8-ch)
MX7581 (67µs/8-ch)
10 Bits
Internal T/H
† ☆ MAX1160 (20Msps)
† ☆ MAX1161 (40Msps)
10 Bits
Single Channel
Internal T/H
MAX151 (2.5µs/ref)
MAX177 (8.33µs/ref)
★ MAX1243 (2.7V/7.5µs/serial)
External T/H
MAX173 (5µs/ref)
Multichannel
Internal T/H
† MAX1204 (5V/7.5µs/8-ch/ref/3V logic)
MAX1249 (2.7V/7.5µs/4-ch)
MAX148 (2.7V/7.5µs/serial/8-ch)
† MAX149 (2.7V/7.5µs/ref/serial/8-ch)
MAX192 (7.5µs/ref/serial/8-ch)
Internal T/H
† ☆ MAX1110 (2.7V/16µs/8-ch/ref)
† MAX1111 (2.7V/16µs/4-ch/ref)
† ☆ MAX1112 (5V/16µs/8-ch/ref)
† MAX1113 (5V/16µs/4-ch/ref)
★ MAX113 (3V/1.8µs/4-ch)
★☆ MAX117 (3V/1.8µs/8-ch)
MAX154 (2µs/4-ch/ref)
☆ MAX155 (3µs/8-ch/ref/simultaneous T/Hs)
MAX156 (3µs/4-ch/ref/simultaneous T/Hs)
MAX158 (2µs/8-ch/ref)
MX7824 (2µs/4-ch)
MX7828 (2µs/8-ch)
12 Bits
Single Channel
Internal T/H
☆ MAX120 (1.6µs/ref)
☆ MAX122 (2.6µs/ref)
★☆ MAX1241 (2.7V/7.5µs/serial)
MAX163 (8µs/ref)
MAX164 (8µs/ref)
MAX167 (8µs/ref)
☆ MAX176 (3.5µs/ref/serial)
MAX178 (60µs/ref)
☆ MAX187 (8.5µs/ref/serial)
☆ MAX189 (8.5µs/serial)
☆ MAX190 (7.8µs/ref/serial & parallel)
☆ MAX191 (7.5µs/ref/serial & parallel)
External T/H
MAX162 (3.25µs/ref)
MAX170 (5µs/ref/serial)
MAX172 (10µs/ref)
MAX174 (8µs/ref)
MAX183 (3.25µs)
MAX184 (5µs)
MAX185 (10µs)
MX574A (25µs/ref)
MX674A (15µs/ref)
MX7572-05 (5µs/ref)
MX7572-12 (12µs/ref)
MX7578 (100µs)
MX7672-03 (3µs)
MX7672-05 (5µs)
MX7672-10 (10µs)
Multichannel
Internal T/H
† ☆ MAX1202 (5V/7.5µs/8-ch/ref/3V logic)
★ MAX1245 (2.375V/serial/8-ch)
★☆ MAX1247 (2.7V/7.5µs/4-ch)
† MAX146 (2.7V/7.5µs/ref/serial/8-ch)
☆ MAX147 (2.7V/7.5µs/serial/8-ch)
☆ MAX180 (8.33µs/ref/8-ch)
☆ MAX181 (8.33µs/ref/6-ch)
MAX182 (60µs/ref/4-ch)
☆ MAX186 (7.5µs/ref/serial/8-ch)
☆ MAX188 (7.5µs/serial/8-ch)
☆ MAX196 (6µs/ref/6-ch)
☆ MAX197(6µs/ref/8-ch)
☆ MAX198 (6µs/ref/6-ch)
☆ MAX199 (6µs/ref/8-ch)
External T/H
MX7582 (100µs/4-ch)
14 Bits
Internal T/H
☆ MAX121 (2.9µs/ref/serial)
☆ MAX194 (10µs/serial)
16 Bits
Internal T/H
☆ MAX195 (10µs/serial)
Multichannel
☆ MAX125 (3µs/ref/ 2x4-ch/ 4 T/H ±5V input)
☆ MAX126 (3µs/ref/ 2x4-ch/ 4 T/H ±2.5V input)
★ New product
† Future product
☆ Evaluation kit available

A/D Converters

see previous page for
Fast Conversion (<100µs)
and Ultra-High-Speed
Conversion (<1µs)

Slow Conversion (>10ms) (Integrating & Σ - Δ ADCs)

LCD DISPLAY

MAX130 (3 1/2 D, B/G)
MAX131 (3 1/2 D, B/G, L)
MAX136 (3 1/2 D, B/G, HOLD, L)
MAX138 (3 1/2 D, B/G, S/S)
ICL7106 (3 1/2 D, Z)
ICL7116 (3 1/2 D, Z, HOLD)
ICL7126 (3 1/2 D, Z, L)
ICL7129A (4 1/2 D)
ICL7136 (3 1/2 D, Z, L)

LED DISPLAY

MAX139 (3 1/2 D, B/G, S/S)
MAX140 (3 1/2 D, B/G, S/S)
ICL7107 (3 1/2 D, Z)
ICL7117 (3 1/2 D, Z, HOLD)
ICL7137 (3 1/2 D, Z, L)

µP INTERFACE

☆ MAX132 (±18 bit, serial, L)
☆ MAX133 (±40,000 count, L)
☆ MAX134 (±40,000 count, L)
MAX135 (±15 bit, L)
ICL7109 (12 bit, Z)
ICL7135 (±20,000 count)

Σ - Δ ADCs

☆ MAX110 (±14 bit, serial, no ext. components, L)

☆ MAX111 (±14 bit, serial, no ext. components, L)

★ New product
☆ Evaluation kit available

NOTES: HOLD – Includes display-hold input
S/S – Includes +5V single supply
B/G – Includes bandgap reference
Z – Includes zener reference
L – Low power

Sampling A/D Converters

Part Number	Resolution (Bits)	Sample Rate (kHz max)	Conversion Time (µs max)	Input Channels	Reference Voltage* (V)	Data-Bus Interface (Bits)	Supply Voltage (V)	Input Ranges (V)	EV Kit	Features	Price† 1000-up ($)
MAX114	8	1000	0.66	4	E	µP/8	+5	+5		5V, 8-bit, 4-channel ADC with power-down	3.30
MAX118	8	1000	0.66	8	E	µP/8	+5	+5	Yes	5V, 8-bit, 8-channel ADC with power-down	3.40
MAX153	8	1000	0.66	1	E	µP/8	+5 or ±5	+5 or ±2.5	Yes	High-speed ADC with 1µA power-down	2.95
MAX150	8	500	1.34	1	E or I/+2.5	µP/8	+5	+5		Complete ADC with T/H and reference	5.85
MAX113	8	400	1.8	4	E	µP/8	+2.7 to +3.6	+3		3V, 8-bit, 4-channel ADC with power-down	3.45
MAX117	8	400	1.8	8	E	µP/8	+2.7 to +3.6	+3	Yes	3V, 8-bit, 8-channel ADC with power-down	3.55
MAX152	8	400	1.8	1	E	µP/8	+3 or ±3	+3 or ±1.5	Yes	3V ADC with 1µA power-down	3.10
MAX154	8	400	2	4	E or I/+2.5	µP/8	+5	+5		4-channel ADC with T/H and reference	6.45
MAX158	8	400	2	8	E or I/+2.5	µP/8	+5	+5		8-channel ADC with T/H and reference	6.85
MAX155	8	250	3.6	8	E or I/+2.5	µP/8	+5 or ±5	+2.5 or ±2.5	Yes	8-channel ADC with simult. T/Hs and reference	9.50
MAX156	8	250	3.6	4	E or I/+2.5	µP/8	+5 or ±5	+2.5 or ±2.5		4-channel ADC with simult. T/Hs and reference	7.19
MAX165	8	200	5	1	E or I/+1.23	µP/8	+5	+5		Low-cost sampling ADC with reference	3.95
MAX166	8	200	5	1	E or I/+1.23	µP/8	+5	+5		Differential-input complete ADC	4.20
MAX1110	8	50	16	8	E or I/+2.048	Serial	+2.7 to +5.5	$+V_{REF}$ or $\pm V_{REF}/2$	Yes	2.7V, 8-channel, 250µA ADC with power-down	††
MAX1111	8	50	16	4	E or I/+2.048	Serial	+2.7 to +5.5	$+V_{REF}$ or $\pm V_{REF}/2$		2.7V, 4-channel, 250µA ADC with power-down	††
MAX1112	8	50	16	8	E or I/+4.096	Serial	+5	$+V_{REF}$ or $\pm V_{REF}/2$	Yes	5V, 8-channel, 250µA ADC with power-down	††
MAX1113	8	50	16	4	E or I/+4.096	Serial	+5	$+V_{REF}$ or $\pm V_{REF}/2$		5V, 4-channel, 250µA ADC with power-down	††
MAX151	10	300	2.5	1	E or I/+4.0	µP/10	±5	+5		Sampling ADC with ref	7.95
MAX1249	10	133	7.5	4	E	Serial	+2.7 to +5.25	$+V_{REF}$ or $\pm V_{REF}/2$		2.7V, 10-bit, low-power, serial, 4-channel ADC	3.95
MAX192	10	133	7.5	8	I/+4.096	Serial	+5	+5 or ±2.5		Low power, low cost, small package	2.95**
MAX148	10	133	7.5	8	E	Serial	+2.7 to +5.25	+2.5, ±1.25		2.7V, 8-channel, low-power ADC	4.10
MAX149	10	133	7.5	8	I/+2.5	Serial	+2.7 to +3.6	+2.5, ±1.25		2.7V, 8-channel, low-power ADC w/reference	††
MAX177	10 or 12	100	8.33	1	I/-5.25	µP/8 or 12	+5 & -12 to -15	±2.5		MAX167 with 10-bit accuracy	7.96
MAX1243	10	75	7.5	1	E	Serial	+2.7 to +5.25	$+V_{REF}$ or $\pm V_{REF}/2$		2.7V, 10-bit serial ADC in 8-pin package	3.45
MAX120	12	500	1.6	1	I/-5.0	µP/12	+5 & -12 to -15	±5	Yes	High-speed complete sampling ADC	11.50
MAX122	12	333	2.6	1	I/-5.0	µP/12	+5 & -12 to -15	±5	Yes	High-speed complete sampling ADC	8.95
MAX176	12	250	3.5	1	I/-5.0	Serial	+5 & -12 to -15	±5	Yes	Serial ADC, 8-pin miniDIP with T/H	9.85
MAX1247	12	133	7.5	4	E	Serial	+2.7 to +5.25	$+V_{REF}$ or $\pm V_{REF}/2$	Yes	2.7V, 12-bit, low-power, serial, 4-channel ADC	††
MAX146	12	133	7.5	8	I/+2.5	Serial	+2.7 to +3.6	+2.5, ±1.25		2.7V, 8-channel, low-power ADC w/reference	††
MAX147	12	133	7.5	8	E	Serial	+2.7 to +5.25	+2.5, ±1.25	Yes	2.7V, 8-channel, low-power ADC	5.95
MAX186	12	133	7.5	8	E or I/+4.096	Serial	+5	+5	Yes	7mW, 10µA power-down	6.75
MAX188	12	133	7.5	8	E	Serial	+5	+5	Yes	MAX186 without reference	6.25
MAX196	12	100	6	6	E or I/+4.096	µP/12	+5	±10, +10, ±5, +5	Yes	Multi-range, fault protected, 6-channel	9.90
MAX197	12	100	6	8	E or I/+4.096	µP/8	+5	±10, +10, ±5, +5	Yes	Multi-range, fault protected, 8-channel	9.90
MAX198	12	100	6	6	E or I/+4.096	µP/12	+5	±4, +4, ±2, +2	Yes	Multi-range, fault protected, 6-channel	9.90
MAX199	12	100	6	8	E or I/+4.096	µP/8	+5	±4, +4, ±2, +2	Yes	Multi-range, fault protected, 8-channel	9.90
MAX1245	12	100	7.5	8	E	Serial	+2.375 to +3.6	$+V_{REF}$ or $\pm V_{REF}/2$		2.375V, 12-bit 8-channel serial ADC	6.25
MAX191	12	100	7.5	1	E or I/+4.096	Serial and µP/8	+5 or ±5	+5 or ±2.5	Yes	15mW, 20µA power-down	9.60
MAX163	12	100	8.33	1	I/-5.0	µP/8 or 12	+5 & -12 to -15	+5		Complete sampling ADC with reference	14.40
MAX164	12	100	8.33	1	I/-5.0	µP/8 or 12	+5 & -12 to -15	±5		Complete sampling ADC with reference	14.40
MAX167	12	100	8.33	1	I/-5.0	µP/8 or 12	+5 & -12 to -15	±2.5		Complete sampling ADC with reference	14.40
MAX180	12	100	8.33	8	E or I/-5.0	µP/8 or 12	+5 & -12 to -15	+5 or ±2.5	Yes	Data-acquisition system	12.75
MAX181	12	100	8.33	6	E or I/-5.0	µP/8 or 12	+5 & -12 to -15	+5 or ±2.5	Yes	Data-acquisition system	12.75
MAX1241	12	75	7.5	1	E	Serial	+2.7 to +5.25	$+V_{REF}$ or $\pm V_{REF}/2$	Yes	2.7V, 12-bit serial ADC in 8-pin package	4.95
MAX190	12	75	7.8	1	E or I/+4.096	Serial and µP/8	+5	+5	Yes	Use MAX191 for new designs	10.00
MAX187	12	75	8.5	1	E or I/+4.096	Serial	+5	+5	Yes	7mW, 8-pin package	6.45
MAX189	12	75	8.5	1	E	Serial	+5	+5	Yes	MAX187 without reference	5.95
MAX178	12	20	60	1	E or I/+5.0	µP/8 or 12	±5 & +15	+5		1LSB TUE, has T/H and reference	15.24
MAX182	12	20	60	4	E or I/+5.0	µP/8 or 12	±5 & +15	+5		1LSB TUE, has T/H and reference	17.55
MAX170	12	125***	5	1	I/-5.25	Serial	+5 & -12 to -15	+5		Serial ADC, 8-pin miniDIP with external T/H	11.96

* E = external reference, I = internal reference

** 25,000 pc. price, factory direct

*** With external track/hold

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

†† Future product—contact factory for pricing and availability. Specifications are preliminary.

Part Number	Resolution (Bits)	Sample Rate (kHz max)	Conversion Time (µs max)	Input Channels	Reference Voltage* (V)	Data-Bus Interface (Bits)	Supply Voltage (V)	Input Ranges (V)	EV Kit	Features	Price† 1000-up ($)
MAX121	14	308	2.9	1	I/-5.0	Serial	+5 & -12 to -15	±5	Yes	High-speed, complete sampling ADC with DSP interface, 16-pin pkg.	12.00
MAX194	14	85	9.4	1	E	Serial	±5	+5 or ±5	Yes	14-bit, high-speed serial ADC	14.00
MAX195	16	85	10	1	E	Serial	±5	+5 or ±5	Yes	High-speed serial 16-pin ADC	24.00

Low-Power A/D Converters

Part Number	Resolution (Bits)	Input Channels	Data-Bus Interface (Bits)	Supply Voltage (V)	Supply Current (mA)	Power-Down Current (µA)	Conversion Time (µs max)	Reference Voltage* (V)	EV Kit	Features	Price† 1000-up ($)
MAX113	8	4	µP/8	+3 to +3.6	1.5	1	1.8	E		3V, 8-bit, 4-channel ADC with power-down	3.45
MAX117	8	8	µP/8	+3 to +3.6	1.5	1	1.8	E	Yes	3V, 8-bit, 8-channel ADC with power-down	3.55
MAX152	8	1	µP/8	+3 or ±3	1.5	1	1.8	E	Yes	3V ADC with 1µA power-down	3.10
MAX114	8	4	µP/8	+5	8	1	0.66	E		5V, 8-bit, 4-channel ADC with power-down	3.30
MAX118	8	8	µP/8	+5	8	1	0.66	E	Yes	5V, 8-bit, 8-channel ADC with power-down	3.40
MAX153	8	1	µP/8	+5 or ±5	8	1	0.66	E	Yes	High-speed ADC with 1µA power-down	2.95
MAX1110	8	8	Serial	+2.7 to +5.5	0.25	2	16	E or I/+2.048	Yes	2.7V 8-channel 250µA ADC with power-down	††
MAX1111	8	4	Serial	+2.7 to +5.5	0.25	2	16	E or I/+2.048		2.7V 4-channel 250µA ADC with power-down	††
MAX1112	8	8	Serial	+5	0.25	2	16	E or I/+4.096	Yes	5V 8-channel 250µA ADC with power-down	††
MAX1113	8	4	Serial	+5	0.25	2	16	E or I/+4.096		5V 4-channel 250µA ADC with power-down	††
MAX1243	10	1	Serial	+2.7 to +5.25	0.9	1	7.5	E		2.7V, 10-bit serial ADC in 8-pin package	3.45
MAX1249	10	4	Serial	+2.7 to +5.25	0.9	1	7.5	E		2.7V, 10-bit, low-power, serial, 4-channel ADC	3.95
MAX148	10	8	Serial	+2.7 to +5.25	0.9	1	7.5	E		2.7V, 8-channel serial ADC	4.10
MAX149	10	8	Serial	+2.7 to +3.6	1.5	1	7.5	I/+2.5		2.7V, 8-channel serial ADC with reference	††
MAX192	10	8	Serial	+5	1.5	2	7.5	I/+4.096		Low power, low cost, small package	2.95**
MAX1204	10	8	Serial	+5 or ±5	1.5	2	7.5	E or I/+4.096		5V 10-bit 8-channel ADC with 3V logic interface	††
MAX1241	12	1	Serial	+2.7 to +5.25	0.9	1	7.5	E	Yes	2.7V, 12-bit serial ADC in 8-pin package	4.95
MAX1245	12	8	Serial	+2.375 to +3.6	0.8	1	7.5	E		2.375V, 12-bit 8-channel serial ADC	6.25
MAX1247	12	4	Serial	+2.7 to +5.25	0.9	1	7.5	E	Yes	2.7V, 12-bit, low-power, serial, 4-channel ADC	5.80
MAX146	12	8	Serial	+2.7 to +3.6	0.9	1	7.5	I/+2.5		2.7V, 8-channel serial ADC with reference	††
MAX147	12	8	Serial	+2.7 to +5.25	1.5	1	7.5	E	Yes	2.7V, 8-channel serial ADC	5.95
MAX186	12	8	Serial	+5 or ±5	1.5	2	7.5	I/+4.096	Yes	7mW, 10µA power-down	6.75
MAX187	12	1	Serial	+5	1.5	2	8.5	I/+4.096	Yes	7mW, 8-pin package	6.45
MAX188	12	8	Serial	+5 or ±5	1	2	7.5	E	Yes	MAX186 without reference	6.25
MAX189	12	1	Serial	+5	1	2	8.5	E	Yes	MAX187 without reference	5.95
MAX191	12	1	Serial and µP/8	+5 or ±5	2.5	20	7.5	E or I/+4.096	Yes	15mW, 20µA power-down	9.60
MAX1202	12	8	Serial	+5 or ±5	1.5	2	7.5	E or I/+4.096		5V 12-bit 8-channel ADC with 3V logic interface	††
MAX194	14	1	Serial	±5	5.5	10	9.4	E	Yes	14-bit, high-speed serial ADC	14.00
MAX110	14 + sign	2	Serial	±5	550µA	1	20ms	E	Yes	Low-power, shutdown mode, dual supplies	4.80
MAX111	14 + sign	2	Serial	+5	640µA	1	20ms	E	Yes	Low-power, shutdown mode, single supply	4.80
MAX135	15 + sign	1	µP/8	±5	60µA	1	10ms	E		High-resolution ADC, <1mW	8.00
MAX195	16	1	Serial	±5	5.5	10	10	E	Yes	High-speed serial 16-pin ADC	24.00
MAX132	18 + sign	1	Serial	±5	60µA	1	10ms	E	Yes	Serial high-resolution ADC, <1mW	8.00

* E = external reference, I = internal reference

** 25,000 pc. price, factory direct

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†† Future product—contact factory for pricing and availability. Specifications are preliminary.

Part Number	Resolution (Bits)	Input Channels	Conversion Time (µs max)	Sample Rate (kHz max)	Reference Voltage (V_{REF})* (V)	Data-Bus Interface (Bits)	Supply Voltage (V)	Input Ranges (V)	EV Kit	Features	Price† 1000-up ($)
MAX114	8	4	0.66	1000	E	µP/8	+5	+5 or ±2.5		5V, 4-channel ADC with 1µA power-down	3.30
MAX113	8	4	1.8	400	E	µP/8	+3	+3 or ±1.5		3V, 4-channel ADC with 1µA power-down	3.45
MAX154	8	4	2	400	E or I/+2.5	µP/8	+5	+5		4-channel ADC with T/H and reference	6.45
MX7824	8	4	2	400	E	µP/8	+5	+5		Plug-in replacement for AD7824	8.33
MAX156	8	4	3.6	250	E or I/+2.5	µP/8	+5 or ±5	+2.5 or ±2.5		4-channel ADC with simult. T/Hs and reference	7.19
MAX1111	8	4	16	50	E or I/+2.048	Serial	+2.7 to +5	+V_{REF} or ±V_{REF}		2.7V 8-channel 250µA ADC with power-down	††
MAX1113	8	4	16	50	E or I/+4.096	Serial	+5	+V_{REF} or ±V_{REF}		5V 8-channel 250µA ADC with power-down	††
MAX118	8	8	0.66	1000	E	µP/8	+5	+5 or ±2.5	Yes	5V, 8-channel ADC with 1µA power-down	3.40
MAX117	8	8	1.8	400	E	µP/8	+3	+3 or ±1.5	Yes	3V, 8-channel ADC with 1µA power-down	3.55
MAX158	8	8	2	400	E or I/+2.5	µP/8	+5	+5		8-channel ADC with T/H and reference	6.85
MX7828	8	8	2	400	E	µP/8	+5	+5		Plug-in replacement for AD7828	8.73
MAX155	8	8	3.6	250	E or I/+2.5	µP/8	+5 or ±5	+2.5 or ±2.5	Yes	8-channel ADC with simult. T/Hs and reference	9.50
MAX1110	8	8	16	50	E or I/+2.048	Serial	+2.7 to +5	+V_{REF} or ±V_{REF}	Yes	2.7V 8-channel 250µA ADC with power-down	††
MAX1112	8	8	16	50	E or I/+4.096	Serial	+5	+V_{REF} or ±V_{REF}	Yes	5V 8-channel 250µA ADC with power-down	††
MAX161	8	8	20	–	E	µP/8	+5	+10		8-channel ADC with RAM buffer	11.12
MX7581	8	8	66.6	–	E	µP/8	+5	+10		Plug-in replacement for AD7581	11.08
MAX1249	10	4	7.5	133	E	Serial	+2.7 to +5.25	+V_{REF} or ±V_{REF}/2		2.7V, 10-bit, low-power serial ADC	3.95
MAX1204	10	8	7.5	133	E or I/+4.096	Serial	+5 or ±5	+V_{REF} or ±V_{REF}		5V, 10-bit, 8-channel ADC with 3V logic interface	††
MAX192	10	8	7.5	133	I/+4.096	Serial	+5	+5 or ±2.5		Low power, low cost, small package	2.95**
MAX148	10	8	7.5	133	E	Serial	+2.7 to +5.25	+V_{REF} or ±V_{REF}/2		2.7V, lowest power 10-bit ADC	4.10
MAX149	10	8	7.5	133	I/+2.5	Serial	+2.7 to +3.6	+2.5 to +1.25		8-channel serial ADC with reference	††
MAX1247	12	4	7.5	133	E	Serial	+2.7 to +5.25	+V_{REF} or ±V_{REF}/2	Yes	2.7V, 12-bit, low-power serial ADC	5.80
MAX182	12	4	60	20	E or I/+5.0	µP/8 or 12	±5 & +15	+5		1LSB TUE, has T/H and ref	17.55
MX7582	12	4	100	–	E	µP/8 or 12	±5 & +15	+5		Plug-in replacement for AD7582	19.50
MAX196	12	6	6	100	E or I/+4.096	µP/12	+5	±10, +10, ±5, +5	Yes	Multi-range, fault protected	9.90
MAX198	12	6	6	100	E or I/+4.096	µP/12	+5	±4, +4, ±2, +2	Yes	Multi-range, fault protected	9.90
MAX181	12	6	8.33	100	E or I/-5.0	µP/8 or 12	+5 & -12 to -15	+5 or ±2.5	Yes	Data-acquisition system	12.75
MAX197	12	8	6	100	E or I/+4.096	µP/8	+5	±10, +10, ±5, +5	Yes	Multi-range, fault protected	9.90
MAX199	12	8	6	100	E or I/+4.096	µP/8	+5	±4, +4, ±2, +2	Yes	Multi-range, fault protected	9.90
MAX1202	12	8	7.5	133	E or I/+4.096	Serial	+5 or ±5	+V_{REF} or ±V_{REF}	Yes	5V, 12-bit, 8-channel ADC with 3V logic interface	††
MAX1245	12	8	7.5	100	E	Serial	+2.375 to +3.6	+V_{REF} or ±V_{REF}/2		2.375V 12-Bit, 8-Ch serial ADC	3.95
MAX146	12	8	7.5	133	I/+2.5	Serial	+2.7 to +3.6	+2.5 or ±1.25		2.7V, 8-channel serial ADC with reference	††
MAX147	12	8	7.5	133	E	Serial	+2.7 to +5.25	+V_{REF} or ±V_{REF}/2	Yes	2.7V, lowest power 12-bit ADC	5.95
MAX186	12	8	7.5	133	E or I/+4.096	Serial	+5 or ±5	+5 or ±2.5	Yes	7mW, 10µA power-down	8.95
MAX188	12	8	7.5	133	E	Serial	+5 or ±5	+5 or ±2.5	Yes	MAX186 without reference	8.45
MAX180	12	8	8.33	100	E or I/-5.0	µP/8 or 12	+5 & -12 to -15	+5 or ±2.5	Yes	Data-acquisition system	12.75
MAX125	14	4	3	75	E or I/+2.5	µP/14	±5	±5	Yes	14-bit 2x4 channels, simultaneous T/H, ±5V input	††
MAX126	14	4	3	75	E or I/+2.5	µP/14	±5	±2.5	Yes	14-bit 2x4 channels, simultaneous T/H, ±2.5V input	††
MAX110	14 + sign	2	20ms	–	E	Serial	±5	±3	Yes	Low power, shutdown mode, dual supplies	4.80
MAX111	14 + sign	2	20ms	–	E	Serial	+5	±2	Yes	Low power, shutdown mode, single supply	4.80

* E = external reference, I = internal reference

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†† Future product—contact factory for pricing and availability. Specifications are preliminary.

Part Number	Resolution (Bits)	Input Channels	Conversion Time (µs max)	Sample Rate (kHz max)	Reference Voltage (V_{REF})* (V)	Data-Bus Interface (Bits)	Supply Voltage (V)	Input Ranges (V)	EV Kit	Features	Price† 1000-up ($)
MAX1247	12	4	7.5	133	E	Serial	+2.7 to +5.25	+V_{REF} or ±V_{REF}/2	Yes	2.7V, 12-bit, low-power serial ADC	5.80
MAX182	12	4	60	20	E or I/+5.0	µP/8 or 12	±5 & +15	+5		1LSB TUE, has T/H and ref	17.55
MX7582	12	4	100	–	E	µP/8 or 12	±5 & +15	+5		Plug-in replacement for AD7582	19.50
MAX196	12	6	6	100	E or I/+4.096	µP/12	+5	±10, +10, ±5, +5	Yes	Multi-range, fault protected	9.90
MAX198	12	6	6	100	E or I/+4.096	µP/12	+5	±4, +4, ±2, +2	Yes	Multi-range, fault protected	9.90
MAX181	12	6	8.33	100	E or I/-5.0	µP/8 or 12	+5 & -12 to -15	+5 or ±2.5	Yes	Data-acquisition system	12.75
MAX197	12	8	6	100	E or I/+4.096	µP/8	+5	±10, +10, ±5, +5	Yes	Multi-range, fault protected	9.90
MAX199	12	8	6	100	E or I/+4.096	µP/8	+5	±4, +4, ±2, +2	Yes	Multi-range, fault protected	9.90
MAX1245	12	8	7.5	100	E	Serial	+2.375 to +3.6	+V_{REF} or ±V_{REF}/2		2.375V 12-Bit, 8-Ch serial ADC	3.95
MAX146	12	8	7.5	133	I/+2.5	Serial	+2.7 to +3.6	+2.5 or ±1.25		2.7V, 8-channel serial ADC with reference	††
MAX147	12	8	7.5	133	E	Serial	+2.7 to +5.25	+V_{REF} or ±V_{REF}/2	Yes	2.7V, lowest power 12-bit ADC	5.95
MAX186	12	8	7.5	133	E or I/+4.096	Serial	+5 or ±5	+5 or ±2.5	Yes	7mW, 10µA power-down	8.95
MAX188	12	8	7.5	133	E	Serial	+5 or ±5	+5 or ±2.5	Yes	MAX186 without reference	8.45
MAX180	12	8	8.33	100	E or I/-5.0	µP/8 or 12	+5 & -12 to -15	+5 or ±2.5	Yes	Data-acquisition system	12.75
MAX110	14 + sign	2	20ms	–	E	Serial	±5	±3	Yes	Low power, shutdown mode, dual supplies	4.80
MAX111	14 + sign	2	20ms	–	E	Serial	+5	±2	Yes	Low power, shutdown mode, single supply	4.80

Integrating A/D Converters

Part Number	Resolution (digits)	Resolution (counts)	Output Type	Supply Voltage (V)	Supply Current (mA), max(typ)	References	EV Kit	Features	Price† 1000-up ($)
DUAL-SLOPE ADCs									
MAX130	3 1/2	±2000	LCD	+4.5 to +14	0.25(0.1)	Bandgap		Replacement for ICL7106	4.86
MAX131	3 1/2	±2000	LCD	+4.5 to +14	0.1(0.06)	Bandgap		Replacement for ICL7136	4.86
MAX136	3 1/2	±2000	LCD	+9	0.15(0.06)	Bandgap		Hold function, low power	4.32
MAX138	3 1/2	±2000	LCD	+2.25 to +7	0.8(0.2)	Bandgap		± inputs with single supply	4.40
ICL7106	3 1/2	±2000	LCD	+9	1.8(0.6)	Zener		For digital multimeters	4.32
ICL7116	3 1/2	±2000	LCD	+9	1.8(0.8)	Zener		ICL7106 with display hold	4.32
ICL7126	3 1/2	±2000	LCD	+9	0.1(0.06)	Zener		Use ICL7136 for new designs	4.32
ICL7136	3 1/2	±2000	LCD	+9	0.1(0.06)	Zener		Low power/noise ICL7106	4.32
MAX139	3 1/2	±2000	LED	+5	0.8(0.2)	Bandgap		± inputs with single supply	4.40
MAX140	3 1/2	±2000	LED	+5	0.8(0.2)	Bandgap		Low segment current (2mA)	4.40
ICL7107	3 1/2	±2000	LED	+9	1.8(0.6)	Zener		For digital panel meters	4.32
ICL7117	3 1/2	±2000	LED	±5	1.8(0.8)	Zener		ICL7107 with display hold	4.32
ICL7137	3 1/2	±2000	LED	±5	0.2(0.06)	Zener		Low power when LEDs off	4.32
MAX133	3 3/4	±40,000	µP	+9	0.2(0.09)	External	Yes	20 conv/sec, ±10µV resolution	9.75
MAX134	3 3/4	±40,000	µP	±5	0.2(0.09)	External	Yes	20 conv/sec, ±10µV resolution	9.75
ICL7109	12 bits + sign	±4096	8-/16-bit µP/UART	±5	1.5(0.7)	Zener		3-state binary outputs	5.10
ICL7129A	4 1/2	±20,000	Triplexed LCD	+9	1.4(1)	External		Lowest noise ±3µV	7.96
ICL7135	4 1/2	±20,000	Multiplexed BCD	±5	2(1)	External		For DMM, DPM, data loggers	5.48
MAX135	15 bits + sign	±20,000	µP/8	±5	0.125(0.06)	External		Three-state twos-complement outputs	8.00
MAX132	18 bits + sign	±260,000	Serial µP	±5	0.125(0.06)	External	Yes	Serial high-resolution ADC, <1mW	8.00
SIGMA-DELTA ADCs									
MAX110	14 bits + sign	–	Serial	±5	0.95(0.55)	External	Yes	No external components, low power, dual supplies	4.80
MAX111	14 bits + sign	–	Serial	+5	1.2(0.64)	External	Yes	No external components, low power, single supply	4.80

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Ultra-High-Speed A/D Converters

Part Number	Resolution (Bits)	Sample Rate (Msps max)	Input Channels	Reference Voltage* (V)	Data-Bus Interface (Bits)	Supply Voltage (V)	Input Ranges (V)	EV Kit	Features	Price† 1000-up ($)
MAX1001	4	60	2	I	Parallel	+5	±250mV, ±500mV	Yes	Dual ADC with osc & PGA	††
MAX1004	4	90	2	I	Parallel	+5 & +3.3	±250mV, ±500mV	Yes	Dual ADC with osc & PGA	††
MAX1002	6	60	2	I	Parallel	+5	±250mV, ±500mV	Yes	Dual ADC with osc & PGA	††
MAX1003	6	90	2	I	Parallel	+5 & +3.3	±250mV, ±500mV	Yes	Dual ADC with osc & PGA	††
MAX118	8	1	8	E	µP/8	+5	+5	Yes	5V, 8-bit, 8-channel ADC with power-down	3.40
MAX153	8	1	1	E	Parallel	+5 or ±5	+5 or ±2.5	Yes	1µA shutdown, SSOP package	6.63
MAX1114	8	150	1	E	Parallel	-5.2	0 to +2	Yes	Wide bandwidth, high SNR, grades 8	57.70**
MAX100	8	250	1	E	Parallel	+5 & -5.2	±0.27	Yes	50Ω I/P, highest bandwidth	‡
MAX1125	8	300	1	E	Parallel	-5.2	0 to +2	Yes	Wide bandwidth, demuxed output	80.70**
MAX101A	8	500	1	E	Parallel	+5 & -5.2	±0.27	Yes	50Ω I/P, highest bandwidth	‡
MAX1150	8	500	1	E	Parallel	-5.2	0 to +2	Yes	Wide bandwidth, demuxed output	††
MAX1151	8	750	1	E	Parallel	-5.2	0 to +2	Yes	Wide bandwidth, demuxed output	††
MAX104	8	1000	1	E	Parallel	±5	300mV	Yes	7.3 ENOB at 500, demuxed outputs	††
MAX1160	10	20	1	E	Parallel	+5	±2	Yes	Internal, 9pF capacitance	††
MAX1161	10	40	1	E	Parallel	+5	±2	Yes	Internal, 9pF capacitance	††
MAX1170	12	10	1	E	Parallel	+5	±2	Yes	Low input capacitance, high SFDR	‡
MAX1171	12	20	1	E	Parallel	+5	±2	Yes	Low input capacitance, high SFDR	‡
MAX1172	12	30	1	E	Parallel	+5	±2	Yes	Low input capacitance, high SFDR	‡

General-Purpose A/D Converters[1]

Part Number	Resolution (Bits)	Conversion Time (µs max)	Input Channels	Sample Rate (kHz max)	Reference Voltage* (V)	Data-Bus Interface (Bits)	Supply Voltage (V)	Input Ranges (V)	Features	Price† 1000-up ($)
MX7821	8	0.66	1	500	E	µP/8	+5 or ±5	+5 or ±2.5	Complete ADC with T/H	7.54
MX7820	8	1.34	1	500	E	µP/8	+5	+5	Plug-in replacement for AD7820	7.93
ADC0820	8	1.38	1	400	E	µP/8	+5	+5	Complete ADC with T/H	7.16
MX7824	8	2	4	400	E	µP/8	+5	+5	Plug-in replacement for AD7824	8.33
MX7828	8	2	8	400	E	µP/8	+5	+5	Plug-in replacement for AD7828	8.73
MAX160	8	4	1	–	E	µP/8	+5	+10 or ±5	Ratiometric single-supply ADC	7.20
MX7575	8	5	1	200	E	µP/8	+5	+5	Plug-in replacement for AD7575	3.74
MX7576	8	10	1	–	E	µP/8	+5	+5	Plug-in replacement for AD7576	3.52
MX7574	8	15	1	–	E	µP/8	+5	+10 or ±5	Plug-in replacement for AD7574	4.80
MX7581	8	66.6	8	–	E	µP/8	+5	+10	Plug-in replacement for AD7581	11.08
MAX173	10 or 12	5	1	–	I/-5.25	µP/8 or 12	+5 & -12 to -15	+5	MAX172 with 10-bit accuracy	5.26
MAX162	12	3.25	1	–	I/-5.25	µP/8 or 12	+5 & -12 to -15	+5	High-speed ADC with internal ref	19.20
MAX183	12	3.25	1	–	E	µP/8 or 12	+5 & -12 to -15	+5, ±5 or +10	High-speed ADC	9.00
MX7672-03	12	3.25	1	–	E	µP/8 or 12	+5 & -12	+5, ±5 or +10	Plug-in replacement for AD7672-03	57.38
MAX184	12	5	1	–	E	µP/8 or 12	+5 & -12 to -15	+5, ±5 or +10	High-speed ADC with external ref	8.25
MX7572-05	12	5	1	–	I/-5.25	µP/8 or 12	+5 & -15	+5	Plug-in replacement for AD7572-05	20.00
MX7672-05	12	5	1	–	E	µP/8 or 12	+5 & -12	+5, ±5 or +10	Plug-in replacement for AD7672-05	33.66
MAX174	12	8	1	–	E or I/+10.0	µP/8 or 12	+5 & ±12 to ±15	±5, ±10, +10 or +20	Upgrades AD574A/AD674A	28.13
MAX172	12	10	1	–	I/-5.25	µP/8 or 12	+5 & -12 to -15	+5	Plug-in upgrade for AD7572-12	9.60
MAX185	12	10.4	1	–	E	µP/8 or 12	+5 & -12 to -15	+5, ±5 or +10	High-speed ADC with external ref	7.20
MX7672-10	12	10.4	1	–	E	µP/8 or 12	+5 & -12	+5, ±5 or +10	Plug-in replacement for AD7672-05	25.25
MX7572-12	12	12	1	–	I/-5.25	µP/8 or 12	+5 & -15	+5	Plug-in replacement for AD7572-12	14.00
MX674A	12	15	1	–	E or I/+10.0	µP/8 or 12	+5 & ±12 to ±15	±5, ±10, +10 or +20	Plug-in replacement for AD674A	23.44
MX574A	12	25	1	–	E or I/+10.0	µP/8 or 12	+5 & ±12 to ±15	±5, ±10, +10 or +20	Plug-in replacement for AD574A	11.97
MAX178	12	60	1	20	E or I/+5.0	µP/8 or 12	±5 & +15	+5	1LSB TUE, has T/H and ref	15.24
MX7578	12	100	1	–	E	µP/8 or 12	±5 & +15	+5	Plug-in replacement for AD7578	16.96
MX7582	12	100	4	–	E	µP/8 or 12	±5 & +15	+5	Plug-in replacement for AD7582	19.50

[1] Not recommended for new designs

* E = external reference, I = internal reference

** 1,000 pc. factory-direct price for B-grade. Contact factory for A-grade pricing.

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

†† Future product—contact factory for pricing and availability. Specifications are preliminary.

‡ Contact factory for pricing.

MAXIM

1Gsps, 8-Bit ADC with Track/Hold

General Description

The MAX104 ECL-compatible, 1Gsps, 8-bit analog-to-digital converter (ADC) allows accurate digitizing of analog signals from DC to 1.5GHz. Designed with Maxim's proprietary advanced GST-2 bipolar process, the MAX104 contains a high-performance track/hold (T/H) amplifier and a quantizer on a single monolithic die.

The innovative design of the internal T/H, which has an exceptionally wide input bandwidth of 1.5GHz, results in high, 7.3 effective bits performance at Nyquist. Special comparator design and decoding circuitry reduce out-of-sequence code errors and provide excellent metastable performance of less than one error per 10^{12} clock cycles. Unlike other ADCs, which can have errors that result in false full-scale or zero-scale outputs, the MAX104 keeps the error magnitude to 1LSB.

The analog input is designed for differential or single-ended use with a 300mV input range. Dual differential ECL-compatible output data paths provide for easy interfacing and include an 8:16 demultiplexer that reduces output data rates to one-half the clock rate. Control inputs are provided for interleaving additional MAX104 devices to increase the effective system sampling rate.

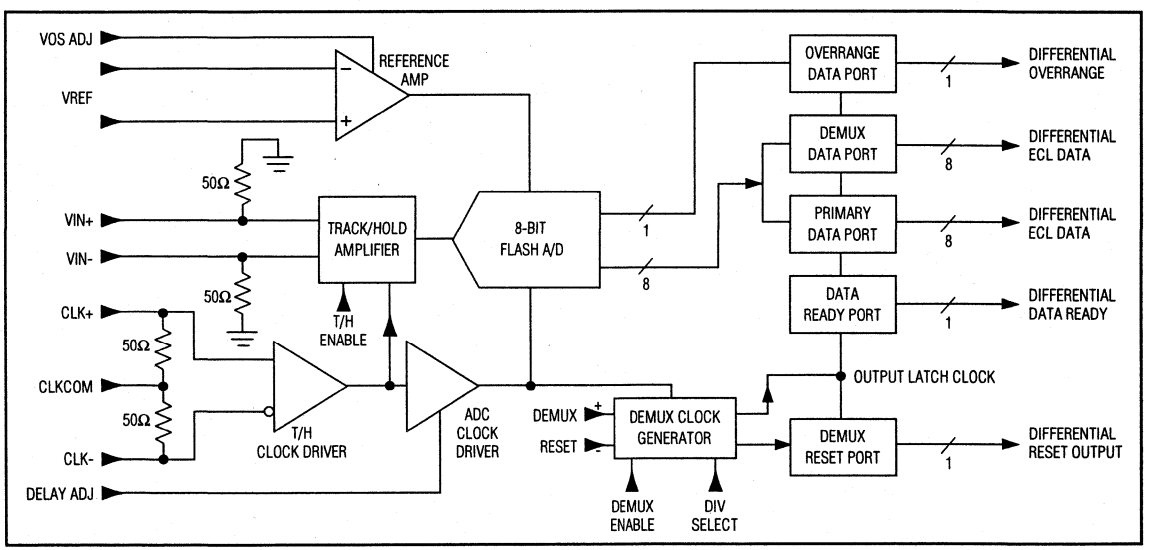
Features

- **1Gsps (min) Conversion Rate**
- **7.3 Effective Bits at 500MHz**
- **Less than ±1/2LSB DNL and INL**
- **50Ω Differential Input**
- **300mV Input Signal Range**
- **On-Chip Differential Reference Amplifier**
- **4.5W Power Dissipation**
- **Latched, ECL-Compatible Differential Outputs with Overrange Bit**
- **Low Error Rate, Less than 10^{-12} Metastable States**
- **Selectable On-Chip 8:16 Demultiplexer**
- **Internal Demux Reset Input**
- **±5V Power Supplies**
- **192-Pin Super Ball Grid Array Package**

Applications

Digital RF/IF Signal Processing
High-Speed Data Acquisition
High-Energy Physics
Medical Systems
Radar/Sonar/ECM Systems

Functional Diagram



For the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

19-1081; Rev 1; 8/96

MAXIM

+3V, 400ksps, 4/8-Channel, 8-Bit ADCs with 1µA Power-Down

General Description

The MAX113/MAX117 are microprocessor-compatible, 8-bit, 4-channel and 8-channel analog-to-digital converters (ADCs). They operate from a single +3V supply and use a half-flash technique to achieve a 1.8µs conversion time (400ksps). A power-down pin ($\overline{PWRDN}$) reduces current consumption to 1µA typical. The devices return from power-down mode to normal operating mode in less than 900ns, allowing large supply-current reductions in burst-mode applications. (In burst mode, the ADC wakes up from a low-power state at specified intervals to sample the analog input signals.) Both converters include a track/hold, enabling the ADC to digitize fast analog signals.

Microprocessor (µP) interfaces are simplified because the ADC can appear as a memory location or I/O port without external interface logic. The data outputs use latched, three-state buffer circuitry for direct connection to an 8-bit parallel µP data bus or system input port. The MAX113/MAX117 input/reference configuration enables ratiometric operation.

The 4-channel MAX113 is available in a 24-pin DIP or SSOP. The 8-channel MAX117 is available in a 28-pin DIP or SSOP. For +5V applications, refer to the MAX114/MAX118 data sheet.

Applications

Battery-Powered Systems
System-Health Monitoring
Communications Systems
Portable Equipment
Remote Data Acquisition

Features

- **+3.0V to +3.6V Single-Supply Operation**
- **4 (MAX113) or 8 (MAX117) Analog Input Channels**
- **Low Power: 1.5mA (operating mode)**
  1µA (power-down mode)
- **Total Unadjusted Error ≤ 1LSB**
- **Fast Conversion Time: 1.8µs per Channel**
- **No External Clock Required**
- **Internal Track/Hold**
- **Ratiometric Reference Inputs**
- **Internally Connected 8th Channel Monitors Reference Voltage (MAX117)**

Ordering Information

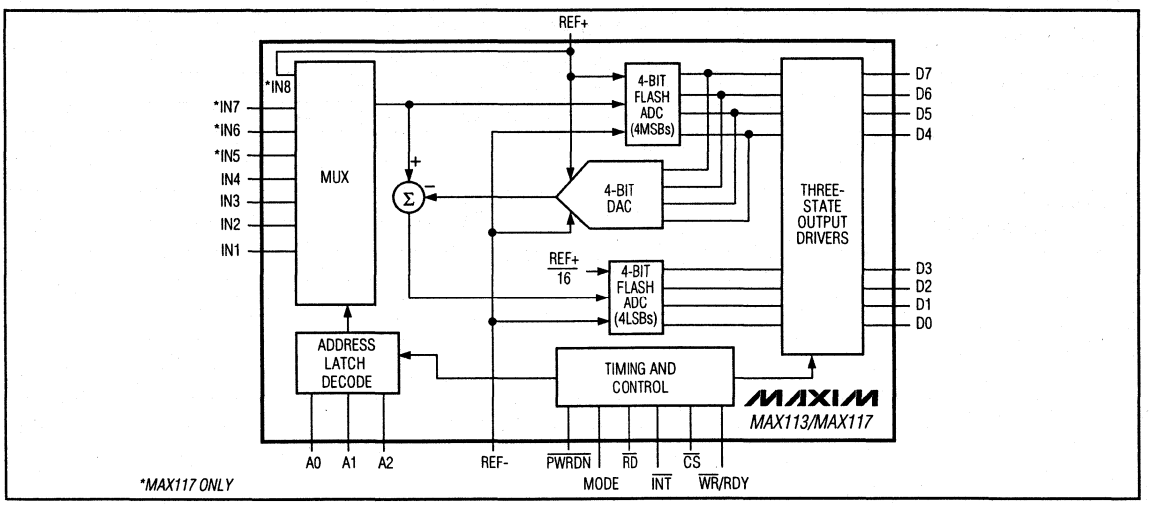
PART	TEMP. RANGE	PIN-PACKAGE
MAX113CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX113CAG	0°C to +70°C	24 SSOP
MAX113C/D	0°C to +70°C	Dice*
MAX113ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX113EAG	-40°C to +85°C	24 SSOP
MAX113MRG	-55°C to +125°C	24 Narrow CERDIP**

Ordering Information continued at end of data sheet.

**Dice are specified at T_A = +25°C, DC parameters only.*
***Contact factory for availability.*

Pin Configuration appears at end of data sheet.

Functional Diagram



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

+3V, 400ksps, 4/8-Channel, 8-Bit ADCs with 1µA Power-Down

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +7V
Digital Input Voltage to GND .....-0.3V to (V_{DD} + 0.3V)
Digital Output Voltage to GND .....-0.3V to (V_{DD} + 0.3V)
REF+ to GND.....-0.3V to (V_{DD} + 0.3V)
REF- to GND.....-0.3V to (V_{DD} + 0.3V)
IN_ to GND .....-0.3V to (V_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
24 Narrow Plastic DIP
(derate 13.33mW/°C above +70°C) 1.08W
24 SSOP (derate 8.00mW/°C above +70°C).....640mW
24 Narrow CERDIP (derate 12.50mW/°C above +70°C) 1W
28 Wide Plastic DIP
(derate 14.29mW/°C above +70°C) 1.14W
28 SSOP (derate 9.52mW/°C above +70°C).....762mW
28 Wide CERDIP (derate 16.67mW/°C above +70°C)....1.33W
Operating Temperature Ranges
MAX113C_G/MAX117C_I .....0°C to +70°C
MAX113E_G/MAX117E_I.....-40°C to +85°C
MAX113MRG/MAX117MJI.....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +3V to +3.6V, REF+ = 3V, REF- = GND, Read Mode (MODE = GND), T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY (Note 1)						
Resolution	N		8			Bits
Total Unadjusted Error	TUE				±1	LSB
Differential Nonlinearity	DNL	No-missing-codes guaranteed			±1	LSB
Zero-Code Error					±1	LSB
Full-Scale Error					±1	LSB
Channel-to-Channel Mismatch					±1/4	LSB
DYNAMIC PERFORMANCE						
Signal-to-Noise Plus Distortion Ratio	SINAD	MAX11_C/E, f_{SAMPLE} = 400kHz, f_{IN} = 30.273kHz	45			dB
		MAX11_M, f_{SAMPLE} = 340kHz, f_{IN} = 30.725kHz	45			
Total Harmonic Distortion	THD	MAX11_C/E, f_{SAMPLE} = 400kHz, f_{IN} = 30.273kHz			-50	dB
		MAX11_M, f_{SAMPLE} = 340kHz, f_{IN} = 30.725kHz			-50	
Spurious-Free Dynamic Range	SFDR	MAX11_C/E, f_{SAMPLE} = 400kHz, f_{IN} = 30.273kHz	50			dB
		MAX11_M, f_{SAMPLE} = 340kHz, f_{IN} = 30.725kHz	50			
Input Full-Power Bandwidth		$V_{IN_}$ = 3Vp-p		0.3		MHz
Input Slew Rate, Tracking			0.28	0.5		V/µs
ANALOG INPUT						
Input Voltage Range	$V_{IN_}$		V_{REF-}		V_{REF+}	V
Input Leakage Current	$I_{IN_}$	GND < $V_{IN_}$ < V_{DD}			±3	µA
Input Capacitance	$C_{IN_}$			32		pF
REFERENCE INPUT						
Reference Resistance	R_{REF}		1	2	4	kΩ
REF+ Input Voltage Range			V_{REF-}		V_{DD}	V
REF- Input Voltage Range			GND		V_{REF+}	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3V to +3.6V, REF+ = 3V, REF- = GND, Read Mode (MODE = GND), T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LOGIC INPUTS							
Input High Voltage	V_{INH}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{PWRDN}$, A0, A1, A2		2			V
		MODE		2.4			
Input Low Voltage	V_{INL}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{PWRDN}$, A0, A1, A2				0.66	V
		MODE				0.8	
Input High Current	I_{INH}	$\overline{CS}$, $\overline{RD}$, $\overline{PWRDN}$, A0, A1, A2				±1	µA
		$\overline{WR}$				±3	
		MODE			15	100	
Input Low Current	I_{INL}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{PWRDN}$, MODE, A0, A1, A2				±1	µA
Input Capacitance (Note 2)	C_{IN}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{PWRDN}$, MODE, A0, A1, A2			5	8	pF
LOGIC OUTPUTS							
Output Low Voltage	V_{OL}	I_{SINK} = 20µA, $\overline{INT}$, D0–D7				0.1	V
		I_{SINK} = 400µA, $\overline{INT}$, D0–D7				0.4	
		RDY, I_{SINK} = 1mA				0.4	
Output High Voltage	V_{OH}	I_{SOURCE} = 20µA, $\overline{INT}$, D0–D7		V_{DD} - 0.1			V
		I_{SOURCE} = 400µA, $\overline{INT}$, D0–D7		V_{DD} - 0.4			
Three-State Current	I_{LKG}	D0–D7, RDY, digital outputs = 0V to V_{DD}				±3	µA
Three-State Capacitance (Note 2)	C_{OUT}	D0–D7, RDY			5	8	pF
POWER REQUIREMENTS							
Supply Voltage	V_{DD}			3.0		3.6	V
V_{DD} Supply Current	I_{DD}	V_{DD} = 3.6V, $\overline{CS}$ = $\overline{RD}$ = 0V, $\overline{PWRDN}$ = V_{DD}	MAX11_C		2.5	5	mA
			MAX11_E/M		2.5	6	
		V_{DD} = 3.0V, $\overline{CS}$ = $\overline{RD}$ = 0V, $\overline{PWRDN}$ = V_{DD}	MAX11_C		1.5	3	
			MAX11_E/M		1.5	3.5	
Power-Down V_{DD} Current		$\overline{CS}$ = $\overline{RD}$ = V_{DD}, $\overline{PWRDN}$ = 0V (Note 3)			1	10	µA
Power-Supply Rejection	PSR	V_{DD} = 3.0V to 3.6V, V_{REF} = 3.0V			±1/16	±1/4	LSB

Note 1: Accuracy measurements performed at V_{DD} = +3.0V. Operation over supply range is guaranteed by power-supply rejection test.
Note 2: Guaranteed by design.
Note 3: Power-down current increases if logic inputs are not driven to GND or V_{DD}.

+3V, 400ksps, 4/8-Channel, 8-Bit ADCs with 1µA Power-Down

TIMING CHARACTERISTICS

(V_{DD} = +3V, T_A = +25°C, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C ALL GRADES			T_A = T_{MIN} to T_{MAX}				UNITS
						MAX117C/E		MAX117M		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Conversion Time (WR-RD Mode)	t_{CWR}	t_{RD} < t_{INTL}, C_L = 100pF (Note 5)			1.8		2.06		2.4	µs
Conversion Time (RD Mode)	t_{CRD}				2.0		2.4		2.6	µs
Power-Up Time	t_{UP}				0.9		1.2		1.4	µs
$\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Setup Time	t_{CSS}		0			0		0		ns
$\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Hold Time	t_{CSH}		0			0		0		ns
$\overline{CS}$ to RDY Delay	t_{RDY}	C_L = 50pF, R_L = 5.1kΩ to V_{DD}			100		120		140	ns
Data Access Time (RD Mode)	t_{ACC0}	C_L = 100pF (Note 5)			t_{CRD} + 100		t_{CRD} + 130		t_{CRD} + 150	ns
$\overline{RD}$ to $\overline{INT}$ Delay (RD Mode)	t_{INTH}	C_L = 50pF		100	160		170		180	ns
Data Hold Time	t_{DH}	(Note 6)			100		130		150	ns
Minimum Acquisition Time	t_{ACQ}	(Note 7)	450			600		700		ns
$\overline{WR}$ Pulse Width	t_{WR}		0.6		10	0.66	10	0.8	10	µs
Delay Between $\overline{WR}$ and $\overline{RD}$ Pulses	t_{RD}		0.8			0.9		1.0		µs
$\overline{RD}$ Pulse Width (WR-RD Mode)	t_{READ1}	t_{RD} < t_{INTL}, determined by t_{ACC1}	400			500		600		ns
Data Access Time (WR-RD Mode)	t_{ACC1}	t_{RD} < t_{INTL}, C_L = 100pF (Note 5)			400		500		600	ns
$\overline{RD}$ to $\overline{INT}$ Delay	t_{RI}				300		340		400	ns
$\overline{WR}$ to $\overline{INT}$ Delay	t_{INTL}	C_L = 50pF		0.7	1.45		1.6		1.8	µs
$\overline{RD}$ Pulse Width (WR-RD Mode)	t_{READ2}	t_{RD} > t_{INTL}, determined by t_{ACC2}	180			220		250		ns
Data Access Time (WR-RD Mode)	t_{ACC2}	t_{RD} > t_{INTL}, C_L = 100pF (Note 5)			180		220		250	ns
$\overline{WR}$ to $\overline{INT}$ Delay	t_{IHWR}	Pipelined mode, C_L = 50pF			180		200		240	ns
Data Access Time After $\overline{INT}$	t_{ID}	Pipelined mode, C_L = 100pF			100		130		150	ns
Multiplexer Address Hold Time	t_{AH}		50			60		70		ns

Note 4: Input control signals are specified with t_r = t_f = 5ns, 10% to 90% of 3V, and timed from a voltage level of 1.3V. Timing delays get shorter at higher supply voltages. See the Conversion Time vs. Supply Voltage graph in the *Typical Operating Characteristics* to extrapolate timing delays at other power-supply voltages.

Note 5: See Figure 1 for load circuit. Parameter defined as the time required for the output to cross 0.66V or 2.0V.

Note 6: See Figure 2 for load circuit. Parameter defined as the time required for the data lines to change 0.5V.

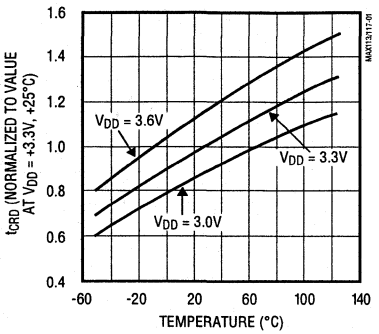
Note 7: Also defined as the Minimum Address-Valid to Convert-Start Time.

+3V, 400ksps, 4/8-Channel, 8-Bit ADCs with 1µA Power-Down

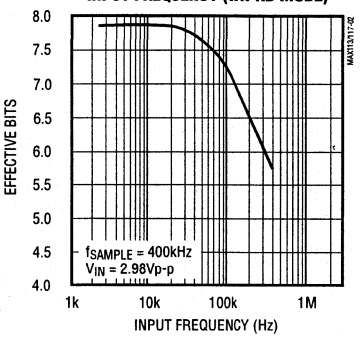
Typical Operating Characteristics

(V_{DD} = +3V, T_A = +25°C, unless otherwise noted.)

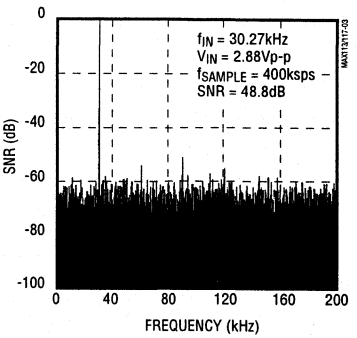
CONVERSION TIME vs. AMBIENT TEMPERATURE



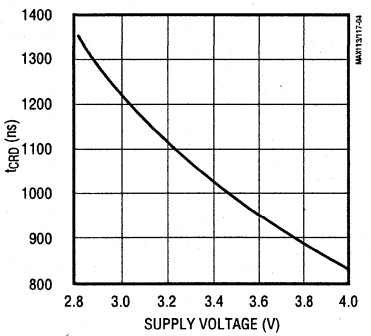
EFFECTIVE BITS vs. INPUT FREQUENCY (WR-RD MODE)



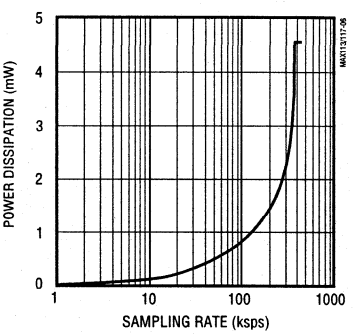
SIGNAL-TO-NOISE RATIO



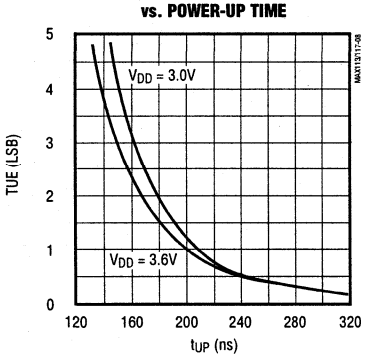
CONVERSION TIME vs. SUPPLY VOLTAGE



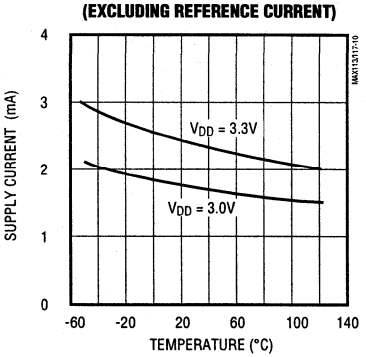
AVERAGE POWER CONSUMPTION vs. SAMPLING RATE USING PWRDN



TOTAL UNADJUSTED ERROR vs. POWER-UP TIME



SUPPLY CURRENT vs. TEMPERATURE (EXCLUDING REFERENCE CURRENT)



7

+3V, 400ksps, 4/8-Channel, 8-Bit ADCs with 1µA Power-Down

Pin Description

PIN		NAME	FUNCTION
MAX113	MAX117		
—	1	IN6	Analog Input Channel 6
—	2	IN5	Analog Input Channel 5
1	3	IN4	Analog Input Channel 4
2	4	IN3	Analog Input Channel 3
3	5	IN2	Analog Input Channel 2
4	6	IN1	Analog Input Channel 1
5	7	MODE	Mode Selection Input. Internally pulled low with a 15µA current source. MODE = 0 activates read mode; MODE = 1 activates write-read mode (see *Digital Interface* section).
6	8	D0	Three-State Data Output (LSB)
7, 8, 9	9, 10, 11	D1, D2, D3	Three-State Data Outputs
10	12	$\overline{RD}$	Read Input. $\overline{RD}$ must be low to access data (see *Digital Interface* section).
11	13	$\overline{INT}$	Interrupt Output. $\overline{INT}$ goes low to indicate end of conversion (see *Digital Interface* section).
12	14	GND	Ground
13	15	REF-	Lower limit of reference span. REF- sets the zero-code voltage. Range is GND ≤ V_{REF-} < V_{REF+}.
14	16	REF+	Upper limit of reference span. REF+ sets the full-scale input voltage. Range is V_{REF-} < V_{REF+} ≤ V_{DD}. Internally hardwired to IN8 (Table 1).
15	17	$\overline{WR}$/RDY	Write-Control Input/Ready-Status Output (see *Digital Interface* section)
16	18	$\overline{CS}$	Chip-Select Input. $\overline{CS}$ must be low for the device to recognize $\overline{WR}$ or $\overline{RD}$ inputs.
17, 18, 19	19, 20, 21	D4, D5, D6	Three-State Data Outputs
20	22	D7	Three-State Data Output (MSB)
—	23	A2	Multiplexer Channel Address Input (MSB)
21	24	A1	Multiplexer Channel Address Input
22	25	A0	Multiplexer Channel Address Input (LSB)
23	26	$\overline{PWRDN}$	Power-Down Input. $\overline{PWRDN}$ reduces supply current when low.
24	27	V_{DD}	Positive Supply, +3.0V to +3.6V
—	28	IN7	Analog Input Channel 7

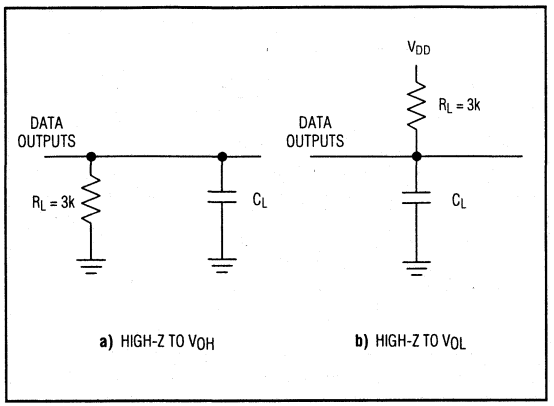


Figure 1. Load Circuits for Data-Access Time Test

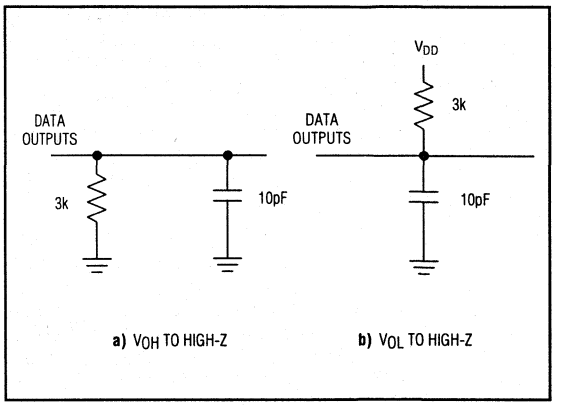


Figure 2. Load Circuits for Data-Hold Time Test

Detailed Description

Converter Operation

The MAX113/MAX117 use a half-flash conversion technique (see *Functional Diagram*) in which two 4-bit flash ADC sections achieve an 8-bit result. Using 15 comparators, the flash ADC compares the unknown input voltage to the reference ladder and provides the upper four data bits. An internal digital-to-analog converter (DAC) uses the four most significant bits (MSBs) to generate both the analog result from the first flash conversion and a residue voltage that is the difference between the unknown input and the DAC voltage. The residue is then compared again with the flash comparators to obtain the lower four data bits (LSBs).

An internal analog multiplexer enables the devices to read four (MAX113) or eight (MAX117) different analog voltages under microprocessor (µP) control. One of the MAX117's analog channels, IN8, is internally hardwired and always reads V_{REF+} when selected.

Power-Down Mode

In burst-mode or low-sample-rate applications, the MAX113/MAX117 can be shut down between conversions, reducing supply current to microamp levels (see *Typical Operating Characteristics*). A logic low on the $\overline{PWRDN}$ pin shuts the devices down, reducing supply current typically to 1µA when powered from a single +3V supply. A logic high on $\overline{PWRDN}$ wakes up the MAX113/MAX117, and the selected analog input enters the track mode. The signal is fully acquired after 900ns (this includes both the power-up delay and the track/hold acquisition time), and a new conversion can be started. If the power-down feature is not required, connect $\overline{PWRDN}$ to V_{DD}. For minimum current consumption, keep digital inputs at the supply rails in power-down mode. Refer to the *Reference* section for information on reducing the reference current during power-down.

Digital Interface

The MAX113/MAX117 have two basic interface modes, which are set by the MODE pin. When MODE is low, the converters are in read mode; when MODE is high, the converters are set up for write-read mode. The A0, A1, and A2 inputs control channel selection, as shown in Table 1. The address must be valid for a minimum time, t_{ACQ}, before the next conversion starts.

Table 1. Truth Table for Input Channel Selection

MAX113		MAX117			SELECTED CHANNEL
A1	A0	A2	A1	A0	
0	0	0	0	0	IN1
0	1	0	0	1	IN2
1	0	0	1	0	IN3
1	1	0	1	1	IN4
—	—	1	0	0	IN5
—	—	1	0	1	IN6
—	—	1	1	0	IN7
—	—	1	1	1	IN8 (reads V_{REF+} if selected)

+3V, 400ksps, 4/8-Channel, 8-Bit ADCs with 1µA Power-Down

Read Mode (MODE = 0)

In read mode, conversions and data access are controlled by the $\overline{RD}$ input (Figure 3). The comparator inputs track the analog input voltage for the duration of t_{ACQ}. A conversion is initiated by driving $\overline{CS}$ and $\overline{RD}$ low. With µPs that can be forced into a wait state, hold $\overline{RD}$ low until output data appears. The µP starts the conversion, waits, and then reads data with a single read instruction.

In read mode, $\overline{WR}$/RDY is configured as a status output (RDY), so it can drive the ready or wait input of a µP. RDY is an open-collector output (no internal pull-up) that goes low after the falling edge of $\overline{CS}$ and goes high at the end of the conversion. If not used, the $\overline{WR}$/RDY pin can be left unconnected. The $\overline{INT}$ output goes low at the end of the conversion and returns high on the rising edge of $\overline{CS}$ or $\overline{RD}$.

Write-Read Mode (MODE = 1)

Figures 4 and 5 show the operating sequence for write-read mode. The comparator inputs track the analog input voltage for the duration of t_{ACQ}. The conversion is initiated by a falling edge of $\overline{WR}$. When $\overline{WR}$ returns high, the result of the four-MSBs flash is latched into the output buffers and the conversion of the four-LSBs flash starts. $\overline{INT}$ goes low, indicating conversion end, and the lower four data bits are latched into the output buffers. The data is then accessible after $\overline{RD}$ goes low (see *Timing Characteristics*).

A minimum acquisition time (t_{ACQ}) is required from $\overline{INT}$ going low to the start of another conversion ($\overline{WR}$ going low).

Options for reading data from the converter include using internal delay, reading before delay, and pipelined operation (discussed in the following sections).

Using Internal Delay

The µP waits for the $\overline{INT}$ output to go low before reading the data (Figure 4). $\overline{INT}$ goes low after the rising edge of $\overline{WR}$, indicating that the conversion is complete and the result is available in the output latch. With $\overline{CS}$ low, data outputs D0–D7 can be accessed by pulling $\overline{RD}$ low. $\overline{INT}$ is then reset by the rising edge of $\overline{CS}$ or $\overline{RD}$.

Fastest Conversion: Reading Before Delay

An external method of controlling the conversion time is shown in Figure 5. The internally generated delay (t_{INTL}) varies slightly with temperature and supply voltage, and can be overridden with $\overline{RD}$ to achieve the fastest conversion time. $\overline{RD}$ is brought low after the rising edge of $\overline{WR}$, but before $\overline{INT}$ goes low. This completes the conversion and enables the output buffers

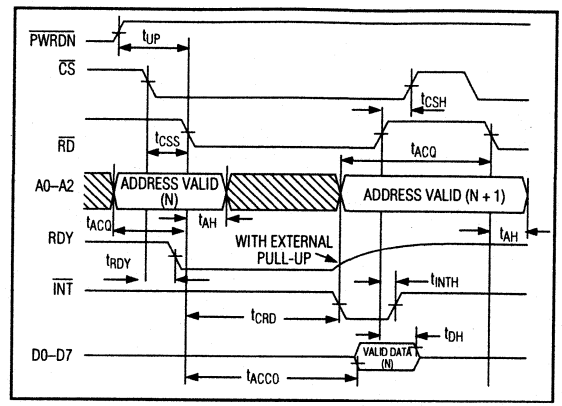


Figure 3. Read Mode Timing (Mode = 0)

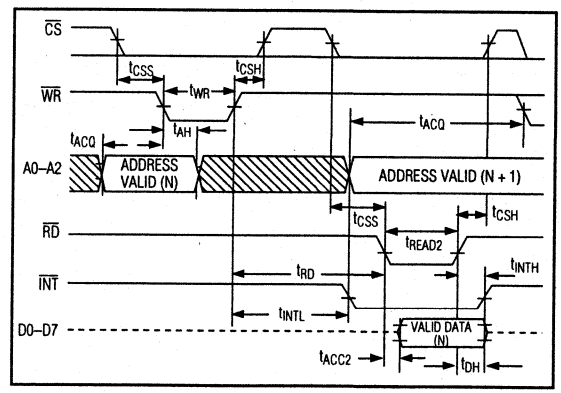


Figure 4. Write-Read Mode Timing ($t_{RD} > t_{INTL}$) (Mode = 1)

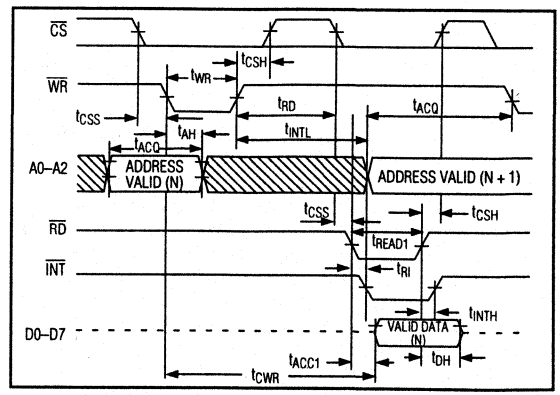


Figure 5. Write-Read Mode Timing ($t_{RD} < t_{INTL}$) (Mode = 1)

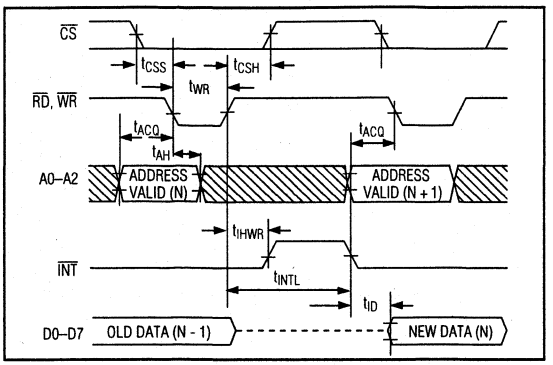


Figure 6. Pipelined Mode Timing (WR = RD) (Mode = 1)

that contain the conversion result (D0–D7). INT also goes low after the falling edge of RD and is reset on the rising edge of RD or CS. The total conversion time is therefore: $t_{WR} + t_{RD} + t_{ACC1} = 1800ns$.

Pipelined Operation

Besides the two standard write-read-mode options, "pipelined" operation can be achieved by connecting WR and RD together (Figure 6). With CS low, driving WR and RD low initiates a conversion and concurrently reads the result of the previous conversion.

Analog Considerations

Reference

Figures 7a, 7b, and 7c show typical reference connections. The voltages at REF+ and REF- set the ADC's analog input range (Figure 10). The voltage at REF- defines the input that produces an output code of all zeros, and the voltage at REF+ defines the input that produces an output code of all ones.

The internal resistance from REF+ to REF- can be as low as 1kΩ, and current will flow through it even when the MAX113/MAX117 are shut down. Figure 7d shows how an N-channel MOSFET can be connected to REF- to break this current path during power-down. The FET should have an on-resistance of less than 2Ω with a 3V gate drive. When REF- is switched, as in Figure 7d, a new conversion can be initiated after waiting a time equal to the power-up delay (t_{UP}) plus the N-channel FET's turn-on time.

Although REF+ is frequently connected to V_{DD}, the circuit of Figure 7d uses a low-current, low-dropout, 2.5V voltage reference: the MAX872. Since the MAX872 cannot continuously furnish enough current for the reference resistance, this circuit is intended for applications where the MAX113/MAX117 are normally in standby and are turned on in order to make measurements at intervals greater than 100µs. C1 (the capacitor connected to REF+) is slowly charged by the MAX872 during the standby period, and furnishes the reference current during the short measurement period.

The 4.7µF value of C1 ensures a voltage drop of less than 1/2LSB when performing four to eight successive conversions. Larger capacitors reduce the error still further. Use ceramic or tantalum capacitors for C1.

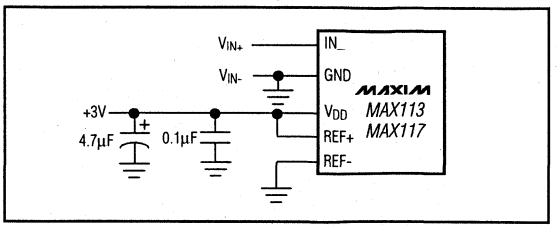


Figure 7a. Power Supply as Reference

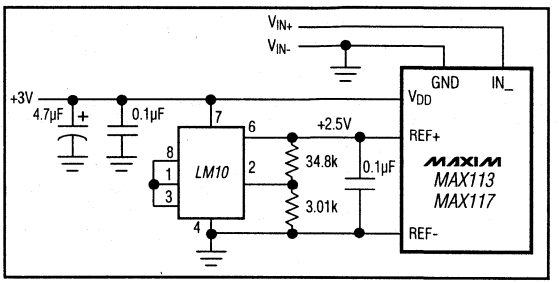


Figure 7b. External Reference, 2.5V Full Scale

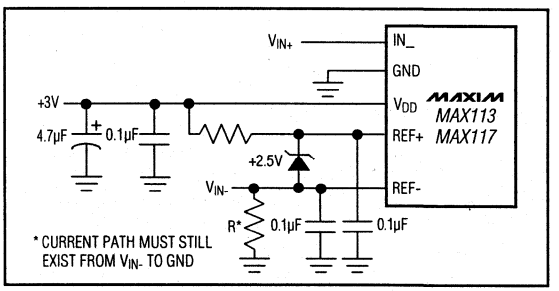


Figure 7c. Input Not Referenced to GND

+3V, 400ksps, 4/8-Channel, 8-Bit ADCs with 1µA Power-Down

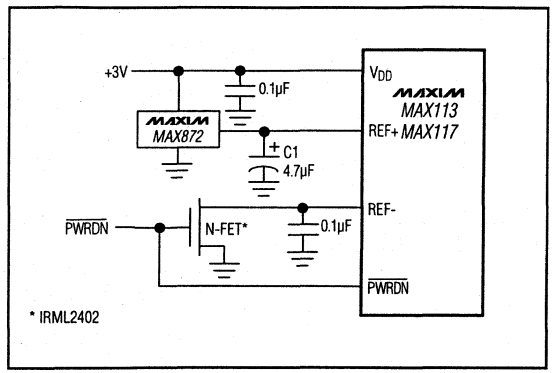


Figure 7d. An N-channel MOSFET switches off the reference load during power-down

Initial Power-Up

When power is first applied, perform a conversion to initialize the MAX113/MAX117. Disregard the output data.

Bypassing

Use a 4.7µF electrolytic in parallel with a 0.1µF ceramic capacitor to bypass V_{DD} to GND. Minimize capacitor lead lengths.

Bypass the reference inputs with 0.1µF capacitors, as shown in Figures 7a, 7b, and 7c.

Analog Inputs

Figure 8 shows the equivalent circuit of the MAX113/MAX117 input. When a conversion starts and $\overline{WR}$ is low, $V_{IN_}$ is connected to sixteen 0.6pF capacitors. During this acquisition phase, the input capacitors charge to the input voltage through the resistance of the internal analog switches. In addition, about 22pF of stray capacitance must be charged. The input can be modeled as an equivalent RC network (Figure 9). As source impedance increases, the capacitors take longer to charge.

The typical 32pF input capacitance allows source resistance as high as 1.5kΩ without setup problems. For larger resistances, the acquisition time (t_{ACQ}) must be increased.

Internal protection diodes, which clamp the analog input to V_{DD} and GND, allow the channel input pins to swing from GND - 0.3V to V_{DD} + 0.3V without damage. However, for accurate conversions near full scale and zero scale the inputs must not exceed V_{DD} by more than 50mV or be lower than GND by 50mV.

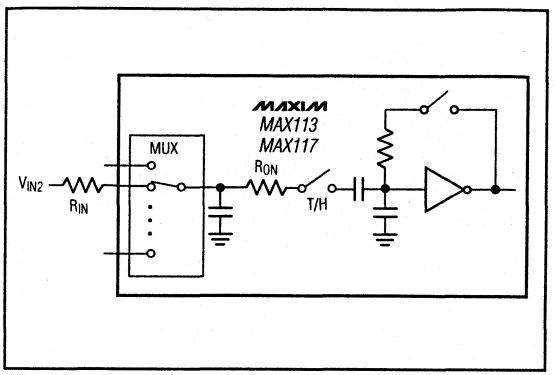


Figure 8. Equivalent Input Circuit

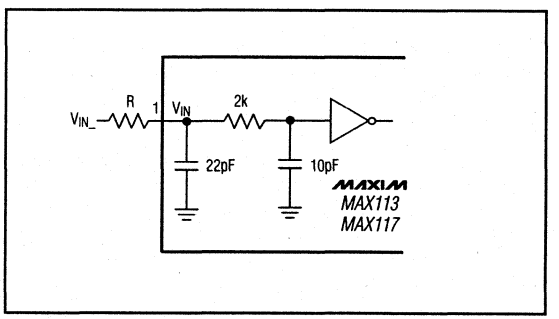


Figure 9. RC Network Equivalent Input Model

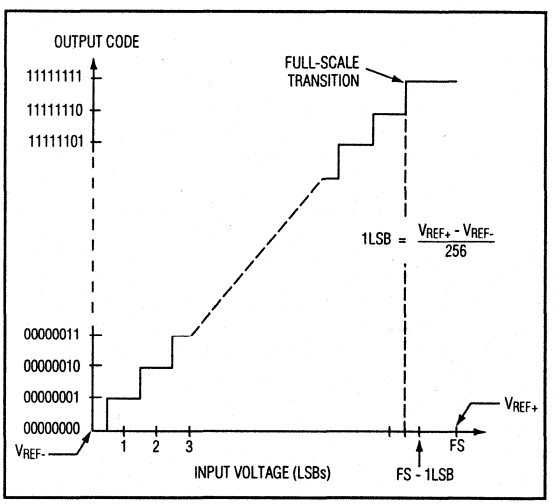


Figure 10. Transfer Function

If the analog input exceeds 50mV beyond the supplies, limit the input current to no more than two milliamperes, as excessive current will degrade the conversion accuracy of the on channel.

Track/Hold

The track/hold enters hold mode when a conversion starts ($\overline{RD}$ low or $\overline{WR}$ low). INT goes low at the end of the conversion, at which point the track/hold enters track mode. The next conversion can start after the minimum acquisition time, t_{ACQ}.

Transfer Function

Figure 10 shows the MAX113/MAX117's nominal transfer function. Code transitions occur halfway between successive-integer LSB values. Output coding is binary with 1LSB = (V_{REF+} - V_{REF-}) / 256.

Conversion Rate

The maximum sampling rate (f_{MAX}) for the MAX113/MAX117 is achieved in write-read mode (t_{RD} < t_{INTL}) and is calculated as follows:

$$f_{MAX} = \frac{1}{t_{WR} + t_{RD} + t_{RI} + t_{ACQ}}$$

$$f_{MAX} = \frac{1}{600ns + 800ns + 300ns + 450ns}$$

$$f_{MAX} = 465kHz$$

where t_{WR} = the write pulse width, t_{RD} = the delay between write and read pulses, t_{RI} = $\overline{RD}$ to $\overline{INT}$ delay, and t_{ACQ} = minimum acquisition time.

Signal-to-Noise Ratio and Effective Number of Bits

Signal-to-noise plus distortion (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to all other ADC output signals. The output spectrum is limited to frequencies above DC and below one-half the ADC sample rate.

The theoretical minimum analog-to-digital noise is caused by quantization error, and results directly from the ADC's resolution: SNR = (6.02N + 1.76)dB, where N is the number of bits of resolution. Therefore, a perfect 8-bit ADC can do no better than 50dB.

The FFT Plot (see *Typical Operating Characteristics*) shows the result of sampling a pure 30.27kHz sinusoid at a 400kHz rate. This FFT plot of the output shows the output level in various spectral bands.

The effective resolution (or "effective number of bits") the ADC provides can be measured by transposing the equation that converts resolution to SNR: N = (SINAD - 1.76) / 6.02 (see *Typical Operating Characteristics*).

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal (in the frequency band above DC and below one-half the sample rate) to the fundamental itself. This is expressed as:

$$THD = 20\log\left[\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + ...V_N^2}}{V_1}\right]$$

where V_1 is the fundamental RMS amplitude, and V_2 through V_N are the amplitudes of the 2nd through Nth harmonics.

Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is the ratio of the fundamental RMS amplitude to the amplitude of the next largest spectral component (in the frequency band above DC and below one-half the sample rate). Usually the next largest spectral component occurs at some harmonic of the input frequency. However, if the ADC is exceptionally linear, it may occur only at a random peak in the ADC's noise floor. See the Signal-to-Noise Ratio graph in *Typical Operating Characteristics*.

+3V, 400ksps, 4/8-Channel, 8-Bit ADCs with 1µA Power-Down

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX117CPI	0°C to +70°C	28 Wide Plastic DIP
MAX117CAI	0°C to +70°C	28 SSOP
MAX117C/D	0°C to +70°C	Dice*
MAX117EPI	-40°C to +85°C	28 Wide Plastic DIP
MAX117EAI	-40°C to +85°C	28 SSOP
MAX117MJI	-55°C to +125°C	28 Wide CERDIP**

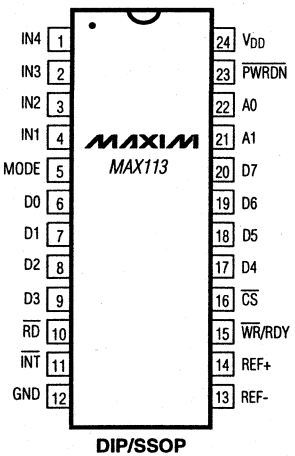
*Dice are specified at T_A = +25°C, DC parameters only.
**Contact factory for availability.

Chip Information

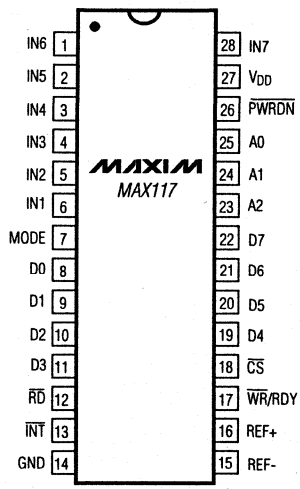
TRANSISTOR COUNT: 2011

Pin Configurations

TOP VIEW



DIP/SSOP



DIP/SSOP

19-1083; Rev 1; 8/96

MAXIM

+5V, 1Msps, 4 & 8-Channel, 8-Bit ADCs with 1µA Power-Down

General Description

The MAX114/MAX118 are microprocessor-compatible, 8-bit, 4-channel and 8-channel analog-to-digital converters (ADCs). They operate from a single +5V supply and use a half-flash technique to achieve a 660ns conversion time (1Msps). A power-down ($\overline{PWRDN}$) pin reduces current consumption typically to 1µA. The devices return from power-down mode to normal operating mode in less than 200ns, allowing large supply-current reductions in burst-mode applications (in burst mode, the ADC wakes up from a low-power state at specified intervals to sample the analog input signals). Both converters include a track/hold, enabling the ADC to digitize fast analog signals.

Microprocessor (µP) interfaces are simplified because the ADC can appear as a memory location or I/O port without external interface logic. The data outputs use latched, three-state buffer circuitry for direct connection to an 8-bit parallel µP data bus or system input port. The MAX114/MAX118 input/reference configuration enables ratiometric operation.

The 4-channel MAX114 is available in a 24-pin DIP or SSOP. The 8-channel MAX118 is available in a 28-pin DIP or SSOP. For +3V applications, refer to the MAX113/MAX117 data sheet.

Applications

High-Speed DSP
Portable Equipment
Remote Data Acquisition
Communications Systems

Features

- ♦ **Single +5V Supply Operation**
- ♦ **4 (MAX114) or 8 (MAX118) Analog Input Channels**
- ♦ **Low Power: 40mW (operating mode)**
  5µW (power-down mode)
- ♦ **Total Unadjusted Error ≤1LSB**
- ♦ **Fast Conversion Time: 660ns per Channel**
- ♦ **No External Clock Required**
- ♦ **Internal Track/Hold**
- ♦ **1MHz Full-Power Bandwidth**
- ♦ **Internally Connected 8th Channel Monitors Reference Voltage (MAX118)**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX114CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX114CAG	0°C to +70°C	24 SSOP
MAX114C/D	0°C to +70°C	Dice*
MAX114ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX114EAG	-40°C to +85°C	24 SSOP
MAX114MRG	-55°C to +125°C	24 Narrow CERDIP**

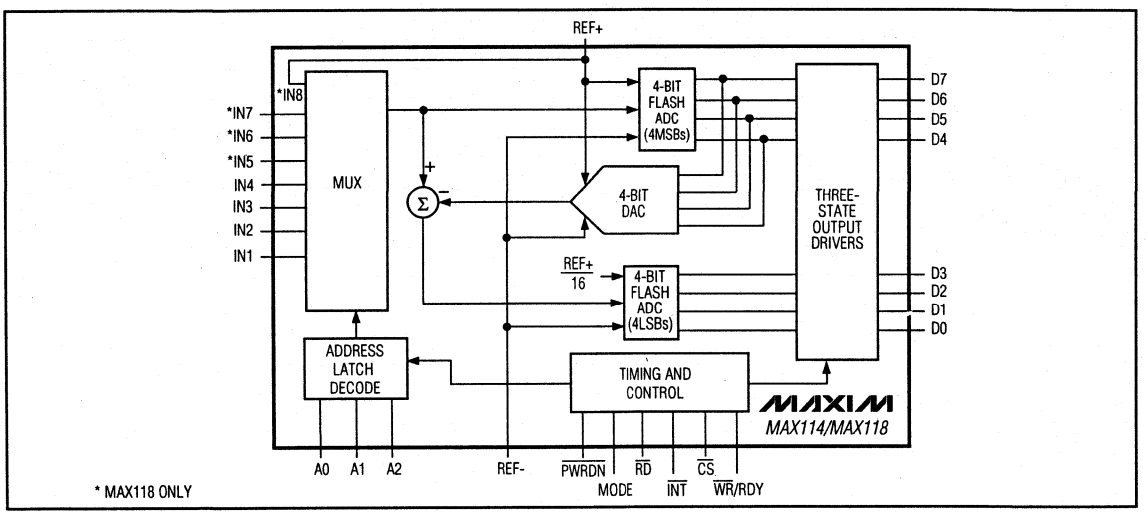
Ordering Information continued on last page.

**Dice are specified at T_A = +25°C, DC parameters only.*

***Contact factory for availability.*

Pin Configurations appear on last page.

Functional Diagram



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+5V, 1Msps, 4 & 8-Channel, 8-Bit ADCs with 1µA Power-Down

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +7V
Digital Input Voltage to GND .....-0.3V to (V_{DD} + 0.3V)
Digital Output Voltage to GND .....-0.3V to (V_{DD} + 0.3V)
REF+ to GND .....-0.3V to (V_{DD} + 0.3V)
REF- to GND .....-0.3V to (V_{DD} + 0.3V)
IN_ to GND .....-0.3V to (V_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
24-Pin Narrow Plastic DIP
(derate 13.33mW/°C above +70°C) 1.08W
24-Pin SSOP (derate 8.00mW/°C above +70°C) 640mW
24-Pin Narrow CERDIP
(derate 12.50mW/°C above +70°C) 1W
28-Pin Wide Plastic DIP
(derate 14.29mW/°C above +70°C) 1.14W
28-Pin SSOP (derate 9.52mW/°C above +70°C) 762mW
28-Pin Wide CERDIP
(derate 16.67mW/°C above +70°C) 1.33W
Operating Temperature Ranges
MAX114/MAX118C_ _ .....0°C to +70°C
MAX114/MAX118E_ _ .....-40°C to +85°C
MAX114/MAX118M_ _ .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±5%, REF+ = 5V, REF- = GND, Read Mode (MODE = GND), T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY (Note 1)						
Resolution	N		8			Bits
Total Unadjusted Error	TUE				±1	LSB
Differential Nonlinearity	DNL	No-missing-codes guaranteed			±1	LSB
Zero-Code Error					±1	LSB
Full-Scale Error					±1	LSB
Channel-to-Channel Mismatch					±1/4	LSB
DYNAMIC PERFORMANCE						
Signal-to-Noise Plus Distortion Ratio	SINAD	MAX11_C/E, f_{SAMPLE} = 1MHz, $f_{IN_}$ = 195.8kHz	45			dB
		MAX11_M, f_{SAMPLE} = 740kHz, $f_{IN_}$ = 195.7kHz	45			
Total Harmonic Distortion	THD	MAX11_C/E, f_{SAMPLE} = 1MHz, $f_{IN_}$ = 195.8kHz			-50	dB
		MAX11_M, f_{SAMPLE} = 740kHz, $f_{IN_}$ = 195.7kHz			-50	
Spurious-Free Dynamic Range	SFDR	MAX11_C/E, f_{SAMPLE} = 1MHz, $f_{IN_}$ = 195.8kHz	50			dB
		MAX11_M, f_{SAMPLE} = 740kHz, $f_{IN_}$ = 195.7kHz	50			
Input Full-Power Bandwidth		$V_{IN_}$ = 5Vp-p		1		MHz
Input Slew Rate, Tracking			3.1	15		V/µs
ANALOG INPUT						
Input Voltage Range	$V_{IN_}$		V_{REF-}		V_{REF+}	V
Input Leakage Current	$I_{IN_}$	GND < $V_{IN_}$ < V_{DD}			±3	µA
Input Capacitance	$C_{IN_}$			32		pF
REFERENCE INPUT						
Reference Resistance	R_{REF}		1	2	4	kΩ
REF+ Input Voltage Range			V_{REF-}		V_{DD}	V
REF- Input Voltage Range			GND		V_{REF+}	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±5%, REF+ = 5V, REF- = GND, Read Mode (MODE = GND), T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LOGIC INPUTS							
Input High Voltage	V_{INH}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{PWRDN}$, A0, A1, A2		2.4			V
		MODE		3.5			
Input Low Voltage	V_{INL}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{PWRDN}$, A0, A1, A2				0.8	V
		MODE				1.5	
Input High Current	I_{INH}	$\overline{CS}$, $\overline{RD}$, $\overline{PWRDN}$, A0, A1, A2				±1	µA
		$\overline{WR}$				±3	
		MODE			50	200	
Input Low Current	I_{INL}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{PWRDN}$, MODE, A0, A1, A2				±1	µA
Input Capacitance (Note 2)	C_{IN}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{PWRDN}$, MODE, A0, A1, A2			5	8	pF
LOGIC OUTPUTS							
Output Low Voltage	V_{OL}	I_{SINK} = 1.6mA, $\overline{INT}$, D0–D7				0.4	V
		RDY, I_{SINK} = 2.6mA				0.4	
Output High Voltage	V_{OH}	I_{SOURCE} = 360µA, $\overline{INT}$, D0–D7		4			V
Three-State Current	I_{LKG}	D0–D7, RDY, digital outputs = 0V to V_{DD}				±3	µA
Three-State Capacitance (Note 2)	C_{OUT}	D0–D7, RDY			5	8	pF
POWER REQUIREMENTS							
Supply Voltage	V_{DD}			4.75		5.25	V
V_{DD} Supply Current	I_{DD}	$\overline{CS}$ = $\overline{RD}$ = 0V, $\overline{PWRDN}$ = V_{DD}	MAX11_C		8	15	mA
			MAX11_E/M		8	20	
Power-Down V_{DD} Current		$\overline{CS}$ = $\overline{RD}$ = V_{DD}, $\overline{PWRDN}$ = 0V (Note 3)			1	10	µA
Power-Supply Rejection	PSR	V_{DD} = 4.75V to 5.25V, V_{REF} = 4.75V			±1/16	±1/4	LSB

Note 2: Guaranteed by design.
Note 3: Power-down current increases if logic inputs are not driven to GND or V_{DD}.

+5V, 1Msps, 4 & 8-Channel, 8-Bit ADCs with 1µA Power-Down

TIMING CHARACTERISTICS

(V_{DD} = +4.75V, T_A = +25°C, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C ALL GRADES			T_A = T_{MIN} to T_{MAX}				UNITS
						MAX11_C/E		MAX11_M		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Conversion Time (WR-RD Mode)	t_{CWR}	t_{RD} < t_{INTL}, (Note 5) C_L = 20pF			660					ns
		t_{RD} < t_{INTL}, (Note 5) C_L = 100pF			685		865		1125	
Conversion Time (RD Mode)	t_{CRD}				700		875		975	ns
Power-Up Time	t_{UP}				320		370		520	ns
$\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Setup Time	t_{CSS}		0			0		0		ns
$\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Hold Time	t_{CSH}		0			0		0		ns
$\overline{CS}$ to RDY Delay	t_{RDY}	C_L = 50pF, R_L = 5.1kΩ to V_{DD}			70		85		100	ns
Data-Access Time (RD Mode)	t_{ACC0}	C_L = 100pF (Note 5)			t_{CRD} + 50		t_{CRD} + 65		t_{CRD} + 75	ns
$\overline{RD}$ to $\overline{INT}$ Delay (RD Mode)	t_{INTH}	C_L = 50pF		50	80		85		90	ns
Data Hold Time	t_{DH}	(Note 6)			60		70		80	ns
Minimum Acquisition Time	t_{ACQ}	(Note 7)	160			185		260		ns
$\overline{WR}$ Pulse Width	t_{WR}		0.25		10	0.28	10	0.4	10	µs
Delay Between $\overline{WR}$ and $\overline{RD}$ Pulses	t_{RD}		0.25			0.35		0.45		µs
$\overline{RD}$ Pulse Width (WR-RD Mode)	t_{READ1}	t_{RD} < t_{INTL}, determined by t_{ACC1}	160			205		240		ns
Data-Access Time (WR-RD Mode)	t_{ACC1}	t_{RD} < t_{INTL}, C_L = 100pF (Note 5)			185		235		275	ns
$\overline{RD}$ to $\overline{INT}$ Delay	t_{RI}				150		185		220	ns
$\overline{WR}$ to $\overline{INT}$ Delay	t_{INTL}	C_L = 50pF		380	500		610		700	ns
$\overline{RD}$ Pulse Width (WR-RD Mode)	t_{READ2}	t_{RD} > t_{INTL}, determined by t_{ACC2}	65			75		85		ns
Data-Access Time (WR-RD Mode)	t_{ACC2}	t_{RD} > t_{INTL}, C_L = 100pF (Note 5)			90		110		130	ns
$\overline{WR}$ to $\overline{INT}$ Delay	t_{IHWR}	Pipelined mode, C_L = 50pF			80		100		120	ns
Data-Access Time after $\overline{INT}$	t_{ID}	Pipelined mode, C_L = 100pF			45		60		70	ns
Multiplexer Address Hold Time	t_{AH}		30			35		40		ns

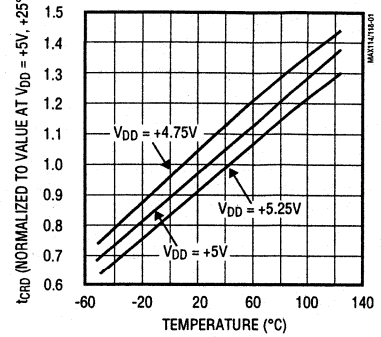
Note 4: Input control signals are specified with t_r = t_f = 5ns, 10% to 90% of 5V, and timed from a voltage level of 1.6V.
Note 5: See Figure 1 for load circuit. Parameter defined as the time required for the output to cross 0.8V or 2.4V.
Note 6: See Figure 2 for load circuit. Parameter defined as the time required for the data lines to change 0.5V.
Note 7: Also defined as the Minimum Address-Valid to Convert-Start Time.

+5V, 1Msps, 4 & 8-Channel, 8-Bit ADCs with 1µA Power-Down

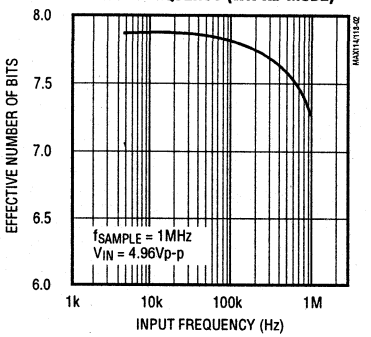
Typical Operating Characteristics

(V_{DD} = +5V, T_A = +25°C, unless otherwise noted.)

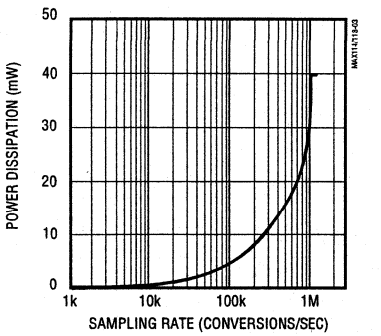
CONVERSION TIME vs. AMBIENT TEMPERATURE



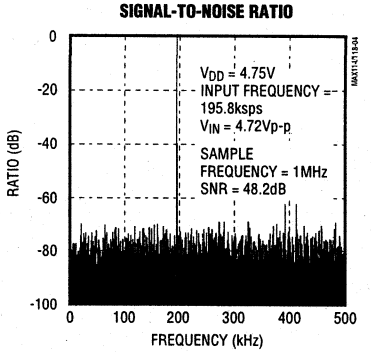
EFFECTIVE NUMBER OF BITS vs. INPUT FREQUENCY (WR-RD MODE)



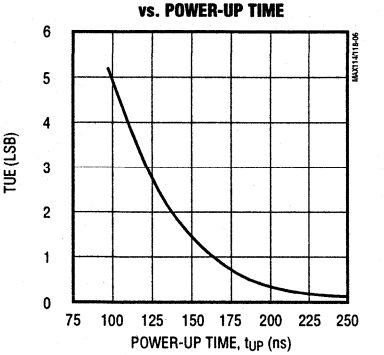
AVERAGE POWER CONSUMPTION vs. SAMPLING RATE USING $\overline{PWRDN}$



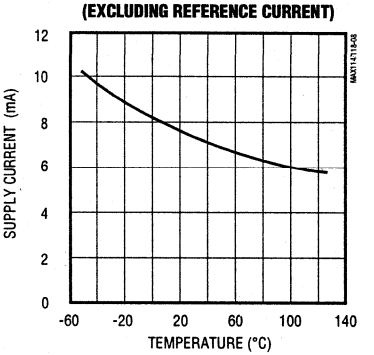
SIGNAL-TO-NOISE RATIO



TOTAL UNADJUSTED ERROR vs. POWER-UP TIME



SUPPLY CURRENT vs. TEMPERATURE (EXCLUDING REFERENCE CURRENT)



7

+5V, 1Msps, 4 & 8-Channel, 8-Bit ADCs with 1µA Power-Down

Pin Description

PIN		NAME	FUNCTION
MAX114	MAX118		
—	1	IN6	Analog Input Channel 6
—	2	IN5	Analog Input Channel 5
1	3	IN4	Analog Input Channel 4
2	4	IN3	Analog Input Channel 3
3	5	IN2	Analog Input Channel 2
4	6	IN1	Analog Input Channel 1
5	7	MODE	Mode Selection Input. Internally pulled low with a 50µA current source. MODE = 0 activates read mode; MODE = 1 activates write-read mode (see *Digital Interface* Section).
6	8	D0	Three-State Data Output (LSB)
7, 8, 9	9, 10, 11	D1, D2, D3	Three-State Data Outputs
10	12	$\overline{RD}$	Read Input. $\overline{RD}$ must be low to access data (see *Digital Interface* section).
11	13	$\overline{INT}$	Interrupt Output. $\overline{INT}$ goes low to indicate end of conversion (see *Digital Interface* section).
12	14	GND	Ground
13	15	REF-	Lower Limit of Reference Span. REF- sets the zero-code voltage. Range is GND ≤ V_{REF-} < V_{REF+}.
14	16	REF+	Upper Limit of Reference Span. REF+ sets the full-scale input voltage. Range is V_{REF-} < V_{REF+} ≤ V_{DD}. Internally hard-wired to IN8 (Table 1).
15	17	$\overline{WR}$/RDY	Write-Control Input/Ready-Status Output (see *Digital Interface* section)
16	18	$\overline{CS}$	Chip-Select Input. $\overline{CS}$ must be low for the device to recognize $\overline{WR}$ or $\overline{RD}$ inputs.
17, 18, 19	19, 20, 21	D4, D5, D6	Three-State Data Outputs
20	22	D7	Three-State Data Output (MSB)
—	23	A2	Multiplexer Channel Address Input (MSB)
21	24	A1	Multiplexer Channel Address Input
22	25	A0	Multiplexer Channel Address Input (LSB)
23	26	$\overline{PWRDN}$	Power-Down Input. $\overline{PWRDN}$ reduces supply current when low.
24	27	V_{DD}	Positive Supply, +5V
—	28	IN7	Analog Input Channel 7

Detailed Description

Converter Operation

The MAX114/MAX118 use a half-flash conversion technique (see *Functional Diagram*) in which two 4-bit flash ADC sections achieve an 8-bit result. Using 15 comparators, the flash ADC compares the unknown input voltage to the reference ladder and provides the upper four data bits. An internal digital-to-analog converter (DAC) uses the four most significant bits (MSBs) to generate both the analog result from the first flash conversion and a residue voltage that is the difference between the unknown input and the DAC voltage. The residue is then compared again with the flash comparators to obtain the lower four data bits (LSBs).

An internal analog multiplexer enables the devices to read four (MAX114) or eight (MAX118) different analog voltages under microprocessor (µP) control. One of the MAX118's analog channels, IN8, is internally hardwired and always reads V_{REF+} when selected.

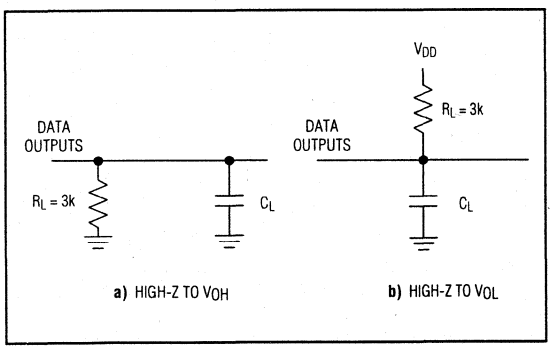


Figure 1. Load Circuits for Data-Access Time Test

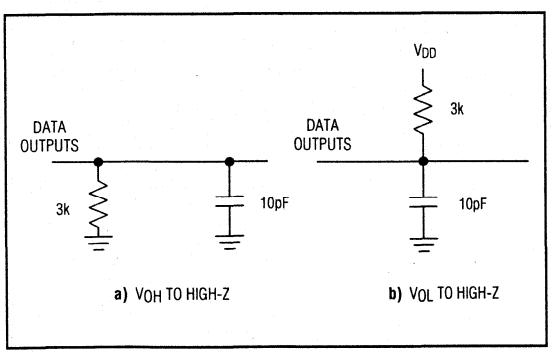


Figure 2. Load Circuits for Data-Hold Time Test

Power-Down Mode

In burst-mode or low sample-rate applications, the MAX114/MAX118 can be shut down between conversions, reducing supply current to microamp levels (see *Typical Operating Characteristics*). A logic low on the $\overline{PWRDN}$ pin shuts the devices down, reducing supply current typically to 1µA when powered from a single +5V supply. A logic high on $\overline{PWRDN}$ wakes up the MAX114/MAX118, and the selected analog input enters the track mode. The signal is fully acquired after 360ns (this includes both the power-up delay and the track/hold acquisition time), and a new conversion can be started. If the power-down feature is not required, connect $\overline{PWRDN}$ to V_{DD}. For minimum current consumption, keep digital inputs at the supply rails in power-down mode. Refer to the *Reference* section for information on reducing reference current during power-down.

Digital Interface

The MAX114/MAX118 have two basic interface modes, which are set by the MODE pin. When MODE is low, the converters are in read mode; when MODE is high, the converters are set up for write-read mode. The A0, A1, and A2 inputs control channel selection, as shown in Table 1. The address must be valid for a minimum time, t_{ACQ}, before the next conversion starts.

Table 1. Truth Table for Input Channel Selection

MAX114		MAX118			SELECTED CHANNEL
A1	A0	A2	A1	A0	
0	0	0	0	0	IN1
0	1	0	0	1	IN2
1	0	0	1	0	IN3
1	1	0	1	1	IN4
—	—	1	0	0	IN5
—	—	1	0	1	IN6
—	—	1	1	0	IN7
—	—	1	1	1	IN8 (reads V_{REF+} if selected)

Read Mode (MODE = 0)

In read mode, conversions and data access are controlled by the $\overline{RD}$ input (Figure 3). The comparator inputs track the analog input voltage for the duration of t_{ACQ}. Initiate a conversion by driving $\overline{CS}$ and $\overline{RD}$ low. With µPs that can be forced into a wait state, hold $\overline{RD}$ low until output data appears. The µP starts the conversion, waits, and then reads data with a single read instruction.

+5V, 1Msps, 4 & 8-Channel, 8-Bit ADCs with 1µA Power-Down

In read mode, $\overline{WR}$/RDY is configured as a status output (RDY), so it can drive the ready or wait input of a µP. RDY is an open-collector output (no internal pull-up) that goes low after the falling edge of $\overline{CS}$ and goes high at the end of the conversion. If not used, the $\overline{WR}$/RDY pin can be left unconnected. The $\overline{INT}$ output goes low at the end of the conversion and returns high on the rising edge of $\overline{CS}$ or $\overline{RD}$.

Write-Read Mode (MODE = 1)

Figures 4 and 5 show the operating sequence for write-read mode. The comparator inputs track the analog input voltage for the duration of t_{ACQ}. The conversion is initiated by a falling edge of $\overline{WR}$. When $\overline{WR}$ returns high, the result of the four-MSBs flash is latched into the output buffers and the conversion of the four-LSBs flash starts. $\overline{INT}$ goes low, indicating conversion end, and the lower four data bits are latched into the output buffers. The data is then accessible after $\overline{RD}$ goes low (see *Timing Characteristics*).

A minimum acquisition time (t_{ACQ}) is required from $\overline{INT}$ going low to the start of another conversion ($\overline{WR}$ going low).

Options for reading data from the converter include using internal delay, reading before delay, and pipelined operation (discussed in the following sections).

Using Internal Delay

The µP waits for the $\overline{INT}$ output to go low before reading the data (Figure 4). $\overline{INT}$ goes low after the rising edge of $\overline{WR}$, indicating that the conversion is complete and the result is available in the output latch. With $\overline{CS}$ low, data outputs D0–D7 can be accessed by pulling $\overline{RD}$ low. $\overline{INT}$ is then reset by the rising edge of $\overline{CS}$ or $\overline{RD}$.

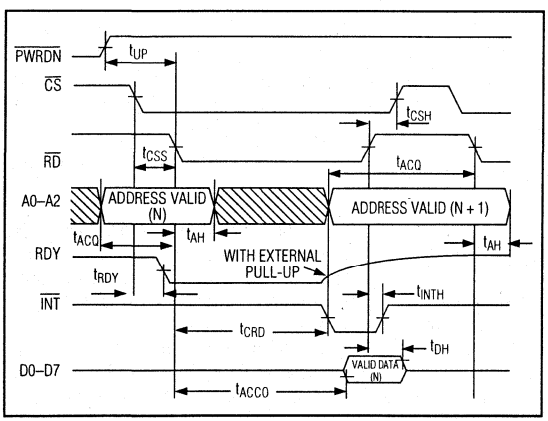


Figure 3. Read Mode Timing (MODE = 0)

Fastest Conversion: Reading Before Delay

Figure 5 shows an external method of controlling the conversion time. The internally generated delay (t_{INTL}) varies slightly with temperature and supply voltage, and can be overridden with $\overline{RD}$ to achieve the fastest conversion time. $\overline{RD}$ is brought low after the rising edge of $\overline{WR}$, but before $\overline{INT}$ goes low. This completes the conversion and enables the output buffers that contain the conversion result (D0–D7). $\overline{INT}$ also goes low after the falling edge of $\overline{RD}$ and is reset on the rising edge of $\overline{RD}$ or $\overline{CS}$. The total conversion time is therefore: $t_{WR} + t_{RD} + t_{ACC1} = 660ns$.

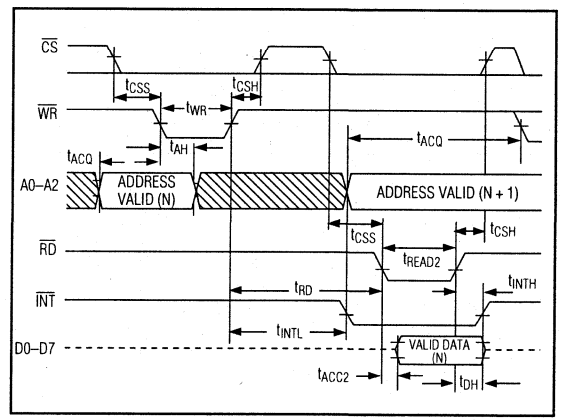


Figure 4. Write-Read Mode Timing ($t_{RD} > t_{INTL}$) (MODE = 1)

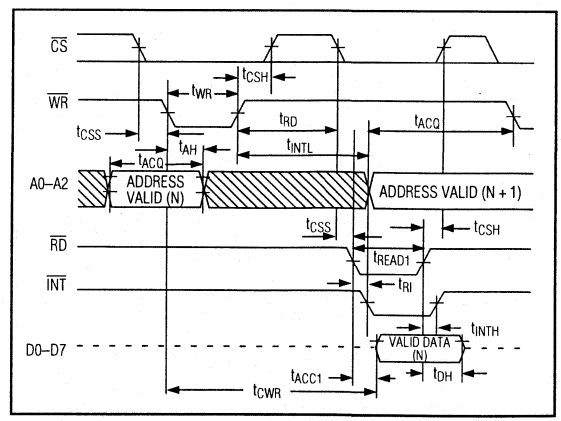


Figure 5. Write-Read Mode Timing ($t_{RD} < t_{INTL}$) (MODE = 1)

Pipelined Operation

Besides the two standard write-read-mode options, pipelined operation can be achieved by connecting $\overline{WR}$ to $\overline{RD}$ (Figure 6). With $\overline{CS}$ low, driving $\overline{WR}$ and $\overline{RD}$ low initiates a conversion and concurrently reads the result of the previous conversion.

Analog Considerations

Reference

Figures 7a, 7b, and 7c show typical reference connections. The voltages at REF+ and REF- set the ADC's analog input range (see Figure 10). The voltage at REF- defines the input that produces an output code of all zeros, and the voltage at REF+ defines the input that produces an output code of all ones.

The internal resistance from REF+ to REF- can be as low as 1kΩ, and current will flow through it even when the MAX114/MAX118 are shut down. Figure 7d shows how an N-channel MOSFET can be connected to REF-

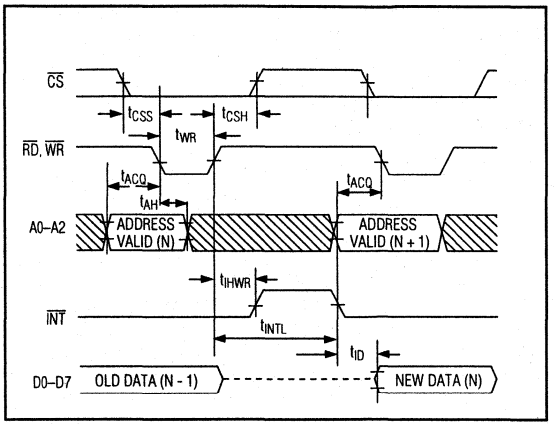


Figure 6. Pipelined Mode Timing ($\overline{WR}$ = $\overline{RD}$) (MODE = 1)

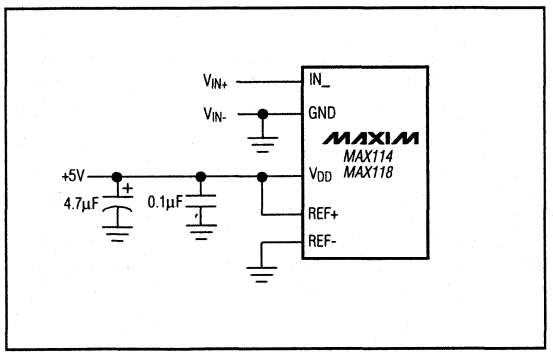


Figure 7a. Power Supply as Reference

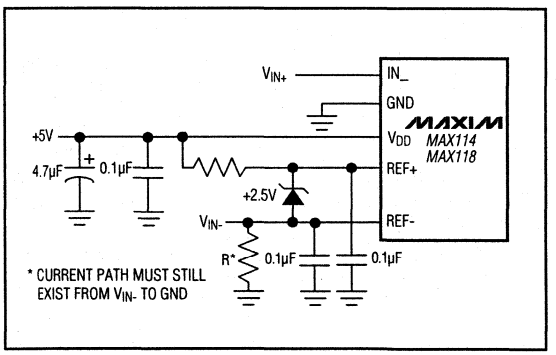


Figure 7c. Input Not Referenced to GND

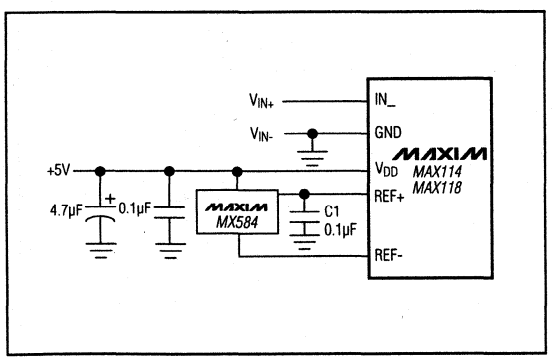


Figure 7b. External Reference, 4.096V Full Scale

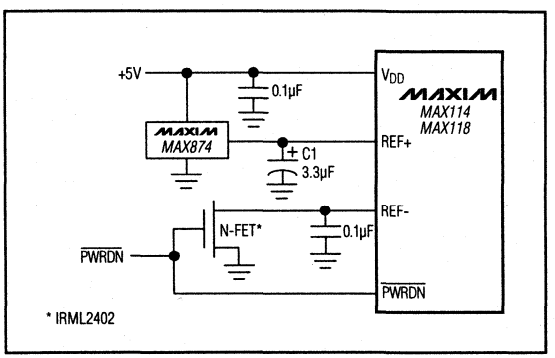


Figure 7d. An N-channel MOSFET switches off the reference load during power-down

+5V, 1Msps, 4 & 8-Channel, 8-Bit ADCs with 1µA Power-Down

to break this current path during power-down. The FET should have an on-resistance of less than 2Ω with a 5V gate drive. When REF- is switched, as in Figure 7d, a new conversion can be initiated after waiting a period of time equal to the power-up delay (t_{UP}) plus the N-channel FET's turn-on time.

Although REF+ is frequently connected to V_{DD}, the circuit of Figure 7d uses a low-current, low-dropout, 4.096V voltage reference: the MAX874. Since the MAX874 cannot continuously furnish enough current for the reference resistance, this circuit is intended for applications where the MAX114/MAX118 are normally in standby and are turned on in order to make measurements at intervals greater than 65µs. C1 (the capacitor connected to REF+) is slowly charged by the MAX874 during the standby period, and furnishes the reference current during the short measurement period.

C1's 3.3µF value ensures a voltage drop of less than 1/2LSB when performing four to eight successive conversions. Larger capacitors reduce the error still further. Use ceramic or tantalum capacitors for C1.

Initial Power-Up

When power is first applied, perform a conversion to initialize the MAX114/MAX118. Disregard the output data.

Bypassing

Use a 4.7µF electrolytic in parallel with a 0.1µF ceramic capacitor to bypass V_{DD} to GND. Minimize capacitor lead lengths.

Bypass the reference inputs with 0.1µF capacitors, as shown in Figures 7a, 7b, and 7c.

Analog Inputs

Figure 8 shows the equivalent circuit of the MAX114/MAX118 input. When a conversion starts and $\overline{WR}$ is low, $V_{IN_}$ is connected to sixteen 0.6pF capacitors. During this acquisition phase, the input capacitors charge to the input voltage through the resistance of the internal analog switches. In addition, about 22pF of stray capacitance must be charged. The input can be modeled as an equivalent RC network (Figure 9). As source impedance increases, the capacitors take longer to charge.

The typical 32pF input capacitance allows source resistance as high as 800Ω without setup problems. For larger resistances, the acquisition time (t_{ACQ}) must be increased.

Internal protection diodes, which clamp the analog input to V_{DD} and GND, allow the channel input pins to swing from GND - 0.3V to V_{DD} + 0.3V without damage. However, for accurate conversions near full scale, the inputs must not exceed V_{DD} by more than 50mV or be lower than GND by 50mV.

If the analog input exceeds 50mV beyond the supplies, limit the input current to no more than 2mA, as excessive current will degrade the conversion accuracy of the on channel.

Track/Hold

The track/hold enters hold mode when a conversion starts ($\overline{RD}$ low or $\overline{WR}$ low). INT goes low at the end of the conversion, at which point the track/hold enters track mode. The next conversion can start after the minimum acquisition time, t_{ACQ}.

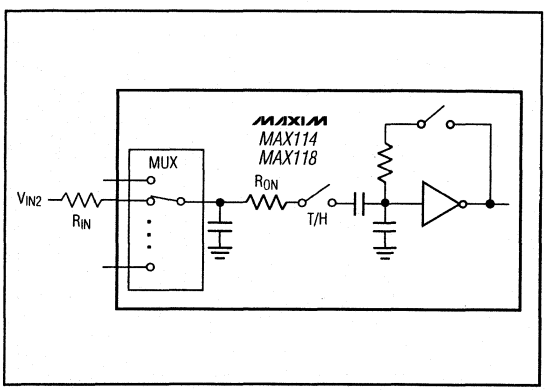


Figure 8. Equivalent Input Circuit

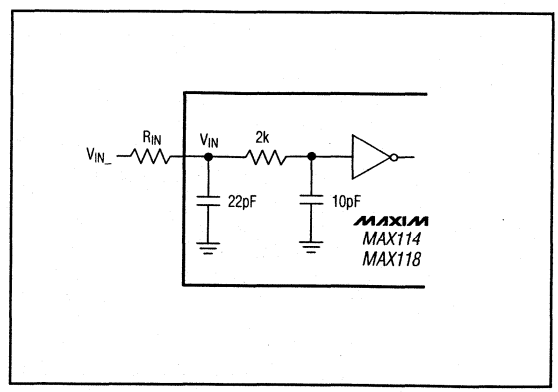


Figure 9. RC Network Equivalent Input Model

Transfer Function

Figure 10 shows the MAX114/MAX118's nominal transfer function. Code transitions occur halfway between successive-integer LSB values. Output coding is binary with 1LSB = (V_{REF+} - V_{REF-}) / 256.

Conversion Rate

The maximum sampling rate (f_{MAX}) for the MAX114/MAX118 is achieved in write-read mode (t_{RD} < t_{INTL}), and is calculated as follows:

$$f_{MAX} = \frac{1}{t_{WR} + t_{RD} + t_{RI} + t_{ACQ}}$$

$$f_{MAX} = \frac{1}{250ns + 250ns + 150ns + 160ns}$$

$$f_{MAX} = 1.23MHz$$

where t_{WR} = the write pulse width, t_{RD} = the delay between write and read pulses, t_{RI} = $\overline{RD}$ to $\overline{INT}$ delay, and t_{ACQ} = minimum acquisition time.

Signal-to-Noise Ratio and Effective Number of Bits

Signal-to-noise plus distortion (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to all other ADC output signals. The output spectrum is limited to frequencies above DC and below one-half the ADC sample rate.

The theoretical minimum analog-to-digital noise is caused by quantization error, and results directly from the ADC's resolution: SNR = (6.02N + 1.76)dB, where N is the number of bits of resolution. Therefore, a perfect 8-bit ADC can do no better than 50dB.

The FFT Plot (see *Typical Operating Characteristics*) shows the result of sampling a pure 195.8kHz sinusoid at a 1MHz rate. This FFT plot of the output shows the output level in various spectral bands.

The effective resolution (or "effective number of bits") the ADC provides can be measured by transposing the equation that converts resolution to SNR: N = (SINAD - 1.76) / 6.02 (see *Typical Operating Characteristics*).

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal (in the frequency band above DC and below one-half the sample rate) to the fundamental itself. This is expressed as:

$$THD = 20\log\left[\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \ldots V_N^2}}{V_1}\right]$$

where V_1 is the fundamental RMS amplitude, and V_2 through V_N are the amplitudes of the 2nd through Nth harmonics.

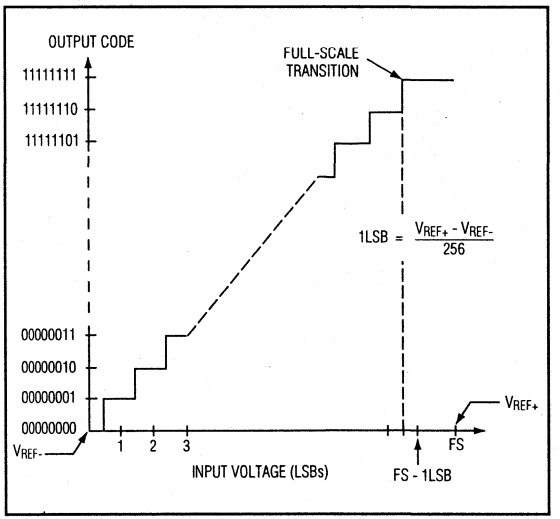


Figure 10. Transfer Function

Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is the ratio of the fundamental RMS amplitude to the amplitude of the next largest spectral component (in the frequency band above DC and below one-half the sample rate). Usually the next largest spectral component occurs at some harmonic of the input frequency. However, if the ADC is exceptionally linear, it may occur only at a random peak in the ADC's noise floor. See the Signal-to-Noise Ratio graph in *Typical Operating Characteristics*.

+5V, 1Msps, 4 & 8-Channel, 8-Bit ADCs with 1µA Power-Down

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX118CPI	0°C to +70°C	28 Wide Plastic DIP
MAX118CAI	0°C to +70°C	28 SSOP
MAX118C/D	0°C to +70°C	Dice*
MAX118EPI	-40°C to +85°C	28 Wide Plastic DIP
MAX118EAI	-40°C to +85°C	28 SSOP
MAX118MJI	-55°C to +125°C	28 Wide CERDIP**

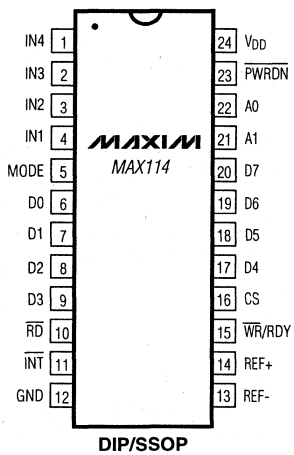
*Dice are specified at T_A = +25°C, DC parameters only.
**Contact factory for availability.

Chip Information

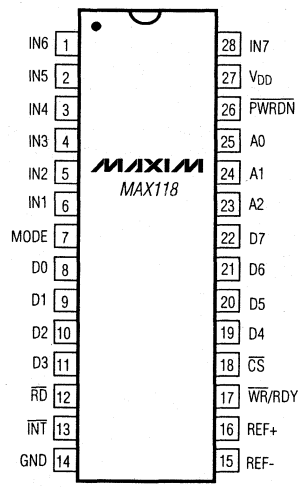
TRANSISTOR COUNT: 2011

Pin Configurations

TOP VIEW



DIP/SSOP



DIP/SSOP

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

10/96

MAXIM

2x4-Channel, Simultaneous-Sampling 14-Bit DAS

General Description

The MAX125/MAX126 are high-speed, multi-channel, 14-bit data-acquisition systems (DAS) with simultaneous track/holds. These devices contain a 14-bit, 3µs successive-approximation analog-to-digital converter (ADC), a +2.5V reference, a buffered reference input, an internal 16MHz clock, and a bank of four simultaneous-sampling track/hold (T/H) amplifiers that preserve the relative phase information of the sampled inputs. The MAX125/MAX126 have two multiplexed inputs for each T/H, allowing a total of eight inputs. In addition, the converter is overvoltage tolerant to ±16.5V; when a conversion is in process, a fault condition on any other channel will **not** affect the conversion result.

An on-board sequencer converts from 1 to 4 channels. In the default mode, four T/H outputs are converted successively starting with channel 1 and ending with channel 4. An interrupt signal ($\overline{INT}$) is provided after the fourth conversion is complete. Convert 1, 2, or 3 channels by reprogramming the MAX125/MAX126 through the bidirectional parallel interface. Once programmed, the MAX125/MAX126 will continue to convert the specified number of channels until they are reprogrammed. The $\overline{INT}$ signal always follows the end of the last conversion in a conversion sequence. The ADC converts each assigned channel in 3µs and stores the result in an internal 14x4 RAM. Upon completion of the conversions, data can be accessed by applying successive pulses to the $\overline{RD}$ pin. Four successive reads access four data words sequentially.

The parallel interface's data-access and bus-release timing specifications are compatible with most popular digital signal processors and 16-bit/32-bit microprocessors, so the MAX125/MAX126 can be connected directly to these processors without resorting to wait states.

Applications

Multi-Phase Motor Control

Power-Grid Synchronization

Power-Factor Monitoring

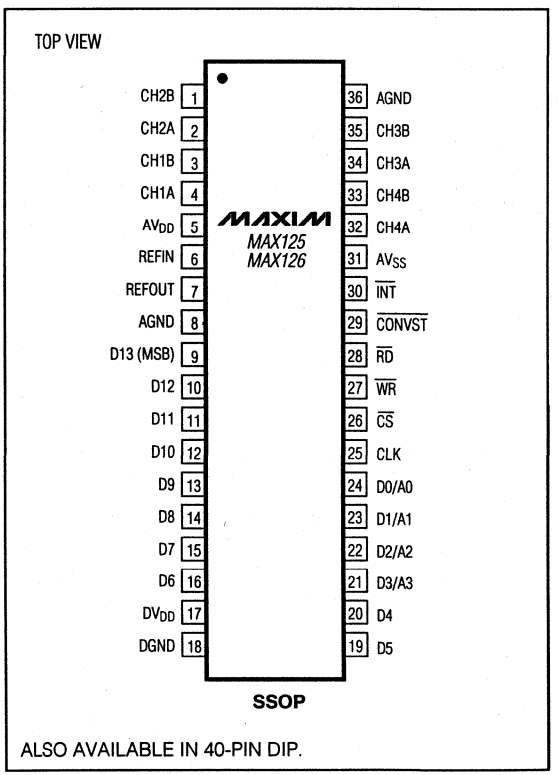
Digital Signal Processing

Vibration and Waveform Analysis

Features

- ♦ **Eight Single-Ended Inputs with Four Simultaneous-Sampling T/H Amplifiers**
- ♦ **3µs Conversion Time per Channel**
- ♦ **75ksps Throughput for Four Channels**
- ♦ **±5V Input Range (MAX125)**
  ±2.5V Input Range (MAX126)
- ♦ **Fault-Protected Input Multiplexer (±16.5V)**
- ♦ **±5V Supplies**
- ♦ **Internal, Buffered +2.5V Reference**
- ♦ **On-Board Sequencer Converts from 1 to 4 Channels**
- ♦ **High-Speed Parallel Interface with Fast Bus Relinquish Times**

Pin Configuration



ALSO AVAILABLE IN 40-PIN DIP.

7

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ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

10/96

MAXIM

+3V, Low-Power, 8-Channel, Serial 12-Bit DAS

General Description

The MAX146 is a +3V-powered, 12-bit data-acquisition system (DAS) that includes an 8-channel multiplexer, 2.5MHz bandwidth track/hold, 133ksps throughput, and serial interface. Its low power dissipation (less than 5mW) makes it ideal for battery-powered applications. Its analog inputs are software configurable for unipolar/bipolar and single-ended/differential operation.

The MAX146 has a 4-wire serial interface that operates at up to 2MHz and is compatible with SPI™, QSPI™, and Microwire™. A serial strobe output allows direct connection to TMS320-family digital signal processors. The MAX146 uses either its internal clock or an external serial-interface clock to perform successive-approximation conversions.

This device has an internal 2.50V reference and a reference-buffer amplifier that simplifies gain trim. It also provides a hard-wired shutdown ($\overline{SHDN}$) pin and two software-selectable power-down modes. Accessing the serial interface automatically powers up the device. By using the technique of powering down between conversions, the supply current can be reduced to under 10µA at slower sampling rates.

The MAX146 is available in a 20-pin DIP package, and in a 20-pin SSOP that occupies 50% less area than an SO package. For +5V operation, see the MAX186/MAX188 data sheet.

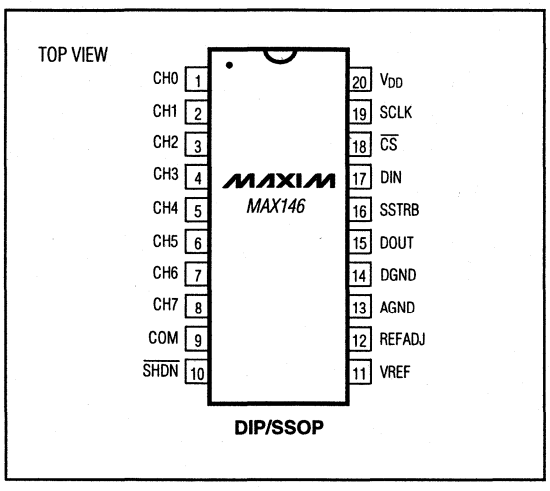
Features

- **8 Single-Ended or 4 Differential Inputs**
- **Single +2.7V to +3.6V Operation**
- **Low Power: 1.5mA (operating mode)**
  2µA (power-down mode)
- **Internal Track/Hold, 133kHz Sampling Rate**
- **Internal 2.50V Reference**
- **SPI™, QSPI™, Microwire™, TMS320-Compatible 4-Wire Serial Interface**
- **20-Pin DIP/SSOP Packages**

Applications

Portable Data Logging
Data Acquisition
High-Accuracy Process Control
Battery-Powered Instruments
Medical Instruments

Pin Configuration



Ordering Information

PART†	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX146ACPP	0°C to +70°C	20 Plastic DIP	±1/2
MAX146BCPP	0°C to +70°C	20 Plastic DIP	±1
MAX146ACAP	0°C to +70°C	20 SSOP	±1/2
MAX146BCAP	0°C to +70°C	20 SSOP	±1
MAX146BC/D	0°C to +70°C	Dice*	±1
MAX146AEPP	-40°C to +85°C	20 Plastic DIP	±1/2
MAX146BEPP	-40°C to +85°C	20 Plastic DIP	±1
MAX146AEAP	-40°C to +85°C	20 SSOP	±1/2
MAX146BEAP	-40°C to +85°C	20 SSOP	±1
MAX146AMJP	-55°C to +125°C	20 CERDIP	±1/2
MAX146BMJP	-55°C to +125°C	20 CERDIP	±1

**Dice are specified at T_A = +25°C, DC parameters only.*
†Contact factory for availability of SO package.

SPI and QSPI are trademarks of Motorola, Inc. Microwire is a trademark of National Semiconductor Corp.

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19-0465; Rev 0; 1/96

EVALUATION KIT AVAILABLE

MAXIM

+2.7V, Low-Power, 8-Channel, Serial 12-Bit ADC

General Description

The MAX147 12-bit data-acquisition system combines an 8-channel multiplexer, high-bandwidth track/hold, and serial interface with high conversion speed and ultra-low power consumption. It operates from a single +2.7V to +5.25V supply, and its analog inputs are software configurable for unipolar/bipolar and single-ended/differential operation.

The 4-wire serial interface directly connects to SPI™, QSPI™, and Microwire™ devices without external logic. A serial strobe output allows direct connection to TMS320-family digital signal processors. The MAX147 works with an external reference, and uses either the internal clock or an external serial-interface clock to perform successive-approximation analog-to-digital conversions.

This device provides a hard-wired $\overline{SHDN}$ pin and a software-selectable power-down. Accessing the serial interface automatically powers up the MAX147, and the quick turn-on time allows it to be shut down between all conversions. This technique can cut supply current to under 10µA at reduced sampling rates.

The MAX147 is available in a 20-pin DIP package and an SSOP that occupies 30% less area than an 8-pin DIP.

Applications

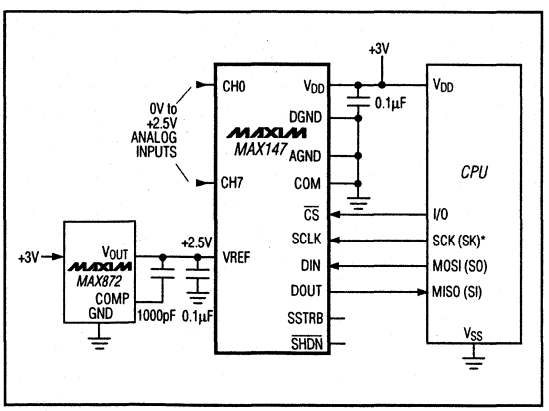
Portable Data Logging

Medical Instruments

Data Acquisition

Battery-Powered Instruments

Typical Operating Circuit



Features

- ♦ **8-Channel Single-Ended or 4-Channel Differential Inputs**
- ♦ **Single +2.7V to +5.25V Operation**
- ♦ **Low Power: 0.9mA (operating mode)**
  1µA (power-down mode)
- ♦ **Internal Track/Hold, 133kHz Sampling Rate**
- ♦ **SPI/QSPI/Microwire/TMS320-Compatible 4-Wire Serial Interface**
- ♦ **Software-Configurable Unipolar or Bipolar Inputs**
- ♦ **20-Pin DIP/SSOP Packages**

Ordering Information

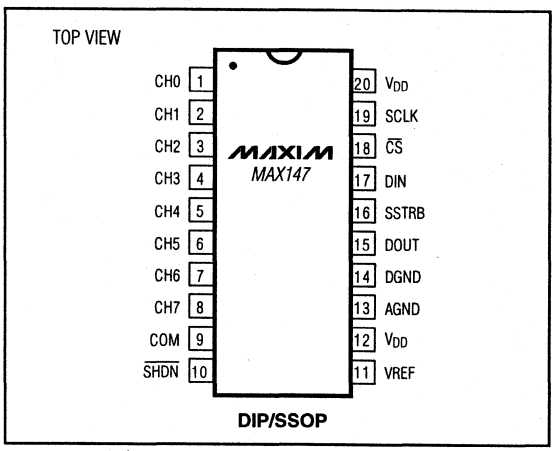
PART†	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX147ACPP	0°C to +70°C	20 Plastic DIP	±1/2
MAX147BCPP	0°C to +70°C	20 Plastic DIP	±1
MAX147ACAP	0°C to +70°C	20 SSOP	±1/2
MAX147BCAP	0°C to +70°C	20 SSOP	±1
MAX147BC/D	0°C to +70°C	Dice*	±1

Ordering Information continued at end of data sheet.

† *Contact factory for availability of SO package.*

* *Dice are specified at T_A = +25°C, DC parameters only.*

Pin Configuration



SPI and QSPI are registered trademarks of Motorola, Inc. Microwire is a registered trademark of National Semiconductor Corp.

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+2.7V, Low-Power, 8-Channel, Serial 12-Bit ADC

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND, DGND ..... -0.3V to +6V
AGND to DGND ..... -0.3V to +0.3V
CH0–CH7, COM to AGND, DGND ..... -0.3V to (V_{DD} + 0.3V)
VREF to AGND ..... -0.3V to (V_{DD} + 0.3V)
Digital Inputs to DGND ..... -0.3V to +6V
Digital Outputs to DGND ..... -0.3V to (V_{DD} + 0.3V)
Digital Output Sink Current 25mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
SSOP (derate 8.00mW/°C above +70°C) 640mW
CERDIP (derate 11.11mW/°C above +70°C) 889mW
Operating Temperature Ranges
MAX147_C_P ..... 0°C to +70°C
MAX147_E_P ..... -40°C to +85°C
MAX147_MJP ..... -55°C to +125°C
Storage Temperature Range ..... -60°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +3.6V, COM = 0V, f_{CLK} = 2.0MHz, external clock (50% duty cycle), 15 clocks/conversion cycle (133ksps), VREF = 2.500V applied to VREF pin, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)						
Resolution			12			Bits
Relative Accuracy (Note 2)	INL	MAX147A		±0.15	±0.5	LSB
		MAX147B			±1.0	
Differential Nonlinearity	DNL	No missing codes over temperature			±1	LSB
Offset Error		MAX147A		±0.5	±3	LSB
		MAX147B		±0.5	±4	
Gain Error (Note 3)				±0.5	±4	LSB
Gain Temperature Coefficient				±0.25		ppm/°C
Channel-to-Channel Offset Matching				±0.2		LSB
DYNAMIC SPECIFICATIONS (10kHz sine wave input, 0Vp-p to 2.500Vp-p, 133ksps, 2.0MHz external clock, bipolar input mode)						
Signal-to-Noise + Distortion Ratio	SINAD		70			dB
Total Harmonic Distortion	THD	Up to the 5th harmonic			-80	dB
Spurious-Free Dynamic Range	SFDR		80			dB
Channel-to-Channel Crosstalk		65kHz, 2.500V_{p-p} (Note 4)		-85		dB
Small-Signal Bandwidth		-3dB rolloff		2.25		MHz
Full-Power Bandwidth				1.0		MHz
CONVERSION RATE						
Conversion Time (Note 5)	t_{CONV}	Internal clock, $\overline{SHDN}$ = FLOAT	5.5		7.5	µs
		Internal clock, $\overline{SHDN}$ = V_{DD}	35		65	
		External clock = 2MHz, 12 clocks/conversion	6			
Track/Hold Acquisition Time	t_{ACQ}				1.5	µs
Aperture Delay				30		ns
Aperture Jitter				<50		ps
Internal Clock Frequency		$\overline{SHDN}$ = FLOAT		1.8		MHz
		$\overline{SHDN}$ = V_{DD}		0.225		
External Clock Frequency			0.1		2.0	MHz
		Data transfer only	0		2.0	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +3.6V, COM = 0V, f_{CLK} = 2.0MHz, external clock (50% duty cycle), 15 clocks/conversion cycle (133ksps), VREF = 2.500V applied to VREF pin, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG/COM INPUTS						
Input Voltage Range, Single-Ended and Differential (Note 6)		Unipolar, COM = 0V			0 to VREF	V
		Bipolar, COM = VREF/2			±VREF/2	
Multiplexer Leakage Current		On/off leakage current, V_{IN} = 0V or V_{DD}		±0.01	±1	µA
Input Capacitance		(Note 7)		16		pF
EXTERNAL REFERENCE						
VREF Input Voltage Range (Note 8)			1.0		V_{DD} + 50mV	V
VREF Input Current		VREF = 2.500V		100	150	µA
VREF Input Resistance			18	25		kΩ
Shutdown VREF Input Current				0.01	10	µA
DIGITAL INPUTS (DIN, SCLK, $\overline{CS}$, $\overline{SHDN}$)						
DIN, SCLK, $\overline{CS}$ Input High Voltage	V_{INH}	V_{DD} ≤ 3.6V	2.0			V
		V_{DD} > 3.6V	3.0			
DIN, SCLK, $\overline{CS}$ Input Low Voltage	V_{INL}				0.8	V
DIN, SCLK, $\overline{CS}$ Input Hysteresis	V_{HYST}			0.2		V
DIN, SCLK, $\overline{CS}$ Input Leakage	I_{IN}	V_{IN} = 0V or V_{DD}		±0.01	±1	µA
DIN, SCLK, $\overline{CS}$ Input Capacitance	C_{IN}	(Note 7)			15	pF
$\overline{SHDN}$ Input High Voltage	V_{INH}		V_{DD} - 0.4			V
$\overline{SHDN}$ Input Low Voltage	V_{INL}				0.4	V
$\overline{SHDN}$ Input Current	I_{IN}	$\overline{SHDN}$ = 0V or V_{DD}			±4.0	µA
$\overline{SHDN}$ Input Mid Voltage	V_{IM}		1.1		V_{DD} - 1.1	V
$\overline{SHDN}$ Voltage, Floating	V_{FLT}	$\overline{SHDN}$ = open		V_{DD}/2		V
$\overline{SHDN}$ Maximum Allowed Leakage, Mid Input		$\overline{SHDN}$ = open			±100	nA
DIGITAL OUTPUTS (DOUT, SSTRB)						
Output Voltage Low	V_{OL}	I_{SINK} = 5mA			0.4	V
		I_{SINK} = 16mA			0.8	
Output Voltage High	V_{OH}	I_{SOURCE} = 0.5mA	V_{DD} - 0.5			V
Three-State Leakage Current	I_L	$\overline{CS}$ = V_{DD}		±0.01	±10	µA
Three-State Output Capacitance	C_{OUT}	$\overline{CS}$ = V_{DD} (Note 7)			15	pF
POWER REQUIREMENTS						
Positive Supply Voltage	V_{DD}	(Note 9)	2.70		5.25	V
Positive Supply Current	I_{DD}	Operating mode, full-scale input		0.9	1.5	mA
		Power-down		1.2	10	µA
Supply Rejection (Note 10)	PSR	V_{DD} = 2.7V to 3.6V, full-scale input, external reference = 2.500V		±0.3		mV

+2.7V, Low-Power, 8-Channel, Serial 12-Bit ADC

TIMING CHARACTERISTICS

(V_{DD} = +2.7V to +3.6V, COM = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

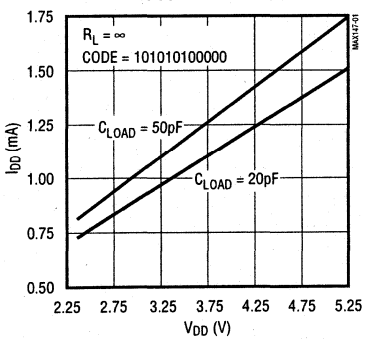
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Acquisition Time	t_{ACQ}			1.5			µs
DIN to SCLK Setup	t_{DS}			100			ns
DIN to SCLK Hold	t_{DH}					0	ns
SCLK Fall to Output Data Valid	t_{DO}	Figure 1, C_{LOAD} = 50pF	MAX147_C/E	20		200	ns
			MAX147_M	20		240	
$\overline{CS}$ Fall to Output Enable	t_{DV}	Figure 1, C_{LOAD} = 50pF				240	ns
$\overline{CS}$ Rise to Output Disable	t_{TR}	Figure 2, C_{LOAD} = 50pF				240	ns
$\overline{CS}$ to SCLK Rise Setup	t_{CSS}			100			ns
$\overline{CS}$ to SCLK Rise Hold	t_{CSH}			0			ns
SCLK Pulse Width High	t_{CH}			200			ns
SCLK Pulse Width Low	t_{CL}			200			ns
SCLK Fall to SSTRB	t_{SSTRB}	Figure 1				240	ns
$\overline{CS}$ Fall to SSTRB Output Enable	t_{SDV}	External clock mode only, Figure 1				240	ns
$\overline{CS}$ Rise to SSTRB Output Disable	t_{STR}	External clock mode only, Figure 2				240	ns
SSTRB Rise to SCLK Rise	t_{SCK}	Internal clock mode only (Note 7)		0			ns

Note 1: Tested at V_{DD} = 2.7V; COM = 0V; unipolar single-ended input mode.
Note 2: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range has been calibrated.
Note 3: External reference (VREF = +2.500V), offset nulled.
Note 4: Ground "on" channel; sine wave applied to all "off" channels.
Note 5: Conversion time defined as the number of clock cycles multiplied by the clock period; clock has 50% duty cycle.
Note 6: The common-mode range for the analog inputs is from AGND to V_{DD}.
Note 7: Guaranteed by design. Not subject to production testing.
Note 8: ADC performance is limited by the converter's noise floor, typically 300µVp-p.
Note 9: Electrical Characteristics are guaranteed from 2.7V to 3.6V. For operation beyond this range, see the *Typical Operating Characteristics*. For guaranteed specifications beyond 2.7V to 3.6V, contact the factory.
Note 10: Measured as $|V_{FS}(2.7V) - V_{FS}(3.6V)|$.

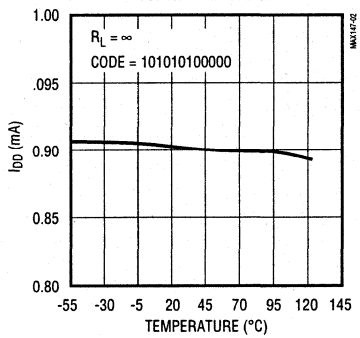
Typical Operating Characteristics

(V_{DD} = 3.0V, VREF = 2.500V, f_{CLK} = 2.0MHz, C_{LOAD} = 20pF, T_A = +25°C, unless otherwise noted.)

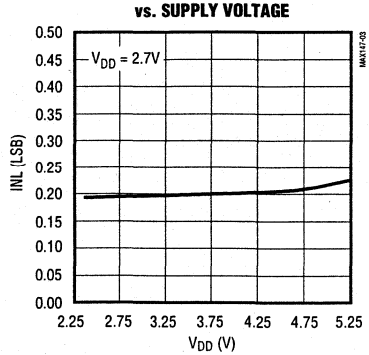
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



INTEGRAL NONLINEARITY vs. SUPPLY VOLTAGE

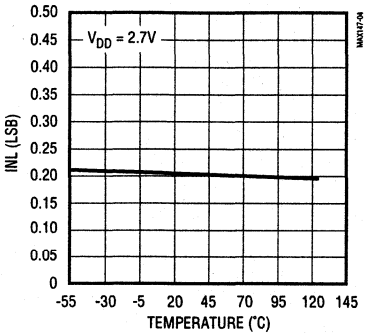


+2.7V, Low-Power, 8-Channel, Serial 12-Bit ADC

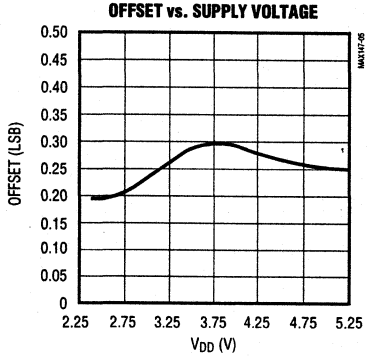
Typical Operating Characteristics (continued)

(V_{DD} = 3.0V, V_{REF} = 2.500V, f_{CLK} = 2.0MHz, C_{LOAD} = 20pF, T_A = +25°C, unless otherwise noted.)

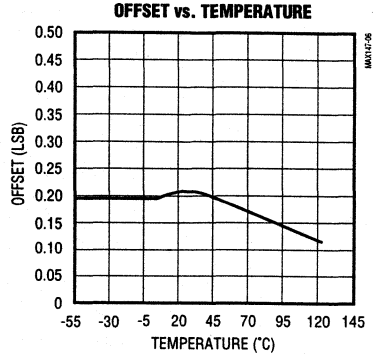
INTEGRAL NONLINEARITY vs. TEMPERATURE



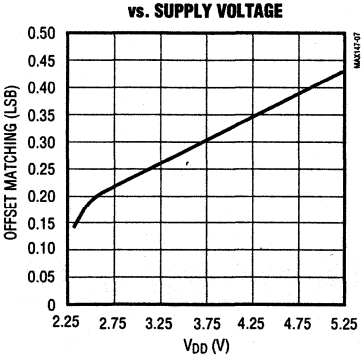
OFFSET vs. SUPPLY VOLTAGE



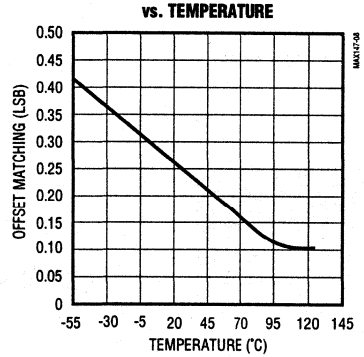
OFFSET vs. TEMPERATURE



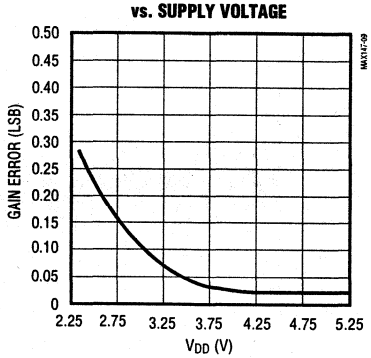
CHANNEL-TO-CHANNEL OFFSET MATCHING vs. SUPPLY VOLTAGE



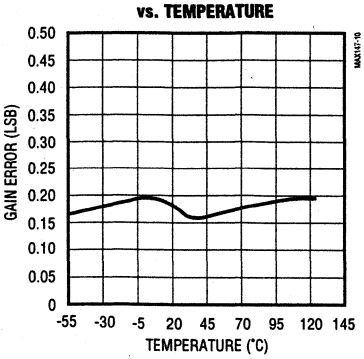
CHANNEL-TO-CHANNEL OFFSET MATCHING vs. TEMPERATURE



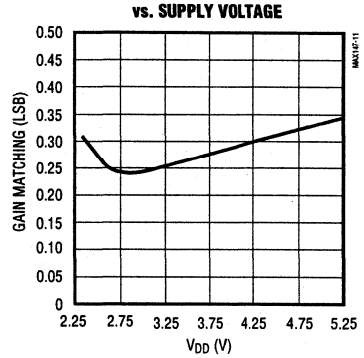
GAIN ERROR vs. SUPPLY VOLTAGE



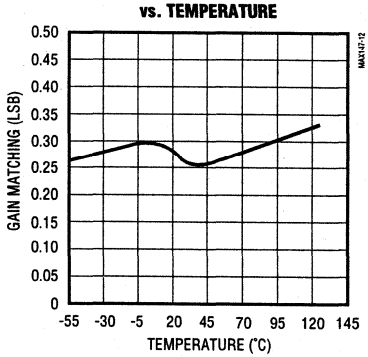
GAIN ERROR vs. TEMPERATURE



CHANNEL-TO-CHANNEL GAIN MATCHING vs. SUPPLY VOLTAGE



CHANNEL-TO-CHANNEL GAIN MATCHING vs. TEMPERATURE



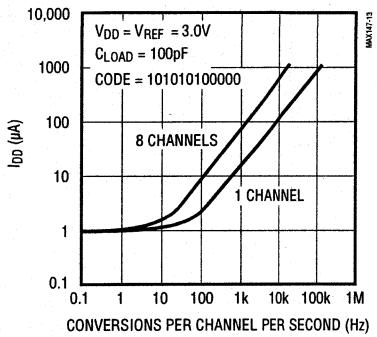
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+2.7V, Low-Power, 8-Channel, Serial 12-Bit ADC

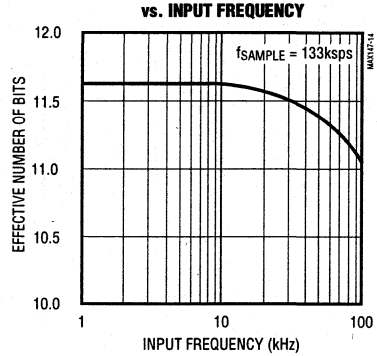
Typical Operating Characteristics (continued)

(V_{DD} = 3.0V, V_{REF} = 2.500V, f_{CLK} = 2.0MHz, C_{LOAD} = 20pF, T_A = +25°C, unless otherwise noted.)

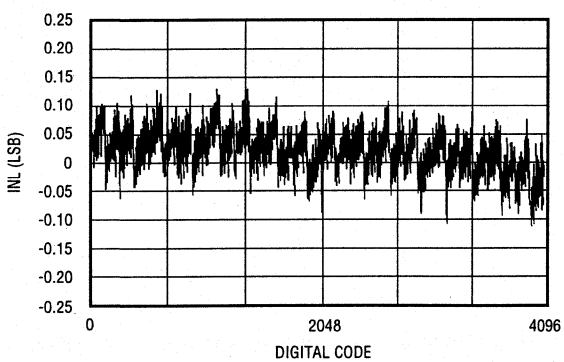
AVERAGE SUPPLY CURRENT vs. CONVERSION RATE



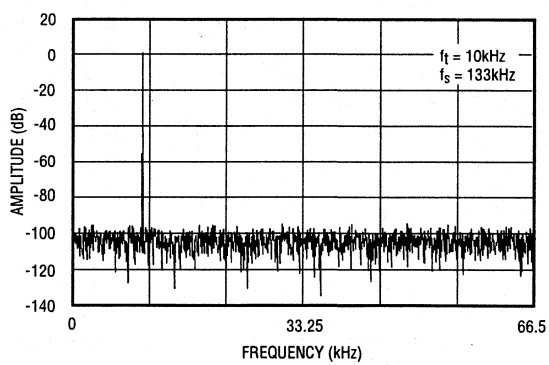
EFFECTIVE NUMBER OF BITS vs. INPUT FREQUENCY



INTEGRAL NONLINEARITY



FFT PLOT



Pin Description

PIN	NAME	FUNCTION
1–8	CH0–CH7	Sampling Analog Inputs
9	COM	Ground reference for analog inputs. Sets zero-code voltage in single-ended mode. Must be stable to ±0.5LSB.
10	$\overline{SHDN}$	Three-Level Shutdown Input. Pulling $\overline{SHDN}$ low shuts the MAX147 down to 10µA (max) supply current, otherwise the MAX147 is fully operational. Letting $\overline{SHDN}$ float sets the internal clock frequency to 1.8MHz. Pulling $\overline{SHDN}$ high sets the internal clock frequency to 225kHz. See *Hardware Power-Down* section.
11	VREF	External Reference Voltage Input for analog-to-digital conversion.
12, 20	V_{DD}	Positive Supply Voltage
13	AGND	Analog Ground
14	DGND	Digital Ground
15	DOUT	Serial Data Output. Data is clocked out at the falling edge of SCLK. High impedance when $\overline{CS}$ is high.
16	SSTRB	Serial Strobe Output. In internal clock mode, SSTRB goes low when the MAX147 begins the A/D conversion and goes high when the conversion is done. In external clock mode, SSTRB pulses high for one clock period before the MSB decision. High impedance when $\overline{CS}$ is high (external clock mode).
17	DIN	Serial Data Input. Data is clocked in at the rising edge of SCLK.
18	$\overline{CS}$	Active-Low Chip Select. Data will not be clocked into DIN unless $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT is high impedance.
19	SCLK	Serial Clock Input. Clocks data in and out of serial interface. In external clock mode, SCLK also sets the conversion speed. (Duty cycle must be 40% to 60%.)

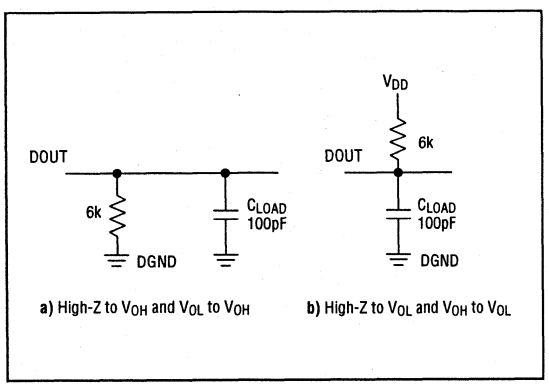


Figure 1. Load Circuits for Enable Time

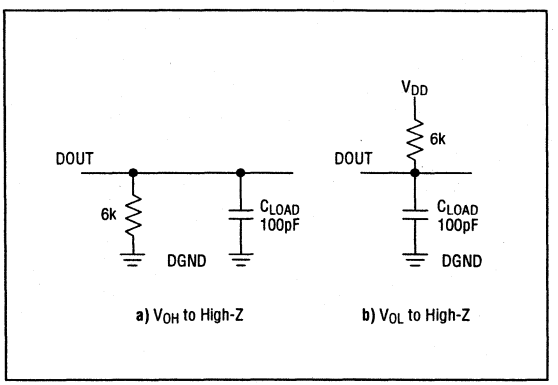


Figure 2. Load Circuits for Disable Time

+2.7V, Low-Power, 8-Channel, Serial 12-Bit ADC

Detailed Description

The MAX147 analog-to-digital converter (ADC) uses a successive-approximation conversion technique and input track/hold (T/H) circuitry to convert an analog signal to a 12-bit digital output. A flexible serial interface provides easy interface to microprocessors (µPs). No external hold capacitors are required. Figure 3 shows the block diagram of the MAX147.

Pseudo-Differential Input

The sampling architecture of the ADC's analog comparator is illustrated in the equivalent input circuit (Figure 4). In single-ended mode, IN+ is internally switched to CH0–CH7, and IN- is switched to COM. In differential mode, IN+ and IN- are selected from the following pairs: CH0/CH1, CH2/CH3, CH4/CH5, and CH6/CH7. Configure the channels with Tables 2 and 3.

In differential mode, IN- and IN+ are internally switched to either of the analog inputs. This configuration is pseudo-differential to the effect that only the signal at IN+ is sampled. The return side (IN-) must remain stable within ±0.5LSB (±0.1LSB for best results) with respect to AGND during a conversion. To accomplish this, connect a 0.1µF capacitor from IN- (the selected analog input) to AGND.

During the acquisition interval, the channel selected as the positive input (IN+) charges capacitor C_{HOLD}. The acquisition interval spans three SCLK cycles and ends on the falling SCLK edge after the last bit of the input control word has been entered. At the end of the acquisition interval, the T/H switch opens, retaining charge on C_{HOLD} as a sample of the signal at IN+.

The conversion interval begins with the input multiplexer switching C_{HOLD} from the positive input (IN+) to the negative input (IN-). In single-ended mode, IN- is simply COM. This unbalances node ZERO at the input of the comparator. The capacitive DAC adjusts during the remainder of the conversion cycle to restore node ZERO to 0V within the limits of 12-bit resolution. This action is equivalent to transferring a charge of 16pF x [(V_{IN+}) - (V_{IN-})] from C_{HOLD} to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog input signal.

Track/Hold

The T/H enters its tracking mode on the falling clock edge after the fifth bit of the 8-bit control word has been shifted in. It enters its hold mode on the falling clock edge after the eighth bit of the control word has been shifted in. If the converter is set up for single-ended inputs, IN- is connected to COM, and the converter samples the "+" input. If the converter is set up for differential inputs, IN- connects to the "-" input, and the difference of |IN+ - IN-| is sampled. At the end of the conversion, the positive input connects back to IN+, and C_{HOLD} charges to the input signal.

The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens, and more time must be allowed between conversions. The acquisition time,

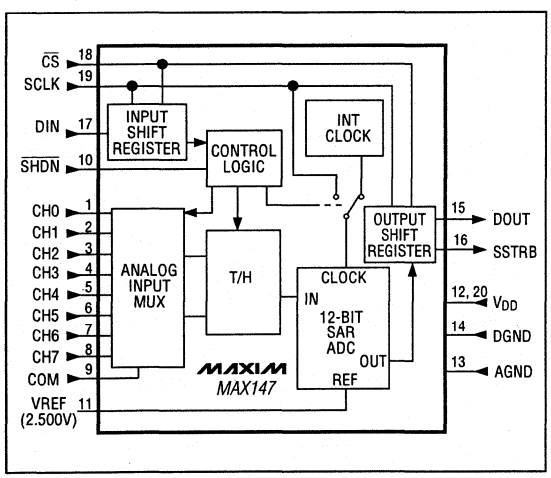


Figure 3. Block Diagram

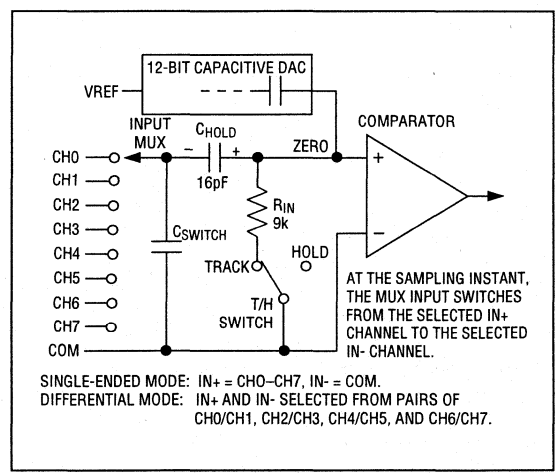


Figure 4. Equivalent Input Circuit

t_{ACQ}, is the maximum time the device takes to acquire the signal, and is also the minimum time needed for the signal to be acquired. It is calculated by:

$$t_{ACQ} = 9 \times (R_S + R_{IN}) \times 16pF$$

where R_{IN} = 9kΩ, R_S = the source impedance of the input signal, and t_{ACQ} is never less than 1.5µs. Note that source impedances below 1kΩ do not significantly affect the AC performance of the ADC.

Input Bandwidth

The ADC's input tracking circuitry has a 2.25MHz small-signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

Analog Input Protection

Internal protection diodes, which clamp the analog input to V_{DD} and AGND, allow the channel input pins to swing from AGND - 0.3V to V_{DD} + 0.3V without damage. However, for accurate conversions near full scale, the inputs must not exceed V_{DD} by more than 50mV or be lower than AGND by 50mV.

If the analog input exceeds 50mV beyond the supplies, do not forward bias the protection diodes of off channels over two milliamperes, as excessive current will degrade the conversion accuracy of the on channel.

Quick Look

To quickly evaluate the MAX147's analog performance, use the circuit of Figure 5. The MAX147 requires a control byte to be written to DIN before each conversion. Tying DIN to +3V feeds in control bytes of $FF (HEX), which trigger single-ended unipolar conversions on CH7 in external clock mode without powering down between conversions. In external clock mode, the SSTRB output pulses high for one clock period before the most significant bit of the 12-bit conversion result is shifted out of DOUT. Varying the analog input to CH7 will alter the sequence of bits from DOUT. A total of 15 clock cycles is required per conversion. All transitions of the SSTRB and DOUT outputs occur on the falling edge of SCLK.

How to Start a Conversion

A conversion is started by clocking a control byte into DIN. With $\overline{CS}$ low, each rising edge on SCLK clocks a bit from DIN into the MAX147's internal shift register. After $\overline{CS}$ falls, the first arriving logic "1" bit defines the MSB of the control byte. Until this first "start" bit arrives, any number of logic "0" bits can be clocked into DIN with no effect. Table 1 shows the control-byte format.

The MAX147 is compatible with Microwire™, SPI™, and QSPI™ devices. For SPI, select the correct clock polarity and sampling edge in the SPI control registers: set CPOL = 0 and CPHA = 0. Microwire, SPI, and QSPI all transmit a byte and receive a byte at the same time. Using the *Typical Operating Circuit,* the simplest software interface requires only three 8-bit transfers to

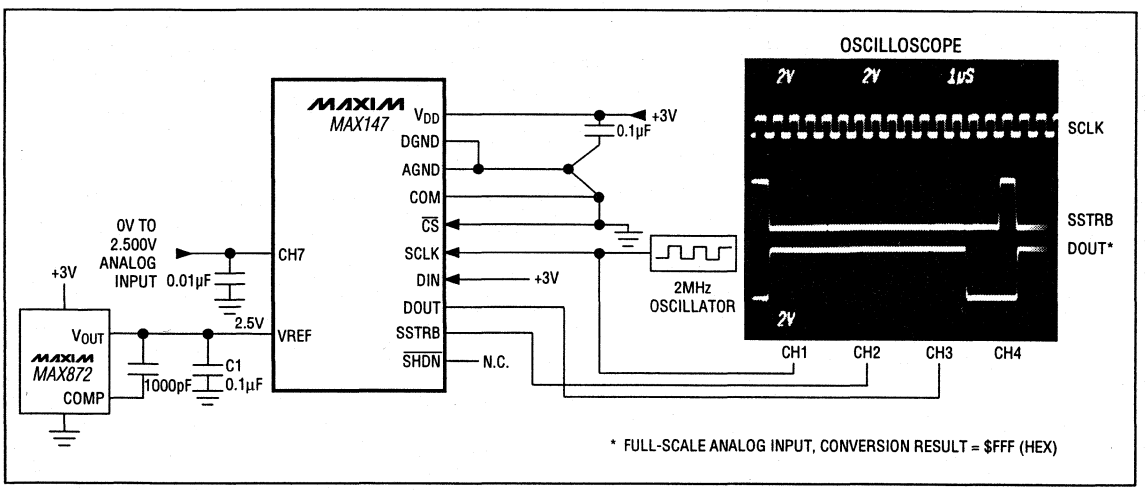


Figure 5. Quick-Look Circuit

+2.7V, Low-Power, 8-Channel, Serial 12-Bit ADC

Table 1. Control-Byte Format

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
START	SEL2	SEL1	SEL0	UNI/$\overline{\text{BIP}}$	SGL/$\overline{\text{DIF}}$	PD1	PD0

BIT	NAME	DESCRIPTION
7(MSB)	START	The first logic "1" bit after $\overline{\text{CS}}$ goes low defines the beginning of the control byte.
6 5 4	SEL2 SEL1 SEL0	These three bits select which of the eight channels are used for the conversion (Tables 2 and 3).
3	UNI/$\overline{\text{BIP}}$	1 = unipolar, 0 = bipolar. Selects unipolar or bipolar conversion mode. In unipolar mode, an analog input signal from 0V to VREF can be converted; in bipolar mode, the signal can range from -VREF/2 to +VREF/2.
2	SGL/$\overline{\text{DIF}}$	1 = single ended, 0 = differential. Selects single-ended or differential conversions. In single-ended mode, input signal voltages are referred to COM. In differential mode, the voltage difference between two channels is measured (Tables 2 and 3).
1 0(LSB)	PD1 PD0	Selects clock and power-down modes. PD1 PD0 Mode 0 0 Power-down (I_Q = 1.2µA) 0 1 Unassigned 1 0 Internal clock mode 1 1 External clock mode

Table 2. Channel Selection in Single-Ended Mode (SGL/$\overline{\text{DIF}}$ = 1)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	COM
0	0	0	+								–
1	0	0		+							–
0	0	1			+						–
1	0	1				+					–
0	1	0					+				–
1	1	0						+			–
0	1	1							+		–
1	1	1								+	–

Table 3. Channel Selection in Differential Mode (SGL/$\overline{\text{DIF}}$ = 0)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7
0	0	0	+	–						
0	0	1			+	–				
0	1	0					+	–		
0	1	1							+	–
1	0	0	–	+						
1	0	1			–	+				
1	1	0					–	+		
1	1	1							–	+

perform a conversion (one 8-bit transfer to configure the ADC, and two more 8-bit transfers to clock out the 12-bit conversion result). See Figure 17 for MAX147 QSPI connections.

Simple Software Interface

Make sure the CPU's serial interface runs in master mode so the CPU generates the serial clock. Choose a clock frequency from 100kHz to 2MHz.

1) Set up the control byte for external clock mode and call it TB1. TB1 should be of the format: 1XXXXX11 binary, where the Xs denote the particular channel and conversion mode selected.
2) Use a general-purpose I/O line on the CPU to pull $\overline{CS}$ low.
3) Transmit TB1 and, simultaneously, receive a byte and call it RB1. Ignore RB1.
4) Transmit a byte of all zeros ($00 HEX) and, simultaneously, receive byte RB2.
5) Transmit a byte of all zeros ($00 HEX) and, simultaneously, receive byte RB3.
6) Pull $\overline{CS}$ high.

Figure 6 shows the timing for this sequence. Bytes RB2 and RB3 will contain the result of the conversion padded with one leading zero and three trailing zeros. The total conversion time is a function of the serial clock frequency and the amount of idle time between 8-bit transfers. Make sure that the total conversion time does not exceed 120µs, to avoid excessive T/H droop.

Digital Output

In unipolar input mode, the output is straight binary (Figure 14). For bipolar inputs, the output is twos-complement (Figure 15). Data is clocked out at the falling edge of SCLK in MSB-first format.

Clock Modes

The MAX147 may use either an external serial clock or the internal clock to perform the successive-approximation conversion. In both clock modes, the external clock shifts data in and out of the MAX147. The T/H acquires the input signal as the last three bits of the control byte are clocked into DIN. Bits PD1 and PD0 of the control byte program the clock mode. Figures 7–10 show the timing characteristics common to both modes.

External Clock

In external clock mode, the external clock not only shifts data in and out, it also drives the analog-to-digital conversion steps. SSTRB pulses high for one clock period after the last bit of the control byte. Successive-approximation bit decisions are made and appear at DOUT on each of the next 12 SCLK falling edges (Figure 6). SSTRB and DOUT go into a high-impedance state when $\overline{CS}$ goes high; after the next $\overline{CS}$ falling edge, SSTRB will output a logic low. Figure 8 shows the SSTRB timing in external clock mode.

The conversion must complete in some minimum time, or droop on the sample-and-hold capacitors may degrade conversion results. Use internal clock mode if the serial clock frequency is less than 100kHz, or if serial-clock interruptions could cause the conversion interval to exceed 120µs.

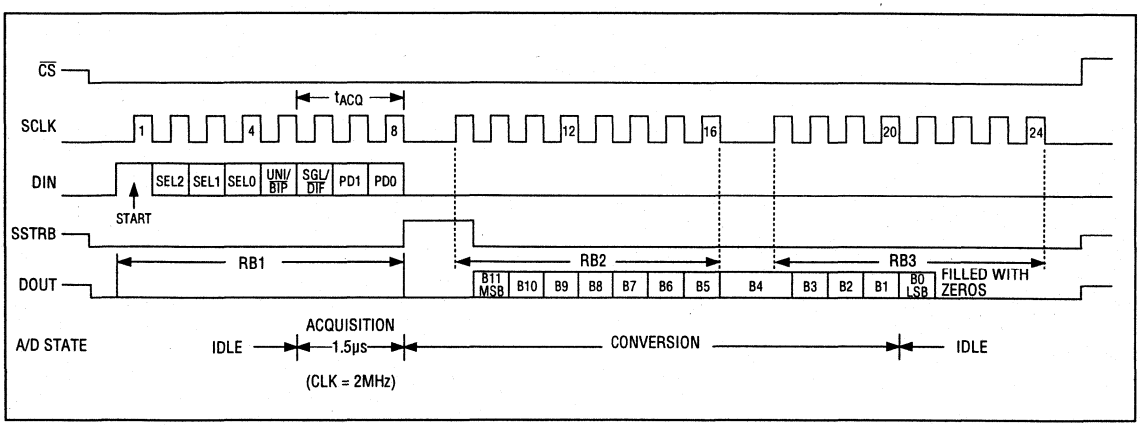


Figure 6. 24-Bit External-Clock-Mode Conversion Timing (Microwire and SPI Compatible, QSPI Compatible with $f_{CLK} \leq 2MHz$).

+2.7V, Low-Power, 8-Channel, Serial 12-Bit ADC

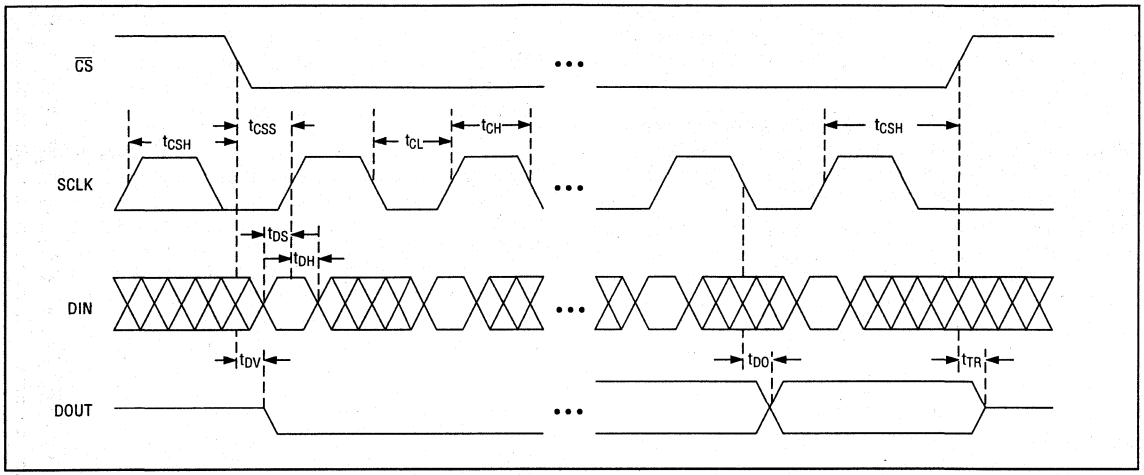


Figure 7. Detailed Serial-Interface Timing

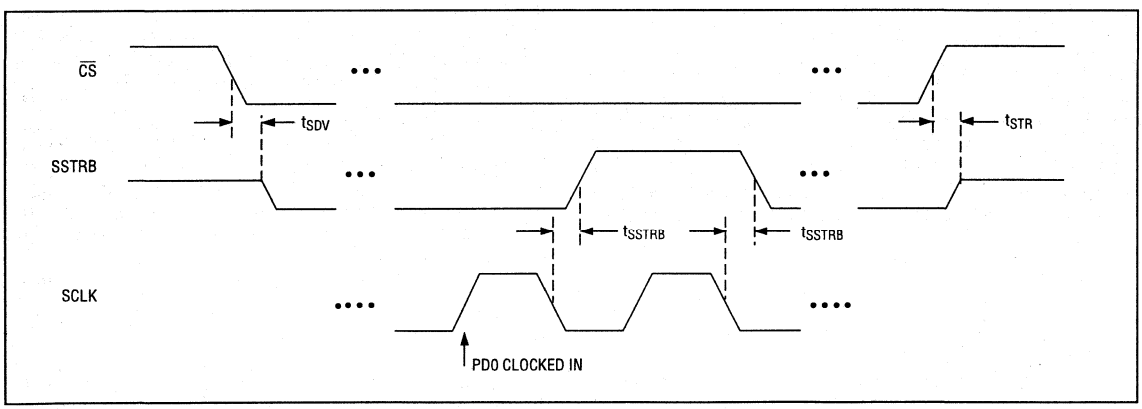


Figure 8. External-Clock-Mode SSTRB Detailed Timing

Internal Clock

In internal clock mode, the MAX147 generates its own conversion clock internally. This frees the µP from the burden of running the SAR conversion clock and allows the conversion results to be read back at the processor's convenience, at any clock rate from zero to 2MHz. SSTRB goes low at the start of the conversion and then goes high when the conversion is complete. SSTRB will be low for a maximum of 7.5µs ($\overline{SHDN}$ = FLOAT), during which time SCLK should remain low for best noise performance.

An internal register stores data when the conversion is in progress. SCLK clocks the data out of this register at any time after the conversion is complete. After SSTRB goes high, the next falling clock edge will produce the MSB of the conversion at DOUT, followed by the remaining bits in MSB-first format (Figure 9). $\overline{CS}$ does not need to be held low once a conversion is started. Pulling $\overline{CS}$ high prevents data from being clocked into the MAX147 and three-states DOUT, but it does not adversely affect an internal clock-mode conversion already in progress. When internal clock mode is

selected, SSTRB does not go into a high-impedance state when $\overline{CS}$ goes high.

Figure 10 shows the SSTRB timing in internal clock mode. In this mode, data can be shifted in and out of the MAX147 at clock rates exceeding 2.0MHz, provided that the minimum acquisition time, t_{ACQ}, is kept above 1.5µs.

Data Framing

The falling edge of $\overline{CS}$ does **not** start a conversion on the MAX147. The first logic high clocked into DIN is interpreted as a start bit and defines the first bit of the control byte. A conversion starts on the falling edge of SCLK, after the eighth bit of the control byte (the PD0 bit) is clocked into DIN. The start bit is defined as:

The first high bit clocked into DIN with $\overline{CS}$ low any time the converter is idle; e.g., after V_{DD} is applied.

OR

The first high bit clocked into DIN after bit 5 of a conversion in progress is clocked onto the DOUT pin.

If $\overline{CS}$ is toggled before the current conversion is complete, then the next high bit clocked into DIN is recognized as a start bit; the current conversion is terminated, and a new one is started.

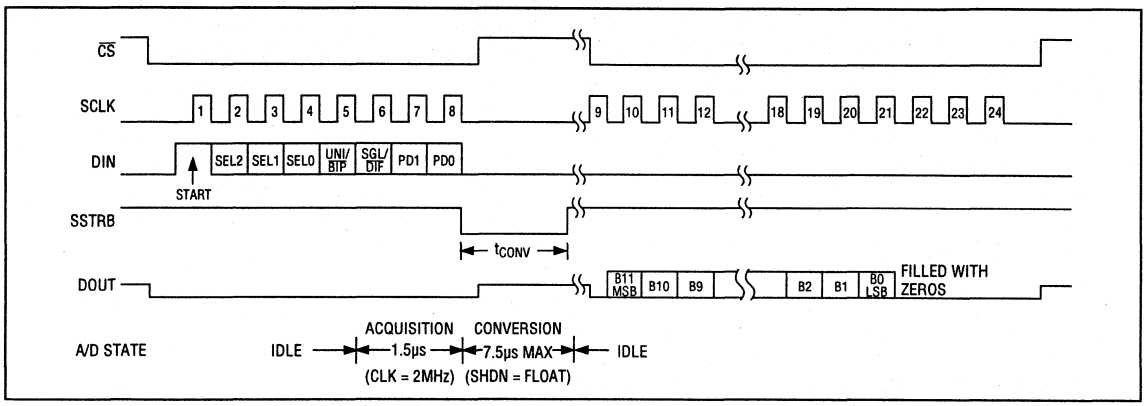


Figure 9. Internal Clock Mode Timing

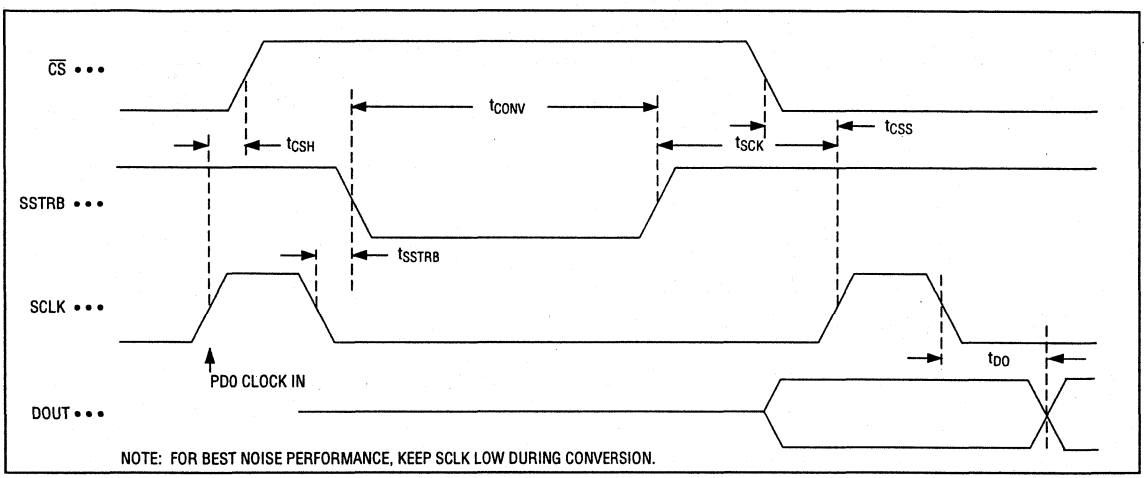


Figure 10. Internal Clock Mode SSTRB Detailed Timing

+2.7V, Low-Power, 8-Channel, Serial 12-Bit ADC

The fastest the MAX147 can run is 15 clocks per conversion. Figure 11a shows the serial-interface timing necessary to perform a conversion every 15 SCLK cycles in external clock mode.

Most microcontrollers require that conversions occur in multiples of eight SCLK clocks; 16 clocks per conversion will typically be the fastest that a microcontroller can drive the MAX147. Figure 11b shows the serial-interface timing necessary to perform a conversion every 16 SCLK cycles in external clock mode.

Applications Information

Power-On Reset

When power is first applied, and if $\overline{SHDN}$ is not pulled low, internal power-on reset circuitry will activate the MAX147 in internal clock mode, ready to convert with SSTRB = high. After the power supplies have been stabilized, the internal reset time is 10µs, and no conversions should be performed during this phase. SSTRB is high on power-up and, if $\overline{CS}$ is low, the first logical 1 on DIN will be interpreted as a start bit. Until a conversion takes place, DOUT will shift out zeros.

Power-Down

The MAX147's automatic power-down mode can save considerable power when operating at speeds below the maximum sampling rate. Figure 13 shows the average supply current as a function of the sampling rate. You can save power by placing the converter in a low-current shutdown state between conversions.

Select power-down via bits 1 and 0 of the DIN control byte with $\overline{SHDN}$ high (Tables 1 and 4). Pull $\overline{SHDN}$ low at any time to shut down the converter completely. $\overline{SHDN}$ overrides bits 1 and 0 of the control byte (Table 6).

Power-down mode turns off all chip functions that draw quiescent current, reducing I_{DD} typically to 1.2µA.

Figures 12a and 12b illustrate the various power-down sequences in both external and internal clock modes.

Software Power-Down

Software power-down is activated using bits PD1 and PD0 of the control byte. As shown in Table 6, PD1 and PD0 also specify the clock mode. When software shutdown is asserted, the ADC will continue to operate in the last specified clock mode until the conversion is complete. Then

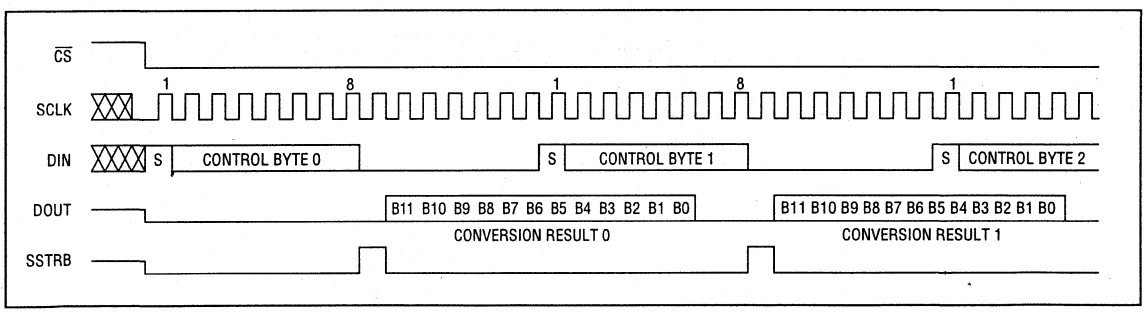


Figure 11a. External Clock Mode, 15 Clocks/Conversion Timing

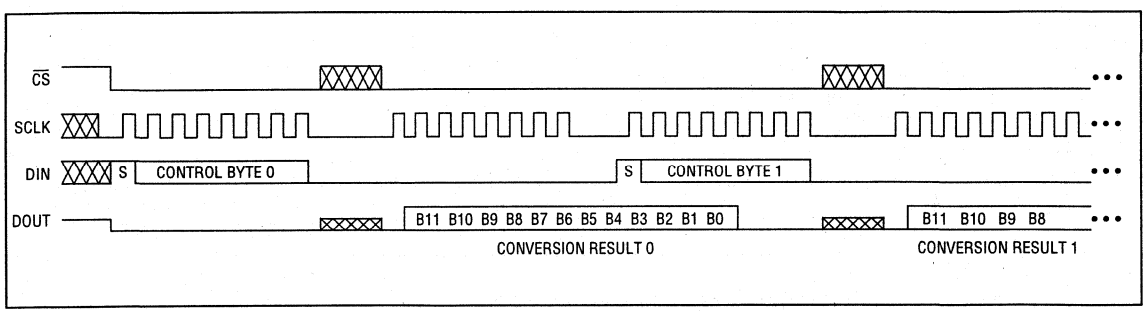


Figure 11b. External Clock Mode, 16 Clocks/Conversion Timing

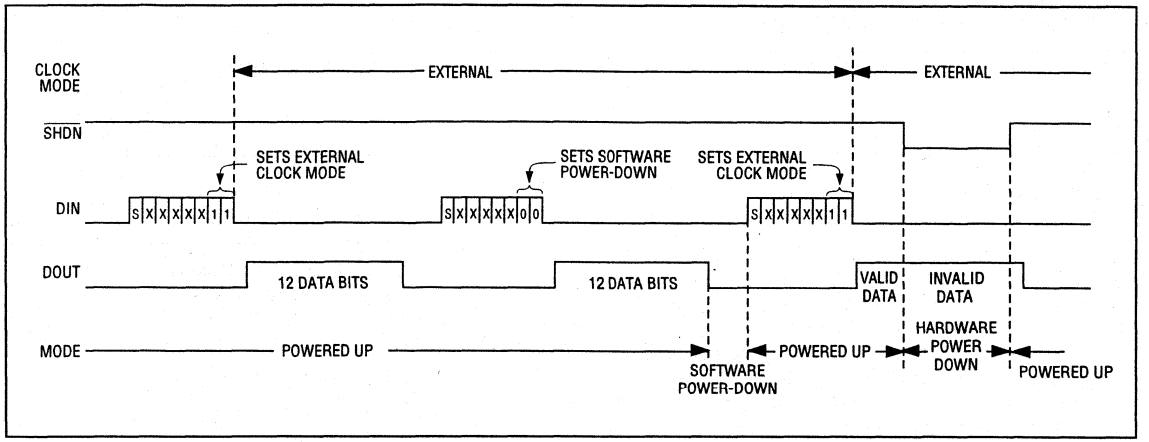


Figure 12a. Timing Diagram Power-Down Modes, External Clock

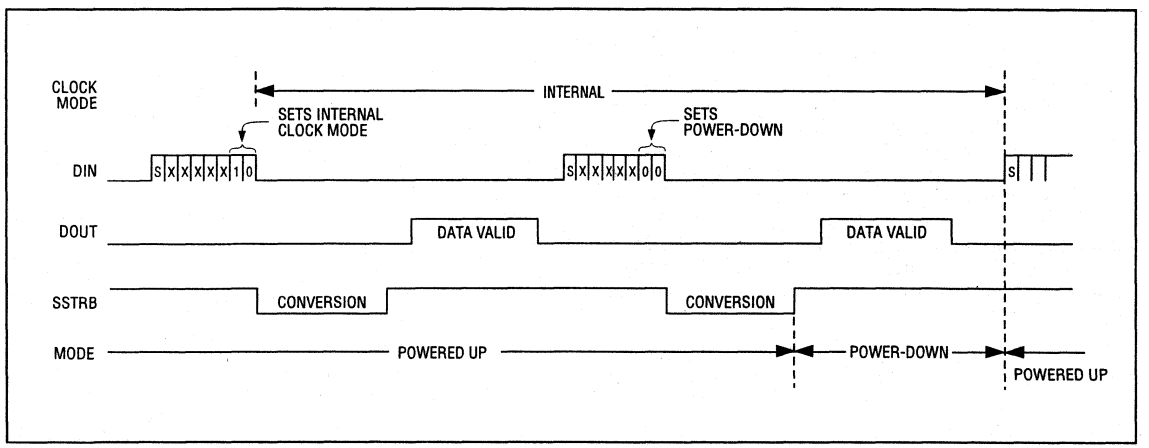


Figure 12b. Timing Diagram Power-Down Modes, Internal Clock

Table 4. Software Power-Down and Clock Mode

PD1	PD0	DEVICE MODE
1	1	External Clock
1	0	Internal Clock
0	1	Unassigned
0	0	Power-Down

Table 5. Hard-Wired Power-Down and Internal Clock Frequency

$\overline{SHDN}$ STATE	DEVICE MODE	INTERNAL CLOCK FREQUENCY
1	Enabled	225kHz
Floating	Enabled	1.8MHz
0	Power-Down	N/A

+2.7V, Low-Power, 8-Channel, Serial 12-Bit ADC

Table 6. Full Scale and Zero Scale

UNIPOLAR MODE		BIPOLAR MODE		
Full Scale	Zero Scale	Positive Full Scale	Zero Scale	Negative Full Scale
VREF + COM	COM	VREF/2 + COM	COM	-VREF/2 + COM

the ADC powers down into a low quiescent-current state. In internal clock mode, the interface remains active and conversion results may be clocked out after the MAX147 has entered a software power-down.

The first logical 1 on DIN will be interpreted as a start bit, and powers up the MAX147. Following the start bit, the data input word or control byte also determines clock mode and power-down states. For example, if the DIN word contains PD1 = 1, then the chip will remain powered up. If PD0 = PD1 = 0, a power-down will resume after one conversion.

Hardware Power-Down

Pulling $\overline{SHDN}$ low places the converter in hardware power-down. Unlike the software power-down mode, the conversion is not completed; it stops coincidentally with $\overline{SHDN}$ being brought low. $\overline{SHDN}$ also controls the clock frequency in internal clock mode. Letting $\overline{SHDN}$ float sets the internal clock frequency to 1.8MHz. When returning to normal operation with $\overline{SHDN}$ floating, there is a t_{RC} delay of approximately 2MΩ x C_L, where C_L is the capacitive loading on the $\overline{SHDN}$ pin. Pulling $\overline{SHDN}$ high sets the internal clock frequency to 225kHz. This feature eases the settling-time requirement for the reference voltage.

External Reference

An external reference is required for the MAX147. The reference voltage range is 1V to V_{DD}.

At VREF, the input impedance is a minimum of 18kΩ for DC currents. During a conversion, the reference must be able to deliver up to 250µA DC load current and have an output impedance of 10Ω or less. If the reference has higher output impedance or is noisy, bypass it close to the VREF pin with a 0.1µF capacitor.

Transfer Function

Table 6 shows the full-scale voltage ranges for unipolar and bipolar modes using a 2.5V reference.

The external reference must have a temperature coefficient of 4ppm/°C or less to achieve accuracy to within 1LSB over the commercial temperature range of 0°C to +70°C. See the MAX872 for a micropower 2.5V reference.

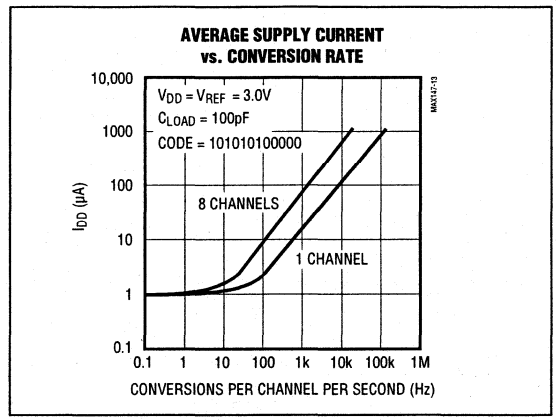


Figure 13. Average Supply Current vs. Conversion Rate

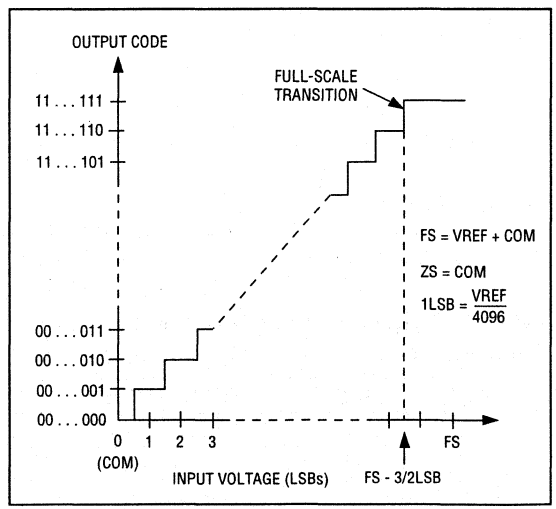


Figure 14. Unipolar Transfer Function, Full Scale (FS) = VREF + COM, Zero Scale (ZS) = COM

Figure 14 depicts the nominal, unipolar input/output (I/O) transfer function, and Figure 15 shows the bipolar input/output transfer function. Code transitions occur halfway between successive-integer LSB values. Output coding is binary, with 1LSB = 610µV (2.500V / 4096) for unipolar operation and 1LSB = 610µV [(2.500V / 2 - -2.500V / 2) / 4096] for bipolar operation.

Layout, Grounding, and Bypassing

For best performance, use printed circuit boards. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

Figure 16 shows the recommended system ground connections. A single-point analog ground ("star" ground point) should be established at AGND, separate from the logic ground. Connect all other analog grounds and DGND to the star ground. No other digital system ground should be connected to this ground. The ground return to the power supply for the star ground should be low impedance and as short as possible for noise-free operation.

High-frequency noise in the V_{DD} power supply may affect the high-speed comparator in the ADC. Bypass the supply to the star ground with 0.1µF and 4.7µF capacitors close to pin 20 of the MAX147. Minimize capacitor lead lengths for best supply-noise rejection. If the +3V power supply is very noisy, a 10Ω resistor can be connected as a lowpass filter (Figure 16).

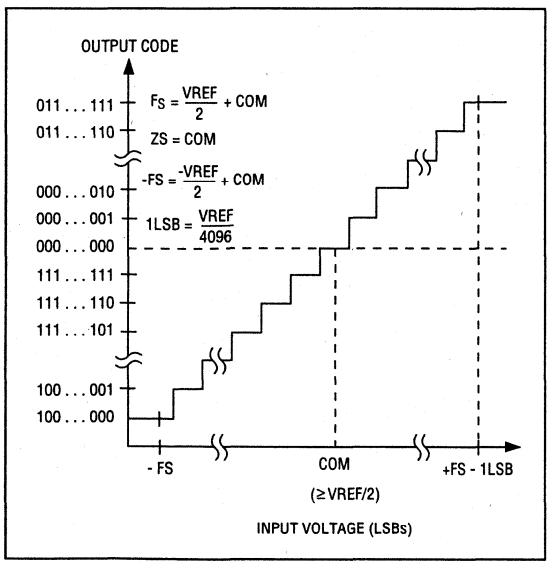


Figure 15. Bipolar Transfer Function, Full Scale (FS) = VREF/2 + COM, Zero Scale (ZS) = COM

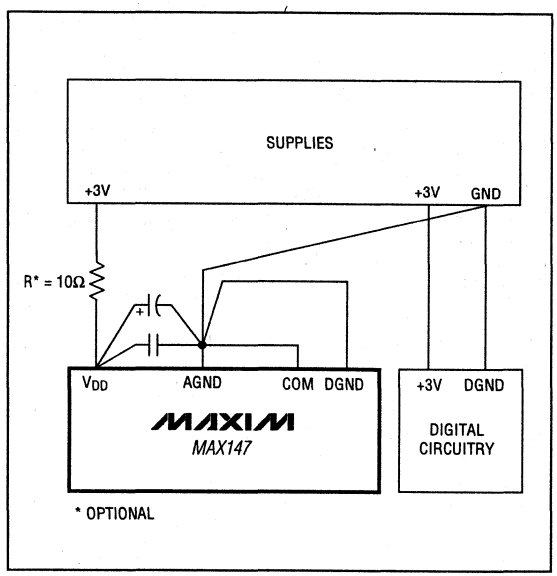


Figure 16. Power-Supply Grounding Connection

+2.7V, Low-Power, 8-Channel, Serial 12-Bit ADC

High-Speed Digital Interfacing with QSPI

The MAX147 can interface with QSPI using the circuit in Figure 17 (f_{SCLK} = 2.0MHz, C_{POL} = 0, C_{PHA} = 0). This QSPI circuit can be programmed to do a conversion on each of the eight channels. The result is stored in memory without taxing the CPU, since QSPI incorporates its own micro-sequencer.

Because the maximum external clock frequency is 2.0MHz, the MAX147 is QSPI compatible up to 2MHz.

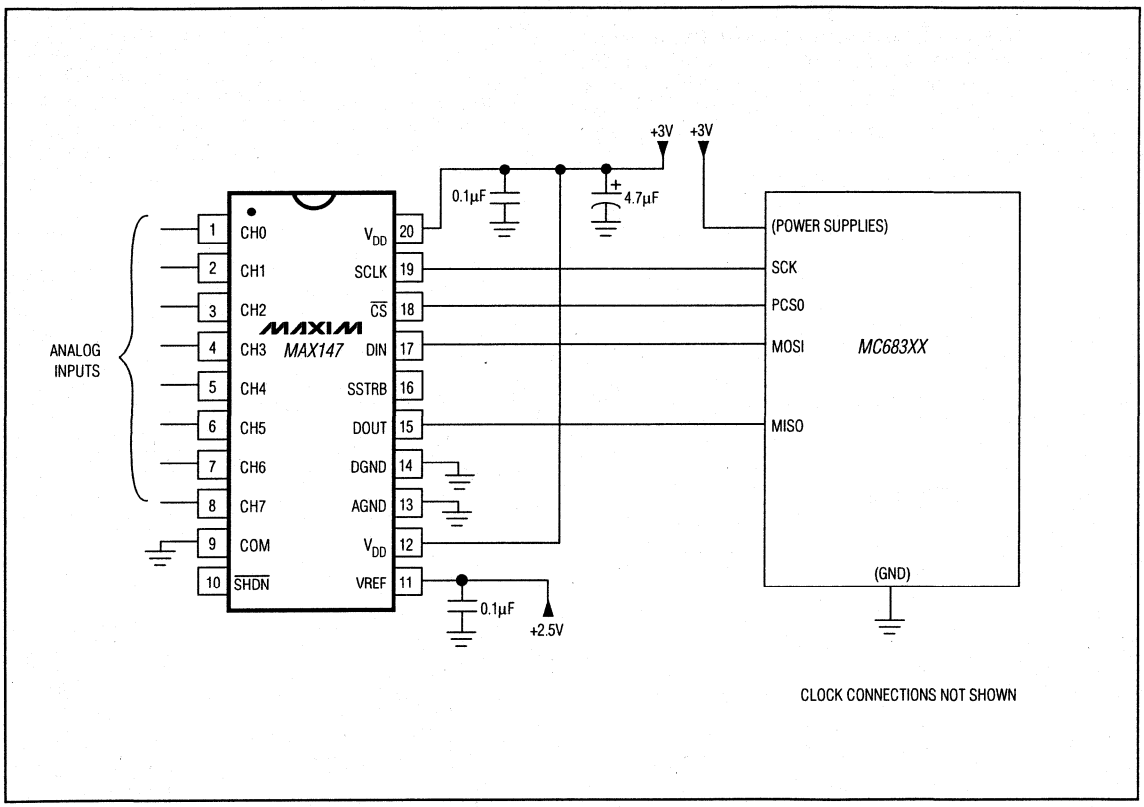


Figure 17. MAX147 QSPI Connections

TMS320LC3x-to-MAX147 Interface

Figure 18 shows an application circuit to interface the MAX147 to the TMS320 in external clock mode. The timing diagram for this interface circuit is shown in Figure 19.

Use the following steps to initiate a conversion in the MAX147 and to read the results:

1) The TMS320 should be configured with CLKX (transmit clock) as an active-high output clock and CLKR (TMS320 receive clock) as an active-high input clock. CLKX and CLKR on the TMS320 are tied together with the MAX147's SCLK input.
2) The MAX147's $\overline{CS}$ pin is driven low by the TMS320's XF_ I/O port, to enable data to be clocked into the MAX147's DIN.
3) An 8-bit word (1XXXXX11) should be written to the MAX147 to initiate a conversion and place the device into external clock mode. Refer to Table 1 to select the proper XXXXX bit values for your specific application.
4) The MAX147's SSTRB output is monitored via the TMS320's FSR input. A falling edge on the SSTRB output indicates that the conversion is in progress and data is ready to be received from the MAX147.
5) The TMS320 reads in one data bit on each of the next 16 rising edges of SCLK. These data bits represent the 12-bit conversion result followed by four trailing bits, which should be ignored.
6) Pull $\overline{CS}$ high to disable the MAX147 until the next conversion is initiated.

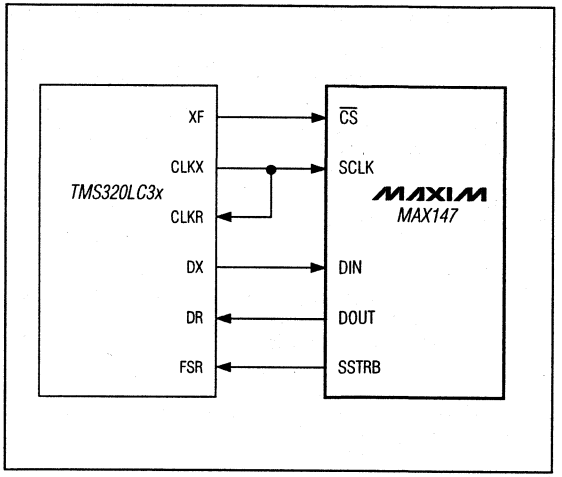


Figure 18. MAX147-to-TMS320 Serial Interface

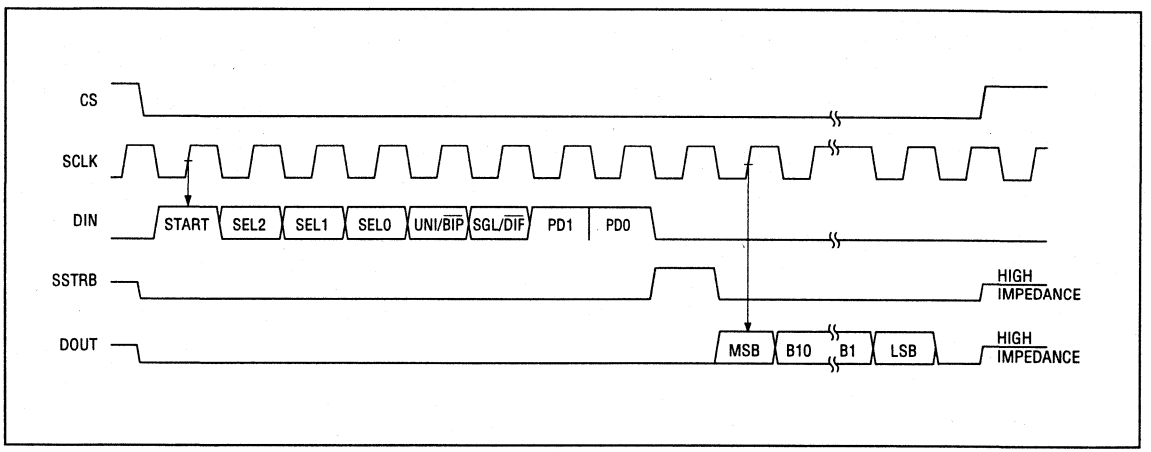


Figure 19. TMS320 Serial-Interface Timing Diagram

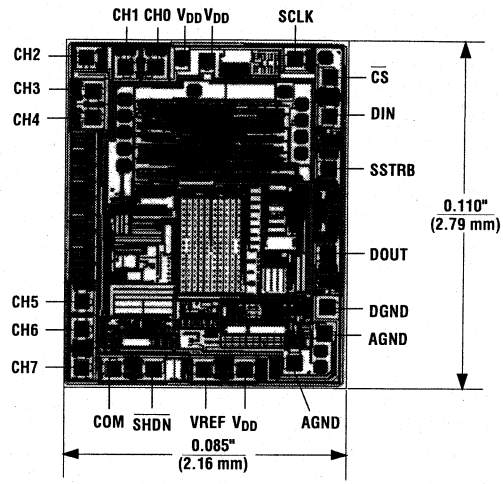
+2.7V, Low-Power, 8-Channel, Serial 12-Bit ADC

_Ordering Information (continued)

PART†	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX147AEPP	-40°C to +85°C	20 Plastic DIP	±1/2
MAX147BEPP	-40°C to +85°C	20 Plastic DIP	±1
MAX147AEAP	-40°C to +85°C	20 SSOP	±1/2
MAX147BEAP	-40°C to +85°C	20 SSOP	±1
MAX147AMJP	-55°C to +125°C	20 CERDIP**	±1/2
MAX147BMJP	-55°C to +125°C	20 CERDIP**	±1

† *Contact factory for availability of SO package.*
* *Dice are specified at T_A = +25°C, DC parameters only.*
** *Contact factory for availability.*

Chip Topography



TRANSISTOR COUNT: 2554
SUBSTRATE CONNECTED TO DGND

19-0464; Rev 0; 1/96

MAXIM

+2.7V, Low-Power, 8-Channel, Serial 10-Bit ADC

General Description

The MAX148 10-bit data-acquisition system combines an 8-channel multiplexer, high-bandwidth track/hold, and serial interface with high conversion speed and ultra-low power consumption. It operates from a single +2.7V to +5.25V supply, and its analog inputs are software configurable for unipolar/bipolar and single-ended/differential operation.

The 4-wire serial interface directly connects to SPI™, QSPI™, and Microwire™ devices without external logic. A serial strobe output allows direct connection to TMS320-family digital signal processors. The MAX148 requires an external reference, and uses either the internal clock or an external serial-interface clock to perform successive-approximation analog-to-digital conversions.

This device provides a hard-wired $\overline{SHDN}$ pin and a software-selectable power-down. Accessing the serial interface automatically powers up the MAX148, and the quick turn-on time allows it to be shut down between conversions. This technique can cut supply current to under 10µA at reduced sampling rates.

The MAX148 is available in a 20-pin DIP package and an SSOP that occupies 30% less area than an 8-pin DIP.

Applications

Portable Data Logging
Pen-Entry Devices
Battery-Powered Instruments
Data Acquisition
Medical Instruments

Features

- **8-Channel Single-Ended or 4-Channel Differential Inputs**
- **Single +2.7V to +5.25V Supply Operation**
- **Low Power: 0.9mA (operating mode)**
  1µA (power-down mode)
- **Internal Track/Hold, 133kHz Sampling Rate**
- **SPI/QSPI/Microwire/TMS320-Compatible 4-Wire Serial Interface**
- **Software-Configurable Unipolar or Bipolar Inputs**
- **20-Pin DIP/SSOP Packages**
- **Pin-Compatible 12-Bit Upgrade: MAX147**

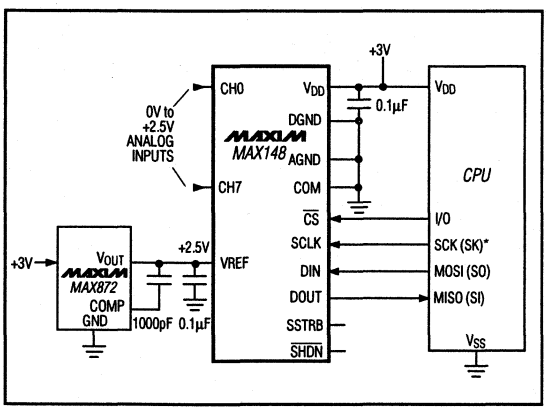
Ordering Information

PART†	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX148ACPP	0°C to +70°C	20 Plastic DIP	±1/2
MAX148BCPP	0°C to +70°C	20 Plastic DIP	±1
MAX148ACAP	0°C to +70°C	20 SSOP	±1/2
MAX148BCAP	0°C to +70°C	20 SSOP	±1

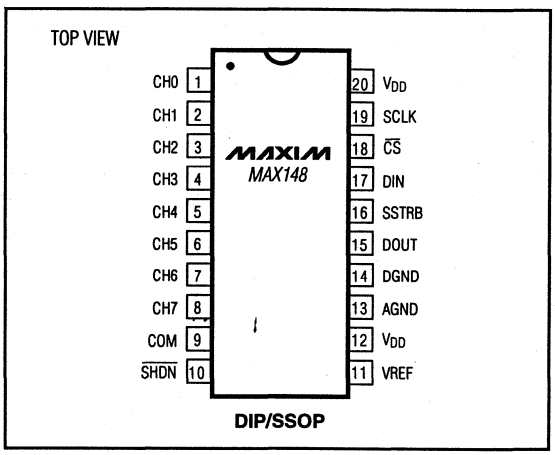
Ordering Information continued at end of data sheet.

† *Contact factory for availability of SO package.*

Typical Operating Circuit



Pin Configuration



SPI and QSPI are registered trademarks of Motorola, Inc. Microwire is a registered trademark of National Semiconductor Corp.

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

+2.7V, Low-Power, 8-Channel, Serial 10-Bit ADC

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND, DGND ..... -0.3V to +6V
AGND to DGND ..... -0.3V to +0.3V
CH0–CH7, COM to AGND, DGND ..... -0.3V to (V_{DD} + 0.3V)
VREF to AGND ..... -0.3V to (V_{DD} + 0.3V)
Digital Inputs to DGND ..... -0.3V to +6V
Digital Outputs to DGND ..... -0.3V to (V_{DD} + 0.3V)
Digital Output Sink Current 25mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
SSOP (derate 8.00mW/°C above +70°C) 640mW
CERDIP (derate 11.11mW/°C above +70°C) 889mW
Operating Temperature Ranges
MAX148_C_P ..... 0°C to +70°C
MAX148_E_P ..... -40°C to +85°C
MAX148_MJP ..... -55°C to +125°C
Storage Temperature Range ..... -60°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +3.6V, COM = 0V, f_{CLK} = 2.0MHz, external clock (50% duty cycle), 15 clocks/conversion cycle (133ksps), VREF = +2.500V applied to VREF pin, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)						
Resolution			10			Bits
Relative Accuracy (Note 2)	INL	MAX148A			±0.5	LSB
		MAX148B			±1.0	
Differential Nonlinearity	DNL	No missing codes over temperature			±1	LSB
Offset Error		MAX148A		±0.15	±1	LSB
		MAX148B		±0.15	±2	
Gain Error (Note 3)		MAX148A			±1	LSB
		MAX148B			±2	
Gain Temperature Coefficient				±0.25		ppm/°C
Channel-to-Channel Offset Matching				±0.05		LSB
DYNAMIC SPECIFICATIONS (10kHz sine wave input, 0Vp-p to 2.500Vp-p, 133ksps, 2.0MHz external clock, bipolar input mode)						
Signal-to-Noise + Distortion Ratio	SINAD			66		dB
Total Harmonic Distortion	THD	Up to the 5th harmonic		-70		dB
Spurious-Free Dynamic Range	SFDR			70		dB
Channel-to-Channel Crosstalk		65kHz, 2.500V_{p-p} (Note 4)		-75		dB
Small-Signal Bandwidth		-3dB rolloff		2.25		MHz
Full-Power Bandwidth				1.0		MHz
CONVERSION RATE						
Conversion Time (Note 5)	t_{CONV}	Internal clock, $\overline{SHDN}$ = FLOAT	5.5		7.5	µs
		Internal clock, $\overline{SHDN}$ = V_{DD}	35		65	
		External clock = 2MHz, 12 clocks/conversion	6			
Track/Hold Acquisition Time	t_{ACQ}				1.5	µs
Aperture Delay				30		ns
Aperture Jitter				<50		ps
Internal Clock Frequency		$\overline{SHDN}$ = FLOAT		1.8		MHz
		$\overline{SHDN}$ = V_{DD}		0.225		
External Clock Frequency			0.1		2.0	MHz
		Data transfer only	0		2.0	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +3.6V, COM = 0V, f_{CLK} = 2.0MHz, external clock (50% duty cycle), 15 clocks/conversion cycle (133ksps), VREF = +2.500V applied to VREF pin, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG/COM INPUTS						
Input Voltage Range, Single-Ended and Differential (Note 6)		Unipolar, COM = 0V			0 to VREF	V
		Bipolar, COM = VREF/2			±VREF/2	
Multiplexer Leakage Current		On/off leakage current, V_{IN} = 0V or V_{DD}		±0.01	±1	µA
Input Capacitance		(Note 7)		16		pF
EXTERNAL REFERENCE						
VREF Input Voltage Range (Note 8)			1.0		V_{DD} + 50mV	V
VREF Input Current		VREF = 2.500V		100	150	µA
VREF Input Resistance			18	25		kΩ
Shutdown VREF Input Current				0.01	10	µA
DIGITAL INPUTS (DIN, SCLK, $\overline{CS}$, $\overline{SHDN}$)						
DIN, SCLK, $\overline{CS}$ Input High Voltage	V_{INH}	$V_{DD} \le 3.6V$	2.0			V
		$V_{DD} > 3.6V$	3.0			
DIN, SCLK, $\overline{CS}$ Input Low Voltage	V_{INL}				0.8	V
DIN, SCLK, $\overline{CS}$ Input Hysteresis	V_{HYST}			0.2		V
DIN, SCLK, $\overline{CS}$ Input Leakage	I_{IN}	V_{IN} = 0V or V_{DD}		±0.01	±1	µA
DIN, SCLK, $\overline{CS}$ Input Capacitance	C_{IN}	(Note 7)			15	pF
$\overline{SHDN}$ Input High Voltage	V_{INH}		V_{DD} - 0.4			V
$\overline{SHDN}$ Input Low Voltage	V_{INL}				0.4	V
$\overline{SHDN}$ Input Current	I_{IN}	$\overline{SHDN}$ = 0V or V_{DD}			±4.0	µA
$\overline{SHDN}$ Input Mid Voltage	V_{IM}		1.1		V_{DD} - 1.1	V
$\overline{SHDN}$ Voltage, Floating	V_{FLT}	$\overline{SHDN}$ = open		V_{DD}/2		V
$\overline{SHDN}$ Maximum Allowed Leakage, Mid Input		$\overline{SHDN}$ = open			±100	nA
DIGITAL OUTPUTS (DOUT, SSTRB)						
Output Voltage Low	V_{OL}	I_{SINK} = 5mA			0.4	V
		I_{SINK} = 16mA			0.8	
Output Voltage High	V_{OH}	I_{SOURCE} = 0.5mA	V_{DD} - 0.5			V
Three-State Leakage Current	I_L	$\overline{CS}$ = V_{DD}		±0.01	±10	µA
Three-State Output Capacitance	C_{OUT}	$\overline{CS}$ = V_{DD} (Note 7)			15	pF
POWER REQUIREMENTS						
Positive Supply Voltage	V_{DD}	(Note 9)	2.70		5.25	V
Positive Supply Current	I_{DD}	Operating mode, full-scale input		0.9	1.5	mA
		Power-down		1.2	10	µA
Supply Rejection (Note 10)	PSR	V_{DD} = 2.7V to 3.6V, full-scale input, external reference = 2.500V		±0.3		mV

+2.7V, Low-Power, 8-Channel, Serial 10-Bit ADC

TIMING CHARACTERISTICS

(V_{DD} = +2.7V to +3.6V, COM = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Acquisition Time	t_{ACQ}			1.5			µs
DIN to SCLK Setup	t_{DS}			100			ns
DIN to SCLK Hold	t_{DH}					0	ns
SCLK Fall to Output Data Valid	t_{DO}	Figure 1, C_{LOAD} = 50pF	MAX148_C/E	20		200	ns
			MAX148_M	20		240	
$\overline{CS}$ Fall to Output Enable	t_{DV}	Figure 1, C_{LOAD} = 50pF				240	ns
$\overline{CS}$ Rise to Output Disable	t_{TR}	Figure 2, C_{LOAD} = 50pF				240	ns
$\overline{CS}$ to SCLK Rise Setup	t_{CSS}			100			ns
$\overline{CS}$ to SCLK Rise Hold	t_{CSH}			0			ns
SCLK Pulse Width High	t_{CH}			200			ns
SCLK Pulse Width Low	t_{CL}			200			ns
SCLK Fall to SSTRB	t_{SSTRB}	Figure 1				240	ns
$\overline{CS}$ Fall to SSTRB Output Enable	t_{SDV}	External clock mode only, Figure 1				240	ns
$\overline{CS}$ Rise to SSTRB Output Disable	t_{STR}	External clock mode only, Figure 2				240	ns
SSTRB Rise to SCLK Rise	t_{SCK}	Internal clock mode only (Note 7)		0			ns

Note 1: Tested at V_{DD} = +2.7V; COM = 0V; unipolar single-ended input mode.

Note 2: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range has been calibrated.

Note 3: External reference (VREF = +2.500V), offset nulled.

Note 4: Ground "on" channel; sine wave applied to all "off" channels.

Note 5: Conversion time defined as the number of clock cycles multiplied by the clock period; clock has 50% duty cycle.

Note 6: The common-mode range for the analog inputs is from AGND to V_{DD}.

Note 7: Guaranteed by design. Not subject to production testing.

Note 8: ADC performance is limited by the converter's noise floor, typically 300µVp-p.

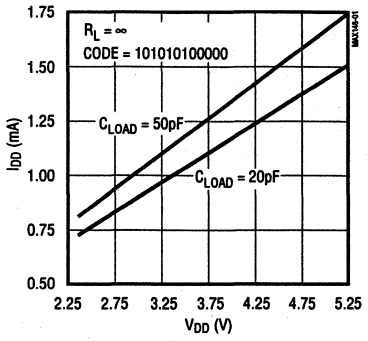
Note 9: Electrical Characteristics are guaranteed from 2.7V to 3.6V. For operation beyond this range, see the *Typical Operating Characteristics*. For guaranteed specifications beyond 2.7V to 3.6V, contact the factory.

Note 10: Measured as $|V_{FS}(2.7V) - V_{FS}(3.6V)|$.

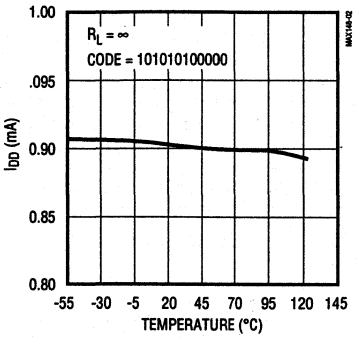
Typical Operating Characteristics

(V_{DD} = 3.0V, VREF = 2.5V, f_{CLK} = 2.0MHz, C_{LOAD} = 20pF, T_A = +25°C, unless otherwise noted.)

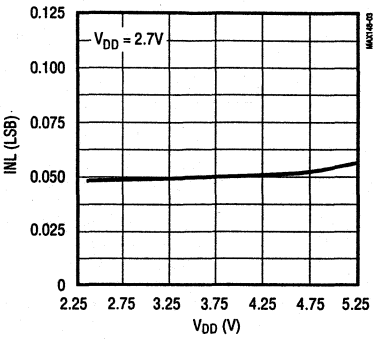
SUPPLY CURRENT vs. SUPPLY VOLTAGE



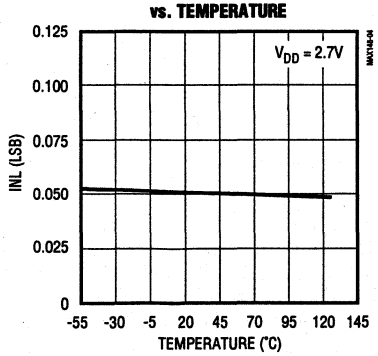
SUPPLY CURRENT vs. TEMPERATURE



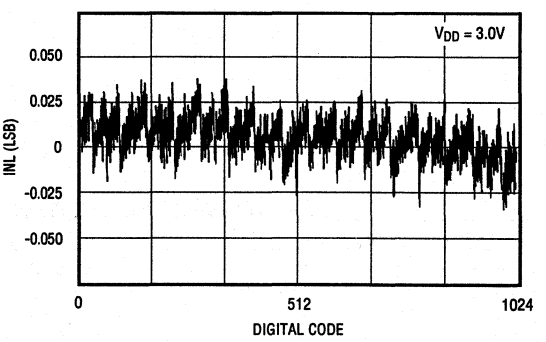
INTEGRAL NONLINEARITY vs. SUPPLY VOLTAGE



INTEGRAL NONLINEARITY vs. TEMPERATURE



INTEGRAL NONLINEARITY



7

+2.7V, Low-Power, 8-Channel, Serial 10-Bit ADC

Pin Description

PIN	NAME	FUNCTION
1–8	CH0–CH7	Sampling Analog Inputs
9	COM	Ground reference for analog inputs. Sets zero-code voltage in single-ended mode. Must be stable to ±0.5LSB.
10	$\overline{SHDN}$	Three-Level Shutdown Input. Pulling $\overline{SHDN}$ low shuts the MAX148 down to 10µA (max) supply current; otherwise the MAX148 is fully operational. Letting $\overline{SHDN}$ float sets the internal clock frequency to 1.8MHz. Pulling $\overline{SHDN}$ high sets the internal clock frequency to 225kHz. See *Hardware Power-Down* section.
11	VREF	External Reference Voltage Input for analog-to-digital conversion.
12, 20	V_{DD}	Positive Supply Voltage
13	AGND	Analog Ground
14	DGND	Digital Ground
15	DOUT	Serial Data Output. Data is clocked out at the falling edge of SCLK. High impedance when $\overline{CS}$ is high.
16	SSTRB	Serial Strobe Output. In internal clock mode, SSTRB goes low when the MAX148 begins the A/D conversion and goes high when the conversion is done. In external clock mode, SSTRB pulses high for one clock period before the MSB decision. High impedance when $\overline{CS}$ is high (external clock mode).
17	DIN	Serial Data Input. Data is clocked in at the rising edge of SCLK.
18	$\overline{CS}$	Active-Low Chip Select. Data will not be clocked into DIN unless $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT is high impedance.
19	SCLK	Serial Clock Input. Clocks data in and out of serial interface. In external clock mode, SCLK also sets the conversion speed. (Duty cycle must be 40% to 60%.)

Detailed Description

The MAX148 analog-to-digital converter (ADC) uses a successive-approximation conversion technique and input track/hold (T/H) circuitry to convert an analog signal to a 10-bit digital output. A flexible serial interface provides easy interface to microprocessors (µPs). No external hold capacitors are required. Figure 3 shows the block diagram for the MAX148.

Pseudo-Differential Input

The sampling architecture of the ADC's analog comparator is illustrated in the equivalent input circuit (Figure 4). In single-ended mode, IN+ is internally switched to CH0–CH7, and IN- is switched to COM. In differential mode, IN+ and IN- are selected from the following pairs: CH0/CH1, CH2/CH3, CH4/CH5, and CH6/CH7. Configure the channels with Tables 2 and 3.

In differential mode, IN- and IN+ are internally switched to either of the analog inputs. This configuration is pseudo-differential to the effect that only the signal at IN+ is sampled. The return side (IN-) must remain stable within ±0.5LSB (±0.1LSB for best results) with respect to AGND during a conversion. To accomplish this, connect a 0.1µF capacitor from IN- (the selected analog input) to AGND.

During the acquisition interval, the channel selected as the positive input (IN+) charges capacitor C_{HOLD}. The acquisition interval spans three SCLK cycles and ends on the falling SCLK edge after the last bit of the input control word has been entered. At the end of the acquisition interval, the T/H switch opens, retaining charge on C_{HOLD} as a sample of the signal at IN+.

The conversion interval begins with the input multiplexer switching C_{HOLD} from the positive input (IN+) to the negative input (IN-). In single-ended mode, IN- is simply COM. This unbalances node ZERO at the input of the comparator. The capacitive DAC adjusts during the remainder of the conversion cycle to restore node ZERO

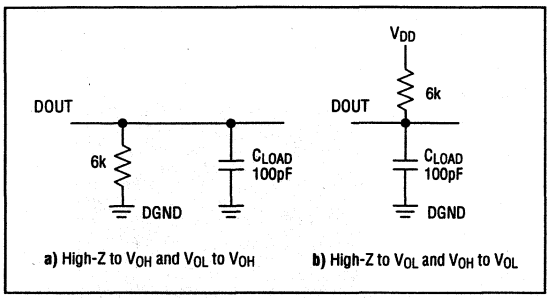


Figure 1. Load Circuits for Enable Time

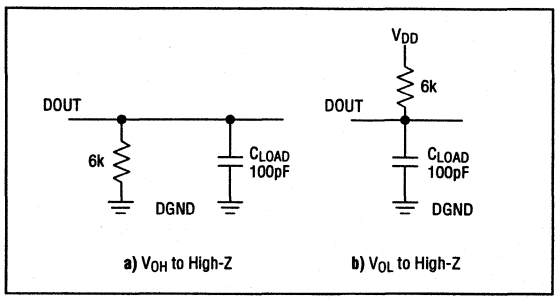


Figure 2. Load Circuits for Disable Time

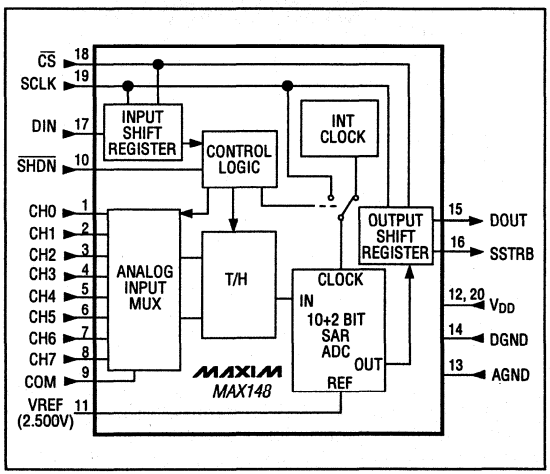


Figure 3. Block Diagram

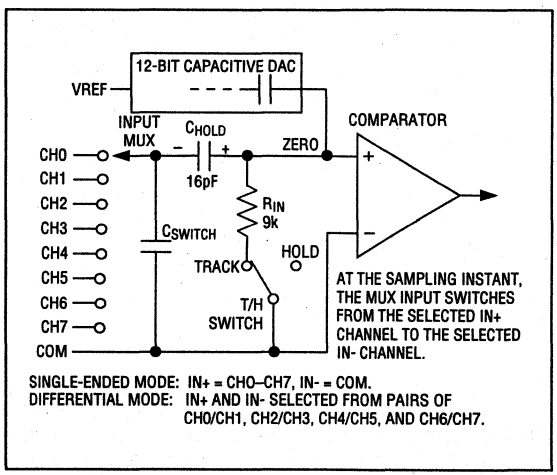


Figure 4. Equivalent Input Circuit

to 0V within the limits of 10-bit resolution. This action is equivalent to transferring a charge of 16pF x [(V_{IN+}) - (V_{IN-})] from C_{HOLD} to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog input signal.

Track/Hold

The T/H enters its tracking mode on the falling clock edge after the fifth bit of the 8-bit control word has been shifted in. It enters its hold mode on the falling clock edge after the eighth bit of the control word has been shifted in. If the converter is set up for single-ended inputs, IN- is connected to COM, and the converter samples the "+" input. If the converter is set up for differential inputs, IN- connects to the "-" input, and the difference of |IN+ - IN-| is sampled. At the end of the conversion, the positive input connects back to IN+, and C_{HOLD} charges to the input signal.

The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens, and more time must be allowed between conversions. The acquisition time, t_{ACQ}, is the maximum time the device takes to acquire the signal, and is also the minimum time needed for the signal to be acquired. It is calculated by:

$$t_{ACQ} = 7 \times (R_S + R_{IN}) \times 16pF$$

where R_{IN} = 9kΩ, R_S = the source impedance of the input signal, and t_{ACQ} is never less than 1.5µs. Note that source impedances below 4kΩ do not significantly affect the AC performance of the ADC.

+2.7V, Low-Power, 8-Channel, Serial 10-Bit ADC

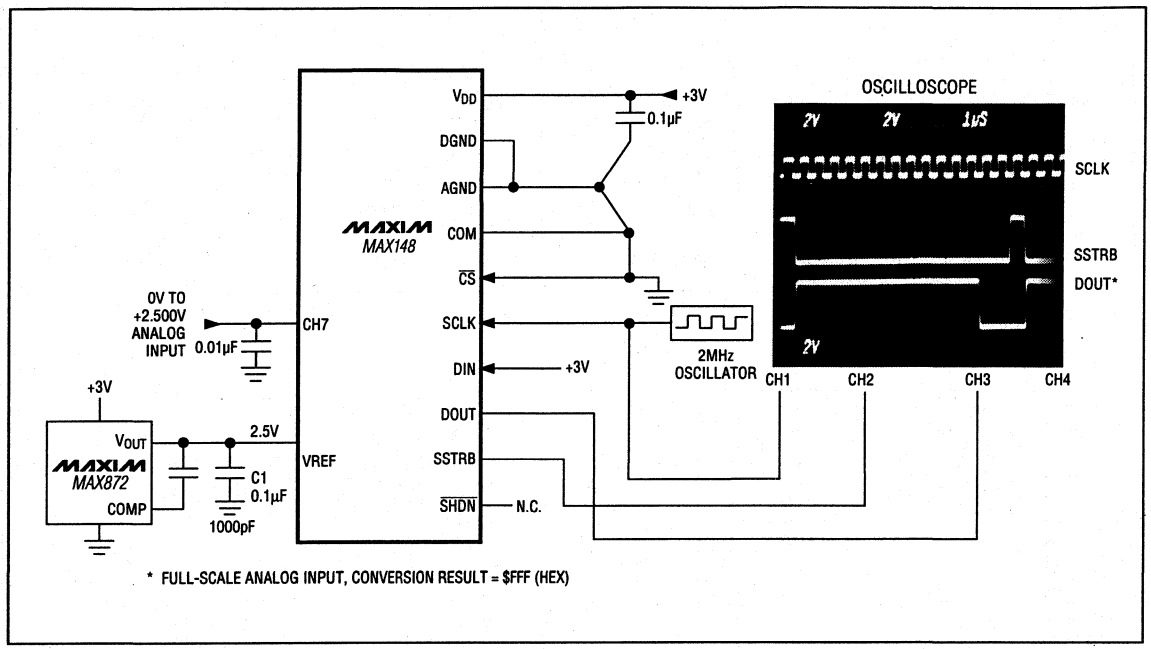


Figure 5. Quick-Look Circuit

Input Bandwidth

The ADC's input tracking circuitry has a 2.25MHz small-signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

Analog Input Protection

Internal protection diodes, which clamp the analog input to V_{DD} and AGND, allow the channel input pins to swing from AGND - 0.3V to V_{DD} + 0.3V without damage. However, for accurate conversions near full scale, the inputs must not exceed V_{DD} by more than 50mV or be lower than AGND by 50mV.

If the analog input exceeds 50mV beyond the supplies, do not forward bias the protection diodes of off channels over two milliamperes, as excessive current will degrade the conversion accuracy of the on channel.

Quick Look

To quickly evaluate the MAX148's analog performance, use the circuit of Figure 5. The MAX148 requires a control byte to be written to DIN before each conversion. Tying DIN to +3V feeds in control bytes of $FF (HEX), which trigger single-ended unipolar conversions on CH7 in external clock mode without powering down between conversions. In external clock mode, the SSTRB output pulses high for one clock period before the most significant bit of the conversion result is shifted out of DOUT. Varying the analog input to CH7 will alter the sequence of bits from DOUT. A total of 15 clock cycles is required per conversion. All transitions of the SSTRB and DOUT outputs occur on the falling edge of SCLK.

How to Start a Conversion

A conversion is started by clocking a control byte into DIN. With $\overline{CS}$ low, each rising edge on SCLK clocks a bit from DIN into the MAX148's internal shift register. After $\overline{CS}$ falls, the first arriving logic "1" bit defines the MSB of the control byte. Until this first "start" bit arrives, any number of logic "0" bits can be clocked into DIN with no effect. Table 1 shows the control-byte format.

Table 1. Control-Byte Format

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
START	SEL2	SEL1	SEL0	UNI/$\overline{BIP}$	SGL/$\overline{DIF}$	PD1	PD0

BIT	NAME	DESCRIPTION
7(MSB)	START	The first logic "1" bit after $\overline{CS}$ goes low defines the beginning of the control byte.
6 5 4	SEL2 SEL1 SEL0	These three bits select which of the eight channels are used for the conversion (Tables 2 and 3).
3	UNI/$\overline{BIP}$	1 = unipolar, 0 = bipolar. Selects unipolar or bipolar conversion mode. In unipolar mode, an analog input signal from 0V to VREF can be converted; in bipolar mode, the signal can range from -VREF/2 to +VREF/2.
2	SGL/$\overline{DIF}$	1 = single ended, 0 = differential. Selects single-ended or differential conversions. In single-ended mode, input signal voltages are referred to COM. In differential mode, the voltage difference between two channels is measured (Tables 2 and 3).
1 0(LSB)	PD1 PD0	Selects clock and power-down modes. PD1 PD0 Mode 0 0 Power-down (I_Q = 1.2µA) 0 1 Unassigned 1 0 Internal clock mode 1 1 External clock mode

Table 2. Channel Selection in Single-Ended Mode (SGL/$\overline{DIF}$ = 1)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	COM
0	0	0	+								–
1	0	0		+							–
0	0	1			+						–
1	0	1				+					–
0	1	0					+				–
1	1	0						+			–
0	1	1							+		–
1	1	1								+	–

Table 3. Channel Selection in Differential Mode (SGL/$\overline{DIF}$ = 0)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7
0	0	0	+	–						
0	0	1			+	–				
0	1	0					+	–		
0	1	1							+	–
1	0	0	–	+						
1	0	1			–	+				
1	1	0					–	+		
1	1	1							–	+

+2.7V, Low-Power, 8-Channel, Serial 10-Bit ADC

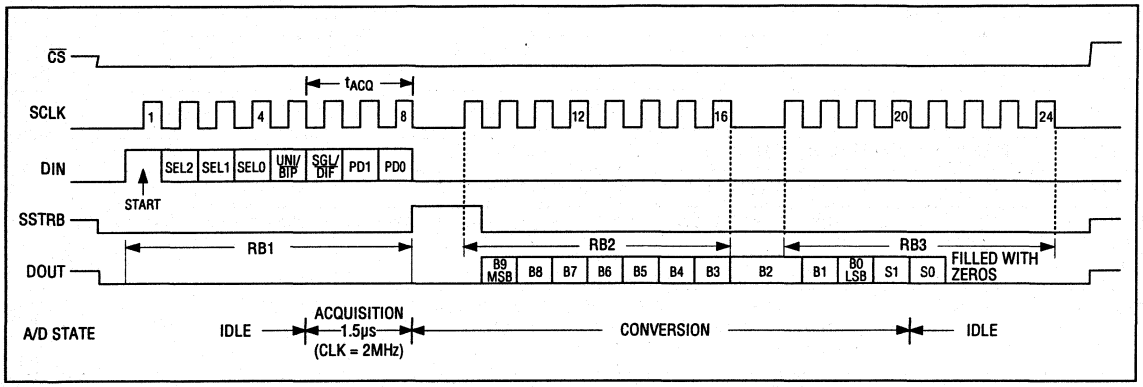


Figure 6. 24-Bit External-Clock-Mode Conversion Timing (Microwire and SPI Compatible, QSPI Compatible with $f_{CLK} \leq 2MHz$).

The MAX148 is compatible with Microwire™, SPI™, and QSPI™ devices. For SPI, select the correct clock polarity and sampling edge in the SPI control registers: set CPOL = 0 and CPHA = 0. Microwire, SPI, and QSPI all transmit a byte and receive a byte at the same time. Using the *Typical Operating Circuit,* the simplest software interface requires only three 8-bit transfers to perform a conversion (one 8-bit transfer to configure the ADC, and two more 8-bit transfers to clock out the conversion result). See Figure 17 for MAX148 QSPI connections.

Simple Software Interface

Make sure the CPU's serial interface runs in master mode so the CPU generates the serial clock. Choose a clock frequency from 100kHz to 2MHz.

1) Set up the control byte for external clock mode and call it TB1. TB1 should be of the format: 1XXXXX11 binary, where the Xs denote the particular channel and conversion mode selected.
2) Use a general-purpose I/O line on the CPU to pull $\overline{CS}$ low.
3) Transmit TB1 and, simultaneously, receive a byte and call it RB1. Ignore RB1.
4) Transmit a byte of all zeros ($00 HEX) and, simultaneously, receive byte RB2.
5) Transmit a byte of all zeros ($00 HEX) and, simultaneously, receive byte RB3.
6) Pull $\overline{CS}$ high.

Figure 6 shows the timing for this sequence. Bytes RB2 and RB3 will contain the result of the conversion padded with one leading zero, two sub-LSB bits, and three trailing zeros. The total conversion time is a function of the serial clock frequency and the amount of idle time between 8-bit transfers. Make sure that the total conversion time does not exceed 120µs, to avoid excessive T/H droop.

Digital Output

In unipolar input mode, the output is straight binary (Figure 14). For bipolar inputs, the output is twos-complement (Figure 15). Data is clocked out at the falling edge of SCLK in MSB-first format.

Clock Modes

The MAX148 may use either an external serial clock or the internal clock to perform the successive-approximation conversion. In both clock modes, the external clock shifts data in and out of the MAX148. The T/H acquires the input signal as the last three bits of the control byte are clocked into DIN. Bits PD1 and PD0 of the control byte program the clock mode. Figures 7–10 show the timing characteristics common to both modes.

External Clock

In external clock mode, the external clock not only shifts data in and out, it also drives the analog-to-digital conversion steps. SSTRB pulses high for one clock period after the last bit of the control byte. Successive-approximation bit decisions are made and appear at DOUT on each of the next 12 SCLK falling edges (Figure 6). SSTRB and DOUT go into a high-impedance state when $\overline{CS}$ goes high; after the next $\overline{CS}$ falling edge, SSTRB will output a logic low. Figure 8 shows the SSTRB timing in external clock mode.

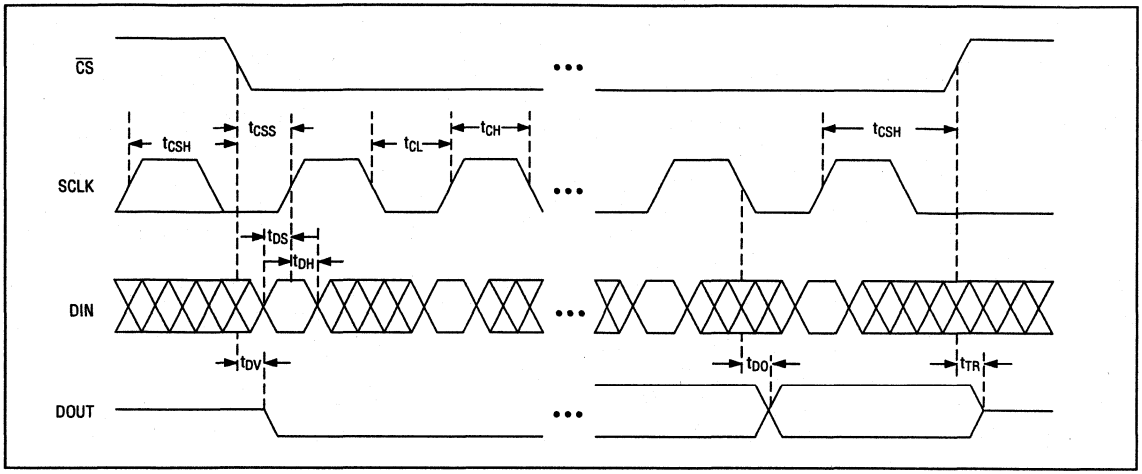


Figure 7. Detailed Serial-Interface Timing

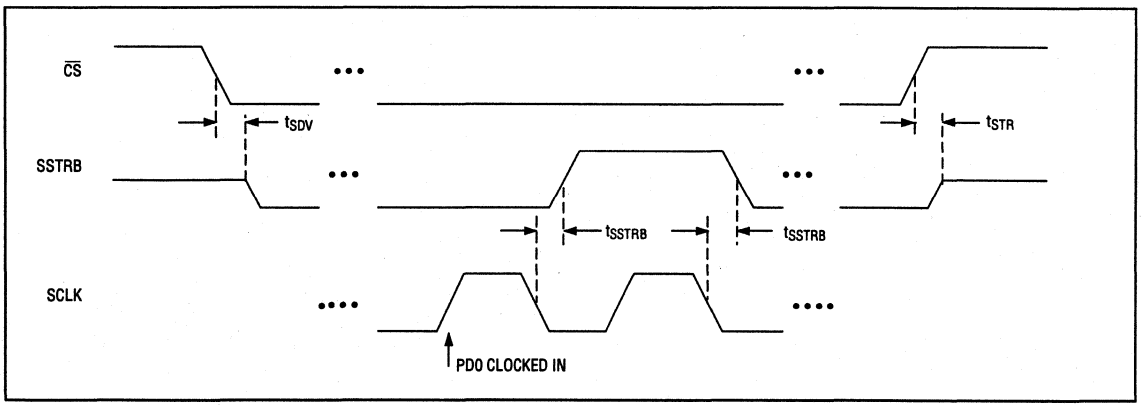


Figure 8. External-Clock-Mode SSTRB Detailed Timing

The conversion must complete in some minimum time, or droop on the sample-and-hold capacitors may degrade conversion results. Use internal clock mode if the serial clock frequency is less than 100kHz, or if serial-clock interruptions could cause the conversion interval to exceed 120µs.

Internal Clock

In internal clock mode, the MAX148 generates its own conversion clock internally. This frees the µP from the burden of running the SAR conversion clock and allows the conversion results to be read back at the processor's convenience, at any clock rate from zero to 2MHz. SSTRB goes low at the start of the conversion and then goes high when the conversion is complete. SSTRB will be low for a maximum of 7.5µs ($\overline{SHDN}$ = FLOAT), during which time SCLK should remain low for best noise performance.

An internal register stores data when the conversion is in progress. SCLK clocks the data out of this register at any time after the conversion is complete. After SSTRB goes high, the next falling clock edge will produce the MSB of the conversion at DOUT, followed by the

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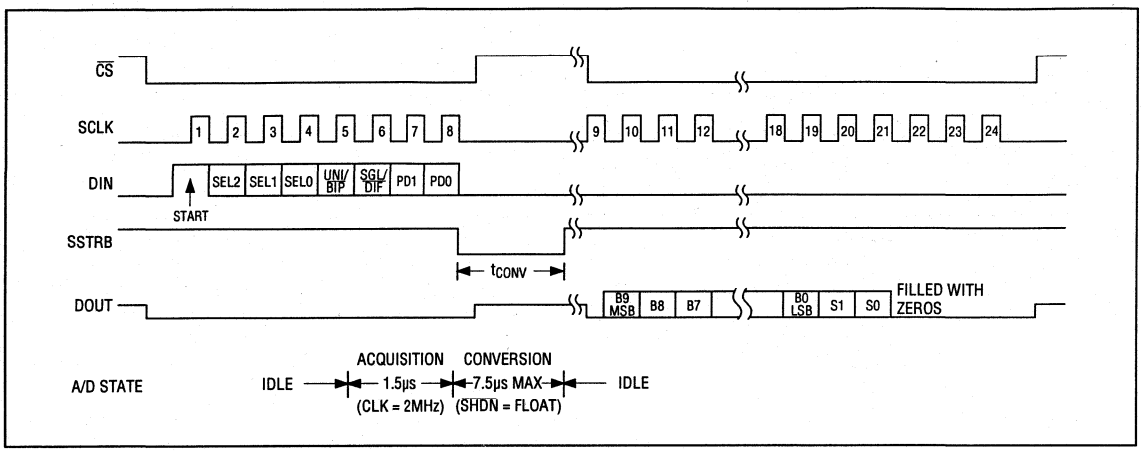


Figure 9. Internal Clock Mode Timing

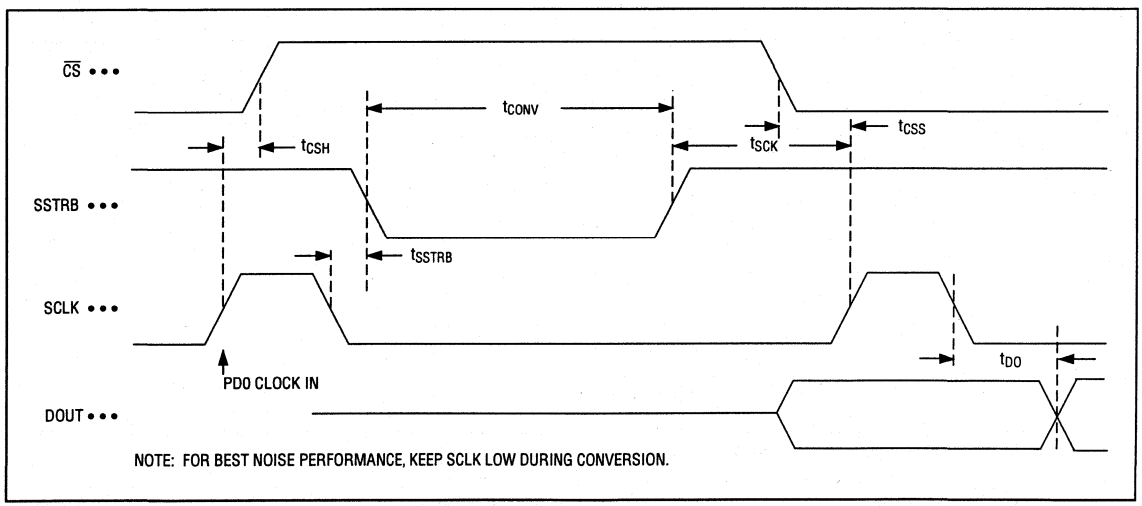


Figure 10. Internal Clock Mode SSTRB Detailed Timing

remaining bits in MSB-first format (Figure 9). $\overline{CS}$ does not need to be held low once a conversion is started. Pulling $\overline{CS}$ high prevents data from being clocked into the MAX148 and three-states DOUT, but it does not adversely affect an internal clock-mode conversion already in progress. When internal clock mode is selected, SSTRB does not go into a high-impedance state when $\overline{CS}$ goes high.

Figure 10 shows the SSTRB timing in internal clock mode. In this mode, data can be shifted in and out of the MAX148 at clock rates exceeding 2.0MHz, provided that the minimum acquisition time, t_{ACQ}, is kept above 1.5µs.

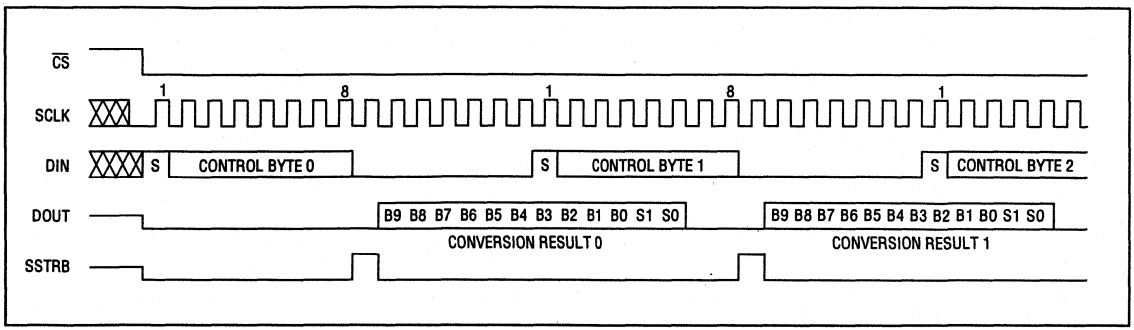


Figure 11a. External Clock Mode, 15 Clocks/Conversion Timing

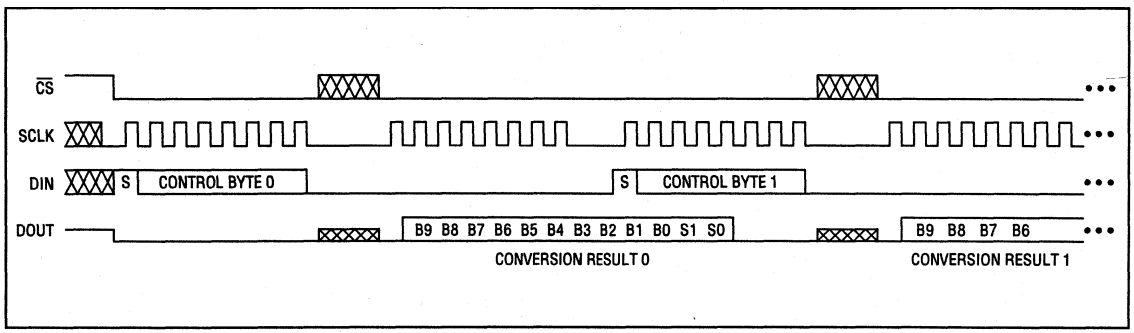


Figure 11b. External Clock Mode, 16 Clocks/Conversion Timing

Data Framing

The falling edge of $\overline{CS}$ does **not** start a conversion on the MAX148. The first logic high clocked into DIN is interpreted as a start bit and defines the first bit of the control byte. A conversion starts on the falling edge of SCLK, after the eighth bit of the control byte (the PD0 bit) is clocked into DIN. The start bit is defined as:

The first high bit clocked into DIN with $\overline{CS}$ low any time the converter is idle; e.g., after V_{DD} is applied.

OR

The first high bit clocked into DIN after bit 3 (B3) of a conversion in progress is clocked onto the DOUT pin.

If $\overline{CS}$ is toggled before the current conversion is complete, then the next high bit clocked into DIN is recognized as a start bit; the current conversion is terminated and a new one started.

The fastest the MAX148 can run is 15 clocks per conversion. Figure 11a shows the serial-interface timing necessary to perform a conversion every 15 SCLK cycles in external clock mode.

Most microcontrollers require that conversions occur in multiples of eight SCLK clocks; 16 clocks per conversion will typically be the fastest that a microcontroller can drive the MAX148. Figure 11b shows the serial-interface timing necessary to perform a conversion every 16 SCLK cycles in external clock mode.

+2.7V, Low-Power, 8-Channel, Serial 10-Bit ADC

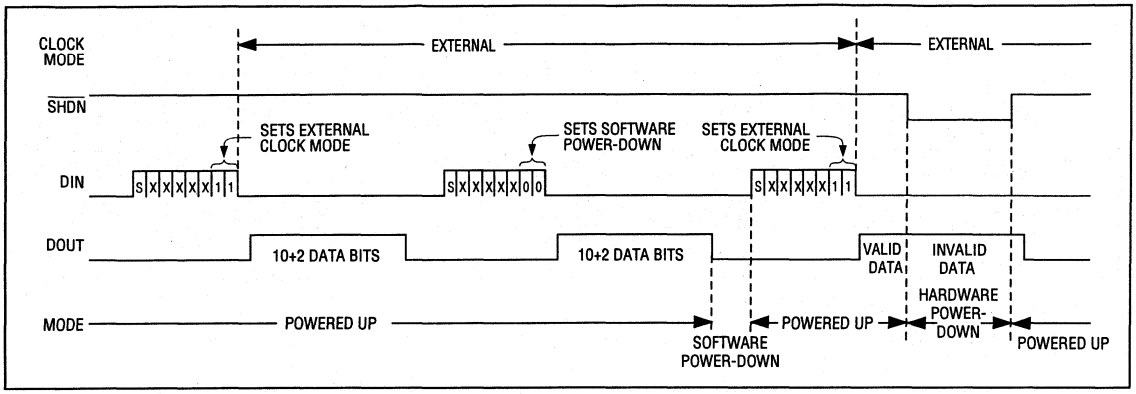


Figure 12a. Timing Diagram Power-Down Modes, External Clock

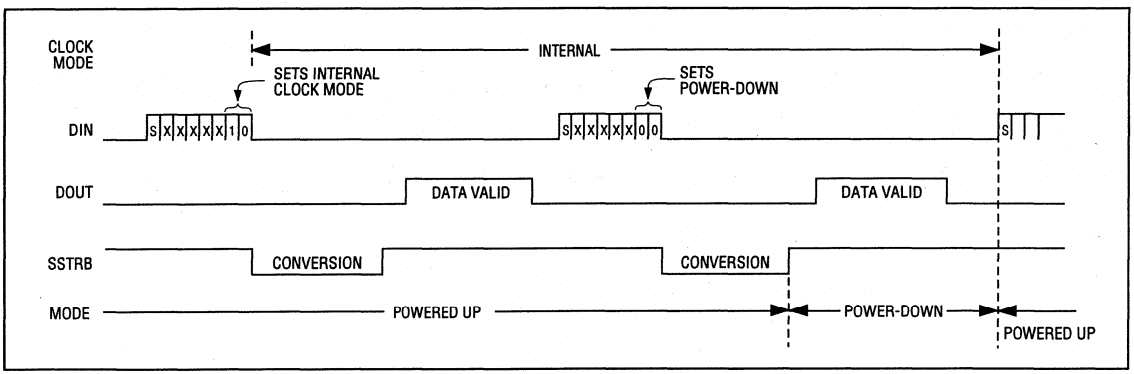


Figure 12b. Timing Diagram Power-Down Modes, Internal Clock

Applications Information

Power-On Reset

When power is first applied, and if $\overline{SHDN}$ is not pulled low, internal power-on reset circuitry will activate the MAX148 in internal clock mode, ready to convert with SSTRB = high. After the power supplies have been stabilized, the internal reset time is 10µs, and no conversions should be performed during this phase. SSTRB is high on power-up and, if $\overline{CS}$ is low, the first logical 1 on DIN will be interpreted as a start bit. Until a conversion takes place, DOUT will shift out zeros.

Power-Down

The MAX148's automatic power-down mode can save considerable power when operating at speeds below the maximum sampling rate.

Figure 13 shows the average supply current as a function of the sampling rate. You can save power by placing the converter in a low-current shutdown state between conversions.

Select power-down via bits 1 and 0 of the DIN control byte with $\overline{SHDN}$ high (Tables 1 and 4). Pull $\overline{SHDN}$ low at any time to shut down the converter completely. $\overline{SHDN}$ overrides bits 1 and 0 of the control byte (Table 6).

Power-down mode turns off all chip functions that draw quiescent current, reducing I_{DD} typically to 1.2µA.

Figures 12a and 12b illustrate the various power-down sequences in both external and internal clock modes.

Table 4. Software Power-Down and Clock Mode

PD1	PD0	DEVICE MODE
1	1	External Clock Mode
1	0	Internal Clock Mode
0	1	Unassigned
0	0	Power-Down Mode

Table 5. Hard-Wired Power-Down and Internal Clock Frequency

$\overline{SHDN}$ STATE	DEVICE MODE	INTERNAL CLOCK FREQUENCY
1	Enabled	225kHz
Floating	Enabled	1.8MHz
0	Power-Down	N/A

Table 6. Full Scale and Zero Scale

UNIPOLAR MODE		BIPOLAR MODE		
Full Scale	Zero Scale	Positive Full Scale	Zero Scale	Negative Full Scale
VREF + COM	COM	VREF/2 + COM	COM	-VREF/2 + COM

Software Power-Down

Software power-down is activated using bits PD1 and PD0 of the control byte. As shown in Table 6, PD1 and PD0 also specify the clock mode. When software shutdown is asserted, the ADC will continue to operate in the last specified clock mode until the conversion is complete. Then the ADC powers down into a low quiescent-current state. In internal clock mode, the interface remains active and conversion results may be clocked out after the MAX148 has entered a software power-down.

The first logical 1 on DIN will be interpreted as a start bit, and powers up the MAX148. Following the start bit, the data input word or control byte also determines clock mode and power-down states. For example, if the DIN word contains PD1 = 1, then the chip will remain powered up. If PD0 = PD1 = 0, a power-down will resume after one conversion.

Hardware Power-Down

Pulling $\overline{SHDN}$ low places the converter in hardware power-down. Unlike the software power-down mode, the conversion is not completed; it stops coincidentally with $\overline{SHDN}$ being brought low. $\overline{SHDN}$ also controls the clock frequency in internal clock mode. Letting $\overline{SHDN}$ float sets the internal clock frequency to 1.8MHz. When returning to normal operation with $\overline{SHDN}$ floating, there is a t_{RC} delay of approximately 2MΩ x C_L, where C_L is the capacitive loading on the $\overline{SHDN}$ pin. Pulling $\overline{SHDN}$ high sets the internal clock frequency to 225kHz. This feature eases the settling-time requirement for the reference voltage.

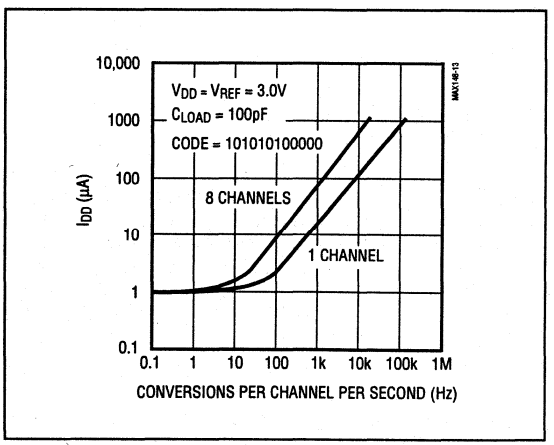


Figure 13. Average Supply Current vs. Conversions per Sample per Second in Power-Down

External Reference

An external reference is required for the MAX148. The reference voltage range is 1V to V_{DD}.

At VREF, the input impedance is a minimum of 18kΩ for DC currents. During a conversion, the reference must be able to deliver up to 250µA DC load current and have an output impedance of 10Ω or less. If the reference has higher output impedance or is noisy, bypass it close to the VREF pin with a 0.1µF capacitor.

+2.7V, Low-Power, 8-Channel, Serial 10-Bit ADC

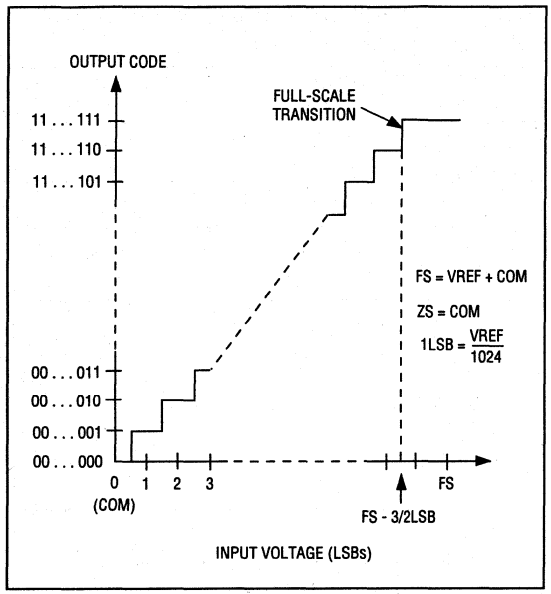


Figure 14. Unipolar Transfer Function, Full Scale (FS) = VREF + COM, Zero Scale (ZS) = COM

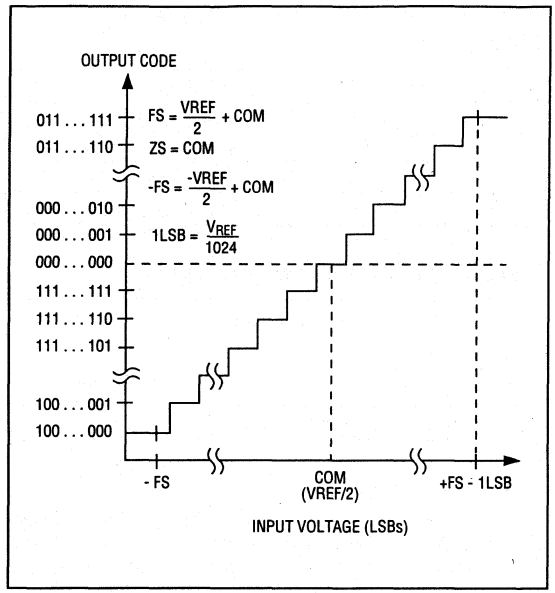


Figure 15. Bipolar Transfer Function, Full Scale (FS) = VREF/2 + COM , Zero Scale (ZS) = COM

Transfer Function

Table 6 shows the full-scale voltage ranges for unipolar and bipolar modes. The external reference must have a temperature coefficient of 20ppm/°C or less to achieve accuracy to within 1LSB over the commercial temperature range of 0°C to +70°C. See the MAX872 for a micropower 2.5V reference.

Figure 14 depicts the nominal, unipolar input/output (I/O) transfer function, and Figure 15 shows the bipolar input/output transfer function. Code transitions occur halfway between successive-integer LSB values. Output coding is binary, with 1LSB = 2.44mV (2.500V / 1024) for unipolar operation and 1LSB = 2.44mV [(2.500V / 2 - -2.500V / 2) / 1024] for bipolar operation.

Layout, Grounding, and Bypassing

For best performance, use printed circuit boards. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other.

Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

Figure 16 shows the recommended system ground connections. A single-point analog ground ("star" ground point) should be established at AGND, separate from the logic ground. Connect all other analog grounds and DGND to the star ground. No other digital system ground should be connected to this ground. The ground return to the power supply for the star ground should be low impedance and as short as possible for noise-free operation.

High-frequency noise in the V_{DD} power supply may affect the high-speed comparator in the ADC. Bypass the supply to the star ground with 0.1µF and 4.7µF capacitors close to pin 20 of the MAX148. Minimize capacitor lead lengths for best supply-noise rejection. If the +3V power supply is very noisy, a 10Ω resistor can be connected as a lowpass filter (Figure 16).

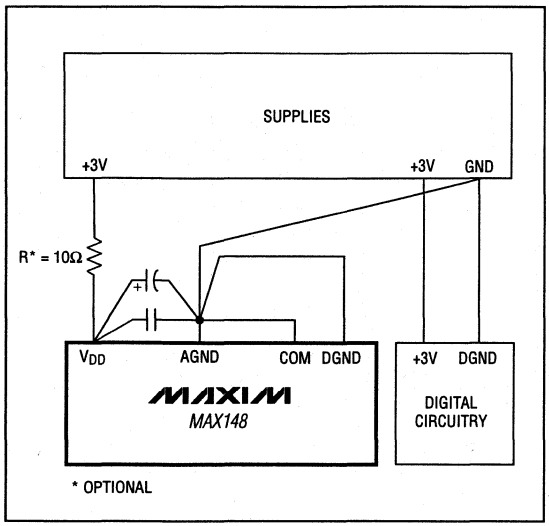


Figure 16. Power-Supply Grounding Connection

High-Speed Digital Interfacing with QSPI

The MAX148 can interface with QSPI using the circuit in Figure 17 (f_{SCLK} = 2.0MHz, C_{POL} = 0, C_{PHA} = 0). This QSPI circuit can be programmed to do a conversion on each of the eight channels. The result is stored in memory without taxing the CPU, since QSPI incorporates its own micro-sequencer.

Because the maximum external clock frequency is 2.0MHz, the MAX148 is QSPI compatible up to 2MHz.

TMS320LC3x-to-MAX148 Interface

Figure 18 shows an application circuit to interface the MAX148 to the TMS320 in external clock mode. The timing diagram for this interface circuit is shown in Figure 19.

Use the following steps to initiate a conversion in the MAX148 and to read the results:

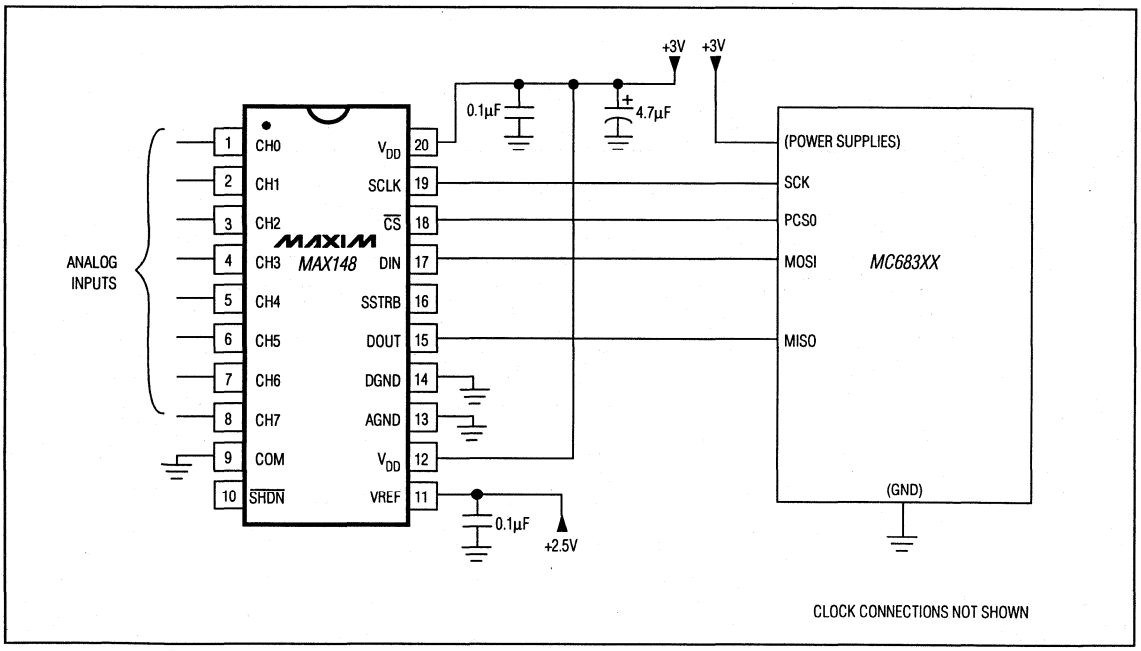


Figure 17. MAX148 QSPI Connections

7

+2.7V, Low-Power, 8-Channel, Serial 10-Bit ADC

1) The TMS320 should be configured with CLKX (transmit clock) as an active-high output clock and CLKR (TMS320 receive clock) as an active-high input clock. CLKX and CLKR on the TMS320 are tied together with the MAX148's SCLK input.
2) The MAX148's $\overline{CS}$ pin is driven low by the TMS320's XF_ I/O port, to enable data to be clocked into the MAX148's DIN.
3) An 8-bit word (1XXXXX11) should be written to the MAX148 to initiate a conversion and place the device into external clock mode. Refer to Table 1 to select the proper XXXXX bit values for your specific application.
4) The MAX148's SSTRB output is monitored via the TMS320's FSR input. A falling edge on the SSTRB output indicates that the conversion is in progress and data is ready to be received from the MAX148.
5) The TMS320 reads in one data bit on each of the next 16 rising edges of SCLK. These data bits represent the 10+2-bit conversion result followed by four trailing bits, which should be ignored.
6) Pull $\overline{CS}$ high to disable the MAX148 until the next conversion is initiated.

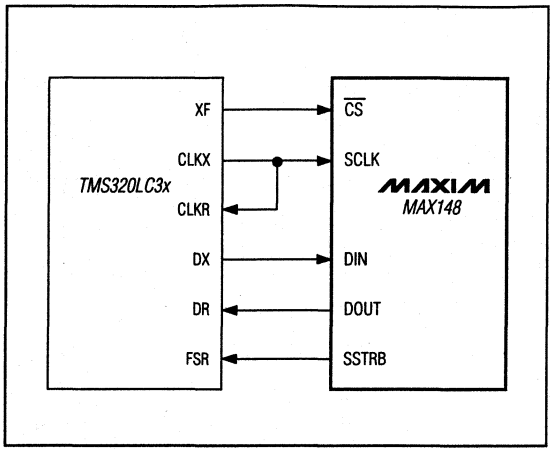


Figure 18. MAX148-to-TMS320 Serial Interface

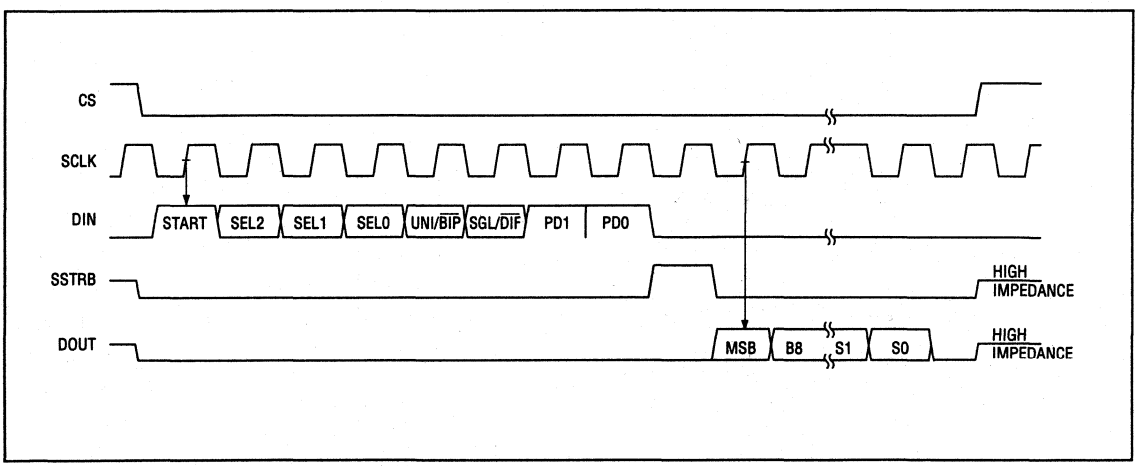


Figure 19. TMS320 Serial-Interface Timing Diagram

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX148AEPP	-40°C to +85°C	20 Plastic DIP	±1/2
MAX148BEPP	-40°C to +85°C	20 Plastic DIP	±1
MAX148AEAP	-40°C to +85°C	20 SSOP	±1/2
MAX148BEAP	-40°C to +85°C	20 SSOP	±1
MAX148AMJP	-55°C to +125°C	20 CERDIP**	±1/2
MAX148BMJP	-55°C to +125°C	20 CERDIP**	±1

** *Contact factory for availability.*

Chip Information

TRANSISTOR COUNT: 2554

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

10/96

MAXIM

+2.7V, Low-Power, 8-Channel, Serial 10-Bit ADC

General Description

The MAX149 is a 10-bit data-acquisition system that combines an 8-channel multiplexer, high-bandwidth track/hold, and serial interface with very low power consumption. The device operates from a single +2.7V to 3.6V supply. Its analog inputs are software configurable for unipolar/bipolar and single-ended/differential operation.

The 4-wire serial interface directly connects to SPI™, QSPI™, and Microwire™ devices without external logic. A serial strobe output allows direct connection to TMS320-family digital signal processors. The MAX149 uses either the internal clock or an external serial-interface clock to perform successive-approximation analog-to-digital conversions.

This device provides a hard-wired shutdown pin ($\overline{SHDN}$) and two software-selectable power-down modes. Accessing the serial interface automatically powers up the MAX149, and a quick turn-on time allows it to be shut down between conversions. Using this technique of powering down between conversions, supply current can be cut to under 10µA at reduced sampling rates.

The MAX149 has an internal 2.50V reference and a reference-buffer amplifier that simplifies gain trim. If an internal reference is not required, consider the pin-compatible MAX148. The MAX149 is available in 20-pin DIP packages, and in a 20-pin SSOP that occupies 30% less area than an 8-pin DIP.

Applications

Portable Data Logging

Data-Acquisition Systems

Pen-Entry Devices

Battery-Powered Instruments

Medical Instruments

Features

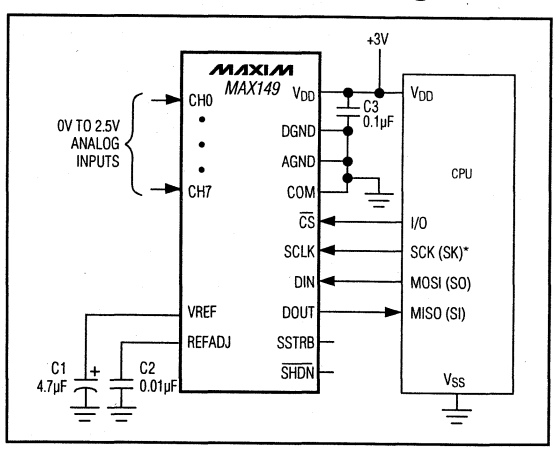
- ♦ **8 Single-Ended or 4 Differential Inputs**
- ♦ **Single +2.7V to +3.6V Operation**
- ♦ **Low Power: 1.5mA (operating mode)**
  2µA (power-down mode)
- ♦ **Internal Track/Hold, 133kHz Sampling Rate**
- ♦ **Internal 2.50V Reference**
- ♦ **SPI, QSPI, Microwire, TMS320-Compatible 4-Wire Serial Interface**
- ♦ **Software-Configurable Unipolar or Bipolar Inputs**
- ♦ **20-Pin DIP/SSOP Packages**

Ordering Information

PART†	TEMP. RANGE	PIN-PACKAGE
MAX149ACPP	0°C to +70°C	20 Plastic DIP
MAX149BCPP	0°C to +70°C	20 Plastic DIP
MAX149ACAP	0°C to +70°C	20 SSOP
MAX149BCAP	0°C to +70°C	20 SSOP
MAX149AEPP	-40°C to +85°C	20 Plastic DIP
MAX149BEPP	-40°C to +85°C	20 Plastic DIP
MAX149AEAP	-40°C to +85°C	20 SSOP
MAX149BEAP	-40°C to +85°C	20 SSOP
MAX149AMJP	-55°C to +125°C	20 CERDIP
MAX149BMJP	-55°C to +125°C	20 CERDIP

†*Contact factory for availability of SO package.*

Typical Operating Circuit

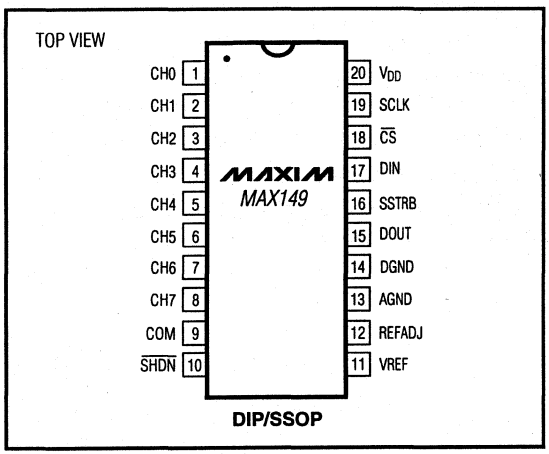


SPI and QSPI are registered trademarks of Motorola, Inc.
Microwire is a registered trademark of National Semiconductor Corp.

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+2.7V, Low-Power, 8-Channel, Serial 10-Bit ADC

Pin Configuration



19-0435; Rev 0; 9/95

EVALUATION KIT AVAILABLE

MAXIM

Multirange, Single +5V, 12-Bit DAS with 12-Bit Bus Interface

General Description

The MAX196/MAX198 multirange, 12-bit data-acquisition systems (DAS) require only a single +5V supply for operation, yet convert analog signals at their inputs up to ±10V (MAX196) and ±4V (MAX198). These systems provide six analog input channels that are independently software programmable for a variety of ranges: ±10V, ±5V, 0V to +10V, and 0V to +5V for the MAX196; ±V_{REF}, ±V_{REF}/2, 0V to +V_{REF}, and 0V to +V_{REF}/2 for the MAX198. This range switching increases the effective dynamic range to 14 bits and provides the flexibility to interface ±12V, ±15V, and 4mA to 20mA powered sensors to a single +5V system. In addition, these converters are fault protected to ±16.5V; a fault condition on any channel will **not** affect the conversion result of the selected channel. Other features include a 5MHz bandwidth track/hold, 100ksps throughput rate, software-selectable internal/external clock, internal/external acquisition control, 12-bit parallel interface, and internal 4.096V or external reference.

Two programmable power-down modes (STBYPD, FULLPD) provide low-current shutdown between conversions. In STBYPD mode, the reference buffer remains active, eliminating start-up delays.

The MAX196/MAX198 employ a standard microprocessor (µP) interface. A three-state data I/O port is configured to operate with 16-bit data buses, and data-access and bus-release timing specifications are compatible with most popular µPs. All logic inputs and outputs are TTL/CMOS compatible.

These devices are available in 28-pin DIP, wide SO, SSOP (55% smaller in area than wide SO), and ceramic SB packages. For 8+4 bus interface, see the MAX197 and the MAX199 data sheets. An evaluation kit will be available after December 1995 (MAX196EVKIT-DIP).

Applications

Industrial-Control Systems
Robotics
Data-Acquisition Systems
Automatic Testing Systems
Medical Instruments
Telecommunications

Functional Diagram appears at end of data sheet.

Features

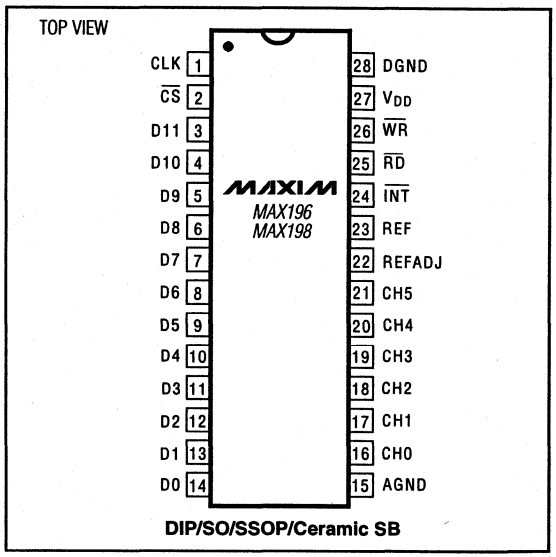
- **12-Bit Resolution, 1/2LSB Linearity**
- **Single +5V Supply Operation**
- **Software-Selectable Input Ranges: ±10V, ±5V, 0V to +10V, 0V to +5V (MAX196) ±V_{REF}, ±V_{REF}/2, 0V to +V_{REF}, 0V to +V_{REF}/2 (MAX198)**
- **Internal 4.096V or External Reference**
- **Fault-Protected Input Multiplexer**
- **6 Analog Input Channels**
- **6µs Conversion Time, 100ksps Sampling Rate**
- **Internal or External Acquisition Control**
- **Two Power-Down Modes**
- **Internal or External Clock**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX196ACNI	0°C to +70°C	28 Narrow Plastic DIP
MAX196BCNI	0°C to +70°C	28 Narrow Plastic DIP
MAX196ACWI	0°C to +70°C	28 Wide SO
MAX196BCWI	0°C to +70°C	28 Wide SO
MAX196ACAI	0°C to +70°C	28 SSOP
MAX196BCAI	0°C to +70°C	28 SSOP

Ordering Information continued at end of data sheet.

Pin Configuration



DIP/SO/SSOP/Ceramic SB

7

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Multirange, Single +5V, 12-Bit DAS with 12-Bit Bus Interface

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND .....-0.3V to +7V
AGND to DGND .....-0.3V to +0.3V
REF to AGND .....-0.3V to (V_{DD} + 0.3V)
REFADJ to AGND .....-0.3V to (V_{DD} + 0.3V)
Digital Inputs to DGND .....-0.3V to (V_{DD} + 0.3V)
Digital Outputs to DGND .....-0.3V to (V_{DD} + 0.3V)
CH0–CH5 to AGND .....±16.5V
Continuous Power Dissipation (T_A = +70°C)
Narrow Plastic DIP (derate 14.29mW/°C above +70°C) 1143mW
Wide SO (derate 12.50mW/°C above +70°C).....1000mW
SSOP (derate 9.52mW/°C above +70°C) 762mW
Narrow Ceramic SB (derate 20.00mW/°C above +70°C)..1600mW
Operating Temperature Ranges
MAX196_C_ I/MAX198_C_ I .....0°C to +70°C
MAX196_E_ I/MAX198_E_ I .....-40°C to +85°C
MAX196_MYI/MAX198_MYI.....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ±5%; unipolar/bipolar range; external reference mode, V_{REF} = 4.096V; 4.7µF at REF pin; external clock, f_{CLK} = 2.0MHz with 50% duty cycle; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY (Note 1)							
Resolution				12			Bits
Integral Nonlinearity	INL	MAX196A/MAX198A				±1/2	LSB
		MAX196B/MAX198B				±1	
Differential Nonlinearity	DNL					±1	LSB
Offset Error		Unipolar	MAX196A/MAX198A			±3	LSB
			MAX196B/MAX198B			±5	
		Bipolar	MAX196A/MAX198A			±5	
			MAX196B/MAX198B			±10	
Channel-to-Channel Offset Error Matching		Unipolar			±0.1		LSB
		Bipolar			±0.5		
Gain Error (Note 2)		Unipolar	MAX196A/MAX198A			±7	LSB
			MAX196B/MAX198B			±10	
		Bipolar	MAX196A/MAX198A			±7	
			MAX196B/MAX198B			±10	
Gain Temperature Coefficient (Note 2)		Unipolar			3		ppm/°C
		Bipolar			5		
DYNAMIC SPECIFICATIONS (10kHz sine-wave input, ±10Vp-p (MAX196) or ±4.096Vp-p (MAX198), f_{SAMPLE} = 100ksps)							
Signal-to-Noise + Distortion Ratio	SINAD	MAX196A/MAX198A		70			dB
		MAX196B/MAX198B		69			
Total Harmonic Distortion	THD	Up to the 5th harmonic			-85	-78	dB
Spurious-Free Dynamic Range	SFDR			80			dB
Channel-to-Channel Crosstalk		50kHz, V_{IN} = ±5V (MAX196) or ±4V (MAX198) (Note 3)			-86		dB
Aperture Delay		External CLK mode/external acquisition control			15		ns
Aperture Jitter		External CLK mode/external acquisition control			<50		ps
		Internal CLK mode/internal acquisition control (Note 4)			10		ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V ±5%; unipolar/bipolar range; external reference mode, V_{REF} = 4.096V; 4.7µF at REF pin; external clock, f_{CLK} = 2.0MHz with 50% duty cycle; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
ANALOG INPUT								
Track/Hold Acquisition Time		f_{CLK} = 2.0MHz					3	µs
Small-Signal Bandwidth		-3dB rolloff	±10V or ±V_{REF} range			5		MHz
			±5V or ±V_{REF}/2 range			2.5		
			0V to 10V or 0V to V_{REF} range			2.5		
			0V to 5V or 0V to V_{REF}/2 range			1.25		
Input Voltage Range (see Table 3)	V_{IN}	Unipolar	MAX196		0		10	V
					0		5	
			MAX198		0		V_{REF}	
					0		V_{REF}/2	
		Bipolar	MAX196		-10		10	
					-5		5	
			MAX198		-V_{REF}		V_{REF}	
					-V_{REF}/2		V_{REF}/2	
Input Current	I_{IN}	Unipolar	MAX196	0V to 10V range			720	µA
				0V to 5V range			360	
			MAX198			0.1	10	
		Bipolar	MAX196	±10V range	-1200		720	
				±5V range	-600		360	
			MAX198	±V_{REF} range	-1200		10	
				±V_{REF}/2 range	-600		10	
Input Resistance	$\frac{\Delta V_{IN}}{\Delta I_{IN}}$	Unipolar				21		kΩ
		Bipolar				16		
Input Capacitance		(Note 5)					40	pF
INTERNAL REFERENCE								
REF Output Voltage	V_{REF}	T_A = +25°C			4.076	4.096	4.116	V
REF Output Tempco (Contact Maxim Applications for guaranteed temperature drift specifications)	TC V_{REF}	MAX196_C/MAX198_C				15		ppm/°C
		MAX196_E/MAX198_E				30		
		MAX196_M/MAX198_M				40		
Output Short-Circuit Current							30	mA
Load Regulation		0mA to 0.5mA output current (Note 6)					10	mV
Capacitive Bypass at REF					4.7			µF
REFADJ Output Voltage					2.465	2.500	2.535	V
REFADJ Adjustment Range		With recommended circuit (Figure 1)				±1.5		%
Buffer Voltage Gain						1.6384		V/V

Multirange, Single +5V, 12-Bit DAS with 12-Bit Bus Interface

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V ±5%; unipolar/bipolar range; external reference mode, V_{REF} = 4.096V; 4.7µF at REF pin; external clock, f_{CLK} = 2.0MHz with 50% duty cycle; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REFERENCE INPUT (buffer disabled, reference input applied to REF pin)							
Input Voltage Range				2.4		4.18	V
Input Current		V_{REF} = 4.18V	Normal, or STANDBY power-down mode			400	µA
			FULL power-down mode			1	
Input Resistance		Normal, or STANDBY power-down mode		10			kΩ
		FULL power-down mode		5			MΩ
REFADJ Threshold for Buffer Disable				V_{DD} - 50mV			V
POWER REQUIREMENTS							
Supply Voltage	V_{DD}			4.75		5.25	V
Supply Current	I_{DD}	Normal mode, bipolar ranges				18	mA
		Normal mode, unipolar ranges			6	10	
		STANDBY power-down mode			700	850	µA
		FULL power-down mode (Note 7)			60	120	
Power-Supply Rejection Ratio (Note 8)	PSRR	External reference = 4.096V			±0.1	±1/2	LSB
		Internal reference			±1/2		
TIMING							
Internal Clock Frequency	f_{CLK}	C_{CLK} = 100pF		1.25	1.56	2.00	MHz
External Clock Frequency Range	f_{CLK}			0.1		2.0	MHz
Acquisition Time	t_{ACQI}	Internal acquisition	External CLK	3.0			µs
			Internal CLK	3.0		5.0	
	t_{ACQE}	External acquisition (Note 9)		3.0			
		After FULLPD or STBYPD			5		
Conversion Time	t_{CONV}	External CLK		6.0			µs
		Internal CLK, C_{CLK} = 100pF		6.0	7.7	10.0	
Throughput Rate		External CLK				100	ksps
		Internal CLK, C_{CLK} = 100pF		62			
Bandgap Reference Start-Up Time		Power-up (Note 10)			200		µs
Reference Buffer Settling		To 0.1mV REF bypass capacitor fully discharged	C_{REF} = 4.7µF		8		ms
			C_{REF} = 33µF		60		
DIGITAL INPUTS (D7–D0, CLK, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$) (Note 11)							
Input High Voltage	V_{INH}			2.4			V
Input Low Voltage	V_{INL}					0.8	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}				±10	µA
Input Capacitance	C_{IN}	(Note 5)				15	pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V ±5%; unipolar/bipolar range; external reference mode, V_{REF} = 4.096V; 4.7µF at REF pin; external clock, f_{CLK} = 2.0MHz with 50% duty cycle; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL OUTPUTS (D11–D0, $\overline{INT}$)						
Output Low Voltage	V_{OL}	V_{DD} = 4.75V, I_{SINK} = 1.6mA			0.4	V
Output High Voltage	V_{OH}	V_{DD} = 4.75V, I_{SOURCE} = 1mA	V_{DD} - 1			V
Three-State Output Capacitance	C_{OUT}	(Note 5)			15	pF

TIMING CHARACTERISTICS

(V_{DD} = 5V ±5%; unipolar/bipolar range; external reference mode, V_{REF} = 4.096V; 4.7µF at REF pin; external clock, f_{CLK} = 2.0MHz with 50% duty cycle; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CS}$ Pulse Width	t_{CS}		80			ns
$\overline{WR}$ Pulse Width	t_{WR}		80			ns
$\overline{CS}$ to $\overline{WR}$ Setup Time	t_{CSWS}		0			ns
$\overline{CS}$ to $\overline{WR}$ Hold Time	t_{CSWH}		0			ns
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_{CSRS}		0			ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_{CSRH}		0			ns
CLK to $\overline{WR}$ Setup Time	t_{CWS}				100	ns
CLK to $\overline{WR}$ Hold Time	t_{CWH}				50	ns
Data Valid to $\overline{WR}$ Setup	t_{DS}		60			ns
Data Valid to $\overline{WR}$ Hold	t_{DH}		0			ns
$\overline{RD}$ Low to Output Data Valid	t_{DO}	Figure 2, C_L = 100pF (Note 12)			120	ns
$\overline{RD}$ High to Output Disable	t_{TR}	(Note 13)			70	ns
$\overline{RD}$ Low to $\overline{INT}$ High Delay	t_{INT1}				120	ns

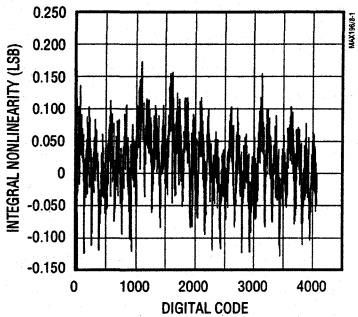
Note 1: Accuracy specifications tested at V_{DD} = 5.0V. Performance at power-supply tolerance limits guaranteed by Power-Supply Rejection test. Tested for the ±10V (MAX196) and ±4.096V (MAX198) input ranges.
Note 2: External reference: V_{REF} = 4.096V, offset error nulled, ideal last code transition = FS - 3/2LSB.
Note 3: Ground "on" channel; sine wave applied to all "off" channels.
Note 4: Maximum full-power input frequency for 1LSB error with 10ns jitter = 3kHz.
Note 5: Guaranteed by design. Not tested.
Note 6: Use static loads only.
Note 7: Tested using internal reference.
Note 8: PSRR measured at full-scale.
Note 9: External acquisition timing: starts at data valid at ACQMOD = low control byte; ends at rising edge of $\overline{WR}$ with ACQMOD = high control byte.
Note 10: Not subject to production testing. Provided for design guidance only.
Note 11: All input control signals specified with t_R = t_F = 5ns from a voltage level of 0.8V to 2.4V.
Note 12: t_{DO} is measured with the load circuits of Figure 2 and defined as the time required for an output to cross 0.8V or 2.4V.
Note 13: t_{TR} is defined as the time required for the data lines to change by 0.5V.

Multirange, Single +5V, 12-Bit DAS with 12-Bit Bus Interface

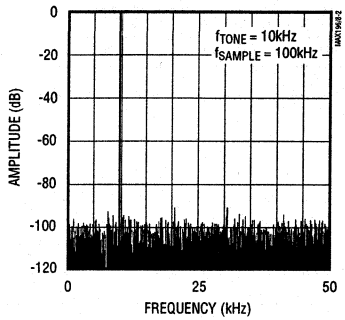
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

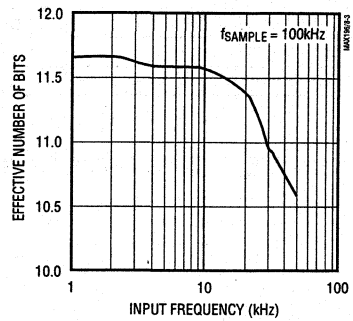
INTEGRAL NONLINEARITY vs. DIGITAL CODE



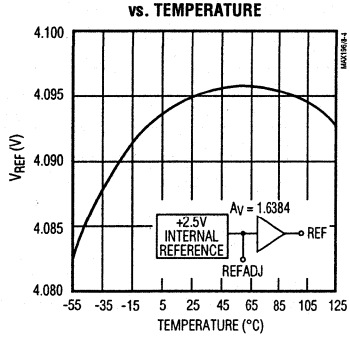
FFT PLOT



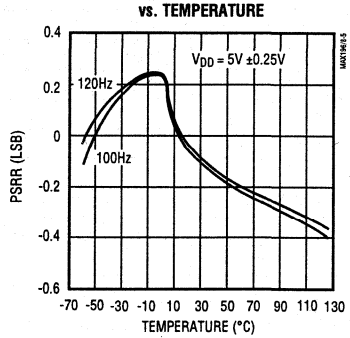
EFFECTIVE NUMBER OF BITS vs. INPUT FREQUENCY



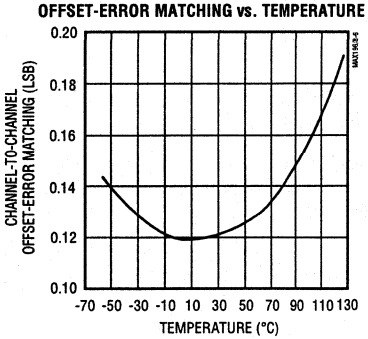
REFERENCE OUTPUT VOLTAGE (V_{REF}) vs. TEMPERATURE



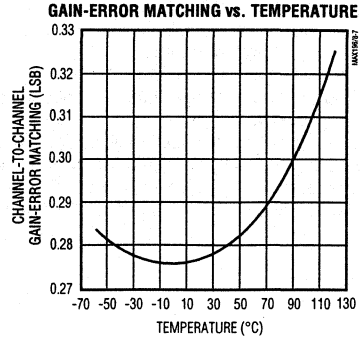
POWER-SUPPLY REJECTION RATIO vs. TEMPERATURE



CHANNEL-TO-CHANNEL OFFSET-ERROR MATCHING vs. TEMPERATURE



CHANNEL-TO-CHANNEL GAIN-ERROR MATCHING vs. TEMPERATURE



Multirange, Single +5V, 12-Bit DAS with 12-Bit Bus Interface

Pin Description

PIN	NAME	FUNCTION
1	CLK	Clock Input. In external clock mode, drive CLK with a TTL/CMOS-compatible clock. In internal clock mode, place a capacitor (C_{CLK}) from this pin to ground to set the internal clock frequency; f_{CLK} = 1.56MHz typical with C_{CLK} = 100pF.
2	$\overline{CS}$	Chip Select, active low
3–14	D11–D0	Three-State Digital I/O, D11 = MSB
15	AGND	Analog Ground
16–21	CH0–CH5	Analog Input Channels
22	REFADJ	Bandgap Voltage-Reference Output/External Adjust Pin. Bypass with a 0.01µF capacitor to AGND. Connect to V_{DD} when using an external reference at the REF pin.
23	REF	Reference Buffer Output/ADC Reference Input. In internal reference mode, the reference buffer provides a 4.096V nominal output, externally adjustable at REFADJ. In external reference mode, disable the internal buffer by pulling REFADJ to V_{DD}.
24	$\overline{INT}$	$\overline{INT}$ goes low when conversion is complete and output data is ready.
25	$\overline{RD}$	If $\overline{CS}$ is low, a falling edge on $\overline{RD}$ will enable a read operation on the data bus.
26	$\overline{WR}$	In the internal acquisition mode, when $\overline{CS}$ is low, a rising edge on $\overline{WR}$ latches in configuration data and starts an acquisition plus a conversion cycle. In the external acquisition mode, when $\overline{CS}$ is low, the first rising edge on $\overline{WR}$ starts an acquisition, and a second rising edge on $\overline{WR}$ ends acquisition and starts a conversion cycle.
27	V_{DD}	+5V Supply. Bypass with 0.1µF capacitor to AGND.
28	DGND	Digital Ground

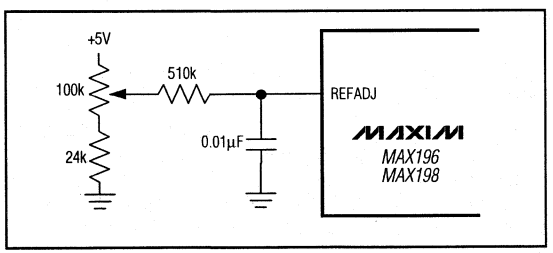


Figure 1. Reference-Adjust Circuit

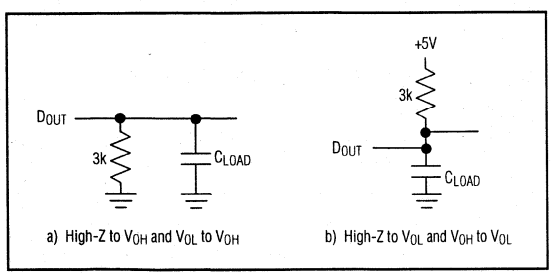


Figure 2. Load Circuits for Enable Time

Detailed Description

Converter Operation

The MAX196/MAX198 multirange, fault-tolerant ADCs use successive approximation and internal input track/hold (T/H) circuitry to convert an analog signal to a 12-bit digital output. The 12-bit parallel-output format provides easy interface to microprocessors (µPs). Figure 3 shows the MAX196/MAX198 in the simplest operational configuration.

Analog-Input Track/Hold

In the internal acquisition control mode (control bit D5 set to 0), the T/H enters its tracking mode on $\overline{WR}$'s rising edge, and enters its hold mode when the internally timed (6 clock cycles) acquisition interval ends. In bipolar mode and unipolar mode (MAX196 only), a low-impedance input source, which settles in less than 1.5µs, is required to maintain conversion accuracy at the maximum conversion rate.

When the MAX198 is configured for unipolar mode, the input does not need to be driven from a low-impedance source. The acquisition time (t_{AZ}) is a function of the source output resistance (R_S), the channel input resistance (R_{IN}), and the T/H capacitance.

Multirange, Single +5V, 12-Bit DAS with 12-Bit Bus Interface

Acquisition time is calculated as follows:

For 0V to V_{REF}: $t_{AZ} = 9 \times (R_S + R_{IN}) \times 16pF$

For 0V to $V_{REF}/2$: $t_{AZ} = 9 \times (R_S + R_{IN}) \times 32pF$

where R_{IN} = 7kΩ and t_{AZ} is never less than 2µs (0V to V_{REF} range) or 3µs (0V to $V_{REF}/2$ range).

In the external acquisition control mode (D5 = 1), the T/H enters its tracking mode on the first $\overline{WR}$ rising edge and enters its hold mode when it detects the second $\overline{WR}$ rising edge with D5 = 0 (see *External Acquisition* section).

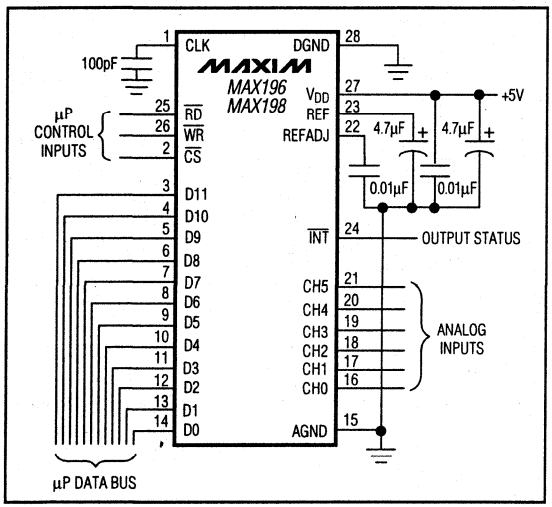


Figure 3. Operational Diagram

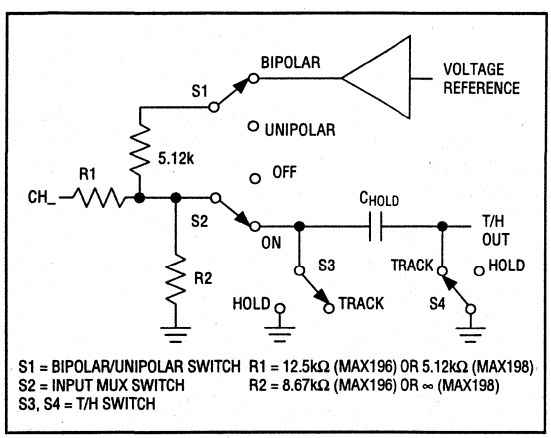


Figure 4. Equivalent Input Circuit

Input Bandwidth

The ADC's input tracking circuitry has a 5MHz small-signal bandwidth. When using the internal acquisition mode with an external clock frequency of 2MHz, a 100ksps throughput rate can be achieved. It is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended (MAX274/MAX275 continuous-time filters).

Input Range and Protection

Figure 4 shows the equivalent input circuit. The full-scale input voltage depends on the voltage at the reference (V_{REF}). The MAX196 uses a scaling factor, which allows input voltage ranges of ±10V, ±5V, 0V to +10V, or 0V to +5V with a 4.096V voltage reference (Table 1). Program the desired range by setting the appropriate control bits (D3, D4) in the control byte (Tables 2 and 3). The MAX198 does not use a scaling factor, so its input voltage range directly corresponds with the reference voltage. It can be programmed for input voltages of ±V_{REF}, ±$V_{REF}/2$, 0V to V_{REF}, or 0V to $V_{REF}/2$ (Table 3). When an external reference is applied at REFADJ, the voltage at REF is given by $V_{REF} = 1.6384 \times V_{REFADJ}$ ($2.4V < V_{REF} < 4.18V$).

The input channels are overvoltage protected to ±16.5V. This protection is active even if the device is in power-down mode.

Even with V_{DD} = 0V, the input resistive network provides current-limiting that adequately protects the device.

Digital Interface

Input data (control byte) and output data are multiplexed on a three-state parallel interface. This parallel I/O can easily be interfaced with a µP. $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ control the write and read operations. $\overline{CS}$ is the standard chip-select signal, which enables a µP to address the MAX196/MAX198 as an I/O port. When high, it disables the $\overline{WR}$ and $\overline{RD}$ inputs and forces the interface into a high-Z state.

Table 1. Full Scale and Zero Scale (MAX196 only)

RANGE (V)	ZERO SCALE (V)	-FULL SCALE	+FULL SCALE
0 to +5	0	—	V_{REF} x 1.2207
0 to +10	0	—	V_{REF} x 2.4414
±5	—	-V_{REF} x 1.2207	V_{REF} x 1.2207
±10	—	-V_{REF} x 2.4414	V_{REF} x 2.4414

Table 2. Control-Byte Format

D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
PD1	PD0	ACQMOD	RNG	BIP	A2	A1	A0

BIT	NAME	DESCRIPTION
7, 6	PD1, PD0	These two bits select the clock and power-down modes (Table 4).
5	ACQMOD	0 = internally controlled acquisition (6 clock cycles), 1 = externally controlled acquisition
4	RNG	Selects the full-scale voltage magnitude at the input (Table 3).
3	BIP	Selects unipolar or bipolar conversion mode (Table 3).
2, 1, 0	A2, A1, A0	These are address bits for the input mux to select the "on" channel (Table 5).

Table 3. Range and Polarity Selection

BIP	RNG	INPUT RANGE (V) (MAX196)	INPUT RANGE (V) (MAX198)
0	0	0 to 5	0 to $V_{REF}/2$
0	1	0 to 10	0 to V_{REF}
1	0	±5	$\pm V_{REF}/2$
1	1	±10	$\pm V_{REF}$

Table 4. Clock and Power-Down Selection

PD1	PD0	DEVICE MODE
0	0	Normal Operation / External Clock Mode
0	1	Normal Operation / Internal Clock Mode
1	0	Standby Power-Down (STBYPD); clock mode is unaffected
1	1	Full Power-Down (FULLPD); clock mode is unaffected

Table 5. Channel Selection

A2	A1	A0	CH0	CH1	CH2	CH3	CH4	CH5
0	0	0	*					
0	0	1		*				
0	1	0			*			
0	1	1				*		
1	0	0					*	
1	0	1						*

Multirange, Single +5V, 12-Bit DAS with 12-Bit Bus Interface

Input Format

The control byte is latched into the device, on pins D7–D0, during a write cycle. Table 2 shows the control-byte format.

Output Data Format

The output data format is binary in unipolar mode and twos-complement binary in bipolar mode. When reading the output data, $\overline{CS}$ and $\overline{RD}$ must be low.

How to Start a Conversion

Conversions are initiated with a write operation, which selects the mux channel and configures the MAX196/MAX198 for either a unipolar or bipolar input range. A write pulse ($\overline{WR}$ + $\overline{CS}$) can either start an acquisition interval or initiate a combined acquisition plus conversion. The sampling interval occurs at the end of the acquisition interval. The ACQMOD bit in the input control byte offers two options for acquiring the signal: internal or external. The conversion period lasts for 12 clock cycles in either internal or external clock or acquisition mode.

Writing a new control byte during a conversion cycle will abort the conversion and start a new acquisition interval.

Internal Acquisition

Select internal acquisition by writing the control byte with the ACQMOD bit cleared (ACQMOD = 0). This causes the write pulse to initiate an acquisition interval whose duration is internally timed. Conversion starts when this six-clock-cycle acquisition interval (3µs with f_{CLK} = 2MHz) ends (see Figure 5).

External Acquisition

Use the external acquisition timing mode for precise control of the sampling aperture and/or independent control of acquisition and conversion times. The user controls acquisition and start-of-conversion with two separate write pulses. The first pulse, written with ACQMOD = 1, starts an acquisition interval of indeterminate length. The second write pulse, written with ACQMOD = 0, terminates acquisition and starts conversion on $\overline{WR}$'s rising edge (Figure 6). However, if the second control byte contains ACQMOD = 1, an indefinite acquisition interval is restarted.

The address bits for the input mux must have the same values on the first and second write pulses. Power-down mode bits (PD0, PD1) can assume new values on the second write pulse (see *Power-Down Mode* section).

How to Read a Conversion

A standard interrupt signal, $\overline{INT}$, is provided to allow the device to flag the µP when the conversion has ended and a valid result is available. $\overline{INT}$ goes low when conversion is complete and the output data is ready (Figures 5 and 6). It returns high on the first read cycle or if a new control byte is written.

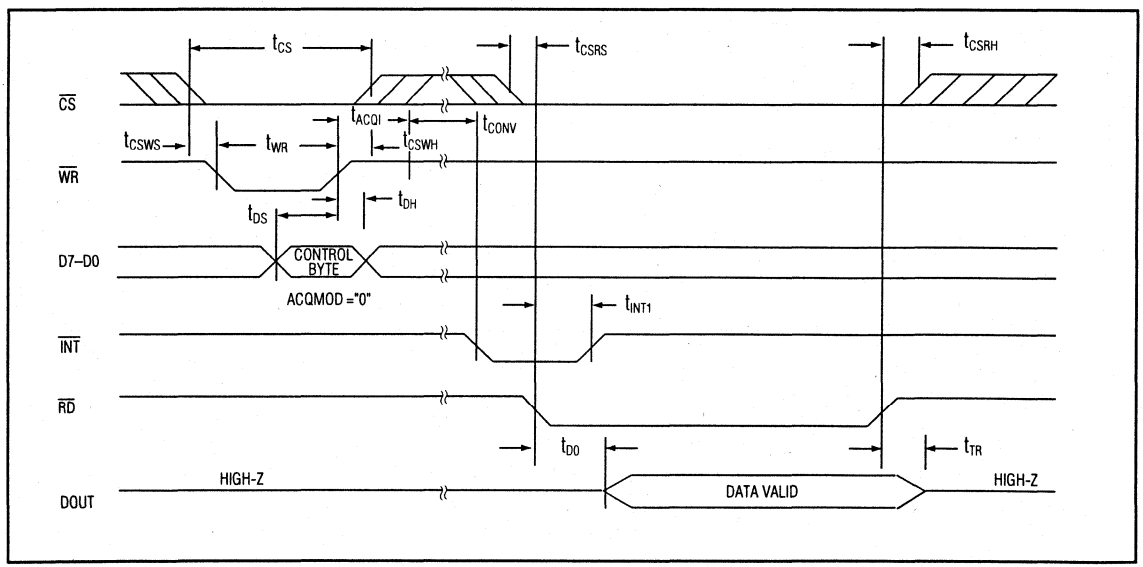


Figure 5. Conversion Timing Using Internal Acquisition Mode

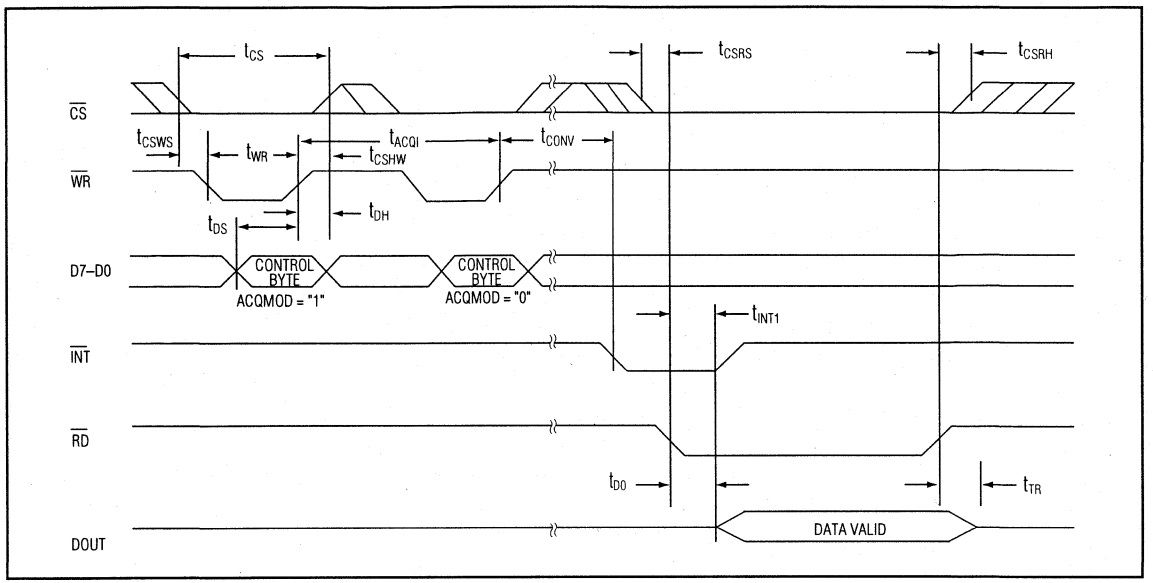


Figure 6. Conversion Timing Using External Acquisition Mode

Clock Modes

The MAX196/MAX198 operate with either an internal or an external clock. Control bits (D6, D7) select either internal or external clock mode. Once the desired clock mode is selected, changing these bits to program power-down will not affect the clock mode. In each mode, internal or external acquisition can be used. At power-up, external clock mode is selected.

Internal Clock Mode

Select internal clock mode to free the µP from the burden of running the SAR conversion clock. To select this mode, write the control byte with D7 = 0 and D6 = 1. A 100pF capacitor between the CLK pin and ground sets this frequency to 1.56MHz nominal. Figure 7 shows a linear relationship between the internal clock period and the value of the external capacitor used.

External Clock Mode

Select external clock mode by writing the control byte with D7 = 0 and D6 = 0. Figure 8 shows CLK and $\overline{WR}$ timing relationships in internal and external acquisition modes, with an external clock. A 100kHz to 2.0MHz external clock with 45% to 55% duty cycle is required for proper operation. Operating at clock frequencies lower than 100kHz will cause a voltage droop across the hold capacitor, and subsequently degrade performance.

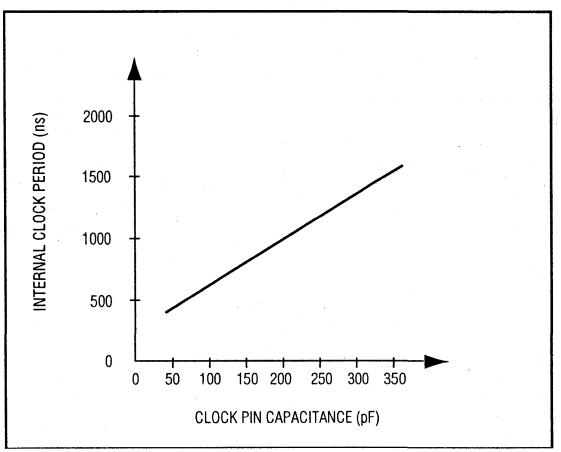


Figure 7. Internal Clock Period vs. Clock Pin Capacitance

Multirange, Single +5V, 12-Bit DAS with 12-Bit Bus Interface

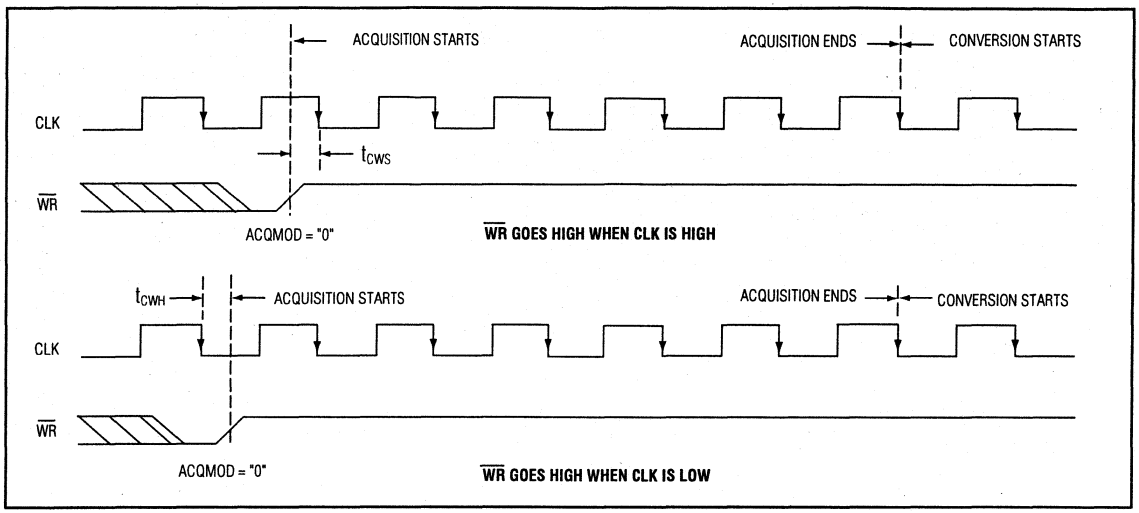


Figure 8a. External Clock and $\overline{WR}$ Timing (Internal Acquisition Mode)

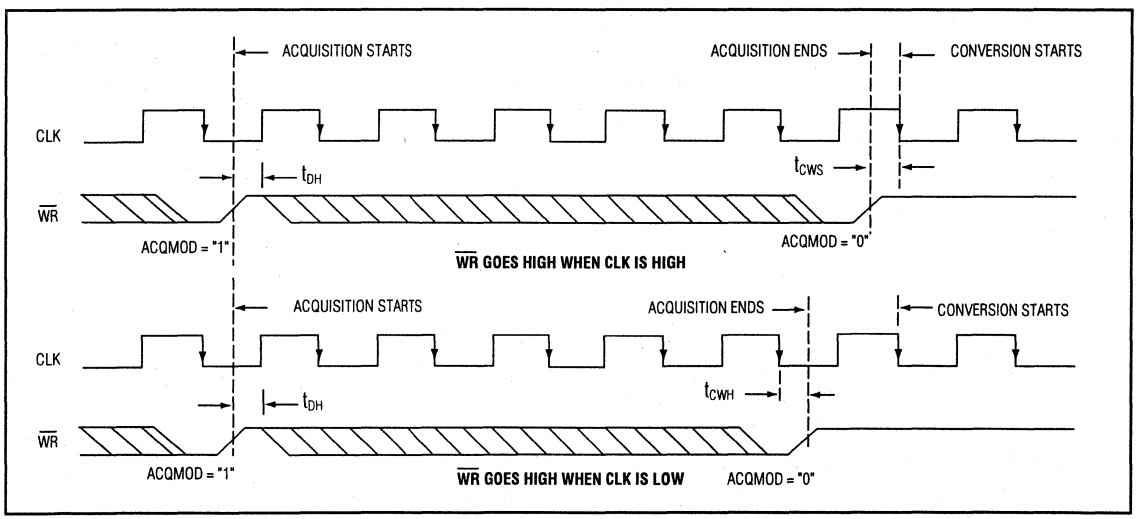


Figure 8b. External Clock and $\overline{WR}$ Timing (External Acquisition Mode)

Applications Information

Power-On Reset

At power-up, the internal power-on reset circuitry sets $\overline{INT}$ high and puts the device in normal operation/external clock mode. This state is selected to keep the internal clock from loading the external clock driver when the part is used in external clock mode.

Internal or External Reference

The MAX196/MAX198 can operate with either an internal or external reference. An external reference can be connected to either the REF pin or the REFADJ pin (Figure 9).

To use the REF input directly, disable the internal buffer by tying REFADJ to V_{DD}. Using the REFADJ input eliminates the need to buffer the reference externally. When the reference is applied at REFADJ, bypass REFADJ with a 0.01µF capacitor to AGND.

The REFADJ internal buffer gain is trimmed to 1.6384 to provide 4.096V at the REF pin from a 2.5V reference.

Internal Reference

The internally trimmed 2.50V reference is gained through the REFADJ buffer to provide 4.096V at REF. Bypass the REF pin with a 4.7µF capacitor to AGND and the REFADJ pin with a 0.01µF capacitor to AGND. The internal reference voltage is adjustable to ±1.5% (±65 LSBs) with the reference-adjust circuit of Figure 1.

External Reference

At REF and REFADJ, the input impedance is a minimum of 10kΩ for DC currents. During conversions, an external reference at REF must be able to deliver 400µA DC load currents, and must have an output impedance of 10Ω or less. If the reference has higher output impedance or is noisy, bypass it close to the REF pin with a 4.7µF capacitor to AGND.

With an external reference voltage of less than 4.096V at the REF pin or less than 2.5V at the REFADJ pin, the increase in the ratio of the RMS noise to the LSB value (FS / 4096) results in performance degradation (loss of effective bits).

Power-Down Mode

To save power, you can put the converter into low-current shutdown mode between conversions. Two programmable power-down modes are available: STBYPD and FULLPD. Select STBYPD or FULLPD by programming PD0 and PD1 in the input control byte. When power-down is asserted, it becomes effective only after the end of conversion. In all power-down modes, the interface remains active and conversion

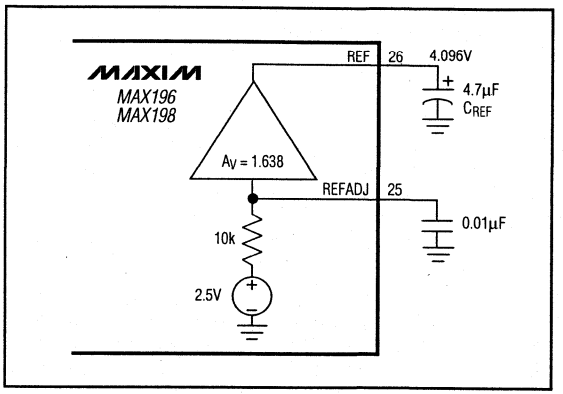


Figure 9a. Internal Reference

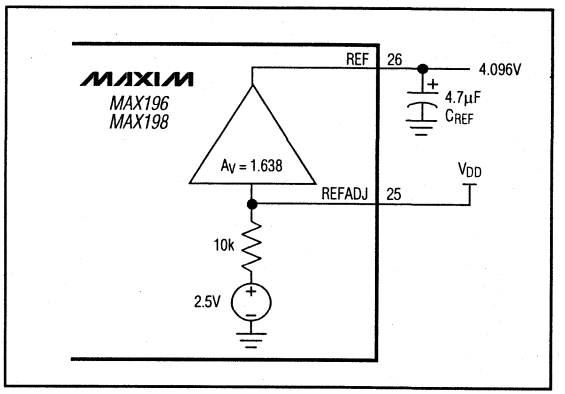


Figure 9b. External Reference, Reference at REF

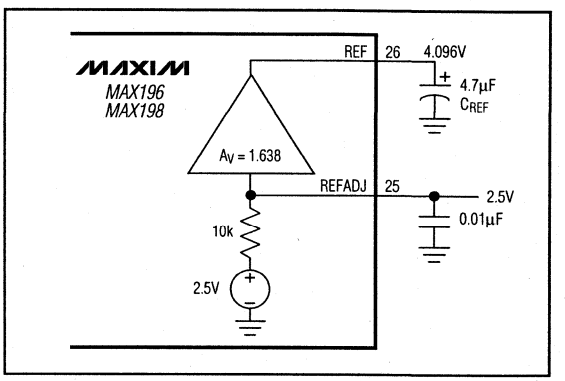


Figure 9c. The external reference overdrives the internal reference.

Multirange, Single +5V, 12-Bit DAS with 12-Bit Bus Interface

results may be read. Input overvoltage protection is active in all power-down modes. The device returns to normal operation on the first $\overline{WR}$ falling edge during write operation.

Choosing Power-Down Modes

The bandgap reference and reference buffer remain active in STBYPD mode, maintaining the voltage on the 4.7µF capacitor at the REF pin. This is a "DC" state that does not degrade after power-down of any duration. Therefore, you can use any sampling rate with this mode, without regard to start-up delays.

However, in FULLPD mode, only the bandgap reference is active. Connect a 33µF capacitor between REF and AGND to maintain the reference voltage between conversions and to reduce transients when the buffer is enabled and disabled. Throughput rates down to 1ksps can be achieved without allotting extra acquisition time for reference recovery prior to conversion. This allows conversion to begin immediately after power-down ends. If the discharge of the REF capacitor during FULLPD exceeds the desired limits for accuracy (less than a fraction of an LSB), run a STBYPD power-down cycle prior to starting conversions. Take into account that the reference buffer recharges the bypass capacitor at an 80mV/ms slew rate, and add 50µs for settling time. Throughput rates of 10ksps offer typical supply currents of 470µA, using the recommended 33µF capacitor value.

Auto-Shutdown

Selecting STBYPD on every conversion automatically shuts the MAX196/MAX198 down after each conversion without requiring any start-up time on the next conversion.

Transfer Function

Output data coding for the MAX196/MAX198 is binary in unipolar mode with 1LSB = (FS / 4096) and twos-complement binary in bipolar mode with 1LSB = [(2 x |FS|) / 4096]. Code transitions occur halfway between successive-integer LSB values. Figures 10 and 11 show the input/output (I/O) transfer functions for unipolar and bipolar operations, respectively. For full-scale (FS) values, refer to Table 1.

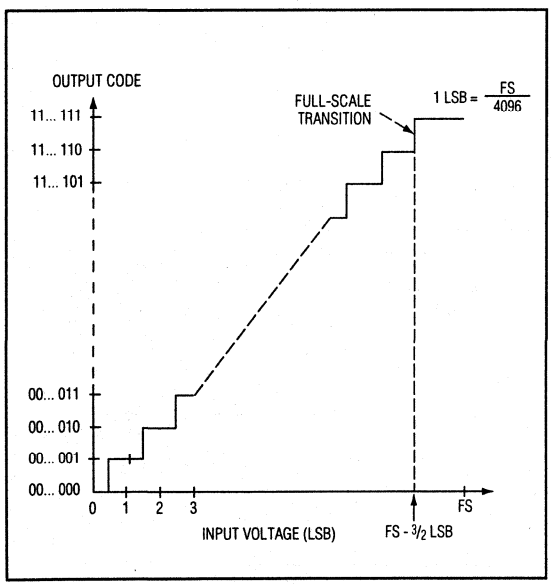


Figure 10. Unipolar Transfer Function

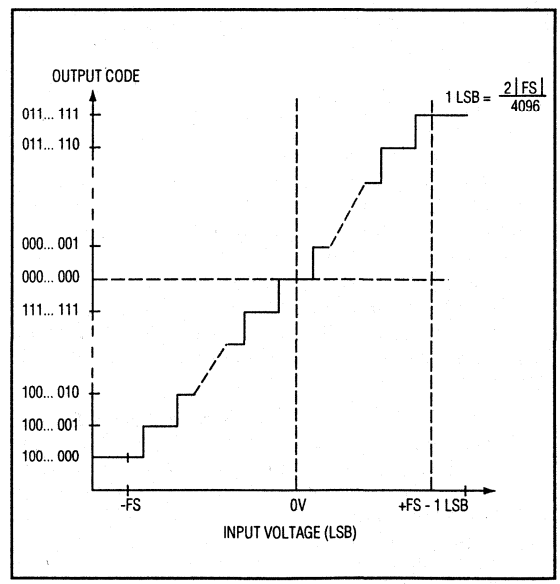


Figure 11. Bipolar Transfer Function

Multirange, Single +5V, 12-Bit DAS with 12-Bit Bus Interface

Layout, Grounding, and Bypassing

Careful printed circuit board layout is essential for best system performance. For best performance, use a ground plane. To reduce crosstalk and noise injection, keep analog and digital signals separate. Digital ground lines can run between digital signal lines to minimize interference. Connect analog grounds and DGND in a star configuration to AGND. For noise-free operation, ensure the ground return from AGND to the supply ground is low impedance and as short as possible. Connect the logic grounds directly to the supply ground. Bypass V_{DD} with 0.1µF and 4.7µF capacitors to AGND to minimize high- and low-frequency fluctuations. If the supply is excessively noisy, connect a 5Ω resistor between the supply and V_{DD}, as shown in Figure 12.

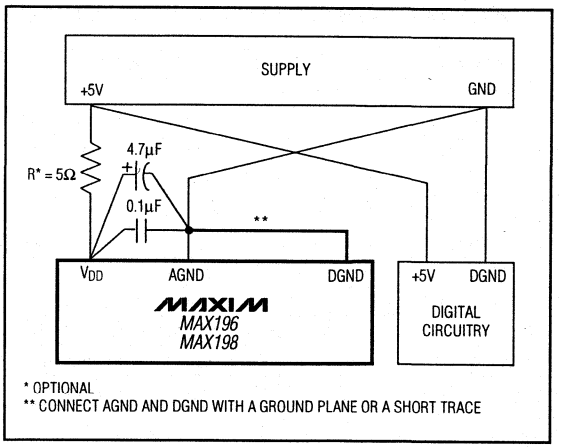
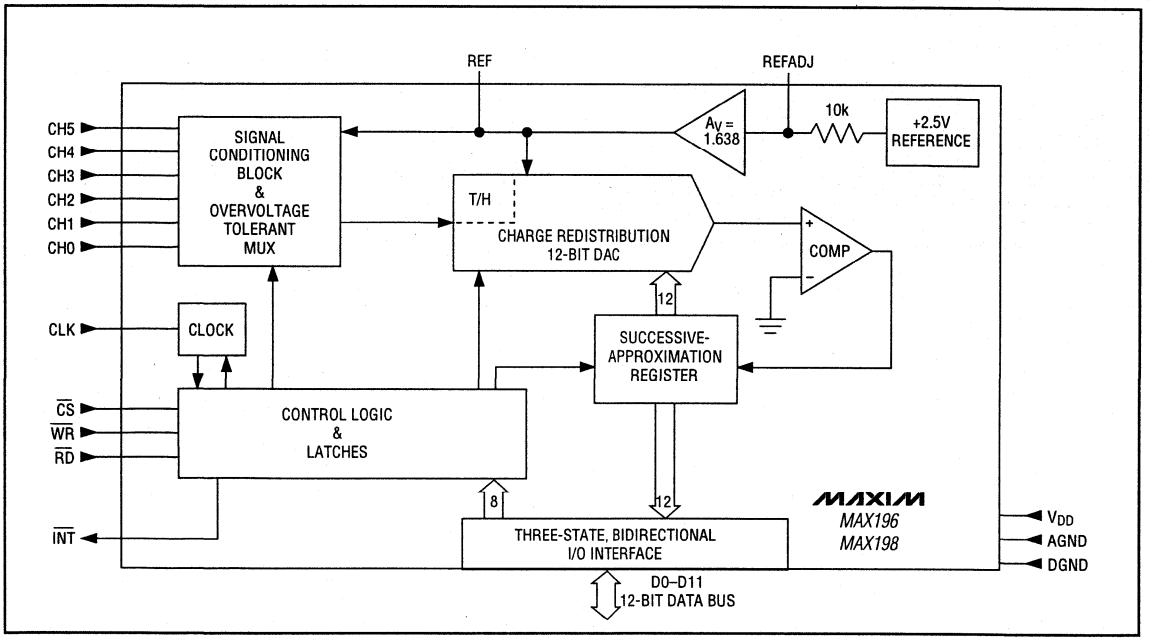


Figure 12. Power-Supply Grounding Connection

Functional Diagram



Multirange, Single +5V, 12-Bit DAS with 12-Bit Bus Interface

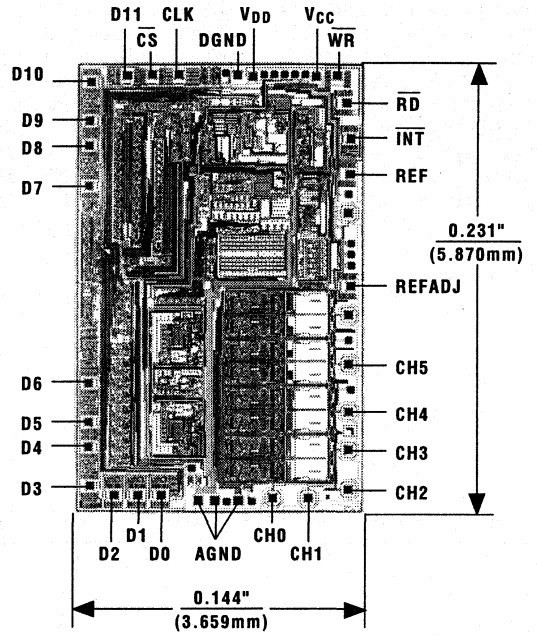
_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX196BC/D	0°C to +70°C	Dice*
MAX196AENI	-40°C to +85°C	28 Narrow Plastic DIP
MAX196BENI	-40°C to +85°C	28 Narrow Plastic DIP
MAX196AEWI	-40°C to +85°C	28 Wide SO
MAX196BEWI	-40°C to +85°C	28 Wide SO
MAX196AEAI	-40°C to +85°C	28 SSOP
MAX196BEAI	-40°C to +85°C	28 SSOP
MAX196AMYI	-55°C to +125°C	28 Narrow Ceramic SB**
MAX196BMYI	-55°C to +125°C	28 Narrow Ceramic SB**
MAX198ACNI	0°C to +70°C	28 Narrow Plastic DIP
MAX198BCNI	0°C to +70°C	28 Narrow Plastic DIP
MAX198ACWI	0°C to +70°C	28 Wide SO
MAX198BCWI	0°C to +70°C	28 Wide SO
MAX198ACAI	0°C to +70°C	28 SSOP
MAX198BCAI	0°C to +70°C	28 SSOP
MAX198BC/D	0°C to +70°C	Dice*
MAX198AENI	-40°C to +85°C	28 Narrow Plastic DIP
MAX198BENI	-40°C to +85°C	28 Narrow Plastic DIP
MAX198AEWI	-40°C to +85°C	28 Wide SO
MAX198BEWI	-40°C to +85°C	28 Wide SO
MAX198AEAI	-40°C to +85°C	28 SSOP
MAX198BEAI	-40°C to +85°C	28 SSOP
MAX198AMYI	-55°C to +125°C	28 Narrow Ceramic SB**
MAX198BMYI	-55°C to +125°C	28 Narrow Ceramic SB**

* *Dice are specified at T_A = +25°C, DC parameters only.*

** *Contact factory for availability and processing to MIL-STD-883.*

Chip Topography



TRANSISTOR COUNT: 2956

SUBSTRATE CONNECTED TO GND

19-0381; Rev 1; 6/96

EVALUATION KIT AVAILABLE

MAXIM

Multi-Range (±10V, ±5V, +10V, +5V), Single +5V, 12-Bit DAS with 8+4 Bus Interface

General Description

The MAX197 multi-range, 12-bit data-acquisition system (DAS) requires only a single +5V supply for operation, yet accepts signals at its analog inputs that may span both above the power-supply rail and below ground. This system provides 8 analog input channels that are independently software programmable for a variety of ranges: ±10V, ±5V, 0V to +10V, or 0V to +5V. This increases effective dynamic range to 14 bits, and provides the user flexibility to interface 4mA-to-20mA, ±12V, and ±15V powered sensors to a single +5V system. In addition, the converter is overvoltage tolerant to ±16.5V; a fault condition on any channel will **not** affect the conversion result of the selected channel. Other features include a 5MHz bandwidth track/hold, a 100ksps throughput rate, software-selectable internal or external clock and acquisition, 8+4 parallel interface, and an internal 4.096V or an external reference.

A hardware $\overline{SHDN}$ pin and two programmable power-down modes (STBYPD, FULLPD) are provided for low-current shutdown between conversions. In STBYPD mode, the reference buffer remains active, eliminating start-up delays.

The MAX197 employs a standard microprocessor (µP) interface. A three-state data I/O port is configured to operate with 8-bit data buses, and data-access and bus-release timing specifications are compatible with most popular µPs. All logic inputs and outputs are TTL/CMOS compatible.

The MAX197 is available in 28-pin DIP, wide SO, SSOP, and ceramic SB packages.

For a different combination of ranges (±4V, ±2V, 0V to 4V, 0V to 2V), see the MAX199 data sheet. For 12-bit bus interface, see the MAX196 and MAX198 data sheets.

Applications

Industrial-Control Systems
Robotics
Data-Acquisition Systems
Automatic Testing Systems
Medical Instruments
Telecommunications

Functional Diagram appears at end of data sheet.

Features

- ♦ **12-Bit Resolution, 1/2LSB Linearity**
- ♦ **Single +5V Operation**
- ♦ **Software-Selectable Input Ranges: ±10V, ±5V, 0V to 10V, 0V to 5V**
- ♦ **Fault-Protected Input Multiplexer (±16.5V)**
- ♦ **8 Analog Input Channels**
- ♦ **6µs Conversion Time, 100ksps Sampling Rate**
- ♦ **Internal or External Acquisition Control**
- ♦ **Internal 4.096V or External Reference**
- ♦ **Two Power-Down Modes**
- ♦ **Internal or External Clock**

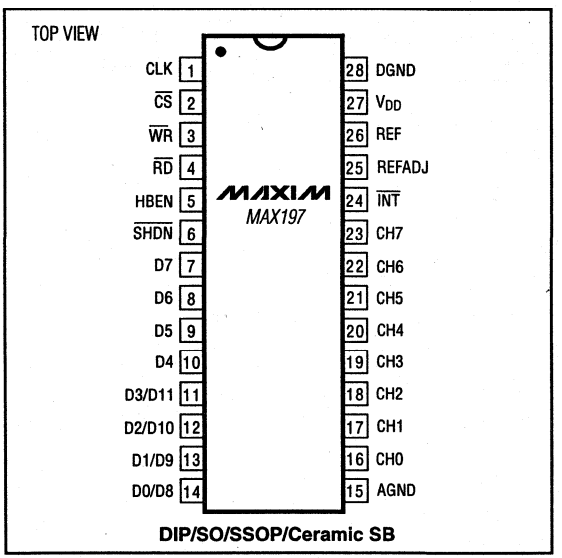
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX197ACNI	0°C to +70°C	28 Narrow Plastic DIP
MAX197BCNI	0°C to +70°C	28 Narrow Plastic DIP
MAX197ACWI	0°C to +70°C	28 Wide SO
MAX197BCWI	0°C to +70°C	28 Wide SO
MAX197ACAI	0°C to +70°C	28 SSOP
MAX197BCAI	0°C to +70°C	28 SSOP
MAX197BC/D	0°C to +70°C	Dice*

Ordering Information continued at end of data sheet.

**Dice are specified at TA = +25°C, DC parameters only.*

Pin Configuration



DIP/SO/SSOP/Ceramic SB

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Multi-Range (±10V, ±5V, +10V, +5V), Single +5V, 12-Bit DAS with 8+4 Bus Interface

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND .....-0.3V to +7V
AGND to DGND .....-0.3V to +0.3V
REF to AGND .....-0.3V to (V_{DD} + 0.3V)
REFADJ to AGND .....-0.3V to (V_{DD} + 0.3V)
Digital Inputs to DGND .....-0.3V to (V_{DD} + 0.3V)
Digital Outputs to DGND .....-0.3V to (V_{DD} + 0.3V)
CH0–CH7 to AGND .....±16.5V
Continuous Power Dissipation (T_A = +70°C)
Narrow Plastic DIP (derate 14.29mW/°C above +70°C)....1143mW
Wide SO (derate 12.50mW/°C above +70°C).....1000mW
SSOP (derate 9.52mW/°C above +70°C) 762mW
Narrow Ceramic SB (derate 20.00mW/°C above +70°C)..1600mW

Operating Temperature Ranges
MAX197_C_ _ .....0°C to +70°C
MAX197_E_ _ .....-40°C to +85°C
MAX197_M_ _ .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ±5%; unipolar/bipolar range; external reference mode, V_{REF} = 4.096V; 4.7µF at REF pin; external clock, f_{CLK} = 2.0MHz with 50% duty cycle; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY (Note 1)							
Resolution				12			Bits
Integral Nonlinearity	INL	MAX197A				±1/2	LSB
		MAX197B				±1	
Differential Nonlinearity	DNL					±1	LSB
Offset Error		Unipolar	MAX197A			±3	LSB
			MAX197B			±5	
		Bipolar	MAX197A			±5	
			MAX197B			±10	
Channel-to-Channel Offset Error Matching		Unipolar			±0.1		LSB
		Bipolar			±0.5		
Gain Error (Note 2)		Unipolar	MAX197A			±7	LSB
			MAX197B			±10	
		Bipolar	MAX197A			±7	
			MAX197B			±10	
Gain Temperature Coefficient (Note 2)		Unipolar			3		ppm/°C
		Bipolar			5		
DYNAMIC SPECIFICATIONS (10kHz sine-wave input, ±10Vp-p, f_{SAMPLE} = 100ksps)							
Signal-to-Noise + Distortion Ratio	SINAD		MAX197A	70			dB
			MAX197B	69			
Total Harmonic Distortion	THD	Up to the 5th harmonic			-85	-78	dB
Spurious-Free Dynamic Range	SFDR			80			dB
Channel-to-Channel Crosstalk		50kHz, V_{IN} = ±5V (Note 3)			-86		dB
Aperture Delay		External CLK mode/external acquisition control			15		ns
Aperture Jitter		External CLK mode/external acquisition control			<50		ps
		Internal CLK mode/internal acquisition control (Note 4)			10		ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V ±5%; unipolar/bipolar range; external reference mode, V_{REF} = 4.096V; 4.7µF at REF pin; external clock, f_{CLK} = 2.0MHz with 50% duty cycle; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG INPUT							
Track/Hold Acquisition Time		f_{CLK} = 2.0MHz				3	µs
Small-Signal Bandwidth		-3dB rolloff	±10V range		5		MHz
			±5V range		2.5		
			0V to 10V range		2.5		
			0V to 5V range		1.25		
Input Voltage Range (See Table 1)		Unipolar		0		10	V
				0		5	
		Bipolar		-10		10	
				-5		5	
Input Current		Unipolar	0V to 10V range			720	µA
			0V to 5V range			360	
		Bipolar	-10V to 10V range	-1200		720	
			-5V to 5V range	-600		360	
Input Dynamic Resistance		Unipolar			21		kΩ
		Bipolar			16		
Input Capacitance		(Note 5)				40	pF
INTERNAL REFERENCE							
REF Output Voltage	V_{REF}	T_A = +25°C		4.076	4.096	4.116	V
REF Output Tempco	TC V_{REF}				40		ppm/°C
Output Short-Circuit Current						30	mA
Load Regulation		0mA to 0.5mA output current (Note 6)				7.5	mV
Capacitive Bypass at REF				4.7			µF
REFADJ Output Voltage				2.465	2.500	2.535	V
REFADJ Adjustment Range		With recommended circuit (Figure 1)			±1.5		%
Buffer Voltage Gain					1.6384		V/V
REFERENCE INPUT (Buffer disabled, reference input applied to REF pin)							
Input Voltage Range				2.4		4.18	V
Input Current		V_{REF} = 4.18V	Normal or STANDBY power-down mode			400	µA
			FULL power-down mode			1	
Input Resistance		Normal or STANDBY power-down mode		10			kΩ
		FULL power-down mode		5			MΩ
REFADJ Threshold for Buffer Disable				V_{DD} - 50mV			V

Multi-Range (±10V, ±5V, +10V, +5V), Single +5V, 12-Bit DAS with 8+4 Bus Interface

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V ±5%; unipolar/bipolar range; external reference mode, V_{REF} = 4.096V; 4.7µF at REF pin; external clock, f_{CLK} = 2.0MHz with 50% duty cycle; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER REQUIREMENTS							
Supply Voltage	V_{DD}			4.75		5.25	V
Supply Current	I_{DD}	Normal mode, bipolar ranges				18	mA
		Normal mode, unipolar ranges			6	10	
		Standby power-down (STBYPD)			700	850	µA
		Full power-down mode (FULLPD) (Note 7)				120	
Power-Supply Rejection Ratio (Note 8)	PSRR	External reference = 4.096V				±1/2	LSB
		Internal reference			±1/2		
TIMING							
Internal Clock Frequency	f_{CLK}	C_{CLK} = 100pF		1.25	1.56	2.00	MHz
External Clock Frequency Range	f_{CLK}			0.1		2.0	MHz
Acquisition Time	t_{ACQI}	Internal acquisition	External CLK	3.0			µs
			Internal CLK	3.0		5.0	
	t_{ACQE}	External acquisition (Note 9)		3.0			
		After FULLPD or STBYPD			5		
Conversion Time	t_{CONV}	External CLK		6.0			µs
		Internal CLK, C_{CLK} = 100pF		6.0	7.7	10.0	
Throughput Rate		External CLK				100	ksps
		Internal CLK, C_{CLK} = 100pF		62			
Bandgap Reference Start-Up Time		Power-up (Note 10)			200		µs
Reference Buffer Settling		To 0.1mV REF bypass capacitor fully discharged	C_{REF} = 4.7µF		8		ms
			C_{REF} = 33µF		60		
DIGITAL INPUTS (D7–D0, CLK, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, HBEN, $\overline{SHDN}$) (Note 11)							
Input High Voltage	V_{INH}			2.4			V
Input Low Voltage	V_{INL}					0.8	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}				±10	µA
Input Capacitance	C_{IN}	(Note 5)				15	pF
DIGITAL OUTPUTS (D7–D4, D3/D11, D2/D10, D1/D9, D0/D8, $\overline{INT}$)							
Output Low Voltage	V_{OL}	V_{DD} = 4.75V, I_{SINK} = 1.6mA				0.4	V
Output High Voltage	V_{OH}	V_{DD} = 4.75V, I_{SOURCE} = 1mA		V_{DD} - 1			V
Three-State Output Capacitance	C_{OUT}	(Note 5)				15	pF

TIMING CHARACTERISTICS

(V_{DD} = 5V ±5%; unipolar/bipolar range; external reference mode, V_{REF} = 4.096V; 4.7µF at REF pin; external clock, f_{CLK} = 2.0MHz with 50% duty cycle; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CS}$ Pulse Width	t_{CS}		80			ns
$\overline{WR}$ Pulse Width	t_{WR}		80			ns
$\overline{CS}$ to $\overline{WR}$ Setup Time	t_{CSWS}		0			ns
$\overline{CS}$ to $\overline{WR}$ Hold Time	t_{CSWH}		0			ns
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_{CSRS}		0			ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_{CSRH}		0			ns
CLK to $\overline{WR}$ Setup Time	t_{CWS}				100	ns
CLK to $\overline{WR}$ Hold Time	t_{CWH}				50	ns
Data Valid to $\overline{WR}$ Setup	t_{DS}		60			ns
Data Valid to $\overline{WR}$ Hold	t_{DH}		0			ns
$\overline{RD}$ Low to Output Data Valid	t_{DO}	Figure 2, C_L = 100pF (Note 12)			120	ns
HBEN High or HBEN Low to Output Valid	t_{DO1}	Figure 2, C_L = 100pF (Note 12)			120	ns
$\overline{RD}$ High to Output Disable	t_{TR}	(Note 13)			70	ns
$\overline{RD}$ Low to $\overline{INT}$ High Delay	t_{INT1}				120	ns

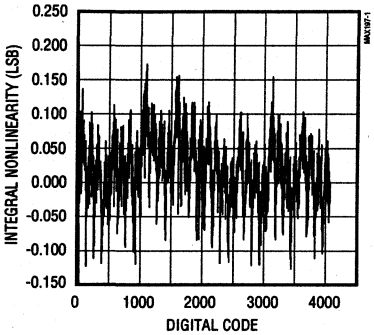
Note 1: Accuracy specifications tested at V_{DD} = 5.0V. Performance at power-supply tolerance limits guaranteed by Power-Supply Rejection test. Tested for the ±10V input range.
Note 2: External reference: V_{REF} = 4.096V, offset error nulled, ideal last code transition = FS - 3/2LSB.
Note 3: Ground "on" channel; sine wave applied to all "off" channels.
Note 4: Maximum full-power input frequency for 1LSB error with 10ns jitter = 3kHz.
Note 5: Guaranteed by design. Not tested.
Note 6: Use static loads only.
Note 7: Tested using internal reference.
Note 8: PSRR measured at full-scale.
Note 9: External acquisition timing: starts at data valid at ACQMOD = low control byte; ends at rising edge of $\overline{WR}$ with ACQMOD = high control byte.
Note 10: Not subject to production testing. Provided for design guidance only.
Note 11: All input control signals specified with t_R = t_F = 5ns from a voltage level of 0.8V to 2.4V.
Note 12: t_{DO} and t_{DO1} are measured with the load circuits of Figure 2 and defined as the time required for an output to cross 0.8V or 2.4V.
Note 13: t_{TR} is defined as the time required for the data lines to change by 0.5V.

Multi-Range (±10V, ±5V, +10V, +5V), Single +5V, 12-Bit DAS with 8+4 Bus Interface

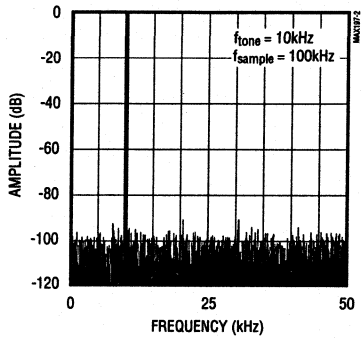
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

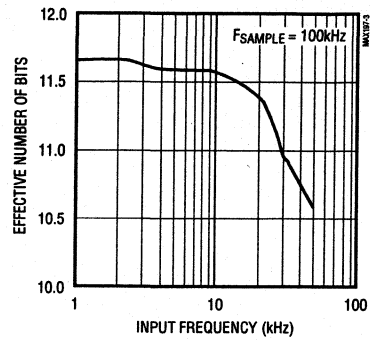
INTEGRAL NONLINEARITY vs. DIGITAL CODE



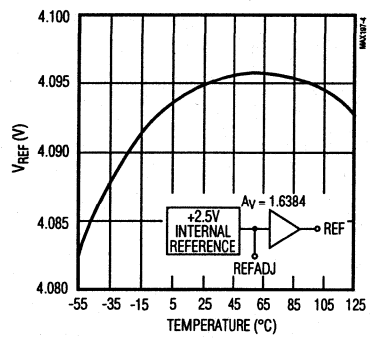
FFT PLOT



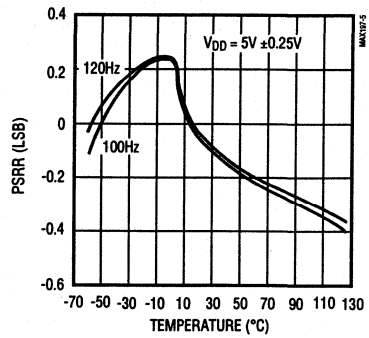
EFFECTIVE NUMBER OF BITS vs. INPUT FREQUENCY



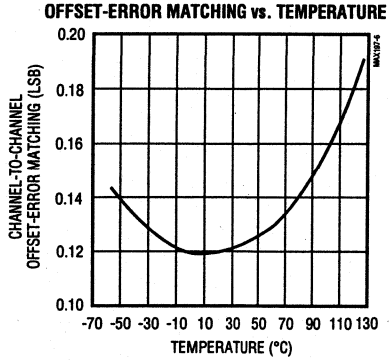
REFERENCE OUTPUT VOLTAGE (V_{REF}) vs. TEMPERATURE



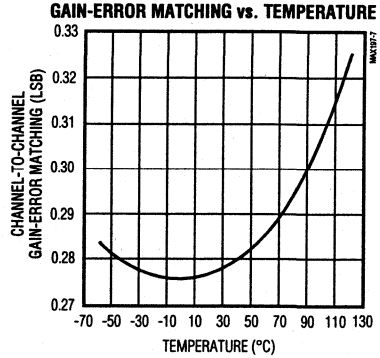
POWER-SUPPLY REJECTION RATIO vs. TEMPERATURE



CHANNEL-TO-CHANNEL OFFSET-ERROR MATCHING vs. TEMPERATURE



CHANNEL-TO-CHANNEL GAIN-ERROR MATCHING vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1	CLK	Clock Input. In external clock mode, drive CLK with a TTL/CMOS compatible clock. In internal clock mode, place a capacitor from this pin to ground to set the internal clock frequency; f_{CLK} = 1.56MHz typical with C_{CLK} = 100pF.
2	$\overline{CS}$	Chip Select, active low.
3	$\overline{WR}$	When $\overline{CS}$ is low, in the internal acquisition mode, a rising edge on $\overline{WR}$ latches in configuration data and starts an acquisition plus a conversion cycle. When $\overline{CS}$ is low, in the external acquisition mode, the first rising edge on $\overline{WR}$ starts an acquisition and a second rising edge on $\overline{WR}$ ends acquisition and starts a conversion cycle.
4	$\overline{RD}$	If $\overline{CS}$ is low, a falling edge on $\overline{RD}$ will enable a read operation on the data bus.
5	HBEN	Used to multiplex the 12-bit conversion result. When high, the 4 MSBs are multiplexed on the data bus; when low, the 8 LSBs are available on the bus.
6	$\overline{SHDN}$	Shutdown. Puts the device into full power-down (FULLPD) mode when pulled low.
7–10	D7–D4	Three-State Digital I/O
11	D3/D11	Three-State Digital I/O. D3 output (HBEN = low), D11 output (HBEN = high).
12	D2/D10	Three-State Digital I/O. D2 output (HBEN = low), D10 output (HBEN = high).
13	D1/D9	Three-State Digital I/O. D1 output (HBEN = low), D9 output (HBEN = high).
14	D0/D8	Three-State Digital I/O. D0 output (HBEN = low), D8 output (HBEN = high). D0 = LSB.
15	AGND	Analog Ground
16–23	CH0–CH7	Analog Input Channels
24	$\overline{INT}$	$\overline{INT}$ goes low when conversion is complete and output data is ready.
25	REFADJ	Bandgap Voltage-Reference Output/External Adjust Pin. Bypass with a 0.01µF capacitor to AGND. Connect to V_{DD} when using an external reference at the REF pin.
26	REF	Reference Buffer Output/ADC Reference Input. In internal reference mode, the reference buffer provides a 4.096V nominal output, externally adjustable at REFADJ. In external reference mode, disable the internal buffer by pulling REFADJ to V_{DD}.
27	V_{DD}	+5V Supply. Bypass with 0.1µF capacitor to AGND.
28	DGND	Digital Ground

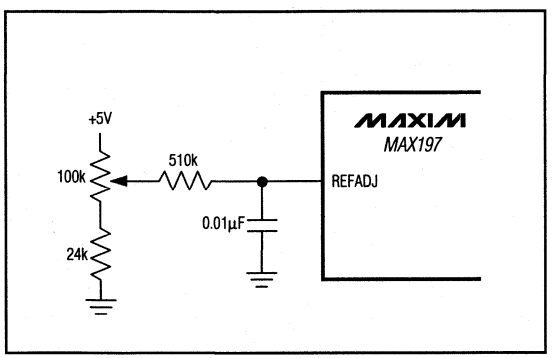


Figure 1. Reference-Adjust Circuit

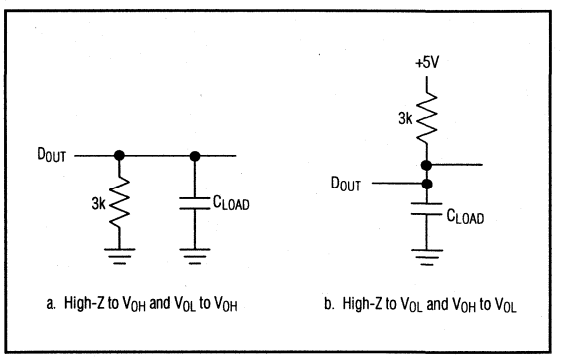


Figure 2. Load Circuits for Enable Time

Multi-Range (±10V, ±5V, +10V, +5V), Single +5V, 12-Bit DAS with 8+4 Bus Interface

Detailed Description

Converter Operation

The MAX197, a multi-range, fault-tolerant ADC, uses successive approximation and internal input track/hold (T/H) circuitry to convert an analog signal to a 12-bit digital output. The parallel-output format provides easy interface to microprocessors (µPs). Figure 3 shows the MAX197 in its simplest operational configuration.

Analog-Input Track/Hold

In the internal acquisition control mode (control bit D5 set to 0), the T/H enters its tracking mode on $\overline{WR}$'s rising edge, and enters its hold mode when the internally timed (6 clock cycles) acquisition interval ends. A low impedance input source, which settles in less than 1.5µs, is required to maintain conversion accuracy at the maximum conversion rate.

In the external acquisition control mode (D5 = 1), the T/H enters its tracking mode on the first $\overline{WR}$ rising edge and enters its hold mode when it detects the second $\overline{WR}$ rising edge with D5 = 0. See the *External Acquisition* section.

Input Bandwidth

The ADC's input tracking circuitry has a 5MHz small-signal bandwidth. When using the internal acquisition mode with an external clock frequency of 2MHz, a 100ksps throughput rate can be achieved. It is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended (MAX274/MAX275 continuous-time filters).

Input Range and Protection

Figure 4 shows the equivalent input circuit. With V_{REF} = 4.096V, the MAX197 can be programmed for input ranges of ±10V, ±5V, 0V to 10V, or 0V to 5V by setting the appropriate control bits (D3, D4) in the control byte (see Tables 2 and 3). The full-scale input voltage depends on the voltage at REF (Table 1). When an external reference is applied at REFADJ, the voltage at REF is given by $V_{REF} = 1.6384 \times V_{REFADJ}$ ($2.4V < V_{REF} < 4.18V$).

Table 1. Full Scale and Zero Scale

RANGE (V)	ZERO SCALE (V)	-FULL SCALE	+FULL SCALE
0 to 5	0	—	V_{REF} x 1.2207
0 to 10	0	—	V_{REF} x 2.4414
±5	—	-V_{REF} x 1.2207	V_{REF} x 1.2207
±10	—	-V_{REF} x 2.4414	V_{REF} x 2.4414

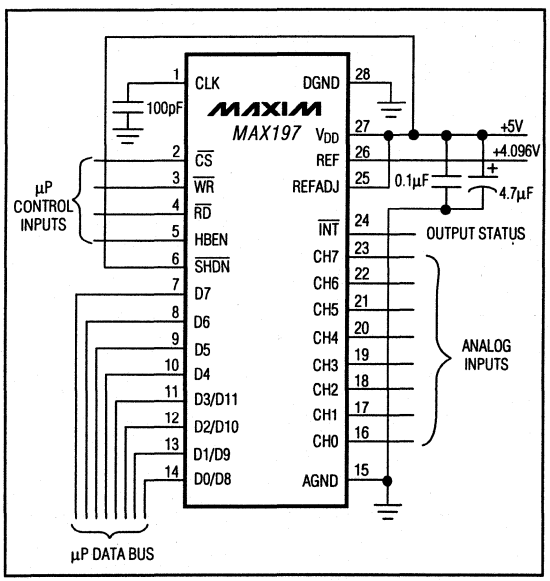


Figure 3. Operational Diagram

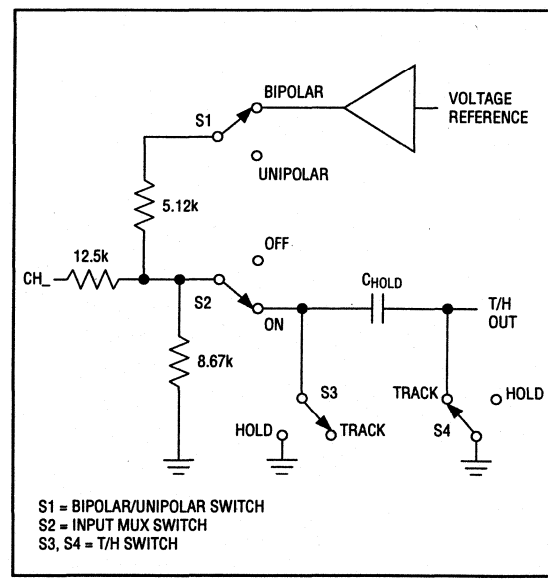


Figure 4. Equivalent Input Circuit

Multi-Range (±10V, ±5V, +10V, +5V), Single +5V, 12-Bit DAS with 8+4 Bus Interface

The input channels are overvoltage protected to ±16.5V. This protection is active even if the device is in power-down mode.

Even with V_{DD} = 0V, the input resistive network provides current-limiting that adequately protects the device.

Digital Interface

Input data (control byte) and output data are multiplexed on a three-state parallel interface. This parallel I/O can easily be interfaced with a µP. $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ control the write and read operations. $\overline{CS}$ is the standard chip-select signal, which enables a µP to address the MAX197 as an I/O port. When high, it disables the $\overline{WR}$ and $\overline{RD}$ inputs and forces the interface into a high-Z state.

Input Format

The control byte is latched into the device, on pins D7–D0, during a write cycle. Table 2 shows the control-byte format.

Output Data Format

The output data format is binary in unipolar mode and twos-complement binary in bipolar mode. When reading the output data, $\overline{CS}$, and $\overline{RD}$ must be low. When HBEN is low, the lower eight bits are read. When HBEN is high, the upper four MSBs are available and the output data bits D4–D7 are either set low (in unipolar mode) or set to the value of the MSB (in bipolar mode) (Table 6).

Table 2. Control-Byte Format

D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
PD1	PD0	ACQMOD	RNG	BIP	A2	A1	A0

BIT	NAME	DESCRIPTION
7, 6	PD1, PD0	These two bits select the clock and power-down modes (Table 4).
5	ACQMOD	0 = internally controlled acquisition (6 clock cycles), 1 = externally controlled acquisition
4	RNG	Selects the full-scale voltage magnitude at the input (Table 3).
3	BIP	Selects unipolar or bipolar conversion mode (Table 3).
2, 1, 0	A2, A1, A0	These are address bits for the input mux to select the "on" channel (Table 5).

Table 3. Range and Polarity Selection

BIP	RNG	INPUT RANGE (V)
0	0	0 to 5
0	1	0 to 10
1	0	±5
1	1	±10

Table 4. Clock and Power-Down Selection

PD1	PD0	DEVICE MODE
0	0	Normal Operation / External Clock Mode
0	1	Normal Operation / Internal Clock Mode
1	0	Standby Power-Down (STBYPD); clock mode is unaffected
1	1	Full Power-Down (FULLPD); clock mode is unaffected

Table 5. Channel Selection

A2	A1	A0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7
0	0	0	*							
0	0	1		*						
0	1	0			*					
0	1	1				*				
1	0	0					*			
1	0	1						*		
1	1	0							*	
1	1	1								*

Multi-Range (±10V, ±5V, +10V, +5V), Single +5V, 12-Bit DAS with 8+4 Bus Interface

Table 6. Data-Bus Output

PIN	HBEN = LOW	HBEN = HIGH
D0	B0 (LSB)	B8
D1	B1	B9
D2	B2	B10
D3	B3	B11 (MSB)
D4	B4	B11 (BIP = 1) / 0 (BIP = 0)
D5	B5	B11 (BIP = 1) / 0 (BIP = 0)
D6	B6	B11 (BIP = 1) / 0 (BIP = 0)
D7	B7	B11 (BIP = 1) / 0 (BIP = 0)

How to Start a Conversion

Conversions are initiated with a write operation, which selects the mux channel and configures the MAX197 for either unipolar or bipolar input range. A write pulse ($\overline{WR}$ + $\overline{CS}$) can either start an acquisition interval or initiate a combined acquisition plus conversion. The sampling interval occurs at the end of the acquisition interval. The ACQMOD bit in the input control byte offers two options for acquiring the signal: internal or external. The conversion period lasts for 12 clock cycles in either internal or external clock or acquisition mode.

Writing a new control byte during conversion cycle will abort conversion and start a new acquisition interval.

Internal Acquisition

Select internal acquisition by writing the control byte with the ACQMOD bit cleared (ACQMOD = 0). This causes the write pulse to initiate an acquisition interval whose duration is internally timed. Conversion starts when this six-clock-cycle acquisition interval (3µs with f_{CLK} = 2MHz) ends. See Figure 5.

External Acquisition

Use the external acquisition timing mode for precise control of the sampling aperture and/or independent control of acquisition and conversion times. The user controls acquisition and start-of-conversion with two separate write pulses. The first pulse, written with ACQMOD = 1, starts an acquisition interval of indeterminate length. The second write pulse, written with ACQMOD = 0, terminates acquisition and starts conversion on $\overline{WR}$'s rising edge (Figure 6). However, if the second control byte contains ACQMOD = 1, an indefinite acquisition interval is restarted.

The address bits for the input mux must have the same values on the first and second write pulses. Power-down mode bits (PD0, PD1) can assume new values on the second write pulse (see *Power-Down Mode*).

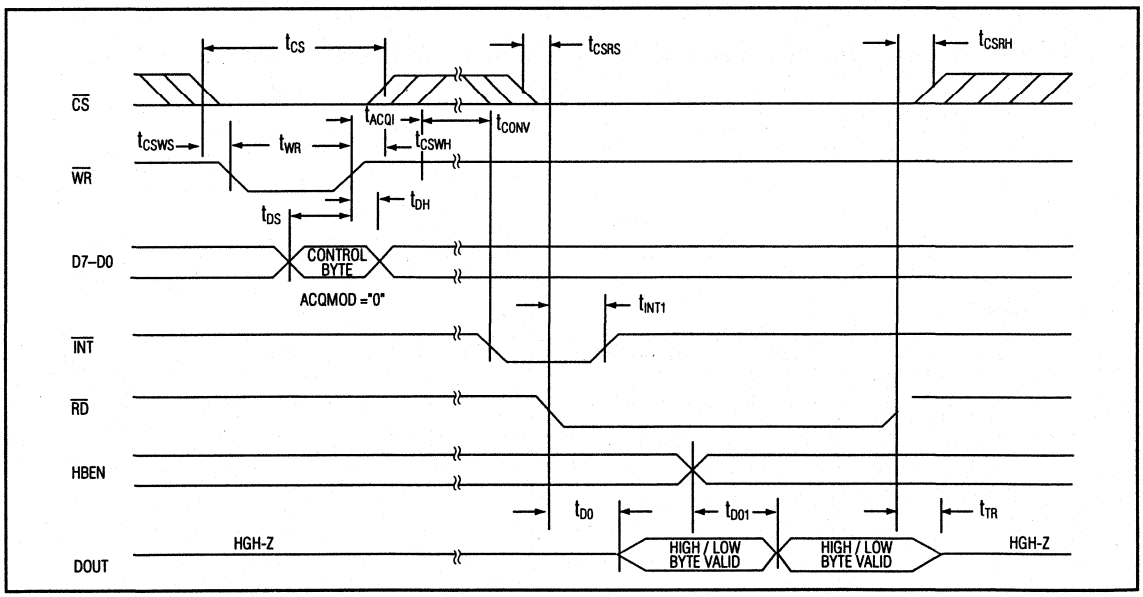


Figure 5. Conversion Timing Using Internal Acquisition Mode

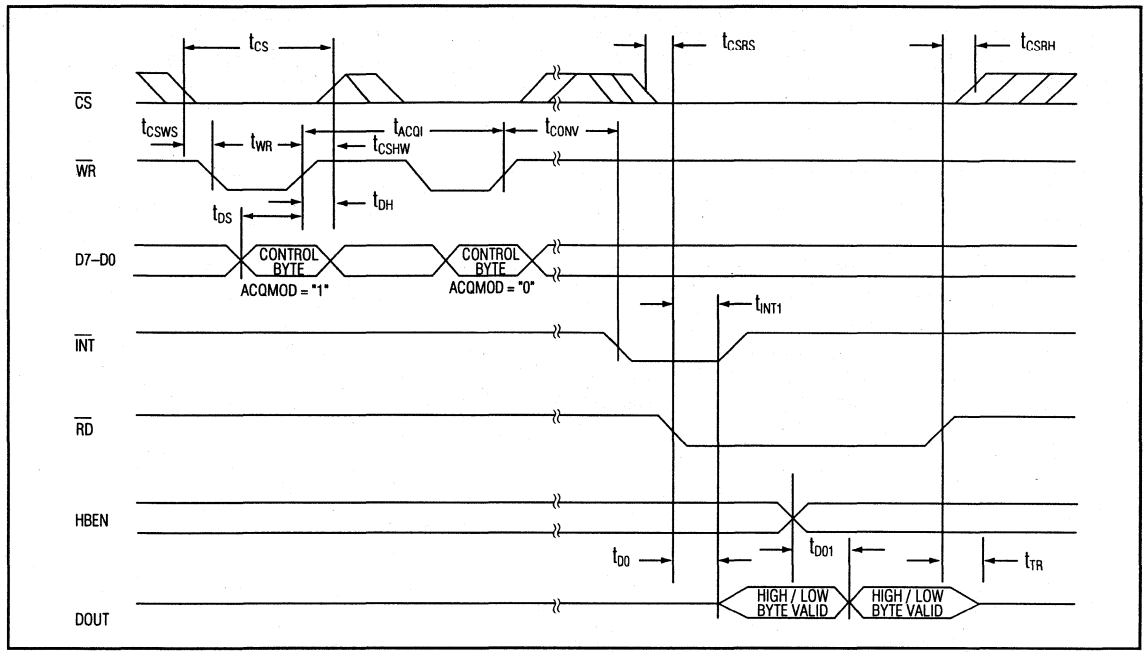


Figure 6. Conversion Timing Using External Acquisition Mode

How to Read a Conversion

A standard interrupt signal, $\overline{INT}$, is provided to allow the device to flag the µP when the conversion has ended and a valid result is available. $\overline{INT}$ goes low when conversion is complete and the output data is ready (Figures 5 and 6). It returns high on the first read cycle or if a new control byte is written.

Clock Modes

The MAX197 operates with either an internal or an external clock. Control bits (D6, D7) select either internal or external clock mode. Once the desired clock mode is selected, changing these bits to program power-down will not affect the clock mode. In each mode, internal or external acquisition can be used. At power-up, external clock mode is selected.

Internal Clock Mode

Select internal clock mode to free the µP from the burden of running the SAR conversion clock. To select this mode, write the control byte with D7 = 0 and D6 = 1. A 100pF capacitor between the CLK pin and ground sets this frequency to 1.56MHz nominal. Figure 7 shows a linear relationship between the internal clock period and the value of the external capacitor used.

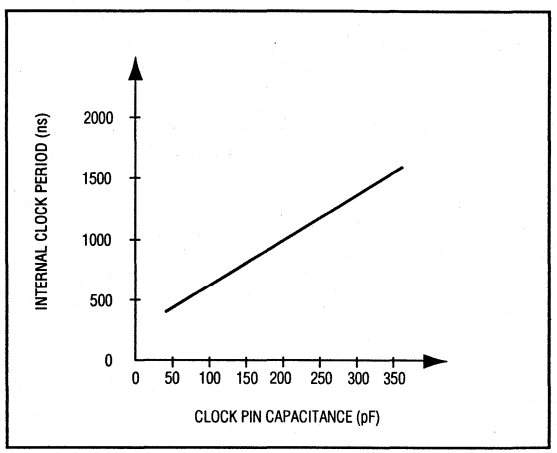


Figure 7. Internal Clock Period vs. Clock Pin Capacitance

Multi-Range (±10V, ±5V, +10V, +5V), Single +5V, 12-Bit DAS with 8+4 Bus Interface

External Clock Mode

Select external clock mode by writing the control byte with D7 = 0 and D6 = 0. Figure 8 shows CLK and $\overline{WR}$ timing relationships in internal and external acquisition modes, with an external clock. A 100kHz to 2.0MHz external clock with 45% to 55% duty cycle is required for proper operation. Operating at clock frequencies lower than 100kHz will cause a voltage droop across the hold capacitor, and subsequently degrade performance.

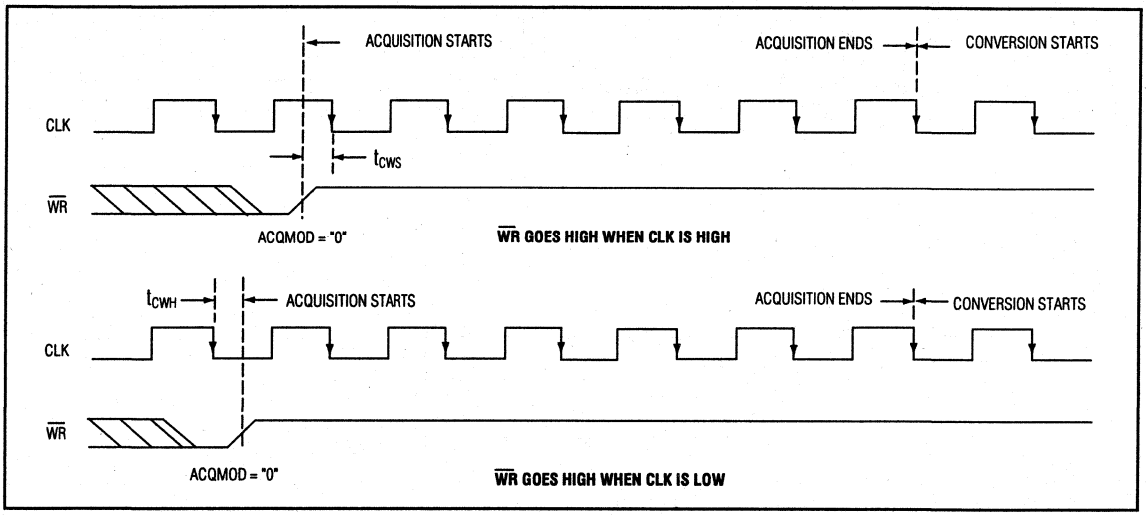


Figure 8a. External Clock and $\overline{WR}$ Timing (Internal Acquisition Mode)

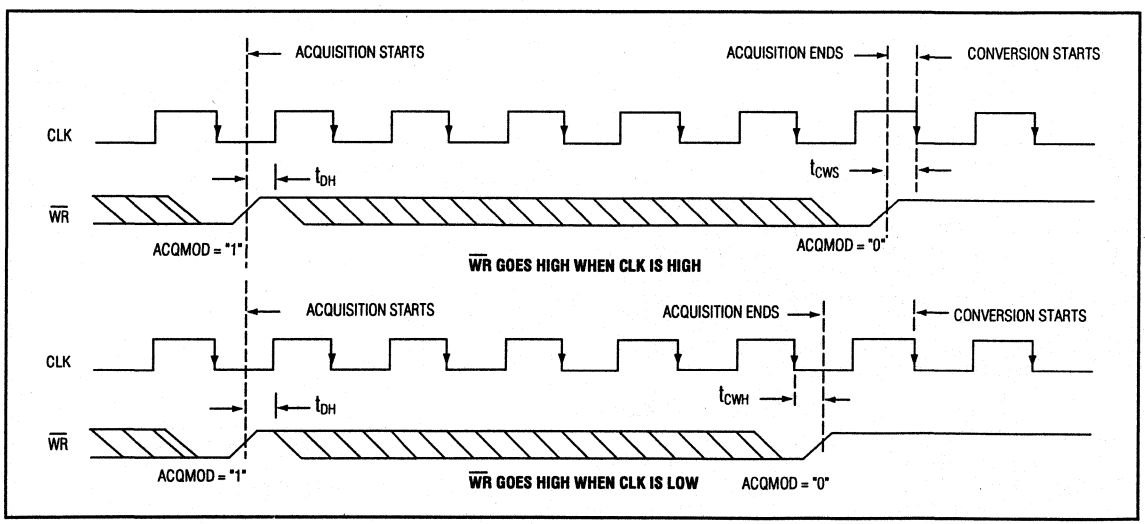


Figure 8b. External Clock and $\overline{WR}$ Timing (External Acquisition Mode)

Multi-Range (±10V, ±5V, +10V, +5V), Single +5V, 12-Bit DAS with 8+4 Bus Interface

Applications Information

Power-On Reset

At power-up, the internal power-supply circuitry sets $\overline{INT}$ high and puts the device in normal operation/external clock mode. This state is selected to keep the internal clock from loading the external clock driver when the part is used in external clock mode.

Internal or External Reference

The MAX197 can operate with either an internal or an external reference. An external reference can be connected to either the REF pin or to the REFADJ pin (Figure 9).

To use the REF input directly, disable the internal buffer by tying REFADJ to V_{DD}. Using the REFADJ input eliminates the need to buffer the reference externally. When the reference is applied at REFADJ, bypass REFADJ with a 0.01µF capacitor to AGND.

The REFADJ internal buffer gain is trimmed to 1.6384 to provide 4.096V at the REF pin from a 2.5V reference.

Internal Reference

The internally trimmed 2.50V reference is gained through the REFADJ buffer to provide 4.096V at REF. Bypass the REF pin with a 4.7µF capacitor to AGND and the REFADJ pin with a 0.01µF capacitor to AGND. The internal reference voltage is adjustable to ±1.5% (±65 LSBs) with the reference-adjust circuit of Figure 1.

External Reference

At REF and REFADJ, the input impedance is a minimum of 10kΩ for DC currents. During conversions, an external reference at REF must be able to deliver 400µA DC load currents, and must have an output impedance of 10Ω or less. If the reference has higher input impedance or is noisy, bypass it close to the REF pin with a 4.7µF capacitor to AGND.

With an external reference voltage of less than 4.096V at the REF pin or less than 2.5V at the REFADJ pin, the increase in the ratio of the RMS noise to the LSB value (FS / 4096) results in performance degradation (loss of effective bits).

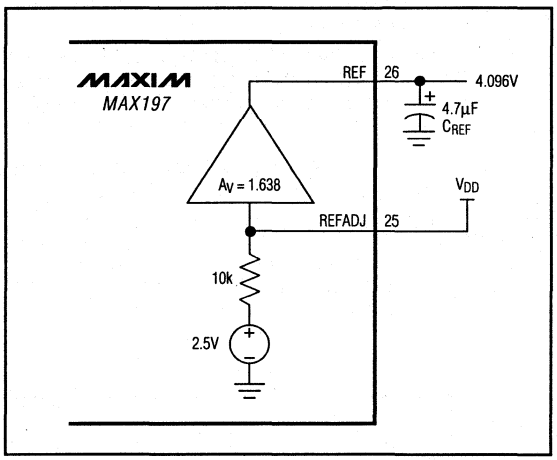


Figure 9b. External Reference, Reference at REF

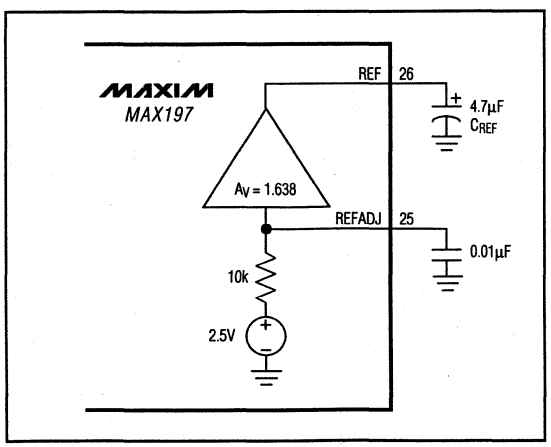


Figure 9a. Internal Reference

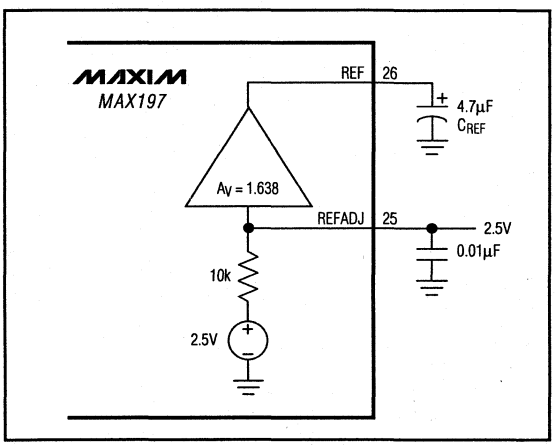


Figure 9c. External Reference, Reference at REFADJ

Multi-Range (±10V, ±5V, +10V, +5V), Single +5V, 12-Bit DAS with 8+4 Bus Interface

Power-Down Mode

To save power, you can put the converter into low-current shutdown mode between conversions. Two programmable power-down modes are available, in addition to a hardware shutdown. Select STBYPD or FULLPD by programming PD0 and PD1 in the input control byte. When software power-down is asserted, it becomes effective only after the end of conversion. In all power-down modes, the interface remains active and conversion results may be read. Input overvoltage protection is active in all power-down modes. The device returns to normal operation on the first $\overline{WR}$ falling edge during write operation.

For hardware-controlled (FULLPD) power-down, pull the $\overline{SHDN}$ pin low. When hardware shutdown is asserted, it becomes effective immediately and the conversion is aborted.

Choosing Power-Down Modes

The bandgap reference and reference buffer remain active in STBYPD mode, maintaining the voltage on the 4.7µF capacitor at the REF pin. This is a "DC" state that does not degrade after power-down of any duration. Therefore, you can use any sampling rate with this mode, without regard to start-up delays.

However, in FULLPD mode, only the bandgap reference is active. Connect a 33µF capacitor between REF and AGND to maintain the reference voltage between conversion and to reduce transients when the buffer is enabled and disabled. Throughput rates down to 1ksps can be achieved without allotting extra acquisition time for reference recovery prior to conversion. This allows conversion to begin immediately after power-down ends. If the discharge of the REF capacitor during FULLPD exceeds the desired limits for accuracy (less than a fraction of an LSB), run a STBYPD power-down cycle prior to starting conversions. Take into account that the reference buffer recharges the bypass capacitor at an 80mV/ms slew rate and add 50µs for settling time. Throughput rates of 10ksps offer typical supply currents of 470µA, using the recommended 33µF capacitor value.

Auto-Shutdown

Selecting STBYPD on every conversion automatically shuts the MAX197 down after each conversion without requiring any start-up time on the next conversion.

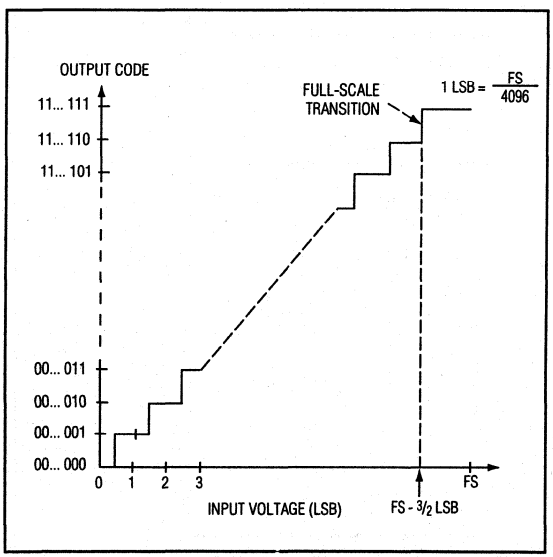


Figure 10. Unipolar Transfer Function

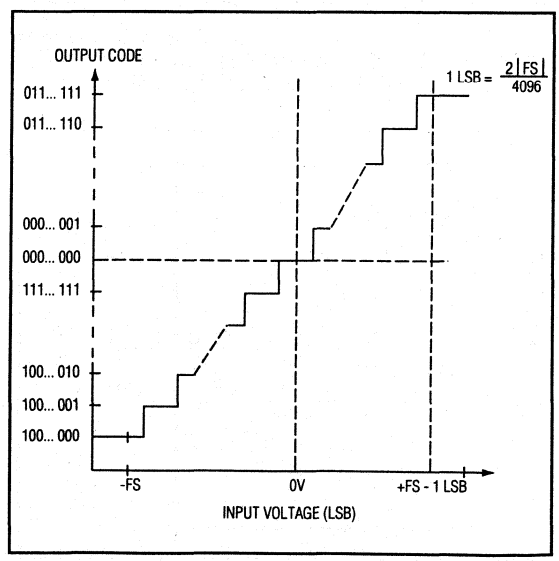


Figure 11. Bipolar Transfer Function

Multi-Range (±10V, ±5V, +10V, +5V), Single +5V, 12-Bit DAS with 8+4 Bus Interface

Transfer Function

Output data coding for the MAX197 is binary in unipolar mode with 1LSB = (FS / 4096) and twos-complement binary in bipolar mode with 1LSB = ((2 x |FS|) / 4096). Code transitions occur halfway between successive-integer LSB values. Figures 10 and 11 show the input/output (I/O) transfer functions for unipolar and bipolar operations, respectively. For full-scale (FS) values, refer to Table 1.

Layout, Grounding, and Bypassing

Careful printed circuit board layout is essential for best system performance. For best performance, use a ground plane. To reduce crosstalk and noise injection, keep analog and digital signals separate. Digital ground lines can run between digital signal lines to minimize interference. Connect analog grounds and DGND in a star configuration to AGND. For noise-free operation, ensure the ground return from AGND to the supply ground is low impedance and as short as possible. Connect the logic grounds directly to the supply ground. Bypass V_{DD} with 0.1µF and 4.7µF capacitors to AGND to minimize high- and low-frequency fluctuations. If the supply is excessively noisy, connect a 5Ω resistor between the supply and V_{DD}, as shown in Figure 12.

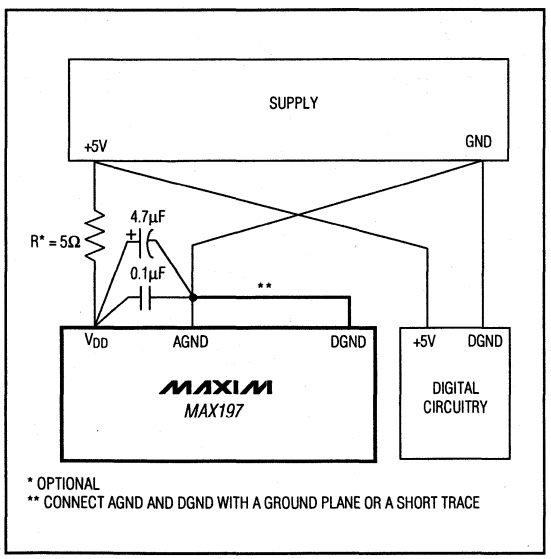


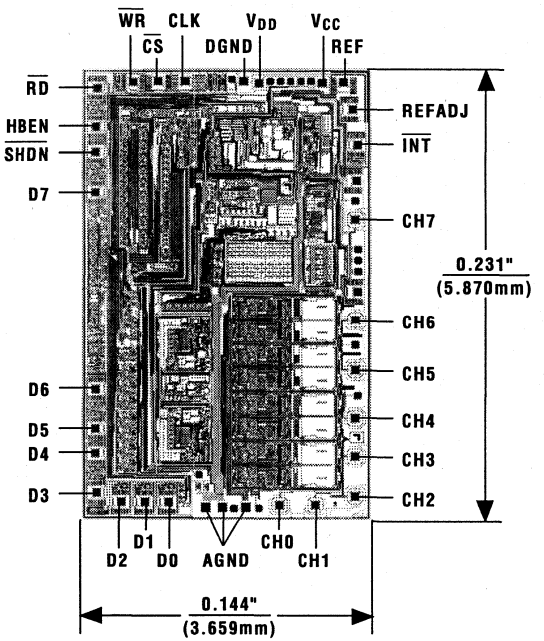
Figure 12. Power-Supply Grounding Connection

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX197AENI	-40°C to +85°C	28 Narrow Plastic DIP
MAX197BENI	-40°C to +85°C	28 Narrow Plastic DIP
MAX197AEWI	-40°C to +85°C	28 Wide SO
MAX197BEWI	-40°C to +85°C	28 Wide SO
MAX197AEAI	-40°C to +85°C	28 SSOP
MAX197BEAI	-40°C to +85°C	28 SSOP
MAX197AMYI	-55°C to +125°C	28 Narrow Ceramic SB**
MAX197BMYI	-55°C to +125°C	28 Narrow Ceramic SB**

*** Contact factory for availability and processing to MIL-STD-883.*

Chip Topography

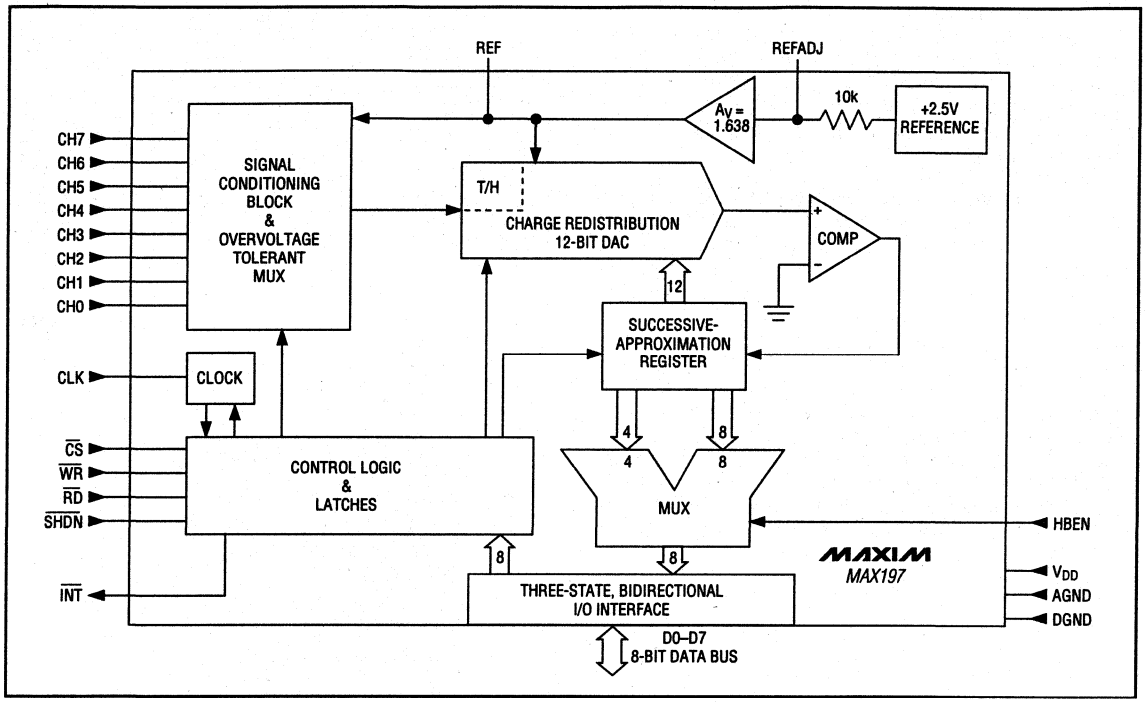


TRANSISTOR COUNT: 2956

SUBSTRATE CONNECTED TO GND

Multi-Range (±10V, ±5V, +10V, +5V), Single +5V, 12-Bit DAS with 8+4 Bus Interface

Functional Diagram



ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
11/96

MAXIM

Low-Power, 60Msps/90Msps, Dual 6-Bit ADCs

General Description

The MAX1002/MAX1003 are dual, 6-bit analog-to-digital converters (ADCs) that combine high-speed, low-power operation with a user-selectable input full-scale range, an on-chip reference, and a clock oscillator. The ADCs convert two analog input signals into two 6-bit offset-binary-coded digital outputs at sampling rates up to 90Msps (MAX1003), while achieving integral nonlinearity (INL) and differential nonlinearity (DNL) of less than ±1/2LSB. The ability to directly interface with baseband I and Q signals makes these parts ideal for use in direct-broadcast satellite, quadrature phase-shift keying (QPSK), demodulation, and similar applications.

The MAX1002/MAX1003 input amplifiers feature true differential inputs, a -0.5dB analog bandwidth of 50MHz, and user-programmable input full-scale ranges of 125mVp-p, 250mVp-p, or 500mVp-p. With an AC-coupled input signal, matching performance between input channels is better than 0.2dB gain, 1/2LSB offset, and 1° phase. Resolution is 5.8 effective bits with a 20MHz analog input signals or 5.7 effective bits with a 50MHz input signal.

The MAX1002 operates with a single +5V power supply and provides TTL-compatible digital outputs, while the MAX1003 operates with +5V analog and +3.3V digital supplies for easy interfacing to +3.3V-logic-compatible digital signal processors and microprocessors. Both devices are available in a 36-pin SSOP package.

Features

- ♦ **Two Matched 6-Bit ADCs**
- ♦ **High Sampling Rates:**
  90Msps per ADC (MAX1003)
  60Msps per ADC (MAX1002)
- ♦ **Low Power Dissipation: 375mW**
- ♦ **High Effective Bits (ENOB) Performance:**
  5.8 ENOB with 20MHz Analog Input
  5.7 ENOB with 50MHz Analog Input
- ♦ **±1/2LSB Maximum INL and DNL**
- ♦ **Internal Voltage Reference**
- ♦ **On-Board Oscillator (may be overdriven)**
- ♦ **50MHz (-0.5dB) Bandwidth Input Amplifiers with True Differential Inputs**
- ♦ **User-Selectable Full-Scale Range (125mVp-p, 250mVp-p, or 500mVp-p)**
- ♦ **0.2dB Channel-to-Channel Gain Matching**
- ♦ **1/2LSB Channel-to-Channel Offset Matching**
- ♦ **Single-Ended or Differential Input Drive**
- ♦ **Flexible Digital Outputs:**
  +3.3V CMOS-Compatible (MAX1003)
  TTL-Compatible (MAX1002)

Applications

Direct-Broadcast Satellite (DBS) Receivers
Cable Set-Top Boxes
VSAT Receivers
Wireless Local Area Networks (WLAN)

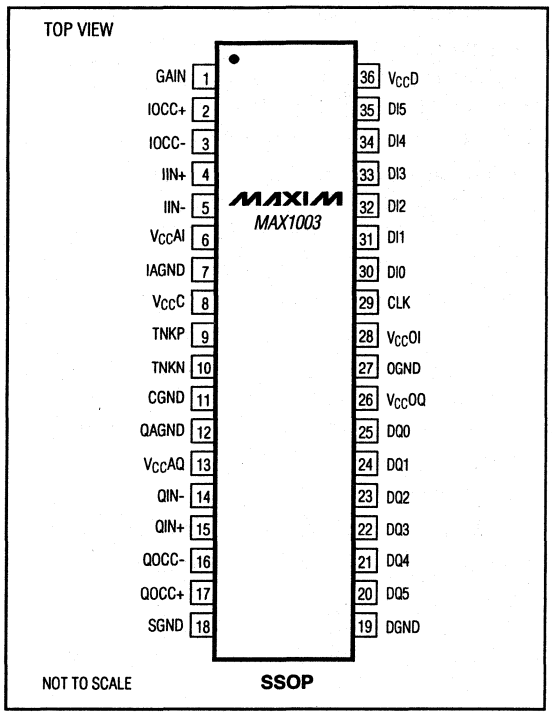
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1002CAX	0°C to +70°C	36 SSOP
MAX1003CAX	0°C to +70°C	36 SSOP

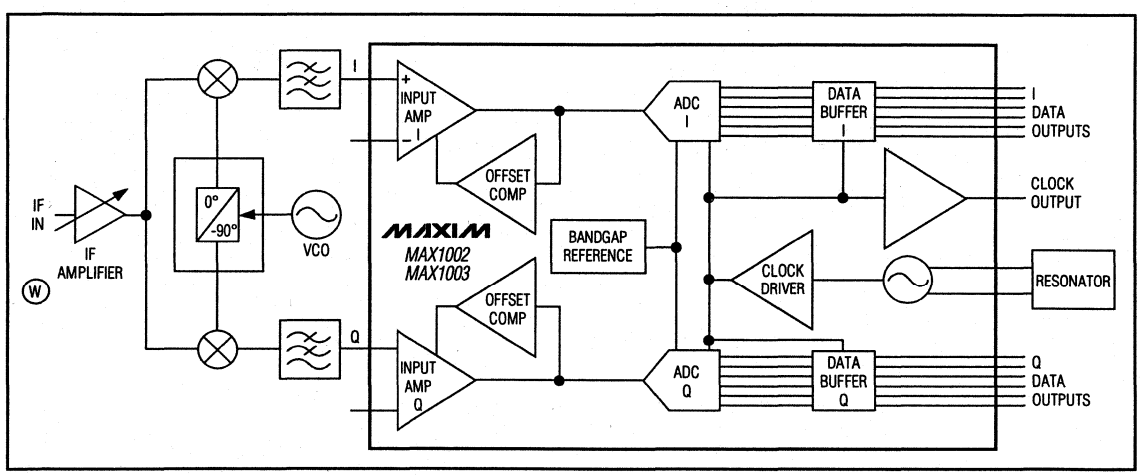
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Low-Power, 60Msps/90Msps, Dual 6-Bit ADCs

Pin Configuration



Typical Application Circuit



ADVANCE INFORMATION

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11/96

MAXIM

+2.7V, Low-Power, 4/8-Channel, 8-Bit ADCs with Serial Interface

General Description

The MAX1110/MAX1111 are complete, low-power, multichannel, 8-bit analog-to-digital converters (ADCs) that feature an internal track/hold, clock, and reference, as well as a serial interface. They operate with a single +2.7V to +5.5V supply, and require only 250µA while sampling at rates up to 50ksps. The MAX1110 is an 8-channel ADC, while the MAX1111 is a 4-channel ADC. The analog inputs are software configurable for unipolar/bipolar and single-ended/differential operation.

The 4-wire serial interface is compatible with SPI™/QSPI™ and Microwire™ interface standards. A serial strobe output allows direct connection to TMS320-family digital signal processors. The MAX1110/MAX1111 use either the internal clock or an external serial-interface clock to perform successive-approximation conversions. Their three-level $\overline{SHDN}$ pin disables the internal voltage reference when driven high, allowing the use of an external reference.

In addition to the hard-wired $\overline{SHDN}$ pin, the devices provide a software-selectable power-down mode. Accessing the serial interface automatically powers up the devices. The quick turn-on time allows the MAX1110/MAX111 to be shut down between conversions, reducing power dissipation below 30µW at slower sampling rates.

The MAX1110 is available in 20-pin DIP and SSOP packages, and the MAX1111 is available in a 16-pin DIP and QSOP packages.

Applications

Portable Instruments

Medical Equipment

Sensor-Based Systems

Remote Systems

Power Management

Solar-Powered Data Acquisition

Features

- **8-Channel Single-Ended or 4-Channel Differential Inputs (MAX1110)**

  4-Channel Single-Ended or 2-Channel Differential Inputs (MAX1111)
- **Single +2.7V to +5.5V Supply**
- **Low Power: 250µA Operating Current**
  2µA Power-Down Current
- **Internal Track/Hold, 50ksps Sampling Rate**
- **Internal 2.048V Reference**
- **SPI/QSPI/Microwire/TMS320-Compatible Serial Interface**
- **Software-Configurable Unipolar or Bipolar Inputs**
- **Small Packages:**
  16-Pin DIP/QSOP (MAX1111)
  20-Pin DIP/SSOP (MAX1110)

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1110CPP	0°C to +70°C	20 Plastic DIP
MAX1110CAP	0°C to +70°C	20 SSOP
MAX1110C/D	0°C to +70°C	Dice*
MAX1110EPP	-40°C to +85°C	20 Plastic DIP
MAX1110EAP	-40°C to +85°C	20 SSOP
MAX1110MJP	-55°C to +125°C	20 CERDIP**
MAX1111CPE	0°C to +70°C	16 Plastic DIP
MAX1111CEE	0°C to +70°C	16 QSOP
MAX1111C/D	0°C to +70°C	Dice*
MAX1111EPE	-40°C to +85°C	16 Plastic DIP
MAX1111EEE	-40°C to +85°C	16 QSOP
MAX1111MJE	-55°C to +125°C	16 CERDIP**

**Dice are specified at T_A = +25°C, DC parameters only.*

***Contact factory for availability.*

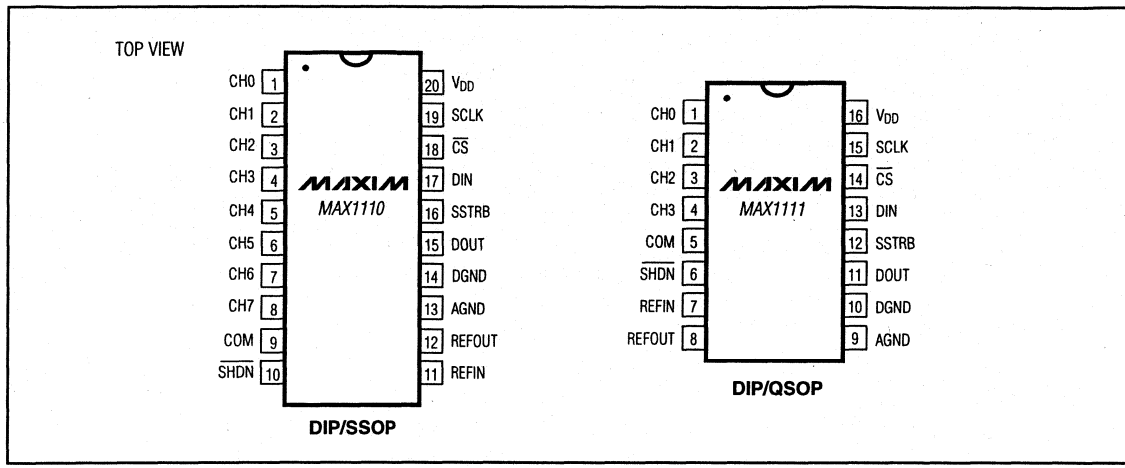
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Microwire is a registered trademark of National Semiconductor Corp.

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+2.7V, Low-Power, 4/8-Channel, 8-Bit ADCs with Serial Interface

Pin Configurations



ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
11/96

MAXIM

+5V, Low-Power, 4/8-Channel, 8-Bit ADCs with Serial Interface

General Description

The MAX1112/MAX1113 are complete, low-power, multichannel, 8-bit analog-to-digital converters (ADCs) that feature an internal track/hold, clock, and reference, as well as a serial interface. They operate with a single +5V supply, and require only 250µA while sampling at rates up to 50ksps. The MAX1112 is an 8-channel ADC, while the MAX1113 is a 4-channel ADC. The analog inputs are software configurable for unipolar/bipolar and single-ended/differential operation.

The 4-wire serial interface is compatible with SPI™/QSPI™ and Microwire™ interface standards. A serial strobe output allows direct connection to TMS320-family digital signal processors. The MAX1112/MAX1113 use either the internal clock or an external serial-interface clock to perform successive-approximation conversions. Their three-level $\overline{SHDN}$ pin disables the internal voltage reference when driven high, allowing the use of an external reference.

In addition to the hard-wired $\overline{SHDN}$ pin, the devices provide a software-selectable power-down mode. Accessing the serial interface automatically powers up the devices. The quick turn-on time allows the MAX1112/MAX1113 to be shut down between conversions, reducing power dissipation below 50µW at slower sampling rates.

The MAX1112 is available in 20-pin DIP and SSOP packages, and the MAX1113 is available in a 16-pin DIP and QSOP packages.

Applications

Portable Instruments
Medical Equipment
Sensor-Based Systems
Remote Systems
Power Management
Solar-Powered Data Acquisition

Features

- **8-Channel Single-Ended or 4-Channel Differential Inputs (MAX1112)**
  4-Channel Single-Ended or 2-Channel Differential Inputs (MAX1113)
- **Single +5V Supply**
- **Low Power: 250µA Operating Current**
  2µA Power-Down Current
- **Internal Track/Hold, 50ksps Sampling Rate**
- **Internal 4.096V Reference**
- **SPI/QSPI/Microwire/TMS320-Compatible Serial Interface**
- **Software-Configurable Unipolar or Bipolar Inputs**
- **Small Packages:**
  16-Pin DIP/QSOP (MAX1113)
  20-Pin DIP/ SSOP (MAX1112)

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1112CPP	0°C to +70°C	20 Plastic DIP
MAX1112CAP	0°C to +70°C	20 SSOP
MAX1112C/D	0°C to +70°C	Dice*
MAX1112EPP	-40°C to +85°C	20 Plastic DIP
MAX1112EAP	-40°C to +85°C	20 SSOP
MAX1112MJP	-55°C to +125°C	20 CERDIP**
MAX1113CPE	0°C to +70°C	16 Plastic DIP
MAX1113CEE	0°C to +70°C	16 QSOP
MAX1113C/D	0°C to +70°C	Dice*
MAX1113EPE	-40°C to +85°C	16 Plastic DIP
MAX1113EEE	-40°C to +85°C	16 QSOP
MAX1113MJE	-55°C to +125°C	16 CERDIP**

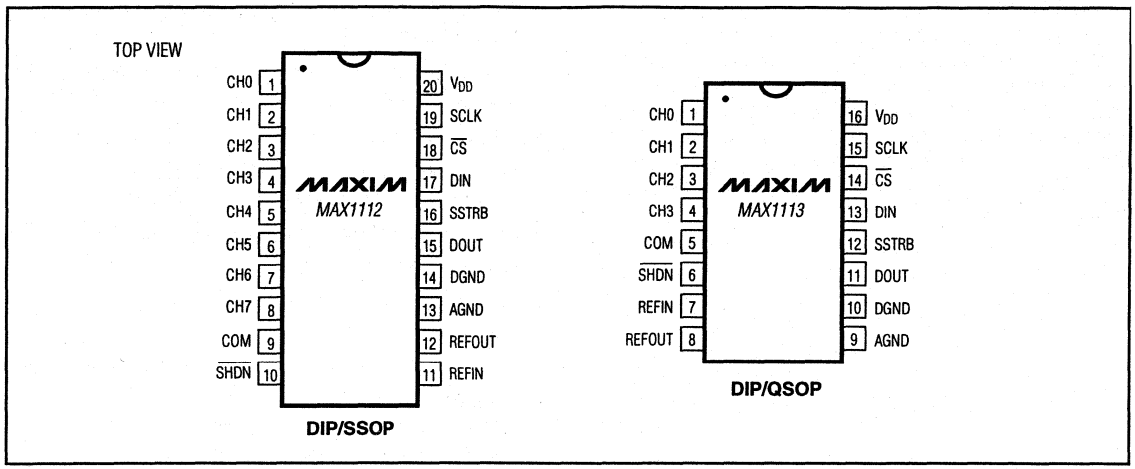
**Dice are specified at T_A = +25°C, DC parameters only.*
***Contact factory for availability.*

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+5V, Low-Power, 4/8-Channel, 8-Bit ADCs with Serial Interface

Pin Configurations



19-1101; Rev 0; 6/96

EVALUATION KIT AVAILABLE

MAXIM

8-Bit, 150Msps Flash ADC

General Description

The MAX1114 is a monolithic, flash analog-to-digital converter (ADC) that can digitize a 2V analog input signal into 8-bit digital words at a typical 150Msps update rate.

For most applications, no external sample-and-hold is required for accurate conversion due to the device's narrow aperture time, wide bandwidth, and low input capacitance. A single standard -5.2V power supply is required to operate the MAX1114, with nominal 2.2W power dissipation. A special decoding scheme reduces metastable errors to 1LSB.

The part is packaged in a 42-pin ceramic sidebraze that is pin-compatible with the CX20116 and CXA1396D. The surface-mount 44-pin CERQUAD allows access to additional reference ladder taps, an overrange bit, and a data-ready output. For higher conversion rates, the pin-compatible 300Msps MAX1125 is available.

Applications

Digital Oscilloscopes

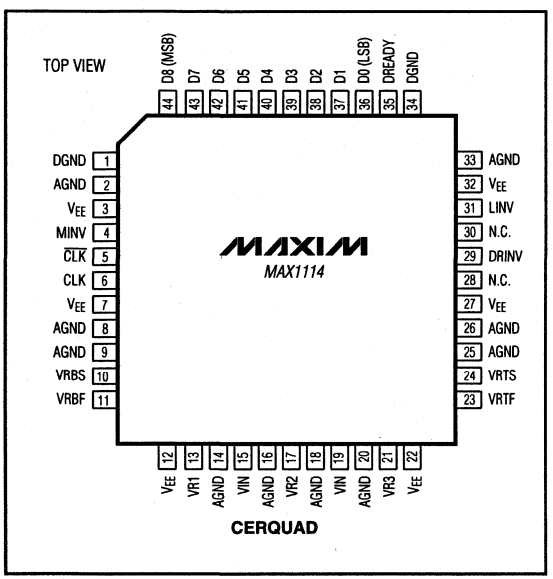
Transient Capture

Radar, EW, ECM

Direct RF Down-Conversion

Medical Electronics
Ultrasound, CAT Instrumentation

Pin Configurations



Features

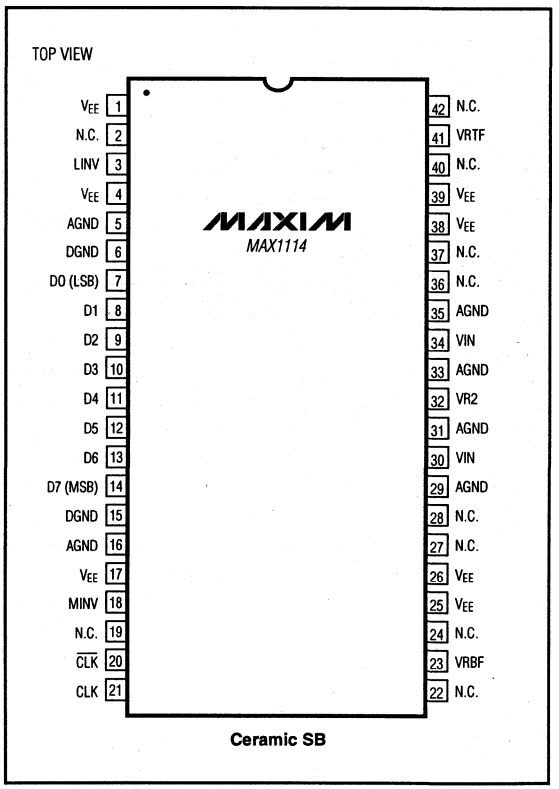
- ♦ Metastable Errors Reduced to 1LSB
- ♦ 10pF Input Capacitance
- ♦ 210MHz Input Bandwidth
- ♦ 150Msps Conversion Rate
- ♦ 2.2W Typical Power Dissipation
- ♦ Single -5.2V Supply

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSBs)
MAX1114AIDO	-20°C to +85°C	42 Ceramic SB	±0.75
MAX1114BIDO	-20°C to +85°C	42 Ceramic SB	±1
MAX1114AIBH	-20°C to +85°C	44 CERQUAD	±0.75
MAX1114BIBH	-20°C to +85°C	44 CERQUAD	±1

Functional Diagram appears at end of data sheet.

Pin Configurations (continued)



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8-Bit, 150Msps Flash ADC

ABSOLUTE MAXIMUM RATINGS

Negative Supply Voltage (V_{EE} TO GND) .....-7.0V to +0.5V
Ground Voltage Differential .....-0.5V to +0.5V
Analog Input Voltage .....V_{EE} to +0.5V
Reference Input Voltage .....V_{EE} to +0.5V
Digital Input Voltage.....V_{EE} to +0.5V
Reference Current V_{RTF} to V_{RBF}.....25mA

Digital Output Current .....0mA to -30mA
Operating Temperature Range .....-25°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec). .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, R_{SOURCE} = 50Ω, VRBF = -2.00V, VR2 = -1.00V, VRTF = 0.00V, f_{CLK} = 150MHz, 50% Duty Cycle, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	TEST LEVEL	MAX1114A			MAX1114B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
DC ACCURACY									
Integral Linearity	f_{CLK} = 100 kHz	VI	-0.75	±0.60	+0.75	-0.95	±0.80	+0.95	LSB
Differential Linearity	f_{CLK} = 100 kHz	VI	-0.75		+0.75	-0.95		+0.95	LSB
No missing codes			Guaranteed			Guaranteed			
ANALOG INPUT									
Offset Error VRT		IV	-30		+30	-30		+30	mV
Offset Error VRB		IV	-30		+30	-30		+30	mV
Input Voltage Range		VI	-2.0		0.0	-2.0		0.0	V
Input Capacitance	Over full input range	V		10			10		pF
Input Resistance		V		15			15		kΩ
Input Current		VI		250	500		250	500	µA
Input Slew Rate		V		1,000			1,000		V/µs
Large-Signal Bandwidth	VIN = full scale	V		210			210		MHz
Small-Signal Bandwidth	IN = 500mVp-p	V		335			335		MHz
REFERENCE INPUT									
Ladder Resistance		VI	100	200	300	100	200	300	Ω
Reference Bandwidth		V		10			10		MHz
TIMING CHARACTERISTICS									
Maximum Sample Rate		VI	125	150		125	150		Msps
Clock to Data Delay		V		2.4			2.4		ns
Output Delay Tempco		V		2			2		ps/°C
CLK-to-Data Ready Delay (t_D)		V		2.0			2.0		ns
Aperture Jitter		V		5			5		ps
Acquisition Time		V		1.5			1.5		ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{EE} = -5.2V, R_{SOURCE} = 50Ω, VRBF = -2.00V, VR2 = -1.00V, VRTF = 0.00V, f_{CLK} = 150MHz, 50% Duty Cycle, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	TEST LEVEL	MAX1114A MIN	MAX1114A TYP	MAX1114A MAX	MAX1114B MIN	MAX1114B TYP	MAX1114B MAX	UNITS
DYNAMIC PERFORMANCE									
Signal-to-Noise Ratio	f_{IN} = 3.58MHz	VI	46	48		45	47		dB
	f_{IN} = 50MHz	VI	42	46		40	44		
Total Harmonic Distortion	f_{IN} = 3.58MHz	VI	-48	-52		-46	-50		dB
	f_{IN} = 50MHz	VI	-40	-44		-39	-43		
Signal-to-Noise and Distortion (SINAD)	f_{IN} = 3.58MHz	VI	45	48		43	46		dB
	f_{IN} = 50MHz	VI	39	42		37	40		
DIGITAL INPUTS									
Digital Input High Voltage (MINV, LINV)		VI	-1.1		-0.7	-1.1		-0.7	V
Digital Input Low Voltage (MINV, LINV)		VI	-2.0		-1.5	-2.0		-1.5	V
Clock Synchronous Input Currents		V		40			40		µA
Clock Low Width, T_{PWL}		VI	4	3		4	3		ns
Clock High Width, T_{PWH}		VI	4	3		4	3		ns
DIGITAL OUTPUTS									
Digital Output High Voltage	50Ω to -2V	VI	-1.1			-1.1			V
Digital Output Low Voltage	50Ω to -2V	VI			-1.5			-1.5	V
POWER SUPPLY REQUIREMENTS									
Supply Current	T_A = +25°C	I		425	550		425	550	mA
Power Dissipation	T_A = +25°C	I		2.2	2.9		2.2	2.9	W

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed; therefore, $T_j = T_C = T_A$.

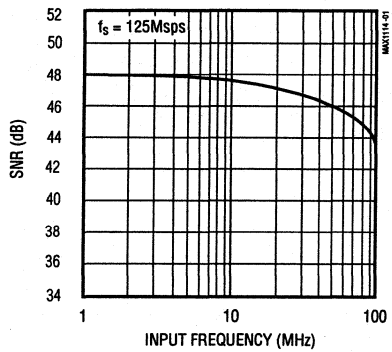
TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = +25°C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = +25°C. Parameter is guaranteed over specified temperature range.

8-Bit, 150Msps Flash ADC

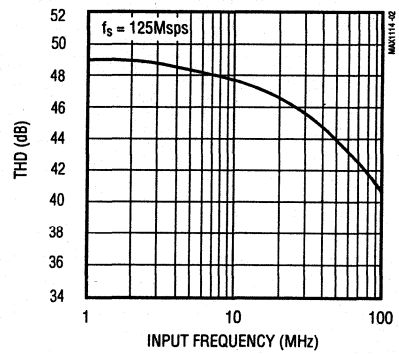
Typical Operating Characteristics

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

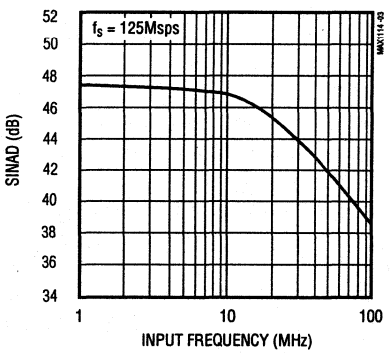
SIGNAL-TO-NOISE RATIO vs. INPUT FREQUENCY



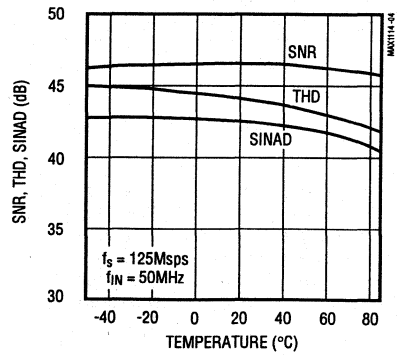
TOTAL HARMONIC DISTORTION vs. INPUT FREQUENCY



SIGNAL-TO-NOISE AND DISTORTION vs. INPUT FREQUENCY



SNR, THD, SINAD vs. TEMPERATURE



Pin Description

PIN		NAME	FUNCTION
Ceramic SB	CERQUAD		
1, 4, 17, 25, 26, 38, 39	3, 7, 12, 22, 27, 32	V_{EE}	Negative Analog Supply (nominally -5.2V)
2, 19, 22, 24, 27, 28, 36, 37, 40, 42	28, 30	N.C.	No Connect. Not internally connected.
3	31	LINV	D0–D6 Output Conversion Control
5, 16, 29, 31, 33, 35	2, 8, 9, 14, 16, 18, 20, 25, 26, 33	AGND	Analog Ground
6, 15	1, 34	DGND	Digital Ground
7	36	D0	Digital Data Output (LSB)
8–13	37–42	D1–D6	Digital Data Outputs
14	43	D7	Digital Data Output (MSB)
18	4	MINV	D7 Output Conversion Control
—	44	D8	Overrange Output
20	5	$\overline{CLK}$	Inverse ECL Clock Input Pin
21	6	CLK	ECL Clock Input Pin
—	10	VRBS	Reference Voltage Bottom, Sense
23	11	VRBF	Reference Voltage Bottom, Force
30, 34	15, 19	VIN	Analog Input. Can be connected to the input signal or used as a sense.
—	13	VR1	Reference Voltage Tap 1 (typically -1.5V)
32	17	VR2	Reference Voltage Tap 2 (typically -1V)
—	21	VR3	Reference Voltage Tap 3 (typically -0.5V)
41	23	VRTF	Reference Voltage Top, Force
—	24	VRTS	Reference Voltage Top, Sense
—	29	DRINV	Data-Ready Inverse
—	35	DREADY	Data-Ready Output

Detailed Description

The MAX1114 is a 150Msps, monolithic, 8-bit parallel flash analog-to-digital converter (ADC) with an analog bandwidth of over 200MHz. A major advance over previous flash converters is the inclusion of 256 input preamplifiers between the reference ladder and input comparators. (See *Functional Diagram.*) This feature not only reduces clock-transient kickback to the input and reference ladder due to a low AC beta, but also reduces the effect of the dynamic state of the input signal on the latching characteristics of the input comparators. The preamplifiers act as buffers and stabilize the input capacitance so it remains constant for varying input voltages and frequencies, making the part easier to drive than previous flash converters. The MAX1114 incorporates a special decoding scheme that reduces metastable errors (sparkle codes or flyers) to a maximum of 1LSB.

8-Bit, 150Msps Flash ADC

The MAX1114 has true differential analog and digital data paths from the preamplifiers to the output buffers (Current-Mode Logic) for reducing potential missing codes while rejecting common-mode noise.

Careful layout of the analog circuitry reduces signature errors. Every comparator has a clock buffer to reduce differential delays and to improve signal-to-noise ratio. The output drive capability of the device can provide full ECL swings into 50Ω loads.

Typical Interface Circuit

Figure 1 shows the typical interface circuit. The MAX1114 is relatively easy to apply, depending on the accuracy needed. Wire-wrap may be employed with careful point-to-point ground connections if desired, but a double-sided PC board with a ground plane on the component side, separated into digital and analog sections gives the best performance. The converter is bonded-out to place the digital pins on the left side of the package and the analog pins on the right side. Additionally, an RF bead connection through a single point from the analog to digital ground planes reduces ground noise pickup.

Figure 2 (CERQUAD package only) shows the most elaborate method of achieving the least error by correcting for integral nonlinearity, input-induced distortion, and power-supply/ground noise. It uses external reference ladder tap connections, an input buffer, and supply decoupling. The function of each pin and external connections to other components is as follows:

V_{EE}, AGND, DGND

V_{EE} is the supply pin with AGND as ground for the device. The power-supply pins should be bypassed as close to the device as possible with at least a 0.01µF ceramic capacitor. A 1µF tantalum should also be used for low-frequency suppression. DGND is the ground for the ECL outputs and should be referenced to the output pulldown voltage and bypassed as shown in Figure 1.

Analog Input VIN

There are two analog input pins that are tied to the same point internally. Either one may be used as an analog input sense and the other for input force. This is convenient for testing the source signal to see if there is sufficient drive capability. The pins can also be tied together and driven by the same source. The MAX1114 is superior to similar devices due to a preamplifier stage before the comparators (Figure 4). This makes the device easier to drive because it has constant capacitance and induces less slew-rate distortion. An optional input buffer may be used.

Clock Inputs CLK, $\overline{CLK}$

The clock inputs are designed to be driven differentially with ECL levels. The clock may be driven single-ended since $\overline{CLK}$ is internally biased to -1.3V (Figure 5). $\overline{CLK}$ may be left open but a 0.01µF bypass capacitor from $\overline{CLK}$ to AGND is recommended. NOTE: System performance may be degraded due to increased clock noise or jitter.

Output Logic Control MINV, LINV

These are ECL-compatible digital controls for changing the output code from straight binary to two's complement, etc. (Table 1 and Figure 4). Both MINV and LINV are in the logic low (0) state when they are left open. The high state can be obtained by tying to AGND through a diode or 3.9kΩ resistor.

Table 1. Output Coding

MINV / LINV	0 / 0	0 / 1	1 / 0	1 / 1
0V	111...11	100...00	011...11	000...00
.	111...10	100...01	011...10	000...01
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
V_{IN} .	100...00	111...11	000...00	011...11
.	011...11	000...00	111...11	100...00
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
.	000...01	011...10	100...01	111...10
-2V	000...00	011...11	100...00	111...11

1: V_{IH}, V_{OH} 0: V_{IL}, V_{OL}

Digital Outputs D0 to D7

The digital outputs can drive ECL levels into 50Ω when pulled down to -2V. When pulled down to -5.2V, the outputs can drive 150Ω to 1kΩ loads.

Reference Inputs VRBF, VR2, VRTF

There are two reference inputs and one external reference voltage tap. These are -2V (VRBF), mid-tap (VR2) and AGND (VRTF). The reference pins can be driven as shown in Figure 1. VR2 should be bypassed to AGND for further noise suppression.

Reference Inputs VRBF, VRBS, VR1, VR2, VR3, VRTF, VRTS (CERQUAD package only)

These are five external reference voltage taps from -2V (VRBF) to AGND (VRTF) which can be used to control integral linearity over temperature. The taps can be driven by op amps (Figure 2). These voltage level inputs can be bypassed to AGND for further noise suppression, if so desired. VRB and VRT have force and sense pins for monitoring the top and bottom voltage references.

Not Connected (N.C.)

All N.C. pins should be tied to DGND on the left side of the package and to AGND on the right side of the package.

Data Ready and Data-Ready Inverse DREADY, DRINV (CERQUAD package only)

The data-ready pin is a flag that goes high or low at the output when data is valid or ready to be received. It is essentially a delay line that accounts for the time necessary for information to be clocked through the MAX1114's decoders and latches. This function is useful for interfacing with high-speed memory. Using the data-ready output to latch the output data ensures minimum setup and hold times. DRINV is a data-ready inverse control pin (Figure 3).

Overrange Input D8 (CERQUAD package only)

When the MAX1114 is in an overrange condition, D8 goes high and all data outputs go high as well. This makes it possible to include the MAX1114 in higher resolution systems.

Operation

The MAX1114 has 256 preamp/comparator pairs that are each supplied with the voltage from VRTF to VRBF divided equally by the resistive ladder as shown in the *Functional Diagram*. This voltage is applied to the positive input of each preamplifier/comparator pair. An analog input voltage applied at VIN is connected to the negative inputs of each preamplifier/comparator pair. The comparator states are then clocked through each comparator's individual clock buffer. When CLK is low, the master, or input stage, of the comparators compares the analog input voltage to the respective reference voltage. When CLK changes from low to high, the comparators are latched to the state prior to the clock transition and output logic codes in sequence from the top comparators, closest to VRTF (0V), down to the point where the magnitude of the input signal changes sign (thermometer code). The output of each comparator is then registered into four 64-to-6 bit decoders when CLK is changed from high to low. At the decoders' output is a set of four 7-bit latches that are enabled (track) when CLK changes from high to low. From here, the outputs of the latches are coded into 6 LSBs from 4 columns and 4 columns are coded into 2 MSBs. Next are the MINV and LINV controls for output inversions that consist of a set of eight XOR gates. Finally, 8 ECL output latches and buffers are used to drive the external loads. The conversion takes one clock cycle from the input to the data outputs.

Evaluation Boards

The MAX1114/MAX1125 evaluation kit (EV kit) demonstrates the full performance of the MAX1114. This board includes a voltage reference circuit, clock driver circuit, output data latches and an on-board reconstruction of the digital data. A separate EV kit manual describing the operation of this board is also available. Contact the factory for price and delivery.

8-Bit, 150Msps Flash ADC

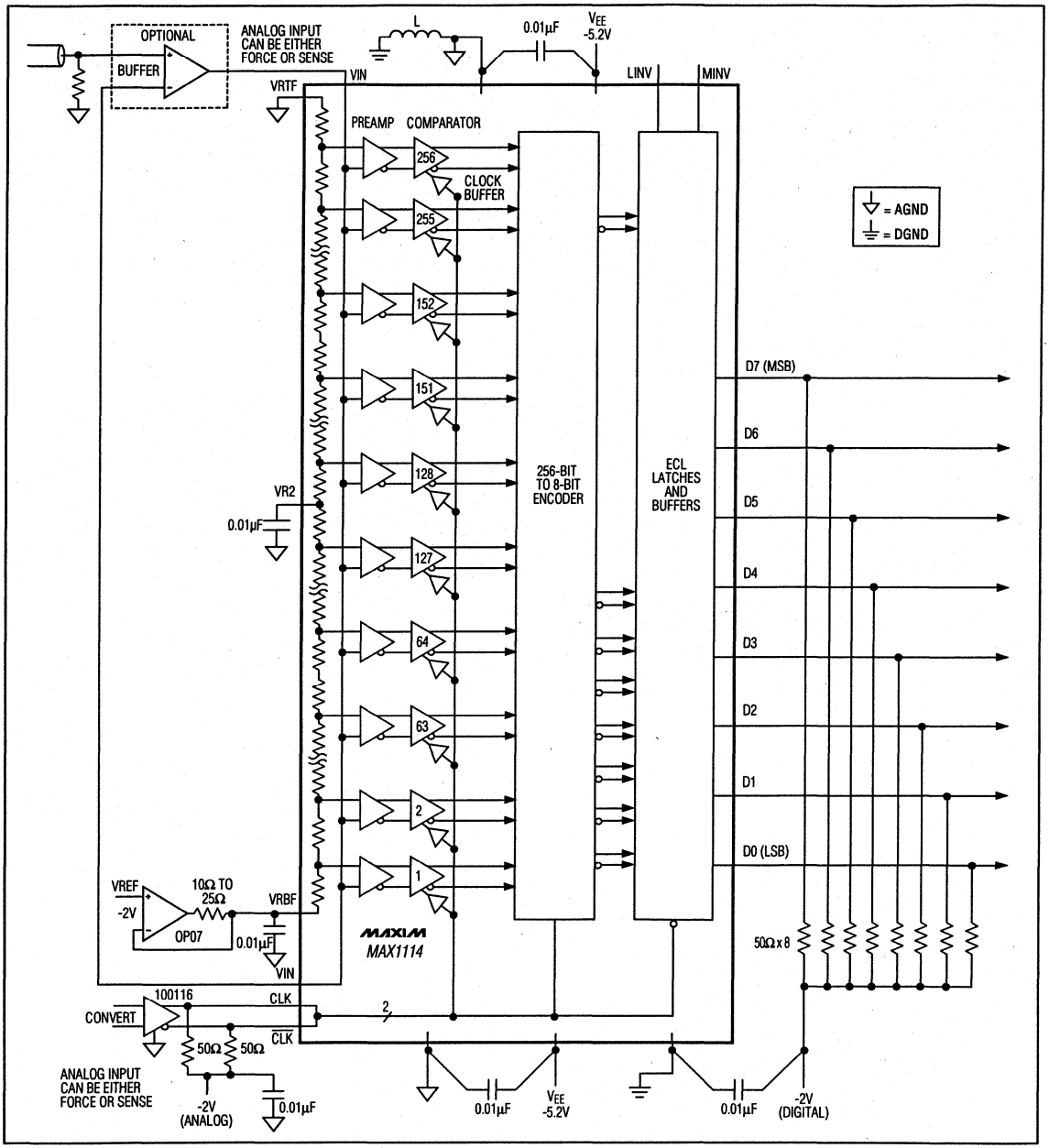


Figure 1. Typical Interface Circuit 1

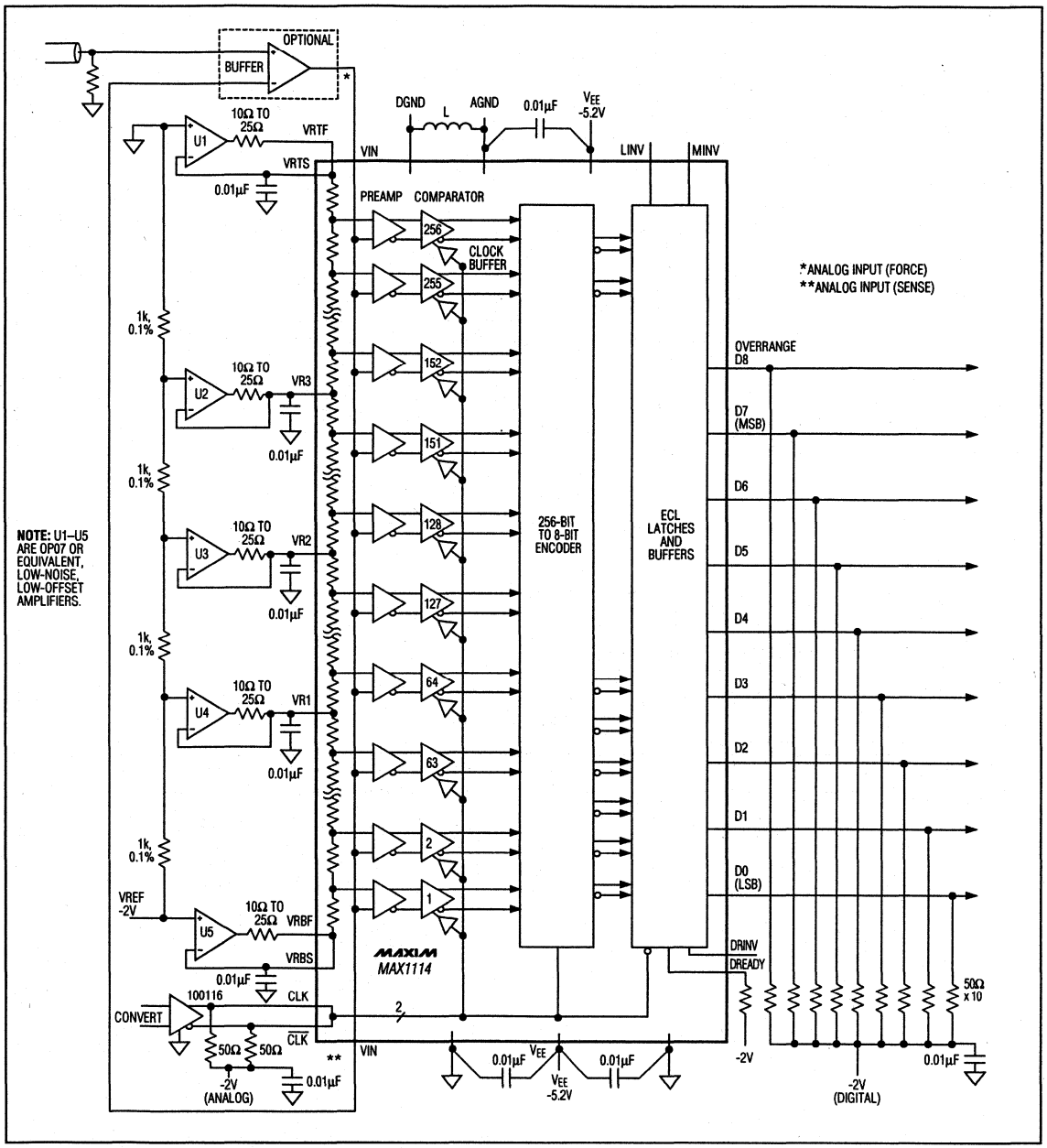


Figure 2. Typical Interface Circuit 2 (CERQUAD package only)

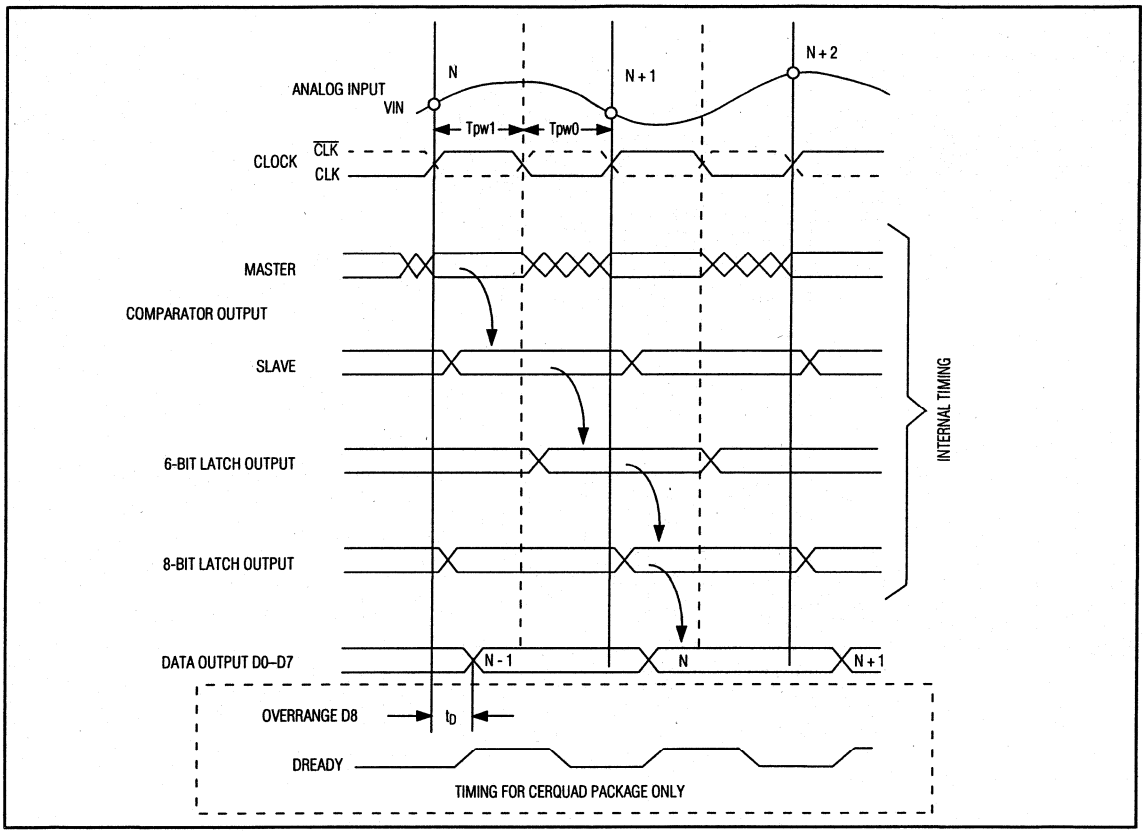


Figure 3. Timing Diagram

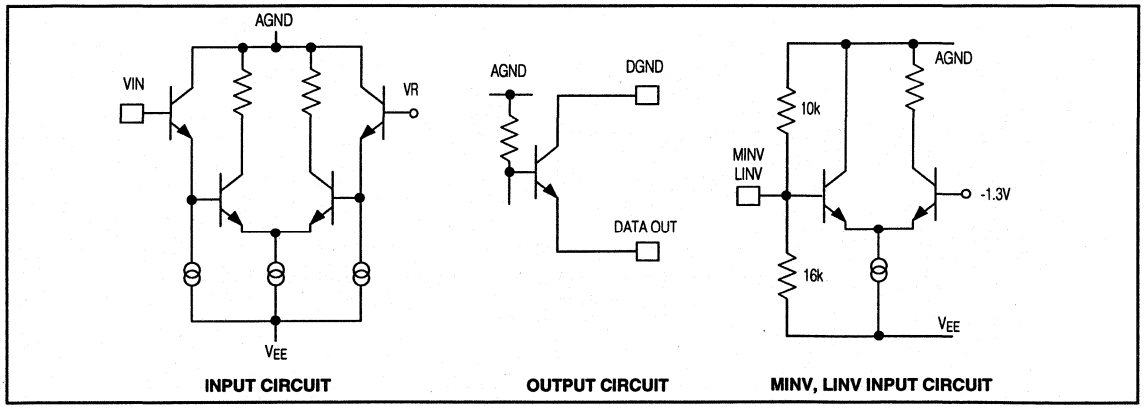


Figure 4. Subcircuit Schematics

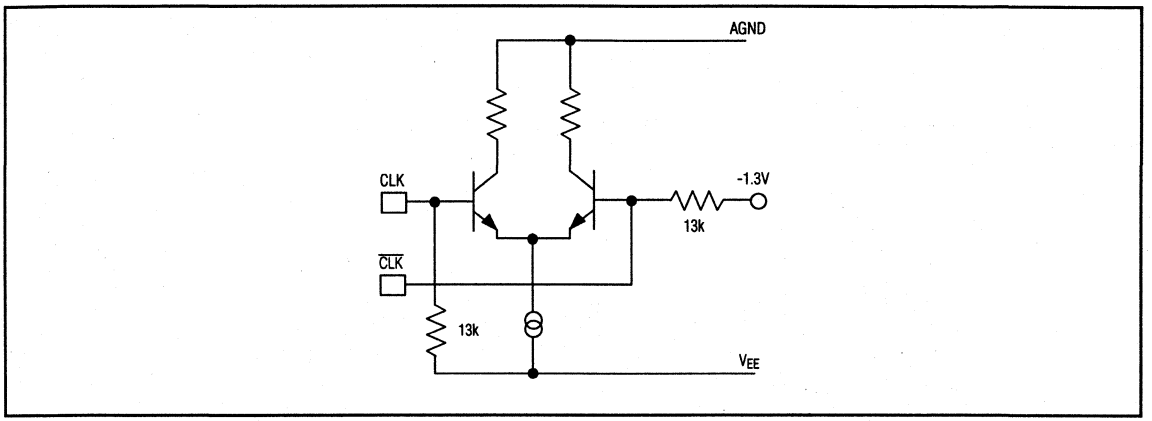


Figure 5. Clock Input

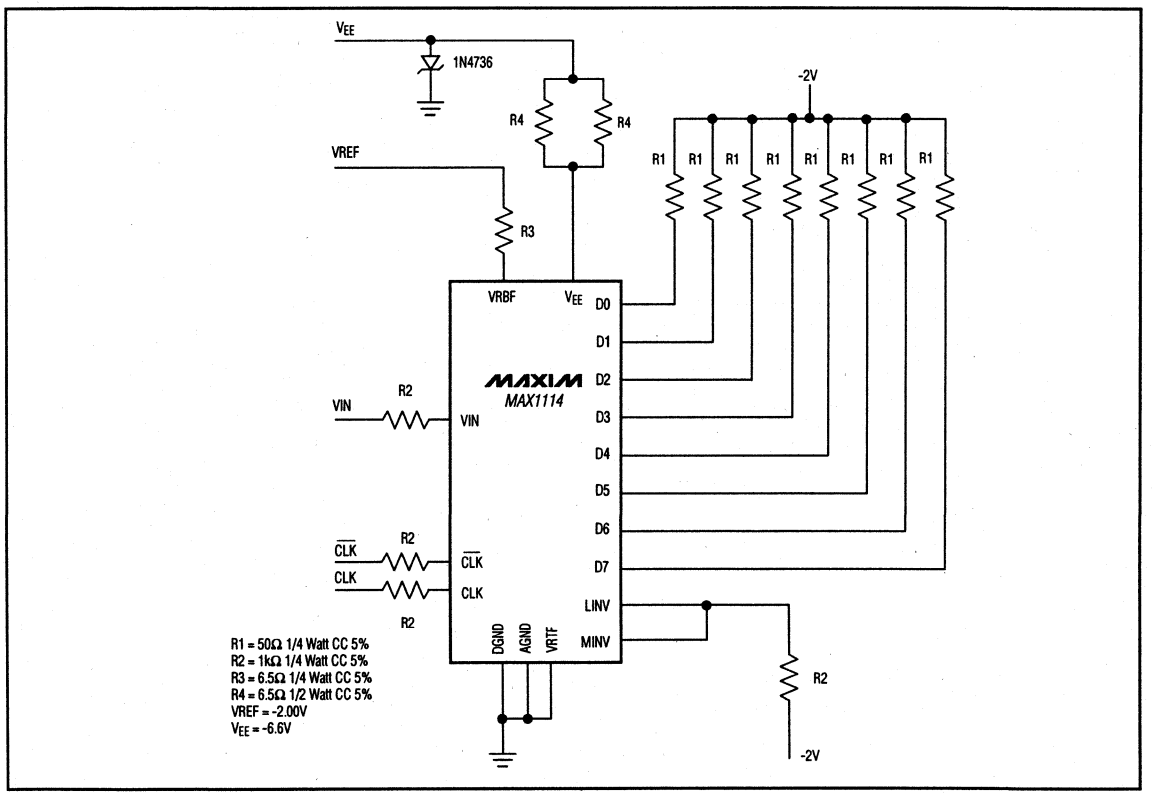
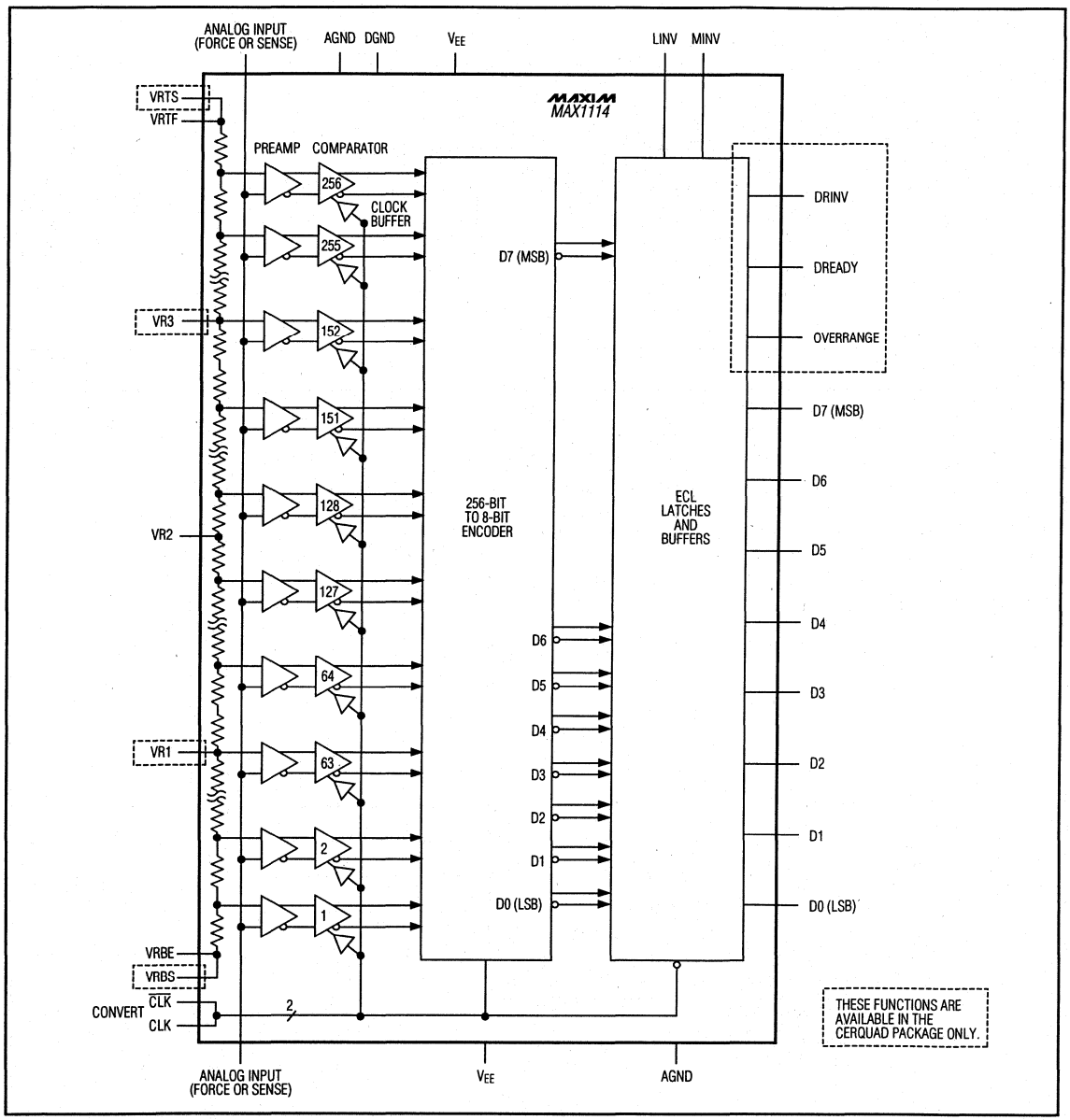


Figure 6. Burn-In Circuit (Ceramic SB package only)

8-Bit, 150Msps Flash ADC

Functional Diagram



19-1100; Rev 0; 6/96

EVALUATION KIT AVAILABLE

MAXIM
8-Bit, 300Msps Flash ADC

General Description

The MAX1125 is a monolithic, flash analog-to-digital converter (ADC) capable of digitizing a 2V analog input signal into 8-bit digital words at a typical 300Msps update rate.

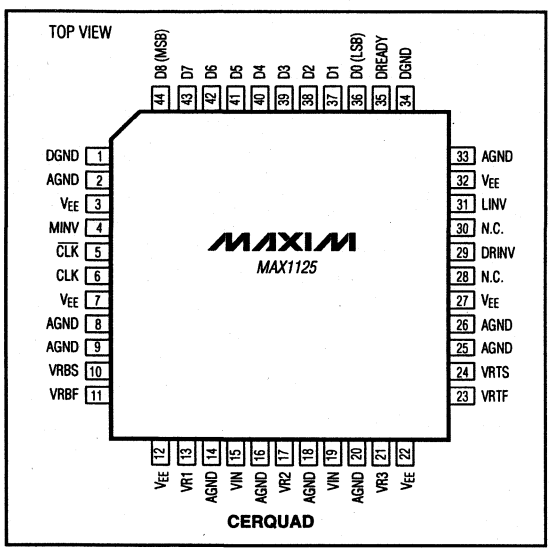
For most applications, no external sample-and-hold is required for accurate conversion due to the device's narrow aperture time, wide bandwidth, and low input capacitance. A single standard -5.2V power supply is required to operate the MAX1125, with nominal 2.2W power dissipation. A special decoding scheme reduces metastable errors to 1LSB.

The part is packaged in a 42-pin ceramic sidebraze. The surface-mount 44-pin CERQUAD package allows access to additional reference ladder taps, an over-range bit, and a data-ready output. The pin- compatible 150Msps MAX1114 is also available.

Applications

Digital Oscilloscopes
Transient Capture
Radar, EW, ECM
Direct RF Down-Conversion
Medical Electronics
Ultrasound, CAT Instrumentation

Pin Configurations



Features

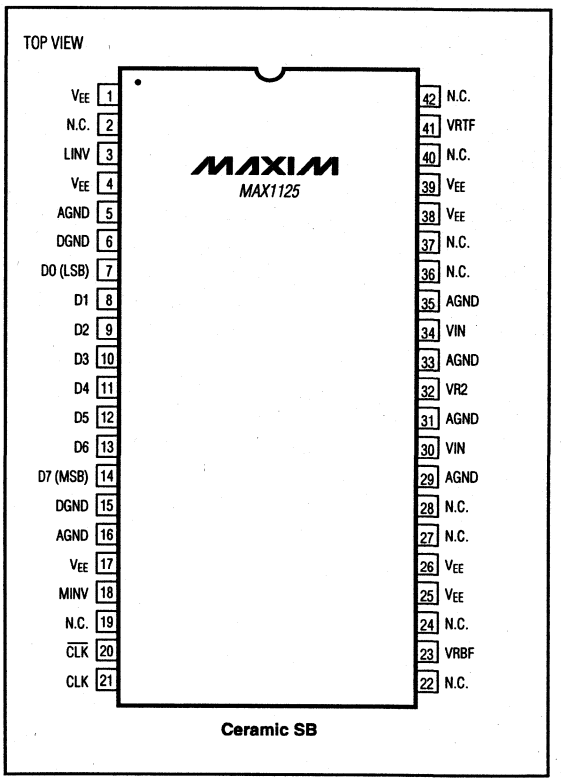
- ♦ Metastable Errors Reduced to 1LSB
- ♦ 10pF Input Capacitance
- ♦ 210MHz Input Bandwidth
- ♦ 300Msps Conversion Rate
- ♦ 2.2W Typical Power Dissipation
- ♦ Single -5.2V Supply

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSBs)
MAX1125AIDO	-20°C to +85°C	42 Ceramic SB	±0.75
MAX1125BIDO	-20°C to +85°C	42 Ceramic SB	±1
MAX1125AIBH	-20°C to +85°C	44 CERQUAD	±0.75
MAX1125BIBH	-20°C to +85°C	44 CERQUAD	±1

Functional Diagram appears at end of data sheet.

Pin Configurations (continued)



7

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

8-Bit, 300Msps Flash ADC

ABSOLUTE MAXIMUM RATINGS

Negative Supply Voltage (V_{EE} TO GND) .....-7.0V to +0.5V
Ground Voltage Differential .....-0.5V to +0.5V
Analog Input Voltage .....V_{EE} to +0.5V
Reference Input Voltage .....V_{EE} to +0.5V
Digital Input Voltage .....V_{EE} to +0.5V
Reference Current V_{RTF} to V_{RBF} 25mA

Digital Output Current .....0mA to -30mA
Operating Temperature Range .....-25°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec). .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, R_{SOURCE} = 50Ω, VRBF = -2.00V, VR2 = -1.00V, VRTF = 0.00V, f_{CLK} = 150MHz, 50% Duty Cycle, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	TEST LEVEL	MAX1125A			MAX1125B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
DC ACCURACY									
Integral Linearity		VI	-0.75	±0.60	+0.75	-0.95	±0.80	+0.95	LSB
Differential Linearity		VI	-0.75		+0.75	-0.95		+0.95	LSB
No Missing Codes			Guaranteed			Guaranteed			
ANALOG INPUT									
Offset Error V_{RT}		IV	-30		+30	-30		+30	mV
Offset Error V_{RB}		IV	-30		+30	-30		+30	mV
Input Voltage Range		VI	-2.0		0.0	-2.0		0.0	V
Input Capacitance	Over full input range	V		10			10		pF
Input Resistance		V		15			15		kΩ
Input Current		VI		250	500		250	500	µA
Input Slew Rate		V		1,000			1,000		V/µs
Large Signal Bandwidth	VIN = full scale	V		210			210		MHz
Small Signal Bandwidth	IN = 500mVp-p	V		335			335		MHz
REFERENCE INPUT									
Ladder Resistance		VI	100	200	300	100	200	300	Ω
Reference Bandwidth		V		10			10		MHz
TIMING CHARACTERISTICS									
Maximum Sample Rate		VI	250	300		250	300		Msps
Clock to Data Delay		V		2.4			2.4		ns
Output Delay TEMPCO		V		2			2		ps/°C
CLK-to-Data Ready Delay (t_D)		V		2.0			2.0		ns
Aperture Jitter		V		5			5		ps
Acquisition Time		V		1.5			1.5		ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{EE} = -5.2V, R_{SOURCE} = 50Ω, VRBF = -2.00V, VR2 = -1.00V, VRTF = 0.00V, f_{CLK} = 150MHz, 50% Duty Cycle, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	TEST LEVEL	MAX1114A MIN	MAX1114A TYP	MAX1114A MAX	MAX1114B MIN	MAX1114B TYP	MAX1114B MAX	UNITS
DYNAMIC PERFORMANCE									
Signal-to-Noise Ratio	f_{IN} = 3.58MHz	VI	45	47		44	46		dB
	f_{IN} = 100MHz	VI	39	42		38	41		
Total Harmonic Distortion	f_{IN} = 3.58MHz	VI	-48	-52		-46	-50		dB
	f_{IN} = 100MHz	VI	-40	-43		-39	-42		
Signal-to-Noise and Distortion (SINAD)	f_{IN} = 3.58MHz	VI	44	46		42	44		dB
	f_{IN} = 100MHz	VI	37	39		35	37		
DIGITAL INPUTS									
Digital Input High Voltage (MINV, LINV)		VI	-1.1		-0.7	-1.1		-0.7	V
Digital Input Low Voltage (MINV, LINV)		VI	-2.0		-1.5	-2.0		-1.5	V
Clock Synchronous Input Currents		V		40			40		µA
Clock Low Width, T_{PWL}		VI	2	1.8		2	1.8		ns
Clock High Width, T_{PWH}		VI	2	1.8		2	1.8		ns
DIGITAL OUTPUTS									
Digital Output High Voltage	50Ω to -2V	VI	-1.1			-1.1			V
Digital Output Low Voltage	50Ω to -2V	VI			-1.5			-1.5	V
POWER-SUPPLY REQUIREMENTS									
Supply Current	T_A = +25 °C	I		425	550		425	550	mA
Power Dissipation	T_A = +25 °C	I		2.2	2.9		2.2	2.9	W

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

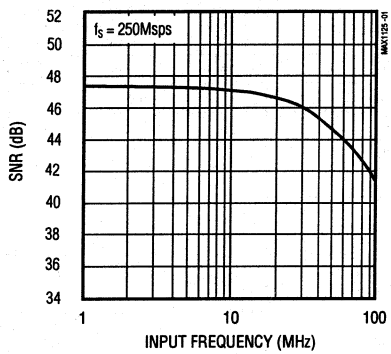
Unless otherwise noted, all tests are pulsed; therefore, T_j = T_C = T_A.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = +25°C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = +25°C. Parameter is guaranteed over specified temperature range.

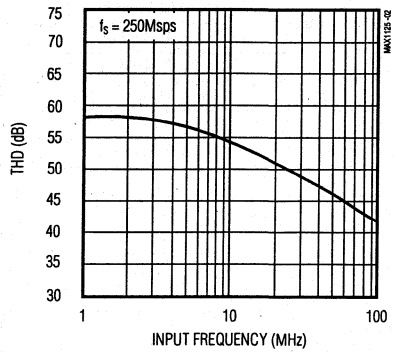
8-Bit, 300Msps Flash ADC

Typical Operating Characteristics

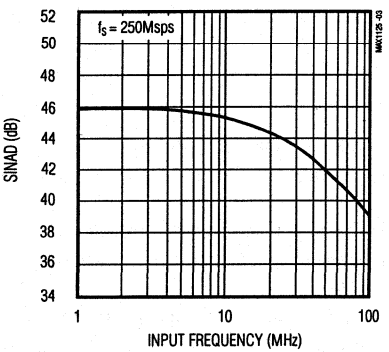
SIGNAL-TO-NOISE RATIO vs. INPUT FREQUENCY



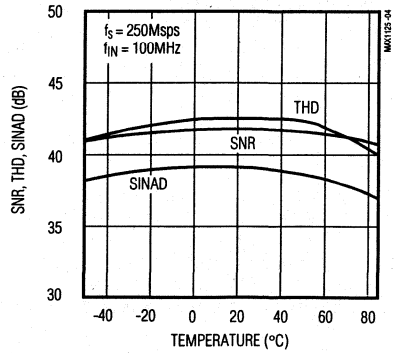
TOTAL HARMONIC DISTORTION vs. INPUT FREQUENCY



SIGNAL-TO-NOISE AND DISTORTION vs. INPUT FREQUENCY



SNR, THD, SINAD vs. TEMPERATURE



Pin Description

PIN		NAME	FUNCTION
Ceramic SB	CERQUAD		
1, 4, 17, 25, 26, 38, 39	3, 7, 12, 22, 27, 32	V_{EE}	Negative Analog Supply (nominally -5.2V)
2, 19, 22, 24, 27, 28, 36, 37, 40, 42	28, 30	N.C.	No Connect. Not internally connected.
3	31	LINV	D0–D6 Output Inversion Control
5, 16, 29, 31, 33, 35	2, 8, 9, 14, 16, 18, 20, 25, 26, 33	AGND	Analog Ground
6, 15	1, 34	DGND	Digital Ground
7	36	D0	Digital Data Output (LSB)
8–13	37–42	D1–D6	Digital Data Output
14	43	D7	Digital Data Output (MSB)
18	4	MINV	D7 Output Inversion Control
—	44	D8	Overrange Output
20	5	$\overline{CLK}$	Inverse ECL Clock Input Pin
21	6	CLK	ECL Clock Input Pin
—	10	VRBS	Reference Voltage Bottom, Sense
23	11	VRBF	Reference Voltage Bottom, Force
30, 34	15, 19	VIN	Analog Input. Can be connected to the input signal or used as a sense.
—	13	VR1	Reference Voltage Tap 1 (typically -1.5V)
32	17	VR2	Reference Voltage Tap 2 (typically -1V)
—	21	VR3	Reference Voltage Tap 3 (typically -0.5V)
41	23	VRTF	Reference Voltage Top, Force
—	24	VRTS	Reference Voltage Top, Sense
—	29	DRINV	Data-Ready Inverse
—	35	DREADY	Data-Ready Output

Detailed Description

The MAX1125 is a 300Msps, monolithic, 8-bit parallel flash analog-to-digital converter (ADC) with an analog bandwidth of over 200MHz. A major advance over previous flash converters is the inclusion of 256 input preamplifiers between the reference ladder and input comparators. (See *Functional Diagram.*) This feature not only reduces clock-transient kickback to the input and reference ladder due to a low AC beta, but also reduces the effect of the dynamic state of the input signal on the latching characteristics of the input comparators. The preamplifiers act as buffers and stabilize the input capacitance so it remains constant for varying input voltages and frequencies, making the part easier to drive than previous flash converters. The MAX1125 incorporates a special decoding scheme that reduces metastable errors (sparkle codes or flyers) to a maximum of 1LSB.

8-Bit, 300Msps Flash ADC

The MAX1125 has true differential analog and digital data paths from the preamplifiers to the output buffers (Current-Mode Logic) for reducing potential missing codes while rejecting common-mode noise.

Careful layout of the analog circuitry reduces signature errors. Every comparator also has a clock buffer to reduce differential delays and to improve signal-to-noise ratio. The output-drive capability of the device can provide full ECL swings into 50Ω loads.

Typical Interface Circuit

Figure 1 shows the typical interface circuit. The MAX1125 is relatively easy to apply depending on the accuracy needed. Wire-wrap may be employed with careful point-to-point ground connections if desired, but a double-sided PC board with a ground plane on the component side, separated into digital and analog sections, gives the best performance. The converter is bonded-out to place the digital pins on the left side of the package and the analog pins on the right side. Additionally, an RF bead connection through a single point from the analog to digital ground planes reduces ground noise pickup.

Figure 2 (CERQUAD package only) shows the most elaborate method of achieving the least error by correcting for integral nonlinearity, input induced distortion, and power-supply/ground noise. It uses external reference ladder tap connections, an input buffer, and supply decoupling. The function of each pin and external connections to other components is as follows:

V_{EE}, AGND, DGND

V_{EE} is the supply pin with AGND as ground for the device. The power-supply pins should be bypassed as close to the device as possible with at least a 0.01µF ceramic capacitor. A 1µF tantalum should also be used for low-frequency suppression. DGND is the ground for the ECL outputs and should be referenced to the output pulldown voltage and bypassed as shown in Figure 1.

Analog Input VIN

There are two analog input pins that are tied to the same point internally. Either one may be used as an analog input sense and the other for input force. This is convenient for testing the source signal to see if there is sufficient drive capability. The pins can also be tied together and driven by the same source. The MAX1125 is superior to similar devices due to a preamplifier stage before the comparators (Figure 4). This makes the device easier to drive because it has constant capacitance and induces less slew-rate distortion. An optional input buffer may be used.

Clock Inputs CLK, $\overline{CLK}$

The clock inputs are designed to be driven differentially with ECL levels. Because $\overline{CLK}$ is internally biased to -1.3V, the clock may be driven single-ended (Figure 5). $\overline{CLK}$ may be left open, but a 0.01µF bypass capacitor from $\overline{CLK}$ to AGND is recommended. NOTE: System performance may be degraded due to increased noise or jitter.

Output Logic Control MINV, LINV

These are ECL-compatible digital controls for changing the output code from straight binary to two's complement, etc. (Table 1 and Figure 4). Both MINV and LINV are in the logic low (0) state when left open. The high state can be obtained by tying to AGND through a diode or 3.9kΩ resistor.

Table 1. Output Coding

MINV LINV	0 0	0 1	1 0	1 1
0V	111...11	100...00	011...11	000...00
.	111...10	100...01	011...10	000...01
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
VIN .	100...00	111...11	000...00	011...11
.	011...11	000...00	111...11	100...00
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
.	000...01	011...10	100...01	111...10
-2V	000...00	011...11	100...00	111...11

1: V_{IH}, V_{OH} 0: V_{IL}, V_{OL}

Digital Outputs D0 to D7

The digital outputs can drive ECL levels into 50Ω when pulled down to -2V. When pulled down to -5.2V, the outputs can drive 150Ω to 1kΩ loads.

Reference Inputs VRBF, VR2, VRTF

There are two reference inputs and one external reference voltage tap. These are -2V (VRBF), mid-tap (VR2) and AGND (VRTF). The reference pins can be driven as shown in Figure 1. VR2 should be bypassed to AGND for further noise suppression.

Reference Inputs VRBF, VRBS, VR1, VR2, VR3, VRTF, VRTS (CERQUAD package only)

These are five external reference voltage taps from -2V (VRBF) to AGND (VRTF) that can be used to control integral linearity over temperature. The taps can be driven by

op amps (Figure 2). These voltage level inputs can be bypassed to AGND for further noise suppression, if so desired. VRB and VRT have force and sense pins for monitoring the top and bottom voltage references.

Not Connected (N.C.)

All N.C. pins should be tied to DGND on the left side of the package and to AGND on the right side of the package.

Data Ready and Data Ready Inverse DREADY, DRINV (CERQUAD package only)

The data-ready pin is a flag that goes high or low at the output when data is valid or ready to be received. It is essentially a delay line that accounts for the time necessary for information to be clocked through the MAX1125's decoders and latches. This function is useful for interfacing with high-speed memory. Using the data-ready output to latch the output data ensures minimum setup and hold times. DRINV is a data-ready inverse control pin (Figure 3).

Overrange Input D8 (CERQUAD package only)

When the MAX1125 is in an overrange state, D8 goes high, and all data outputs go high as well. This makes it possible to include the MAX1125 in higher resolution systems.

Operation

The MAX1125 has 256 preamp/comparator pairs that are each supplied with the voltage from VRTF to VRBF divided equally by the resistive ladder as shown in the *Functional Diagram*. This voltage is applied to the positive input of each preamplifier/comparator pair. An analog input voltage applied at VIN is connected to the negative inputs of each preamplifier/comparator pair. The comparator states are then clocked through each comparator's individual clock buffer. When CLK is low, the comparators' master, or input stage, compares the analog input voltage to the respective reference voltage. When CLK changes from low to high, the comparators are latched to the state prior to the clock transition and output logic codes in sequence from the top comparators, closest to VRTF (0V), down to the point where the magnitude of the input signal changes sign (thermometer code). The output of each comparator is then registered into four 64-to-6 bit decoders when CLK changes from high to low. At the output of the decoders is a set of four 7-bit latches that are enabled (track) when CLK changes from high to low. From here, the outputs of the latches are coded into 6 LSBs from 4 columns and 4 columns are coded into 2 MSBs. Next are the MINV and LINV controls for output inversions that consist of a set of eight XOR gates. Finally, 8 ECL output latches and buffers are used to drive the external loads. The conversion takes one clock cycle from the input to the data outputs.

Evaluation Boards

The MAX1114/MAX1125 evaluation kit (EV kit) demonstrates the full performance of the MAX1125. This board includes a voltage reference circuit, clock driver circuit, output data latches and an on-board reconstruction of the digital data. A separate data sheet describing the operation of this board is also available. Contact the factory for price and delivery.

8-Bit, 300Msps Flash ADC

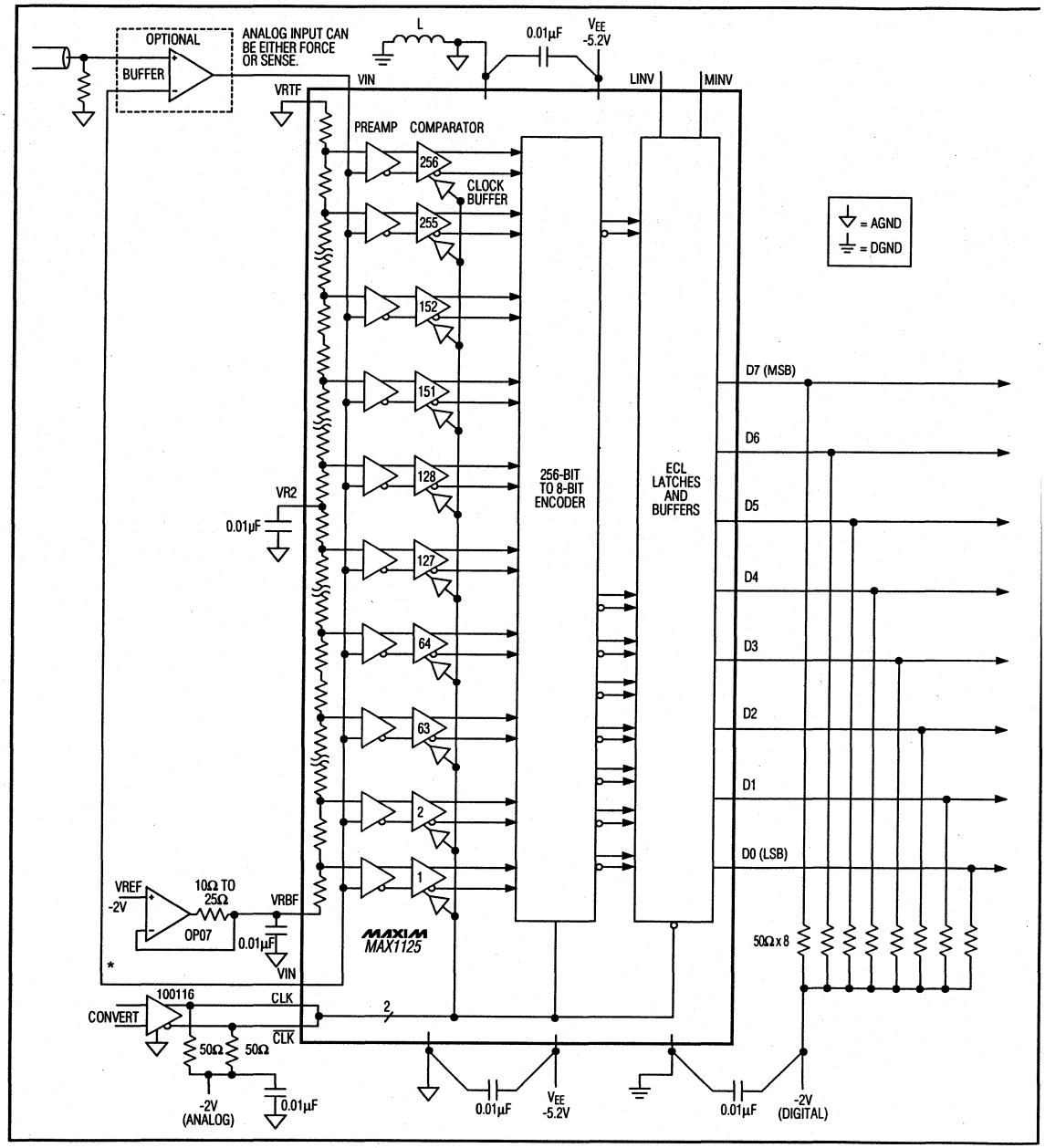


Figure 1. Typical Interface Circuit 1

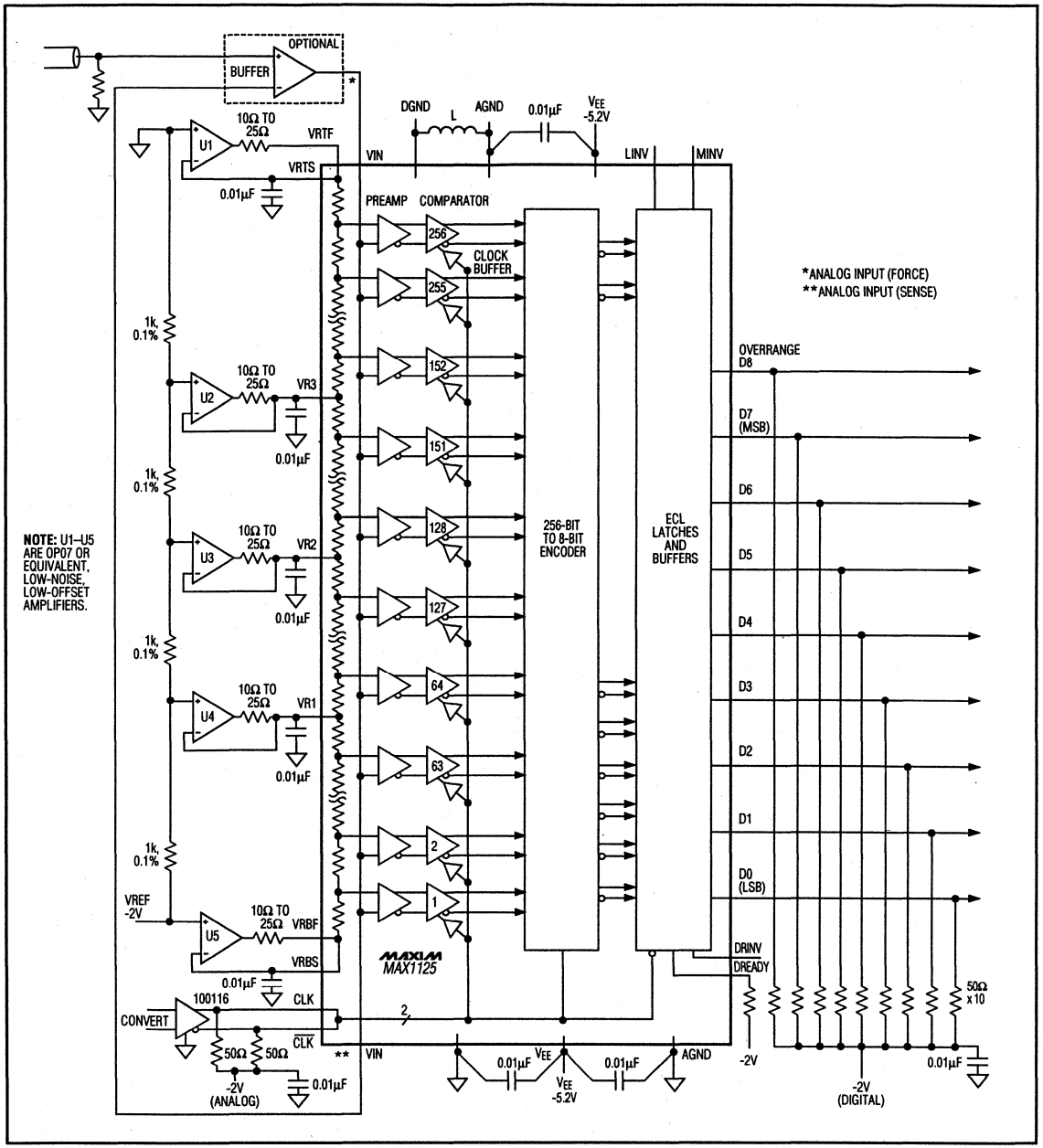


Figure 2. Typical Interface Circuit 2 (CERQUAD package only)

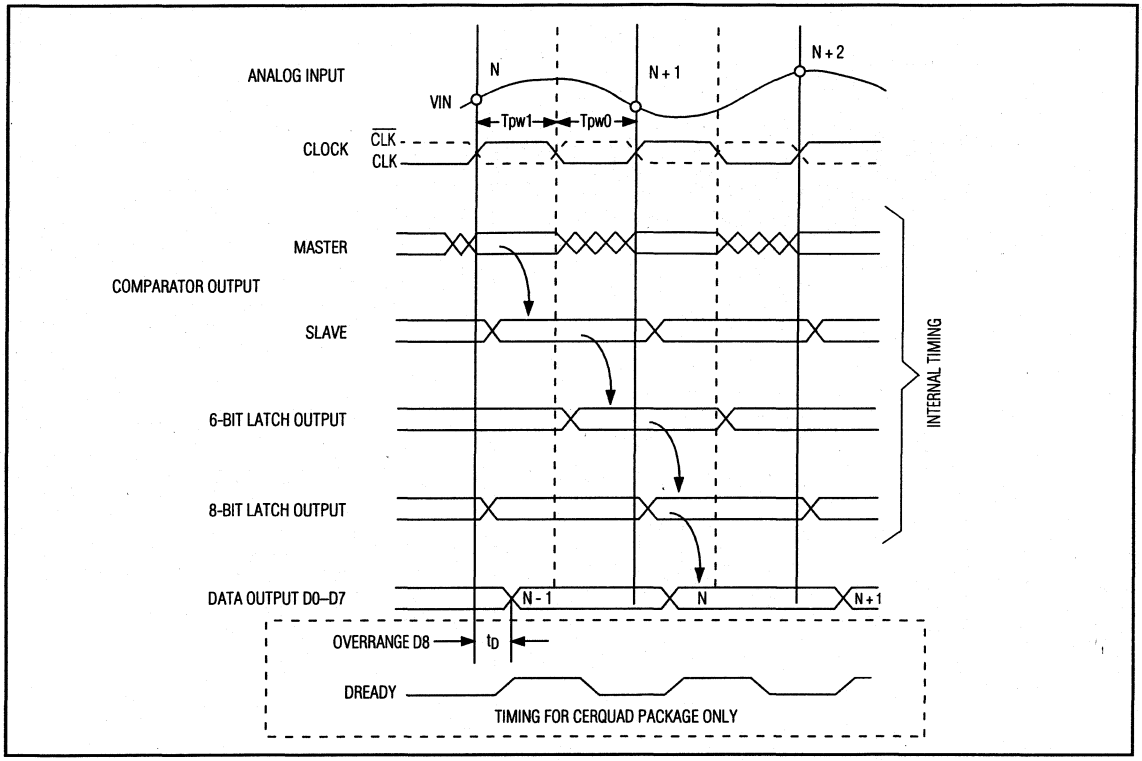


Figure 3. Timing Diagram

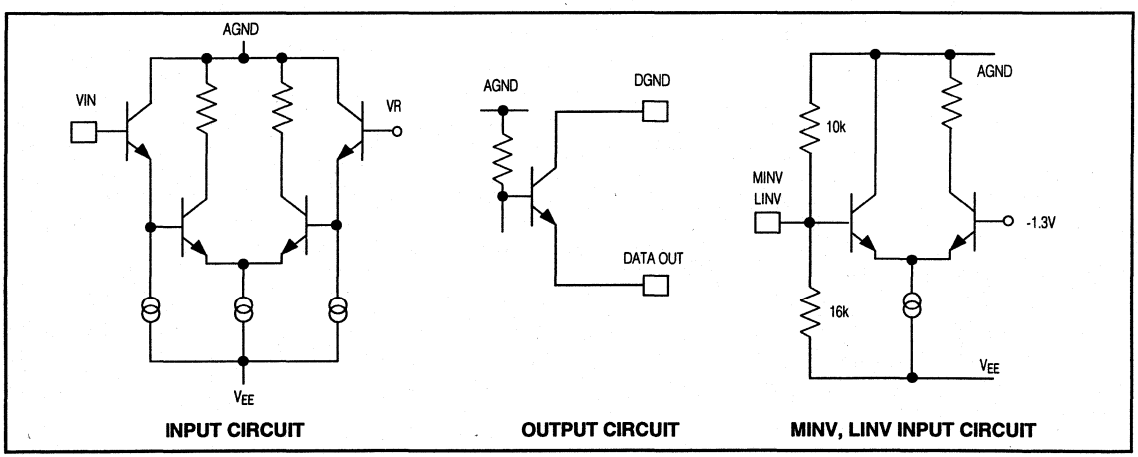


Figure 4. Subcircuit Schematics

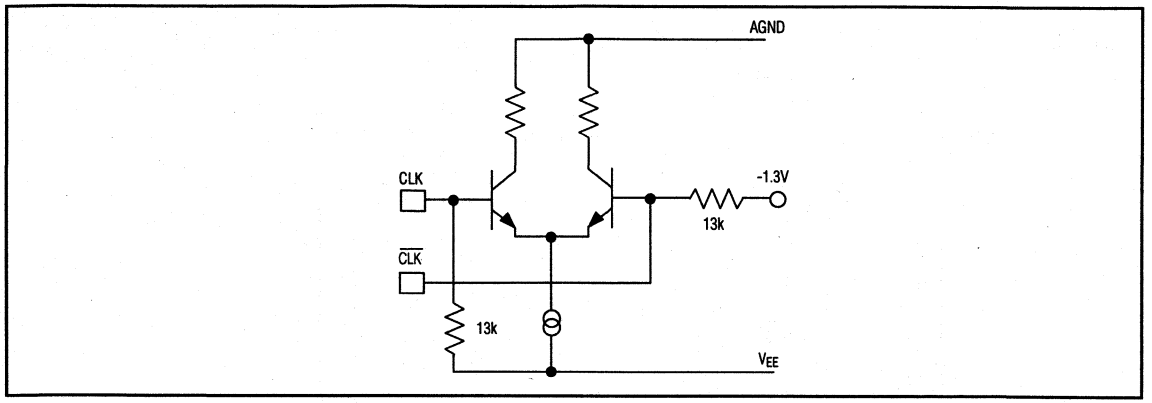


Figure 5. Clock Input

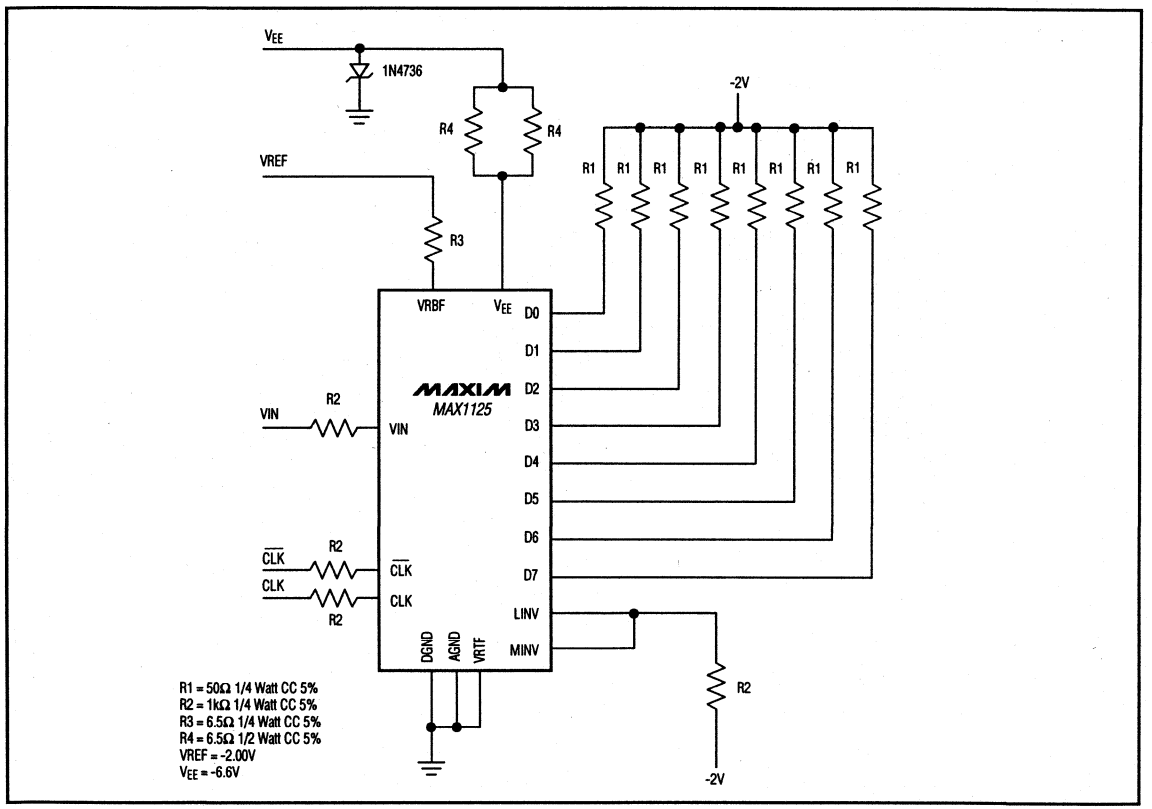
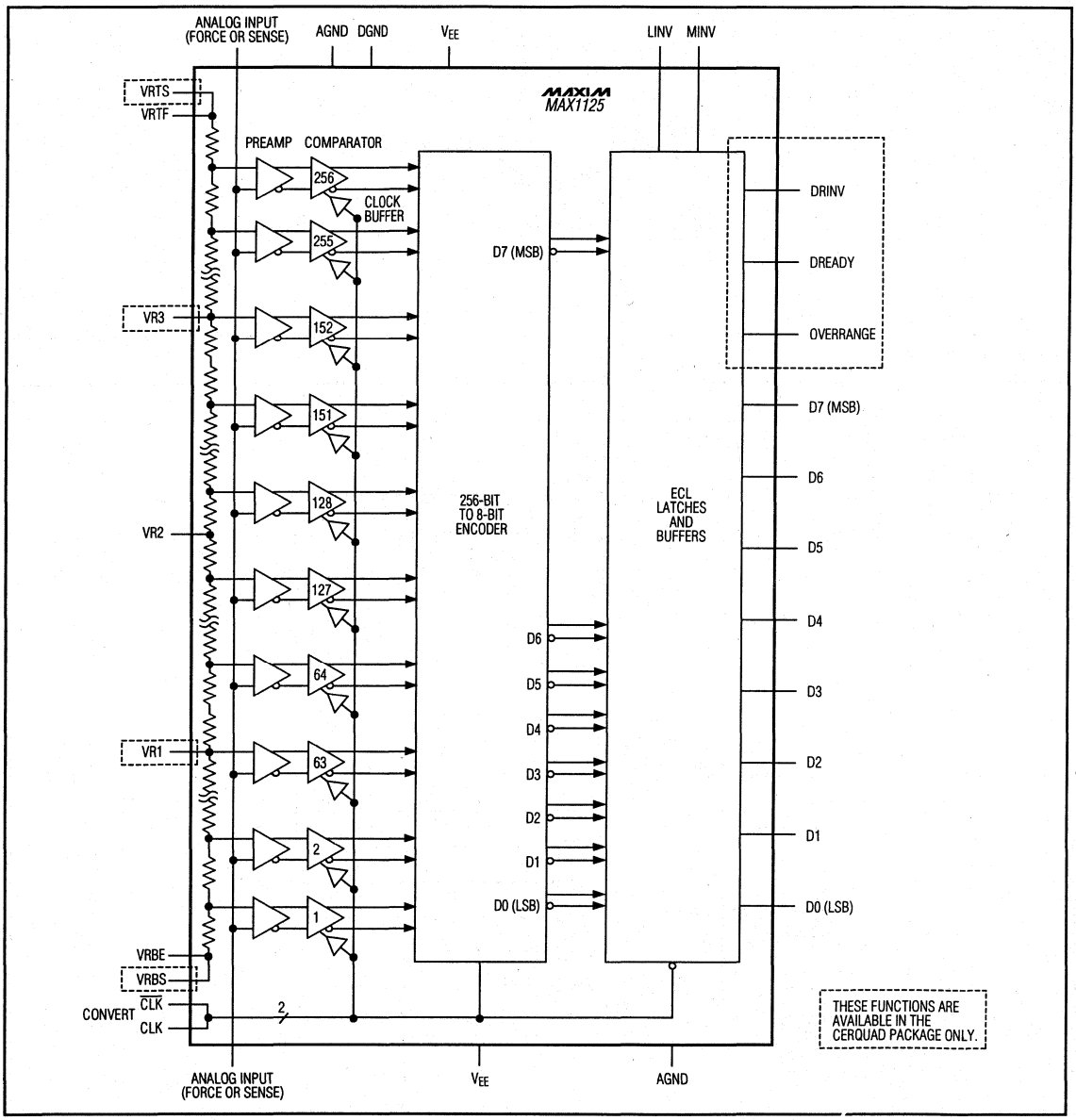


Figure 6. Burn-In Circuit (Ceramic SB package only)

8-Bit, 300Msps Flash ADC

Functional Diagram



19-1169; Rev 0; 12/96

EVALUATION KIT AVAILABLE

MAXIM
8-Bit, 500Msps Flash ADC

General Description

The MAX1150 is a parallel flash analog-to-digital converter (ADC) capable of digitizing full-scale (0V to -2V) inputs into 8-bit digital words at an update rate of 500Msps. The ECL-compatible outputs are demuxed into two separate output banks, each with differential data-ready outputs to ease the task of data capture. The MAX1150's wide input bandwidth and low capacitance eliminate the need for external track/hold amplifiers for most applications. A proprietary decoding scheme reduces metastable errors to 1LSB. This device operates from a single -5.2V supply, with a nominal power dissipation of 5.5W.

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1150AIZS	-20°C to +85°C	80 MQUAD
MAX1150BIZS	-20°C to +85°C	80 MQUAD

Features

- ♦ **1:2 Demuxed ECL-Compatible Outputs**
- ♦ **Wide Input Bandwidth: 900MHz**
- ♦ **Low Input Capacitance: 15pF**
- ♦ **Metastable Errors Reduced to 1LSB**
- ♦ **Single -5.2V Supply**

Applications

Digital Oscilloscopes

Data Acquisition

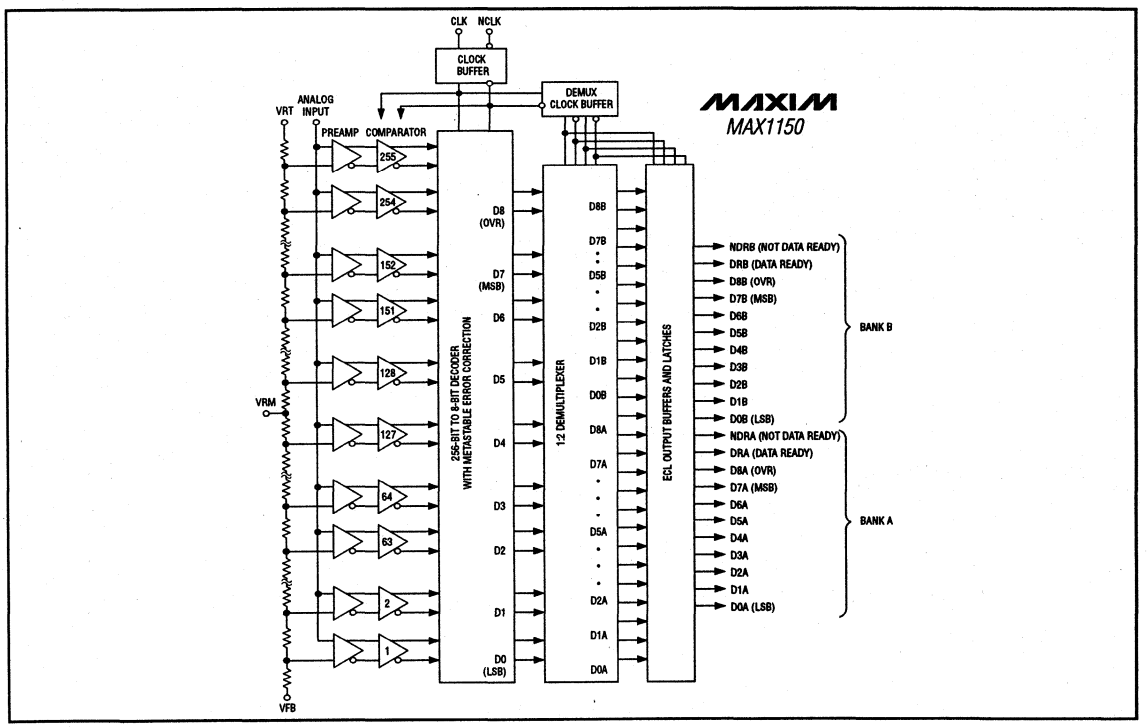
Transient-Capture Applications

Radar, EW, ECM

Direct RF/IF Downconversion

Pin Configuration appears on last page.

Functional Diagram



For the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

8-Bit, 500Msps Flash ADC

ABSOLUTE MAXIMUM RATINGS

Supply Voltages
- Negative Supply Voltage (V_{EE} to GND) .....-7.0V to +0.5V
- Ground Voltage Differential .....-0.5V to +0.5V

Input Voltages
- Analog Input Voltage.....+0.5V to V_{EE}
- Reference Input Voltage .....+0.5V to V_{EE}
- Digital Input Voltage.....+0.5V to V_{EE}
- Reference Current (V_{RT} to V_{RB}) 35mA

Digital Output Current .....0mA to -28mA
Operating Temperature Range .....-20°C to +85°C
Case Temperature .....+125°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10sec).....+300°C
Storage Temperature Range.....-65°C to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, V_{RB} = -2.00V, V_{RM} = -1.00V, V_{RT} = 0.00V, f_{CLK} = 500MHz, duty cycle = 50%, typical thermal impedance (θ_{JC}) = 4°C/W, $T_j = T_C = T_A$ = +25°C.) (Note 1)

PARAMETER	CONDITIONS	TEST LEVEL	MAX1150A MIN	MAX1150A TYP	MAX1150A MAX	MAX1150B MIN	MAX1150B TYP	MAX1150B MAX	UNITS
Resolution				8			8		Bits
DC ACCURACY									
Integral Nonlinearity	f_{CLK} = 100kHz	I	-1.0		1.0	-1.5		1.5	LSB
Differential Nonlinearity	f_{CLK} = 100kHz	I	-0.85		0.95	-0.95		1.5	LSB
No Missing Codes				Guaranteed			Guaranteed		
ANALOG INPUT									
Input Voltage Range		I	V_{RB}		V_{RT}	V_{RB}		V_{RT}	V
Input Bias Current	V_{IN} = 0V	I		0.75	2.0		0.75	2.0	mA
Input Resistance		V		15			15		kΩ
Input Capacitance	Over full input range	V		15			15		pF
Input Bandwidth	Small signal	V		900			900		MHz
	Large signal	V		500			500		
Offset Error V_{RT}		IV	-30		30	-30		30	mV
Offset Error V_{RB}		IV	-30		30	-30		30	mV
Input Slew Rate		V		5			5		V/ns
REFERENCE INPUT									
Ladder Resistance		I	60	80		60	80		Ω
Reference Bandwidth		V		30			30		MHz
TIMING CHARACTERISTICS									
Maximum Sample Rate		I	500			500			MHz
Aperture Jitter		V		2			2		ps
Acquisition Time		V		250			250		ps
CLK to DATA READY Delay		IV	0.9	1.4	1.9	0.9	1.4	1.9	ns
Clock to Data Delay		IV	1.25	1.75	2.25	1.25	1.75	2.25	ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{EE} = -5.2V, V_{RB} = -2.00V, V_{RM} = -1.00V, V_{RT} = 0.00V, f_{CLK} = 500MHz, duty cycle = 50%, typical thermal impedance (θ_{JC}) = 4°C/W, $T_j = T_C = T_A$ = +25°C.) (Note 1)

PARAMETER	CONDITIONS	TEST LEVEL	MAX1150A MIN	MAX1150A TYP	MAX1150A MAX	MAX1150B MIN	MAX1150B TYP	MAX1150B MAX	UNITS
DYNAMIC PERFORMANCE									
Signal-to-Noise Ratio (without harmonics)	f_{IN} = 50MHz	I	47			45			dB
	f_{IN} = 250MHz	I	44			42			
Total Harmonic Distortion	f_{IN} = 50MHz	I	-46			-44			dBc
	f_{IN} = 250MHz	I	-38			-36			
Signal-to-Noise and Distortion	f_{IN} = 50MHz	I	43			41			dB
	f_{IN} = 250MHz	I	37			35			
Spurious-Free Dynamic Range	f_{IN} = 50MHz	I	49			44			dB
	f_{IN} = 250MHz	I	41			36			
DIGITAL INPUTS									
Input High Voltage (CLK, NCLK)		I	-1.1	-0.7		-1.1	-0.7		V
Input Low Voltage (CLK, NCLK)		I		-1.8	-1.5		-1.8	-1.5	V
Clock Pulse Width High (t_{PWH})		I	1.0	0.67		1.0	0.67		ns
Clock Pulse Width Low (t_{PWL})		I	1.0	0.67		1.0	0.67		ns
Clock Synchronous Input Currents		V		2			2		µA
DIGITAL OUTPUTS									
Logic "1" Voltage		I	-1.1	-0.9		-1.1	-0.9		V
Logic "0" Voltage		I		-1.8	-1.5		-1.8	-1.5	V
POWER-SUPPLY REQUIREMENTS									
Supply Voltage (V_{EE})		IV	-4.95	-5.2	-5.45	-4.95	-5.2	-5.45	V
Supply Current (I_{EE})		I		1.05	1.2		1.05	1.2	A
Power Dissipation		I		5.5	6.25		5.5	6.25	W

Note 1: All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device test actually performed during production and Quality Assurance inspection. Unless otherwise noted, all tests are pulsed tests; therefore, $T_j = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = +25°C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = +25°C. Parameter is guaranteed over specified temperature range.

8-Bit, 500Msps Flash ADC

Pin Description

PIN	NAME	FUNCTION
1, 2, 3	D2B, D3B, D4B	Data Output Bank, Bits 2, 3, and 4
4, 5, 19, 20, 22, 23, 27, 28, 38, 39, 40, 46, 47, 49, 60, 67, 79	V_{EE}	Negative Supply, nominally -5.2V
6	D5B	Data Output Bank B, Bit 5
7, 9, 11, 54, 56, 58, 69, 71, 73, 75, 77	DGND	Digital Ground
8	D6B	Data Output Bank B, Bit 6
10	D7B	Data Output Bank B, Bit 7 (MSB)
12	D8B	Data Output Bank B, Bit 8 (OVR)
13, 14, 31, 34, 41, 63, 64	N.C.	No Connection. Not internally connected.
15–18, 25, 26, 29, 30, 36, 37, 44, 45, 51, 52	AGND	Analog Ground
21	VRBF	Reference-Voltage Force Bottom
24	VRBS	Reference-Voltage Sense Bottom
32, 33	VIN	Analog Input Voltage. Can be either voltage or sense.
35	VRM	Reference-Voltage Middle, nominally -1V
42	VRTF	Reference-Voltage Force Top
43	VRTS	Reference-Voltage Sense Top
48	NCLK	Inverse Clock Input
50	CLK	Clock Input
53	DRA	Data Ready Bank A
55	NDRA	Not Data Ready Bank A
57	D0A	Data Output Bank A, Bit 0 (LSB)
59, 61, 62, 65, 66, 68	D1A–D6A	Data Output Bank A, Bits 1–6
70	D7A	Data Output Bank A, Bit 7 (MSB)
72	D8A	Data Output Bank A, Bit 8 (OVR)
74	NDRB	Not Data Ready Bank B
76	DRB	Data Ready Bank B
78	D0B	Data Output Bank B, Bit 0 (LSB)
80	D1B	Data Output Bank B, Bit 1

Detailed Description

The MAX1150 is one of the fastest monolithic, 8-bit, parallel, flash analog-to-digital converters (ADCs) available today. The nominal conversion rate is 500Msps, and the analog bandwidth is in excess of 900MHz. A major advance over previous flash converters is the inclusion of 255 input preamplifiers between the reference ladder and input comparators (see *Functional Diagram*). This not only reduces clock transient kickback to the input and reference ladder, but also reduces the effect of the input signal's dynamic state on the input comparators' latching characteristics. The preamplifiers act as buffers to stabilize the input capacitance so that it remains constant over different input voltage and frequency ranges, making the part easier to drive than previous flash converters. The preamplifiers also add a gain of +2 to the input signal, so that each comparator has a wider overdrive or threshold range to trip into or out of the active state. This gain reduces metastable states that can cause errors at the output.

The MAX1150 has true differential analog and digital data paths from the preamplifiers to the output buffers (current-mode logic) for reducing potential missing codes while rejecting common-mode noise.

Signature errors are also reduced by careful layout of the analog circuitry. The device's output drive capability can provide full ECL swings into 50Ω loads.

Typical Interface Circuit

The circuit of Figure 1 shows a method of achieving the least error by correcting for integral linearity, input-induced distortion, and power- supply/ground noise. This is achieved with the use of external reference-ladder tap connections, an input buffer, and supply decoupling. Contact the factory for the MAX1150/MAX1151 evaluation kit manual, which contains more details on interfacing the MAX1150. The function of each pin and external connections to other components are described in the following sections.

V_{EE}, AGND, DGND

VEE is the supply pin with AGND as ground for the device. The power-supply pins should be bypassed as close to the device as possible with at least a 0.01µF ceramic capacitor. A 1µF tantalum can also be used for low-frequency suppression. DGND is the ground for the ECL outputs, and should be referenced to the output pulldown voltage and appropriately bypassed, as shown in Figure 1.

VIN (Analog Input)

There are two analog input pins that are tied to the same point internally. Either one may be used as an analog input sense, while the other is used for input force. This is convenient for testing the source signal to see if there is sufficient drive capability. The pins can also be tied together and driven by the same source. The MAX1150 is superior to similar devices due to a preamplifier stage before the comparators. This makes the device easier to drive because it has constant capacitance and induces less slew-rate distortion.

CLK, NCLK (Clock Inputs)

The clock inputs are designed to be driven differentially with ECL levels. The duty cycle of the clock should be kept at 50%, to avoid causing larger second harmonics. If this is not important to the intended application, duty cycles other than 50% may be used.

D0 to D8, DR, NDR (A and B)

The digital outputs can drive 50Ω to ECL levels when pulled down to -2V. When pulled down to -5.2V, the outputs can drive 130Ω to 1kΩ loads. All digital outputs are gray code, with the coding as shown in Table 1.

Table 1. Output Coding

V_{IN} (V)	D8	D7 . . . D0
0	1	10000000 10000001 10000011 • • •
-0.5	0	10100001 10100000 11100000 • • •
-1.0	0	11000001 11000000 01000000 • • •
-1.5	0	01100001 01100000 00100000 • • •
-2.0	0	00000011 00000001 00000000

VRBF, VRBS, VRTF, VRTS, VRM (Reference Inputs)

There are two reference inputs and one external reference voltage tap. These are -2V (VRB force and sense), mid-tap (VRM), and AGND (VRT force and sense). The reference pins and tap can be driven by op amps (as shown in Figure 1), or VRM can be bypassed for limited temperature operation. These voltage inputs can be bypassed to AGND for further noise suppression, if desired.

Thermal Management

The typical thermal impedance has (θ_{CA}) for the MQUAD package been measured at θ_{CA} = 17°C/W, in still air with no heatsink.

To ensure rated performance, we highly recommend using this device with a heatsink that can provide adequate air flow. We have found that a Thermalloy 17846 heatsink with a minimum air flow of 1 meter/second (200 linear feet per minute) provides adequate thermal performance under laboratory tests. Application-specific conditions should be taken into account to ensure that the device is properly heat sinked.

8-Bit, 500Msps Flash ADC

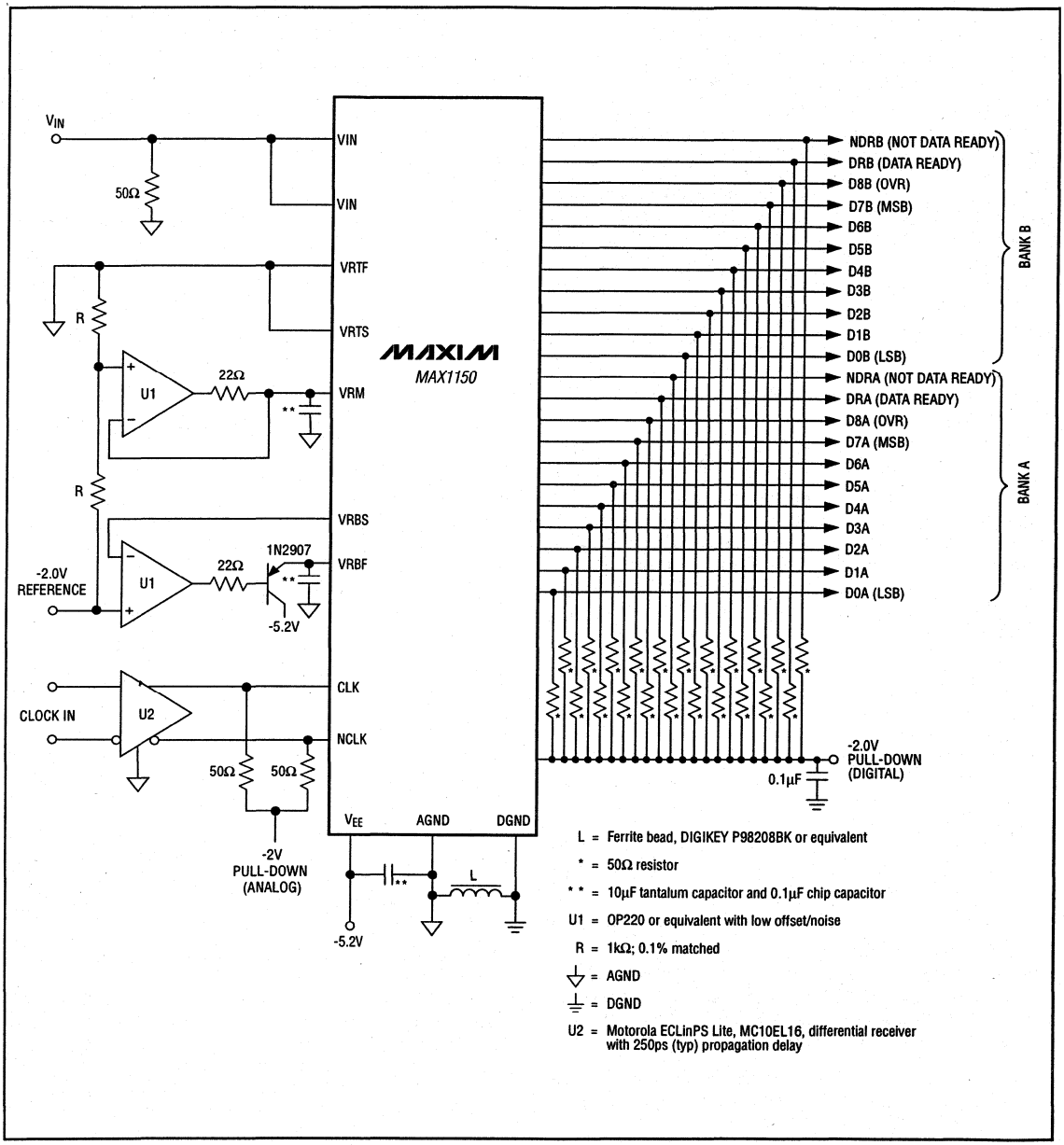


Figure 1. Typical Interface Circuit

Operation

The MAX1150 has 255 preamplifier/comparator pairs; each is supplied with the voltage from VRT to VRB, divided equally by the resistive ladder as shown in the *Functional Diagram.* This voltage is applied to the positive input of each preamplifier/comparator pair. An analog input voltage applied at VIN is connected to the negative inputs of each preamplifier/comparator pair. The comparators are then clocked through each one's individual clock buffer. When the CLK pin is in the low state, the master or input stage of the comparators compares the analog input voltage to the respective reference voltage. When CLK changes from low to high, the comparators are latched to the state prior to the clock transition and output logic codes in sequence from the top comparators, closest to VRT (0V), down to the point where the magnitude of the input signal changes sign (thermometer code). The output of each comparator is then registered into four 64-to-6 bit decoders when CLK is changed from high to low. At the output of the decoders is a set of four 7-bit latches that are enabled (track) when the clock changes from high to low. From here, the output of the latches is coded into six LSBs from four columns, and four columns are coded into two MSBs. Finally, eight ECL output latches and buffers are used to drive the external loads. The conversion takes one clock cycle from the input to the data outputs.

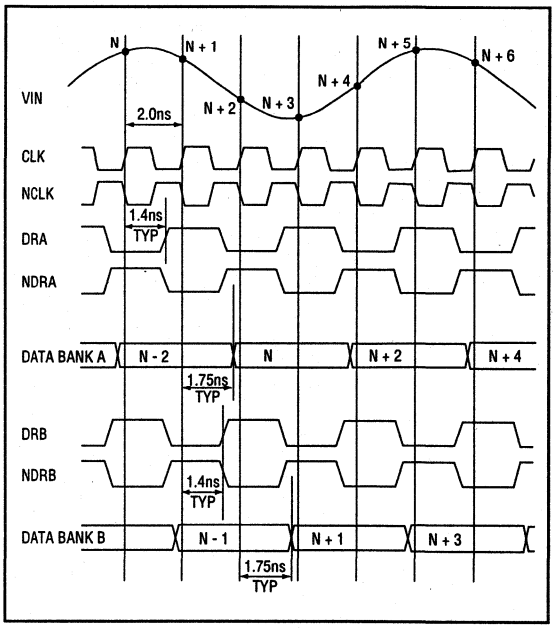


Figure 2. Timing Diagram

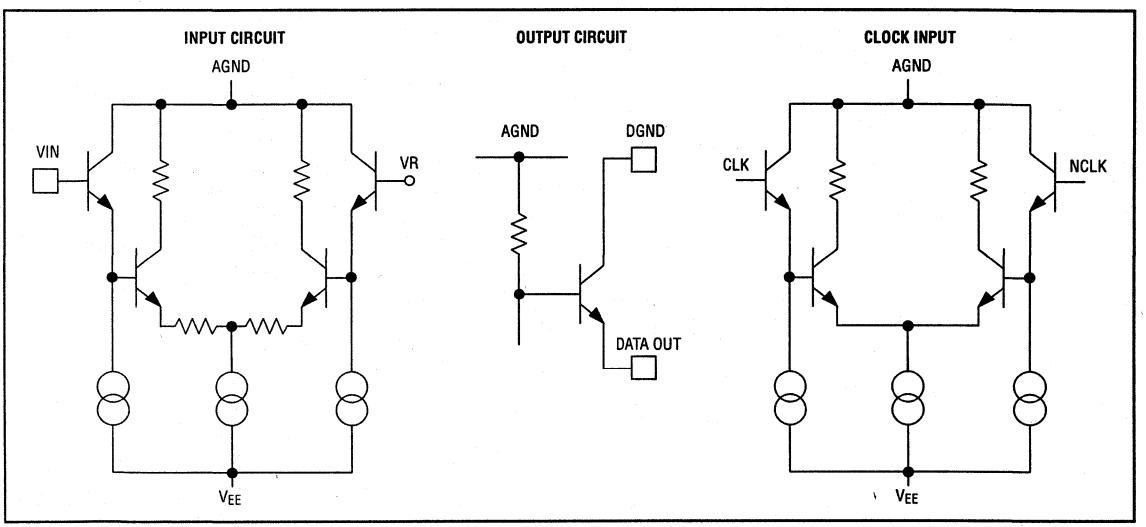
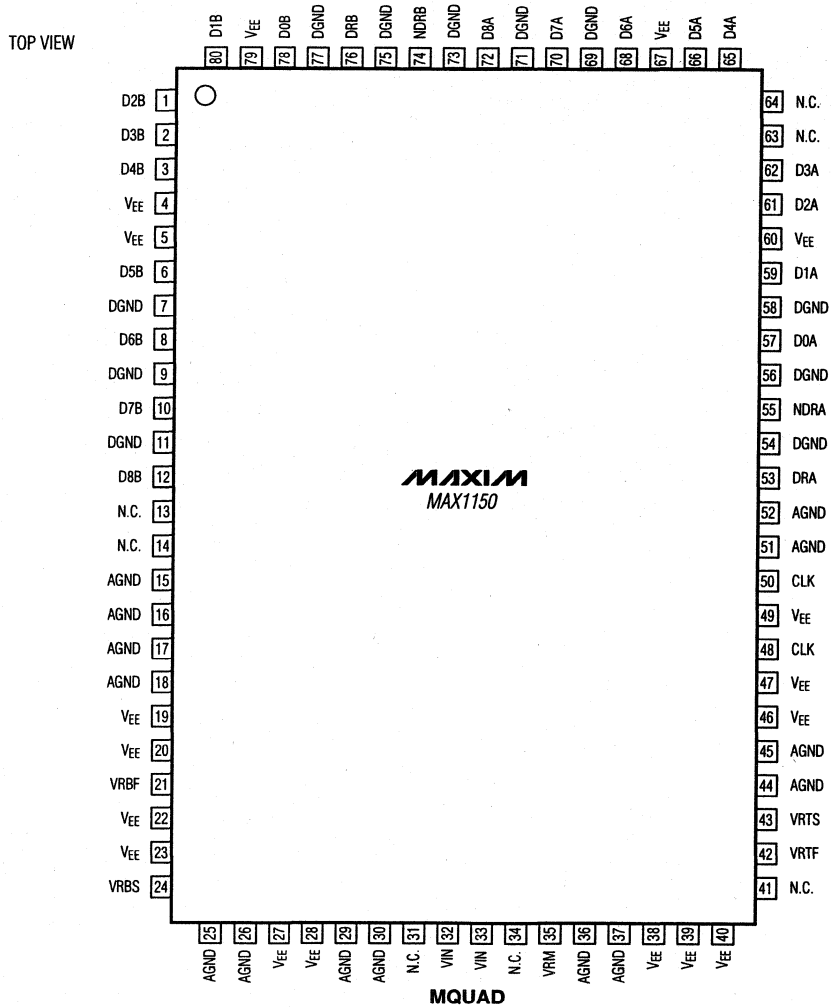


Figure 3. Subcircuit Schematics

8-Bit, 500Msps Flash ADC

Pin Configuration



19-1170; Rev 0; 12/96

EVALUATION KIT AVAILABLE

MAXIM
8-Bit, 750Msps Flash ADC

General Description

The MAX1151 is a parallel flash analog-to-digital converter (ADC) capable of digitizing full-scale (0V to -2V) inputs into 8-bit digital words at an update rate of 750Msps. The ECL-compatible outputs are demuxed into two separate output banks, each with differential data-ready outputs to ease the task of data capture. The MAX1151's wide input bandwidth and low capacitance eliminate the need for external track/hold amplifiers for most applications. A proprietary decoding scheme reduces metastable errors to 1LSB. This device operates from a single -5.2V supply, with a nominal power dissipation of 5.5W.

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1151AIZS	-20°C to +85°C	80 MQUAD
MAX1151BIZS	-20°C to +85°C	80 MQUAD

Features

- ♦ **1:2 Demuxed ECL-Compatible Outputs**
- ♦ **Wide Input Bandwidth: 900MHz**
- ♦ **Low Input Capacitance: 15pF**
- ♦ **Metastable Errors Reduced to 1LSB**
- ♦ **Single -5.2V Supply**

Applications

Digital Oscilloscopes

Data Acquisition

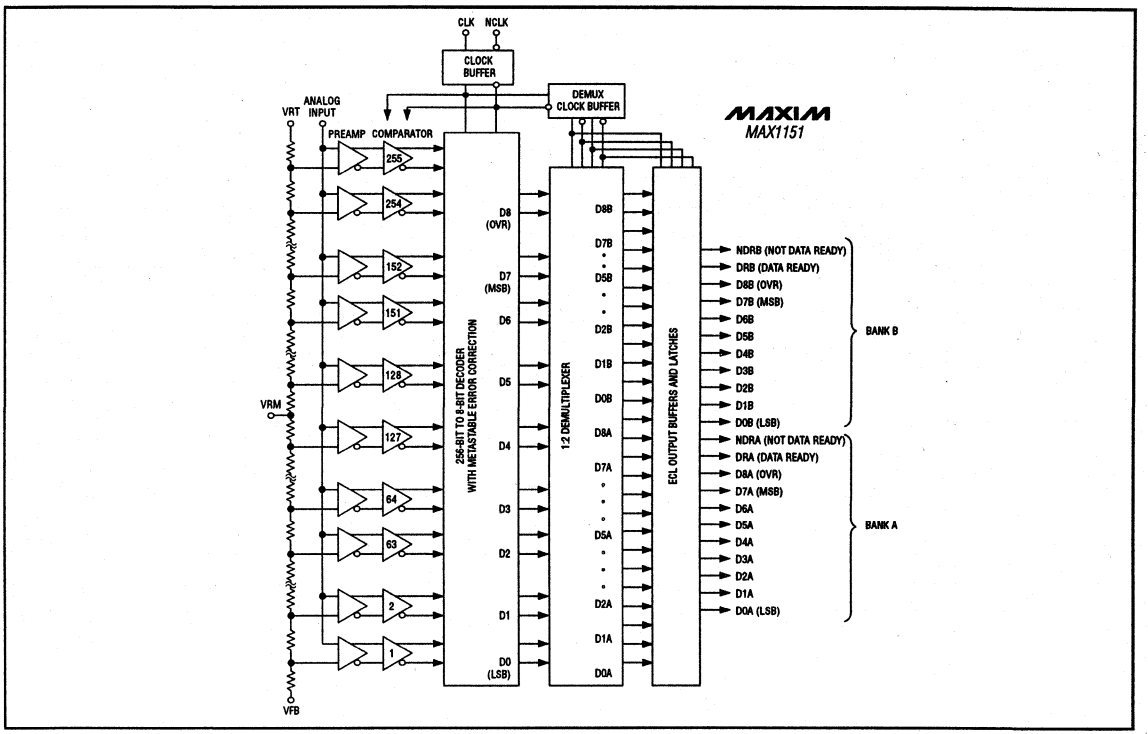
Transient-Capture Applications

Radar, EW, ECM

Direct RF/IF Downconversion

Pin Configuration appears on last page.

Functional Diagram



For the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

8-Bit, 750Msps Flash ADC

ABSOLUTE MAXIMUM RATINGS

Supply Voltages
- Negative Supply Voltage (V_{EE} to GND) .....-7.0V to +0.5V
- Ground Voltage Differential .....-0.5V to +0.5V

Input Voltages
- Analog Input Voltage .....+0.5V to V_{EE}
- Reference Input Voltage .....+0.5V to V_{EE}
- Digital Input Voltage .....+0.5V to V_{EE}
- Reference Current (V_{RT} to V_{RB}).....35mA

Digital Output Current .....0mA to -28mA
Operating Temperature Range .....-20°C to +85°C
Case Temperature .....+125°C
Junction Temperature .....+150°C
Lead Temperature (soldering, 10sec). .....+300°C
Storage Temperature Range .....-65°C to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, V_{RB} = -2.00V, V_{RM} = -1.00V, V_{RT} = 0.00V, f_{CLK} = 750MHz, duty cycle = 50%, typical thermal impedance (θ_{JC}) = 4°C/W, $T_j = T_C = T_A$ = +25°C.) (Note 1)

PARAMETER	CONDITIONS	TEST LEVEL	MAX1151A			MAX1151B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Resolution				8			8		Bits
DC ACCURACY									
Integral Nonlinearity	f_{CLK} = 100kHz	I	-1.0		1.0	-1.5		1.5	LSB
Differential Nonlinearity	f_{CLK} = 100kHz	I	-0.85		0.95	-0.95		1.5	LSB
No Missing Codes				Guaranteed			Guaranteed		
ANALOG INPUT									
Input Voltage Range		I	V_{RB}		V_{RT}	V_{RB}		V_{RT}	V
Input Bias Current	V_{IN} = 0V	I		0.75	2.0		0.75	2.0	mA
Input Resistance		V		15			15		kΩ
Input Capacitance	Over full input range	V		15			15		pF
Input Bandwidth	Small signal	V		900			900		MHz
	Large signal	V		500			500		
Offset Error V_{RT}		IV	-30		30	-30		30	mV
Offset Error V_{RB}		IV	-30		30	-30		30	mV
Input Slew Rate		V		5			5		V/ns
REFERENCE INPUT									
Ladder Resistance		I	60	80		60	80		Ω
Reference Bandwidth		V		30			30		MHz
TIMING CHARACTERISTICS									
Maximum Sample Rate		I	750			750			MHz
Aperture Jitter		V		2			2		ps
Acquisition Time		V		250			250		ps
CLK to DATA READY Delay		IV	0.9	1.4	1.9	0.9	1.4	1.9	ns
Clock to Data Delay		IV	1.25	1.75	2.25	1.25	1.75	2.25	ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{EE} = -5.2V, V_{RB} = -2.00V, V_{RM} = -1.00V, V_{RT} = 0.00V, f_{CLK} = 750MHz, duty cycle = 50%, typical thermal impedance (θ_{JC}) = 4°C/W, $T_j = T_C = T_A$ = +25°C.) (Note 1)

PARAMETER	CONDITIONS	TEST LEVEL	MAX1151A MIN	MAX1151A TYP	MAX1151A MAX	MAX1151B MIN	MAX1151B TYP	MAX1151B MAX	UNITS
DYNAMIC PERFORMANCE									
Signal-to-Noise Ratio (without harmonics)	f_{IN} = 50MHz	I	46			44			dB
	f_{IN} = 250MHz	I	44			42			
Total Harmonic Distortion	f_{IN} = 50MHz	I	-45			-43			dBc
	f_{IN} = 250MHz	I	-37			-35			
Signal-to-Noise and Distortion	f_{IN} = 50MHz	I	43			41			dB
	f_{IN} = 250MHz	I	36			34			
Spurious-Free Dynamic Range	f_{IN} = 50MHz	I	48			44			dB
	f_{IN} = 250MHz	I	40			36			
DIGITAL INPUTS									
Input High Voltage (CLK, NCLK)		I	-1.1	-0.7		-1.1	-0.7		V
Input Low Voltage (CLK, NCLK)		I		-1.8	-1.5		-1.8	-1.5	V
Clock Pulse Width High (t_{PWH})		I	0.67	0.5		0.67	0.5		ns
Clock Pulse Width Low (t_{PWL})		I	0.67	0.5		0.67	0.5		ns
Clock Synchronous Input Currents		V		2			2		µA
DIGITAL OUTPUTS									
Logic "1" Voltage		I	-1.1	-0.9		-1.1	-0.9		V
Logic "0" Voltage		I		-1.8	-1.5		-1.8	-1.5	V
POWER-SUPPLY REQUIREMENTS									
Supply Voltage (V_{EE})		IV	-4.95	-5.2	-5.45	-4.95	-5.2	-5.45	V
Supply Current (I_{EE})		I		1.05	1.2		1.05	1.2	A
Power Dissipation		I		5.5	6.25		5.5	6.25	W

Note 1: All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Unless otherwise noted, all tests are pulsed tests; therefore, $T_j = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = +25°C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = +25°C. Parameter is guaranteed over specified temperature range.

8-Bit, 750Msps Flash ADC

Pin Description

PIN	NAME	FUNCTION
1, 2, 3	D2B, D3B, D4B	Data Output Bank, Bits 2, 3, and 4
4, 5, 19, 20, 22, 23, 27, 28, 38, 39, 40, 46, 47, 49, 60, 67, 79	V_{EE}	Negative Supply, nominally -5.2V
6	D5B	Data Output Bank B, Bit 5
7, 9, 11, 54, 56, 58, 69, 71, 73, 75, 77	DGND	Digital Ground
8	D6B	Data Output Bank B, Bit 6
10	D7B	Data Output Bank B, Bit 7 (MSB)
12	D8B	Data Output Bank B, Bit 8 (OVR)
13, 14, 31, 34, 41, 63, 64	N.C.	No Connection. Not internally connected.
15-18, 25, 26, 29, 30, 36, 37, 44, 45, 51, 52	AGND	Analog Ground
21	VRBF	Reference-Voltage Force Bottom
24	VRBS	Reference-Voltage Sense Bottom
32, 33	VIN	Analog Input Voltage. Can be either voltage or sense.
35	VRM	Reference-Voltage Middle, nominally -1V
42	VRTF	Reference-Voltage Force Top
43	VRTS	Reference-Voltage Sense Top
48	NCLK	Inverse Clock Input
50	CLK	Clock Input
53	DRA	Data Ready Bank A
55	NDRA	Not Data Ready Bank A
57	D0A	Data Output Bank A, Bit 0 (LSB)
59, 61, 62, 65, 66, 68	D1A–D6A	Data Output Bank A, Bits 1–6
70	D7A	Data Output Bank A, Bit 7 (MSB)
72	D8A	Data Output Bank A, Bit 8 (OVR)
74	NDRB	Not Data Ready Bank B
76	DRB	Data Ready Bank B
78	D0B	Data Output Bank B, Bit 0 (LSB)
80	D1B	Data Output Bank B, Bit 1

Detailed Description

The MAX1151 is one of the fastest monolithic, 8-bit, parallel, flash analog-to-digital converters (ADCs) available today. The nominal conversion rate is 750Msps, and the analog bandwidth is in excess of 900MHz. A major advance over previous flash converters is the inclusion of 255 input preamplifiers between the reference ladder and input comparators (see *Functional Diagram*). This not only reduces clock transient kickback to the input and reference ladder but also reduces the effect of the input signal's dynamic state on the input comparators' latching characteristics. The preamplifiers act as buffers to stabilize the input capacitance so that it remains constant over different input voltage and frequency ranges, making the part easier to drive than previous flash converters. The preamplifiers also add a gain of +2 to the input signal, so that each comparator has a wider overdrive or threshold range to trip into or out of the active state. This gain reduces metastable states that can cause errors at the output.

The MAX1151 has true differential analog and digital data paths from the preamplifiers to the output buffers (current-mode logic) for reducing potential missing codes while rejecting common-mode noise.

Signature errors are also reduced by careful layout of the analog circuitry. The device's output drive capability can provide full ECL swings into 50Ω loads.

Typical Interface Circuit

The circuit of Figure 1 shows a method of achieving the least error by correcting for integral linearity, input-induced distortion, and power-supply/ground noise. This is achieved with the use of external reference-ladder tap connections, an input buffer, and supply decoupling. Contact the factory for the MAX1150/MAX1151 evaluation kit manual, which contains more details on interfacing the MAX1151. The function of each pin and external connections to other components are described in the following sections.

VEE, AGND, DGND

V_{EE} is the supply pin with AGND as ground for the device. The power-supply pins should be bypassed as close to the device as possible with at least a 0.01µF ceramic capacitor. A 1µF tantalum can also be used for low-frequency suppression. DGND is the ground for the ECL outputs, and should be referenced to the output pulldown voltage and appropriately bypassed, as shown in Figure 1.

VIN (Analog Input)

There are two analog input pins that are tied to the same point internally. Either one may be used as an analog input sense, while the other is used for input force. This is convenient for testing the source signal to see if there is sufficient drive capability. The pins can also be tied together and driven by the same source. The MAX1151 is superior to similar devices due to a preamplifier stage before the comparators. This makes the device easier to drive because it has constant capacitance and induces less slew-rate distortion.

CLK, NCLK (Clock Inputs)

The clock inputs are designed to be driven differentially with ECL levels. The duty cycle of the clock should be kept at 50%, to avoid causing larger second harmonics. If this is not important to the intended application, duty cycles other than 50% may be used.

D0 to D8, DR, NDR (A and B)

The digital outputs can drive 50Ω to ECL levels when pulled down to -2V. When pulled down to -5.2V, the outputs can drive 130Ω to 1kΩ loads. All digital outputs are gray code, with the coding as shown in Table 1.

Table 1. Output Coding

V_{IN} (V)	D8	D7 . . . D0
0	1	10000000 10000001 10000011 • • •
-0.5	0	10100001 10100000 11100000 • • •
-1.0	0	11000001 11000000 01000000 • • •
-1.5	0	01100001 01100000 00100000 • • •
-2.0	0	00000011 00000001 00000000

VRBF, VRBS, VRTF, VRTS, VRM (Reference Inputs)

There are two reference inputs and one external reference voltage tap. These are -2V (VRB force and sense), mid-tap (VRM), and AGND (VRT force and sense). The reference pins and tap can be driven by op amps (as shown in Figure 1), or VRM can be bypassed for limited temperature operation. These voltage inputs can be bypassed to AGND for further noise suppression, if desired.

Thermal Management

The typical thermal impedance (θ_{CA}) for the MQUAD package has been measured at θ_{CA} = 17°C/W, in still air with no heatsink.

To ensure rated performance, we highly recommend using this device with a heatsink that can provide adequate air flow. We have found that a Thermalloy 17846 heatsink with a minimum air flow of 1 meter/second (200 linear feet per minute) provides adequate thermal performance under laboratory tests. Application-specific conditions should be taken into account to ensure that the device is properly heat sinked.

8-Bit, 750Msps Flash ADC

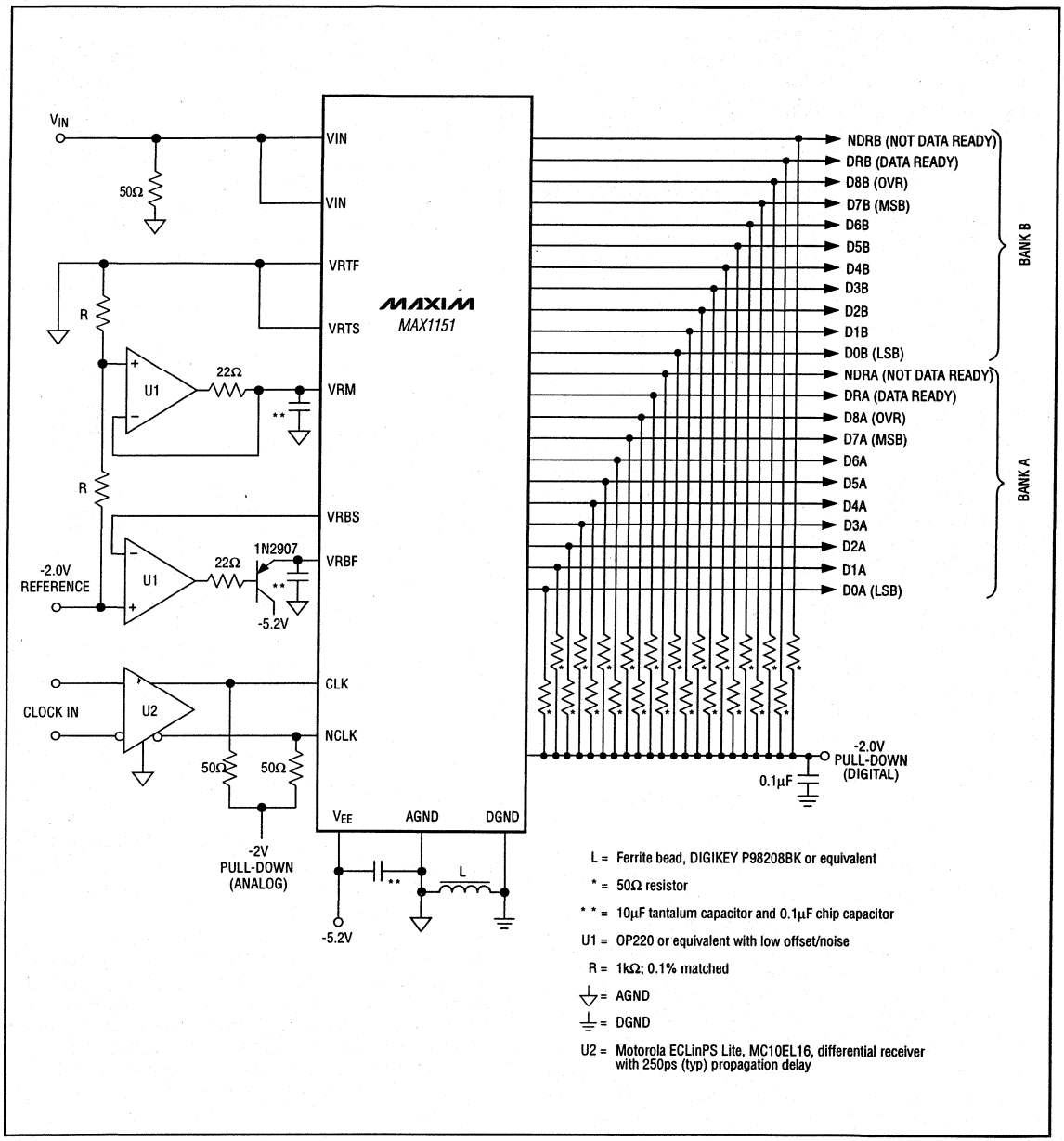


Figure 1. Typical Interface Circuit

Operation

The MAX1151 has 255 preamplifier/comparator pairs; each is supplied with the voltage from VRT to VRB, divided equally by the resistive ladder as shown in the *Functional Diagram*. This voltage is applied to the positive input of each preamplifier/comparator pair. An analog input voltage applied at VIN is connected to the negative inputs of each preamplifier/comparator pair. The comparators are then clocked through each one's individual clock buffer. When the CLK pin is in the low state, the master or input stage of the comparators compares the analog input voltage to the respective reference voltage. When CLK changes from low to high, the comparators are latched to the state prior to the clock transition and output logic codes in sequence from the top comparators, closest to VRT (0V), down to the point where the magnitude of the input signal changes sign (thermometer code). The output of each comparator is then registered into four 64-to-6 bit decoders when CLK is changed from high to low. At the output of the decoders is a set of four 7-bit latches that are enabled (track) when the clock changes from high to low. From here, the output of the latches is coded into six LSBs from four columns, and four columns are coded into two MSBs. Finally, eight ECL output latches and buffers are used to drive the external loads. The conversion takes one clock cycle from the input to the data outputs.

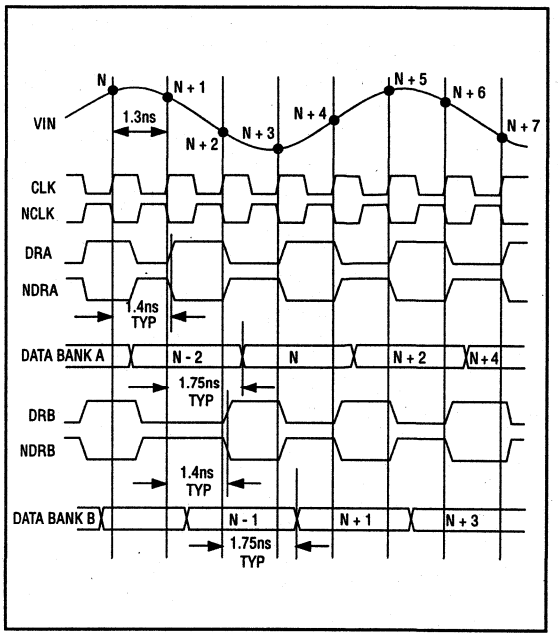


Figure 2. Timing Diagram

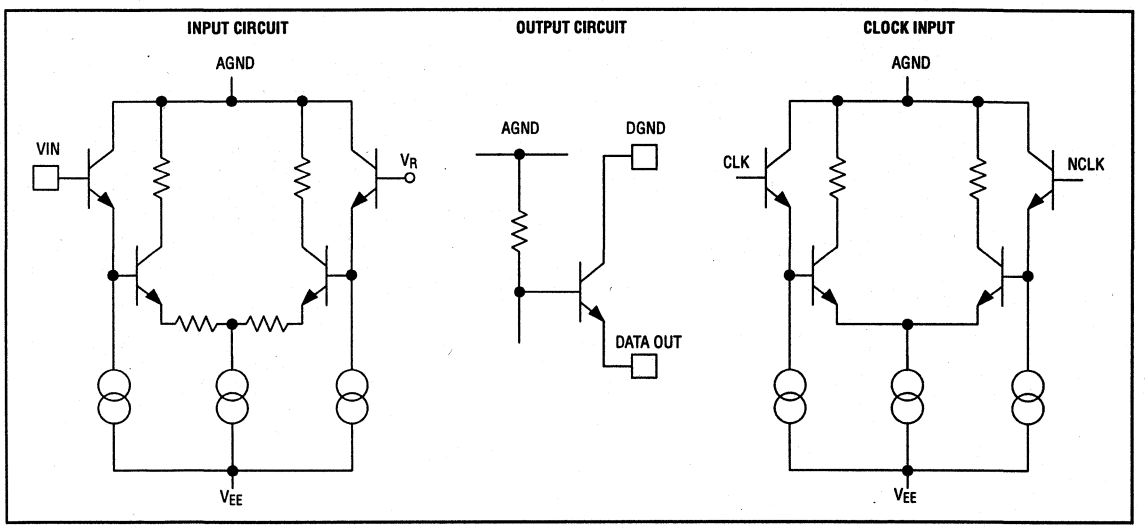
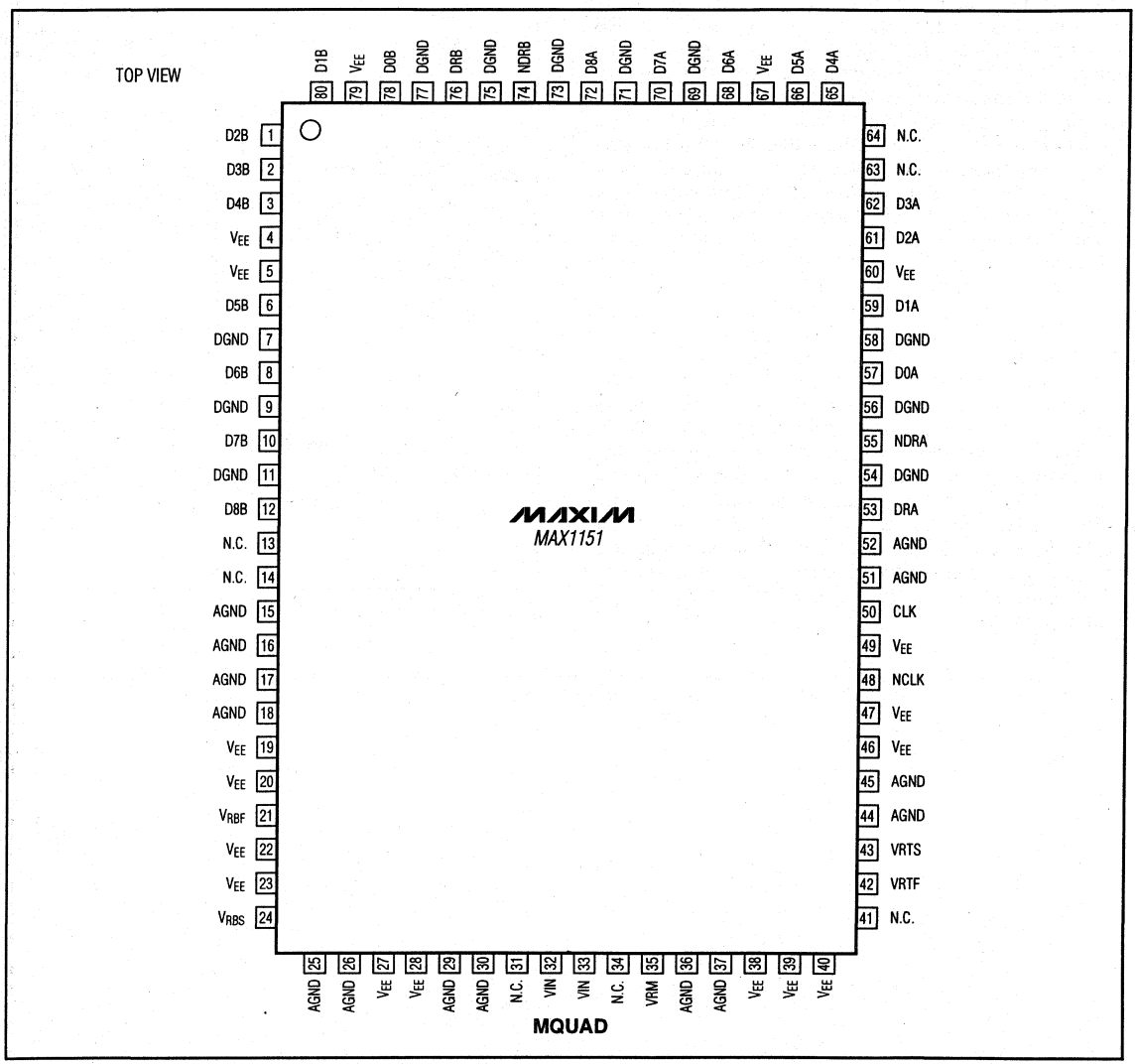


Figure 3. Subcircuit Schematics

8-Bit, 750Msps Flash ADC

Pin Configuration



ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

10/96

MAXIM

10-Bit, 20Msps, TTL-Output ADC

General Description

The MAX1160 10-bit, monolithic analog-to-digital converter (ADC) is capable of 20Msps minimum word rates. An on-board track/hold ensures excellent dynamic performance without the need for external components. A 5pF input capacitance minimizes drive requirement problems.

Inputs and outputs are TTL compatible. An overrange output is provided to indicate overflow conditions. Output data format is straight binary. Power dissipation is very low at only 1W with +5V and -5.2V power-supply voltages. The MAX1160 also accepts wide, ±2V input voltages.

The MAX1160 is available in 28-pin DIP and SO packages in the commercial temperature range.

Applications

Medical Imaging
Professional Video
Radar Receivers
Instrumentation
Digital Communications

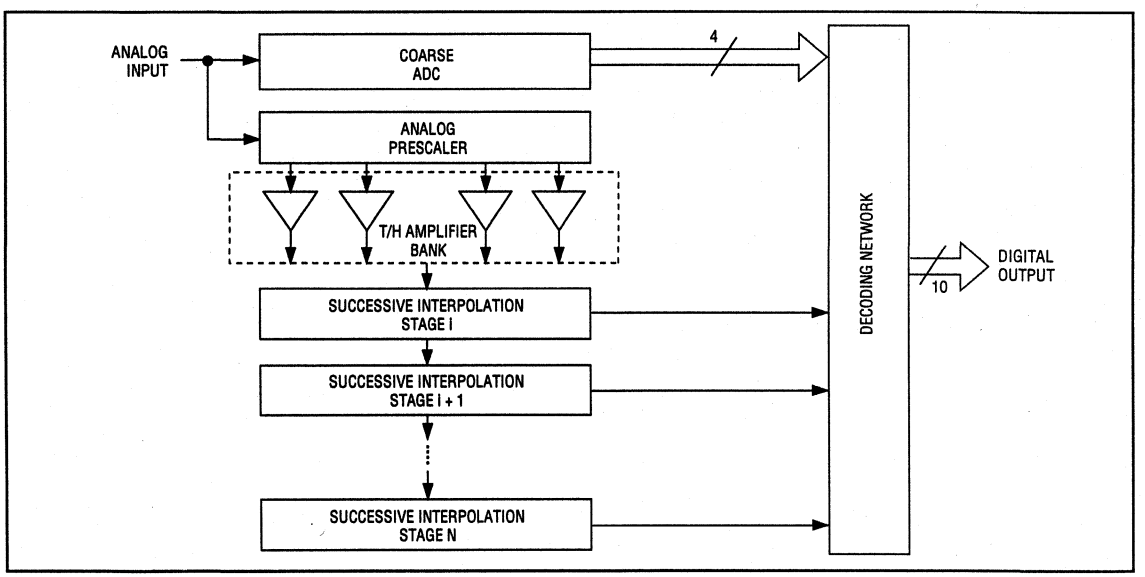
Features

- **Monolithic 20Msps Converter**
- **On-Chip Track/Hold**
- **Bipolar, ±2V Analog Input**
- **60dB SNR at 1MHz Input**
- **Low Power (1W typical)**
- **5pF Input Capacitance**
- **TTL Outputs**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1160ACPI	0°C to +70°C	28 Wide Plastic DIP
MAX1160BCPI	0°C to +70°C	28 Wide Plastic DIP
MAX1160ACWI	0°C to +70°C	28 SO
MAX1160BCWI	0°C to +70°C	28 SO

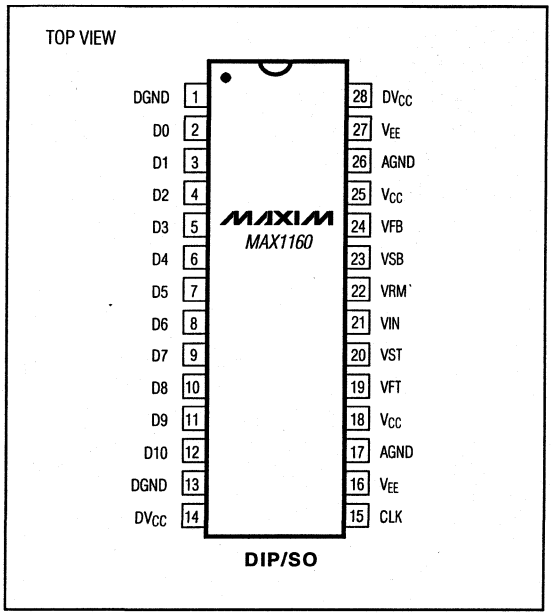
Functional Diagram



For the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

10-Bit, 20Msps, TTL-Output ADC

Pin Configuration



ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

10/96

MAXIM

10-Bit, 40Msps, TTL-Output ADC

General Description

The MAX1161 10-bit, monolithic analog-to-digital converter (ADC) is capable of 40Msps minimum word rates. An on-board track/hold ensures excellent dynamic performance without the need for external components. A 5pF input capacitance minimizes drive requirement problems.

Inputs and outputs are TTL compatible. An overrange output is provided to indicate overflow conditions. Output data format is straight binary. Power dissipation is very low at only 1W with +5V and -5.2V power-supply voltages. The MAX1161 also accepts wide, ±2V input voltages.

The MAX1161 is available in 28-pin DIP and SO packages in the commercial temperature range.

Applications

Medical Imaging
Professional Video
Radar Receivers
Instrumentation
Digital Communications

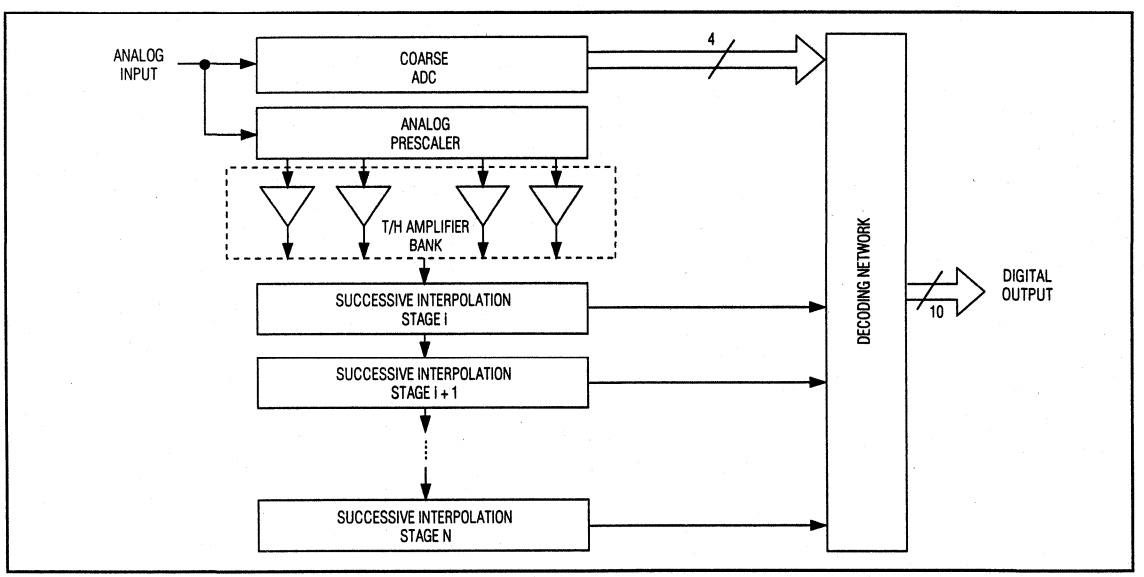
Features

- **Monolithic 40Msps Converter**
- **On-Chip Track/Hold**
- **Bipolar, ±2V Analog Input**
- **57dB SNR at 3.58MHz Input**
- **Low Power (1W typical)**
- **5pF Input Capacitance**
- **TTL Outputs**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1161ACPI	0°C to +70°C	28 Wide Plastic DIP
MAX1161BCPI	0°C to +70°C	28 Wide Plastic DIP
MAX1161ACWI	0°C to +70°C	28 SO
MAX1161BCWI	0°C to +70°C	28 SO

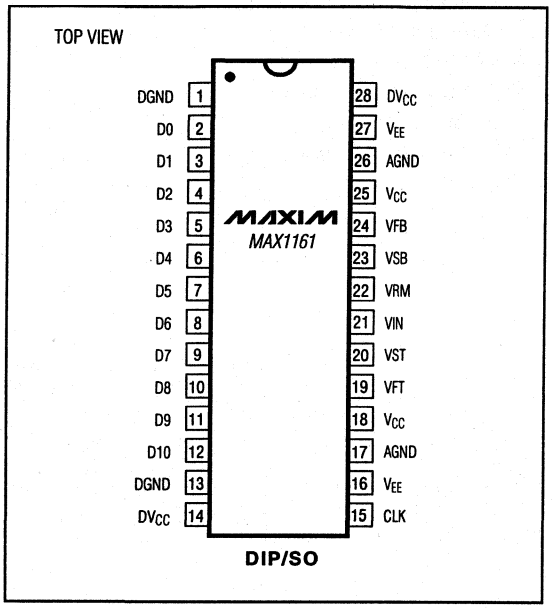
Functional Diagram



For the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

10-Bit, 40Msps, TTL-Output ADC

Pin Configuration



19-1132; Rev 0; 10/96

EVALUATION KIT AVAILABLE

MAXIM

12-Bit, 10Msps, TTL-Output ADC

General Description

The MAX1170 analog-to-digital converter (ADC) is a 12-bit monolithic ADC capable of sample rates greater than 10Msps. An on-board input buffer and track/hold function ensure excellent dynamic performance without the need for external components. A 5pF input capacitance minimizes development problems.

Logic inputs and outputs are TTL compatible. An overrange output signal is provided to indicate overflow conditions. Output data format is straight binary. Power dissipation is a very low 1.1W with power-supply voltages of +5.0V and -5.2V. The MAX1170 also provides a wide input voltage range of ±2.0V.

The MAX1170 is available in a 32-lead ceramic side-brazed package and a 44-lead surface-mount CERQUAD package.

Features

- ♦ **Monolithic, 12-Bit, 10Msps Converter**
- ♦ **On-Chip Track/Hold**
- ♦ **±2.0V Analog Input Range**
- ♦ **High Input Impedance**
- ♦ **66dB SNR at 1MHz Input**
- ♦ **Low Power: 1.1W**
- ♦ **5pF Input Capacitance**
- ♦ **TTL-Compatible Outputs**

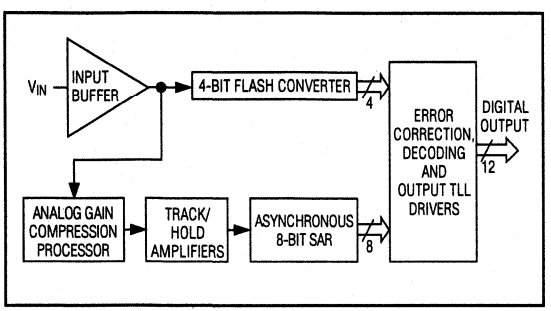
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1170CDJ	0°C to +70°C	32 Ceramic SB
MAX1170CBH	0°C to +70°C	44 CERQUAD

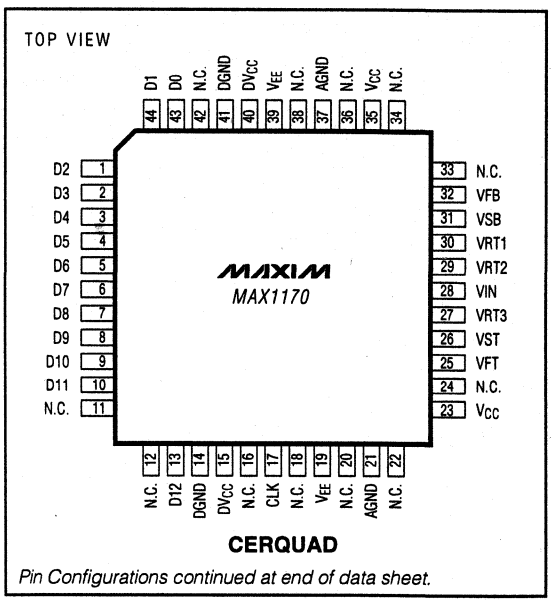
Applications

Radar Receivers
Professional Video
Instrumentation
Imaging
Digital Communications
Digital Spectrum Analyzers

Functional Diagram



Pin Configurations



CERQUAD

Pin Configurations continued at end of data sheet.

For the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

12-Bit, 10Msps, TTL-Output ADC

ABSOLUTE MAXIMUM RATINGS

V_{CC} .....+6V
V_{EE} .....-6V
Analog Input .....$V_{FB} \le V_{IN} \le V_{FT}$
VFB, VFT ..... -3.0V, +3.0V
Reference Ladder Current 12mA
CLK IN .....V_{CC}

Digital Outputs.....0mA to -30mA
Operating Temperature Range.....0°C to +70°C
Junction Temperature (T_j).....+175°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5.0V, V_{EE} = -5.2V, DV_{CC} = +5.0V, V_{IN} = ±2.0V, V_{SB} = -2.0V, V_{ST} = +2.0V, f_{CLK} = 10MHz, 50% clock duty cycle, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Resolution			12			Bits
DC ACCURACY (T_A = +25°C)						
Integral Nonlinearity	± full scale	IV		±2.0		LSB
Differential Nonlinearity	250kHz sample rate	IV		±0.8		LSB
No Missing Codes		I		Guaranteed		
ANALOG INPUT						
Input Voltage Range		VI		±2.0		V
Input Bias Current	T_A = +25°C	I		30	60	µA
Input Resistance	V_{IN} = 0V, T_A = +25°C	I	100	300		kΩ
Input Capacitance		V		5		pF
Input Bandwidth	3dB small signal	V		120		MHz
Positive Full-Scale Error		V		±5.0		LSB
Negative Full-Scale Error		V		±5.0		LSB
REFERENCE INPUT						
Reference Ladder Resistance		VI	500	800		Ω
Reference Ladder Tempco		V		0.8		Ω/°C
TIMING CHARACTERISTICS						
Maximum Conversion Rate		VI	10			MHz
Overvoltage Recovery Time		V		20		ns
Pipeline Delay (Latency)		VI			1	Clock Cycle
Output Delay	T_A = +25°C	V		14	18	ns
Aperture Delay Time	T_A = +25°C	V		1		ns
Aperture Jitter Time	T_A = +25°C	V		5		ps-RMS

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5.0V, V_{EE} = -5.2V, DV_{CC} = +5.0V, V_{IN} = ±2.0V, V_{SB} = -2.0V, V_{ST} = +2.0V, f_{CLK} = 10MHz, 50% clock duty cycle, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		TEST LEVEL	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE							
Effective Number of Bits	f_{IN} = 500kHz				10.2		Bits
	f_{IN} = 1MHz				10.0		
	f_{IN} = 3.58MHz				9.5		
Signal-to-Noise Ratio (without Harmonics)	f_{IN} = 500kHz	T_A = +25°C	I	64	67		dB
		T_A = T_{MIN} to T_{MAX}	IV	58	61		
	f_{IN} = 1MHz	T_A = +25°C	I	64	66		
		T_A = T_{MIN} to T_{MAX}	IV	58	60		
	f_{IN} = 3.58MHz	T_A = +25°C	I	62	64		
		T_A = T_{MIN} to T_{MAX}	IV	58	60		
Harmonic Distortion	f_{IN} = 500kHz	T_A = +25°C	I	63	66		dB
		T_A = T_{MIN} to T_{MAX}	IV	59	62		
	f_{IN} = 1MHz	T_A = +25°C	I	63	65		
		T_A = T_{MIN} to T_{MAX}	IV	59	61		
	f_{IN} = 3.58MHz	T_A = +25°C	I	59	61		
		T_A = T_{MIN} to T_{MAX}	IV	57	59		
Signal-to-Noise and Distortion	f_{IN} = 500kHz	T_A = +25°C	I	60	63		dB
		T_A = T_{MIN} to T_{MAX}	IV	55	58		
	f_{IN} = 1MHz	T_A = +25°C	I	60	62		
		T_A = T_{MIN} to T_{MAX}	IV	55	57		
	f_{IN} = 3.58MHz	T_A = +25°C	I	57	59		
		T_A = T_{MIN} to T_{MAX}	IV	54	56		
Spurious-Free Dynamic Range	f_{IN} = 1MHz, T_A = +25°C		V		74		dBc
Differential Phase	f_{IN} = 3.58MHz and 4.35MHz, T_A = +25°C		V		0.2		Degrees
Differential Gain	f_{IN} = 3.58MHz and 4.35MHz, T_A = +25°C		V		0.7		%
DIGITAL INPUTS							
Logic "1" Voltage			V	2.4		4.0	V
Logic "0" Voltage			V			0.8	V
Maximum Input Current Low	T_A = +25°C		I	0	5	20	µA
Maximum Input Current High	T_A = +25°C		I	0	5	20	µA
Pulse Width Low (CLK)			IV	30			ns
Pulse Width High (CLK)			IV	30		300	ns
DIGITAL OUTPUTS							
Logic "1" Voltage	T_A = +25°C		I	2.4			V
Logic "0" Voltage	T_A = +25°C		I			0.6	V

12-Bit, 10Msps, TTL-Output ADC

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5.0V, V_{EE} = -5.2V, DV_{CC} = +5.0V, V_{IN} = ±2.0V, V_{SB} = -2.0V, V_{ST} = +2.0V, f_{CLK} = 10MHz, 50% clock duty cycle, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
POWER-SUPPLY REQUIREMENTS						
Voltages	V_{CC}	IV	4.75	5.0	5.25	V
	DV_{CC}	IV	4.75	5.0	5.25	
	$-V_{EE}$	IV	-4.95	-5.2	-5.45	
Currents	I_{CC}, T_A = +25°C	I		135	150	mA
	DI_{CC}, $T_A = T_{MIN}$ to T_{MAX}	IV		40	55	
	$-I_{EE}$, T_A = +25°C	I		45	70	
Power Dissipation		VI		1.1	1.3	W
Power-Supply Rejection	5V ±0.25V, -5.2V ±0.25V	V		1.0		LSB

Note 1: Typical thermal impedances (unsoldered, in free air):
32 Ceramic SB: θ_{JA} = 50°C/W
44 CERQUAD: θ_{JA} = 78°C/W, θ_{JA} at 1m/s airflow = 58°C/W, θ_{JC} = 3.3°C/W
Use forced-air cooling or heatsinking to maintain $T_J \leq 150°C$.

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

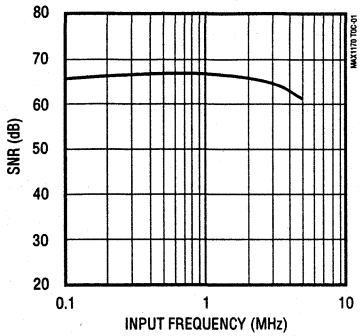
Unless otherwise noted, all tests are pulsed; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = +25°C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = +25°C. Parameter is guaranteed over specified temperature range.

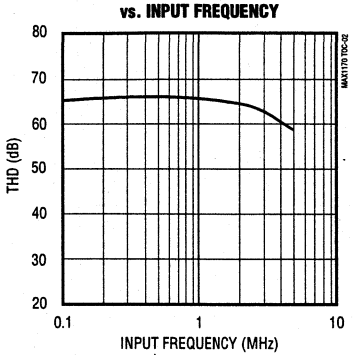
Typical Operating Characteristics

(f_S = 10Msps, f_{IN} = 1MHz, T_A = +25°C, unless otherwise noted.)

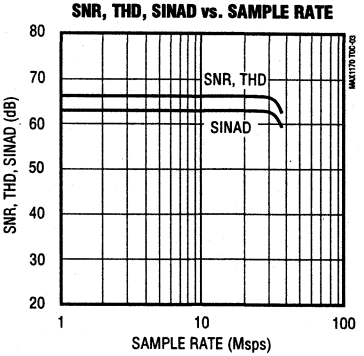
SIGNAL-TO-NOISE RATIO vs. INPUT FREQUENCY



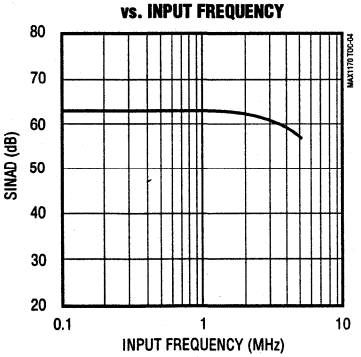
TOTAL HARMONIC DISTORTION vs. INPUT FREQUENCY



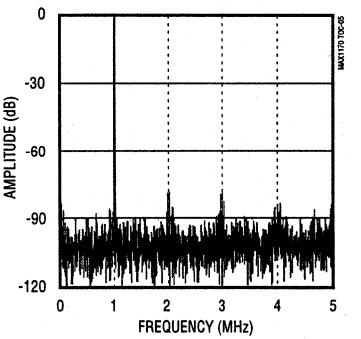
SNR, THD, SINAD vs. SAMPLE RATE



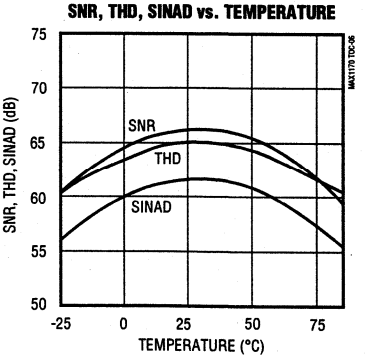
SIGNAL-TO-NOISE AND DISTORTION vs. INPUT FREQUENCY



SPECTRAL RESPONSE



SNR, THD, SINAD vs. TEMPERATURE



12-Bit, 10Msps, TTL-Output ADC

Pin Description

PIN		NAME	FUNCTION
Ceramic SB	CERQUAD		
1, 15	14, 41	DGND	Digital Ground
2–13	43, 44, 1–10	D0–D11	TTL Outputs (D0 = LSB)
14	13	D12	TTL Output Overrange Bit
16, 32	15, 40	DV_{CC}	Digital +5.0V Supply (TTL Outputs)
17	17	CLK	TTL Clock Input
18, 31	19, 39	V_{EE}	-5.2V Supply
19, 30	21, 37	AGND	Analog Ground
20, 29	23, 35	V_{CC}	+5.0V Supply
21	25	VFT	Force for Top of Reference Ladder
22	26	VST	Sense for Top of Reference Ladder
23	27	VRT3	Voltage Reference Tap 3
24	28	VIN	Analog Input, ±2.0V typical
25	29	VRT2	Voltage Reference Tap 2
26	30	VRT1	Voltage Reference Tap 1
27	31	VSB	Sense for Bottom of Reference Ladder
28	32	VFB	Force for Bottom of Reference Ladder
—	11, 12, 16, 18, 20, 22, 24, 33, 34, 36, 38, 42	N.C.	No Connection

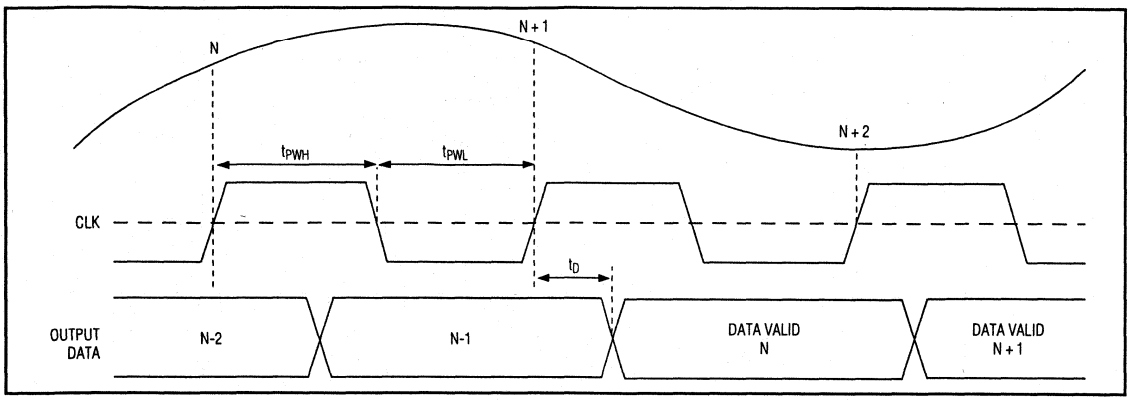


Figure 1a. Timing Diagram

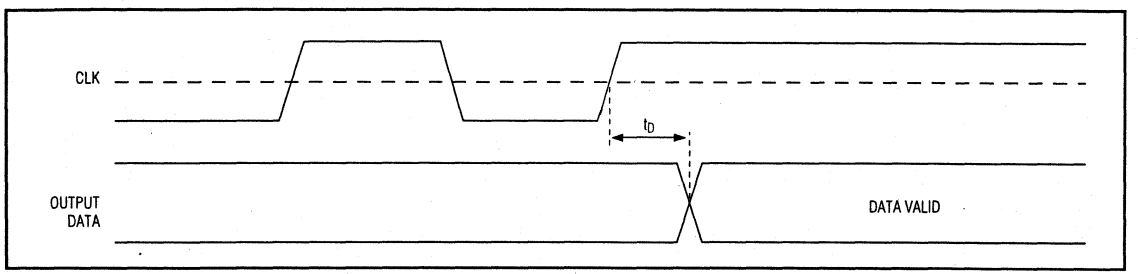


Figure 1b. Single-Event Clock

Table 1. Timing Parameters

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
t_D	CLK to Data Valid Prop Delay		14	18	ns
t_{PWH}	CLK High Pulse Width	30		300	ns
t_{PWL}	CLK Low Pulse Width	30			ns

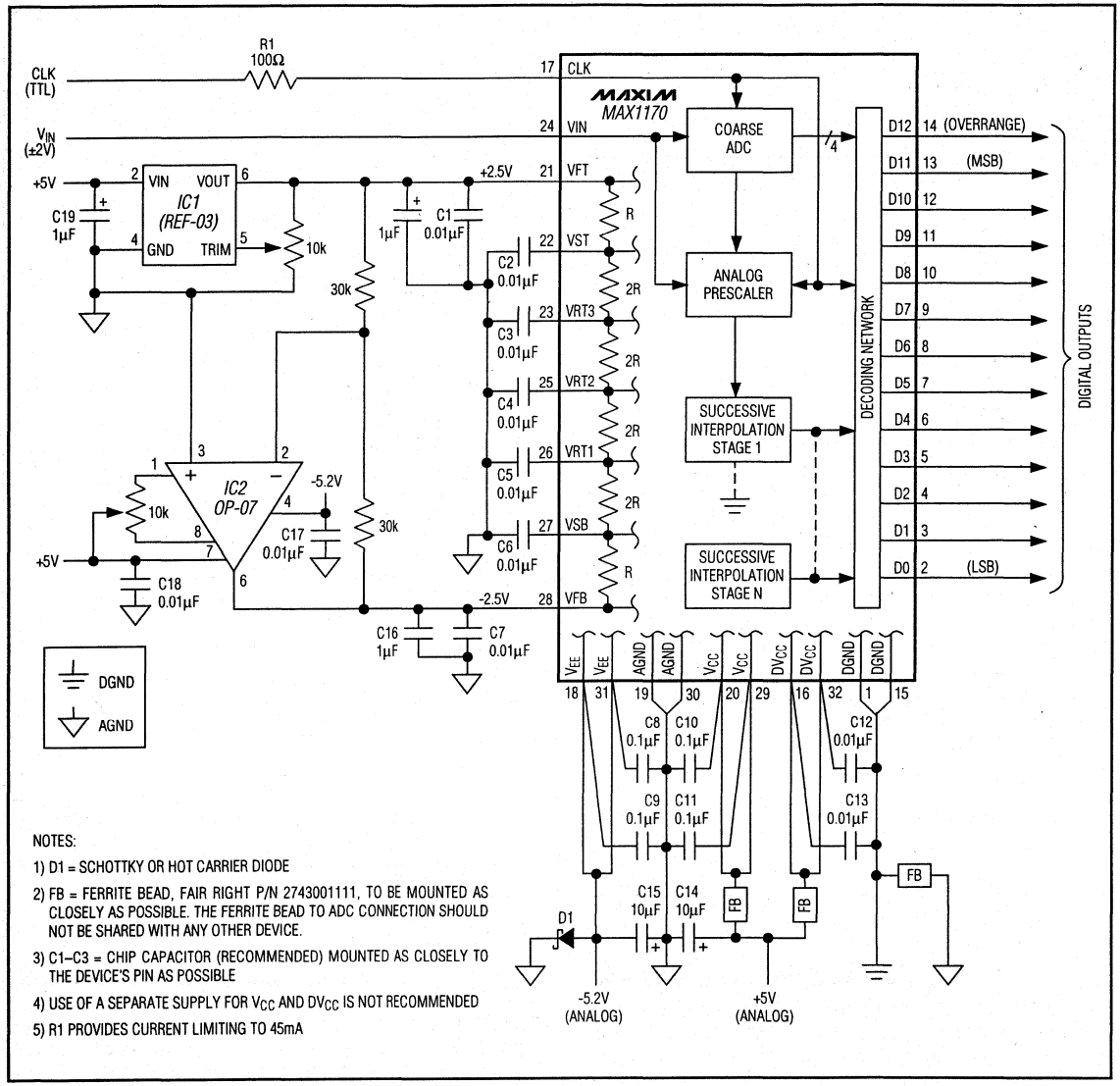
Detailed Description

The MAX1170 requires few external components to achieve the stated operation and performance. Figure 2 shows the typical interface requirements when using the MAX1170 in normal circuit operation. The following section provides a description of the pin functions and outlines critical performance criteria for achieving the optimal device performance.

Power Supplies and Grounding

The MAX1170 requires -5.2V and +5V analog supply voltages. The +5V supply is common to analog V_{CC} and digital DV_{CC}. A ferrite bead in series with each supply line reduces the transient noise injected into the analog V_{CC}. These beads should be connected as close to the device as possible. The connection between the beads and the MAX1170 should not be shared with any other device. Bypass each power-supply pin as close to the device as possible. Use 0.1µF for V_{EE} and V_{CC}, and 0.01µF for DV_{CC} (chip capacitors are preferred).

12-Bit, 10Msps, TTL-Output ADC



NOTES:

1) D1 = SCHOTTKY OR HOT CARRIER DIODE

2) FB = FERRITE BEAD, FAIR RIGHT P/N 2743001111, TO BE MOUNTED AS CLOSELY AS POSSIBLE. THE FERRITE BEAD TO ADC CONNECTION SHOULD NOT BE SHARED WITH ANY OTHER DEVICE.

3) C1–C3 = CHIP CAPACITOR (RECOMMENDED) MOUNTED AS CLOSELY TO THE DEVICE'S PIN AS POSSIBLE

4) USE OF A SEPARATE SUPPLY FOR V_{CC} AND DV_{CC} IS NOT RECOMMENDED

5) R1 PROVIDES CURRENT LIMITING TO 45mA

Figure 2. Typical Interface Circuit

AGND and DGND are the two grounds available on the MAX1170. These two internal grounds are isolated on the device. The use of ground planes is recommended to achieve optimum device performance. DGND is needed for the DV_{CC} return path (40mA typical) and for the return path for all digital output logic interfaces. AGND and DGND should be separated from each other and connected together only at the device through a ferrite bead.

A Schottky or hot carrier diode connected between AGND and V_{EE} is required. The use of separate power supplies between V_{CC} and DV_{CC} is not recommended due to potential power-supply sequencing latchup conditions. Use of the recommended interface circuit shown in Figure 2 will provide optimum device performance for the MAX1170.

Voltage Reference

The MAX1170 requires the use of two voltage references: V_{FT} and V_{FB}. V_{FT} is the force for the top of the voltage reference ladder (+2.5V typical), V_{FB} (-2.5V typical) is the force for the bottom of the voltage reference ladder. Both voltages are applied across an internal reference ladder resistance of 800Ω. The +2.5V voltage source for reference V_{FT} must be current limited to 20mA maximum if a different driving circuit is used in place of the recommended reference circuit shown in Figures 2 and 3.

In addition, there are five reference ladder taps (V_{ST}, VR_{T1}, VR_{T2}, VR_{T3}, and V_{SB}). V_{ST} is the sense for the top of the reference ladder (+2.0V), VR_{T2} is the midpoint of the ladder (0.0V typical), and V_{SB} is the sense for the bottom of the reference ladder (-2.0V). VR_{T1} and VR_{T3} are quarter-point ladder taps (+1.0V and -1.0V typical, respectively). The voltages seen at V_{ST} and V_{SB} are the true full-scale input voltages of the device when V_{FT} and V_{FB} are driven to the recommended voltages (+2.5V and -2.5V typical, respectively). V_{ST} and V_{SB} can be used to monitor the actual full-scale input voltage of the device. VR_{T1}, VR_{T2}, and VR_{T3} should not be driven to the expected ideal values, as is commonly done with standard flash converters. A decoupling capacitor of 0.01µF connected to AGND from each tap is recommended to minimize high-frequency noise injection.

The analog input range will scale proportionally with respect to the reference voltage if a different input range is required. The maximum scaling factor for device operation is ±20% of the recommended reference voltages of V_{FT} and V_{FB}. However, because the MAX1170 is laser trimmed to optimize performance with ±2.5V references, its accuracy will degrade if operated beyond a ±2% range.

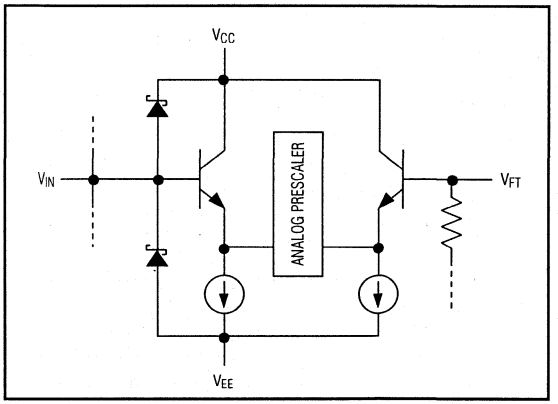


Figure 3. Analog Equivalent Input Circuit

An example of a recommended reference driver circuit is shown in Figure 2. IC1 is REF-03, the +2.5V reference with a tolerance of 0.6% or ±0.015V. The 10kΩ potentiometer supports an adjustable range of 150mV. IC2 is recommended to be an OP-07 or equivalent device. R2 and R3 must be matched to within 0.1% with good TC tracking to maintain a 0.3LSB matching between V_{FT} and V_{FB}. If 0.1% matching is not met, then potentiometer R4 can be used to adjust the V_{FB} voltage to the desired level. Adjust R1 and R4 such that V_{ST} and V_{SB} are exactly +2.0V and -2.0V, respectively.

The following errors are defined:

$$+FS\ error = top\ of\ ladder\ offset\ voltage = \Delta(+FS - V_{ST})$$

$$-FS\ error = bottom\ of\ ladder\ offset\ voltage = \Delta(-FS - V_{SB})$$

Where the +FS (full scale) input voltage is defined as the output 1LSB above the transition of 1–10 and 1–11, and the -FS input voltage is defined as the output 1LSB below the transition of 0–00 and 0–01.

12-Bit, 10Msps, TTL-Output ADC

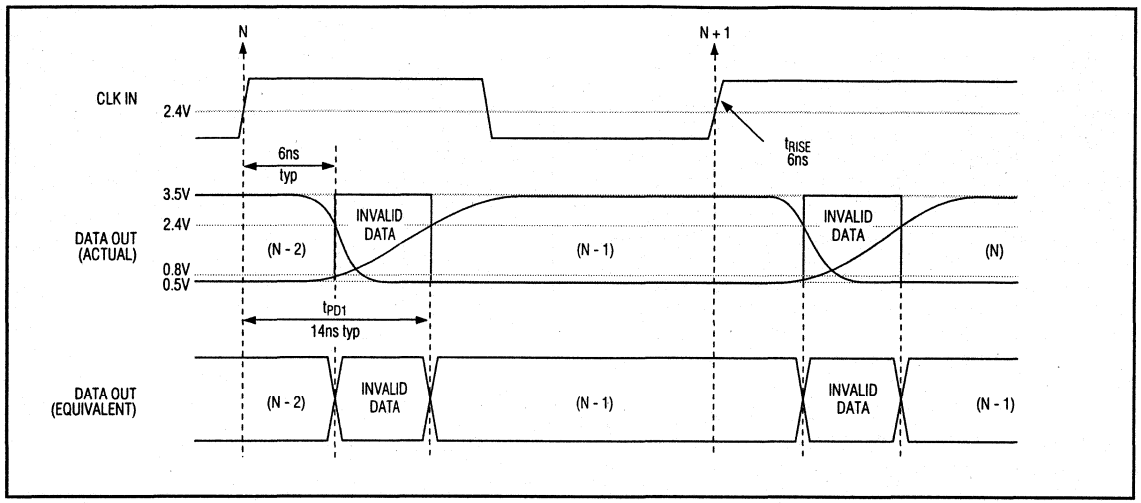


Figure 4. Digital Output Characteristics

Analog Input

V_{IN} is the analog input. The full-scale input range will be 80% of the reference voltage or ±2V with V_{FB} = -2.5V and V_{FT} = +2.5V.

The drive requirements for the analog inputs are minimal compared to those of conventional flash converters, due to the MAX1170's extremely low 5pF input capacitance and high 300kΩ input impedance. For example, for an input signal of ±2Vp-p with an input frequency of 10MHz, the peak output current required for the driving circuit is only 628µA.

Clock Input

The MAX1170 is driven from a single-ended TTL input (CLK). For optimal noise performance, the clock input slew rate should be a minimum of 6ns. Because of this, the use of fast logic is recommended. The clock input duty cycle should be 50% where possible, but performance will not be degraded if kept within the range of 40% to 60%. However, in any case, the clock pulse width (t_{PWH}) must be kept at 300ns maximum to ensure proper operation of the internal track/hold amplifier (Figure 1a). The analog input signal is latched on the rising edge of the CLK.

The clock input must be driven from fast TTL logic ($V_{IH} \leq$ 4.5V, t_{RISE} < 6ns). In the event the clock is driven from a high current source, use a 100Ω resistor (R1, Figure 2) in series to current limit to approximately 45mA.

Digital Outputs

The format of the output data (D0-D11) is straight binary (Table 2). The outputs are latched on the rising edge of CLK with a typical propagation delay of 14ns. There is a one clock cycle latency between CLK and the valid output data (Figure 1a).

The digital outputs' rise times and fall times are not symmetrical. The rise time's typical propagation delay is 14ns, and the typical fall time is 6ns (Figure 4). The nonsymmetrical rise and fall times create approximately 8ns of invalid data.

Table 2. Output Data Information

ANALOG INPUT	OVERRANGE D10	OUTPUT CODE D9–D0
> +2.0V + 1/2LSB	1	11 1111 1111
+2.0V - 1LSB	0	11 1111 111Ø
0.0V	0	ØØ ØØØØ ØØØØ
-2.0V + 1LSB	0	00 0000 000Ø
< -2.0V	0	00 0000 0000

(Ø indicates the flickering bit between logic 0 and 1).

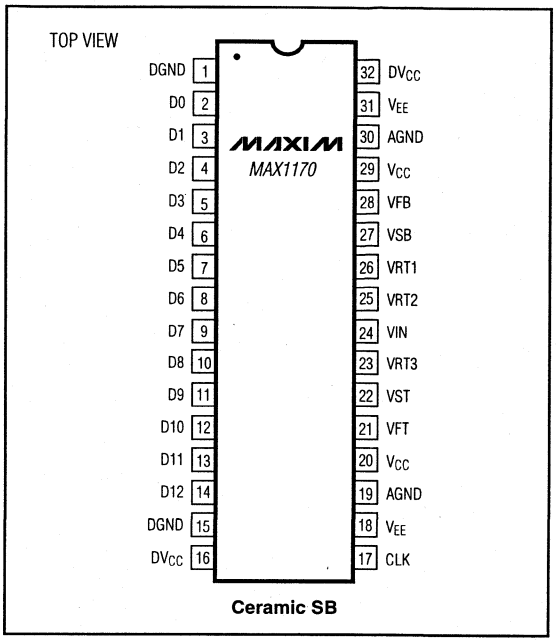
Overrange Output

The overrange output (D12) is an indication that the analog input signal has exceeded the full-scale input voltage by 1LSB. When this condition occurs, the outputs will switch to logic 1s. All other data outputs are unaffected by this operation. This feature makes it possible to include the MAX1170 in higher resolution systems.

Evaluation Board

The MAX1170 evaluation kit (EV kit) is available to aid designers in demonstrating the full performance of the MAX1172 (or of the MAX1170/MAX1171). This board includes a reference circuit, clock driver circuit, output data latches, and on-board reconstruction of the digital data. A separate EV kit manual describing the operation of this board is available. Contact the factory for price and availability.

Pin Configurations (continued)



Ceramic SB

19-1133; Rev 0; 10/96

EVALUATION KIT AVAILABLE

12-Bit, 20Msps, TTL-Output ADC

General Description

The MAX1171 analog-to-digital converter (ADC) is a 12-bit monolithic ADC capable of sample rates greater than 20Msps. An on-board input buffer and track/hold function ensure excellent dynamic performance without the need for external components. A 5pF input capacitance minimizes development problems.

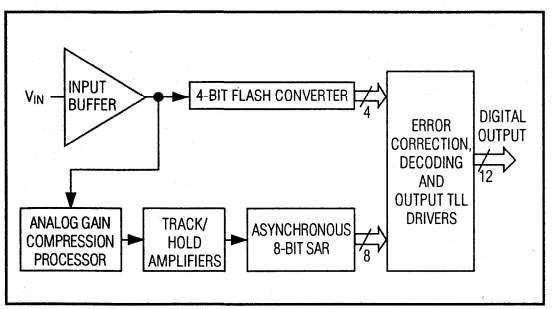
Logic inputs and outputs are TTL compatible. An overrange output signal is provided to indicate overflow conditions. Output data format is straight binary. Power dissipation is a very low 1.1W with power-supply voltages of +5.0V and -5.2V. The MAX1171 also provides a wide input voltage range of ±2.0V.

The MAX1171 is available in a 32-lead ceramic side-brazed package and a 44-lead surface-mount CERQUAD package.

Applications

Radar Receivers
Professional Video
Instrumentation
Imaging
Digital Communications
Digital Spectrum Analyzers

Functional Diagram



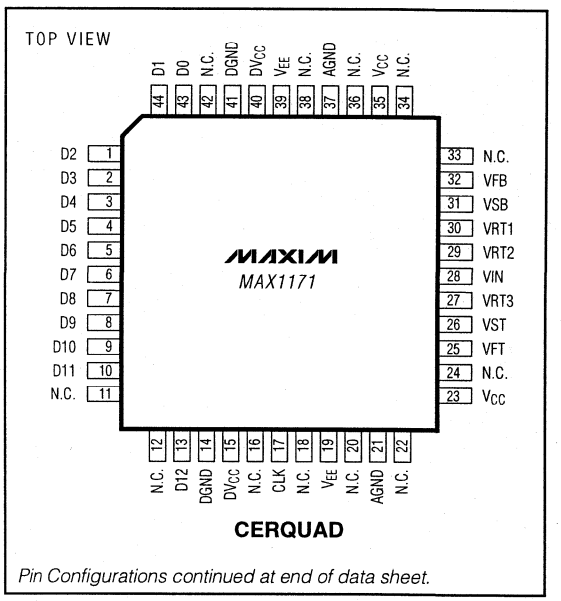
Features

- ♦ **Monolithic, 12-Bit, 20Msps Converter**
- ♦ **On-Chip Track/Hold**
- ♦ **±2.0V Analog Input Range**
- ♦ **66dB SNR at 1MHz Input**
- ♦ **Low Power: 1.1W**
- ♦ **5pF Input Capacitance**
- ♦ **TTL-Compatible Outputs**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1171CDJ	0°C to +70°C	32 Ceramic SB
MAX1171CBH	0°C to +70°C	44 CERQUAD

Pin Configurations



CERQUAD

Pin Configurations continued at end of data sheet.

For the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

12-Bit, 20Msps, TTL-Output ADC

ABSOLUTE MAXIMUM RATINGS

V_{CC} .....+6V
V_{EE} .....-6V
Analog Input .....$V_{FB} \le V_{IN} \le V_{FT}$
VFB, VFT ..... -3.0V, +3.0V
Reference Ladder Current 12mA
CLK IN .....V_{CC}

Digital Outputs.....0mA to -30mA
Operating Temperature Range.....0°C to +70°C
Junction Temperature (T_j).....+175°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functiona operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure t absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5.0V, V_{EE} = -5.2V, DV_{CC} = +5.0V, V_{IN} = ±2.0V, V_{SB} = -2.0V, V_{ST} = +2.0V, f_{CLK} = 20MHz, 50% clock duty cycle $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Resolution			12			Bits
DC ACCURACY (T_A = +25°C)						
Integral Nonlinearity	± full scale	IV		±2.0		LSB
Differential Nonlinearity	250kHz sample rate	IV		±0.8		LSB
No Missing Codes		I		Guaranteed		
ANALOG INPUT						
Input Voltage Range		VI		±2.0		V
Input Bias Current	T_A = +25°C	I		30	60	µA
Input Resistance	V_{IN} = 0V, T_A = +25°C	I	100	300		kΩ
Input Capacitance		V		5		pF
Input Bandwidth	3dB small signal	V		120		MHz
Positive Full-Scale Error		V		±5.0		LSB
Negative Full-Scale Error		V		±5.0		LSB
REFERENCE INPUT						
Reference Ladder Resistance		VI	500	800		Ω
Reference Ladder Tempco		V		0.8		Ω/°C
TIMING CHARACTERISTICS						
Maximum Conversion Rate		VI	20			MHz
Overvoltage Recovery Time		V		20		ns
Pipeline Delay (Latency)		VI			1	Clock Cycle
Output Delay	T_A = +25°C	V		14	18	ns
Aperture Delay Time	T_A = +25°C	V		1		ns
Aperture Jitter Time	T_A = +25°C	V		5		ps-RMS

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5.0V, V_{EE} = -5.2V, DV_{CC} = +5.0V, V_{IN} = ±2.0V, V_{SB} = -2.0V, V_{ST} = +2.0V, f_{CLK} = 20MHz, 50% clock duty cycle, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		TEST LEVEL	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE							
Effective Number of Bits	f_{IN} = 500kHz				10.2		Bits
	f_{IN} = 1MHz				10.0		
	f_{IN} = 3.58MHz				9.5		
Signal-to-Noise Ratio (without Harmonics)	f_{IN} = 500kHz	T_A = +25°C	I	64	67		dB
		T_A = T_{MIN} to T_{MAX}	IV	58	61		
	f_{IN} = 1MHz	T_A = +25°C	I	64	66		
		T_A = T_{MIN} to T_{MAX}	IV	58	60		
	f_{IN} = 3.58MHz	T_A = +25°C	I	62	64		
		T_A = T_{MIN} to T_{MAX}	IV	58	60		
Harmonic Distortion	f_{IN} = 500kHz	T_A = +25°C	I	63	66		dB
		T_A = T_{MIN} to T_{MAX}	IV	59	62		
	f_{IN} = 1MHz	T_A = +25°C	I	63	65		
		T_A = T_{MIN} to T_{MAX}	IV	59	61		
	f_{IN} = 3.58MHz	T_A = +25°C	I	59	61		
		T_A = T_{MIN} to T_{MAX}	IV	57	59		
Signal-to-Noise and Distortion	f_{IN} = 500kHz	T_A = +25°C	I	60	63		dB
		T_A = T_{MIN} to T_{MAX}	IV	55	58		
	f_{IN} = 1MHz	T_A = +25°C	I	60	62		
		T_A = T_{MIN} to T_{MAX}	IV	55	57		
	f_{IN} = 3.58MHz	T_A = +25°C	I	57	59		
		T_A = T_{MIN} to T_{MAX}	IV	54	56		
Spurious-Free Dynamic Range	f_{IN} = 1MHz, T_A = +25°C		V		74		dBc
Differential Phase	f_{IN} = 3.58MHz and 4.35MHz, T_A = +25°C		V		0.2		Degrees
Differential Gain	f_{IN} = 3.58MHz and 4.35MHz, T_A = +25°C		V		0.7		%
DIGITAL INPUTS							
Logic "1" Voltage			V	2.4		4.0	V
Logic "0" Voltage			V			0.8	V
Maximum Input Current Low	T_A = +25°C		I	0	5	20	µA
Maximum Input Current High	T_A = +25°C		I	0	5	20	µA
Pulse Width Low (CLK)			IV	20			ns
Pulse Width High (CLK)			IV	20		300	ns
DIGITAL OUTPUTS							
Logic "1" Voltage	T_A = +25°C		I	2.4			V
Logic "0" Voltage	T_A = +25°C		I			0.6	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5.0V, V_{EE} = -5.2V, DV_{CC} = +5.0V, V_{IN} = ±2.0V, V_{SB} = -2.0V, V_{ST} = +2.0V, f_{CLK} = 20MHz, 50% clock duty cycle $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
POWER-SUPPLY REQUIREMENTS						
Voltages	V_{CC}	IV	4.75	5.0	5.25	V
	DV_{CC}	IV	4.75	5.0	5.25	
	$-V_{EE}$	IV	-4.95	-5.2	-5.45	
Currents	I_{CC}, T_A = +25°C	I		135	150	mA
	DI_{CC}, $T_A = T_{MIN}$ to T_{MAX}	IV		40	55	
	$-I_{EE}$, T_A = +25°C	I		45	70	
Power Dissipation		VI		1.1	1.3	W
Power-Supply Rejection	5V ±0.25V, -5.2V ±0.25V	V		1.0		LSB

Note 1: Typical thermal impedances (unsoldered, in free air):
32 Ceramic SB: θ_{jA} = 50°C/W
44 CERQUAD: θ_{jA} = 78°C/W, θ_{jA} at 1m/s airflow = 58°C/W, θ_{jC} = 3.3°C/W
Use forced-air cooling or heatsinking to maintain $T_j \leq 150°C$.

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

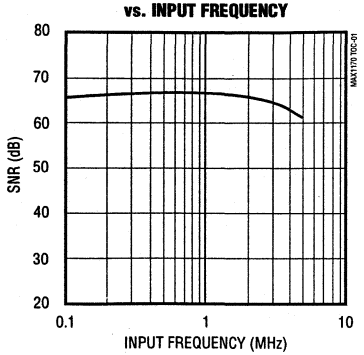
Unless otherwise noted, all tests are pulsed; therefore, $T_j = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = +25°C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = +25°C. Parameter is guaranteed over specified temperature range.

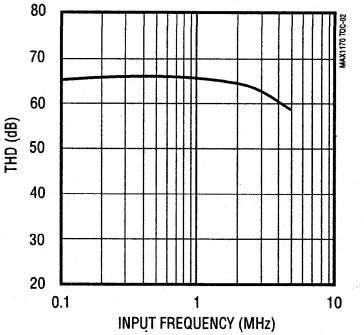
Typical Operating Characteristics

(f_S = 20Msps, f_{IN} = 1MHz, T_A = +25°C, unless otherwise noted.)

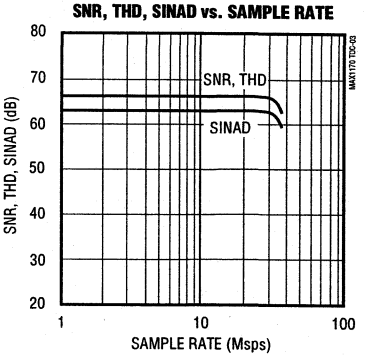
SIGNAL-TO-NOISE RATIO vs. INPUT FREQUENCY



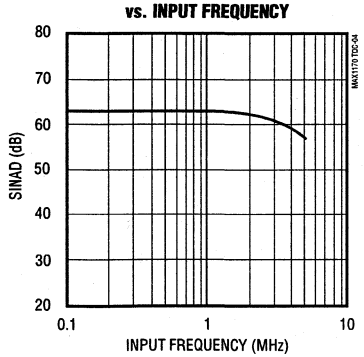
TOTAL HARMONIC DISTORTION vs. INPUT FREQUENCY



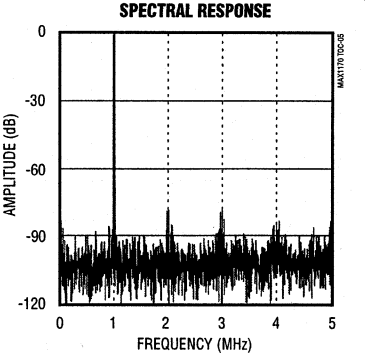
SNR, THD, SINAD vs. SAMPLE RATE



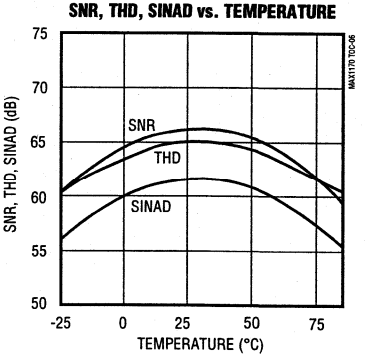
SIGNAL-TO-NOISE AND DISTORTION vs. INPUT FREQUENCY



SPECTRAL RESPONSE



SNR, THD, SINAD vs. TEMPERATURE



12-Bit, 20Msps, TTL-Output ADC

Pin Description

PIN		NAME	FUNCTION
Ceramic SB	CERQUAD		
1, 15	14, 41	DGND	Digital Ground
2–13	43, 44, 1–10	D0–D11	TTL Outputs (D0 = LSB)
14	13	D12	TTL Output Overrange Bit
16, 32	15, 40	DV_{CC}	Digital +5.0V Supply (TTL Outputs)
17	17	CLK	TLL Clock Input
18, 31	19, 39	V_{EE}	-5.2V Supply
19, 30	21, 37	AGND	Analog Ground
20, 29	23, 35	V_{CC}	+5.0V Supply
21	25	VFT	Force for Top of Reference Ladder
22	26	VST	Sense for Top of Reference Ladder
23	27	VRT3	Voltage Reference Tap 3
24	28	VIN	Analog Input, 2.0V typical
25	29	VRT2	Voltage Reference Tap 2
26	30	VRT1	Voltage Reference Tap 1
27	31	VSB	Sense for Bottom of Reference Ladder
28	32	VFB	Force for Bottom of Reference Ladder
—	11, 12, 16, 18, 20, 22, 24, 33, 34, 36, 38, 42	N.C.	No Connection

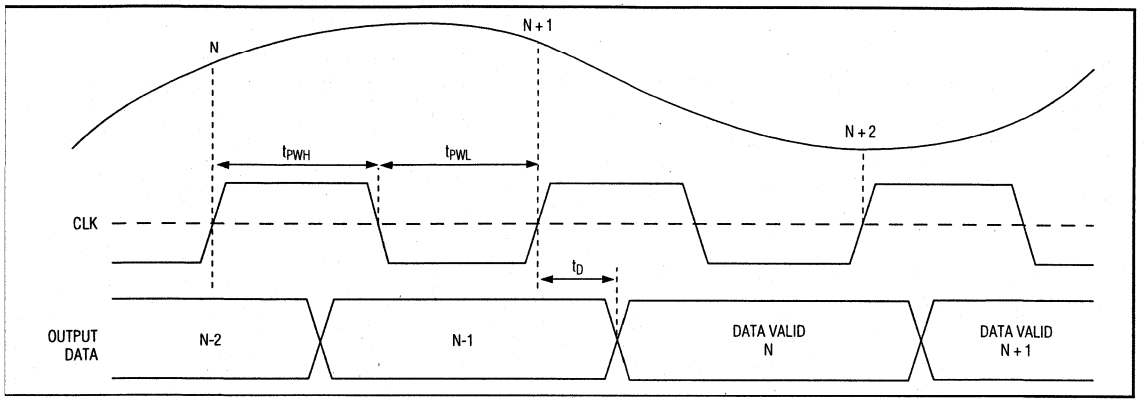


Figure 1a. Timing Diagram

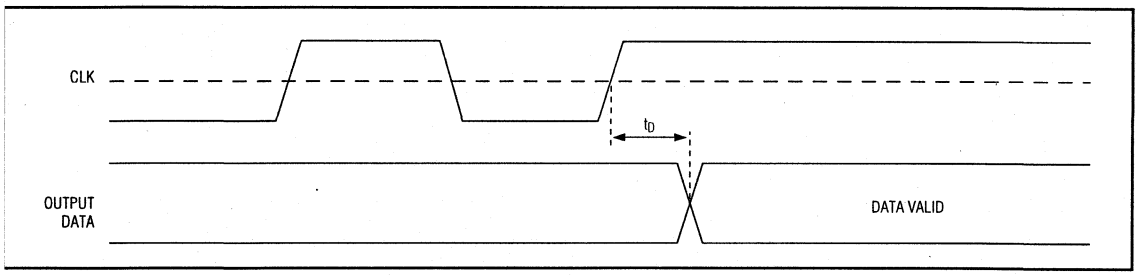


Figure 1b. Single-Event Clock

Table 1. Timing Parameters

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
t_D	CLK to Data Valid Prop Delay		14	18	ns
t_{PWH}	CLK High Pulse Width	20		300	ns
t_{PWL}	CLK Low Pulse Width	20			ns

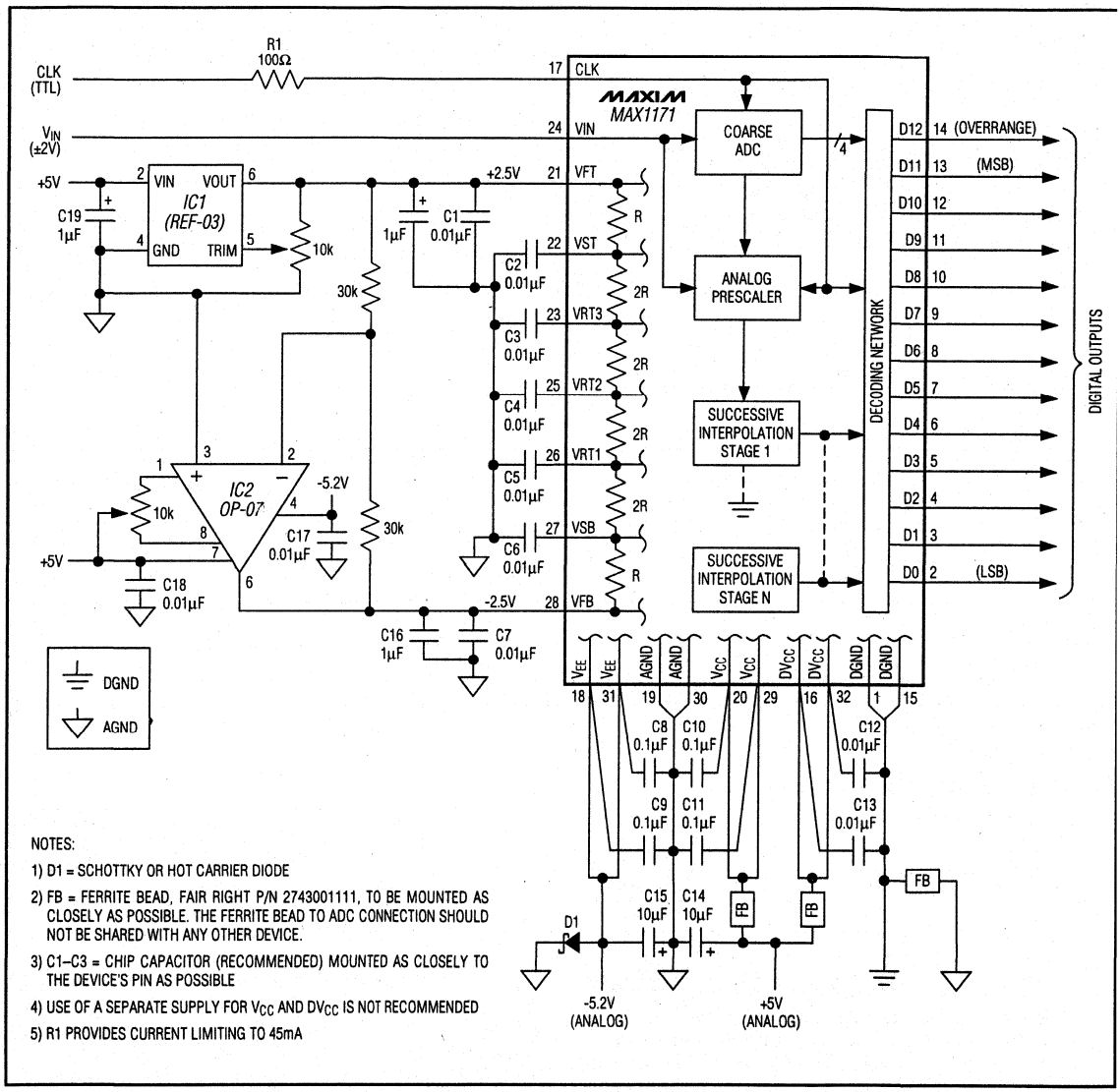
Detailed Description

The MAX1171 requires few external components to achieve the stated operation and performance. Figure 2 shows the typical interface requirements when using the MAX1171 in normal circuit operation. The following section provides a description of the pin functions and outlines critical performance criteria for achieving the optimal device performance.

Power Supplies and Grounding

The MAX1171 requires -5.2V and +5V analog supply voltages. The +5V supply is common to analog V_{CC} and digital DV_{CC}. A ferrite bead in series with each supply line reduces the transient noise injected into the analog V_{CC}. These beads should be connected as close to the device as possible. The connection between the beads and the MAX1171 should not be shared with any other device. Bypass each power-supply pin as close to the device as possible. Use 0.1µF for V_{EE} and V_{CC}, and 0.01µF for DV_{CC} (chip capacitors are preferred).

12-Bit, 20Msps, TTL-Output ADC



NOTES:

1) D1 = SCHOTTKY OR HOT CARRIER DIODE

2) FB = FERRITE BEAD, FAIR RIGHT P/N 2743001111, TO BE MOUNTED AS CLOSELY AS POSSIBLE. THE FERRITE BEAD TO ADC CONNECTION SHOULD NOT BE SHARED WITH ANY OTHER DEVICE.

3) C1–C3 = CHIP CAPACITOR (RECOMMENDED) MOUNTED AS CLOSELY TO THE DEVICE'S PIN AS POSSIBLE

4) USE OF A SEPARATE SUPPLY FOR V_{CC} AND DV_{CC} IS NOT RECOMMENDED

5) R1 PROVIDES CURRENT LIMITING TO 45mA

Figure 2. Typical Interface Circuit

AGND and DGND are the two grounds available on the MAX1171. These two internal grounds are isolated on the device. The use of ground planes is recommended to achieve optimum device performance. DGND is needed for the DV_{CC} return path (40mA typical) and for the return path for all digital output logic interfaces. AGND and DGND should be separated from each other and connected together only at the device through a ferrite bead.

A Schottky or hot carrier diode connected between AGND and V_{EE} is required. The use of separate power supplies between V_{CC} and DV_{CC} is not recommended due to potential power-supply sequencing latchup conditions. Use of the recommended interface circuit shown in Figure 2 will provide optimum device performance for the MAX1171.

Voltage Reference

The MAX1171 requires the use of two voltage references: V_{FT} and V_{FB}. V_{FT} is the force for the top of the voltage reference ladder (+2.5V typical), V_{FB} (-2.5V typical) is the force for the bottom of the voltage reference ladder. Both voltages are applied across an internal reference ladder resistance of 800Ω. The +2.5V voltage source for reference V_{FT} must be current limited to 20mA maximum if a different driving circuit is used in place of the recommended reference circuit shown in Figures 2 and 3.

In addition, there are five reference ladder taps (V_{ST}, VR_{T1}, VR_{T2}, VR_{T3}, and V_{SB}). V_{ST} is the sense for the top of the reference ladder (+2.0V), VR_{T2} is the midpoint of the ladder (0.0V typical), and V_{SB} is the sense for the bottom of the reference ladder (-2.0V). VR_{T1} and VR_{T3} are quarter-point ladder taps (+1.0V and -1.0V typical, respectively). The voltages seen at V_{ST} and V_{SB} are the true full-scale input voltages of the device when V_{FT} and V_{FB} are driven to the recommended voltages (+2.5V and -2.5V typical, respectively). V_{ST} and V_{SB} can be used to monitor the actual full-scale input voltage of the device. VR_{T1}, VR_{T2}, and VR_{T3} should not be driven to the expected ideal values, as is commonly done with standard flash converters. A decoupling capacitor of 0.01µF connected to AGND from each tap is recommended to minimize high-frequency noise injection.

The analog input range will scale proportionally with respect to the reference voltage if a different input range is required. The maximum scaling factor for device operation is ±20% of the recommended reference voltages of V_{FT} and V_{FB}. However, because the MAX1171 is laser trimmed to optimize performance with ±2.5V references, its accuracy will degrade if operated beyond a ±2% range.

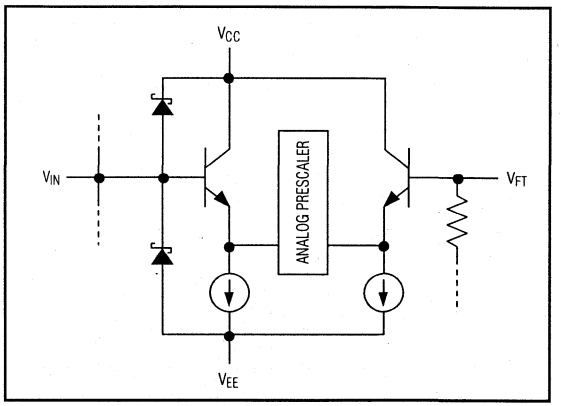


Figure 3. Analog Equivalent Input Circuit

An example of a recommended reference driver circuit is shown in Figure 2. IC1 is REF-03, the +2.5V reference with a tolerance of 0.6% or ±0.015V. The 10kΩ potentiometer supports an adjustable range of 150mV. IC2 is recommended to be an OP-07 or equivalent device. R2 and R3 must be matched to within 0.1% with good TC tracking to maintain a 0.3LSB matching between V_{FT} and V_{FB}. If 0.1% matching is not met, then potentiometer R4 can be used to adjust the V_{FB} voltage to the desired level. Adjust R1 and R4 such that V_{ST} and V_{SB} are exactly +2.0V and -2.0V, respectively.

The following errors are defined:

$$+FS\ error = top\ of\ ladder\ offset\ voltage = \Delta(+FS - V_{ST})$$

$$-FS\ error = bottom\ of\ ladder\ offset\ voltage = \Delta(-FS - V_{SB})$$

Where the +FS (full scale) input voltage is defined as the output 1LSB above the transition of 1–10 and 1–11, and the -FS input voltage is defined as the output 1LSB below the transition of 0–00 and 0–01.

12-Bit, 20Msps, TTL-Output ADC

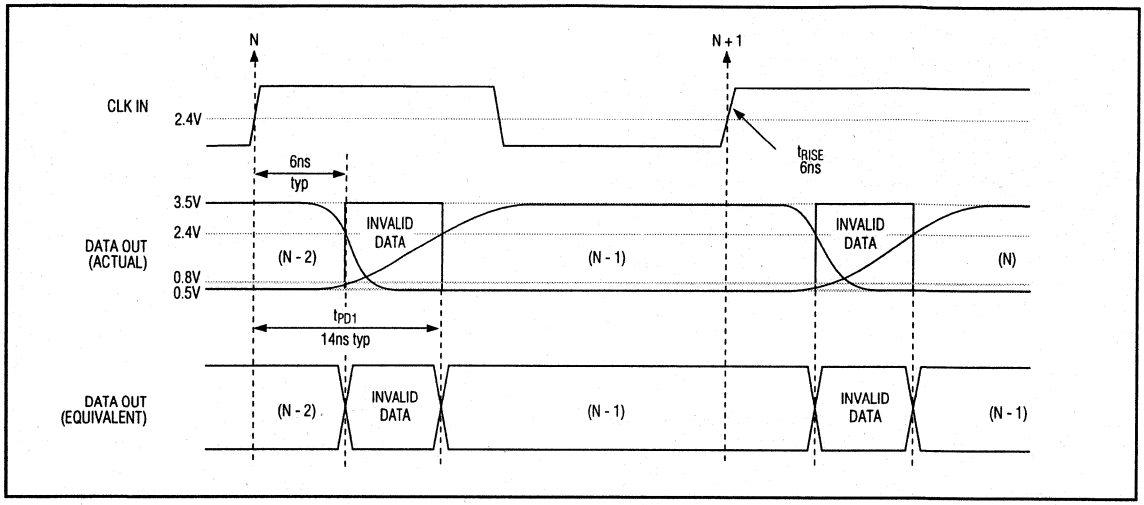


Figure 4. Digital Output Characteristics

Analog Input

V_{IN} is the analog input. The full-scale input range will be 80% of the reference voltage or ±2V with V_{FB} = -2.5V and V_{FT} = +2.5V.

The drive requirements for the analog inputs are minimal compared to those of conventional flash converters, due to the MAX1171's extremely low 5pF input capacitance and high 300kΩ input impedance. For example, for an input signal of ±2Vp-p with an input frequency of 10MHz, the peak output current required for the driving circuit is only 628µA.

Clock Input

The MAX1171 is driven from a single-ended TTL input (CLK). For optimal noise performance, the clock input slew rate should be a minimum of 6ns. Because of this, the use of fast logic is recommended. The clock input duty cycle should be 50% where possible, but performance will not be degraded if kept within the range of 40% to 60%. However, in any case, the clock pulse width (t_{PWH}) must be kept at 300ns maximum to ensure proper operation of the internal track/hold amplifier (Figure 1a). The analog input signal is latched on the rising edge of the CLK.

The clock input must be driven from fast TTL logic ($V_{IH} \leq$ 4.5V, t_{RISE} < 6ns). In the event the clock is driven from a high current source, use a 100Ω resistor (R1, Figure 2) in series to current limit to approximately 45mA.

Digital Outputs

The format of the output data (D0-D11) is straight binary (Table 2). The outputs are latched on the rising edge of CLK with a typical propagation delay of 14ns. There is a one clock cycle latency between CLK and the valid output data (Figure 1a).

The digital outputs' rise times and fall times are not symmetrical. The rise time's typical propagation delay is 14ns, and the typical fall time is 6ns (Figure 4). The nonsymmetrical rise and fall times create approximately 8ns of invalid data.

Table 2. Output Data Information

ANALOG INPUT	OVERRANGE D10	OUTPUT CODE D9–D0
> +2.0V + 1/2LSB	1	11 1111 1111
+2.0V - 1LSB	0	11 1111 111Ø
0.0V	0	ØØ ØØØØ ØØØØ
-2.0V + 1LSB	0	00 0000 000Ø
< -2.0V	0	00 0000 0000

(Ø indicates the flickering bit between logic 0 and 1).

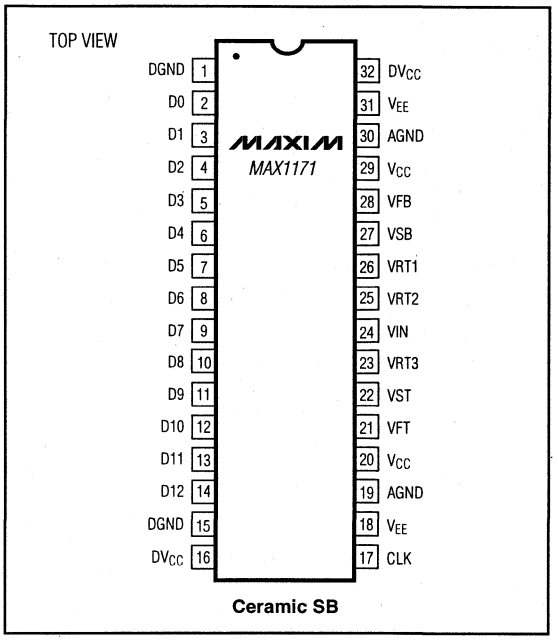
Overrange Output

The overrange output (D12) is an indication that the analog input signal has exceeded the full-scale input voltage by 1LSB. When this condition occurs, the outputs will switch to logic 1s. All other data outputs are unaffected by this operation. This feature makes it possible to include the MAX1171 in higher resolution systems.

Evaluation Board

The MAX1170 evaluation kit (EV kit) is available to aid designers in demonstrating the full performance of the MAX1171 (or of the MAX1170/MAX1172). This board includes a reference circuit, clock driver circuit, output data latches, and on-board reconstruction of the digital data. A separate EV kit manual describing the operation of this board is available. Contact the factory for price and availability.

Pin Configurations (continued)



Ceramic SB

19-1134; Rev 0; 10/96

EVALUATION KIT AVAILABLE

MAXIM

12-Bit, 30Msps, TTL-Output ADC

General Description

The MAX1172 analog-to-digital converter (ADC) is a 12-bit monolithic ADC capable of sample rates greater than 30Msps. An on-board input buffer and track/hold function ensure excellent dynamic performance without the need for external components. A 5pF input capacitance minimizes development problems.

Logic inputs and outputs are TTL compatible. An overrange output signal is provided to indicate overflow conditions. Output data format is straight binary. Power dissipation is a very low 1.1W with power-supply voltages of +5.0V and -5.2V. The MAX1172 also provides a wide input voltage range of ±2.0V.

The MAX1172 is available in a 32-lead ceramic side-brazed package and a 44-lead surface-mount CERQUAD package.

Features

- ♦ **Monolithic, 12-Bit, 30Msps Converter**
- ♦ **On-Chip Track/Hold**
- ♦ **±2.0V Analog Input Range**
- ♦ **High Input Impedance**
- ♦ **66dB SNR at 1MHz Input**
- ♦ **Low Power: 1.1W**
- ♦ **5pF Input Capacitance**
- ♦ **TTL-Compatible Outputs**

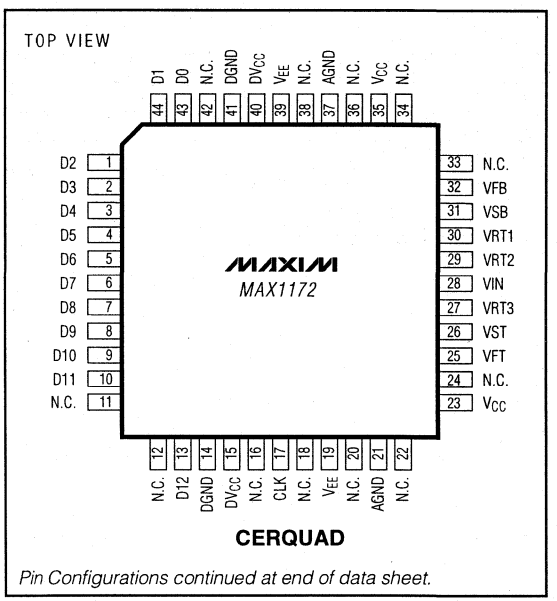
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1172CDJ	0°C to +70°C	32 Ceramic SB
MAX1172CBH	0°C to +70°C	44 CERQUAD

Applications

Radar Receivers
Professional Video
Instrumentation
Imaging
Digital Communications
Digital Spectrum Analyzers

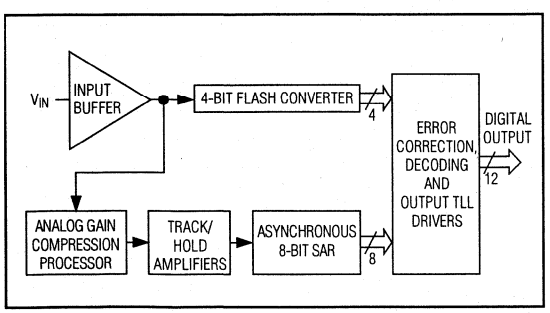
Pin Configurations



CERQUAD

Pin Configurations continued at end of data sheet.

Functional Diagram



For the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

12-Bit, 30Msps, TTL-Output ADC

ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... +6V
V_{EE} ..... -6V
Analog Input ..... $V_{FB} \le V_{IN} \le V_{FT}$
VFB, VFT ..... -3.0V, +3.0V
Reference Ladder Current 12mA
CLK IN ..... V_{CC}

Digital Outputs ..... 0mA to -30mA
Operating Temperature Range ..... 0°C to +70°C
Junction Temperature (T_J) ..... +175°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functiona operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure tc absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5.0V, V_{EE} = -5.2V, DV_{CC} = +5.0V, V_{IN} = ±2.0V, V_{SB} = -2.0V, V_{ST} = +2.0V, f_{CLK} = 30MHz, 50% clock duty cycle, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Resolution			12			Bits
DC ACCURACY (T_A = +25°C)						
Integral Nonlinearity	± full scale	IV		±2.0		LSB
Differential Nonlinearity	250kHz sample rate	IV		±0.8		LSB
No Missing Codes		I		Guaranteed		
ANALOG INPUT						
Input Voltage Range		VI		±2.0		V
Input Bias Current	T_A = +25°C	I		30	60	µA
Input Resistance	V_{IN} = 0V, T_A = +25°C	I	100	300		kΩ
Input Capacitance		V		5		pF
Input Bandwidth	3dB small signal	V		120		MHz
Positive Full-Scale Error		V		±5.0		LSB
Negative Full-Scale Error		V		±5.0		LSB
REFERENCE INPUT						
Reference Ladder Resistance		VI	500	800		Ω
Reference Ladder Tempco		V		0.8		Ω/°C
TIMING CHARACTERISTICS						
Maximum Conversion Rate		VI	30	40		MHz
Overvoltage Recovery Time		V		20		ns
Pipeline Delay (Latency)		VI			1	Clock Cycle
Output Delay	T_A = +25°C	V		14	18	ns
Aperture Delay Time	T_A = +25°C	V		1		ns
Aperture Jitter Time	T_A = +25°C	V		5		ps-RMS

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5.0V, V_{EE} = -5.2V, DV_{CC} = +5.0V, V_{IN} = ±2.0V, V_{SB} = -2.0V, V_{ST} = +2.0V, f_{CLK} = 30MHz, 50% clock duty cycle, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		TEST LEVEL	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE							
Effective Number of Bits	f_{IN} = 500kHz				10.0		Bits
	f_{IN} = 1MHz				9.8		
	f_{IN} = 3.58MHz				9.5		
Signal-to-Noise Ratio (without Harmonics)	f_{IN} = 500kHz	T_A = +25°C	I	63	66		dB
		T_A = T_{MIN} to T_{MAX}	IV	58	61		
	f_{IN} = 1MHz	T_A = +25°C	I	63	65		
		T_A = T_{MIN} to T_{MAX}	IV	58	60		
	f_{IN} = 3.58MHz	T_A = +25°C	I	62	64		
		T_A = T_{MIN} to T_{MAX}	IV	58	60		
Harmonic Distortion	f_{IN} = 500kHz	T_A = +25°C	I	63	65		dB
		T_A = T_{MIN} to T_{MAX}	IV	59	61		
	f_{IN} = 1MHz	T_A = +25°C	I	62	64		
		T_A = T_{MIN} to T_{MAX}	IV	58	60		
	f_{IN} = 3.58MHz	T_A = +25°C	I	59	61		
		T_A = T_{MIN} to T_{MAX}	IV	57	59		
Signal-to-Noise and Distortion	f_{IN} = 500kHz	T_A = +25°C	I	60	62		dB
		T_A = T_{MIN} to T_{MAX}	IV	55	57		
	f_{IN} = 1MHz	T_A = +25°C	I	59	61		
		T_A = T_{MIN} to T_{MAX}	IV	55	57		
	f_{IN} = 3.58MHz	T_A = +25°C	I	57	59		
		T_A = T_{MIN} to T_{MAX}	IV	54	56		
Spurious-Free Dynamic Range	f_{IN} = 1MHz, T_A = +25°C		V		74		dBc
Differential Phase	f_{IN} = 3.58MHz and 4.35MHz, T_A = +25°C		V		0.2		Degrees
Differential Gain	f_{IN} = 3.58MHz and 4.35MHz, T_A = +25°C		V		0.7		%
DIGITAL INPUTS							
Logic "1" Voltage			V	2.4		4.0	V
Logic "0" Voltage			V			0.8	V
Maximum Input Current Low	T_A = +25°C		I	0	5	20	µA
Maximum Input Current High	T_A = +25°C		I	0	5	20	µA
Pulse Width Low (CLK)			IV	15			ns
Pulse Width High (CLK)			IV	15		300	ns
DIGITAL OUTPUTS							
Logic "1" Voltage	T_A = +25°C		I	2.4			V
Logic "0" Voltage	T_A = +25°C		I			0.6	V

12-Bit, 30Msps, TTL-Output ADC

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5.0V, V_{EE} = -5.2V, DV_{CC} = +5.0V, V_{IN} = ±2.0V, V_{SB} = -2.0V, V_{ST} = +2.0V, f_{CLK} = 30MHz, 50% clock duty cycle $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
POWER-SUPPLY REQUIREMENTS						
Voltages	V_{CC}	IV	4.75	5.0	5.25	V
	DV_{CC}	IV	4.75	5.0	5.25	
	$-V_{EE}$	IV	-4.95	-5.2	-5.45	
Currents	I_{CC}, T_A = +25°C	I		135	150	mA
	DI_{CC}, $T_A = T_{MIN}$ to T_{MAX}	IV		40	55	
	$-I_{EE}$, T_A = +25°C	I		45	70	
Power Dissipation		VI		1.1	1.3	W
Power-Supply Rejection	5V ±0.25V, -5.2V ±0.25V	V		1.0		LSB

Note 1: Typical thermal impedances (unsoldered, in free air):
32 Ceramic SB: θ_{jA} = 50°C/W
44 CERQUAD: θ_{jA} = 78°C/W, θ_{jA} at 1m/s airflow = 58°C/W, θ_{jC} = 3.3°C/W
Use forced-air cooling or heatsinking to maintain $T_j \leq 150°C$.

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

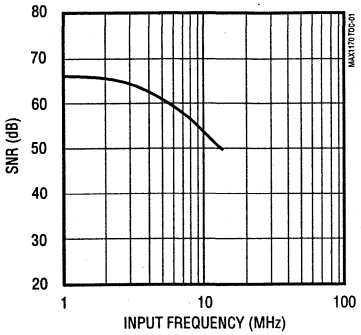
Unless otherwise noted, all tests are pulsed; therefore, $T_j = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = +25°C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = +25°C. Parameter is guaranteed over specified temperature range.

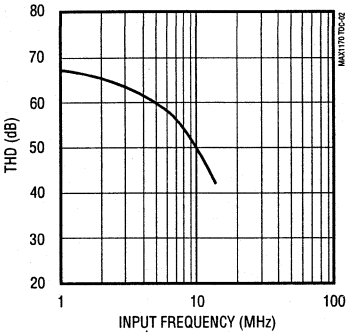
Typical Operating Characteristics

(f_S = 30Msps, f_{IN} = 1MHz, T_A = +25°C, unless otherwise noted.)

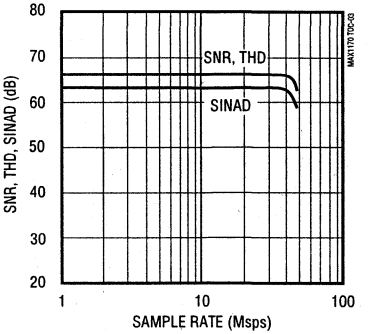
SIGNAL-TO-NOISE RATIO vs. INPUT FREQUENCY



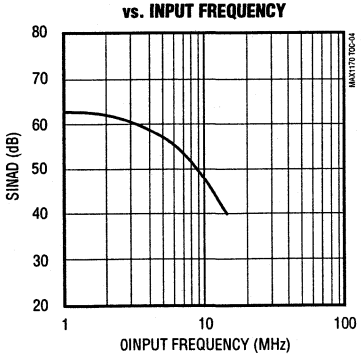
TOTAL HARMONIC DISTORTION vs. INPUT FREQUENCY



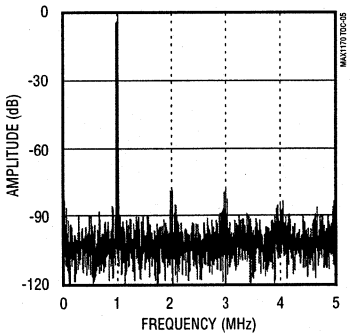
SNR, THD, SINAD vs. SAMPLE RATE



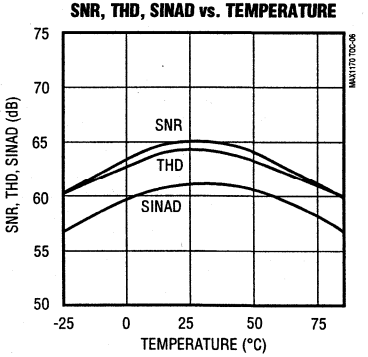
SIGNAL-TO-NOISE AND DISTORTION vs. INPUT FREQUENCY



SPECTRAL RESPONSE



SNR, THD, SINAD vs. TEMPERATURE



7

12-Bit, 30Msps, TTL-Output ADC

Pin Description

PIN		NAME	FUNCTION
Ceramic SB	CERQUAD		
1, 15	14, 41	DGND	Digital Ground
2–13	43, 44, 1–10	D0–D11	TTL Outputs (D0 = LSB)
14	13	D12	TTL Output Overrange Bit
16, 32	15, 40	DV_{CC}	Digital +5.0V Supply (TTL Outputs)
17	17	CLK	TLL Clock Input
18, 31	19, 39	V_{EE}	-5.2V Supply
19, 30	21, 37	AGND	Analog Ground
20, 29	23, 35	V_{CC}	+5.0V Supply
21	25	VFT	Force for Top of Reference Ladder
22	26	VST	Sense for Top of Reference Ladder
23	27	VRT3	Voltage Reference Tap 3
24	28	VIN	Analog Input, ±2.0V typical
25	29	VRT2	Voltage Reference Tap 2
26	30	VRT1	Voltage Reference Tap 1
27	31	VSB	Sense for Bottom of Reference Ladder
28	32	VFB	Force for Bottom of Reference Ladder
—	11, 12, 16, 18, 20, 22, 24, 33, 34, 36, 38, 42	N.C.	No Connection

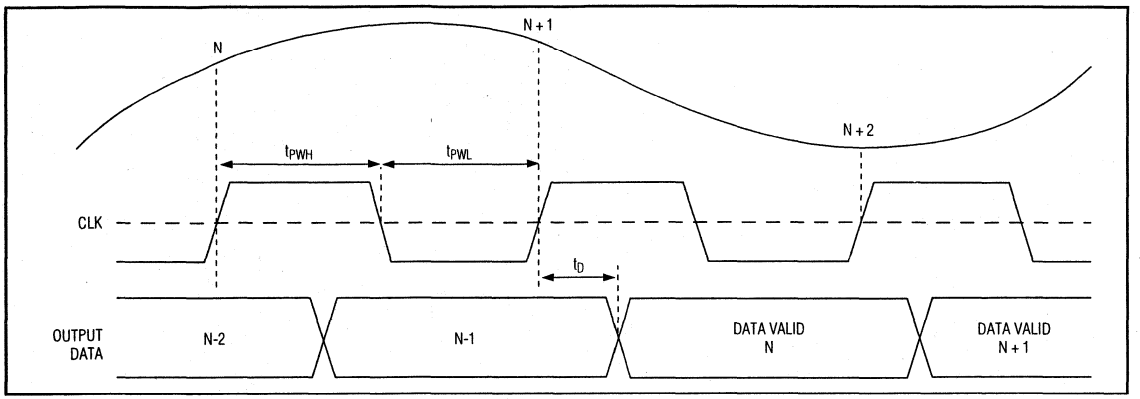


Figure 1a. Timing Diagram

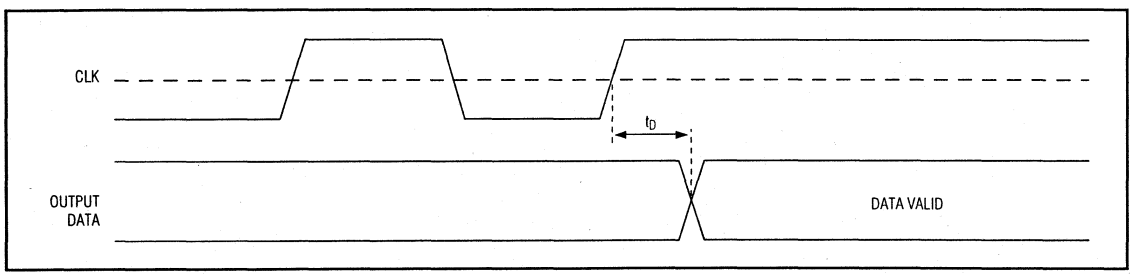


Figure 1b. Single-Event Clock

Table 1. Timing Parameters

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
t_D	CLK to Data Valid Prop Delay		14	18	ns
t_{PWH}	CLK High Pulse Width	15		300	ns
t_{PWL}	CLK Low Pulse Width	15			ns

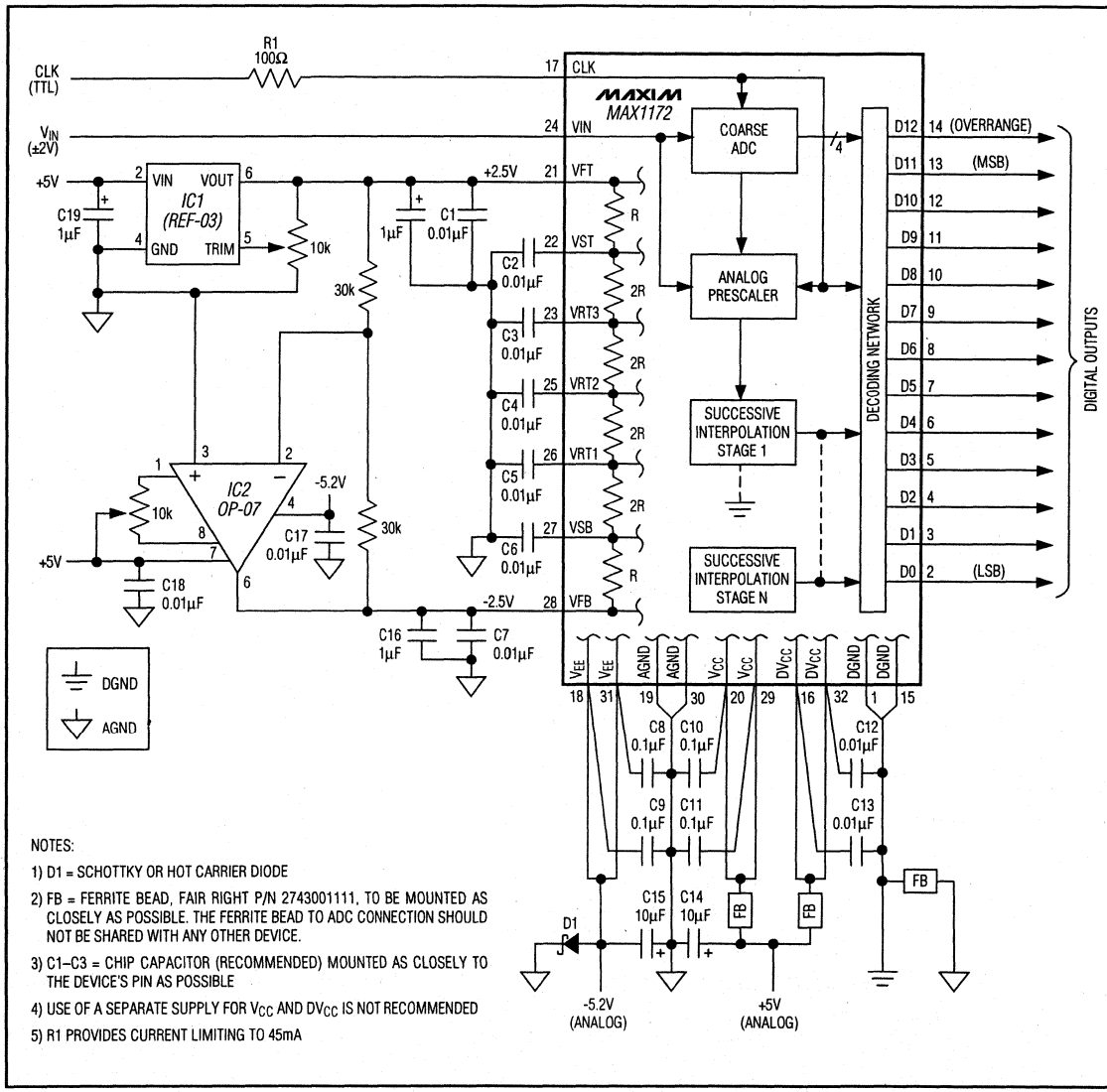
Detailed Description

The MAX1172 requires few external components to achieve the stated operation and performance. Figure 2 shows the typical interface requirements when using the MAX1172 in normal circuit operation. The following section provides a description of the pin functions and outlines critical performance criteria for achieving the optimal device performance.

Power Supplies and Grounding

The MAX1172 requires -5.2V and +5V analog supply voltages. The +5V supply is common to analog V_{CC} and digital DV_{CC}. A ferrite bead in series with each supply line reduces the transient noise injected into the analog V_{CC}. These beads should be connected as close to the device as possible. The connection between the beads and the MAX1172 should not be shared with any other device. Bypass each power-supply pin as close to the device as possible. Use 0.1µF for V_{EE} and V_{CC}, and 0.01µF for DV_{CC} (chip capacitors are preferred).

12-Bit, 30Msps, TTL-Output ADC



NOTES:

1) D1 = SCHOTTKY OR HOT CARRIER DIODE

2) FB = FERRITE BEAD, FAIR RIGHT P/N 2743001111, TO BE MOUNTED AS CLOSELY AS POSSIBLE. THE FERRITE BEAD TO ADC CONNECTION SHOULD NOT BE SHARED WITH ANY OTHER DEVICE.

3) C1–C3 = CHIP CAPACITOR (RECOMMENDED) MOUNTED AS CLOSELY TO THE DEVICE'S PIN AS POSSIBLE

4) USE OF A SEPARATE SUPPLY FOR V_{CC} AND DV_{CC} IS NOT RECOMMENDED

5) R1 PROVIDES CURRENT LIMITING TO 45mA

Figure 2. Typical Interface Circuit

AGND and DGND are the two grounds available on the MAX1172. These two internal grounds are isolated on the device. The use of ground planes is recommended to achieve optimum device performance. DGND is needed for the DV_{CC} return path (40mA typical) and for the return path for all digital output logic interfaces. AGND and DGND should be separated from each other and connected together only at the device through a ferrite bead.

A Schottky or hot carrier diode connected between AGND and V_{EE} is required. The use of separate power supplies between V_{CC} and DV_{CC} is not recommended due to potential power-supply sequencing latchup conditions. Use of the recommended interface circuit shown in Figure 2 will provide optimum device performance for the MAX1172.

Voltage Reference

The MAX1172 requires the use of two voltage references: V_{FT} and V_{FB}. V_{FT} is the force for the top of the voltage reference ladder (+2.5V typical), V_{FB} (-2.5V typical) is the force for the bottom of the voltage reference ladder. Both voltages are applied across an internal reference ladder resistance of 800Ω. The +2.5V voltage source for reference V_{FT} must be current limited to 20mA maximum if a different driving circuit is used in place of the recommended reference circuit shown in Figures 2 and 3.

In addition, there are five reference ladder taps (V_{ST}, VR_{T1}, VR_{T2}, VR_{T3}, and V_{SB}). V_{ST} is the sense for the top of the reference ladder (+2.0V), VR_{T2} is the midpoint of the ladder (0.0V typical), and V_{SB} is the sense for the bottom of the reference ladder (-2.0V). VR_{T1} and VR_{T3} are quarter-point ladder taps (+1.0V and -1.0V typical, respectively). The voltages seen at V_{ST} and V_{SB} are the true full-scale input voltages of the device when V_{FT} and V_{FB} are driven to the recommended voltages (+2.5V and -2.5V typical, respectively). V_{ST} and V_{SB} can be used to monitor the actual full-scale input voltage of the device. VR_{T1}, VR_{T2}, and VR_{T3} should not be driven to the expected ideal values, as is commonly done with standard flash converters. A decoupling capacitor of 0.01µF connected to AGND from each tap is recommended to minimize high-frequency noise injection.

The analog input range will scale proportionally with respect to the reference voltage if a different input range is required. The maximum scaling factor for device operation is ±20% of the recommended reference voltages of V_{FT} and V_{FB}. However, because the MAX1172 is laser trimmed to optimize performance with ±2.5V references, its accuracy will degrade if operated beyond a ±2% range.

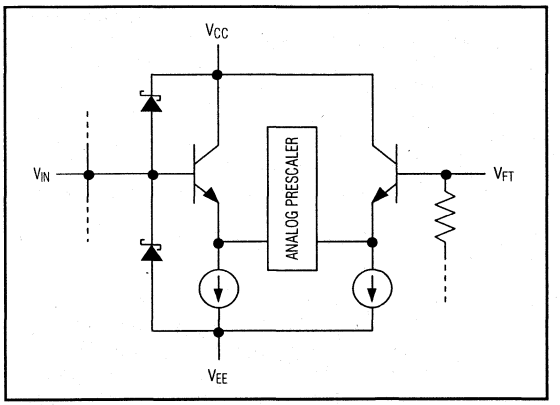


Figure 3. Analog Equivalent Input Circuit

An example of a recommended reference driver circuit is shown in Figure 2. IC1 is REF-03, the +2.5V reference with a tolerance of 0.6% or ±0.015V. The 10kΩ potentiometer supports an adjustable range of 150mV. IC2 is recommended to be an OP-07 or equivalent device. R2 and R3 must be matched to within 0.1% with good TC tracking to maintain a 0.3LSB matching between V_{FT} and V_{FB}. If 0.1% matching is not met, then potentiometer R4 can be used to adjust the V_{FB} voltage to the desired level. Adjust R1 and R4 such that V_{ST} and V_{SB} are exactly +2.0V and -2.0V, respectively.

The following errors are defined:

+FS error = top of ladder offset voltage
= Δ(+FS - V_{ST})

-FS error = bottom of ladder offset voltage
= Δ(-FS - V_{SB})

Where the +FS (full scale) input voltage is defined as the output 1LSB above the transition of 1–10 and 1–11, and the -FS input voltage is defined as the output 1LSB below the transition of 0–00 and 0–01.

12-Bit, 30Msps, TTL-Output ADC

Analog Input

V_{IN} is the analog input. The full-scale input range will be 80% of the reference voltage or ±2V with V_{FB} = -2.5V and V_{FT} = +2.5V.

The drive requirements for the analog inputs are minimal compared to those of conventional flash converters, due to the MAX1172's extremely low 5pF input capacitance and high 300kΩ input impedance. For example, for an input signal of ±2Vp-p with an input frequency of 10MHz, the peak output current required for the driving circuit is only 628µA.

Clock Input

The MAX1172 is driven from a single-ended TTL input (CLK). The clock pulse width (t_{PWH}) must be kept between 15ns and 300ns to ensure proper operation of the internal track/hold amplifier (Figure 1a). When operating the MAX1172 at sampling rates above 3Msps, it is recommended that the clock input duty cycle be kept at 50% to optimize performance (Figure 4). The analog input signal is latched on the rising edge of the CLK.

The clock input must be driven from fast TTL logic (V_{IH} ≤ 4.5V, t_{RISE} < 6ns). In the event the clock is driven from a high current source, use a 100Ω (R1, Figure 2) resistor in series to current limit to approximately 45mA.

Digital Outputs

The format of the output data (D0-D11) is straight binary (Table 2). The outputs are latched on the rising edge of CLK with a typical propagation delay of 14ns. There is a one clock cycle latency between CLK and the valid output data (Figure 1a).

The digital outputs' rise times and fall times are not symmetrical. The rise time's typical propagation delay is 14ns, and the typical fall time is 6ns (Figure 5). The nonsymmetrical rise and fall times create approximately 8ns of invalid data.

Table 2. Output Data Information

ANALOG INPUT	OVERRANGE D10	OUTPUT CODE D9–D0
> +2.0V + 1/2LSB	1	11 1111 1111
+2.0V - 1LSB	0	11 1111 111Ø
0.0V	0	ØØ ØØØØ ØØØØ
-2.0V + 1LSB	0	00 0000 000Ø
< -2.0V	0	00 0000 0000

(Ø indicates the flickering bit between logic 0 and 1).

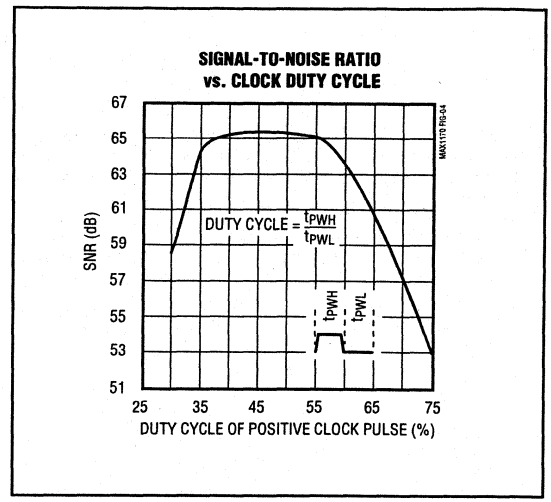


Figure 4. Signal-to-Noise Ratio vs. Clock Duty Cycle

Overrange Output

The overrange output (D12) is an indication that the analog input signal has exceeded the full-scale input voltage by 1LSB. When this condition occurs, the outputs will switch to logic 1s. All other data outputs are unaffected by this operation. This feature makes it possible to include the MAX1172 in higher resolution systems.

Evaluation Board

The MAX1170 evaluation kit (EV kit) is available to aid designers in demonstrating the full performance of the MAX1172 (or of the MAX1170/MAX1171). This board includes a reference circuit, clock driver circuit, output data latches, and on-board reconstruction of the digital data. A separate EV kit manual describing the operation of this board is available. Contact the factory for price and availability.

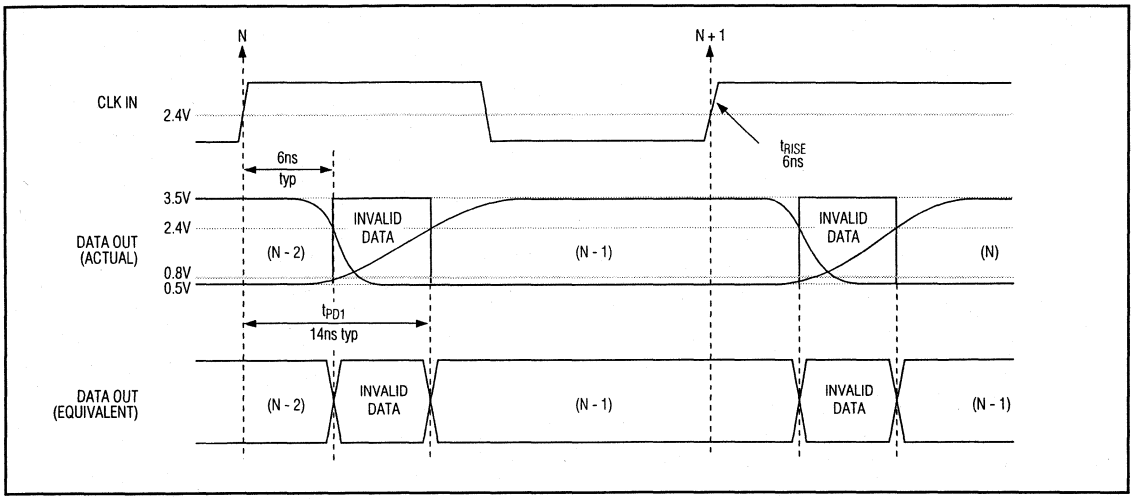
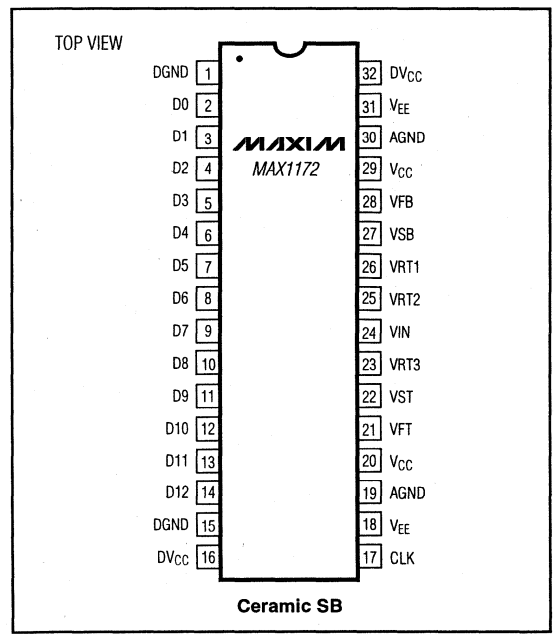


Figure 5. Digital Output Characteristics

Pin Configurations (continued)



ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
1/96

MAXIM

Low-Power, 8-Channel, Serial 12-Bit ADC with Adjustable Output Logic Level

General Description

The MAX1202 is a 12-bit data-acquisition system specifically designed for use in applications with mixed -5V (analog) and +3V (digital) supply voltages. It operates with a single +5V supply or with ±5V supplies, and combines an 8-channel multiplexer, high-bandwidth track/hold, and serial interface with high conversion speed and low power consumption.

A 4-wire serial interface connects directly to SPI™/Microwire™ devices without external logic, and a serial strobe output allows direct connection to TMS320-family digital signal processors. The MAX1202 uses either the internal clock or an external serial-interface clock to perform successive-approximation A/D conversions. The serial interface operates at up to 2MHz.

The MAX1202 features an internal 4.096V reference and a reference-buffer amplifier that simplifies gain trim. It also has a VL pin that is the power supply for the digital outputs. Output logic levels (3V, 3.3V, or 5V) are determined by the value of the voltage applied to this pin.

A hard-wired $\overline{SHDN}$ pin and two software-selectable power-down modes are provided. Accessing the serial interface automatically powers up the device. A quick turn-on time enables the MAX1202 to be shut down between conversions, allowing the user to optimize supply currents. By customizing power-down between conversions, supply current can drop below 10µA at reduced sampling rates.

The MAX1202 is available in a 20-pin DIP package, and in a small SSOP, which occupies 30% less area than an 8-pin DIP.

Applications

5V/3V Mixed-Supply Systems
Data Acquisition
High-Accuracy Process Control
Battery-Powered Instruments
Medical Instruments

SPI is a registered trademark of Motorola, Inc.
Microwire is a registered trademark of National Semiconductor Corp.

Features

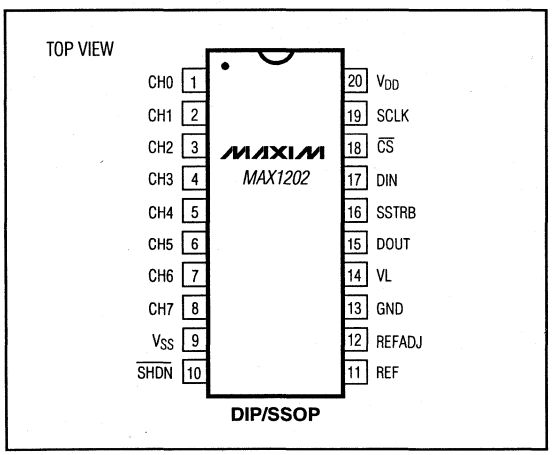
- **8-Channel Single-Ended or 4-Channel Differential Inputs**
- **Single +5V or ±5V Supply Operation**
- **Software-Configurable Unipolar/Bipolar Inputs**
- **User-Selectable Output Logic Levels (2.7V to 5.25V)**
- **Low Power: 1.5mA (operating mode) 2µA (power-down mode)**
- **Internal Track/Hold, 133kHz Sampling Rate**
- **Internal 4.096V Reference**
- **SPI/Microwire/TMS320-Compatible 4-Wire Serial Interface**
- **20-Pin DIP/SSOP Package**
- **Evaluation Kit Will Be Available**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX1202ACPP	0°C to +70°C	20 Plastic DIP	±1/2
MAX1202BCPP	0°C to +70°C	20 Plastic DIP	±1
MAX1202ACAP	0°C to +70°C	20 SSOP	±1/2
MAX1202BCAP	0°C to +70°C	20 SSOP	±1
MAX1202BC/D	0°C to +70°C	Dice*	±1

Ordering Information continued on next page.
**Dice are specified at T_A = +25°C, DC parameters only.*

Pin Configuration



7

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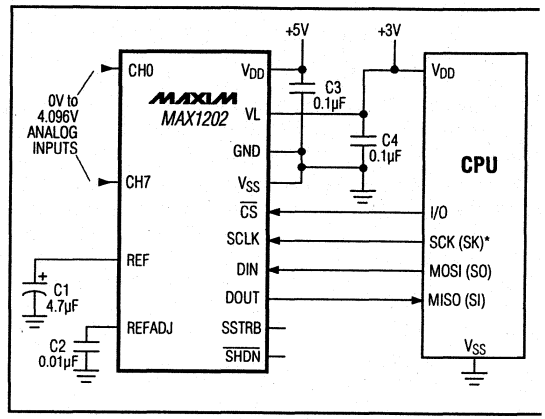
Low-Power, 8-Channel, Serial 12-Bit ADC with Adjustable Output Logic Level

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX1202AEPP	-40°C to +85°C	20 Plastic DIP	±1/2
MAX1202BEPP	-40°C to +85°C	20 Plastic DIP	±1
MAX1202AEAP	-40°C to +85°C	20 SSOP	±1/2
MAX1202BEAP	-40°C to +85°C	20 SSOP	±1
MAX1202BMJP	-55°C to +125°C	20 CERDIP**	±1

***Contact factory for availability.*

_____Typical Operating Circui



ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
11/96

MAXIM

Low-Power, 8-Channel, Serial 10-Bit ADC with Adjustable Output Logic Level

General Description

The MAX1204 is a 10-bit data-acquisition system specifically designed for use in applications with mixed +5V (analog) and +3V (digital) supply voltages. It operates with a single +5V supply or with ±5V supplies, and combines an 8-channel multiplexer, high-bandwidth track/hold, and serial interface with high conversion speed and low power consumption.

A 4-wire serial interface connects directly to SPI™/Microwire™ devices without external logic, and a serial strobe output allows direct connection to TMS320-family digital signal processors. The MAX1204 uses either the internal clock or an external serial-interface clock to perform successive-approximation A/D conversions. The serial interface operates at up to 2MHz.

The MAX1204 features an internal 4.096V reference and a reference-buffer amplifier that simplifies gain trim. It also has a VL pin that is the power supply for the digital outputs. Output logic levels (3V, 3.3V, or 5V) are determined by the value of the voltage applied to this pin.

A hard-wired $\overline{SHDN}$ pin and two software-selectable power-down modes are provided. Accessing the serial interface automatically powers up the device. A quick turn-on time enables the MAX1204 to be shut down between conversions, allowing the user to optimize supply currents. By customizing power-down between conversions, supply current can drop below 10µA at reduced sampling rates.

The MAX1204 is available in a 20-pin DIP package, and in a small SSOP, which occupies 30% less area than an 8-pin DIP.

Applications

5V/3V Mixed-Supply Systems
Data Acquisition
Sensor-Based Systems
Process Control
Battery-Powered Instruments
Medical Instruments

SPI is a registered trademark of Motorola, Inc.
Microwire is a registered trademark of National Semiconductor Corp.

Features

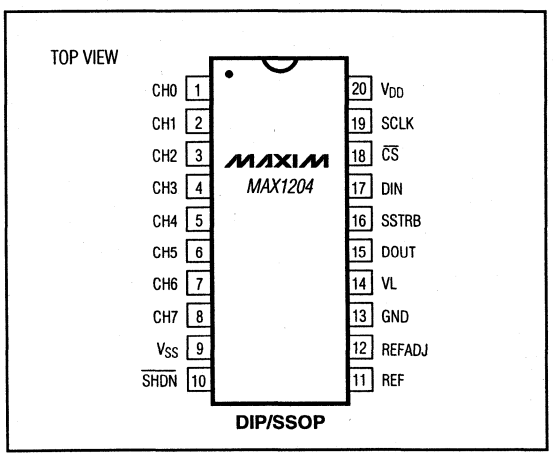
- **8-Channel Single-Ended or 4-Channel Differential Inputs**
- **Single +5V or ±5V Supply Operation**
- **Software-Configurable Unipolar/Bipolar Inputs**
- **User-Selectable Output Logic Levels (2.7V to 5.25V)**
- **Low Power: 1.5mA (operating mode) 2µA (power-down mode)**
- **Internal Track/Hold, 133kHz Sampling Rate**
- **Internal 4.096V Reference**
- **SPI/Microwire/TMS320-Compatible 4-Wire Serial Interface**
- **20-Pin DIP/SSOP Package**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX1204ACPP	0°C to +70°C	20 Plastic DIP	±1/2
MAX1204BCPP	0°C to +70°C	20 Plastic DIP	±1
MAX1204ACAP	0°C to +70°C	20 SSOP	±1/2
MAX1204BCAP	0°C to +70°C	20 SSOP	±1

Ordering Information continued on next page.

Pin Configuration



DIP/SSOP

7

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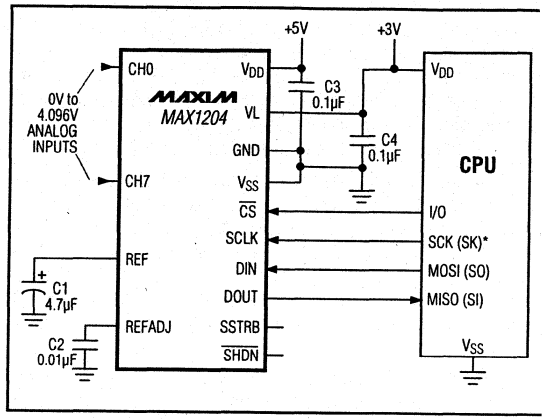
Low-Power, 8-Channel, Serial 10-Bit ADC with Adjustable Output Logic Level

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX1204AEPP	-40°C to +85°C	20 Plastic DIP	±1/2
MAX1204BEPP	-40°C to +85°C	20 Plastic DIP	±1
MAX1204AEAP	-40°C to +85°C	20 SSOP	±1/2
MAX1204BEAP	-40°C to +85°C	20 SSOP	±1
MAX1204BMJP	-55°C to +125°C	20 CERDIP*	±1

Contact factory for availability.

_Typical Operating Circuit



19-1155; Rev 0; 11/96

MAXIM

+2.7V, Low-Power, 12-Bit Serial ADC

General Description

The MAX1241 is a low-power, +2.7V to +5.25V, 12-bit analog-to-digital converter (ADC) available in an 8-pin package. It features a 7.5µs successive-approximation ADC, a fast track/hold (1.5µs), an on-chip clock, and a high-speed, 3-wire serial interface.

Power consumption is only 3mW (V_{DD} = 3V) at the 73ksps maximum sampling speed. A 1µA shutdown mode reduces power at slower throughput rates.

The MAX1241 accepts signals from 0V to V_{REF}, and the reference input range includes the positive supply rail. An external clock accesses data from the 3-wire interface, which connects directly to standard microcontroller I/O ports. The interface is compatible with SPI™, QSPI™, and Microwire™.

Excellent AC characteristics and very low power combined with ease of use and small package size make this converter ideal for remote-sensor and data-acquisition applications, or for other circuits with demanding power consumption and space requirements. The MAX1241 is available in 8-pin DIP and SO packages.

Applications

Battery-Powered Systems

Portable Data Logging

Isolated Data Acquisition

High-Accuracy Process Control

Instrumentation

Features

- **+2.7V to +5.25V Single Supply**
- **12-Bit Resolution**
- **Small Footprint: 8-Pin DIP and SO Packages**
- **Low Power: 3mW (73ksps)**
  66µW (1ksps)
  3µW (power-down mode)
- **Internal Track/Hold, 73ksps Sampling Rate**
- **SPI™/QSPI™/Microwire™ 3-Wire Serial Interface**

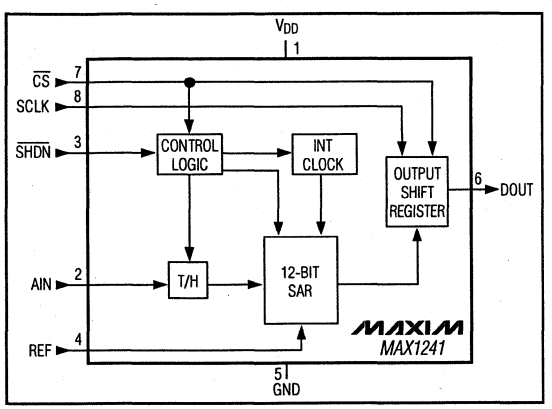
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX1241ACPA	0°C to +70°C	8 Plastic DIP	±1/2
MAX1241BCPA	0°C to +70°C	8 Plastic DIP	±1
MAX1241ACSA	0°C to +70°C	8 SO	±1/2
MAX1241BCSA	0°C to +70°C	8 SO	±1
MAX1241BC/D	0°C to +70°C	Dice*	±1
MAX1241AEPA	-40°C to +85°C	8 Plastic DIP	±1/2
MAX1241BEPA	-40°C to +85°C	8 Plastic DIP	±1
MAX1241AESA	-40°C to +85°C	8 SO	±1/2
MAX1241BESA	-40°C to +85°C	8 SO	±1
MAX1241AMJA	-55°C to +125°C	8 CERDIP**	±1/2
MAX1241BMJA	-55°C to +125°C	8 CERDIP**	±1

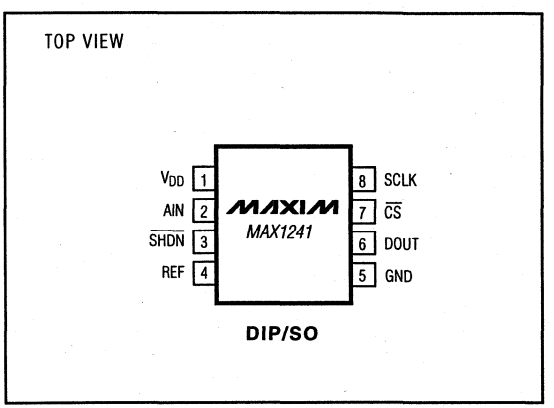
** Dice are specified at T_A = +25°C, DC parameters only.*

*** Contact factory for availability and processing to MIL-STD-883.*

Functional Diagram



Pin Configuration



SPI and QSPI are trademarks of Motorola, Inc. Microwire is a trademark of National Semiconductor Corp.

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+2.7V, Low-Power, 12-Bit Serial ADC

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6V
AIN to GND .....-0.3V to (V_{DD} + 0.3V)
REF to GND .....-0.3V to (V_{DD} + 0.3V)
Digital Inputs to GND.....-0.3V to +6V
DOUT to GND .....-0.3V to (V_{DD} + 0.3V)
DOUT Current .....±25mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C).....471mW
CERDIP (derate 8.00mW/°C above +70°C).....640mW

Operating Temperature Ranges
MAX1241_C_A.....0°C to +70°C
MAX1241_E_ A.....-40°C to +85°C
MAX1241_MJA .....-55°C to +125°C
Storage Temperature Range.....-60°C to +150°C
Lead Temperature (soldering, 10sec).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functiona operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure tc absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +5.25V; 73ksps, f_{SCLK} = 2.1MHz (50% duty cycle); V_{REF} = 2.500V applied to REF pin, 4.7µF capacitor at REF pin T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)						
Resolution			12			Bits
Relative Accuracy (Note 2)	INL	MAX1241A			±0.5	LSB
		MAX1241B			±1.0	
Differential Nonlinearity	DNL	No missing codes over temperature			±1	LSB
Offset Error		MAX1241A		±0.5	±3.0	LSB
		MAX1241B		±0.5	±4.0	
Gain Error (Note 3)				±0.5	±4.0	LSB
Gain Temperature Coefficient				±0.25		ppm/°C
DYNAMIC SPECIFICATIONS (10kHz sine-wave input, 0V to 2.500Vp-p, 73ksps, f_{SCLK} = 2.1MHz)						
Signal-to-Noise Plus Distortion Ratio	SINAD		70			dB
Total Harmonic Distortion	THD	Up to the 5th harmonic			-80	dB
Spurious-Free Dynamic Range	SFDR		80			dB
Small-Signal Bandwidth		- 3dB rolloff		2.25		MHz
Full-Power Bandwidth				1.0		MHz
CONVERSION RATE						
Conversion Time	t_{CONV}		5.5		7.5	µs
Track/Hold Acquisition Time	t_{ACQ}				1.5	µs
Throughput Rate		f_{SCLK} = 2.1MHz			73	ksps
Aperture Delay	t_{APR}	Figure 8		30		ns
Aperture Jitter				<50		ps
ANALOG INPUT						
Input Voltage Range			0		V_{REF}	V
Input Capacitance		(Note 4)		16		pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +5.25V; 73ksps, f_{SCLK} = 2.1MHz (50% duty cycle); V_{REF} = 2.500V applied to REF pin, 4.7µF capacitor at REF pin; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
EXTERNAL REFERENCE (V_{REF} = 2.500V)							
Input Voltage Range				1.00		V_{DD} + 50mV	V
Input Current					100	150	µA
Input Resistance				18	25		kΩ
REF Input Current in Shutdown		$\overline{SHDN}$ = 0V			±0.01	10	µA
Capacitive Bypass at REF				0.1			µF
DIGITAL INPUTS: SCLK, $\overline{CS}$, $\overline{SHDN}$							
SCLK, $\overline{CS}$ Input High Voltage	V_{INH}	$V_{DD} \le 3.6V$		2.0			V
		$V_{DD} > 3.6V$		3.0			
SCLK, $\overline{CS}$ Input Low Voltage	V_{INL}					0.8	V
SCLK, $\overline{CS}$ Input Hysteresis	V_{HYST}				0.2		V
SCLK, $\overline{CS}$ Input Leakage	I_{IN}	V_{IN} = 0V or V_{DD}			±0.01	±1	µA
SCLK, $\overline{CS}$ Input Capacitance	C_{IN}	(Note 4)				15	pF
$\overline{SHDN}$ Input High Voltage	V_{INH}			V_{DD} - 0.4			V
$\overline{SHDN}$ Input Low Voltage	V_{INL}					0.4	V
$\overline{SHDN}$ Input Current	I_{IN}	$\overline{SHDN}$ = 0V or V_{DD}				±4.0	µA
$\overline{SHDN}$ Input Mid Voltage	V_{IM}			1.1		V_{DD} - 1.1	V
$\overline{SHDN}$ Voltage, Floating	V_{FLT}	$\overline{SHDN}$ = open			$V_{DD}/2$		V
$\overline{SHDN}$ Max Allowed Leakage, Mid Input		$\overline{SHDN}$ = open				±100	nA
DIGITAL OUTPUT: DOUT							
Output Voltage Low	V_{OL}	I_{SINK} = 5mA				0.4	V
		I_{SINK} = 16mA				0.8	
Output Voltage High	V_{OH}	I_{SOURCE} = 0.5mA		V_{DD} - 0.5			V
Three-State Leakage Current	I_L	$\overline{CS}$ = V_{DD}			±0.01	±10	µA
Three-State Output Capacitance	C_{OUT}	$\overline{CS}$ = V_{DD} (Note 4)				15	pF
POWER REQUIREMENTS							
Supply Voltage	V_{DD}			2.7		5.25	V
Supply Current	I_{DD}	Operating mode	V_{DD} = 3.6V		0.9	1.5	mA
			V_{DD} = 5.25V		1.6	2.5	
		Power-down, digital inputs at 0V or V_{DD}	V_{DD} = 3.6V		1.2	10	µA
			V_{DD} = 5.25V		3.5	15	
Supply Rejection (Note 5)	PSR	V_{DD} = 2.7V to 5.25V, full-scale input			±0.3		mV

7

TIMING CHARACTERISTICS (Figure 8)

(V_{DD} = +2.7V to +5.25V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Acquisition Time	t_{ACQ}	$\overline{CS}$ = V_{DD} (Note 6)		1.5			µs
SCLK Fall to Output Data Valid	t_{DO}	Figure 1, C_{LOAD} = 50pF	MAX1241_C/E	20		200	ns
			MAX1241_M	20		240	
$\overline{CS}$ Fall to Output Enable	t_{DV}	Figure 1, C_{LOAD} = 50pF				240	ns
$\overline{CS}$ Rise to Output Disable	t_{TR}	Figure 2, C_{LOAD} = 50pF				240	ns
SCLK Clock Frequency	f_{SCLK}			0		2.1	MHz
SCLK Pulse Width High	t_{CH}			200			ns
SCLK Pulse Width Low	t_{CL}			200			ns
SCLK Low to $\overline{CS}$ Fall Setup Time	t_{CSO}			50			ns
DOUT Rise to SCLK Rise (Note 4)	t_{STR}			0			ns
$\overline{CS}$ Pulse Width	t_{CS}			240			ns

Note 1: Tested at V_{DD} = +2.7V.
Note 2: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range and offset have been calibrated.
Note 3: Offset nulled.
Note 4: Guaranteed by design. Not subject to production testing.
Note 5: Measured as [V_{FS}(2.7V) - V_{FS}(5.25V)].
Note 6: To guarantee acquisition time, t_{ACQ} is the maximum time the device takes to acquire the signal, and is also the minimum time needed for the signal to be acquired.

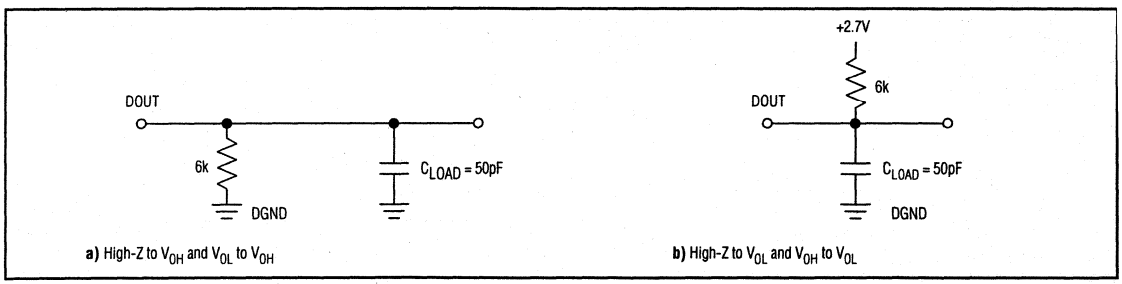


Figure 1. Load Circuits for DOUT Enable Time

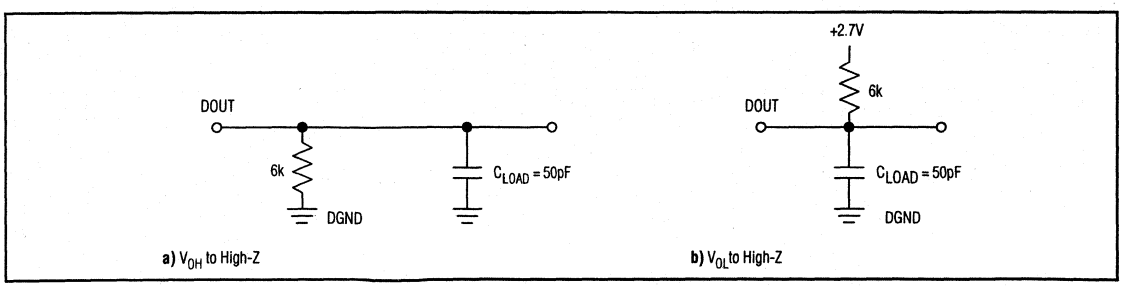
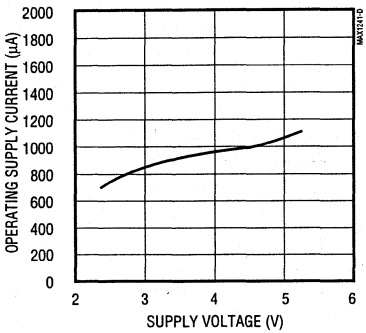


Figure 2. Load Circuits for DOUT Disable Time

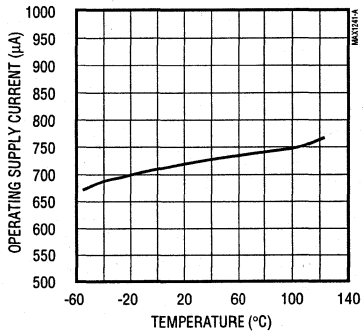
Typical Operating Characteristics

(V_{DD} = 3.0V, REF = 2.5V, f_{SCLK} = 2.1MHz, C_L = 20pF, T_A = +25°C, unless otherwise noted.)

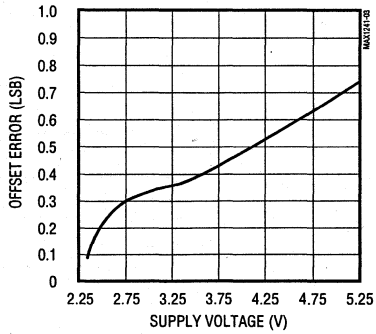
OPERATING SUPPLY CURRENT vs. SUPPLY VOLTAGE



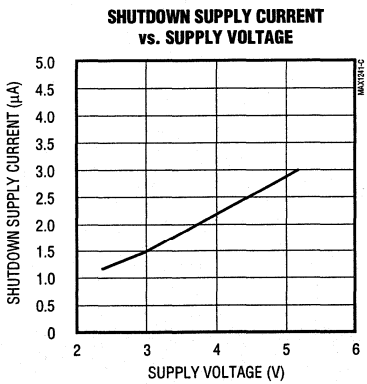
OPERATING SUPPLY CURRENT vs. TEMPERATURE



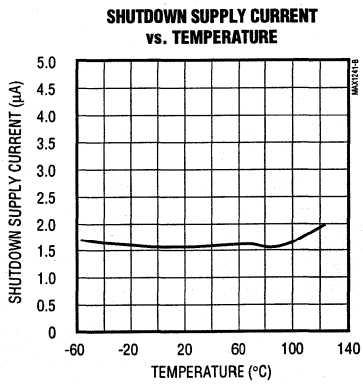
OFFSET ERROR vs. SUPPLY VOLTAGE



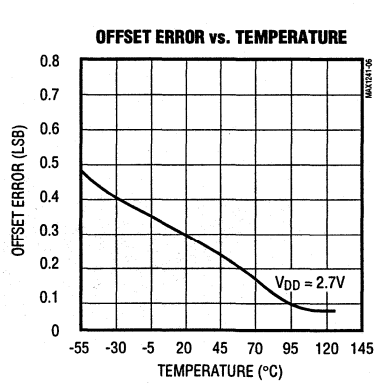
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



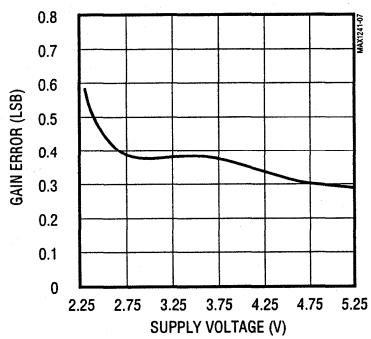
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



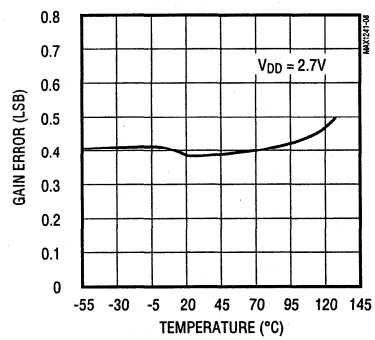
OFFSET ERROR vs. TEMPERATURE



GAIN ERROR vs. SUPPLY VOLTAGE



GAIN ERROR vs. TEMPERATURE



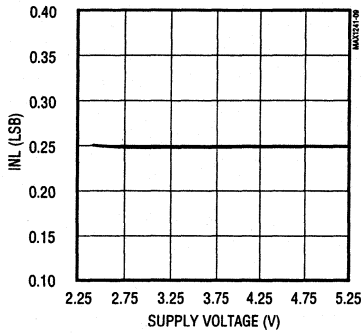
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+2.7V, Low-Power, 12-Bit Serial ADC

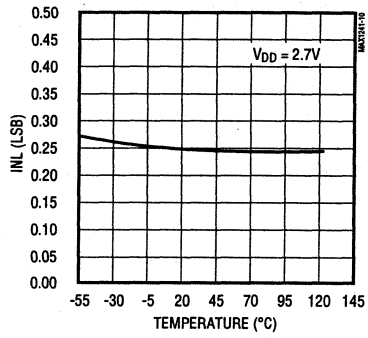
Typical Operating Characteristics

(V_{DD} = 3.0V, REF = 2.5V, f_{SCLK} = 2.1MHz, C_L = 20pF, T_A = +25°C, unless otherwise noted.)

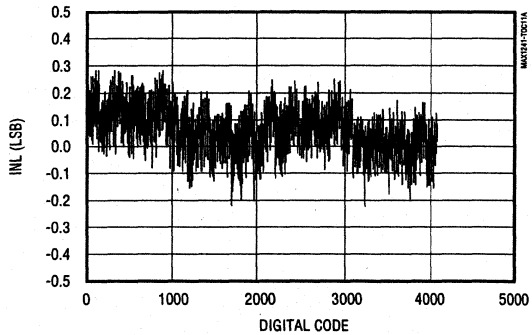
INTEGRAL NONLINEARITY vs. SUPPLY VOLTAGE



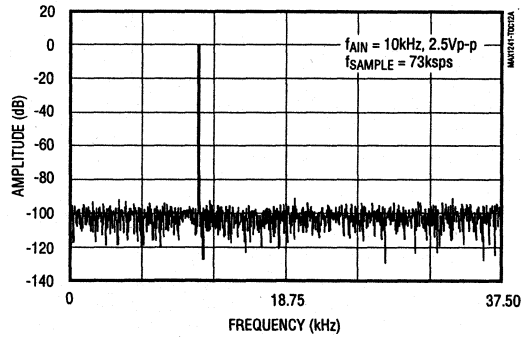
INTEGRAL NONLINEARITY vs. TEMPERATURE



INTEGRAL NONLINEARITY



FFT PLOT



Pin Description

PIN	NAME	FUNCTION
1	V_{DD}	Positive Supply Voltage
2	AIN	Sampling Analog Input, 0V to V_{REF} range
3	$\overline{SHDN}$	Three-Level Shutdown Input. Pulling $\overline{SHDN}$ low shuts the MAX1241 down. The device is fully operational when $\overline{SHDN}$ is floating or pulled high
4	REF	External Reference Voltage Input. Bypass REF with a minimum of 0.1µF.
5	GND	Analog and Digital Ground
6	DOUT	Serial Data Output. Data changes state at SCLK's falling edge. High impedance when $\overline{CS}$ is high.
7	$\overline{CS}$	Active-Low Chip Select initiates conversions on the falling edge. When $\overline{CS}$ is high, DOUT is high impedance.
8	SCLK	Serial Clock Input. SCLK clocks data out at rates up to 2.1MHz.

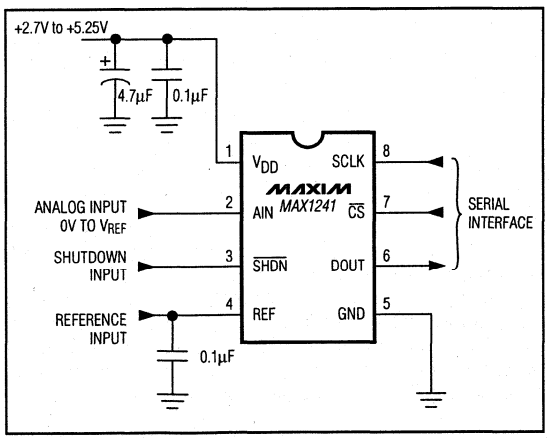


Figure 3. Operational Diagram

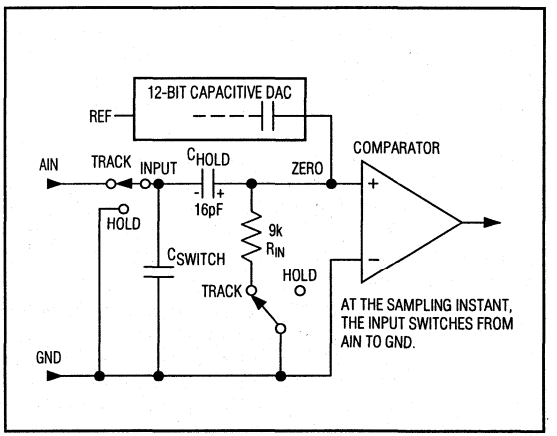


Figure 4. Equivalent Input Circuit

Detailed Description

Converter Operation

The MAX1241 uses input track/hold (T/H) and successive-approximation register (SAR) circuitry to convert an analog input signal to a digital 12-bit output. No external-hold capacitor is needed for the T/H. Figure 3 shows the MAX1241 in its simplest configuration. The MAX1241 converts input signals in the 0V to V_{REF} range in 9µs, including T/H acquisition time. It requires an external reference voltage from 1.0V to V_{DD}. The serial interface requires only three digital lines, SCLK, $\overline{CS}$, and DOUT, and provides an easy interface to microprocessors (µPs).

The MAX1241 has two modes: normal and shutdown. Pulling $\overline{SHDN}$ low shuts the device down and reduces supply current to below 10µA ($V_{DD} \leq 3.6V$), while pulling $\overline{SHDN}$ high or leaving it open puts the device into operational mode. Pulling $\overline{CS}$ low initiates a conversion. The conversion result is available at DOUT in unipolar serial format. The serial data stream consists of a high bit, signaling the end of conversion (EOC), followed by the data bits (MSB first).

Analog Input

Figure 4 illustrates the sampling architecture of the analog-to-digital converter's (ADC's) comparator. The full-scale input voltage is set by the voltage at REF.

+2.7V, Low-Power, 12-Bit Serial ADC

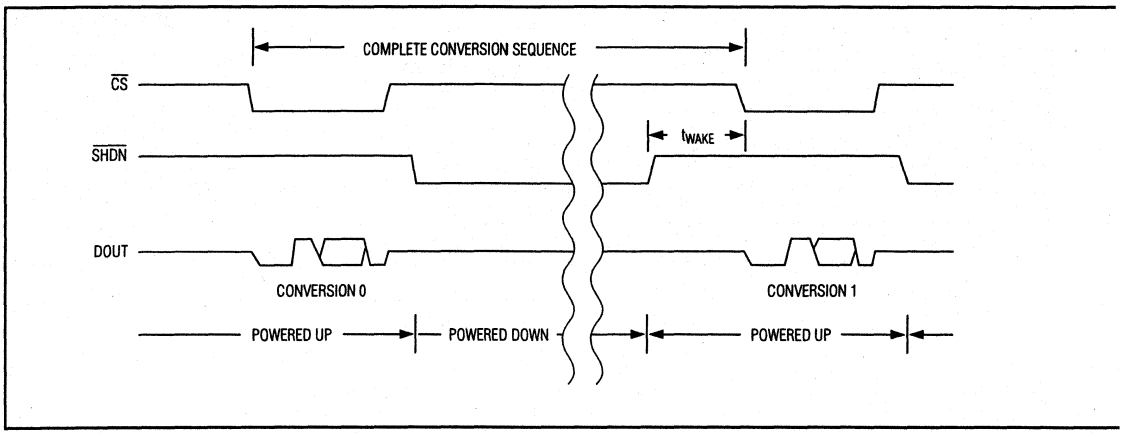


Figure 5. MAX1241 Shutdown Sequence

Track/Hold

In track mode, the analog signal is acquired and stored in the internal hold capacitor. In hold mode, the T/H switch opens and maintains a constant input to the ADC's SAR section.

During acquisition, the analog input AIN charges capacitor C_{HOLD}. Bringing $\overline{CS}$ low ends the acquisition interval. At this instant, the T/H switches the input side of C_{HOLD} to GND. The retained charge on C_{HOLD} represents a sample of the input, unbalancing node ZERO at the comparator's input.

In hold mode, the capacitive digital-to-analog converter (DAC) adjusts during the remainder of the conversion cycle to restore node ZERO to 0V within the limits of 12-bit resolution. This action is equivalent to transferring a charge from C_{HOLD} to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog input signal. At the conversion's end, the input side of C_{HOLD} switches back to AIN, and C_{HOLD} charges to the input signal again.

The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens and more time must be allowed between conversions. The acquisition time, t_{ACQ}, is the maximum time the device takes to acquire the signal, and is also the minimum time needed for the signal to be acquired. Acquisition time is calculated by:

$$t_{ACQ} = 9(R_S + R_{IN}) \times 16pF$$

where R_{IN} = 9kΩ, R_S = the input signal's source impedance, and t_{ACQ} is never less than 1.5µs. Source impedances below 1kΩ do not significantly affect the ADC's AC performance.

Higher source impedances can be used if a 0.01µF capacitor is connected to the analog input. Note that the input capacitor forms an RC filter with the input source impedance, limiting the ADC's signal input.

Input Bandwidth

The ADCs' input tracking circuitry has a 2.25MHz small-signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid aliasing of unwanted high-frequency signals into the frequency band of interest, anti-alias filtering is recommended.

Analog Input Protection

Internal protection diodes, which clamp the analog input to V_{DD} and GND, allow the input to swing from GND - 0.3V to V_{DD} + 0.3V without damage. However, for accurate conversions near full scale, the input must not exceed V_{DD} by more than 50mV, or be lower than GND by 50mV.

If the analog input exceeds 50mV beyond the supplies, limit the input current to 2mA, since larger currents degrade conversion accuracy.

External Reference

The MAX1241 operates with an external reference at the REF pin. Stay within the voltage range +1.0V to V_{DD} to achieve specified accuracy. The minimum input impedance is 18kΩ for DC currents. During conver-

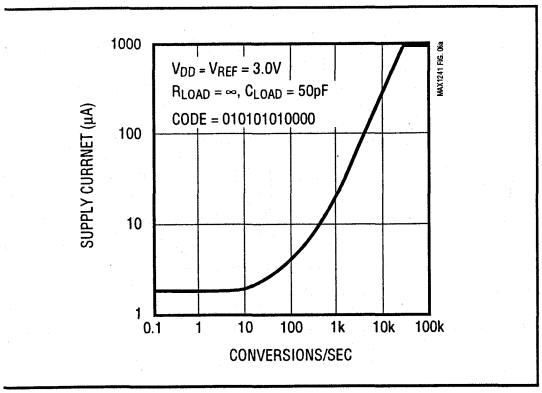


Figure 6. Average Supply Current vs. Conversion Rate

sion, the external reference must be able to deliver up to 250µA of DC load current and have an output impedance of 10Ω or less. The recommended minimum value for the bypass capacitor is 0.1µF. If the reference has higher output impedance or is noisy, bypass it close to the REF pin with a 4.7µF capacitor.

Serial Interface

Initialization After Power-Up and Starting a Conversion

When power is first applied, and if $\overline{SHDN}$ is not pulled low, internal power-on reset circuitry initializes the MAX1241. After the power supplies have been stabilized, the internal reset time is 10µs. No conversions should be performed during this phase. Additional time may be required to fully charge the reference bypass capacitor.

To start a conversion, pull $\overline{CS}$ low. At $\overline{CS}$'s falling edge, the T/H enters its hold mode and a conversion is initiated. After an internally timed conversion period, the end of conversion is signaled by DOUT pulling high. Data can then be shifted out serially with the external clock.

Using $\overline{SHDN}$ to Reduce Supply Current

Power consumption can be reduced significantly by shutting down the MAX1241 between conversions. This is shown in Figure 6, a plot of average supply current vs. conversion rate. The wake-up time, t_{WAKE}, is the time from $\overline{SHDN}$ deasserted to the time when a conversion may be initiated (Figure 5). The MAX1241's wake-up time is largely dependent on the external reference's power-up time. If the external reference is not shut down, the wake-up time is approximately 4µs.

External Clock

The actual conversion does not require the external clock. This allows the conversion result to be read back at the µP's convenience at any clock rate from 0MHz to 2.1MHz. The clock duty cycle is unrestricted if each clock phase is at least 200ns. Do not run the clock while a conversion is in progress.

Timing and Control

Conversion-start and data-read operations are controlled by the $\overline{CS}$ and SCLK digital inputs. The timing diagrams of Figures 7 and 8 outline serial-interface operation.

A $\overline{CS}$ falling edge initiates a conversion sequence: the T/H stage holds the input voltage, the ADC begins to convert, and DOUT changes from high impedance to logic low. SCLK must be kept low during the conversion. An internal register stores the data when the conversion is in progress.

End of conversion (EOC) is signaled by DOUT going high. DOUT's rising edge can be used as a framing signal. SCLK shifts the data out of this register any time after the conversion is complete. DOUT transitions on SCLK's falling edge. The next falling clock edge produces the MSB of the conversion at DOUT, followed by the remaining bits. Since there are 12 data bits and one leading high bit, at least 13 falling clock edges are needed to shift out these bits. Extra clock pulses occurring after the conversion result has been clocked out, and prior to a rising edge of $\overline{CS}$, produce trailing zeros at DOUT and have no effect on converter operation.

Minimum cycle time is accomplished by using DOUT's rising edge as the EOC signal. Clock out the data with 12.5 clock cycles at full speed. Pull $\overline{CS}$ high after reading the conversion's LSB. After the specified minimum time, t_{CS}, $\overline{CS}$ can be pulled low again to initiate the next conversion.

Output Coding and Transfer Function

The data output from the MAX1241 is binary, and Figure 9 depicts the nominal transfer function. Code transitions occur halfway between successive-integer LSB values. If V_{REF} = +2.500V, then 1 LSB = 610µV or 2.500V/4096.

Applications Information

Connection to Standard Interfaces

The MAX1241 serial interface is fully compatible with SPI, QSPI, and Microwire standard serial interfaces (Figure 10).

If a serial interface is available, set the CPU's serial interface in master mode so the CPU generates the serial clock. Choose a clock frequency up to 2.1MHz.

+2.7V, Low-Power, 12-Bit Serial ADC

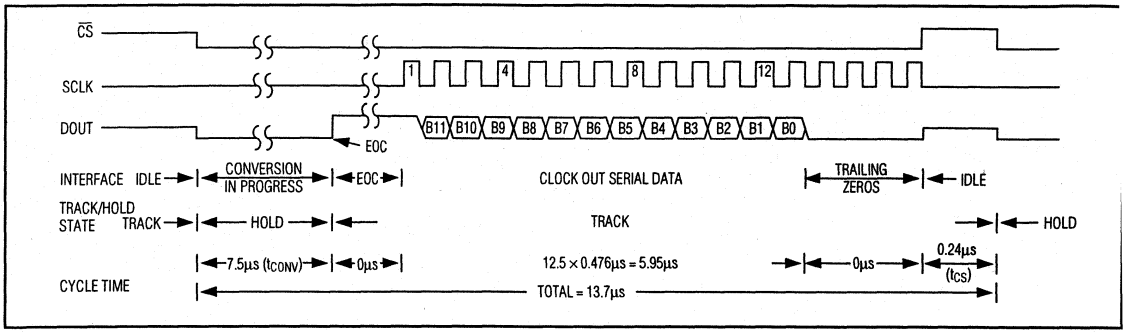


Figure 7. Interface Timing Sequence

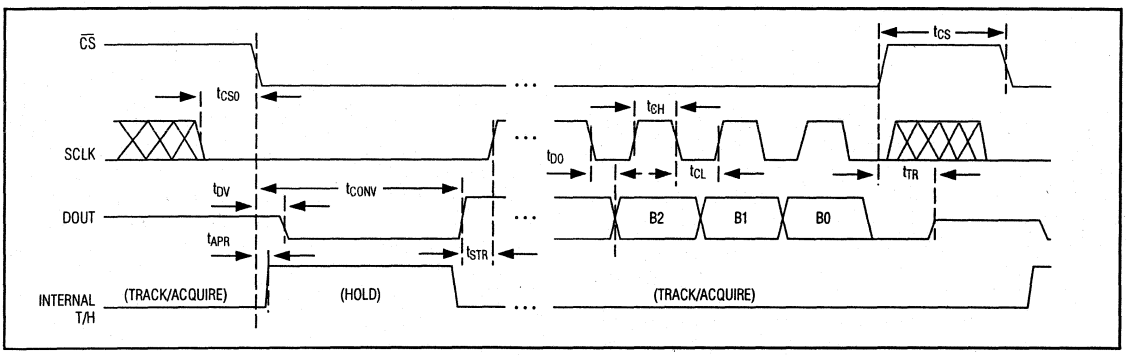


Figure 8. Detailed Serial-Interface Timing

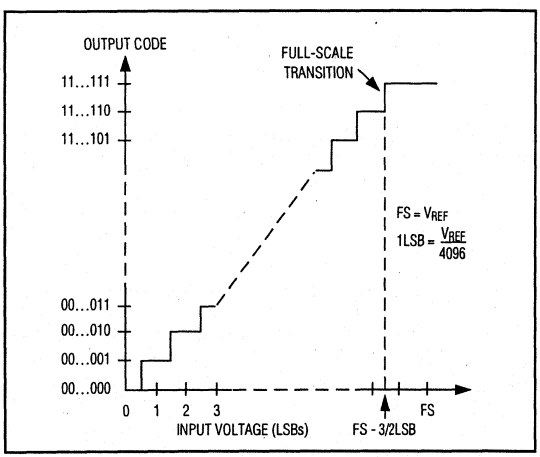


Figure 9. Unipolar Transfer Function, Full Scale (FS) = V_{REF}, Zero Scale (ZS) = GND

1) Use a general-purpose I/O line on the CPU to pull $\overline{CS}$ low. Keep SCLK low.
2) Wait the for the maximum conversion time specified before activating SCLK. Alternatively, look for a DOUT rising edge to determine the end of conversion.
3) Activate SCLK for a minimum of 13 clock cycles. The first falling clock edge will produce the MSB of the DOUT conversion. DOUT output data transitions on SCLK's falling edge and is available in MSB-first format. Observe the SCLK to DOUT valid timing characteristic. Data can be clocked into the µP on SCLK's rising edge.
4) Pull $\overline{CS}$ high at or after the 13th falling clock edge. If $\overline{CS}$ remains low, trailing zeros are clocked out after the LSB.
5) With $\overline{CS}$ = high, wait the minimum specified time, t_{CS}, before initiating a new conversion by pulling $\overline{CS}$ low. If a conversion is aborted by pulling $\overline{CS}$ high before the conversion's end, wait for the minimum acquisition time, t_{ACQ}, before starting a new conversion.

Data can be output in two bytes or continuously, as shown in Figure 7. The bytes will contain the result of the conversion padded with one leading 1, and trailing 0s if SCLK is still active with $\overline{CS}$ kept low.

SPI and Microwire

When using SPI or QSPI, set CPOL = 0 and CPHA = 0. Conversion begins with a $\overline{CS}$ falling edge. DOUT goes low, indicating a conversion in progress. Wait until DOUT goes high or until the maximum specified 7.5µs conversion time elapses. Two consecutive 1-byte reads are required to get the full 12 bits from the ADC. DOUT output data transitions on SCLK's falling edge and is clocked into the µP on SCLK's rising edge.

The first byte contains a leading 1, and seven bits of conversion result. The second byte contains the remaining five bits and three trailing zeros. See Figure 10 for connections and Figure 11 for timing.

QSPI

Set CPOL = CPHA = 0. Unlike SPI, which requires two 1-byte reads to acquire the 12 bits of data from the ADC, QSPI allows the minimum number of clock cycles necessary to clock in the data. The MAX1241 requires 13 clock cycles from the µP to clock out the 12 bits of data with no trailing zeros (Figure 12). The maximum clock frequency to ensure compatibility with QSPI is 2.097MHz.

Layout, Grounding, and Bypassing

For best performance, use printed circuit boards. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

Figure 13 shows the recommended system ground connections. Establish a single-point analog ground ("star" ground point) at GND, separate from the logic ground. Connect all other analog grounds and DGND to this star ground point for further noise reduction. No other digital system ground should be connected to this single-point analog ground. The ground return to the power supply for this ground should be low impedance and as short as possible for noise-free operation.

High-frequency noise in the V_{DD} power supply may affect the ADC's high-speed comparator. Bypass this supply to the single-point analog ground with 0.1µF and 4.7µF bypass capacitors. Minimize capacitor lead lengths for best supply-noise rejection. If the +3V power supply is very noisy, a 10Ω resistor can be connected as a low-pass filter to attenuate supply noise (Figure 13).

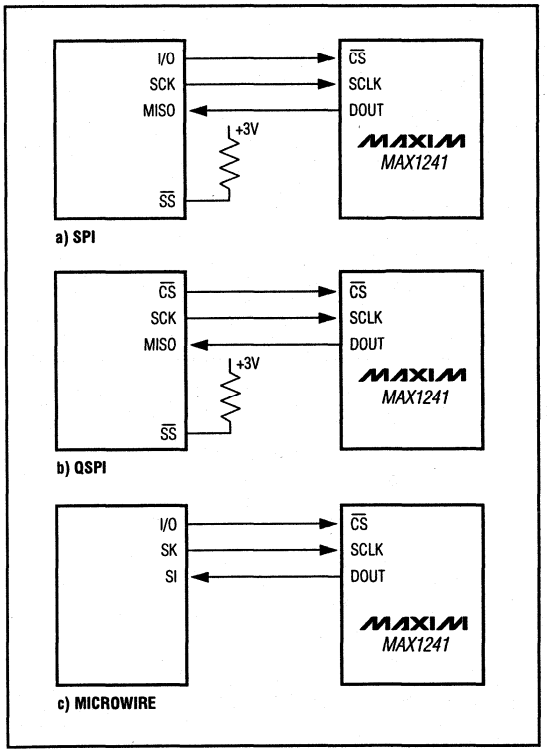


Figure 10. Common Serial-Interface Connections to the MAX1241

+2.7V, Low-Power, 12-Bit Serial ADC

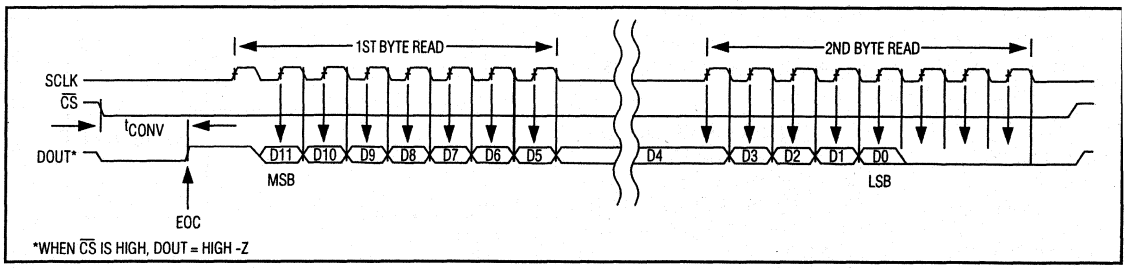


Figure 11. SPI/Microwire Serial Interface Timing (CPOL = CPHA = 0)

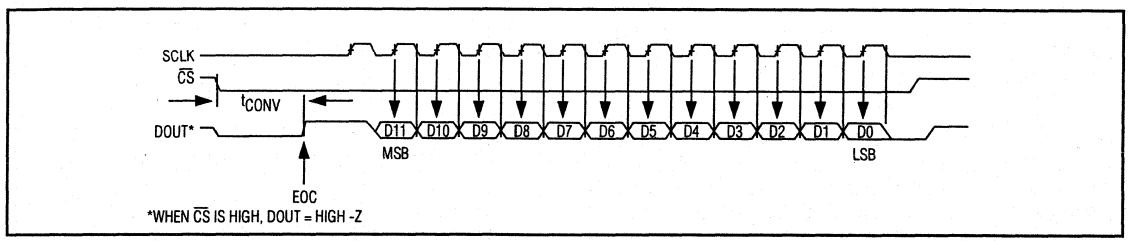


Figure 12. QSPI Serial Interface Timing (CPOL = CPHA = 0)

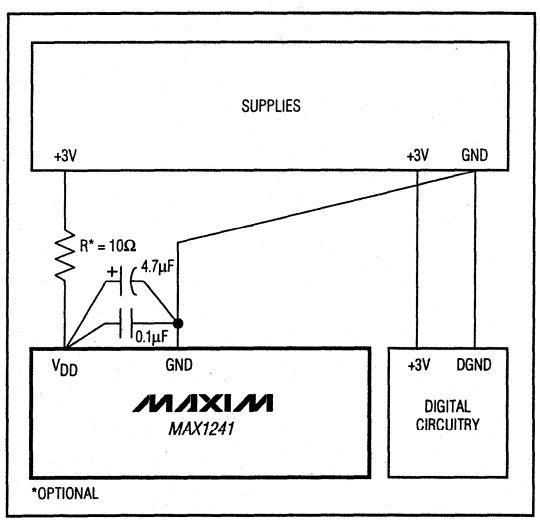


Figure 13. Power-Supply Grounding Condition

Chip Information

TRANSISTOR COUNT: 2554
SUBSTRATE CONNECTED TO GND

19-1156; Rev 0; 11/96

+2.7V, Low-Power, 10-Bit Serial ADC

General Description

The MAX1243 is a low-power, +2.7V to +5.25V, 10-bit analog-to-digital converter (ADC) available in an 8-pin package. It features a 7.5µs successive-approximation ADC, a fast track/hold (1.5µs), an on-chip clock, and a high-speed, 3-wire serial interface.

Power consumption is only 3mW (V_{DD} = 3V) at the 73ksps maximum sampling speed. A 1µA shutdown mode reduces power at slower throughput rates.

The MAX1243 accepts signals from 0V to V_{REF}, and the reference input range includes the positive supply rail. An external clock accesses data from the 3-wire interface, which connects directly to standard microcontroller I/O ports. The interface is compatible with SPI™, QSPI™, and Microwire™.

Excellent AC characteristics and very low power combined with ease of use and small package size make this converter ideal for remote-sensor and data-acquisition applications, or for other circuits with demanding power consumption and space requirements. The MAX1243 is available in 8-pin DIP and SO packages.

Applications

Portable Data Logging
Test Equipment
Isolated Data Acquisition
Process Control Monitoring
Temperature Measurement

Features

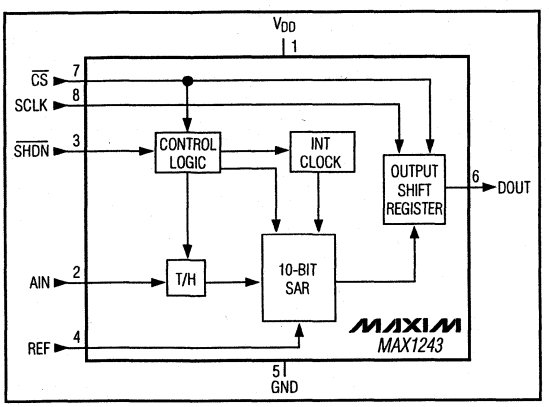
- **+2.7V to +5.25V Single Supply**
- **10-Bit Resolution**
- **Small Footprint: 8-Pin DIP and SO Packages**
- **Low Power: 3mW (73ksps)**
  66µW (1ksps)
  3µW (power-down mode)
- **Internal Track/Hold, 73ksps Sampling Rate**
- **SPI™/QSPI™/Microwire™ 3-Wire Serial Interface**
- **Pin-Compatible 12-Bit Upgrade: MAX1241**

Ordering Information

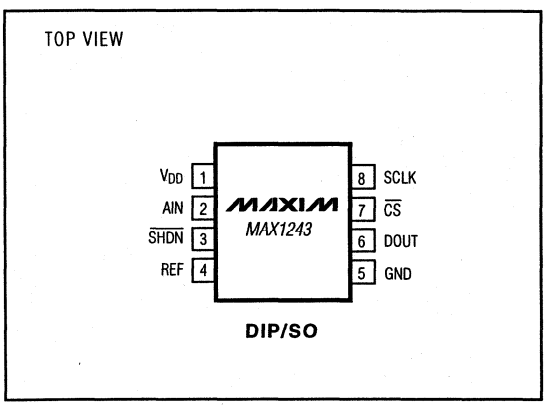
PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX1243ACPA	0°C to +70°C	8 Plastic DIP	±1/2
MAX1243BCPA	0°C to +70°C	8 Plastic DIP	±1
MAX1243ACSA	0°C to +70°C	8 SO	±1/2
MAX1243BCSA	0°C to +70°C	8 SO	±1
MAX1243AEPA	-40°C to +85°C	8 Plastic DIP	±1/2
MAX1243BEPA	-40°C to +85°C	8 Plastic DIP	±1
MAX1243AESA	-40°C to +85°C	8 SO	±1/2
MAX1243BESA	-40°C to +85°C	8 SO	±1
MAX1243AMJA	-55°C to +125°C	8 CERDIP*	±1/2
MAX1243BMJA	-55°C to +125°C	8 CERDIP*	±1

*Contact factory for availability and processing to MIL-STD-883.

Functional Diagram



Pin Configuration



7

SPI and QSPI are trademarks of Motorola, Inc. Microwire is a trademark of National Semiconductor Corp.

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

+2.7V, Low-Power, 10-Bit Serial ADC

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6V
AIN to GND .....-0.3V to (V_{DD} + 0.3V)
REF to GND .....-0.3V to (V_{DD} + 0.3V)
Digital Inputs to GND .....-0.3V to +6V
DOUT to GND .....-0.3V to (V_{DD} + 0.3V)
DOUT Current .....±25mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C) 471mW
CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges
MAX1243_C_A .....0°C to +70°C
MAX1243_E_A .....-40°C to +85°C
MAX1243_MJA .....-55°C to +125°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functiona operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure t absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +5.25V, 73ksps, f_{SCLK} = 2.1MHz (50% duty cycle), V_{REF} = 2.500V applied to REF pin, 4.7µF capacitor at REF pin T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)						
Resolution			10			Bits
Relative Accuracy (Note 2)		MAX1243A		0.15	±0.5	LSB
		MAX1243B			±1.0	
Differential Nonlinearity	DNL	No missing codes over temperature			±1	LSB
Offset Error		MAX1243A		0.15	±1	LSB
		MAX1243B			±2	
Gain Error (Note 3)		MAX1243A			±1	LSB
		MAX1243B			±2	
Gain Temperature Coefficient				±0.25		ppm/°C
DYNAMIC SPECIFICATIONS (10kHz sine-wave input, 0V to 2.500Vp-p, 73ksps, f_{SCLK} = 2.1MHz)						
Signal-to-Noise Plus Distortion Ratio	SINAD			66		dB
Total Harmonic Distortion	THD	Up to the 5th harmonic		-70		dB
Spurious-Free Dynamic Range	SFDR			70		dB
Small-Signal Bandwidth		- 3dB rolloff		2.25		MHz
Full-Power Bandwidth				1.0		MHz
CONVERSION RATE						
Conversion Time	t_{CONV}		5.5		7.5	µs
Track/Hold Acquisition Time	t_{ACQ}				1.5	µs
Throughput Rate		f_{SCLK} = 2.1MHz			73	ksps
Aperture Delay	t_{APR}	Figure 8		30		ns
Aperture Jitter				<50		ps
ANALOG INPUT						
Input Voltage Range			0		V_{REF}	V
Input Capacitance		(Note 4)		16		pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +5.25V, 73ksps, f_{SCLK} = 2.1MHz (50% duty cycle), V_{REF} = 2.500V applied to REF pin, 4.7µF capacitor at REF pin, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
EXTERNAL REFERENCE (V_{REF} = 2.500V)							
Input Voltage Range				1.00		V_{DD} + 50mV	V
Input Current					100	150	µA
Input Resistance				18	25		kΩ
REF Input Current in Shutdown		$\overline{SHDN}$ = 0V			±0.01	10	µA
Capacitive Bypass at REF				0.1			µF
DIGITAL INPUTS: SCLK, $\overline{CS}$, $\overline{SHDN}$							
SCLK, $\overline{CS}$ Input High Voltage	V_{INH}	V_{DD} ≤ 3.6V		2.0			V
		V_{DD} > 3.6V		3.0			
SCLK, $\overline{CS}$ Input Low Voltage	V_{INL}					0.8	V
SCLK, $\overline{CS}$ Input Hysteresis	V_{HYST}				0.2		V
SCLK, $\overline{CS}$ Input Leakage	I_{IN}	V_{IN} = 0V or V_{DD}			±0.01	±1	µA
SCLK, $\overline{CS}$ Input Capacitance	C_{IN}	(Note 4)				15	pF
$\overline{SHDN}$ Input High Voltage	V_{INH}			V_{DD} - 0.4			V
$\overline{SHDN}$ Input Low Voltage	V_{INL}					0.4	V
$\overline{SHDN}$ Input Current	I_{IN}	$\overline{SHDN}$ = 0V or V_{DD}				±4.0	µA
$\overline{SHDN}$ Input Mid Voltage	V_{IM}			1.1		V_{DD} - 1.1	V
$\overline{SHDN}$ Voltage, Floating	V_{FLT}	$\overline{SHDN}$ = open			V_{DD}/2		V
$\overline{SHDN}$ Max Allowed Leakage, Mid Input		$\overline{SHDN}$ = open				±100	nA
DIGITAL OUTPUT: DOUT							
Output Voltage Low	V_{OL}	I_{SINK} = 5mA				0.4	V
		I_{SINK} = 16mA				0.8	
Output Voltage High	V_{OH}	I_{SOURCE} = 0.5mA		V_{DD} - 0.5			V
Three-State Leakage Current	I_L	$\overline{CS}$ = V_{DD}			±0.01	±10	µA
Three-State Output Capacitance	C_{OUT}	$\overline{CS}$ = V_{DD} (Note 4)				15	pF
POWER REQUIREMENTS							
Supply Voltage	V_{DD}			2.7		5.25	V
Supply Current	I_{DD}	Operating mode	V_{DD} = 3.6V		0.9	1.5	mA
			V_{DD} = 5.25V		1.6	2.5	
		Power-down	V_{DD} = 3.6V		1.2	10	µA
			V_{DD} = 5.25V		3.5	15	
Supply Rejection (Note 5)	PSR	V_{DD} = 2.7V to 5.25V, full-scale input			±0.3		mV

7

+2.7V, Low-Power, 10-Bit Serial ADC

TIMING CHARACTERISTICS (Figure 8)

(V_{DD} = +2.7V to +5.25V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Acquisition Time	t_{ACQ}	$\overline{CS}$ = V_{DD} (Note 6)		1.5			µs
SCLK Fall to Output Data Valid	t_{DO}	Figure 1, C_{LOAD} = 50pF	MAX1243_C/E	20		200	ns
			MAX1243_M	20		240	
$\overline{CS}$ Fall to Output Enable	t_{DV}	Figure 1, C_{LOAD} = 50pF				240	ns
$\overline{CS}$ Rise to Output Disable	t_{TR}	Figure 2, C_{LOAD} = 50pF				240	ns
SCLK Clock Frequency	f_{SCLK}			0		2.1	MHz
SCLK Pulse Width High	t_{CH}			200			ns
SCLK Pulse Width Low	t_{CL}			200			ns
SCLK Low to $\overline{CS}$ Fall Setup Time	t_{CS0}			50			ns
DOUT Rise to SCLK Rise (Note 4)	t_{STR}			0			ns
$\overline{CS}$ Pulse Width	t_{CS}			240			ns

Note 1: Tested at V_{DD} = +2.7V.

Note 2: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range and offset have been calibrated.

Note 3: Offset nulled.

Note 4: Guaranteed by design. Not subject to production testing.

Note 5: Measured as [V_{FS}(2.7V) - V_{FS}(5.25V)].

Note 6: To guarantee acquisition time, t_{ACQ} is the maximum time the device takes to acquire the signal, and is also the minimum time needed for the signal to be acquired.

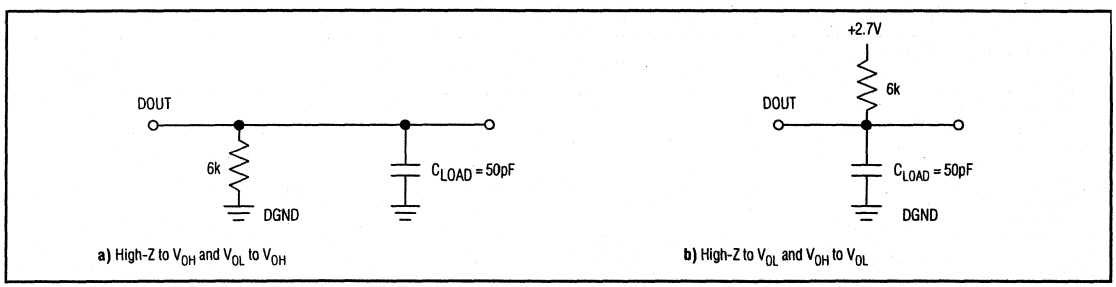


Figure 1. Load Circuits for DOUT Enable Time

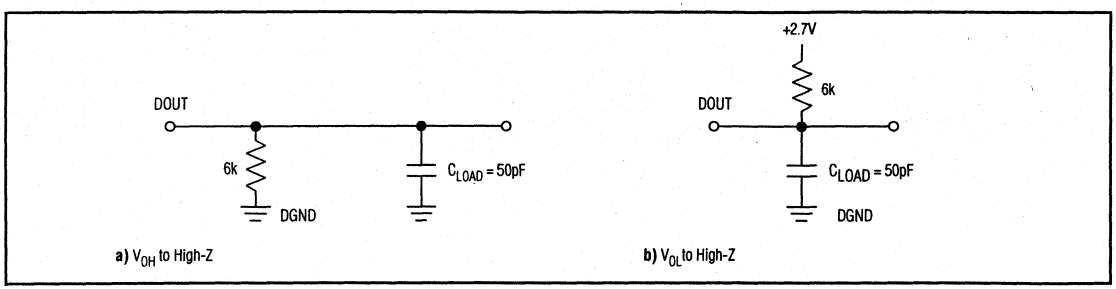
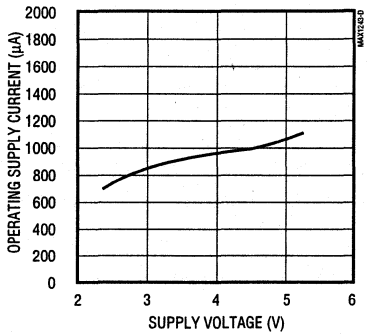


Figure 2. Load Circuits for DOUT Disable Time

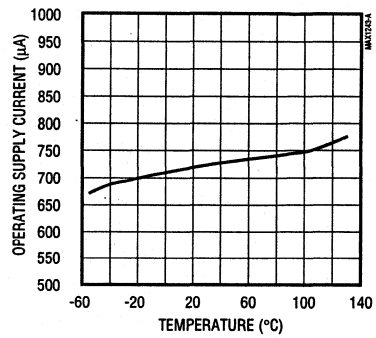
Typical Operating Characteristics

(V_{DD} = 3.0V, REF = 2.5V, f_{SCLK} = 2.1MHz, C_L = 20pF, T_A = +25°C, unless otherwise noted.)

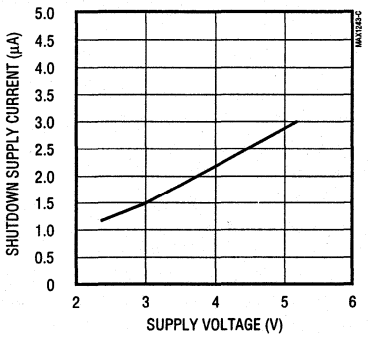
OPERATING SUPPLY CURRENT vs. SUPPLY VOLTAGE



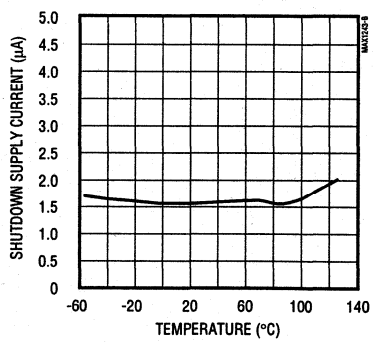
OPERATING SUPPLY CURRENT vs. TEMPERATURE



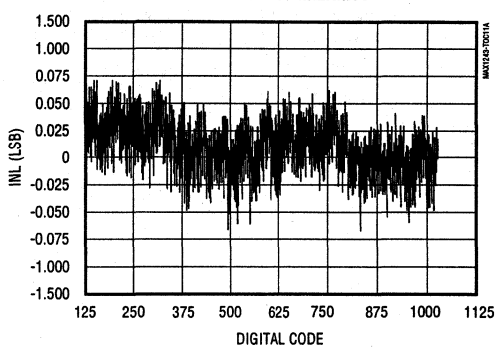
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



INTEGRAL NONLINEARITY



+2.7V, Low-Power, 10-Bit Serial ADC

Pin Description

PIN	NAME	FUNCTION
1	V_{DD}	Positive Supply Voltage
2	AIN	Sampling Analog Input, 0V to V_{REF} range
3	$\overline{SHDN}$	Three-Level Shutdown Input. Pulling $\overline{SHDN}$ low shuts the MAX1243 down. The device is fully operational when $\overline{SHDN}$ is floating or pulled high
4	REF	External Reference Voltage Input. Bypass REF with a minimum of 0.1µF.
5	GND	Analog and Digital Ground
6	DOUT	Serial Data Output. Data changes state at SCLK's falling edge. High impedance when $\overline{CS}$ is high.
7	$\overline{CS}$	Active-Low Chip Select initiates conversions on the falling edge. When $\overline{CS}$ is high, DOUT is high impedance.
8	SCLK	Serial Clock Input. SCLK clocks data out at rates up to 2.1MHz.

Detailed Description

Converter Operation

The MAX1243 uses input track/hold (T/H) and successive-approximation register (SAR) circuitry to convert an analog input signal to a digital 10-bit output. No external-hold capacitor is needed for the T/H. Figure 3 shows the MAX1243 in its simplest configuration. The MAX1243 converts input signals in the 0V to V_{REF} range in 9µs, including T/H acquisition time. It requires an external reference voltage from 1.0V to V_{DD}. The serial interface requires only three digital lines, SCLK, $\overline{CS}$, and DOUT, and provides an easy interface to microprocessors (µPs).

The MAX1243 has two modes: normal and shutdown. Pulling $\overline{SHDN}$ low shuts the device down and reduces supply current to below 10µA ($V_{DD} \leq 3.6V$), while pulling $\overline{SHDN}$ high or leaving it open puts the device into operational mode. A conversion is initiated by pulling $\overline{CS}$ low. The conversion result is available at DOUT in unipolar serial format. The serial data stream consists of a high bit, signaling the end of conversion (EOC), followed by the data bits (MSB first).

Analog Input

Figure 4 illustrates the sampling architecture of the analog-to-digital converter's (ADC's) comparator. The full-scale input voltage is set by the voltage at REF.

Track/Hold

In track mode, the analog signal is acquired and stored in the internal hold capacitor. In hold mode, the T/H switch opens and maintains a constant input to the ADC's SAR section.

During acquisition, the analog input AIN charges capacitor C_{HOLD}. Bringing $\overline{CS}$ low ends the acquisition interval. At this instant, the T/H switches the input side of C_{HOLD} to GND. The retained charge on C_{HOLD} represents a sample of the input, unbalancing node ZERO at the comparator's input.

In hold mode, the capacitive digital-to-analog converter (DAC) adjusts during the remainder of the conversion cycle to restore node ZERO to 0V within the limits of 10-bit resolution. This action is equivalent to transferring a charge from C_{HOLD} to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog input signal. At the conversion's end, the input side of C_{HOLD} switches back to AIN, and C_{HOLD} charges to the input signal again.

The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens and more time must be allowed between conversions. The acquisition time, t_{ACQ}, is the maximum time the device takes to acquire the signal, and is also the minimum time needed for the signal to be acquired. Acquisition time is calculated by:

$$t_{ACQ} = 7(R_S + R_{IN}) \times 16pF$$

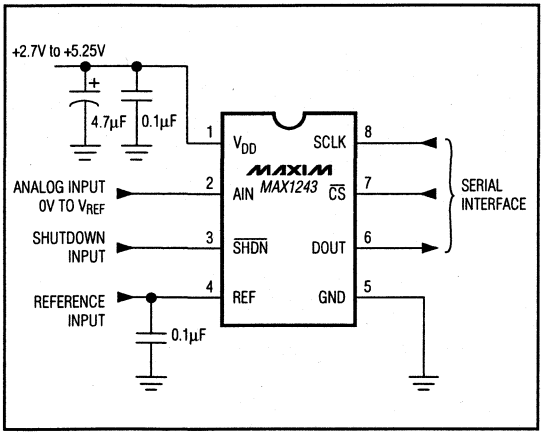


Figure 3. Operational Diagram

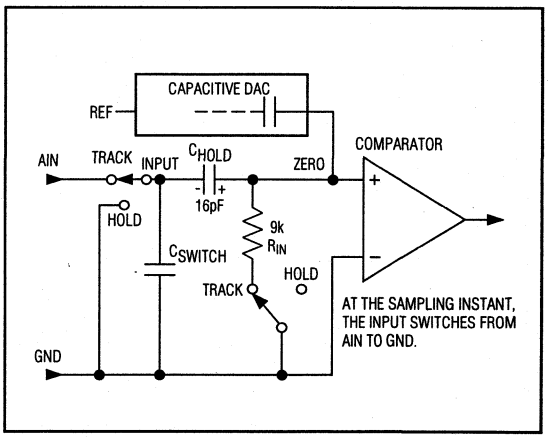


Figure 4. Equivalent Input Circuit

where R_{IN} = 9kΩ, R_S = the input signal's source impedance, and t_{ACQ} is never less than 1.5µs. Source impedances below 4kΩ do not significantly affect the ADC's AC performance.

Higher source impedances can be used if a 0.01µF capacitor is connected to the analog input. Note that the input capacitor forms an RC filter with the input source impedance, limiting the ADC's signal input.

Input Bandwidth

The ADCs' input tracking circuitry has a 2.25MHz small-signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid aliasing of unwanted high-frequency signals into the frequency band of interest, anti-alias filtering is recommended.

Analog Input Protection

Internal protection diodes, which clamp the analog input to V_{DD} and GND, allow the input to swing from GND - 0.3V to V_{DD} + 0.3V without damage. However, for accurate conversions near full scale, the input must not exceed V_{DD} by more than 50mV, or be lower than GND by 50mV.

If the analog input exceeds 50mV beyond the supplies, limit the input current to 2mA, since larger currents degrade conversion accuracy.

External Reference

The MAX1243 operates with an external reference at the REF pin. Stay within the voltage range 1.0V to V_{DD} to achieve specified accuracy. The minimum input impedance is 18kΩ for DC currents. During conversion, the external reference must be able to deliver up to 250µA of DC load current and have an output impedance of 10Ω or less. The recommended minimum value for the bypass capacitor is 0.1µF. If the reference has higher output impedance or is noisy, bypass it close to the REF pin with a 4.7µF capacitor.

Serial Interface

Initialization After Power-Up and Starting a Conversion

When power is first applied, and if $\overline{SHDN}$ is not pulled low, internal power-on reset circuitry initializes the MAX1243. After the power supplies have been stabilized, the internal reset time is 10µs. No conversions should be performed during this phase. Additional time may be required to fully charge the reference bypass capacitor.

To start a conversion, pull $\overline{CS}$ low. At $\overline{CS}$'s falling edge, the T/H enters its hold mode and a conversion is initiated. After an internally timed conversion period, the end of conversion is signaled by DOUT pulling high. Data can then be shifted out serially with the external clock.

+2.7V, Low-Power, 10-Bit Serial ADC

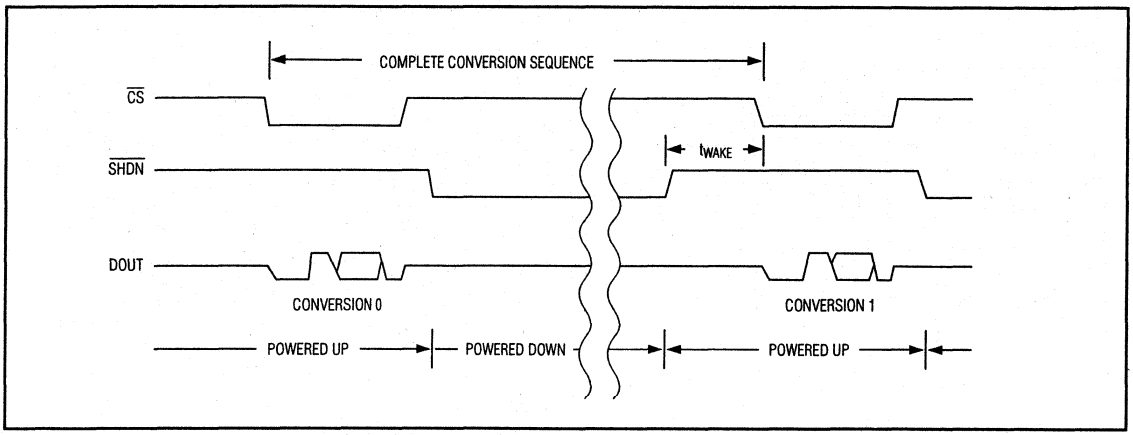


Figure 5. MAX1243 Shutdown Sequence

Using SHDN to Reduce Supply Current

Power consumption can be reduced significantly by shutting down the MAX1243 between conversions. This is shown in Figure 6, a plot of average supply current vs. conversion rate. The wake-up time, tWAKE, is the time from SHDN deasserted to the time when a conversion may be initiated (Figure 5). The MAX1243's wake-up time is largely dependent on the external reference's power-up time. If the external reference is not shut down, the wake-up time is approximately 4µs.

External Clock

The actual conversion does not require the external clock. This allows the conversion result to be read back at the µP's convenience at any clock rate from 0MHz to 2.1MHz. The clock duty cycle is unrestricted if each clock phase is at least 200ns. Do not run the clock while a conversion is in progress.

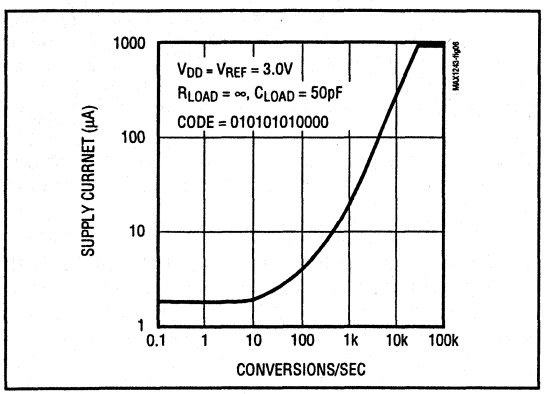


Figure 6. Average Supply Current vs. Conversion Rate

Timing and Control

Conversion-start and data-read operations are controlled by the CS and SCLK digital inputs. The timing diagrams of Figures 7 and 8 outline serial-interface operation.

A CS falling edge initiates a conversion sequence: the T/H stage holds the input voltage, the ADC begins to convert, and DOUT changes from high impedance to logic low. SCLK must be kept low during the conversion. An internal register stores the data when the conversion is in progress.

End of conversion (EOC) is signaled by DOUT going high. DOUT's rising edge can be used as a framing signal. SCLK shifts the data out of this register any time after the conversion is complete. DOUT transitions on SCLK's falling edge. The next falling clock edge produces the MSB of the conversion at DOUT, followed by the remaining bits. Since there are 10 data bits, two sub-bits, and one leading high bit, at least 13 falling clock edges are needed to shift out these bits. Extra clock pulses occurring after the conversion result has been clocked out, and prior to a rising edge of CS, produce trailing zeros at DOUT and have no effect on converter operation.

Minimum cycle time is accomplished by using DOUT's rising edge as the EOC signal. Clock out the data with 10.5 clock cycles at full speed (Figure7b). Pull CS high after reading the conversion's LSB. After the specified minimum time, tCS, CS can be pulled low again to initiate the next conversion.

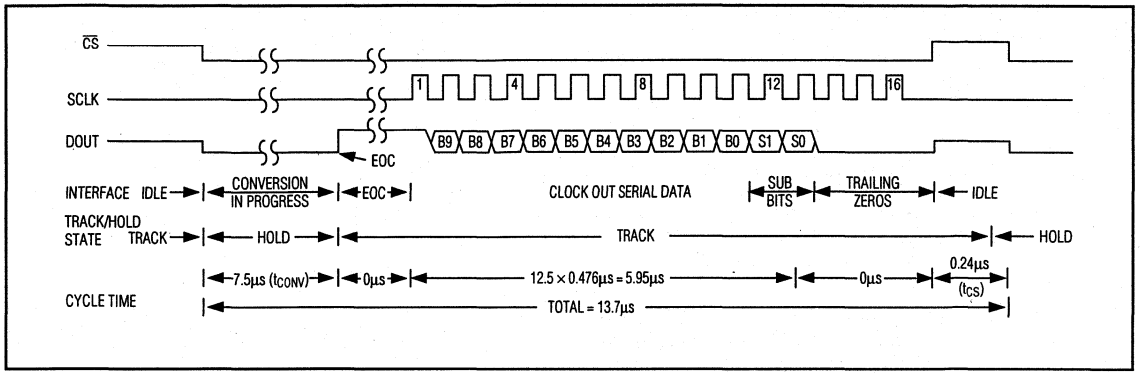


Figure 7a. Interface Timing Sequence

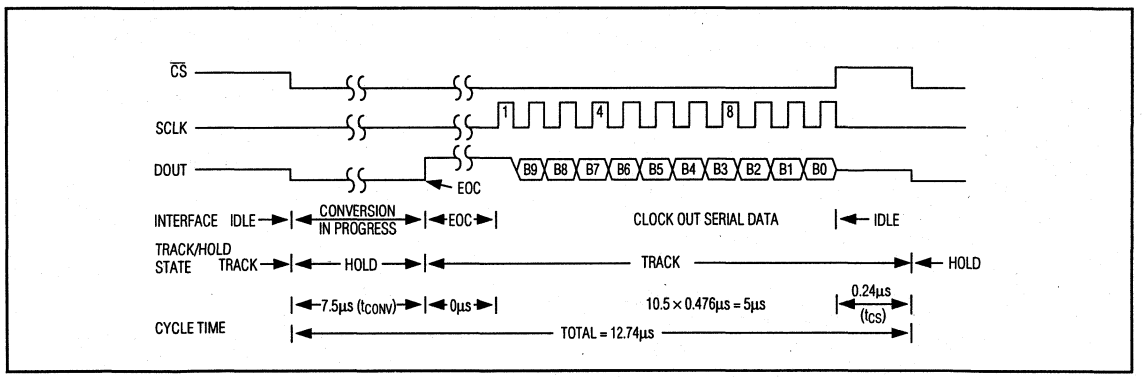


Figure 7b. Interface Timing Sequence—Minimum Cycle Time

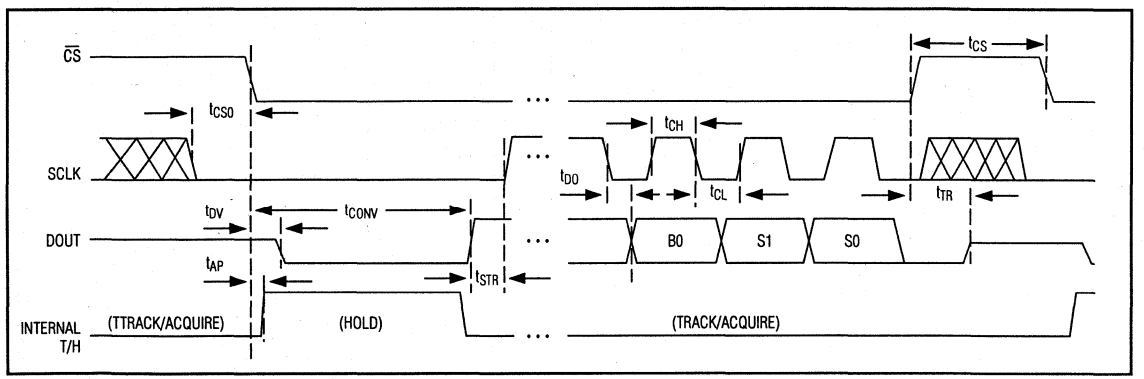


Figure 8. Detailed-Serial Interface Timing

+2.7V, Low-Power, 10-Bit Serial ADC

Output Coding and Transfer Function

The data output from the MAX1243 is binary, and Figure 9 depicts the nominal transfer function. Code transitions occur halfway between successive-integer LSB values. If V_{REF} = +2.500V, then 1LSB = 2.44mV or 2.500V/1024.

Applications Information

Connection to Standard Interfaces

The MAX1243 serial interface is fully compatible with SPI, QSPI, and Microwire standard serial interfaces (Figure 10).

If a serial interface is available, set the CPU's serial interface in master mode so the CPU generates the serial clock. Choose a clock frequency up to 2.1MHz.

1) Use a general-purpose I/O line on the CPU to pull $\overline{CS}$ low. Keep SCLK low.
2) Wait the for the maximum conversion time specified before activating SCLK. Alternatively, look for a DOUT rising edge to determine the end of conversion.
3) Activate SCLK for a minimum of 11 clock cycles. The first falling clock edge will produce the MSB of the DOUT conversion. DOUT output data transitions on SCLK's falling edge and is available in MSB-first format. Observe the SCLK to DOUT valid timing characteristic. Data can be clocked into the µP on SCLK's rising edge.
4) Pull $\overline{CS}$ high at or after the 11th falling clock edge. If $\overline{CS}$ remains low, the two sub-bits and trailing zeros are clocked out after the LSB.
5) With $\overline{CS}$ = high, wait the minimum specified time, t_{CS}, before initiating a new conversion by pulling $\overline{CS}$ low. If a conversion is aborted by pulling $\overline{CS}$ high before the conversion's end, wait for the minimum acquisition time, t_{ACQ}, before starting a new conversion.

Data can be output in two bytes or continuously, as shown in Figures 7a and 7b. The bytes will contain the result of the conversion padded with one leading 1, two sub-bits and trailing 0s if SCLK is still active with $\overline{CS}$ kept low.

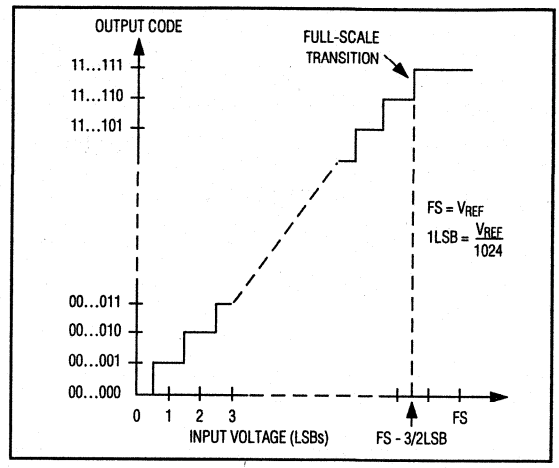


Figure 9. Unipolar Transfer Function, Full Scale (FS) = V_{REF}, Zero Scale (ZS) = GND

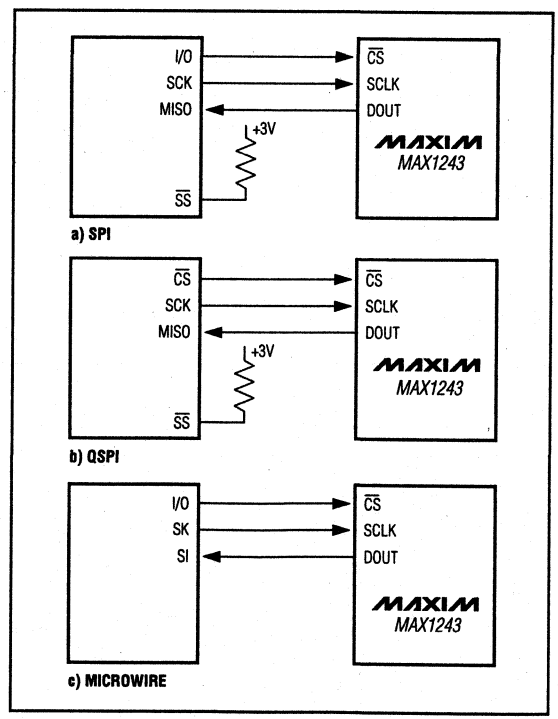


Figure 10. Common Serial-Interface Connections to the MAX1243

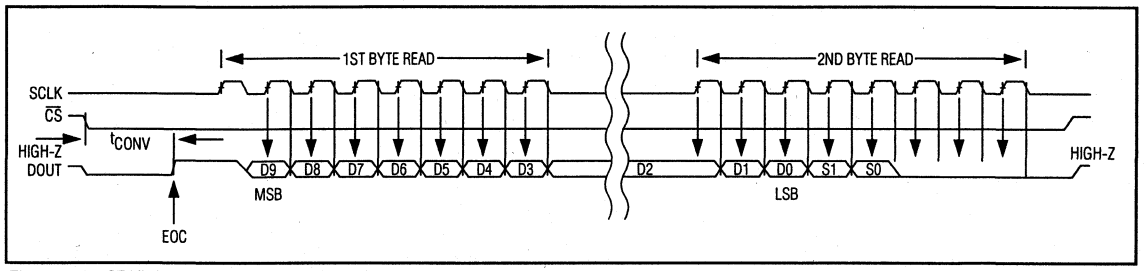


Figure 11. SPI/Microwire Serial Interface Timing (CPOL = CPHA = 0)

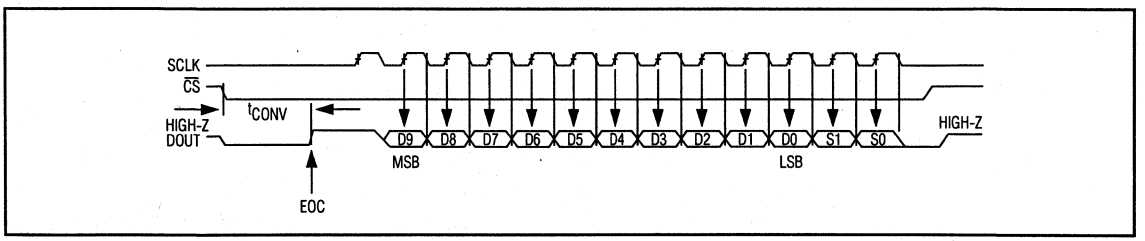


Figure 12. QSPI Serial Interface Timing (CPOL = CPHA = 0)

SPI and Microwire

When using SPI or QSPI, set CPOL = 0 and CPHA = 0. Conversion begins with a $\overline{CS}$ falling edge. DOUT goes low, indicating a conversion in progress. Wait until DOUT goes high or until the maximum specified 7.5µs conversion time elapses. Two consecutive 1-byte reads are required to get the full 10+2 bits from the ADC. DOUT output data transitions on SCLK's falling edge and is clocked into the µP on SCLK's rising edge.

The first byte contains a leading 1, and seven bits of conversion result. The second byte contains the remaining three bits, two sub-bits, and three trailing zeros. See Figure 10 for connections and Figure 11 for timing.

QSPI

Set CPOL = CPHA = 0. Unlike SPI, which requires two 1-byte reads to acquire the 10 bits of data from the ADC, QSPI allows the minimum number of clock cycles necessary to clock in the data. The MAX1243 requires 11 clock cycles from the µP to clock out the 10 bits of data. Additional clock cycles clock out the two sub-bits followed by trailing zeros (Figure 12). The maximum clock frequency to ensure compatibility with QSPI is 2.097MHz.

Layout, Grounding, and Bypassing

For best performance, use printed circuit boards. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

Chip Information

TRANSISTOR COUNT: 2554

SUBSTRATE CONNECTED TO GND

19-1066; Rev 0; 6/96

MAXIM

+2.375V, Low-Power, 8-Channel, Serial 12-Bit ADC

General Description

The MAX1245 12-bit data-acquisition system combines an 8-channel multiplexer, high-bandwidth track/hold, and serial interface with high conversion speed and ultra-low power consumption. It operates from a single +2.375V to +3.3V supply, and its analog inputs are software configurable for unipolar/bipolar and single-ended/differential operation.

The 4-wire serial interface directly connects to SPI™, QSPI™, and Microwire™ devices without external logic. A serial strobe output allows direct connection to TMS320-family digital signal processors. The MAX1245 works with an external reference, and uses either the internal clock or an external serial-interface clock to perform successive-approximation analog-to-digital conversions.

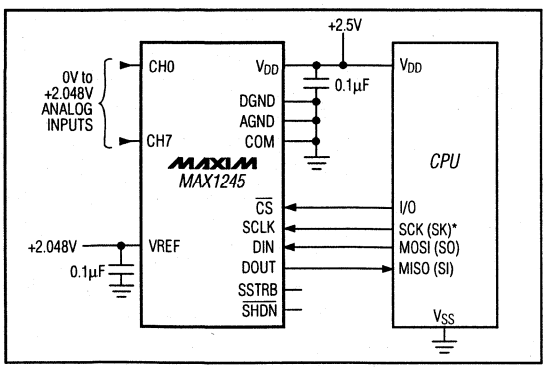
This device provides a hard-wired $\overline{SHDN}$ pin and a software-selectable power-down, and can be programmed to automatically shut down at the end of a conversion. Accessing the serial interface powers up the MAX1245, and the quick turn-on time allows it to be shut down between conversions. This technique can cut supply current to under 10µA at reduced sampling rates.

The MAX1245 is available in a 20-pin DIP package and an SSOP that occupies 30% less area than an 8-pin DIP. For supply voltages from +2.7V to +5.25V, use the pin-compatible MAX147.

Applications

Portable Data Logging
Battery-Powered Instruments
Medical Instruments
Data Acquisition

Typical Operating Circuit



Features

- ♦ **Single +2.375V to +3.3V Operation**
- ♦ **8-Channel Single-Ended or 4-Channel Differential Analog Inputs**
- ♦ **Low Power: 0.8mA (100ksps)**
  10µA (1ksps)
  1µA (power-down mode)
- ♦ **Internal Track/Hold, 100kHz Sampling Rate**
- ♦ **SPI/QSPI/Microwire/TMS320-Compatible 4-Wire Serial Interface**
- ♦ **Software-Configurable Unipolar or Bipolar Inputs**
- ♦ **20-Pin DIP/SSOP Packages**

Ordering Information

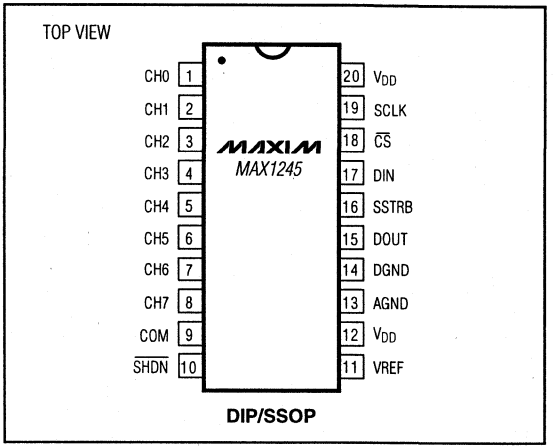
PART†	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX1245ACPP	0°C to +70°C	20 Plastic DIP	±1/2
MAX1245BCPP	0°C to +70°C	20 Plastic DIP	±1
MAX1245ACAP	0°C to +70°C	20 SSOP	±1/2
MAX1245BCAP	0°C to +70°C	20 SSOP	±1
MAX1245BC/D	0°C to +70°C	Dice*	±1

Ordering Information continued at end of data sheet.

† *Contact factory for availability of alternate surface-mount packages.*

* *Contact factory for availability.*

Pin Configuration



SPI and QSPI are registered trademarks of Motorola, Inc. Microwire is a registered trademark of National Semiconductor Corp.

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

+2.375V, Low-Power, 8-Channel, Serial 12-Bit ADC

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND, DGND ..... -0.3V to +6V
AGND to DGND ..... -0.3V to +0.3V
CH0–CH7, COM to AGND, DGND ..... -0.3V to (V_{DD} + 0.3V)
VREF to AGND ..... -0.3V to (V_{DD} + 0.3V)
Digital Inputs to DGND ..... -0.3V to +6V
Digital Outputs to DGND ..... -0.3V to (V_{DD} + 0.3V)
Digital Output Sink Current 25mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
SSOP (derate 8.00mW/°C above +70°C) 640mW
CERDIP (derate 11.11mW/°C above +70°C) 889mW
Operating Temperature Ranges
MAX1245_C_P ..... 0°C to +70°C
MAX1245_E_P ..... -40°C to +85°C
Storage Temperature Range ..... -60°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.375V to +3.3V, COM = 0V, f_{CLK} = 1.5MHz, external clock (50% duty cycle), 15 clocks/conversion cycle (100ksps), VREF = 2.048V applied to VREF pin, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)						
Resolution			12			Bits
Relative Accuracy (Note 2)	INL	MAX1245A			±0.5	LSB
		MAX1245B			±1.0	
Differential Nonlinearity	DNL	No missing codes over temperature			±1	LSB
Offset Error				±0.5	±4	LSB
Gain Error (Note 3)				±0.5	±4	LSB
Gain Temperature Coefficient				±0.25		ppm/°C
Channel-to-Channel Offset Matching				±0.2		LSB
DYNAMIC SPECIFICATIONS (10kHz sine-wave input, 0Vp-p to 2.048Vp-p, 100ksps, 1.5MHz external clock, bipolar input mode)						
Signal-to-Noise + Distortion Ratio	SINAD		68			dB
Total Harmonic Distortion	THD	Up to the 5th harmonic			-76	dB
Spurious-Free Dynamic Range	SFDR		76			dB
Channel-to-Channel Crosstalk		50kHz, $2V_{p-p}$ (Note 4)		-85		dB
Small-Signal Bandwidth		-3dB rolloff		2.25		MHz
Full-Power Bandwidth				1.0		MHz
CONVERSION RATE						
Conversion Time (Note 5)	t_{CONV}	Internal clock, $\overline{SHDN}$ = FLOAT	5.5		7.5	µs
		Internal clock, $\overline{SHDN}$ = V_{DD}	35		65	
		External clock = 1.5MHz, 12 clocks/conversion	8			
Track/Hold Acquisition Time	t_{ACQ}	External clock = 1.5MHz			2.0	µs
Aperture Delay				40		ns
Aperture Jitter				<50		ps
Internal Clock Frequency		$\overline{SHDN}$ = FLOAT		1.5		MHz
		$\overline{SHDN}$ = V_{DD}		0.225		
External Clock Frequency			0.1		1.5	MHz
		Data transfer only	0		1.5	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.375V to +3.3V, COM = 0V, f_{CLK} = 1.5MHz, external clock (50% duty cycle), 15 clocks/conversion cycle (100ksps), VREF = 2.048V applied to VREF pin, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG/COM INPUTS						
Input Voltage Range, Single-Ended and Differential (Note 6)		Unipolar, COM = 0V			0 to VREF	V
		Bipolar, COM = VREF/2			±VREF/2	
Multiplexer Leakage Current		On/off leakage current, V_{IN} = 0V or V_{DD}		±0.01	±1	µA
Input Capacitance		(Note 7)		16		pF
EXTERNAL REFERENCE						
VREF Input Voltage Range (Note 8)			1.0		V_{DD} + 50mV	V
VREF Input Current		VREF = 2.048V		82	120	µA
VREF Input Resistance			18	25		kΩ
Shutdown VREF Input Current				0.01	10	µA
DIGITAL INPUTS (DIN, SCLK, $\overline{CS}$, $\overline{SHDN}$)						
DIN, SCLK, $\overline{CS}$ Input High Voltage	V_{INH}		2.0			V
DIN, SCLK, $\overline{CS}$ Input Low Voltage	V_{INL}				0.8	V
DIN, SCLK, $\overline{CS}$ Input Hysteresis	V_{HYST}			0.2		V
DIN, SCLK, $\overline{CS}$ Input Leakage	I_{IN}	V_{IN} = 0V or V_{DD}		±0.01	±1	µA
DIN, SCLK, $\overline{CS}$ Input Capacitance	C_{IN}	(Note 7)			15	pF
$\overline{SHDN}$ Input High Voltage	V_{INH}		V_{DD} - 0.4			V
$\overline{SHDN}$ Input Low Voltage	V_{INL}				0.4	V
$\overline{SHDN}$ Input Current	I_{IN}	$\overline{SHDN}$ = 0V or V_{DD}			±4.0	µA
$\overline{SHDN}$ Input Mid Voltage	V_{IM}		$V_{DD}/2$ - 0.3		$V_{DD}/2$ + 0.3	V
$\overline{SHDN}$ Voltage, Floating	V_{FLT}	$\overline{SHDN}$ = open		$V_{DD}/2$		V
$\overline{SHDN}$ Maximum Allowed Leakage, Mid Input		$\overline{SHDN}$ = open			±80	nA
DIGITAL OUTPUTS (DOUT, SSTRB)						
Output Voltage Low	V_{OL}	I_{SINK} = 5mA			0.4	V
		I_{SINK} = 16mA		0.5		
Output Voltage High	V_{OH}	I_{SOURCE} =0.5mA	V_{DD} - 0.375			V
Three-State Leakage Current	I_L	$\overline{CS}$ = V_{DD}		±0.01	±10	µA
Three-State Output Capacitance	C_{OUT}	$\overline{CS}$ = V_{DD} (Note 7)			15	pF
POWER REQUIREMENTS						
Positive Supply Voltage	V_{DD}		2.375		3.3	V
Positive Supply Current	I_{DD}	Operating mode, full-scale input		0.8	1.3	mA
		Power-down		1.2	10	µA
Supply Rejection (Note 9)	PSR	V_{DD} = 2.375V to 3.3V, full-scale input, external reference = 2.048V		±0.3		mV

+2.375V, Low-Power, 8-Channel, Serial 12-Bit ADC

TIMING CHARACTERISTICS

(V_{DD} = +2.375V to +3.3V, COM = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

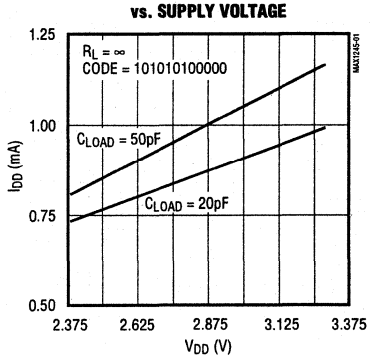
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Acquisition Time	t_{ACQ}		2.0			µs
DIN to SCLK Setup	t_{DS}		200			ns
DIN to SCLK Hold	t_{DH}				0	ns
SCLK Fall to Output Data Valid	t_{DO}	Figure 1	20		260	ns
$\overline{CS}$ Fall to Output Enable	t_{DV}	Figure 1			240	ns
$\overline{CS}$ Rise to Output Disable	t_{TR}	Figure 2			400	ns
$\overline{CS}$ to SCLK Rise Setup	t_{CSS}		200			ns
$\overline{CS}$ to SCLK Rise Hold	t_{CSH}		0			ns
SCLK Pulse Width High	t_{CH}		300			ns
SCLK Pulse Width Low	t_{CL}		300			ns
SCLK Fall to SSTRB	t_{SSTRB}	Figure 1			260	ns
$\overline{CS}$ Fall to SSTRB Output Enable	t_{SDV}	External clock mode only, Figure 1			240	ns
$\overline{CS}$ Rise to SSTRB Output Disable	t_{STR}	External clock mode only, Figure 2			400	ns
SSTRB Rise to SCLK Rise	t_{SCK}	Internal clock mode only (Note 7)	0			ns

Note 1: Tested at V_{DD} = +2.375V; COM = 0V; unipolar single-ended input mode.
Note 2: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range has been calibrated.
Note 3: External reference (VREF = +2.048V), offset nulled.
Note 4: Ground "on" channel; sine wave applied to all "off" channels.
Note 5: Conversion time defined as the number of clock cycles multiplied by the clock period; clock has 50% duty cycle.
Note 6: The common-mode range for the analog inputs is from AGND to V_{DD}.
Note 7: Guaranteed by design. Not subject to production testing.
Note 8: ADC performance is limited by the converter's noise floor, typically 300µVp-p.
Note 9: Measured as $|V_{FS}(2.375V) - V_{FS}(3.3V)|$.

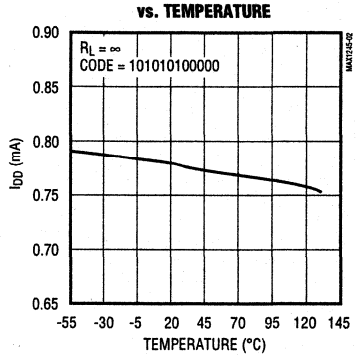
Typical Operating Characteristics

(V_{DD} = 2.5V, VREF = 2.048V, f_{CLK} = 1.5MHz, C_{LOAD} = 20pF, T_A = +25°C, unless otherwise noted.)

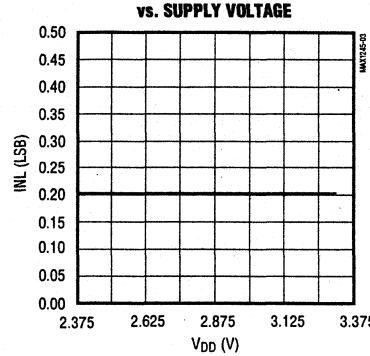
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



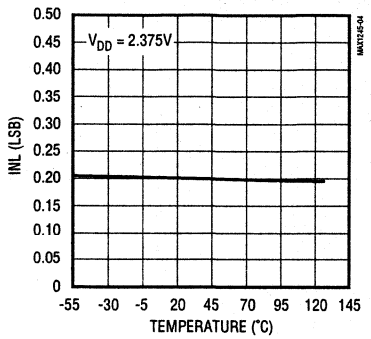
INTEGRAL NONLINEARITY vs. SUPPLY VOLTAGE



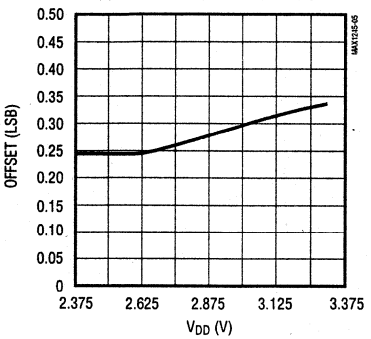
Typical Operating Characteristics (continued)

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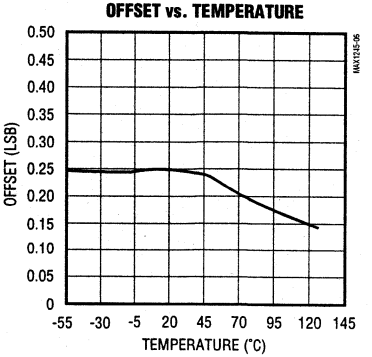
INTEGRAL NONLINEARITY vs. TEMPERATURE



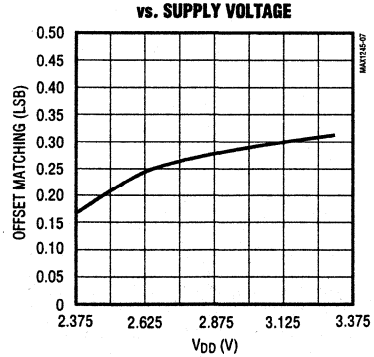
OFFSET vs. SUPPLY VOLTAGE



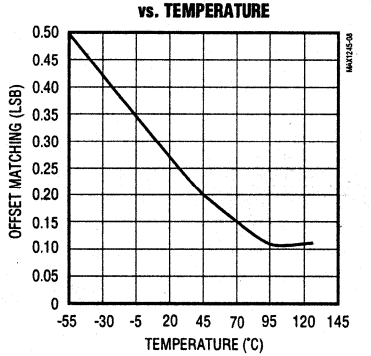
OFFSET vs. TEMPERATURE



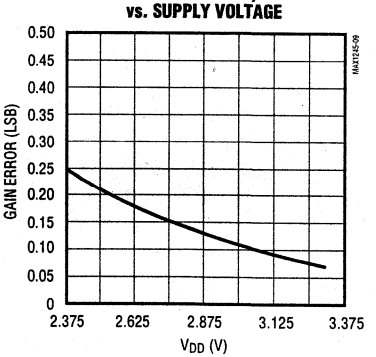
CHANNEL-TO-CHANNEL OFFSET MATCHING vs. SUPPLY VOLTAGE



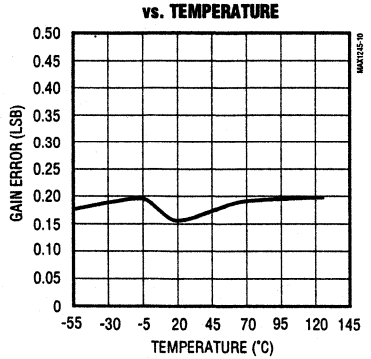
CHANNEL-TO-CHANNEL OFFSET MATCHING vs. TEMPERATURE



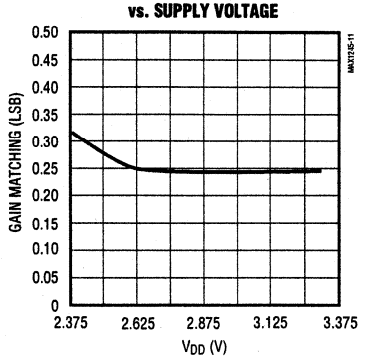
GAIN ERROR vs. SUPPLY VOLTAGE



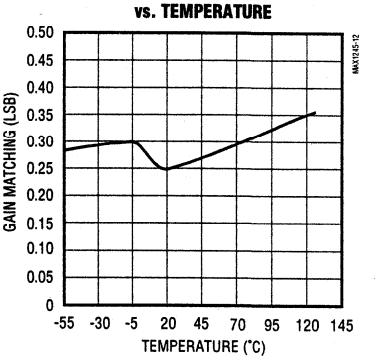
GAIN ERROR vs. TEMPERATURE



CHANNEL-TO-CHANNEL GAIN MATCHING vs. SUPPLY VOLTAGE



CHANNEL-TO-CHANNEL GAIN MATCHING vs. TEMPERATURE

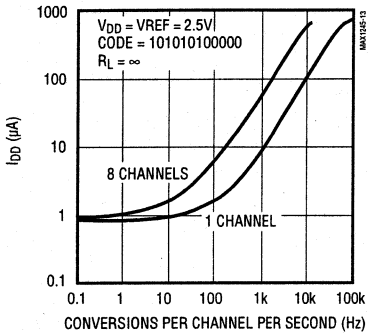


+2.375V, Low-Power, 8-Channel, Serial 12-Bit ADC

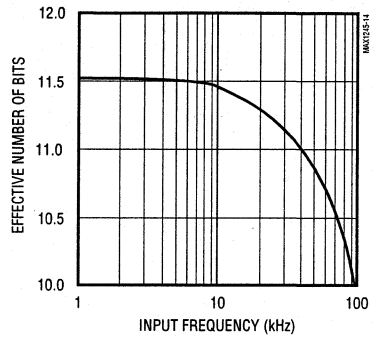
Typical Operating Characteristics (continued)

(V_{DD} = 2.5V, VREF = 2.048V, f_{CLK} = 1.5MHz, C_{LOAD} = 20pF, T_A = +25°C, unless otherwise noted.)

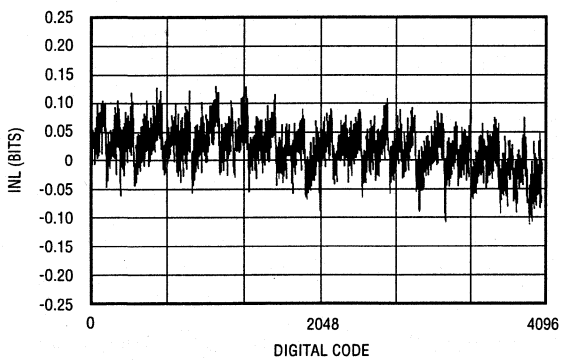
AVERAGE SUPPLY CURRENT vs. CONVERSION RATE



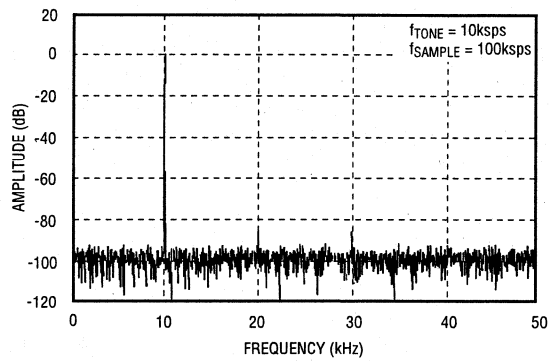
EFFECTIVE NUMBER OF BITS vs. INPUT FREQUENCY



INTEGRAL NONLINEARITY



FFT PLOT



+2.375V, Low-Power, 8-Channel, Serial 12-Bit ADC

Pin Description

PIN	NAME	FUNCTION
1–8	CH0–CH7	Sampling Analog Inputs
9	COM	Ground reference for analog inputs. Sets zero-code voltage in single-ended mode. Must be stable to ±0.5LSB.
10	$\overline{SHDN}$	Three-Level Shutdown Input. Pulling $\overline{SHDN}$ low shuts the MAX1245 down to 10µA (max) supply current; otherwise, the MAX1245 is fully operational. Letting $\overline{SHDN}$ float sets the internal clock frequency to 1.5MHz. Pulling $\overline{SHDN}$ high sets the internal clock frequency to 225kHz. See *Hardware Power-Down* section.
11	VREF	External Reference Voltage Input for analog-to-digital conversion
12, 20	V_{DD}	Positive Supply Voltage
13	AGND	Analog Ground
14	DGND	Digital Ground
15	DOUT	Serial Data Output. Data is clocked out at the falling edge of SCLK. High impedance when $\overline{CS}$ is high.
16	SSTRB	Serial Strobe Output. In internal clock mode, SSTRB goes low when the MAX1245 begins the A/D conversion and goes high when the conversion is done. In external clock mode, SSTRB pulses high for one clock period before the MSB decision. High impedance when $\overline{CS}$ is high (external clock mode).
17	DIN	Serial Data Input. Data is clocked in at the rising edge of SCLK.
18	$\overline{CS}$	Active-Low Chip Select. Data will not be clocked into DIN unless $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT is high impedance.
19	SCLK	Serial Clock Input. Clocks data in and out of serial interface. In external clock mode, SCLK also sets the conversion speed. (Duty cycle must be 40% to 60%.)

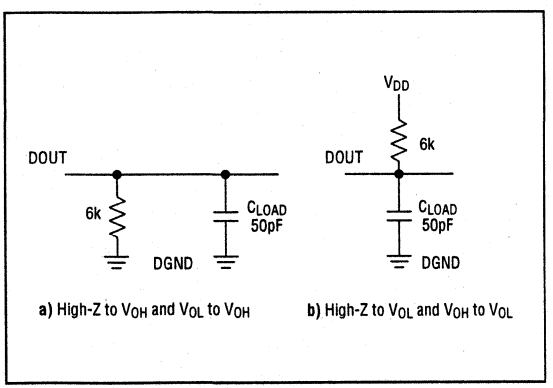


Figure 1. Load Circuits for Enable Time

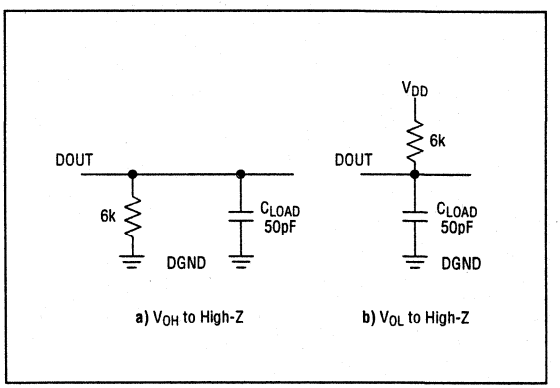


Figure 2. Load Circuits for Disable Time

+2.375V, Low-Power, 8-Channel, Serial 12-Bit ADC

Detailed Description

The MAX1245 analog-to-digital converter (ADC) uses a successive-approximation conversion technique and input track/hold (T/H) circuitry to convert an analog signal to a 12-bit digital output. A flexible serial interface provides easy interface to microprocessors (µPs). No external hold capacitors are required. Figure 3 is a block diagram of the MAX1245.

Pseudo-Differential Input

The sampling architecture of the ADC's analog comparator is illustrated in the equivalent input circuit (Figure 4). In single-ended mode, IN+ is internally switched to CH0–CH7, and IN- is switched to COM. In differential mode, IN+ and IN- are selected from the following pairs: CH0/CH1, CH2/CH3, CH4/CH5, and CH6/CH7. Configure the channels with Tables 2 and 3.

In differential mode, IN- and IN+ are internally switched to either of the analog inputs. This configuration is pseudo-differential to the effect that only the signal at IN+ is sampled. The return side (IN-) must remain stable within ±0.5LSB (±0.1LSB for best results) with respect to AGND during a conversion. To accomplish this, connect a 0.1µF capacitor from IN- (the selected analog input) to AGND.

During the acquisition interval, the channel selected as the positive input (IN+) charges capacitor C_{HOLD}. The acquisition interval spans three SCLK cycles and ends on the falling SCLK edge after the last bit of the input control word has been entered. At the end of the acquisition interval, the T/H switch opens, retaining charge on C_{HOLD} as a sample of the signal at IN+.

The conversion interval begins with the input multiplexer switching C_{HOLD} from the positive input, IN+, to the negative input, IN- (In single-ended mode, IN- is simply COM). This unbalances node ZERO at the input of the comparator. The capacitive DAC adjusts during the remainder of the conversion cycle to restore node ZERO to 0V within the limits of 12-bit resolution. This action is equivalent to transferring a charge of 16pF x [(V_{IN+}) - (V_{IN-})] from C_{HOLD} to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog input signal.

Track/Hold

The T/H enters its tracking mode on the falling clock edge after the fifth bit of the 8-bit control word has been shifted in. It enters its hold mode on the falling clock edge after the eighth bit of the control word has been shifted in. If the converter is set up for single-ended inputs, IN- is connected to COM, and the converter samples the "+" input. If the converter is set up for differential inputs, IN- connects to the "-" input, and the difference of |IN+ - IN-| is sampled. At the end of the conversion, the positive input connects back to IN+, and C_{HOLD} charges to the input signal.

The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens, and more time must be allowed between conversions. The acquisition time, t_{ACQ}, is the maximum time the device takes to acquire the signal, and is also the minimum time needed for the signal to be acquired. It is calculated by:

$$t_{ACQ} = 9 \times (R_S + R_{IN}) \times 16pF$$

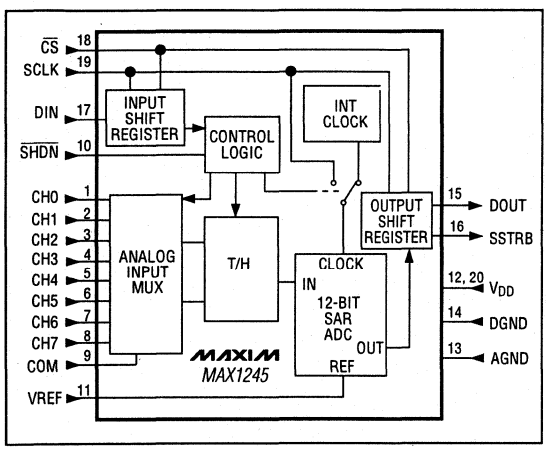


Figure 3. Block Diagram

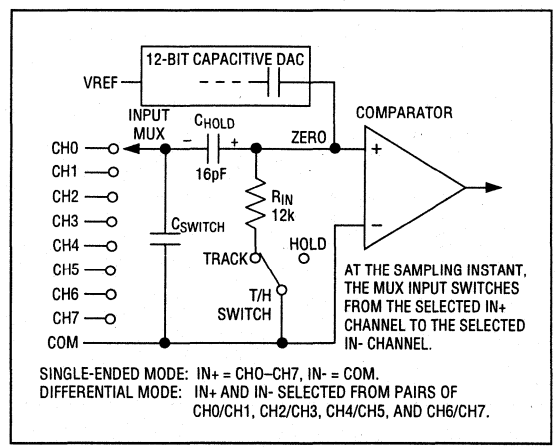


Figure 4. Equivalent Input Circuit

where R_{IN} = 12kΩ, R_S = the source impedance of the input signal, and t_{ACQ} is never less than 2.0µs. Note that source impedances below 1kΩ do not significantly affect the AC performance of the ADC. Higher source impedances can be used if an input capacitor is connected to the analog inputs, as shown in Figure 5. Note that the input capacitor forms an RC filter with the input source impedance, limiting the ADC's signal bandwidth.

Input Bandwidth

The ADC's input tracking circuitry has a 2.25MHz small-signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

Analog Input Protection

Internal protection diodes, which clamp the analog input to V_{DD} and AGND, allow the channel input pins to swing from AGND - 0.3V to V_{DD} + 0.3V without damage. However, for accurate conversions near full scale, the inputs must not exceed V_{DD} by more than 50mV or be lower than AGND by 50mV.

If the analog input exceeds 50mV beyond the supplies, do not forward bias the protection diodes of off channels over two milliamperes, as excessive current will degrade the conversion accuracy of the on channel.

Quick Look

To quickly evaluate the MAX1245's analog performance, use the circuit of Figure 5. The MAX1245 requires a control byte to be written to DIN before each conversion. Tying DIN to V_{DD} feeds in control bytes of $FF (HEX), which trigger single-ended unipolar conversions on CH7 in external clock mode without powering down between conversions. In external clock mode, the SSTRB output pulses high for one clock period before the most significant bit of the 12-bit conversion result is shifted out of DOUT. Varying the analog input to CH7 alters the sequence of bits from DOUT. A total of 15 clock cycles is required per conversion. All transitions of the SSTRB and DOUT outputs occur on the falling edge of SCLK.

How to Start a Conversion

A conversion is started by clocking a control byte into DIN. With $\overline{CS}$ low, each rising edge on SCLK clocks a bit from DIN into the MAX1245's internal shift register. After $\overline{CS}$ falls, the first arriving logic "1" bit defines the MSB of the control byte. Until this first "start" bit arrives, any number of logic "0" bits can be clocked into DIN with no effect. Table 1 shows the control-byte format.

The MAX1245 is compatible with Microwire, SPI, and QSPI devices. For SPI, select the correct clock polarity and sampling edge in the SPI control registers: set CPOL = 0 and CPHA = 0. Microwire, SPI, and QSPI all transmit a byte and receive a byte at the same time. Using the *Typical Operating Circuit,* the simplest software interface requires only three 8-bit transfers to

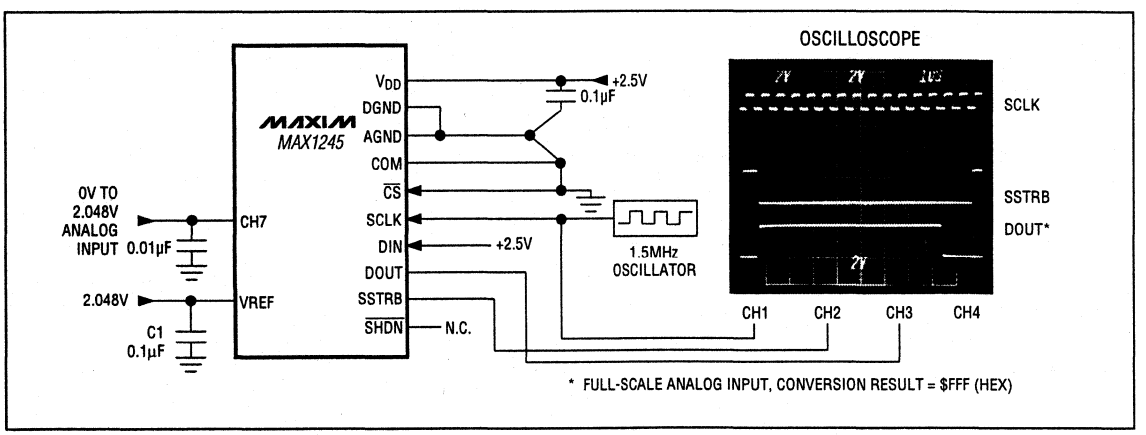


Figure 5. Quick-Look Circuit

+2.375V, Low-Power, 8-Channel, Serial 12-Bit ADC

Table 1. Control-Byte Format

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
START	SEL2	SEL1	SEL0	UNI/$\overline{BIP}$	SGL/$\overline{DIF}$	PD1	PD0

BIT	NAME	DESCRIPTION
7(MSB)	START	The first logic "1" bit after $\overline{CS}$ goes low defines the beginning of the control byte.
6 5 4	SEL2 SEL1 SEL0	These three bits select which of the eight channels are used for the conversion (Tables 2 and 3).
3	UNI/$\overline{BIP}$	1 = unipolar, 0 = bipolar. Selects unipolar or bipolar conversion mode. In unipolar mode, an analog input signal from 0V to VREF can be converted; in bipolar mode, the signal can range from -VREF/2 to +VREF/2.
2	SGL/$\overline{DIF}$	1 = single ended, 0 = differential. Selects single-ended or differential conversions. In single-ended mode, input signal voltages are referred to COM. In differential mode, the voltage difference between two channels is measured (Tables 2 and 3).
1 0(LSB)	PD1 PD0	Selects clock and power-down modes. PD1 PD0 Mode 0 0 Power-down (I_Q = 1.2µA) 0 1 Unassigned 1 0 Internal clock mode 1 1 External clock mode

Table 2. Channel Selection in Single-Ended Mode (SGL/$\overline{DIF}$ = 1)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	COM
0	0	0	+								–
1	0	0		+							–
0	0	1			+						–
1	0	1				+					–
0	1	0					+				–
1	1	0						+			–
0	1	1							+		–
1	1	1								+	–

Table 3. Channel Selection in Differential Mode (SGL/$\overline{DIF}$ = 0)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7
0	0	0	+	–						
0	0	1			+	–				
0	1	0					+	–		
0	1	1							+	–
1	0	0	–	+						
1	0	1			–	+				
1	1	0					–	+		
1	1	1							–	+

perform a conversion (one 8-bit transfer to configure the ADC, and two more 8-bit transfers to clock out the 12-bit conversion result). See Figure 17 for MAX1245 QSPI connections.

Simple Software Interface

Make sure the CPU's serial interface runs in master mode so the CPU generates the serial clock. Choose a clock frequency from 100kHz to 1.5MHz.

1) Set up the control byte for external clock mode and call it TB1. TB1 should be of the format: 1XXXXX11 binary, where the Xs denote the particular channel and conversion mode selected.
2) Use a general-purpose I/O line on the CPU to pull $\overline{CS}$ low.
3) Transmit TB1 and, simultaneously, receive a byte and call it RB1. Ignore RB1.
4) Transmit a byte of all zeros ($00 HEX) and, simultaneously, receive byte RB2.
5) Transmit a byte of all zeros ($00 HEX) and, simultaneously, receive byte RB3.
6) Pull $\overline{CS}$ high.

Figure 6 shows the timing for this sequence. Bytes RB2 and RB3 will contain the result of the conversion padded with one leading zero and three trailing zeros. The total conversion time is a function of the serial clock frequency and the amount of idle time between 8-bit transfers. Make sure that the total conversion time does not exceed 120µs, to avoid excessive T/H droop.

Digital Output

In unipolar input mode, the output is straight binary (Figure 14). For bipolar inputs, the output is two's-complement (Figure 15). Data is clocked out at the falling edge of SCLK in MSB-first format.

Clock Modes

The MAX1245 may use either an external serial clock or the internal clock to perform the successive-approximation conversion. In both clock modes, the external clock shifts data in and out of the MAX1245. The T/H acquires the input signal as the last three bits of the control byte are clocked into DIN. Bits PD1 and PD0 of the control byte program the clock mode. Figures 7–10 show the timing characteristics common to both modes.

External Clock

In external clock mode, the external clock not only shifts data in and out, it also drives the analog-to-digital conversion. SSTRB pulses high for one clock period after the control byte's last bit. Successive-approximation bit decisions are made and appear at DOUT on each of the next 12 SCLK falling edges (Figure 6). SSTRB and DOUT go into a high-impedance state when $\overline{CS}$ goes high; after the next $\overline{CS}$ falling edge, SSTRB outputs a logic low. Figure 8 shows the SSTRB timing in external clock mode.

The conversion must complete in some minimum time, or droop on the sample-and-hold capacitors may degrade conversion results. Use internal clock mode if the serial clock frequency is less than 100kHz, or if serial-clock interruptions could cause the conversion interval to exceed 120µs.

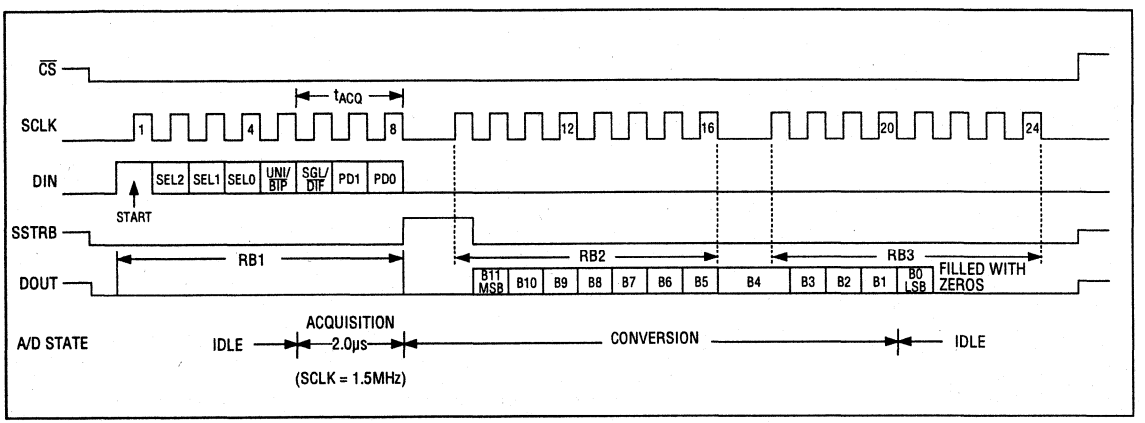


Figure 6. 24-Clock External-Clock-Mode Conversion Timing (Microwire and SPI Compatible, QSPI Compatible with $f_{CLK} \leq 1.5MHz$)

+2.375V, Low-Power, 8-Channel, Serial 12-Bit ADC

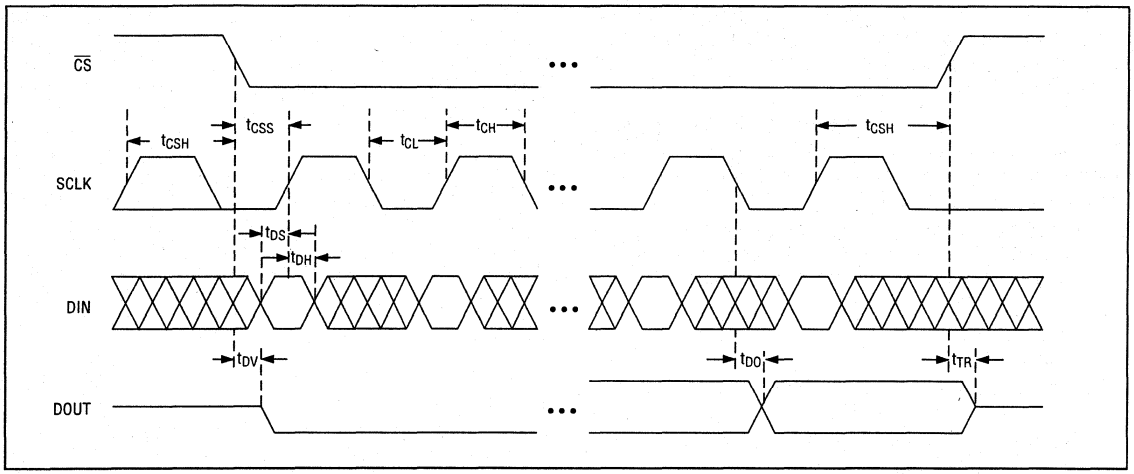


Figure 7. Detailed Serial-Interface Timing

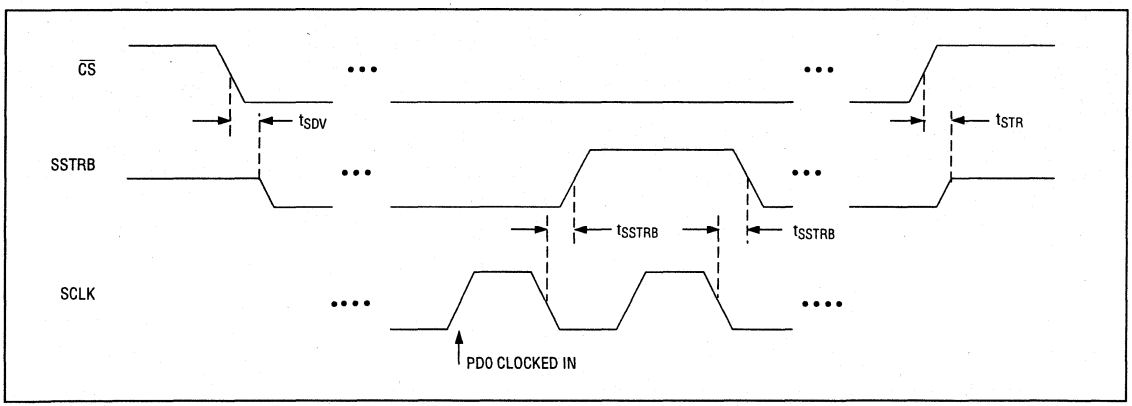


Figure 8. External-Clock-Mode SSTRB Detailed Timing

Internal Clock

In internal clock mode, the MAX1245 generates its own conversion clock internally. This frees the µP from the burden of running the SAR conversion clock and allows the conversion results to be read back at the processor's convenience, at any clock rate from zero to 1.5MHz. SSTRB goes low at the start of the conversion and then goes high when the conversion is complete. SSTRB will be low for a maximum of 7.5µs ($\overline{SHDN}$ = FLOAT), during which time SCLK should remain low for best noise performance.

An internal register stores data when the conversion is in progress. SCLK clocks the data out of this register at any time after the conversion is complete. After SSTRB goes high, the next falling clock edge produces the MSB of the conversion at DOUT, followed by the remaining bits in MSB-first format (Figure 9). $\overline{CS}$ does not need to be held low once a conversion is started. Pulling $\overline{CS}$ high prevents data from being clocked into the MAX1245 and three-states DOUT, but it does not adversely affect an internal clock-mode conversion already in progress. When internal clock mode is

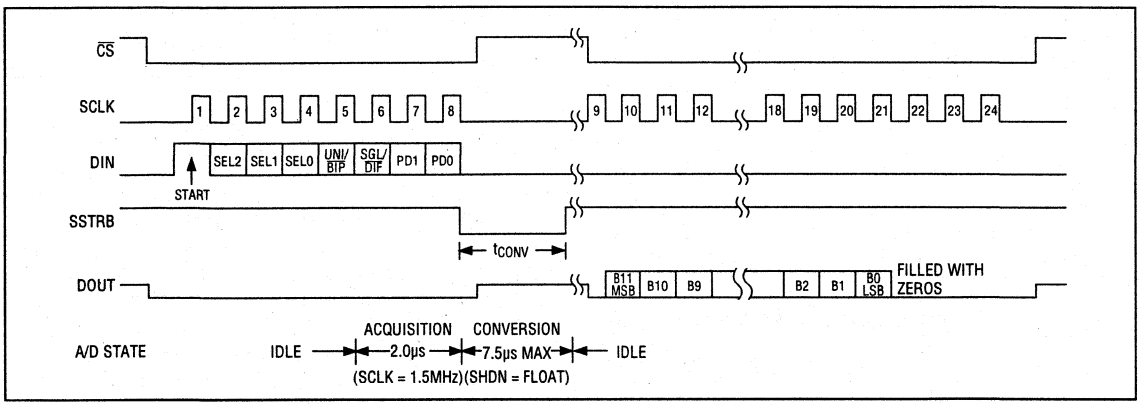


Figure 9. Internal Clock Mode Timing

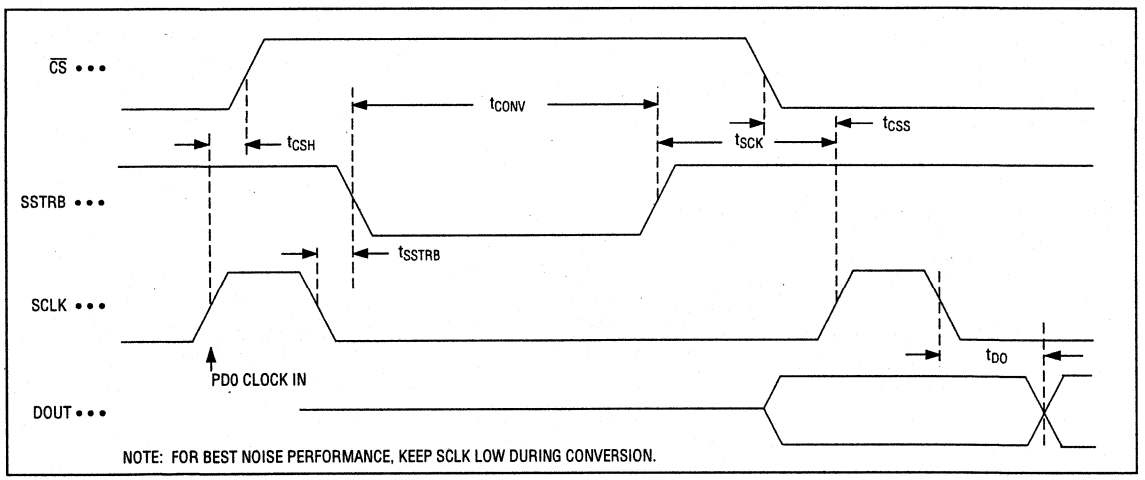


Figure 10. Internal Clock Mode SSTRB Detailed Timing

selected, SSTRB does not go into a high-impedance state when $\overline{CS}$ goes high.

Figure 10 shows the SSTRB timing in internal clock mode. In this mode, data can be shifted in and out of the MAX1245 at clock rates exceeding 1.5MHz, provided that the minimum acquisition time, t_{ACQ}, is kept above 2.0µs.

Data Framing

The falling edge of $\overline{CS}$ does **not** start a conversion on the MAX1245. The first logic high clocked into DIN is interpreted as a start bit and defines the first bit of the control byte. A conversion starts on the falling edge of SCLK, after the eighth bit of the control byte (the PD0 bit) is clocked into DIN. The start bit is defined as:

The first high bit clocked into DIN with $\overline{CS}$ low any time the converter is idle; e.g., after V_{DD} is applied.

OR

The first high bit clocked into DIN after bit 5 of a conversion in progress is clocked onto the DOUT pin.

If $\overline{CS}$ is toggled before the current conversion is complete, then the next high bit clocked into DIN is recognized as a start bit; the current conversion is terminated, and a new one is started.

+2.375V, Low-Power, 8-Channel, Serial 12-Bit ADC

The fastest the MAX1245 can run is 15 clocks per conversion with $\overline{CS}$ held low between conversions. Figure 11a shows the serial-interface timing necessary to perform a conversion every 15 SCLK cycles in external clock mode. If $\overline{CS}$ is low and SCLK is continuous, guarantee a start bit by first clocking in 16 zeros.

Most microcontrollers require that conversions occur in multiples of eight SCLK clocks; 16 clocks per conversion will typically be the fastest that a microcontroller can drive the MAX1245. Figure 11b shows the serial-interface timing necessary to perform a conversion every 16 SCLK cycles in external clock mode.

Applications Information

Power-On Reset

When power is first applied, and if $\overline{SHDN}$ is not pulled low, internal power-on reset circuitry activates the MAX1245 in internal clock mode, ready to convert with SSTRB = high. After the power supplies have stabilized, the internal reset time is 10µs, and no conversions should be performed during this phase. SSTRB is high on power-up and, if $\overline{CS}$ is low, the first logical 1 on DIN will be interpreted as a start bit. Until a conversion takes place, DOUT shifts out zeros.

Power-Down

The MAX1245's automatic power-down mode can save considerable power when operating at speeds below the maximum sampling rate. Figure 13 shows the average supply current as a function of the sampling rate. You can save power by placing the converter in a low-current shutdown state between conversions.

Select power-down via bits 1 and 0 of the DIN control byte with $\overline{SHDN}$ high (Tables 1 and 4). Pull $\overline{SHDN}$ low at any time to shut down the converter completely. $\overline{SHDN}$ overrides bits 1 and 0 of the control byte (Table 5).

Power-down mode turns off all chip functions that draw quiescent current, reducing I_{DD} typically to 1.2µA.

Figures 12a and 12b illustrate the various power-down sequences in both external and internal clock modes.

Software Power-Down

Software power-down is activated using bits PD1 and PD0 of the control byte. As shown in Table 4, PD1 and PD0

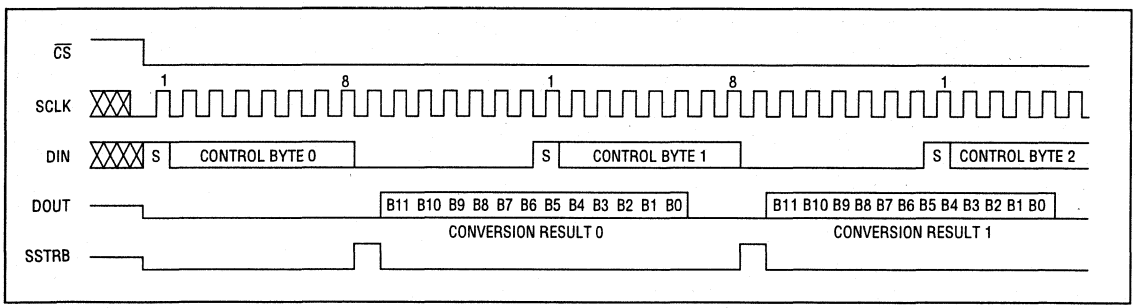


Figure 11a. External Clock Mode, 15 Clocks/Conversion Timing

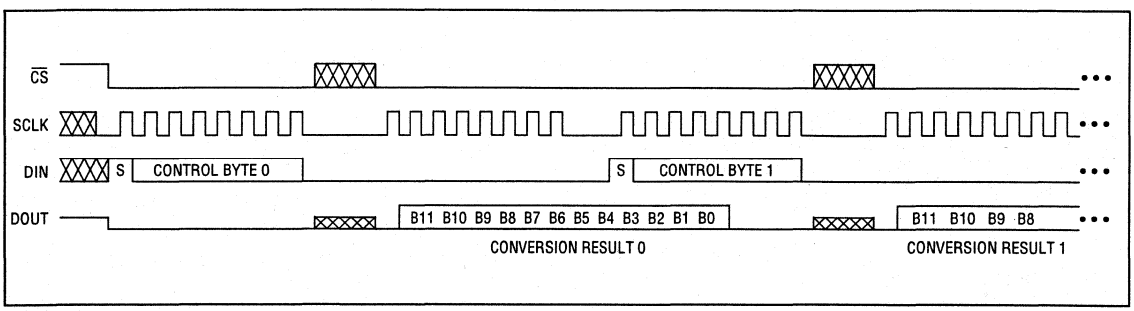


Figure 11b. External Clock Mode, 16 Clocks/Conversion Timing

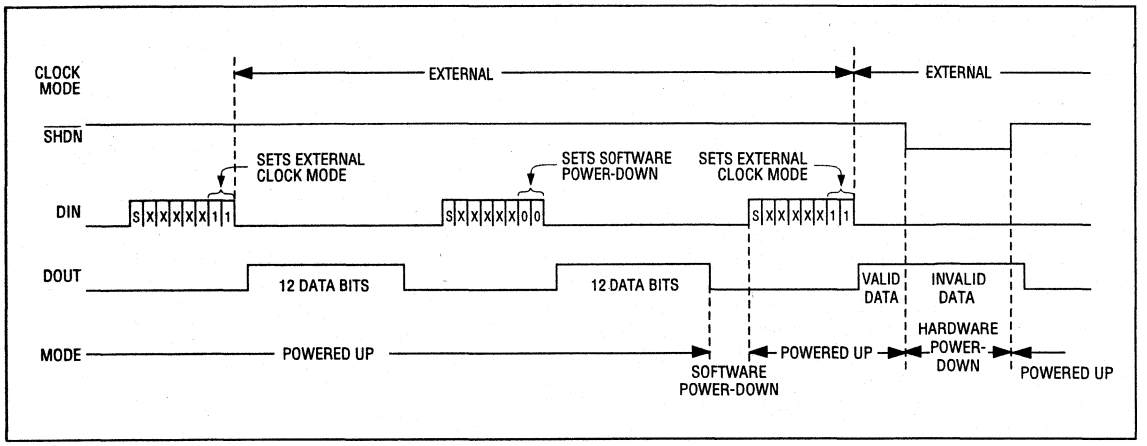


Figure 12a. Timing Diagram Power-Down Modes, External Clock

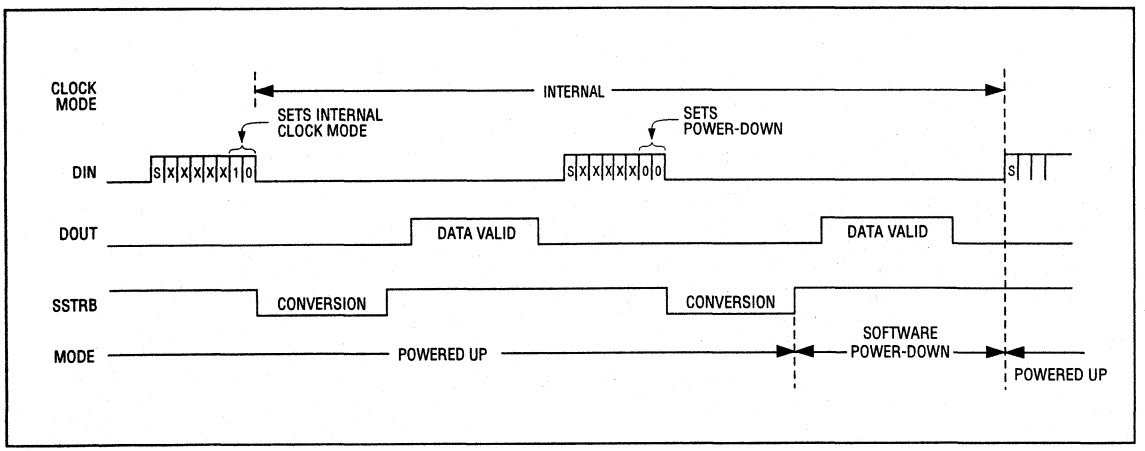


Figure 12b. Timing Diagram Power-Down Modes, Internal Clock

Table 4. Software Power-Down and Clock Mode

PD1	PD0	DEVICE MODE
1	1	External Clock
1	0	Internal Clock
0	1	Unassigned
0	0	Power-Down

Table 5. Hard-Wired Power-Down and Internal Clock Frequency

$\overline{SHDN}$ STATE	DEVICE MODE	INTERNAL CLOCK FREQUENCY
1	Enabled	225kHz
Floating	Enabled	1.5MHz
0	Power-Down	N/A

+2.375V, Low-Power, 8-Channel, Serial 12-Bit ADC

Table 6. Full Scale and Zero Scale

UNIPOLAR MODE		BIPOLAR MODE		
Full Scale	Zero Scale	Positive Full Scale	Zero Scale	Negative Full Scale
VREF + COM	COM	VREF/2 + COM	COM	-VREF/2 + COM

also specify the clock mode. When software shutdown is asserted, the ADC continues to operate in the last specified clock mode until the conversion is complete. Then the ADC powers down into a low quiescent-current state. In internal clock mode, the interface remains active and conversion results can be clocked out after the MAX1245 has entered a software power-down.

The first logical 1 on DIN is interpreted as a start bit, and powers up the MAX1245. Following the start bit, the data input word or control byte also determines clock mode and power-down states. For example, if the DIN word contains PD1 = 1, the chip remains powered up. If PD0 = PD1 = 0, a power-down resumes after one conversion.

Hardware Power-Down

Pulling $\overline{SHDN}$ low places the converter in hardware power-down. Unlike the software power-down mode, the conversion is not completed; it stops coincidentally with $\overline{SHDN}$ being brought low. $\overline{SHDN}$ also controls the clock frequency in internal clock mode. Letting $\overline{SHDN}$ float sets the internal clock frequency to 1.5MHz. When returning to normal operation with $\overline{SHDN}$ floating, there is a t_{RC} delay of approximately 2MΩ x C_L, where C_L is the capacitive loading on the $\overline{SHDN}$ pin. Pulling $\overline{SHDN}$ high sets the internal clock frequency to 225kHz. This feature eases the settling-time requirement for the reference voltage.

External Reference

An external reference is required for the MAX1245. The reference voltage range is 1V to V_{DD}.

At VREF, the input impedance is a minimum of 18kΩ for DC currents. During a conversion, the reference must be able to deliver up to 250µA DC load current and have an output impedance of 10Ω or less. If the reference has higher output impedance or is noisy, bypass it close to the VREF pin with a 0.1µF capacitor.

Transfer Function

Table 6 shows the full-scale voltage ranges for unipolar and bipolar modes using a 2.048V reference.

The external reference must have a temperature coefficient of 4ppm/°C or less to achieve accuracy to within 1LSB over the commercial temperature range of 0°C to +70°C.

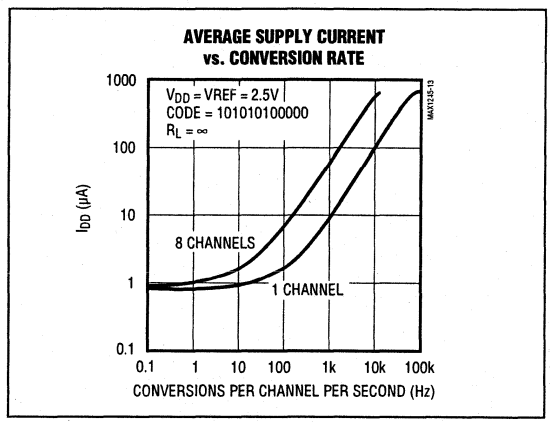


Figure 13. Average Supply Current vs. Conversion Rate

Figure 14 depicts the nominal, unipolar input/output (I/O) transfer function, and Figure 15 shows the bipolar input/output transfer function. Code transitions occur halfway between successive-integer LSB values. Output coding is binary, with 1LSB = 500µV (2.048V / 4096) for unipolar operation and 1LSB = 500µV [(2.048V / 2 - -2.048V / 2) / 4096] for bipolar operation.

Layout, Grounding, and Bypassing

For best performance, use printed circuit boards. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

Figure 16 shows the recommended system ground connections. A single-point analog ground ("star" ground point) should be established at AGND, separate from the logic ground. Connect all other analog grounds and DGND to the star ground. No other digital system ground should be connected to this ground. The ground return to the power supply for the star

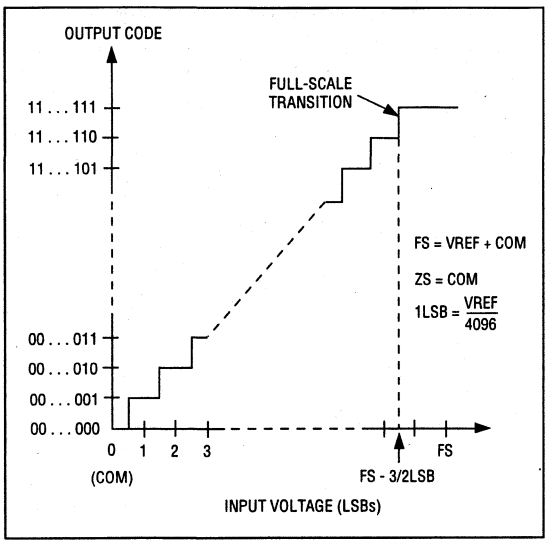


Figure 14. Unipolar Transfer Function, Full Scale (FS) = VREF + COM, Zero Scale (ZS) = COM

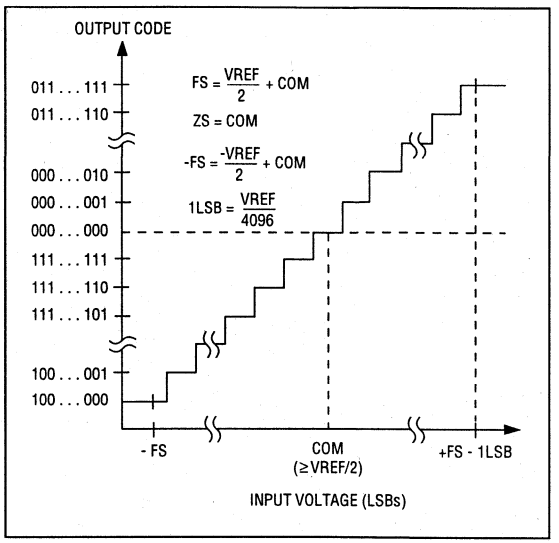


Figure 15. Bipolar Transfer Function, Full Scale (FS) = VREF / 2 + COM, Zero Scale (ZS) = COM

ground should be low impedance and as short as possible for noise-free operation.

High-frequency noise in the V_{DD} power supply may affect the high-speed comparator in the ADC. Bypass the supply to the star ground with 0.1µF and 4.7µF capacitors close to pin 20 of the MAX1245. Minimize capacitor lead lengths for best supply-noise rejection. If the +2.5V power supply is very noisy, a 10Ω resistor can be connected as a lowpass filter (Figure 16).

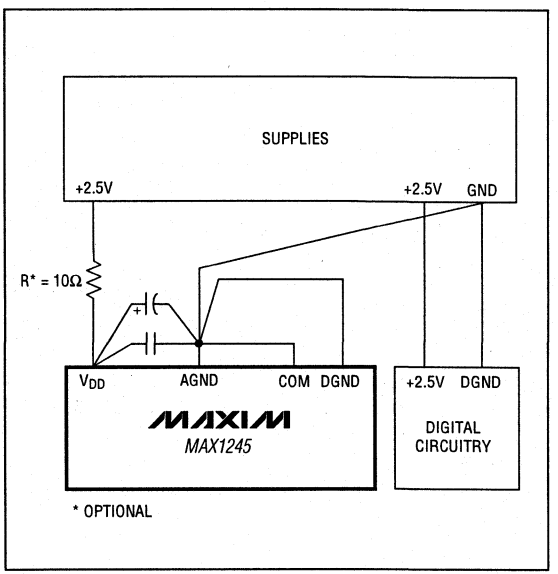


Figure 16. Power-Supply Grounding Connection

+2.375V, Low-Power, 8-Channel, Serial 12-Bit ADC

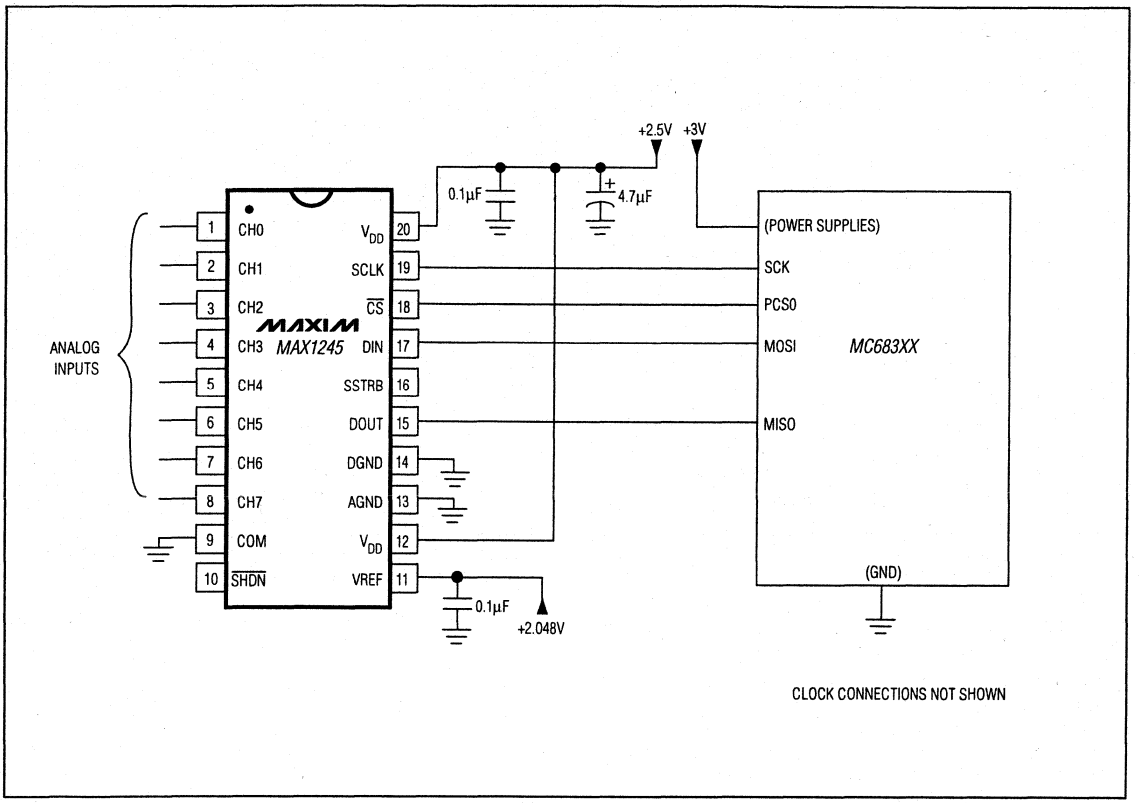


Figure 17. MAX1245 QSPI Connections

High-Speed Digital Interfacing with QSPI

The MAX1245 can interface with QSPI using the circuit in Figure 17 (f_{SCLK} = 1.5MHz, CPOL = 0, CPHA = 0). This QSPI circuit can be programmed to do a conversion on each of the eight channels. The result is stored in memory without taxing the CPU, since QSPI incorporates its own micro-sequencer.

Because the maximum external clock frequency is 1.5MHz, the MAX1245 is QSPI compatible up to 1.5MHz.

TMS320LC3x-to-MAX1245 Interface

Figure 18 shows an application circuit to interface the MAX1245 to the TMS320 in external clock mode. The timing diagram for this interface circuit is shown in Figure 19.

Use the following steps to initiate a conversion in the MAX1245 and to read the results:

1) The TMS320 should be configured with CLKX (transmit clock) as an active-high output clock and CLKR (TMS320 receive clock) as an active-high input clock. CLKX and CLKR on the TMS320 are tied together with the MAX1245's SCLK input.
2) The MAX1245's $\overline{CS}$ pin is driven low by the TMS320's XF_ I/O port, to enable data to be clocked into the MAX1245's DIN.
3) An 8-bit word (1XXXXX11) should be written to the MAX1245 to initiate a conversion and place the device into external clock mode. Refer to Table 1 to select the proper XXXXX bit values for your specific application.
4) The MAX1245's SSTRB output is monitored via the TMS320's FSR input. A falling edge on the SSTRB output indicates that the conversion is in progress and data is ready to be received from the MAX1245.
5) The TMS320 reads in one data bit on each of the next 16 rising edges of SCLK. These data bits represent the 12-bit conversion result followed by four trailing bits, which should be ignored.
6) Pull $\overline{CS}$ high to disable the MAX1245 until the next conversion is initiated.

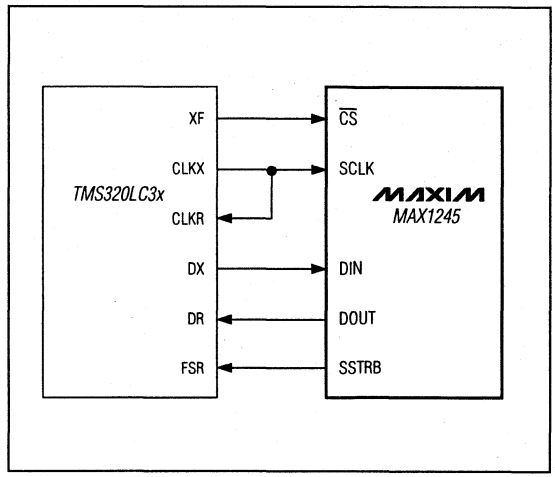


Figure 18. MAX1245-to-TMS320 Serial Interface

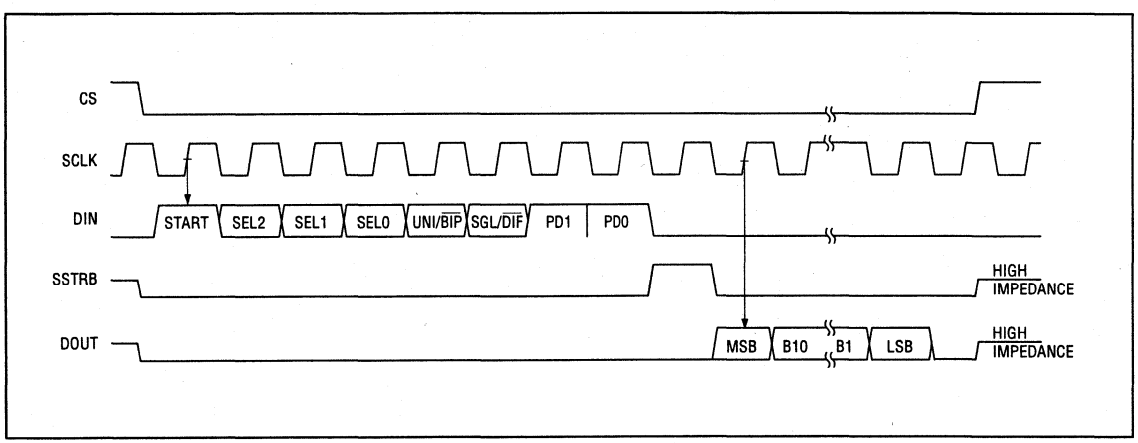


Figure 19. TMS320 Serial-Interface Timing Diagram

+2.375V, Low-Power, 8-Channel, Serial 12-Bit ADC

Ordering Information (continued)

PART†	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX1245AEPP	-40°C to +85°C	20 Plastic DIP	±1/2
MAX1245BEPP	-40°C to +85°C	20 Plastic DIP	±1
MAX1245AEAP	-40°C to +85°C	20 SSOP	±1/2
MAX1245BEAP	-40°C to +85°C	20 SSOP	±1

† *Contact factory for availability of alternate surface-mount packages.*

Chip Information

TRANSISTOR COUNT: 2554

19-1071; Rev 0; 6/96

EVALUATION KIT AVAILABLE

MAXIM

+2.7V to +5.25V, Low-Power, 4-Channel, Serial 12-Bit ADC in QSOP-16

General Description

The MAX1247 12-bit data-acquisition system combines a 4-channel multiplexer, high-bandwidth track/hold, and serial interface with high conversion speed and ultra-low power consumption. It operates from a single +2.7V to +5.25V supply, and its analog inputs are software configurable for unipolar/bipolar and single-ended/differential operation.

The 4-wire serial interface directly connects to SPI™, QSPI™, and Microwire™ devices without external logic. A serial strobe output allows direct connection to TMS320-family digital signal processors. The MAX1247 works with an external reference, and uses either the internal clock or an external serial-interface clock to perform successive-approximation analog-to-digital conversions.

This device provides a hard-wired $\overline{SHDN}$ pin and a software-selectable power-down, and can be programmed to automatically shut down at the end of a conversion. Accessing the serial interface automatically powers up the MAX1247, and the quick turn-on time allows it to be shut down between all conversions. This technique can cut supply current to under 10µA at reduced sampling rates.

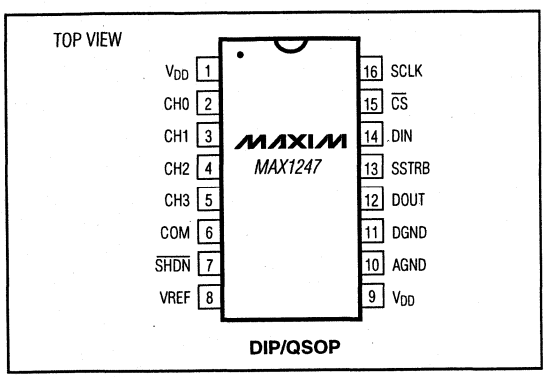
The MAX1247 is available in a 16-pin DIP and a very small QSOP that occupies the same board area as an 8-pin SO.

For an 8-channel version of this device, see the MAX147 data sheet.

Applications

Portable Data Logging
Medical Instruments
Pen Digitizers
Data Acquisition
Battery-Powered Instruments
Process Control

Pin Configuration



Features

- ♦ **4-Channel Single-Ended or 2-Channel Differential Inputs**
- ♦ **Single +2.7V to +5.25V Operation**
- ♦ **Low Power: 0.9mA (133ksps, 3V supply)**
  10µA (1ksps, 3V supply)
  1µA (power-down mode)
- ♦ **Internal Track/Hold, 133kHz Sampling Rate**
- ♦ **SPI/QSPI/Microwire/TMS320-Compatible 4-Wire Serial Interface**
- ♦ **Software-Configurable Unipolar or Bipolar Inputs**
- ♦ **16-Pin QSOP Package (same area as 8-pin SO)**

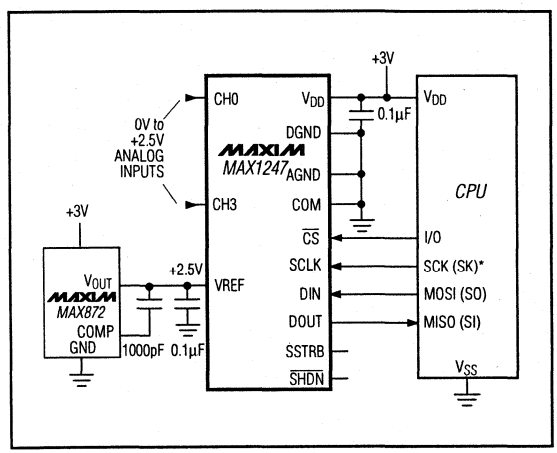
Ordering Information

PART†	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX1247ACPE	0°C to +70°C	16 Plastic DIP	±1/2
MAX1247BCPE	0°C to +70°C	16 Plastic DIP	±1
MAX1247ACEE	0°C to +70°C	16 QSOP	±1/2
MAX1247BCEE	0°C to +70°C	16 QSOP	±1

Ordering Information continued on last page.

† *Contact factory for availability of alternate surface-mount packages.*

Typical Operating Circuit



SPI and QSPI are registered trademarks of Motorola, Inc. Microwire is a registered trademark of National Semiconductor Corp.

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

+2.7V to +5.25V, Low-Power, 4-Channel, Serial 12-Bit ADC in QSOP-16

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND, DGND ..... -0.3V to +6V
AGND to DGND ..... -0.3V to +0.3V
CH0–CH7, COM to AGND, DGND ..... -0.3V to (V_{DD} + 0.3V)
VREF to AGND ..... -0.3V to (V_{DD} + 0.3V)
Digital Inputs to DGND ..... -0.3V to +6V
Digital Outputs to DGND ..... -0.3V to (V_{DD} + 0.3V)
Digital Output Sink Current 25mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
QSOP (derate 8.3mW/°C above +70°C) 667mW
CERDIP (derate 10.00mW/°C above +70°C) 800mW
Operating Temperature Ranges
MAX1247_C_E ..... 0°C to +70°C
MAX1247_E_E ..... -40°C to +85°C
MAX1247_MJE ..... -55°C to +125°C
Storage Temperature Range ..... -60°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +5.25V, COM = 0V, f_{CLK} = 2.0MHz, external clock (50% duty cycle), 15 clocks/conversion cycle (133ksps), VREF = 2.500V applied to VREF pin, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)						
Resolution			12			Bits
Relative Accuracy (Note 2)	INL	MAX1247A		±0.15	±0.5	LSB
		MAX1247B			±1.0	
Differential Nonlinearity	DNL	No missing codes over temperature			±1	LSB
Offset Error		MAX1247A		±0.25	±3	LSB
		MAX1247B		±0.25	±4	
Gain Error (Note 3)				±0.25	±4	LSB
Gain Temperature Coefficient				±0.25		ppm/°C
Channel-to-Channel Offset Matching				±0.25		LSB
DYNAMIC SPECIFICATIONS (10kHz sine-wave input, 0Vp-p to 2.500Vp-p, 133ksps, 2.0MHz external clock, bipolar input mode)						
Signal-to-Noise + Distortion Ratio	SINAD		70			dB
Total Harmonic Distortion	THD	Up to the 5th harmonic			-80	dB
Spurious-Free Dynamic Range	SFDR		80			dB
Channel-to-Channel Crosstalk		65kHz, 2.500V_{p-p} (Note 4)		-85		dB
Small-Signal Bandwidth		-3dB rolloff		2.25		MHz
Full-Power Bandwidth				1.0		MHz
CONVERSION RATE						
Conversion Time (Note 5)	t_{CONV}	Internal clock, $\overline{SHDN}$ = FLOAT	5.5		7.5	µs
		Internal clock, $\overline{SHDN}$ = V_{DD}	35		65	
		External clock = 2MHz, 12 clocks/conversion	6			
Track/Hold Acquisition Time	t_{ACQ}				1.5	µs
Aperture Delay				30		ns
Aperture Jitter				<50		ps
Internal Clock Frequency		$\overline{SHDN}$ = FLOAT		1.8		MHz
		$\overline{SHDN}$ = V_{DD}		0.225		
External Clock Frequency			0.1		2.0	MHz
		Data transfer only	0		2.0	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +5.25V, COM = 0V, f_{CLK} = 2.0MHz, external clock (50% duty cycle), 15 clocks/conversion cycle (133ksps), VREF = 2.500V applied to VREF pin, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG/COM INPUTS							
Input Voltage Range, Single-Ended and Differential (Note 6)		Unipolar, COM = 0V				0 to VREF	V
		Bipolar, COM = VREF / 2				±VREF / 2	
Multiplexer Leakage Current		On/off leakage current, V_{IN} = 0V or V_{DD}			±0.01	±1	µA
Input Capacitance		(Note 7)			16		pF
EXTERNAL REFERENCE							
VREF Input Voltage Range (Note 8)				1.0		V_{DD} + 50mV	V
VREF Input Current		VREF = 2.500V			100	150	µA
VREF Input Resistance				18	25		kΩ
Shutdown VREF Input Current					0.01	10	µA
DIGITAL INPUTS (DIN, SCLK, $\overline{CS}$, $\overline{SHDN}$)							
DIN, SCLK, $\overline{CS}$ Input High Voltage	V_{INH}	$V_{DD} \le 3.6V$		2.0			V
		$V_{DD} > 3.6V$		3.0			
DIN, SCLK, $\overline{CS}$ Input Low Voltage	V_{INL}					0.8	V
DIN, SCLK, $\overline{CS}$ Input Hysteresis	V_{HYST}				0.2		V
DIN, SCLK, $\overline{CS}$ Input Leakage	I_{IN}	V_{IN} = 0V or V_{DD}			±0.01	±1	µA
DIN, SCLK, $\overline{CS}$ Input Capacitance	C_{IN}	(Note 7)				15	pF
$\overline{SHDN}$ Input High Voltage	V_{INH}			V_{DD} - 0.4			V
$\overline{SHDN}$ Input Low Voltage	V_{INL}					0.4	V
$\overline{SHDN}$ Input Current	I_{IN}	$\overline{SHDN}$ = 0V or V_{DD}				±4.0	µA
$\overline{SHDN}$ Input Mid Voltage	V_{IM}			1.1		V_{DD} - 1.1	V
$\overline{SHDN}$ Voltage, Floating	V_{FLT}	$\overline{SHDN}$ = open			V_{DD} / 2		V
$\overline{SHDN}$ Maximum Allowed Leakage, Mid Input		$\overline{SHDN}$ = open				±100	nA
DIGITAL OUTPUTS (DOUT, SSTRB)							
Output Voltage Low	V_{OL}	I_{SINK} = 5mA				0.4	V
		I_{SINK} = 16mA				0.8	
Output Voltage High	V_{OH}	I_{SOURCE} = 0.5mA		V_{DD} - 0.5			V
Three-State Leakage Current	I_L	$\overline{CS}$ = V_{DD}			±0.01	±10	µA
Three-State Output Capacitance	C_{OUT}	$\overline{CS}$ = V_{DD} (Note 7)				15	pF
POWER REQUIREMENTS							
Positive Supply Voltage	V_{DD}			2.70		5.25	V
Positive Supply Current	I_{DD}	Operating mode, full-scale input	V_{DD} = 5.25V		1.8	2.5	mA
			V_{DD} = 3.6V		0.9	1.5	
		Power-down	V_{DD} = 5.25V		3.5	15	µA
			V_{DD} = 3.6V		1.2	10	
Supply Rejection (Note 9)	PSR	V_{DD} = 2.7V to 5.25V, full-scale input, external reference = 2.500V			±0.3		mV

7

+2.7V to +5.25V, Low-Power, 4-Channel, Serial 12-Bit ADC in QSOP-16

TIMING CHARACTERISTICS

(V_{DD} = +2.7V to +5.25V, COM = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

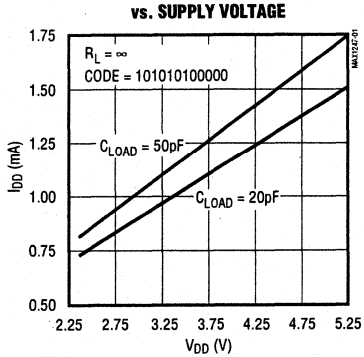
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Acquisition Time	t_{ACQ}			1.5			µs
DIN to SCLK Setup	t_{DS}			100			ns
DIN to SCLK Hold	t_{DH}					0	ns
SCLK Fall to Output Data Valid	t_{DO}	Figure 1	MAX1247_C/E	20		200	ns
			MAX1247_M	20		240	
$\overline{CS}$ Fall to Output Enable	t_{DV}	Figure 1				240	ns
$\overline{CS}$ Rise to Output Disable	t_{TR}	Figure 2				240	ns
$\overline{CS}$ to SCLK Rise Setup	t_{CSS}			100			ns
$\overline{CS}$ to SCLK Rise Hold	t_{CSH}			0			ns
SCLK Pulse Width High	t_{CH}			200			ns
SCLK Pulse Width Low	t_{CL}			200			ns
SCLK Fall to SSTRB	t_{SSTRB}	Figure 1				240	ns
$\overline{CS}$ Fall to SSTRB Output Enable	t_{SDV}	External clock mode only, Figure 1				240	ns
$\overline{CS}$ Rise to SSTRB Output Disable	t_{STR}	External clock mode only, Figure 2				240	ns
SSTRB Rise to SCLK Rise	t_{SCK}	Internal clock mode only (Note 7)		0			ns

Note 1: Tested at V_{DD} = 2.7V; COM = 0V; unipolar single-ended input mode.
Note 2: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range has been calibrated.
Note 3: External reference (VREF = +2.500V), offset nulled.
Note 4: Ground "on" channel; sine wave applied to all "off" channels.
Note 5: Conversion time defined as the number of clock cycles multiplied by the clock period; clock has 50% duty cycle.
Note 6: The common-mode range for the analog inputs is from AGND to V_{DD}.
Note 7: Guaranteed by design. Not subject to production testing.
Note 8: ADC performance is limited by the converter's noise floor, typically 300µVp-p.
Note 9: Measured as $|V_{FS}(2.7V) - V_{FS}(5.25V)|$.

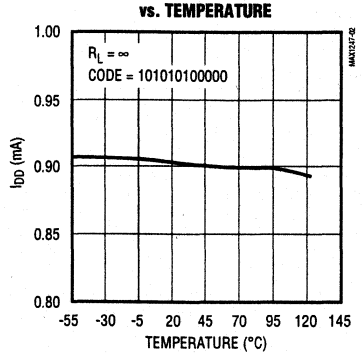
Typical Operating Characteristics

(V_{DD} = 3.0V, VREF = 2.500V, f_{CLK} = 2.0MHz, C_{LOAD} = 20pF, T_A = +25°C, unless otherwise noted.)

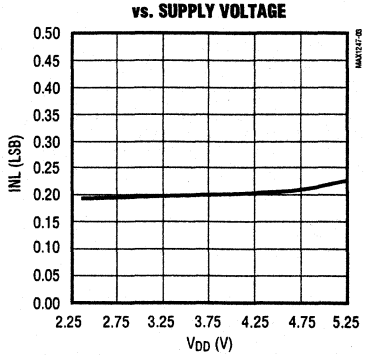
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



INTEGRAL NONLINEARITY vs. SUPPLY VOLTAGE

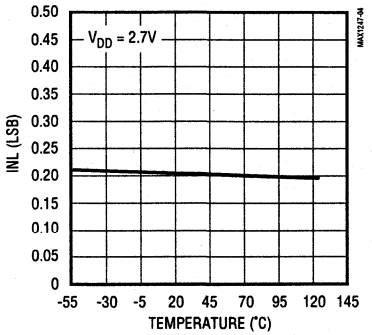


+2.7V to +5.25V, Low-Power, 4-Channel, Serial 12-Bit ADC in QSOP-16

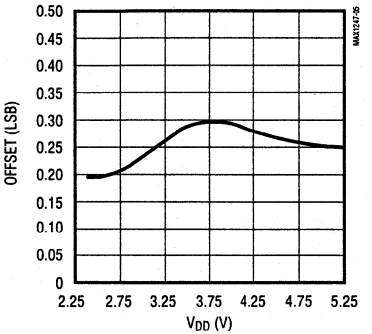
Typical Operating Characteristics (continued)

(V_{DD} = 3.0V, VREF = 2.500V, f_{CLK} = 2.0MHz, C_{LOAD} = 20pF, T_A = +25°C, unless otherwise noted.)

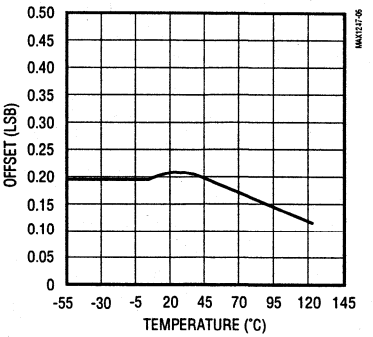
INTEGRAL NONLINEARITY vs. TEMPERATURE



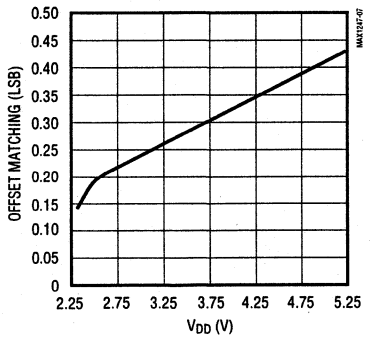
OFFSET vs. SUPPLY VOLTAGE



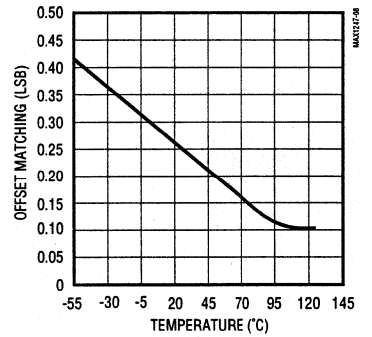
OFFSET vs. TEMPERATURE



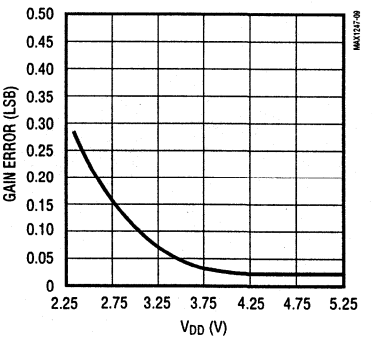
CHANNEL-TO-CHANNEL OFFSET MATCHING vs. SUPPLY VOLTAGE



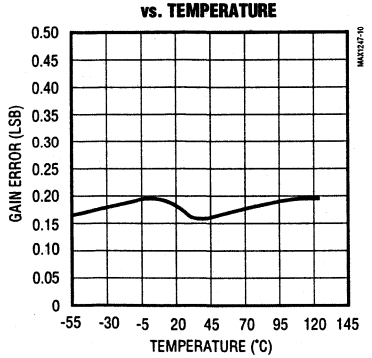
CHANNEL-TO-CHANNEL OFFSET MATCHING vs. TEMPERATURE



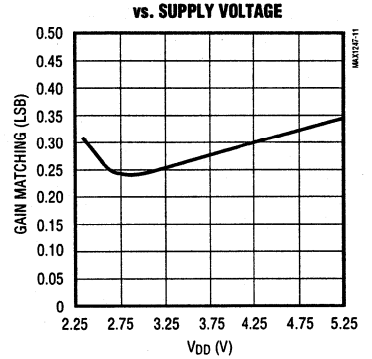
GAIN ERROR vs. SUPPLY VOLTAGE



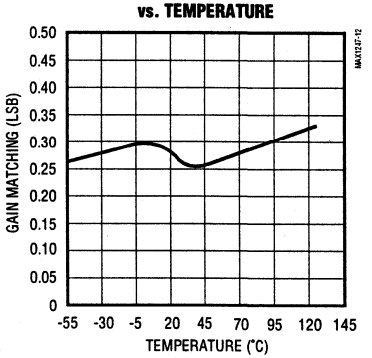
GAIN ERROR vs. TEMPERATURE



CHANNEL-TO-CHANNEL GAIN MATCHING vs. SUPPLY VOLTAGE



CHANNEL-TO-CHANNEL GAIN MATCHING vs. TEMPERATURE

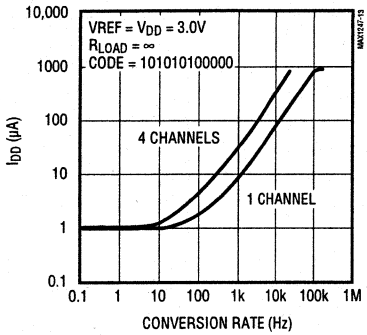


+2.7V to +5.25V, Low-Power, 4-Channel, Serial 12-Bit ADC in QSOP-16

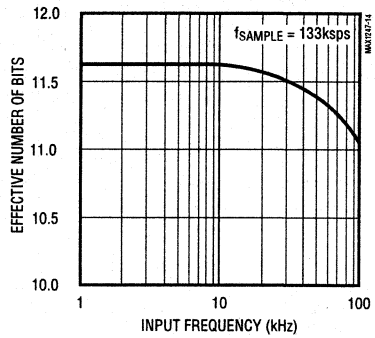
Typical Operating Characteristics (continued)

(V_{DD} = 3.0V, VREF = 2.500V, f_{CLK} = 2.0MHz, C_{LOAD} = 20pF, T_A = +25°C, unless otherwise noted.)

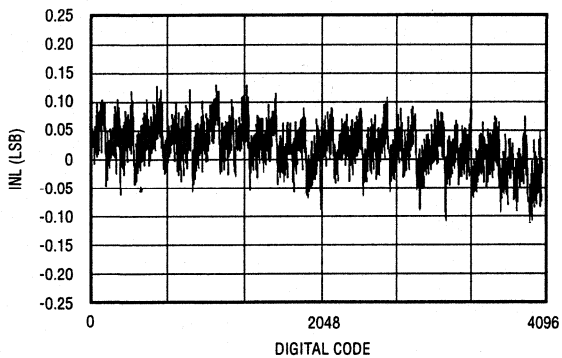
AVERAGE SUPPLY CURRENT vs. CONVERSION RATE



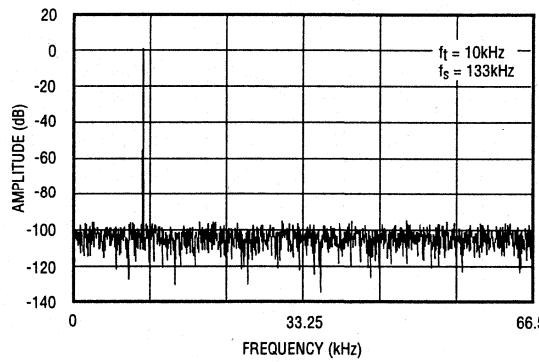
EFFECTIVE NUMBER OF BITS vs. INPUT FREQUENCY



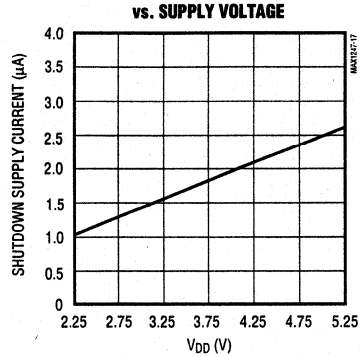
INTEGRAL NONLINEARITY



FFT PLOT



SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



Pin Description

PIN	NAME	FUNCTION
1, 9	V_{DD}	Positive Supply Voltage
2–5	CH0–CH3	Sampling Analog Inputs
6	COM	Ground reference for analog inputs. Sets zero-code voltage in single-ended mode. Must be stable to ±0.5LSB.
7	$\overline{SHDN}$	Three-Level Shutdown Input. Pulling $\overline{SHDN}$ low shuts the MAX1247 down; otherwise, the MAX1247 is fully operational. Letting $\overline{SHDN}$ float sets the internal clock frequency to 1.8MHz. Pulling $\overline{SHDN}$ high sets the internal clock frequency to 225kHz. See *Hardware Power-Down* section.
8	VREF	External Reference Voltage Input for analog-to-digital conversion.
10	AGND	Analog Ground
11	DGND	Digital Ground
12	DOUT	Serial Data Output. Data is clocked out at SCLK's falling edge. High impedance when $\overline{CS}$ is high.
13	SSTRB	Serial Strobe Output. In internal clock mode, SSTRB goes low when the MAX1247 begins the A/D conversion and goes high when the conversion is done. In external clock mode, SSTRB pulses high for one clock period before the MSB decision. High impedance when $\overline{CS}$ is high (external clock mode).
14	DIN	Serial Data Input. Data is clocked in at SCLK's rising edge.
15	$\overline{CS}$	Active-Low Chip Select. Data will not be clocked into DIN unless $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT is high impedance.
16	SCLK	Serial Clock Input. Clocks data in and out of serial interface. In external clock mode, SCLK also sets the conversion speed. (Duty cycle must be 40% to 60%.)

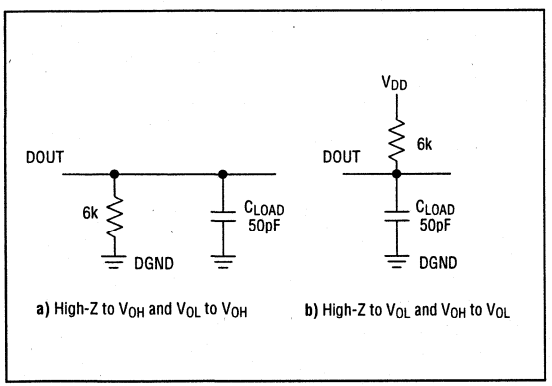


Figure 1. Load Circuits for Enable Time

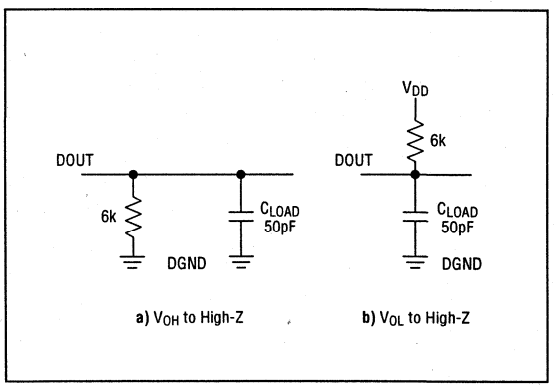


Figure 2. Load Circuits for Disable Time

+2.7V to +5.25V, Low-Power, 4-Channel, Serial 12-Bit ADC in QSOP-16

Detailed Description

The MAX1247 analog-to-digital converter (ADC) uses a successive-approximation conversion technique and input track/hold (T/H) circuitry to convert an analog signal to a 12-bit digital output. A flexible serial interface provides easy interface to microprocessors (µPs). No external hold capacitors are required. Figure 3 is a block diagram of the MAX1247.

Pseudo-Differential Input

The sampling architecture of the ADC's analog comparator is illustrated in the equivalent input circuit (Figure 4). In single-ended mode, IN+ is internally switched to CH0–CH3, and IN- is switched to COM. In differential mode, IN+ and IN- are selected from two pairs: CH0/CH1 and CH2/CH3. Configure the channels with Tables 2 and 3. Please note that the codes for CH0–CH3 in the MAX1247 correspond to the codes for CH2–CH5 in the MAX147.

In differential mode, IN- and IN+ are internally switched to either of the analog inputs. This configuration is pseudo-differential to the effect that only the signal at IN+ is sampled. The return side (IN-) must remain stable within ±0.5LSB (±0.1LSB for best results) with respect to AGND during a conversion. To accomplish this, connect a 0.1µF capacitor from IN- (the selected analog input) to AGND.

During the acquisition interval, the channel selected as the positive input (IN+) charges capacitor C_{HOLD}. The acquisition interval spans three SCLK cycles and ends on the falling SCLK edge after the last bit of the input control word has been entered. At the end of the acquisition interval, the T/H switch opens, retaining charge on C_{HOLD} as a sample of the signal at IN+.

The conversion interval begins with the input multiplexer switching C_{HOLD} from the positive input (IN+) to the negative input (IN-). In single-ended mode, IN- is simply COM. This unbalances node ZERO at the input of the comparator. The capacitive DAC adjusts during the remainder of the conversion cycle to restore node ZERO to 0V within the limits of 12-bit resolution. This action is equivalent to transferring a charge of 16pF x $[(V_{IN+}) - (V_{IN-})]$ from C_{HOLD} to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog input signal.

Track/Hold

The T/H enters its tracking mode on the falling clock edge after the fifth bit of the 8-bit control word has been shifted in. It enters its hold mode on the falling clock edge after the eighth bit of the control word has been shifted in. If the converter is set up for single-ended inputs, IN- is connected to COM, and the converter samples the "+" input. If the converter is set up for differential inputs, IN- connects to the "-" input, and the difference of |IN+ - IN-| is sampled. At the end of the conversion, the positive input connects back to IN+, and C_{HOLD} charges to the input signal.

The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens, and more time must be allowed between conversions. The acquisition time,

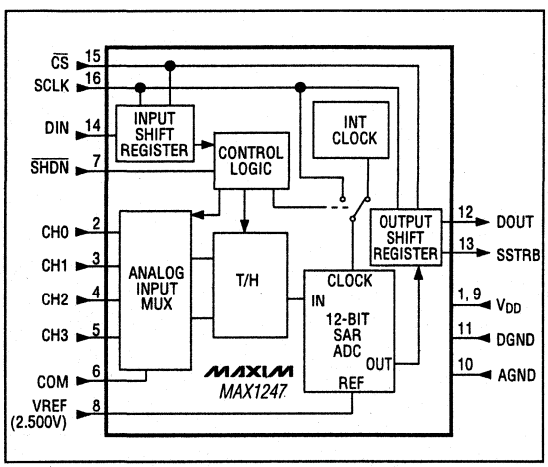


Figure 3. Block Diagram

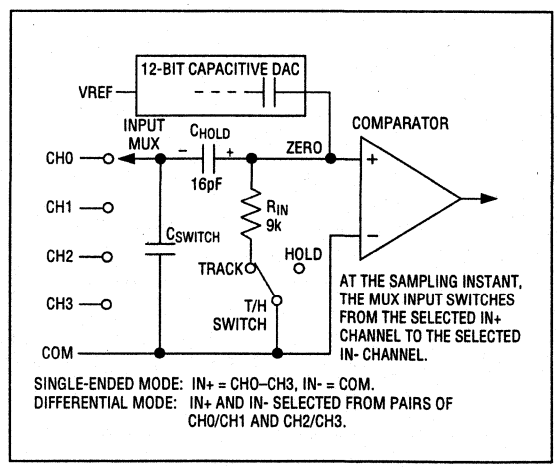


Figure 4. Equivalent Input Circuit

t_{ACQ}, is the maximum time the device takes to acquire the signal, and is also the minimum time needed for the signal to be acquired. It is calculated by:

$$t_{ACQ} = 9 \times (R_S + R_{IN}) \times 16pF$$

where R_{IN} = 9kΩ, R_S = the source impedance of the input signal, and t_{ACQ} is never less than 1.5µs. Note that source impedances below 1kΩ do not significantly affect the AC performance of the ADC.

Higher source impedances can be used if a 0.01µF capacitor is connected to the individual analog inputs. Note that the input capacitor forms an RC filter with the input source impedance, limiting the ADC's signal bandwidth.

Input Bandwidth

The ADC's input tracking circuitry has a 2.25MHz small-signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

Analog Input Protection

Internal protection diodes, which clamp the analog input to V_{DD} and AGND, allow the channel input pins to swing from AGND - 0.3V to V_{DD} + 0.3V without damage. However, for accurate conversions near full scale, the inputs must not exceed V_{DD} by more than 50mV or be lower than AGND by 50mV.

If the analog input exceeds 50mV beyond the supplies, do not forward bias the protection diodes of off channels over 2mA, as excessive current will degrade the conversion accuracy of the on channel.

How to Start a Conversion

A conversion is started by clocking a control byte into DIN. With $\overline{CS}$ low, each rising edge on SCLK clocks a bit from DIN into the MAX1247's internal shift register. After $\overline{CS}$ falls, the first arriving logic "1" bit defines the control byte's MSB. Until this first "start" bit arrives, any number of logic "0" bits can be clocked into DIN with no effect. Table 1 shows the control-byte format.

The MAX1247 is compatible with SPI™, QSPI™, and Microwire™ devices. For SPI, select the correct clock polarity and sampling edge in the SPI control registers: set CPOL = 0 and CPHA = 0. Microwire, SPI, and QSPI all transmit a byte and receive a byte at the same time. Using the *Typical Operating Circuit*, the simplest software interface requires only three 8-bit transfers to perform a conversion (one 8-bit transfer to configure the ADC, and two more 8-bit transfers to clock out the 12-bit conversion result). See Figure 16 for MAX1247 QSPI connections.

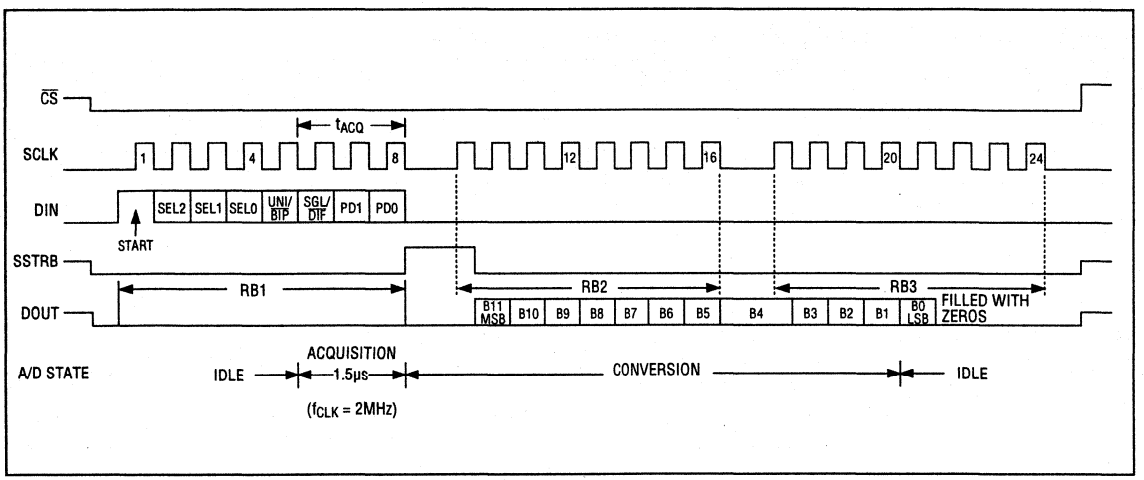


Figure 5. 24-Clock External-Clock-Mode Conversion Timing (Microwire and SPI Compatible, QSPI Compatible with $f_{CLK} \leq 2MHz$)

SPI and QSPI are trademarks of Motorola, Inc.
Microwire is a trademark of National Semiconductor Corp.

+2.7V to +5.25V, Low-Power, 4-Channel, Serial 12-Bit ADC in QSOP-16

Table 1. Control-Byte Format

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
START	SEL2	SEL1	SEL0	UNI/$\overline{BIP}$	SGL/$\overline{DIF}$	PD1	PD0

BIT	NAME	DESCRIPTION
7(MSB)	START	The first logic "1" bit after $\overline{CS}$ goes low defines the beginning of the control byte.
6 5 4	SEL2 SEL1 SEL0	These three bits select which of the four channels are used for the conversion (Tables 2 and 3).
3	UNI/$\overline{BIP}$	1 = unipolar, 0 = bipolar. Selects unipolar or bipolar conversion mode. In unipolar mode, an analog input signal from 0V to VREF can be converted; in bipolar mode, the signal can range from -VREF / 2 to +VREF / 2.
2	SGL/$\overline{DIF}$	1 = single ended, 0 = differential. Selects single-ended or differential conversions. In single-ended mode, input signal voltages are referred to COM. In differential mode, the voltage difference between two channels is measured (Tables 2 and 3).
1 0(LSB)	PD1 PD0	Selects clock and power-down modes. PD1 PD0 Mode 0 0 Power-down 0 1 Unassigned 1 0 Internal clock mode 1 1 External clock mode

Table 2. Channel Selection in Single-Ended Mode (SGL/$\overline{DIF}$ = 1)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	COM
0	0	1	+				–
1	0	1		+			–
0	1	0			+		–
1	1	0				+	–

Table 3. Channel Selection in Differential Mode (SGL/$\overline{DIF}$ = 0)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3
0	0	1	+	–		
0	1	0			+	–
1	0	1	–	+		
1	1	0			–	+

Simple Software Interface

Make sure the CPU's serial interface runs in master mode so the CPU generates the serial clock. Choose a clock frequency from 100kHz to 2MHz.

1) Set up the control byte for external clock mode and call it TB1. TB1 should be of the format: 1XXXXX11 binary, where the Xs denote the particular channel and conversion mode selected.
2) Use a general-purpose I/O line on the CPU to pull $\overline{CS}$ low.
3) Transmit TB1 and, simultaneously, receive a byte and call it RB1. Ignore RB1.
4) Transmit a byte of all zeros ($00 hex) and, simultaneously, receive byte RB2.
5) Transmit a byte of all zeros ($00 hex) and, simultaneously, receive byte RB3.
6) Pull $\overline{CS}$ high.

Figure 5 shows the timing for this sequence. Bytes RB2 and RB3 will contain the result of the conversion padded with one leading zero and three trailing zeros. The total conversion time is a function of the serial clock frequency and the amount of idle time between 8-bit transfers. To avoid excessive T/H droop, make sure the total conversion time does not exceed 120µs.

Digital Output

In unipolar input mode, the output is straight binary (Figure 13). For bipolar inputs, the output is two's complement (Figure 14). Data is clocked out at the falling edge of SCLK in MSB-first format.

Clock Modes

The MAX1247 may use either an external serial clock or the internal clock to perform the successive-approximation conversion. In both clock modes, the external clock shifts data in and out of the MAX1247. The T/H acquires the input signal as the last three bits of the control byte are clocked into DIN. Bits PD1 and PD0 of the control byte program the clock mode. Figures 6–9 show the timing characteristics common to both modes.

External Clock

In external clock mode, the external clock not only shifts data in and out, it also drives the analog-to-digital conversion steps. SSTRB pulses high for one clock period after the last bit of the control byte. Successive-approximation bit decisions are made and appear at DOUT on each of the next 12 SCLK falling edges (Figure 5). SSTRB and DOUT go into a high-impedance state when $\overline{CS}$ goes high; after the next $\overline{CS}$ falling edge, SSTRB will output a logic low. Figure 7 shows the SSTRB timing in external clock mode.

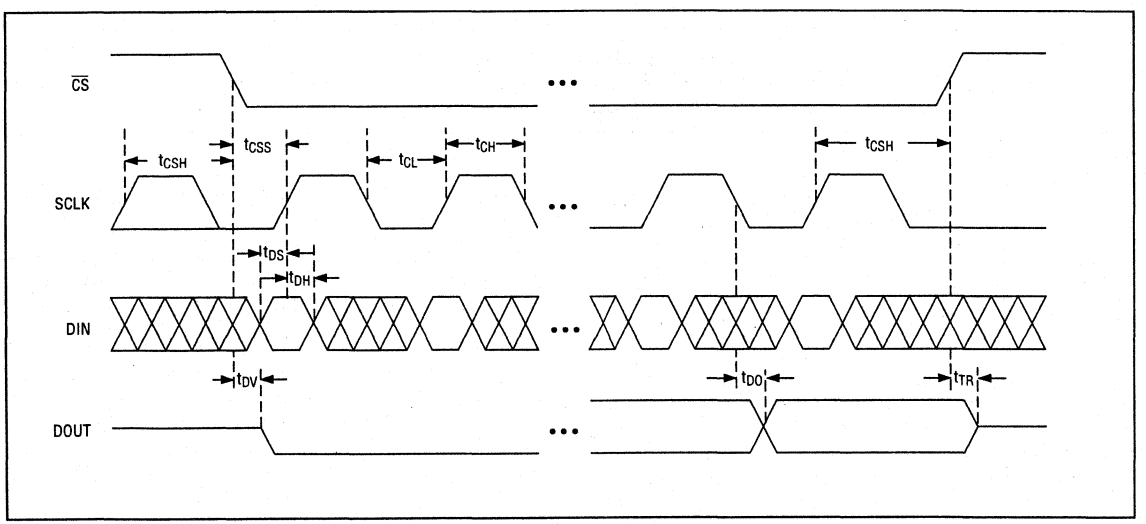


Figure 6. Detailed Serial-Interface Timing

+2.7V to +5.25V, Low-Power, 4-Channel, Serial 12-Bit ADC in QSOP-16

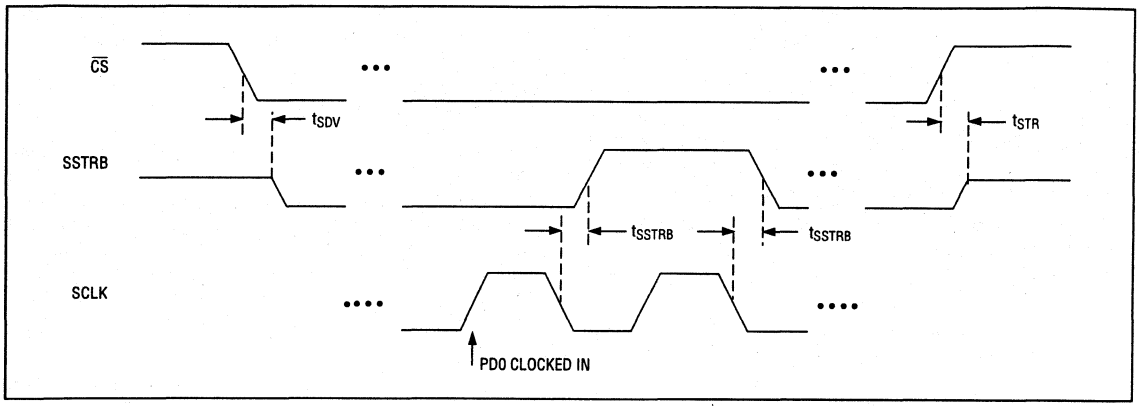


Figure 7. External-Clock-Mode SSTRB Detailed Timing

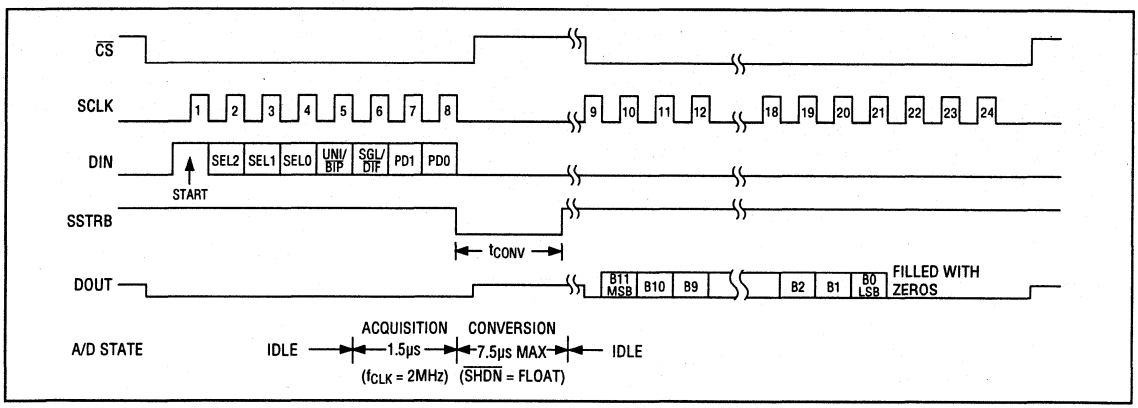


Figure 8. Internal Clock Mode Timing

The conversion must complete in some minimum time, or droop on the sample-and-hold capacitors may degrade conversion results. Use internal clock mode if the serial clock frequency is less than 100kHz, or if serial-clock interruptions could cause the conversion interval to exceed 120µs.

Internal Clock

In internal clock mode, the MAX1247 generates its own conversion clock internally. This frees the µP from the burden of running the SAR conversion clock and allows the conversion results to be read back at the processor's convenience, at any clock rate from 0MHz to 2MHz. SSTRB goes low at the start of the conversion and then goes high when the conversion is complete. SSTRB will be low for a maximum of 7.5µs (SHDN = FLOAT), during which time SCLK should remain low for best noise performance.

An internal register stores data when the conversion is in progress. SCLK clocks the data out of this register at any time after the conversion is complete. After SSTRB goes high, the next falling clock edge will produce the MSB of the conversion at DOUT, followed by the remaining bits in MSB-first format (Figure 8). CS does not need to be held low once a conversion is started. Pulling CS high prevents data from being clocked into the MAX1247 and three-states DOUT, but it does not adversely affect an internal clock-mode conversion already in progress. When internal clock mode is selected, SSTRB does not go into a high-impedance state when CS goes high.

Figure 9 shows the SSTRB timing in internal clock mode. In this mode, data can be shifted in and out of the MAX1247 at clock rates exceeding 2.0MHz, provided that the minimum acquisition time, t_{ACQ}, is kept above 1.5µs.

Data Framing

The falling edge of $\overline{CS}$ does **not** start a conversion on the MAX1247. The first logic high clocked into DIN is interpreted as a start bit and defines the first bit of the control byte. A conversion starts on the falling edge of SCLK, after the eighth bit of the control byte (the PD0 bit) is clocked into DIN. The start bit is defined as:

The first high bit clocked into DIN with $\overline{CS}$ low any time the converter is idle; e.g., after V_{DD} is applied.

OR

The first high bit clocked into DIN after bit 5 of a conversion in progress is clocked onto the DOUT pin.

If $\overline{CS}$ is toggled before the current conversion is complete, the next high bit clocked into DIN is recognized as a start bit; the current conversion is terminated, and a new one is started.

The fastest the MAX1247 can run with $\overline{CS}$ held low between conversions is 15 clocks per conversion.

Figure 10a shows the serial-interface timing necessary to perform a conversion every 15 SCLK cycles in external clock mode. If $\overline{CS}$ is tied low and SCLK is continuous, guarantee a start bit by first clocking in 16 zeros.

Most microcontrollers require that conversions occur in multiples of 8 SCLK clocks; 16 clocks per conversion will typically be the fastest that a microcontroller can drive the MAX1247. Figure 10b shows the serial-interface timing necessary to perform a conversion every 16 SCLK cycles in external clock mode.

Applications Information

Power-On Reset

When power is first applied, and if $\overline{SHDN}$ is not pulled low, internal power-on reset circuitry will activate the MAX1247 in internal clock mode, ready to convert with SSTRB = high. After the power supplies have been stabilized, the internal reset time is 10µs, and no conversions should be performed during this phase. SSTRB is high on power-up and, if $\overline{CS}$ is low, the first logical 1 on DIN will be interpreted as a start bit. Until a conversion takes place, DOUT will shift out zeros.

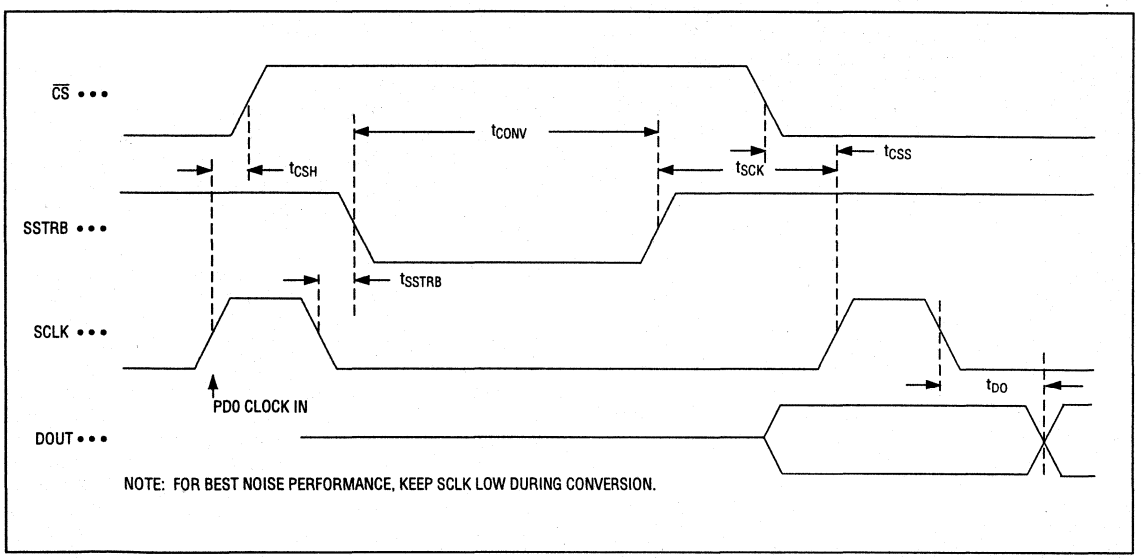


Figure 9. Internal Clock Mode SSTRB Detailed Timing

+2.7V to +5.25V, Low-Power, 4-Channel, Serial 12-Bit ADC in QSOP-16

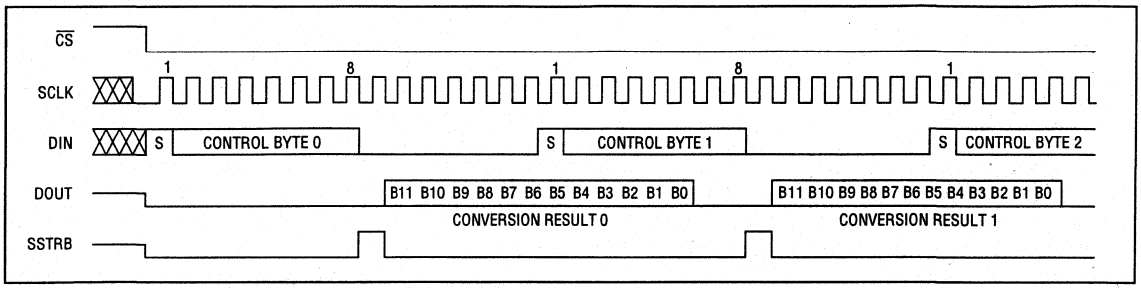


Figure 10a. External Clock Mode, 15 Clocks/Conversion Timing

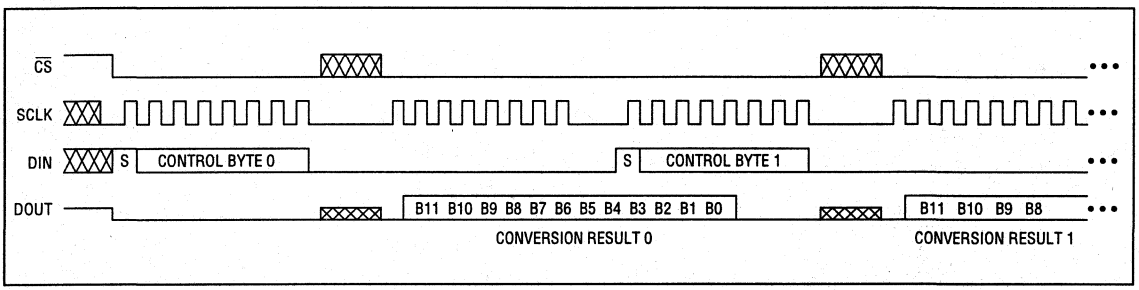


Figure 10b. External Clock Mode, 16 Clocks/Conversion Timing

Power-Down

The MAX1247's automatic power-down mode can save considerable power when operating at speeds below the maximum sampling rate. Figure 12 shows the average supply current as a function of the sampling rate. You can save power by placing the converter in a low-current shutdown state between conversions.

Select power-down via bits 1 and 0 of the DIN control byte with $\overline{SHDN}$ high (Tables 1 and 4). Pull $\overline{SHDN}$ low at any time to shut down the converter completely. $\overline{SHDN}$ overrides bits 1 and 0 of the control byte (Table 6).

Power-down mode turns off all chip functions that draw quiescent current, reducing I_{DD} typically to less than 5µA.

Figures 11a and 11b illustrate the various power-down sequences in both external and internal clock modes.

Software Power-Down

Software power-down is activated using bits PD1 and PD0 of the control byte. As shown in Table 4, PD1 and PD0 also specify the clock mode. When software shutdown is asserted, the ADC will continue to operate in the last specified clock mode until the conversion is complete. Then the ADC powers down into a low quiescent-current state. In internal clock mode, the interface remains active and conversion results may be clocked out after the MAX1247 has entered a software power-down.

The first logical 1 on DIN is interpreted as a start bit and powers up the MAX1247. No additional start-up time is required. Following the start bit, the data input word or control byte also determines clock mode and power-down states. For example, if the DIN word contains PD1 = 1, then the chip remains powered up. If PD0 = PD1 = 0, a power-down resumes after one conversion.

Hardware Power-Down

Pulling $\overline{SHDN}$ low places the converter in hardware power-down. Unlike the software power-down mode, the conversion is not completed; it stops coincidentally with $\overline{SHDN}$ being brought low. $\overline{SHDN}$ also controls the clock frequency in internal clock mode. Letting $\overline{SHDN}$ float sets the internal clock frequency to 1.8MHz. When returning to normal operation with $\overline{SHDN}$ floating, there is a t_{RC} delay of approximately $2M\Omega \times C_L$, where C_L is the capacitive loading on the $\overline{SHDN}$ pin. Pulling $\overline{SHDN}$ high sets the internal clock frequency to 225kHz. This feature eases the settling-time requirement for the reference voltage. The MAX1247 can be considered fully powered-up within 2µs of actively pulling $\overline{SHDN}$ high.

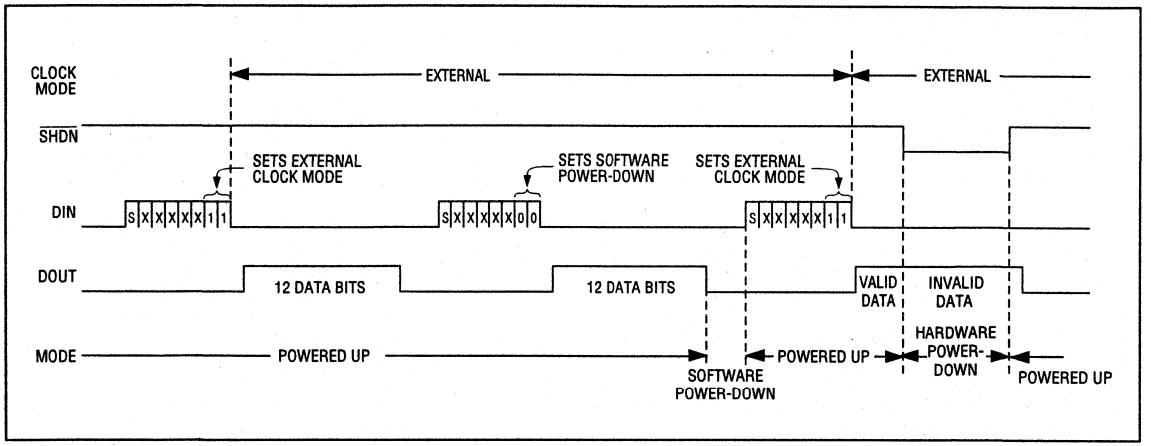


Figure 11a. Timing Diagram Power-Down Modes, External Clock

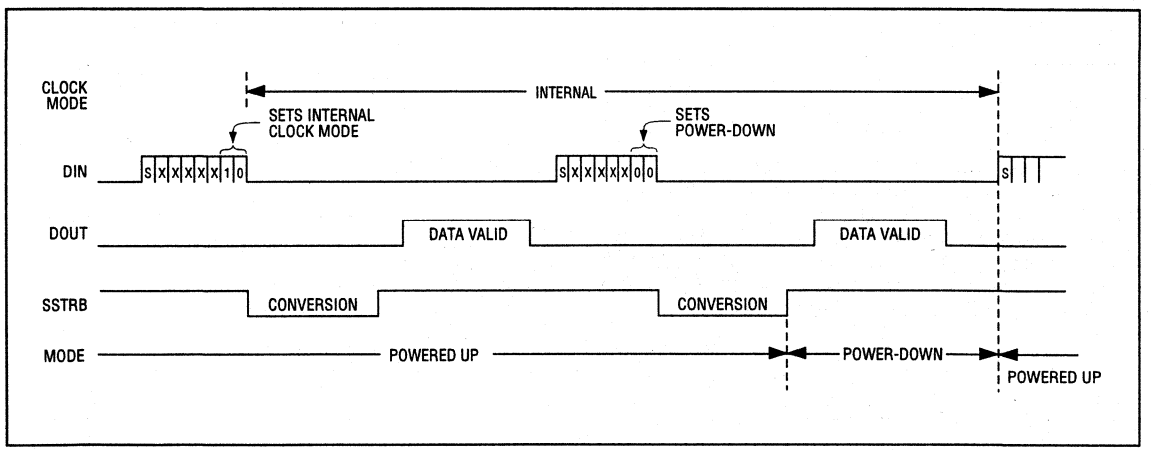


Figure 11b. Timing Diagram Power-Down Modes, Internal Clock

Table 4. Software Power-Down and Clock Mode

PD1	PD0	DEVICE MODE
1	1	External Clock
1	0	Internal Clock
0	1	Unassigned
0	0	Power-Down

Table 5. Hard-Wired Power-Down and Internal Clock Frequency

$\overline{SHDN}$ STATE	DEVICE MODE	INTERNAL CLOCK FREQUENCY
1	Enabled	225kHz
Floating	Enabled	1.8MHz
0	Power-Down	N/A

+2.7V to +5.25V, Low-Power, 4-Channel, Serial 12-Bit ADC in QSOP-16

Table 6. Full Scale and Zero Scale

UNIPOLAR MODE		BIPOLAR MODE		
Full Scale	Zero Scale	Positive Full Scale	Zero Scale	Negative Full Scale
VREF + COM	COM	VREF / 2 + COM	COM	-VREF / 2 + COM

External Reference

An external reference is required for the MAX1247. The reference voltage range is 1V to V_{DD}.

At VREF, the input impedance is a minimum of 18kΩ for DC currents. During a conversion, the reference must be able to deliver up to 250µA DC load current and have an output impedance of 10Ω or less. If the reference has higher output impedance or is noisy, bypass it close to the VREF pin with a 0.1µF capacitor.

Transfer Function

Table 6 shows the full-scale voltage ranges for unipolar and bipolar modes using a 2.5V reference.

The external reference must have a temperature coefficient of 4ppm/°C or less to achieve accuracy to within 1LSB over the commercial temperature range of 0°C to +70°C. See the MAX872 for a micropower 2.5V reference.

Figure 13 depicts the nominal, unipolar input/output (I/O) transfer function, and Figure 14 shows the bipolar input/output transfer function. Code transitions occur halfway between successive-integer LSB values. Output coding is binary, with 1LSB = 610µV (2.500V / 4096) for unipolar operation and 1LSB = 610µV [(2.500V / 2 - -2.500V / 2) / 4096] for bipolar operation.

Layout, Grounding, and Bypassing

For best performance, use printed circuit boards. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

Figure 15 shows the recommended system ground connections. Establish a single-point analog ground ("star" ground point) at AGND, separate from the logic ground. Connect all other analog grounds and DGND to the star ground. No other digital system ground should be connected to this ground. The ground return to the power supply for the star ground should be low impedance and as short as possible for noise-free operation.

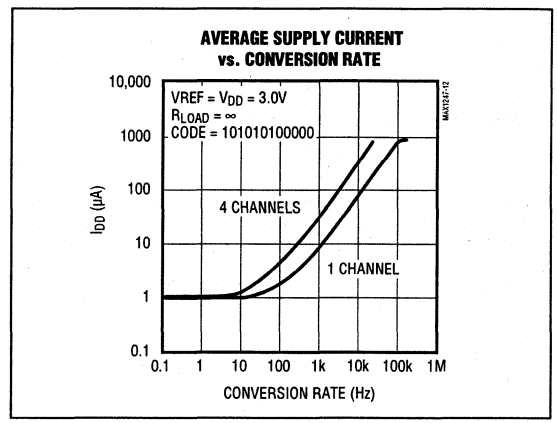


Figure 12. Average Supply Current vs. Conversion Rate

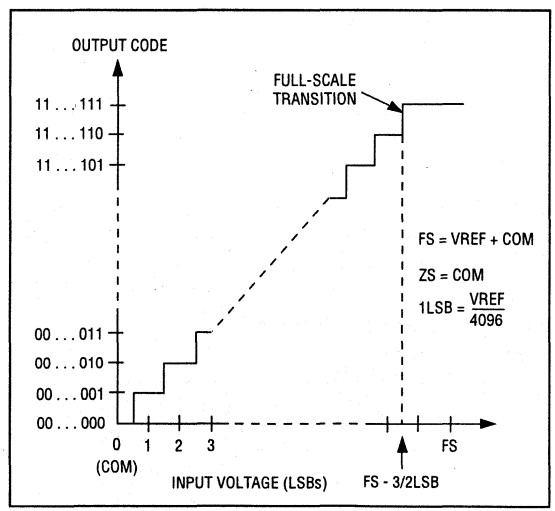


Figure 13. Unipolar Transfer Function, Full Scale (FS) = VREF + COM, Zero Scale (ZS) = COM

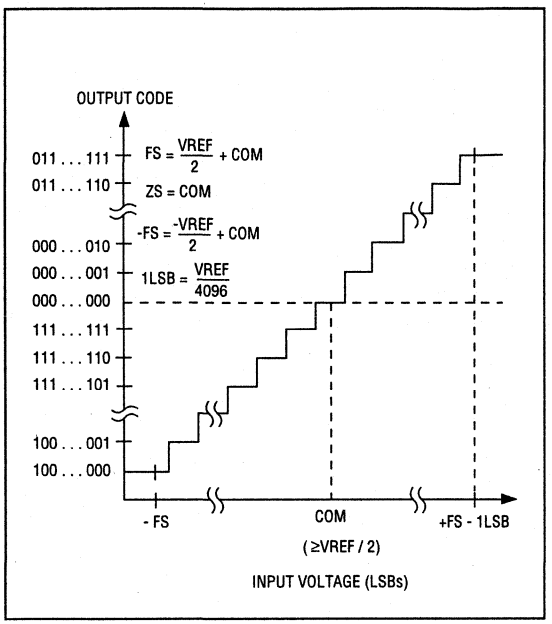


Figure 14. Bipolar Transfer Function, Full Scale (FS) = VREF / 2 + COM, Zero Scale (ZS) = COM

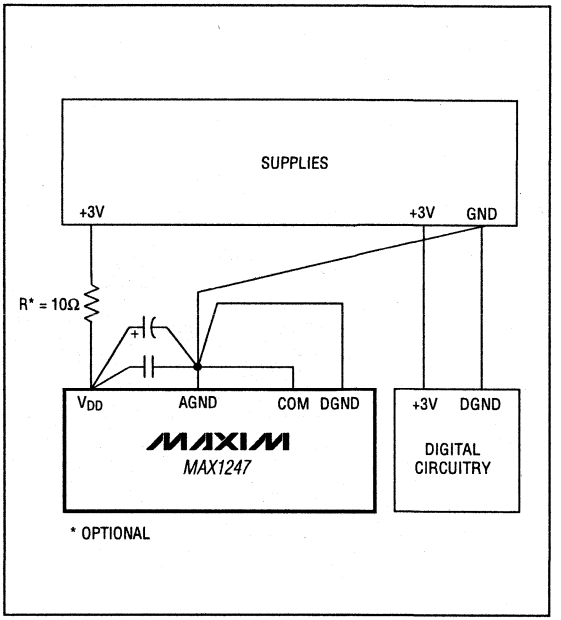


Figure 15. Power-Supply Grounding Connection

High-frequency noise in the V_{DD} power supply may affect the high-speed comparator in the ADC. Bypass the supply to the star ground with 0.1µF and 4.7µF capacitors close to pin 1 of the MAX1247. Minimize capacitor lead lengths for best supply-noise rejection. If the +3V power supply is very noisy, a 10Ω resistor can be connected as a lowpass filter (Figure 15).

+2.7V to +5.25V, Low-Power, 4-Channel, Serial 12-Bit ADC in QSOP-16

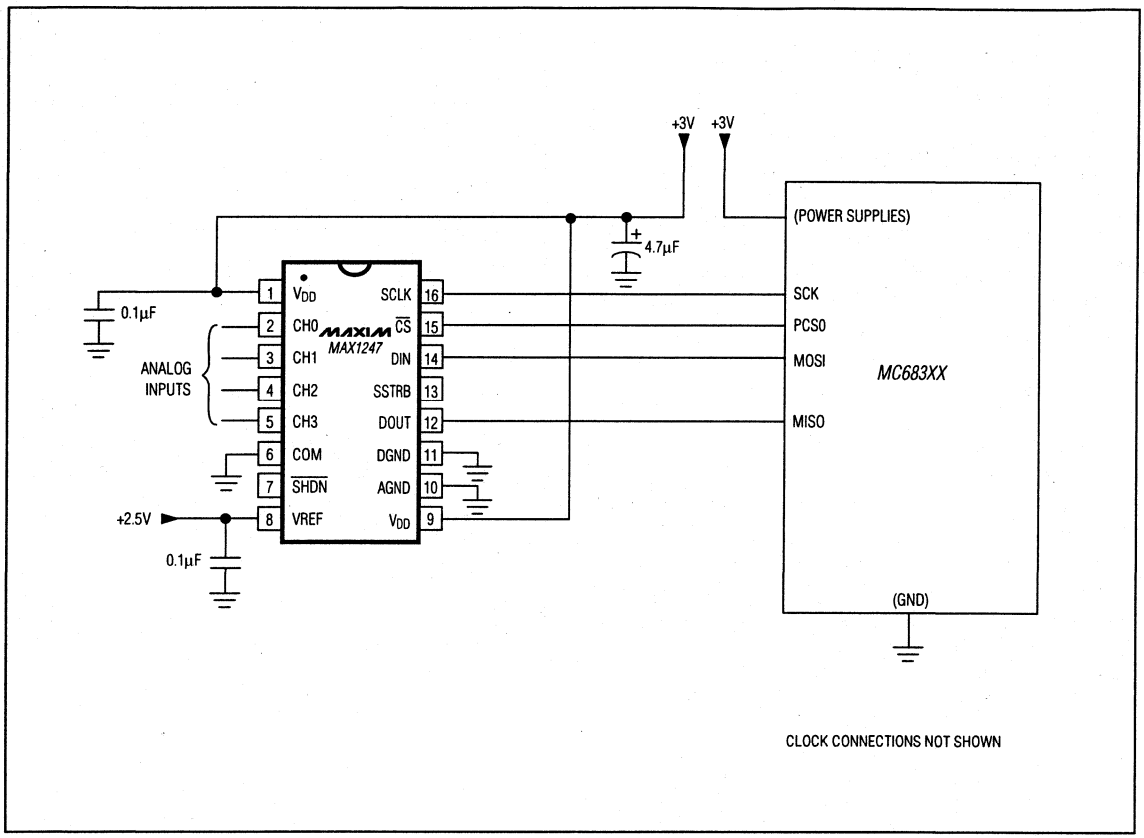


Figure 16. MAX1247 QSPI Connections

High-Speed Digital Interfacing with QSPI

The MAX1247 can interface with QSPI using the circuit in Figure 16 (f_{CLK} = 2.0MHz, CPOL = 0, CPHA = 0). This QSPI circuit can be programmed to do a conversion on each of the eight channels. The result is stored in memory without taxing the CPU, since QSPI incorporates its own micro-sequencer.

The MAX1247 is QSPI compatible up to its maximum external clock frequency of 2.0MHz.

TMS320LC3x-to-MAX1247 Interface

Figure 17 shows an application circuit to interface the MAX1247 to the TMS320 in external clock mode. The timing diagram for this interface circuit is shown in Figure 18.

Use the following steps to initiate a conversion in the MAX1247 and to read the results:

1) The TMS320 should be configured with CLKX (transmit clock) as an active-high output clock and CLKR (TMS320 receive clock) as an active-high input clock. CLKX and CLKR on the TMS320 are tied together with the MAX1247's SCLK input.
2) The MAX1247's $\overline{CS}$ pin is driven low by the TMS320's XF_ I/O port, to enable data to be clocked into the MAX1247's DIN.
3) An 8-bit word (1XXXXX11) should be written to the MAX1247 to initiate a conversion and place the device into external clock mode. Refer to Table 1 to select the proper XXXXX bit values for your specific application.
4) The MAX1247's SSTRB output is monitored via the TMS320's FSR input. A falling edge on the SSTRB output indicates that the conversion is in progress and data is ready to be received from the MAX1247.
5) The TMS320 reads in one data bit on each of the next 16 rising edges of SCLK. These data bits represent the 12-bit conversion result followed by four trailing bits, which should be ignored.
6) Pull $\overline{CS}$ high to disable the MAX1247 until the next conversion is initiated.

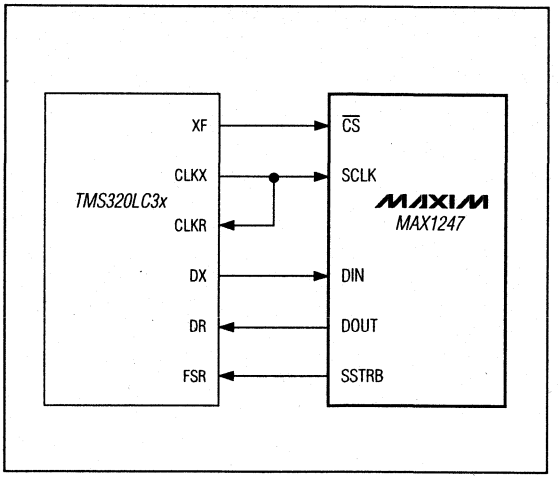


Figure 17. MAX1247-to-TMS320 Serial Interface

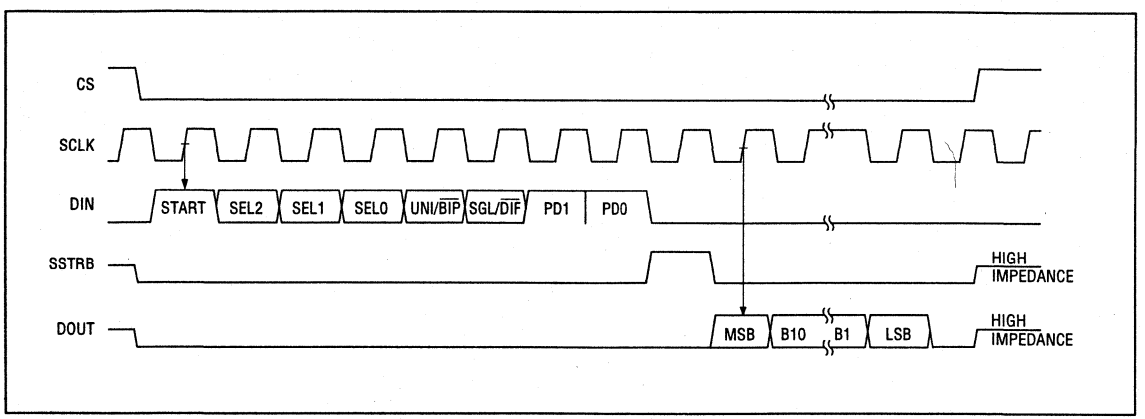


Figure 18. TMS320 Serial-Interface Timing Diagram

+2.7V to +5.25V, Low-Power, 4-Channel, Serial 12-Bit ADC in QSOP-16

_Ordering Information (continued)

PART†	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX1247AEPE	-40°C to +85°C	16 Plastic DIP	±1/2
MAX1247BEPE	-40°C to +85°C	16 Plastic DIP	±1
MAX1247AEEE	-40°C to +85°C	16 QSOP	±1/2
MAX1247BEEE	-40°C to +85°C	16 QSOP	±1
MAX1247AMJE	-55°C to +125°C	16 CERDIP*	±1/2
MAX1247BMJE	-55°C to +125°C	16 CERDIP*	±1

† *Contact factory for availability of alternate surface-mount packages.*

* *Contact factory for availability of CERDIP package, and for processing to MIL-STD-883B.*

Chip Information

TRANSISTOR COUNT: 2554

19-1072; Rev 0; 6/96

MAXIM

+2.7V to +5.25V, Low-Power, 4-Channel, Serial 10-Bit ADC in QSOP-16

General Description

The MAX1249 10-bit data-acquisition system combines a 4-channel multiplexer, high-bandwidth track/hold, and serial interface with high conversion speed and ultra-low power consumption. It operates from a single +2.7V to +5.25V supply, and its analog inputs are software configurable for unipolar/bipolar and single-ended/differential operation.

The 4-wire serial interface directly connects to SPI™, QSPI™, and Microwire™ devices without external logic. A serial strobe output allows direct connection to TMS320-family digital signal processors. The MAX1249 works with an external reference, and uses either the internal clock or an external serial-interface clock to perform successive-approximation analog-to-digital conversions.

This device provides a hard-wired $\overline{SHDN}$ pin and a software-selectable power-down and can be programmed to automatically shut down at the end of a conversion. Accessing the serial interface automatically powers up the MAX1249, and the quick turn-on time allows it to be shut down between all conversions. This technique can cut supply current to under 10µA at reduced sampling rates.

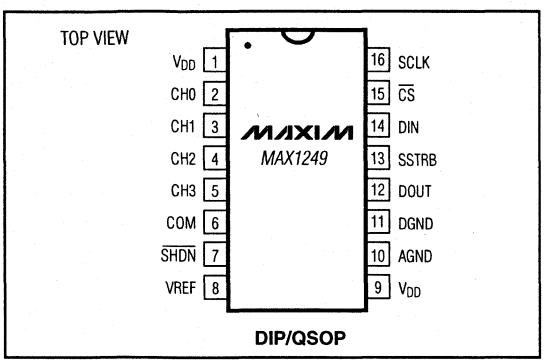
The MAX1249 is available in a 16-pin DIP and a very small QSOP that occupies the same board area as an 8-pin SO.

For an 8-channel version of this device, see the MAX148 data sheet. For a pin- and software-compatible 12-bit upgrade, see the MAX1247 data sheet.

Applications

Portable Data Logging
Medical Instruments
Pen Digitizers
Data Acquisition
Battery-Powered Instruments
System Supervision

Pin Configuration



Features

- 4-Channel Single-Ended or 2-Channel Differential Inputs
- Single +2.7V to +5.25V Operation
- Low Power: 0.9mA (133ksps, +3V supply)
  10µA (1ksps, +3V supply)
  1µA (power-down mode)
- Internal Track/Hold, 133kHz Sampling Rate
- SPI/QSPI/Microwire/TMS320-Compatible 4-Wire Serial Interface
- Software-Configurable Unipolar or Bipolar Inputs
- 16-Pin QSOP Package (same area as 8-pin SO)

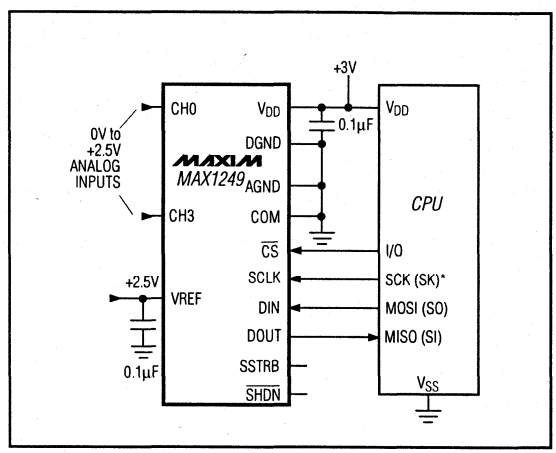
Ordering Information

PART†	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX1249ACPE	0°C to +70°C	16 Plastic DIP	±1/2
MAX1249BCPE	0°C to +70°C	16 Plastic DIP	±1
MAX1249ACEE	0°C to +70°C	16 QSOP	±1/2
MAX1249BCEE	0°C to +70°C	16 QSOP	±1

Ordering Information continued at end of data sheet.

† *Contact factory for availability of alternate surface-mount packages.*

Typical Operating Circuit



SPI and QSPI are registered trademarks of Motorola, Inc. Microwire is a registered trademark of National Semiconductor Corp.

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

+2.7V to +5.25V, Low-Power, 4-Channel, Serial 10-Bit ADC in QSOP-16

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND, DGND ..... -0.3V to +6V
AGND to DGND ..... -0.3V to +0.3V
CH0–CH7, COM to AGND, DGND ..... -0.3V to (V_{DD} + 0.3V)
VREF to AGND ..... -0.3V to (V_{DD} + 0.3V)
Digital Inputs to DGND ..... -0.3V to +6V
Digital Outputs to DGND ..... -0.3V to (V_{DD} + 0.3V)
Digital Output Sink Current 25mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
QSOP (derate 8.3mW/°C above +70°C) 667mW
CERDIP (derate 10.00mW/°C above +70°C) 800mW
Operating Temperature Ranges
MAX1249_C_E ..... 0°C to +70°C
MAX1249_E_E ..... -40°C to +85°C
MAX1249_MJE ..... -55°C to +125°C
Storage Temperature Range ..... -60°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +5.25V, COM = 0V, f_{CLK} = 2.0MHz, external clock (50% duty cycle), 15 clocks/conversion cycle (133ksps), VREF = 2.500V applied to VREF pin, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)						
Resolution			10			Bits
Relative Accuracy (Note 2)	INL	MAX1249A			±0.5	LSB
		MAX1249B			±1.0	
Differential Nonlinearity	DNL	No missing codes over temperature			±1	LSB
Offset Error		MAX1249A			±1	LSB
		MAX1249B			±2	
Gain Error (Note 3)		MAX1249A		0.125	±1	LSB
		MAX1249B			±2	
Gain Temperature Coefficient				±0.25		ppm/°C
Channel-to-Channel Offset Matching				±0.05		LSB
DYNAMIC SPECIFICATIONS (10kHz sine-wave input, 0Vp-p to 2.500Vp-p, 133ksps, 2.0MHz external clock, bipolar input mode)						
Signal-to-Noise + Distortion Ratio	SINAD			66		dB
Total Harmonic Distortion	THD	Up to the 5th harmonic		-70		dB
Spurious-Free Dynamic Range	SFDR			-70		dB
Channel-to-Channel Crosstalk		65kHz, 2.500Vp-p (Note 4)		-75		dB
Small-Signal Bandwidth		-3dB rolloff		2.25		MHz
Full-Power Bandwidth				1.0		MHz
CONVERSION RATE						
Conversion Time (Note 5)	t_{CONV}	Internal clock, $\overline{SHDN}$ = FLOAT	5.5		7.5	µs
		Internal clock, $\overline{SHDN}$ = V_{DD}	35		65	
		External clock = 2MHz, 12 clocks/conversion	6			
Track/Hold Acquisition Time	t_{ACQ}				1.5	µs
Aperture Delay				30		ns
Aperture Jitter				<50		ps
Internal Clock Frequency		$\overline{SHDN}$ = FLOAT		1.8		MHz
		$\overline{SHDN}$ = V_{DD}		0.225		
External Clock Frequency			0.1		2.0	MHz
		Data transfer only	0		2.0	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +5.25V, COM = 0V, f_{CLK} = 2.0MHz, external clock (50% duty cycle), 15 clocks/conversion cycle (133ksps), VREF = 2.500V applied to VREF pin, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG/COM INPUTS							
Input Voltage Range, Single-Ended and Differential (Note 6)		Unipolar, COM = 0V				0 to VREF	V
		Bipolar, COM = VREF / 2				±VREF / 2	
Multiplexer Leakage Current		On/off leakage current, V_{IN} = 0V or V_{DD}			±0.01	±1	µA
Input Capacitance		(Note 7)			16		pF
EXTERNAL REFERENCE							
VREF Input Voltage Range (Note 8)				1.0		V_{DD} + 50mV	V
VREF Input Current		VREF = 2.500V			100	150	µA
VREF Input Resistance				18	25		kΩ
Shutdown VREF Input Current					0.01	10	µA
DIGITAL INPUTS (DIN, SCLK, $\overline{CS}$, $\overline{SHDN}$)							
DIN, SCLK, $\overline{CS}$ Input High Voltage	V_{INH}	$V_{DD} \le 3.6V$		2.0			V
		$V_{DD} > 3.6V$		3.0			
DIN, SCLK, $\overline{CS}$ Input Low Voltage	V_{INL}					0.8	V
DIN, SCLK, $\overline{CS}$ Input Hysteresis	V_{HYST}				0.2		V
DIN, SCLK, $\overline{CS}$ Input Leakage	I_{IN}	V_{IN} = 0V or V_{DD}			±0.01	±1	µA
DIN, SCLK, $\overline{CS}$ Input Capacitance	C_{IN}	(Note 7)				15	pF
$\overline{SHDN}$ Input High Voltage	V_{INH}			V_{DD} - 0.4			V
$\overline{SHDN}$ Input Low Voltage	V_{INL}					0.4	V
$\overline{SHDN}$ Input Current	I_{IN}	$\overline{SHDN}$ = 0V or V_{DD}				±4.0	µA
$\overline{SHDN}$ Input Mid Voltage	V_{IM}			1.1		V_{DD} - 1.1	V
$\overline{SHDN}$ Voltage, Floating	V_{FLT}	$\overline{SHDN}$ = open			V_{DD} / 2		V
$\overline{SHDN}$ Maximum Allowed Leakage, Mid Input		$\overline{SHDN}$ = open				±100	nA
DIGITAL OUTPUTS (DOUT, SSTRB)							
Output Voltage Low	V_{OL}	I_{SINK} = 5mA				0.4	V
		I_{SINK} = 16mA				0.8	
Output Voltage High	V_{OH}	I_{SOURCE} = 0.5mA		V_{DD} - 0.5			V
Three-State Leakage Current	I_L	$\overline{CS}$ = V_{DD}			±0.01	±10	µA
Three-State Output Capacitance	C_{OUT}	$\overline{CS}$ = V_{DD} (Note 7)				15	pF
POWER REQUIREMENTS							
Positive Supply Voltage	V_{DD}			2.70		5.25	V
Positive Supply Current	I_{DD}	Operating mode, full-scale input	V_{DD} = 5.25V		1.8	2.5	mA
			V_{DD} = 3.6V		0.9	1.5	
		Power-down	V_{DD} = 5.25V		3.5	15	µA
			V_{DD} = 3.6V		1.2	10	
Supply Rejection (Note 9)	PSR	V_{DD} = 2.7V to 5.25V, full-scale input, external reference = 2.500V			±0.3		mV

+2.7V to +5.25V, Low-Power, 4-Channel, Serial 10-Bit ADC in QSOP-16

TIMING CHARACTERISTICS

(V_{DD} = +2.7V to +5.25V, COM = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Acquisition Time	t_{ACQ}			1.5			µs
DIN to SCLK Setup	t_{DS}			100			ns
DIN to SCLK Hold	t_{DH}					0	ns
SCLK Fall to Output Data Valid	t_{DO}	Figure 1	MAX1249_C/E	20		200	ns
			MAX1249_M	20		240	
$\overline{CS}$ Fall to Output Enable	t_{DV}	Figure 1				240	ns
$\overline{CS}$ Rise to Output Disable	t_{TR}	Figure 2				240	ns
$\overline{CS}$ to SCLK Rise Setup	t_{CSS}			100			ns
$\overline{CS}$ to SCLK Rise Hold	t_{CSH}			0			ns
SCLK Pulse Width High	t_{CH}			200			ns
SCLK Pulse Width Low	t_{CL}			200			ns
SCLK Fall to SSTRB	t_{SSTRB}	Figure 1				240	ns
$\overline{CS}$ Fall to SSTRB Output Enable	t_{SDV}	External clock mode only, Figure 1				240	ns
$\overline{CS}$ Rise to SSTRB Output Disable	t_{STR}	External clock mode only, Figure 2				240	ns
SSTRB Rise to SCLK Rise	t_{SCK}	Internal clock mode only (Note 7)		0			ns

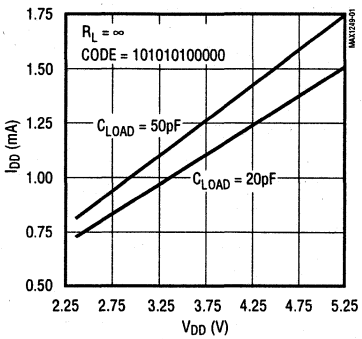
Note 1: Tested at V_{DD} = 2.7V; COM = 0V; unipolar single-ended input mode.
Note 2: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range has been calibrated.
Note 3: External reference (VREF = +2.500V), offset nulled.
Note 4: Ground "on" channel; sine wave applied to all "off" channels.
Note 5: Conversion time defined as the number of clock cycles multiplied by the clock period; clock has 50% duty cycle.
Note 6: The common-mode range for the analog inputs is from AGND to V_{DD}.
Note 7: Guaranteed by design. Not subject to production testing.
Note 8: ADC performance is limited by the converter's noise floor, typically 300µVp-p.
Note 9: Measured as $|V_{FS}(2.7V) - V_{FS}(5.25V)|$.

+2.7V to +5.25V, Low-Power, 4-Channel, Serial 10-Bit ADC in QSOP-16

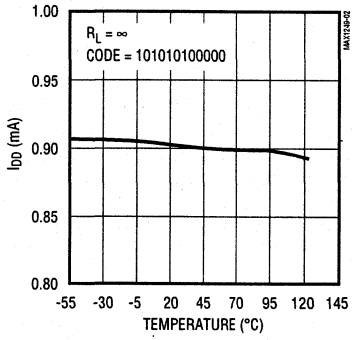
Typical Operating Characteristics

(V_{DD} = 3.0V, VREF = 2.500V, f_{CLK} = 2.0MHz, C_{LOAD} = 20pF, T_A = +25°C, unless otherwise noted.)

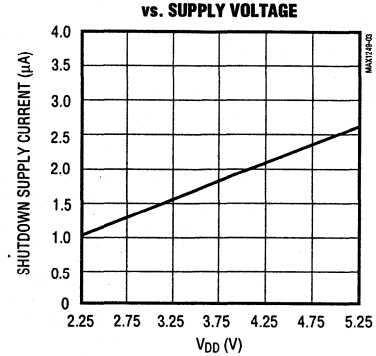
SUPPLY CURRENT vs. SUPPLY VOLTAGE



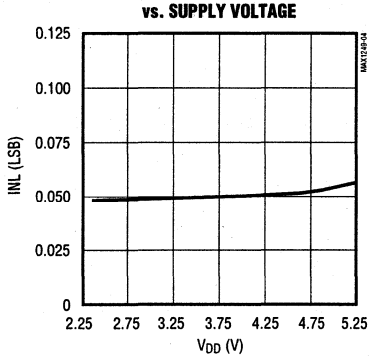
SUPPLY CURRENT vs. TEMPERATURE



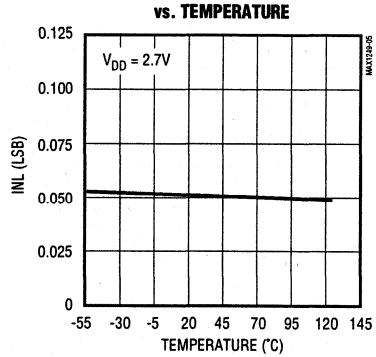
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



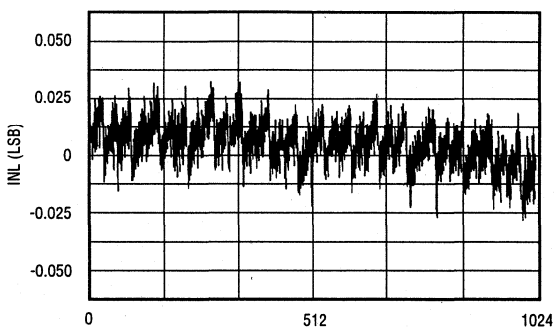
INTEGRAL NONLINEARITY vs. SUPPLY VOLTAGE



INTEGRAL NONLINEARITY vs. TEMPERATURE



INTEGRAL NONLINEARITY



+2.7V to +5.25V, Low-Power, 4-Channel, Serial 10-Bit ADC in QSOP-16

Pin Description

PIN	NAME	FUNCTION
1, 9	V_{DD}	Positive Supply Voltage
2–5	CH0–CH3	Sampling Analog Inputs
6	COM	Ground reference for analog inputs. Sets zero-code voltage in single-ended mode. Must be stable to ±0.5LSB.
7	$\overline{SHDN}$	Three-Level Shutdown Input. Pulling $\overline{SHDN}$ low shuts the MAX1249 down; otherwise, the MAX1249 is fully operational. Letting $\overline{SHDN}$ float sets the internal clock frequency to 1.8MHz. Pulling $\overline{SHDN}$ high sets the internal clock frequency to 225kHz. See *Hardware Power-Down* section.
8	VREF	External Reference Voltage Input for analog-to-digital conversion.
10	AGND	Analog Ground
11	DGND	Digital Ground
12	DOUT	Serial Data Output. Data is clocked out at SCLK's falling edge. High impedance when $\overline{CS}$ is high.
13	SSTRB	Serial Strobe Output. In internal clock mode, SSTRB goes low when the MAX1249 begins the A/D conversion and goes high when the conversion is done. In external clock mode, SSTRB pulses high for one clock period before the MSB decision. High impedance when $\overline{CS}$ is high (external clock mode).
14	DIN	Serial Data Input. Data is clocked in at SCLK's rising edge.
15	$\overline{CS}$	Active-Low Chip Select. Data will not be clocked into DIN unless $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT is high impedance.
16	SCLK	Serial Clock Input. Clocks data in and out of serial interface. In external clock mode, SCLK also sets the conversion speed. (Duty cycle must be 40% to 60%.)

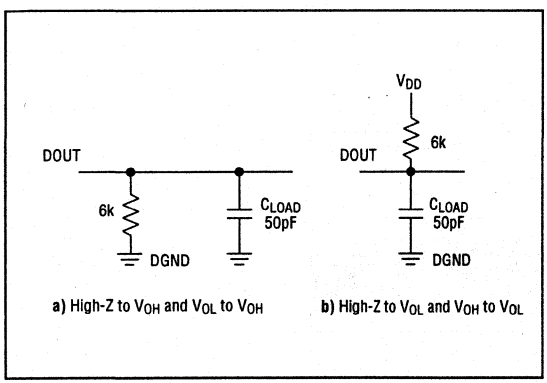


Figure 1. Load Circuits for Enable Time

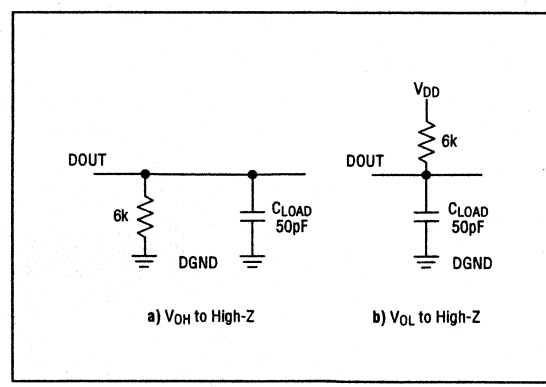


Figure 2. Load Circuits for Disable Time

+2.7V to +5.25V, Low-Power, 4-Channel, Serial 10-Bit ADC in QSOP-16

Detailed Description

The MAX1249 analog-to-digital converter (ADC) uses a successive-approximation conversion technique and input track/hold (T/H) circuitry to convert an analog signal to a 10-bit digital output. A flexible serial interface provides easy interface to microprocessors (µPs). No external hold capacitors are required. Figure 3 is a block diagram of the MAX1249.

Pseudo-Differential Input

The sampling architecture of the ADC's analog comparator is illustrated in the equivalent input circuit (Figure 4). In single-ended mode, IN+ is internally switched to CH0–CH3, and IN- is switched to COM. In differential mode, IN+ and IN- are selected from two pairs: CH0/CH1 and CH2/CH3. Configure the channels with Tables 2 and 3. Please note that the codes for CH0–CH3 in the MAX1249 correspond to the codes for CH2–CH5 in the MAX148.

In differential mode, IN- and IN+ are internally switched to either of the analog inputs. This configuration is pseudo-differential to the effect that only the signal at IN+ is sampled. The return side (IN-) must remain stable within ±0.5LSB (±0.1LSB for best results) with respect to AGND during a conversion. To accomplish this, connect a 0.1µF capacitor from IN- (the selected analog input) to AGND.

During the acquisition interval, the channel selected as the positive input (IN+) charges capacitor C_{HOLD}. The acquisition interval spans three SCLK cycles and ends on the falling SCLK edge after the last bit of the input control word has been entered. At the end of the acquisition interval, the T/H switch opens, retaining charge on C_{HOLD} as a sample of the signal at IN+.

The conversion interval begins with the input multiplexer switching C_{HOLD} from the positive input (IN+) to the negative input (IN-). In single-ended mode, IN- is simply COM. This unbalances node ZERO at the comparator's input. The capacitive DAC adjusts during the remainder of the conversion cycle to restore node ZERO to 0V within the limits of 10-bit resolution. This action is equivalent to transferring a charge of 16pF x $[(V_{IN+}) - (V_{IN-})]$ from C_{HOLD} to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog input signal.

Track/Hold

The T/H enters its tracking mode on the falling clock edge after the fifth bit of the 8-bit control word has been shifted in. It enters its hold mode on the falling clock edge after the eighth bit of the control word has been shifted in. If the converter is set up for single-ended inputs, IN- is connected to COM, and the converter samples the "+" input. If the converter is set up for differential inputs, IN- connects to the "-" input, and the difference of |IN+ - IN-| is sampled. At the end of the conversion, the positive input connects back to IN+, and C_{HOLD} charges to the input signal.

The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens, and more time must be allowed between conversions. The acquisition time,

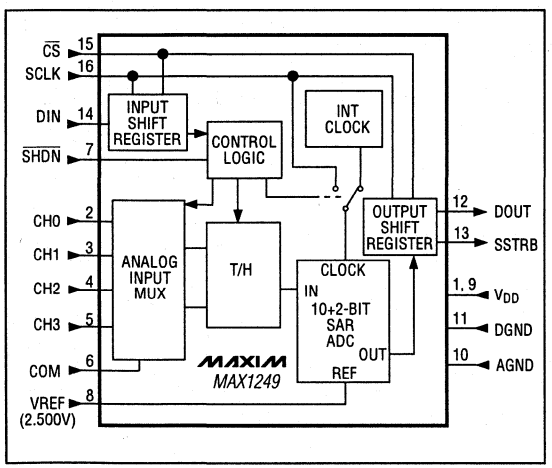


Figure 3. Block Diagram

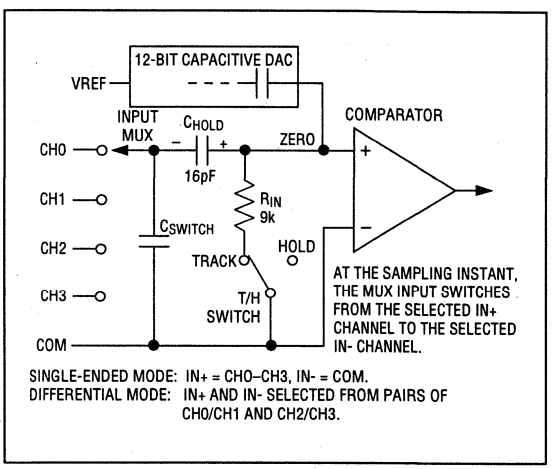


Figure 4. Equivalent Input Circuit

+2.7V to +5.25V, Low-Power, 4-Channel, Serial 10-Bit ADC in QSOP-16

t_{ACQ}, is the maximum time the device takes to acquire the signal, and is also the minimum time needed for the signal to be acquired. It is calculated by:

$$t_{ACQ} = 7 \times (R_S + R_{IN}) \times 16pF$$

where R_{IN} = 9kΩ, R_S = the source impedance of the input signal, and t_{ACQ} is never less than 1.5µs. Note that source impedances below 4kΩ do not significantly affect the ADC's AC performance.

Higher source impedances can be used if a 0.01µF capacitor is connected to the individual analog inputs. Note that the input capacitor forms an RC filter with the input source impedance, limiting the ADC's signal bandwidth.

Input Bandwidth

The ADC's input tracking circuitry has a 2.25MHz small-signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

Analog Input Protection

Internal protection diodes, which clamp the analog input to V_{DD} and AGND, allow the channel input pins to swing from AGND - 0.3V to V_{DD} + 0.3V without damage. However, for accurate conversions near full scale, the inputs must not exceed V_{DD} by more than 50mV or be lower than AGND by 50mV.

If the analog input exceeds 50mV beyond the supplies, do not forward bias the protection diodes of off channels over 2mA, as excessive current will degrade the conversion accuracy of the on channel.

How to Start a Conversion

A conversion is started by clocking a control byte into DIN. With $\overline{CS}$ low, each rising edge on SCLK clocks a bit from DIN into the MAX1249's internal shift register. After $\overline{CS}$ falls, the first arriving logic "1" bit defines the control byte's MSB. Until this first "start" bit arrives, any number of logic "0" bits can be clocked into DIN with no effect. Table 1 shows the control-byte format.

The MAX1249 is compatible with SPI™, QSPI™, and Microwire™ devices. For SPI, select the correct clock polarity and sampling edge in the SPI control registers: set CPOL = 0 and CPHA = 0. Microwire, SPI, and QSPI all transmit a byte and receive a byte at the same time. Using the *Typical Operating Circuit*, the simplest software interface requires only three 8-bit transfers to perform a conversion (one 8-bit transfer to configure the ADC, and two more 8-bit transfers to clock out the 10-bit conversion result). See Figure 16 for MAX1249 QSPI connections.

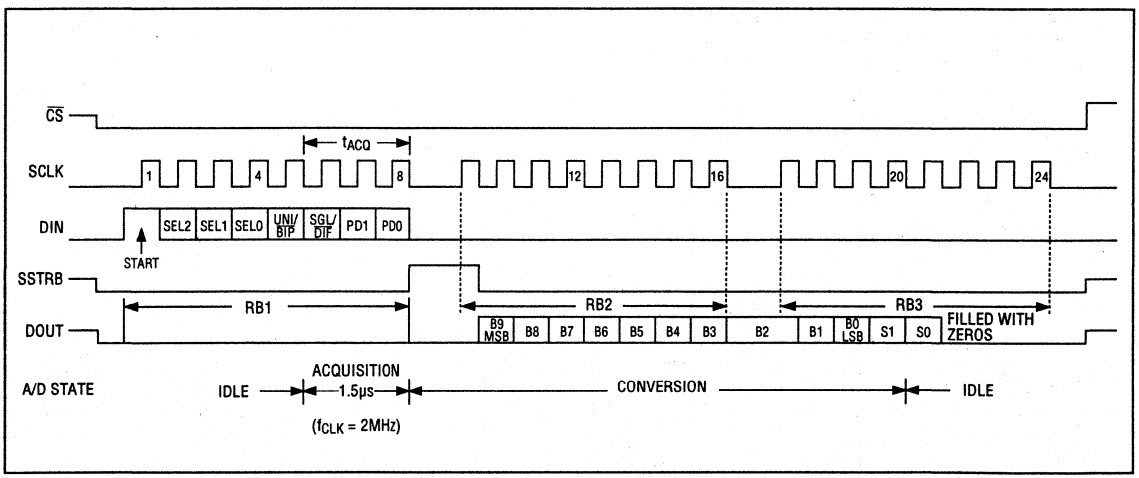


Figure 5. 24-Clock External-Clock-Mode Conversion Timing (Microwire and SPI Compatible, QSPI Compatible with $f_{CLK} \leq 2MHz$)

SPI and QSPI are trademarks of Motorola, Inc.
Microwire is a trademark of National Semiconductor Corp.

Table 1. Control-Byte Format

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
START	SEL2	SEL1	SEL0	UNI/$\overline{BIP}$	SGL/$\overline{DIF}$	PD1	PD0

BIT	NAME	DESCRIPTION
7(MSB)	START	The first logic "1" bit after $\overline{CS}$ goes low defines the beginning of the control byte.
6 5 4	SEL2 SEL1 SEL0	These three bits select which of the four channels are used for the conversion (Tables 2 and 3).
3	UNI/$\overline{BIP}$	1 = unipolar, 0 = bipolar. Selects unipolar or bipolar conversion mode. In unipolar mode, an analog input signal from 0V to VREF can be converted; in bipolar mode, the signal can range from -VREF / 2 to +VREF / 2.
2	SGL/$\overline{DIF}$	1 = single ended, 0 = differential. Selects single-ended or differential conversions. In single-ended mode, input signal voltages are referred to COM. In differential mode, the voltage difference between two channels is measured (Tables 2 and 3).
1 0(LSB)	PD1 PD0	Selects clock and power-down modes. PD1 PD0 Mode 0 0 Power-down 0 1 Unassigned 1 0 Internal clock mode 1 1 External clock mode

Table 2. Channel Selection in Single-Ended Mode (SGL/$\overline{DIF}$ = 1)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	COM
0	0	1	+				-
1	0	1		+			-
0	1	0			+		-
1	1	0				+	-

Table 3. Channel Selection in Differential Mode (SGL/$\overline{DIF}$ = 0)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3
0	0	1	+	-		
0	1	0			+	-
1	0	1	-	+		
1	1	0			-	+

+2.7V to +5.25V, Low-Power, 4-Channel, Serial 10-Bit ADC in QSOP-16

Simple Software Interface

Make sure the CPU's serial interface runs in master mode so the CPU generates the serial clock. Choose a clock frequency from 100kHz to 2MHz.

1) Set up the control byte for external clock mode and call it TB1. TB1 should be of the format: 1XXXXX11 binary, where the Xs denote the particular channel and conversion mode selected.
2) Use a general-purpose I/O line on the CPU to pull $\overline{CS}$ low.
3) Transmit TB1 and, simultaneously, receive a byte and call it RB1. Ignore RB1.
4) Transmit a byte of all zeros ($00 hex) and, simultaneously, receive byte RB2.
5) Transmit a byte of all zeros ($00 hex) and, simultaneously, receive byte RB3.
6) Pull $\overline{CS}$ high.

Figure 5 shows the timing for this sequence. Bytes RB2 and RB3 will contain the result of the conversion padded with one leading zero and three trailing zeros. The total conversion time is a function of the serial clock frequency and the amount of idle time between 8-bit transfers. To avoid excessive T/H droop, make sure the total conversion time does not exceed 120µs.

Digital Output

In unipolar input mode, the output is straight binary (Figure 13). For bipolar inputs, the output is two's complement (Figure 14). Data is clocked out at the falling edge of SCLK in MSB-first format.

Clock Modes

The MAX1249 may use either an external serial clock or the internal clock to perform successive-approximation conversion. In both clock modes, the external clock shifts data in and out of the MAX1249. The T/H acquires the input signal as the last three bits of the control byte are clocked into DIN. Bits PD1 and PD0 of the control byte program the clock mode. Figures 6–9 show the timing characteristics common to both modes.

External Clock

In external clock mode, the external clock not only shifts data in and out, it also drives the analog-to-digital conversion steps. SSTRB pulses high for one clock period after the last bit of the control byte. Successive-approximation bit decisions are made and appear at DOUT on each of the next 12 SCLK falling edges (Figure 5). SSTRB and DOUT go into a high-impedance state when $\overline{CS}$ goes high; after the next $\overline{CS}$ falling edge, SSTRB will output a logic low. Figure 7 shows the SSTRB timing in external clock mode.

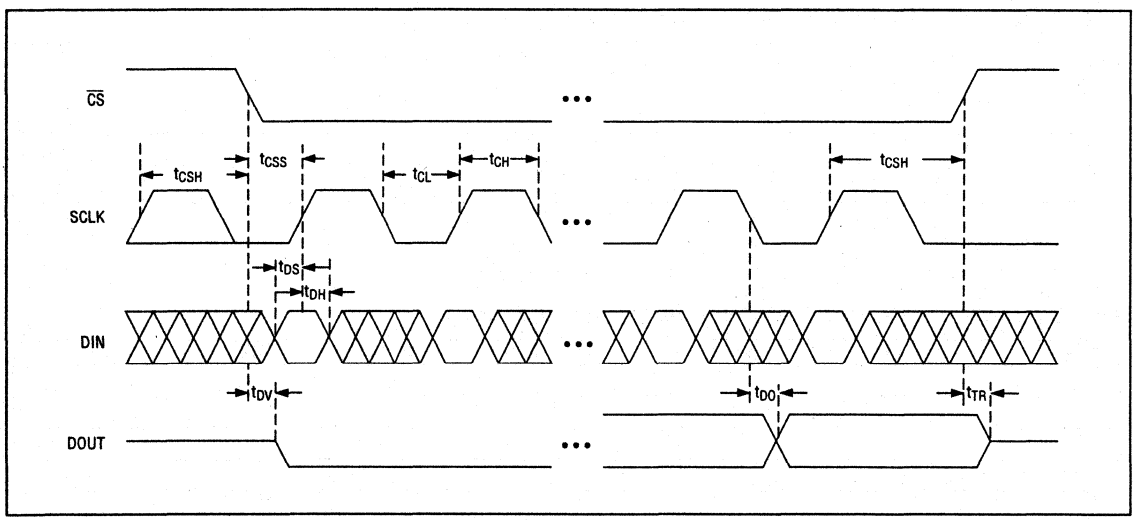


Figure 6. Detailed Serial-Interface Timing

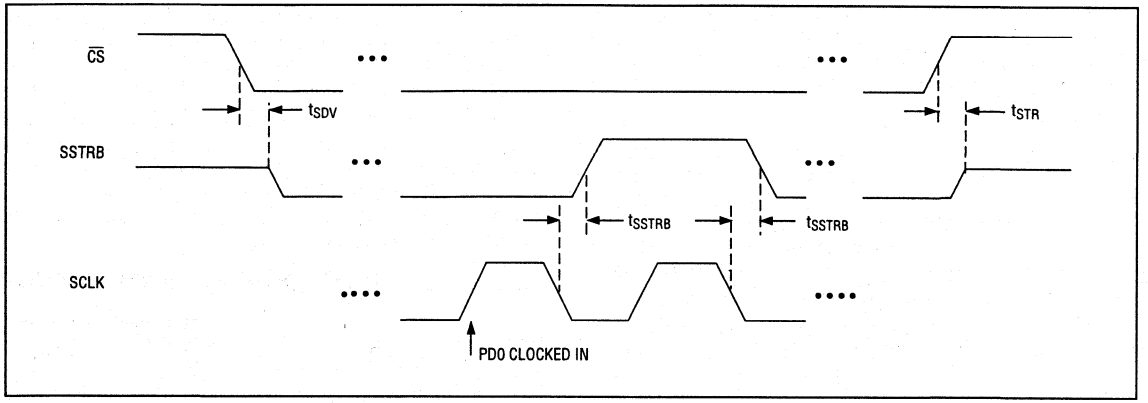


Figure 7. External-Clock-Mode SSTRB Detailed Timing

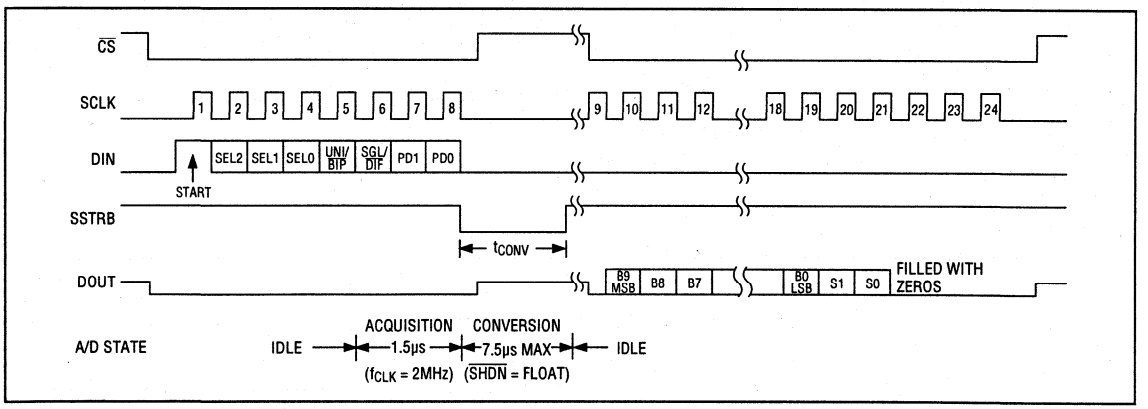


Figure 8. Internal Clock Mode Timing

The conversion must complete in some minimum time, or droop on the sample-and-hold capacitors may degrade conversion results. Use internal clock mode if the serial clock frequency is less than 100kHz, or if serial-clock interruptions could cause the conversion interval to exceed 120µs.

Internal Clock

In internal clock mode, the MAX1249 generates its own conversion clock internally. This frees the µP from the burden of running the SAR conversion clock and allows the conversion results to be read back at the processor's convenience, at any clock rate from 0MHz to 2MHz. SSTRB goes low at the start of the conversion and then goes high when the conversion is complete. SSTRB will be low for a maximum of 7.5µs ($\overline{SHDN}$ = FLOAT), during which time SCLK should remain low for best noise performance.

An internal register stores data when the conversion is in progress. SCLK clocks the data out of this register at any time after the conversion is complete. After SSTRB goes high, the next falling clock edge will produce the MSB of the conversion at DOUT, followed by the remaining bits in MSB-first format (Figure 8). $\overline{CS}$ does not need to be held low once a conversion is started. Pulling $\overline{CS}$ high prevents data from being clocked into the MAX1249 and three-states DOUT, but it does not adversely affect an internal clock-mode conversion already in progress. When internal clock mode is selected, SSTRB does not go into a high-impedance state when $\overline{CS}$ goes high.

+2.7V to +5.25V, Low-Power, 4-Channel, Serial 10-Bit ADC in QSOP-16

Figure 9 shows the SSTRB timing in internal clock mode. In this mode, data can be shifted in and out of the MAX1249 at clock rates exceeding 2.0MHz, provided that the minimum acquisition time, t_{ACQ}, is kept above 1.5µs.

Data Framing

The falling edge of $\overline{CS}$ does **not** start a conversion on the MAX1249. The first logic high clocked into DIN is interpreted as a start bit and defines the first bit of the control byte. A conversion starts on the falling edge of SCLK, after the eighth bit of the control byte (the PD0 bit) is clocked into DIN. The start bit is defined as:

The first high bit clocked into DIN with $\overline{CS}$ low any time the converter is idle; e.g., after V_{DD} is applied.

OR

The first high bit clocked into DIN after bit 3 of a conversion in progress is clocked onto the DOUT pin.

If $\overline{CS}$ is toggled before the current conversion is complete, the next high bit clocked into DIN is recognized as a start bit; the current conversion is terminated, and a new one is started.

The fastest the MAX1249 can run with $\overline{CS}$ held low between conversions is 15 clocks per conversion.

Figure 10a shows the serial-interface timing necessary to perform a conversion every 15 SCLK cycles in external clock mode. If $\overline{CS}$ is tied low and SCLK is continuous, guarantee a start bit by first clocking in 16 zeros.

Most microcontrollers require that conversions occur in multiples of 8 SCLK clocks; 16 clocks per conversion will typically be the fastest that a microcontroller can drive the MAX1249. Figure 10b shows the serial-interface timing necessary to perform a conversion every 16 SCLK cycles in external clock mode.

Applications Information

Power-On Reset

When power is first applied, and if $\overline{SHDN}$ is not pulled low, internal power-on reset circuitry will activate the MAX1249 in internal clock mode, ready to convert with SSTRB = high. After the power supplies have been stabilized, the internal reset time is 10µs, and no conversions should be performed during this phase. SSTRB is high on power-up and, if $\overline{CS}$ is low, the first logical 1 on DIN will be interpreted as a start bit. Until a conversion takes place, DOUT will shift out zeros.

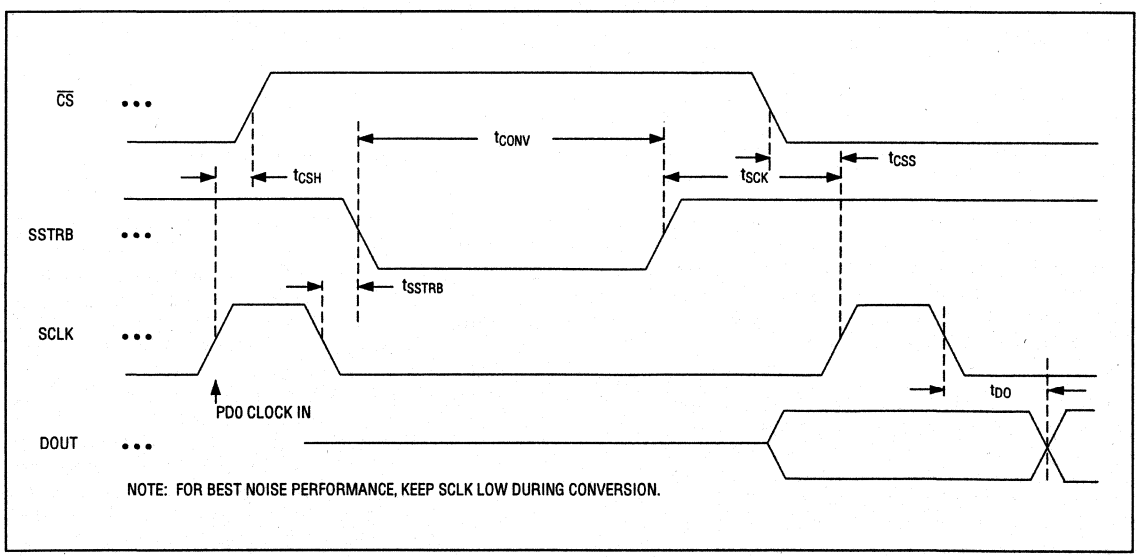


Figure 9. Internal Clock Mode SSTRB Detailed Timing

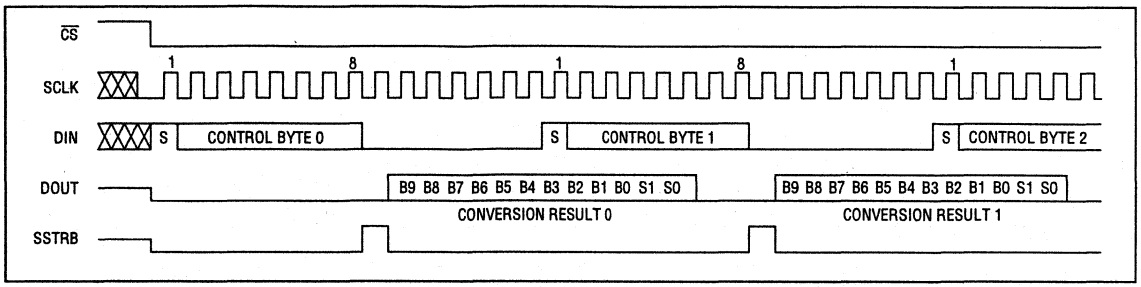


Figure 10a. External Clock Mode, 15 Clocks/Conversion Timing

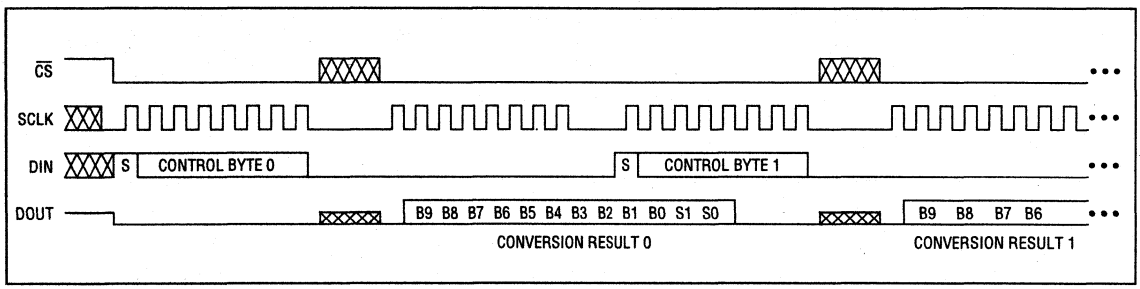


Figure 10b. External Clock Mode, 16 Clocks/Conversion Timing

Power-Down

The MAX1249's automatic power-down mode can save considerable power when operating at speeds below the maximum sampling rate. Figure 12 shows the average supply current as a function of the sampling rate. You can save power by placing the converter in a low-current shutdown state between conversions.

Select power-down via bits 1 and 0 of the DIN control byte with $\overline{SHDN}$ high (Tables 1 and 4). Pull $\overline{SHDN}$ low at any time to shut down the converter completely. $\overline{SHDN}$ overrides bits 1 and 0 of the control byte (Table 6).

Power-down mode turns off all chip functions that draw quiescent current, reducing I_{DD} typically to less than 5µA.

Figures 11a and 11b illustrate the various power-down sequences in both external and internal clock modes.

Software Power-Down

Software power-down is activated using bits PD1 and PD0 of the control byte. As shown in Table 4, PD1 and PD0 also specify the clock mode. When software shutdown is asserted, the ADC will continue to operate in the last specified clock mode until the conversion is complete. Then the ADC powers down into a low quiescent-current state. In internal clock mode, the interface remains active and conversion results may be clocked out after the MAX1249 has entered a software power-down.

The first logical 1 on DIN is interpreted as a start bit and powers up the MAX1249. No additional start-up time is required. Following the start bit, the data input word or control byte also determines clock mode and power-down states. For example, if the DIN word contains PD1 = 1, then the chip remains powered up. If PD0 = PD1 = 0, a power-down resumes after one conversion.

Hardware Power-Down

Pulling $\overline{SHDN}$ low places the converter in hardware power-down. Unlike software power-down mode, the conversion is not completed; it stops coincidentally with $\overline{SHDN}$ being brought low. $\overline{SHDN}$ also controls the clock frequency in internal clock mode. Letting $\overline{SHDN}$ float sets the internal clock frequency to 1.8MHz. When returning to normal operation with $\overline{SHDN}$ floating, there is a t_{RC} delay of approximately 2MΩ x C_L, where C_L is the capacitive loading on the $\overline{SHDN}$ pin. Pulling $\overline{SHDN}$ high sets the internal clock frequency to 225kHz. This feature eases the settling-time requirement for the reference voltage. The MAX1249 can be considered fully powered up within 2µs of actively pulling $\overline{SHDN}$ high.

+2.7V to +5.25V, Low-Power, 4-Channel, Serial 10-Bit ADC in QSOP-16

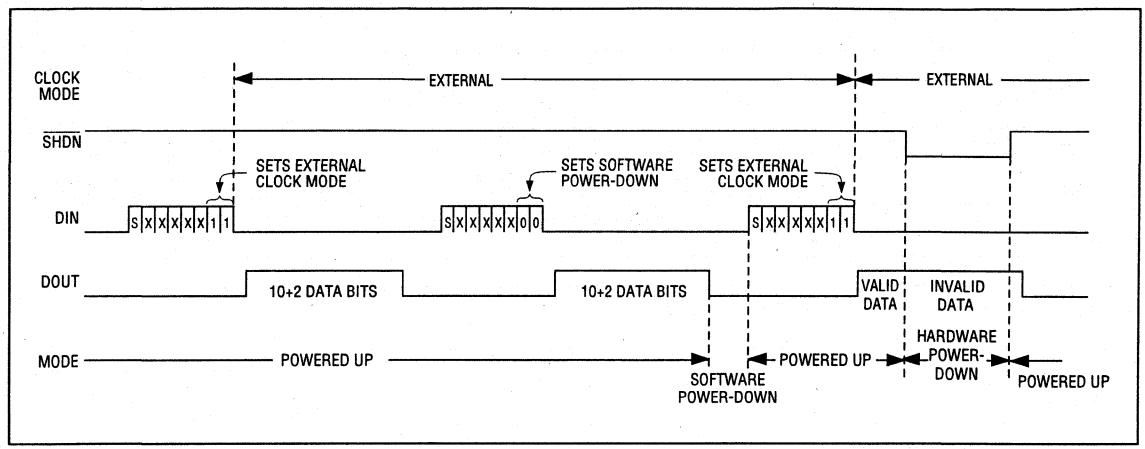


Figure 11a. Timing Diagram Power-Down Modes, External Clock

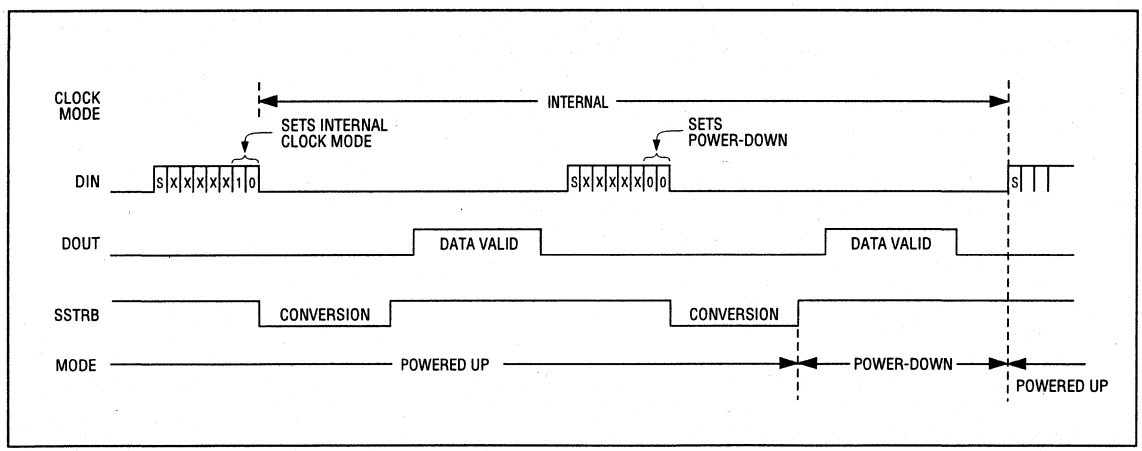


Figure 11b. Timing Diagram Power-Down Modes, Internal Clock

Table 4. Software Power-Down and Clock Mode

PD1	PD0	DEVICE MODE
1	1	External Clock
1	0	Internal Clock
0	1	Unassigned
0	0	Power-Down

Table 5. Hard-Wired Power-Down and Internal Clock Frequency

$\overline{SHDN}$ STATE	DEVICE MODE	INTERNAL CLOCK FREQUENCY
1	Enabled	225kHz
Floating	Enabled	1.8MHz
0	Power-Down	N/A

Table 6. Full Scale and Zero Scale

UNIPOLAR MODE		BIPOLAR MODE		
Full Scale	Zero Scale	Positive Full Scale	Zero Scale	Negative Full Scale
VREF + COM	COM	VREF / 2 + COM	COM	-VREF / 2 + COM

External Reference

An external reference is required for the MAX1249. The reference voltage range is 1V to V_{DD}.

At VREF, the input impedance is a minimum of 18kΩ for DC currents. During a conversion, the reference must be able to deliver up to 250µA DC load current and have an output impedance of 10Ω or less. If the reference has higher output impedance or is noisy, bypass it close to the VREF pin with a 0.1µF capacitor.

Transfer Function

Table 6 shows the full-scale voltage ranges for unipolar and bipolar modes using a 2.5V reference.

The external reference must have a temperature coefficient of 20ppm/°C or less to achieve accuracy to within 1LSB over the commercial temperature range of 0°C to +70°C.

Figure 13 depicts the nominal, unipolar input/output (I/O) transfer function, and Figure 14 shows the bipolar input/output transfer function. Code transitions occur halfway between successive-integer LSB values. Output coding is binary, with 1LSB = 2.44mV (2.500V / 1024) for unipolar operation and 1LSB = 2.44mV [(2.500V / 2 - -2.500V / 2) / 1024] for bipolar operation.

Layout, Grounding, and Bypassing

For best performance, use printed circuit boards. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

Figure 15 shows the recommended system ground connections. Establish a single-point analog ground ("star" ground point) at AGND, separate from the logic ground. Connect all other analog grounds and DGND to the star ground. No other digital system ground should be connected to this ground. The ground return to the power supply for the star ground should be low impedance and as short as possible for noise-free operation.

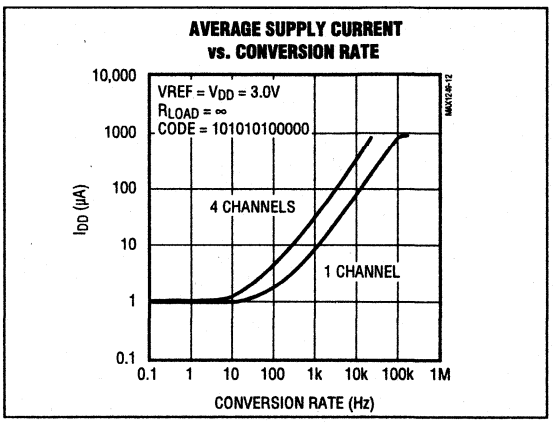


Figure 12. Average Supply Current vs. Conversion Rate

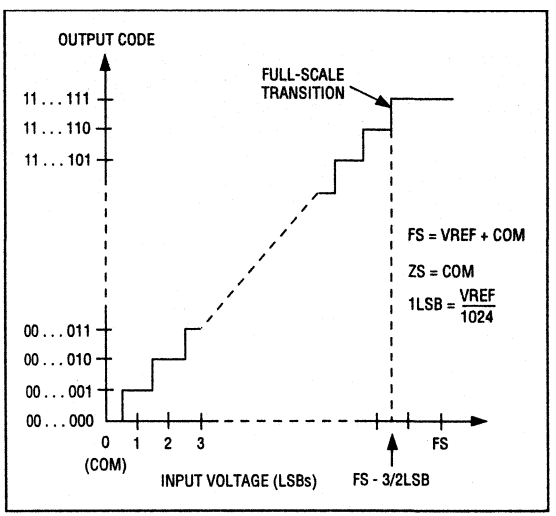


Figure 13. Unipolar Transfer Function, Full Scale (FS) = VREF + COM, Zero Scale (ZS) = COM

+2.7V to +5.25V, Low-Power, 4-Channel, Serial 10-Bit ADC in QSOP-16

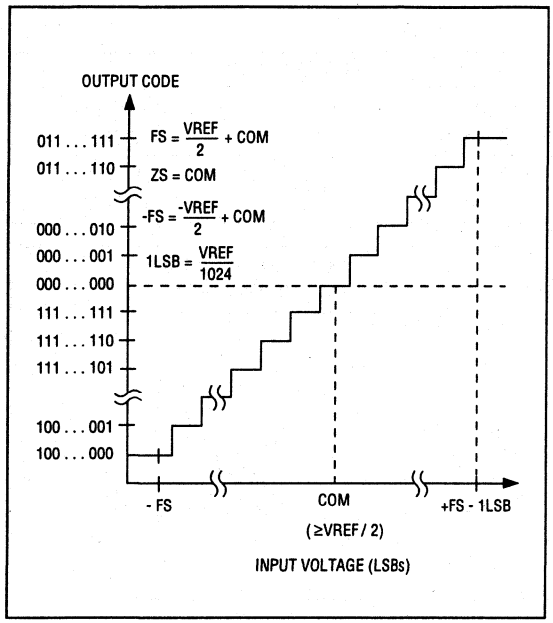


Figure 14. Bipolar Transfer Function, Full Scale (FS) = VREF / 2 + COM, Zero Scale (ZS) = COM

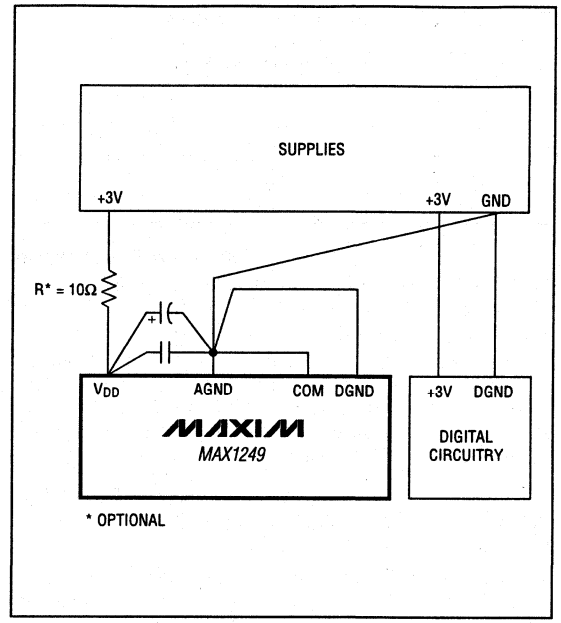


Figure 15. Power-Supply Grounding Connection

High-frequency noise in the V_{DD} power supply may affect the ADC's high-speed comparator. Bypass the supply to the star ground with 0.1µF and 4.7µF capacitors close to pin 1 of the MAX1249. Minimize capacitor lead lengths for best supply-noise rejection. If the +3V power supply is very noisy, a 10Ω resistor can be connected as a lowpass filter (Figure 15).

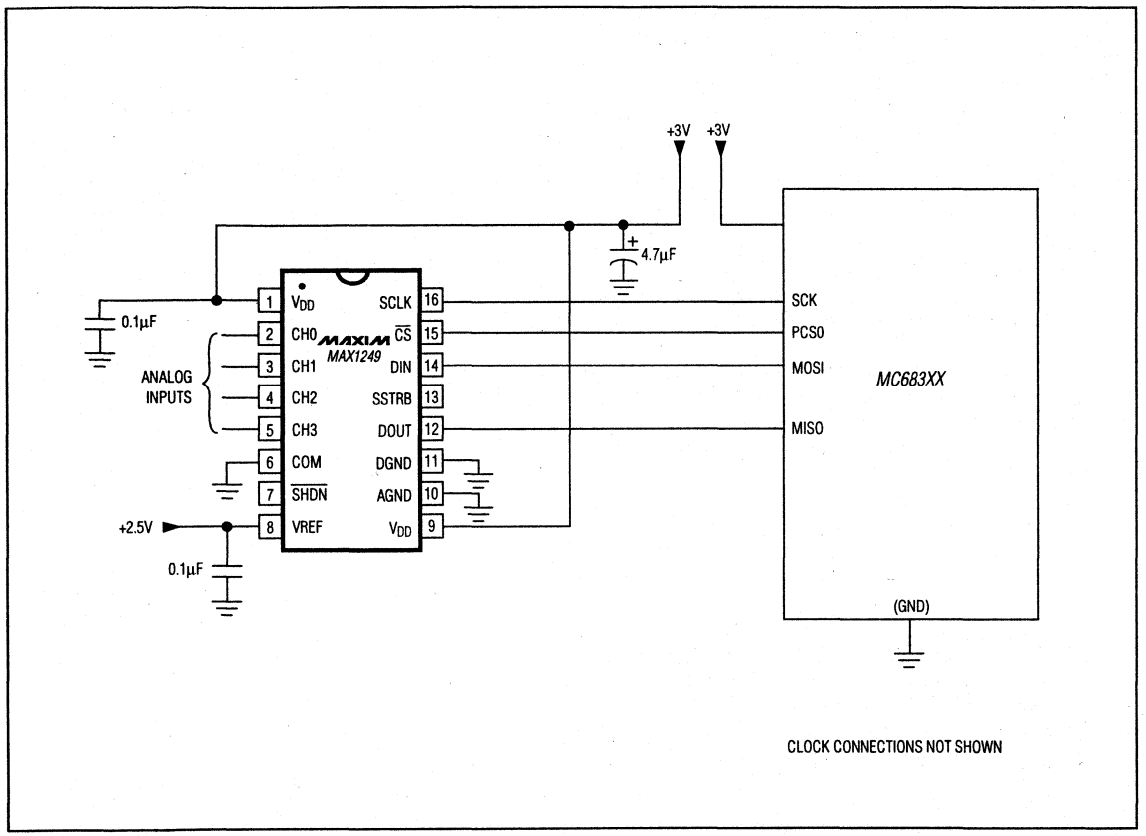


Figure 16. MAX1249 QSPI Connections

High-Speed Digital Interfacing with QSPI

The MAX1249 can interface with QSPI using the circuit in Figure 16 (f_{CLK} = 2.0MHz, CPOL = 0, CPHA = 0). This QSPI circuit can be programmed to do a conversion on each of the four channels. The result is stored in memory without taxing the CPU, since QSPI incorporates its own micro-sequencer.

The MAX1249 is QSPI compatible up to its maximum external clock frequency of 2.0MHz.

+2.7V to +5.25V, Low-Power, 4-Channel, Serial 10-Bit ADC in QSOP-16

TMS320LC3x-to-MAX1249 Interface

Figure 17 shows an application circuit to interface the MAX1249 to the TMS320 in external clock mode. The timing diagram for this interface circuit is shown in Figure 18.

Use the following steps to initiate a conversion in the MAX1249 and to read the results:

1) The TMS320 should be configured with CLKX (transmit clock) as an active-high output clock and CLKR (TMS320 receive clock) as an active-high input clock. CLKX and CLKR on the TMS320 are tied together with the MAX1249's SCLK input.
2) The MAX1249's $\overline{CS}$ pin is driven low by the TMS320's XF_ I/O port, to enable data to be clocked into the MAX1249's DIN.
3) An 8-bit word (1XXXXX11) should be written to the MAX1249 to initiate a conversion and place the device into external clock mode. Refer to Table 1 to select the proper XXXXX bit values for your specific application.
4) The MAX1249's SSTRB output is monitored via the TMS320's FSR input. A falling edge on the SSTRB output indicates that the conversion is in progress and data is ready to be received from the MAX1249.
5) The TMS320 reads in one data bit on each of the next 16 rising edges of SCLK. These data bits represent the 10 + 2-bit conversion result followed by four trailing bits, which should be ignored.
6) Pull $\overline{CS}$ high to disable the MAX1249 until the next conversion is initiated.

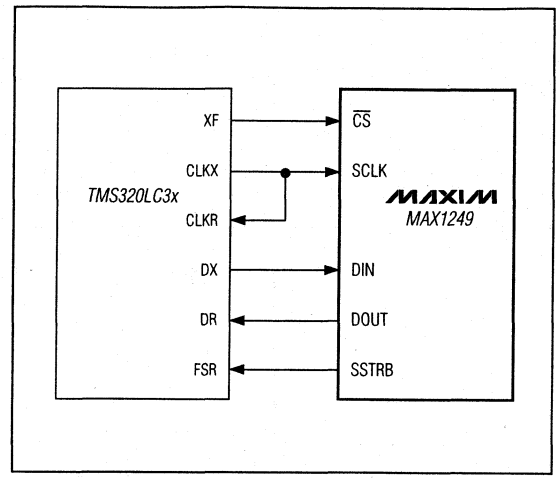


Figure 17. MAX1249-to-TMS320 Serial Interface

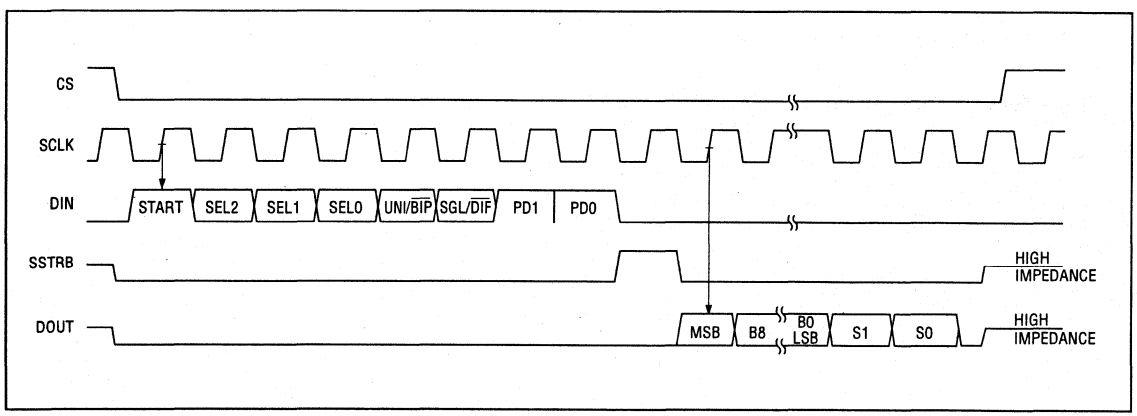


Figure 18. TMS320 Serial-Interface Timing Diagram

_Ordering Information (continued)

PART†	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX1249AEPE	-40°C to +85°C	16 Plastic DIP	±1/2
MAX1249BEPE	-40°C to +85°C	16 Plastic DIP	±1
MAX1249AEEE	-40°C to +85°C	16 QSOP	±1/2
MAX1249BEEE	-40°C to +85°C	16 QSOP	±1
MAX1249AMJE	-55°C to +125°C	16 CERDIP*	±1/2
MAX1249BMJE	-55°C to +125°C	16 CERDIP*	±1

† *Contact factory for availability of alternate surface-mount packages.*

* *Contact factory for availability of CERDIP package, and for processing to MIL-STD-883B.*

Chip Information

TRANSISTOR COUNT: 2554

MAXIM

Video Products/High-Speed Amplifiers

Video Products/High-Speed Amplifiers, Product Tables and Trees 8-3

MAX476	375MHz High-Speed Op Amp with Shutdown	8-7*
MAX477	300MHz High-Speed Amplifier	8-9
MAX496	375MHz, Quad, Gain of +1 Video Buffer	8-21
MAX497	275MHz, Quad, Gain of +2 Video Buffer	8-21
MAX498	310MHz, RGB + Sync Video Multiplexer with High-Speed Amplifier	8-33
MAX499	310MHz, RGB + Sync Video Multiplexer with High-Speed Amplifier	8-33
MAX4100	500MHz, High-Speed, Low-Power Op Amp	8-49
MAX4101	200MHz, A_{VCL} = 2V/V, High-Speed, Low-Power Op Amp	8-49
MAX4102	250MHz, High-Speed, Low-Power, Video Op Amp	8-61
MAX4103	180MHz, A_{VCL} = 2V/V, High-Speed, Low-Power Op Amp	8-61
MAX4106	350MHz, A_{VCL} = 5V/V, High-Speed, Ultra-Low-Noise Op Amp	8-73
MAX4107	300MHz, A_{VCL} = 10V/V, High-Speed, Ultra-Low-Noise Op Amp	8-73
MAX4108	400MHz, High-Speed, Ultra-Low-Distortion Op Amp	8-83
MAX4109	225MHz, A_{VCL} = 2V/V, High-Speed, Ultra-Low-Distortion Op Amp	8-83
MAX4112	500MHz, High-Speed, Current-Mode Feedback Op Amp	8-95
MAX4113	275MHz, A_{VCL} = 8V/V, High-Speed, Current-Mode Feedback Op Amp	8-95
MAX4117	500MHz, A_{VCL} = 2V/V, High-Speed, Current-Mode Feedback Op Amp	8-95
MAX4118	275MHz, A_{VCL} = 8V/V, High-Speed, Current-Mode Feedback Op Amp	8-95
MAX4119	Quad, 500MHz, Low-Power, Current-Mode Feedback Amplifier	8-107*
MAX4120	Quad, 275MHz, Low-Power, Current-Mode Feedback Amplifier	8-107*
MAX4135	1-Input/6-Output Video Distribution Amplifier	8-109
MAX4136	1-Input/6-Output Video Distribution Amplifier	8-109
MAX4137	1-Input/4-Output Video Distribution Amplifier	8-121
MAX4138	1-Input/4-Output Video Distribution Amplifier	8-121
MAX4144	High-Speed Instrumentation Amplifier	8-133
MAX4146	High-Speed Instrumentation Amplifier	8-133
MAX4147	350MHz, Low Power, High-Output-Current, Differential Line Driver	8-145
MAX4158	330MHz, 2-Channel, High-Speed, Video Multiplexer/Amplifier	8-153*
MAX4159	330MHz, 2-Channel, High-Speed, Video Multiplexer/Amplifier	8-153*
MAX4177	380MHz, Unity-Gain, High-Speed Buffer	8-155*
MAX4178	330MHz, Precision, Closed-Loop, Fixed Gain of +1 Buffer	8-157
MAX4180	Low-Power, 340MHz, Single Current-Mode Feedback Amplifier	8-167*
MAX4181	Low-Power, 400MHz, Single Current-Mode Feedback Amplifier	8-167*
MAX4182	Low-Power, 340MHz, Dual Current-Mode Feedback Amplifier	8-167*
MAX4183	Low-Power, 340MHz, Dual Current-Mode Feedback Amplifier	8-167*
MAX4184	Low-Power, 400MHz, Dual Current-Mode Feedback Amplifier	8-167*
MAX4185	Low-Power, 400MHz, Dual Current-Mode Feedback Amplifier	8-167*

*Advance Information–first page of data sheet in preparation.

_Video Products/High-Speed Amplifiers (continued)

MAX4186	Low-Power, 340MHz, Quad Current-Mode Feedback Amplifier	8-167*
MAX4187	Low-Power, 400MHz, Quad Current-Mode Feedback Amplifier	8-167*
MAX4258	275MHz, A_{VCL} = 2V/V, 2-Channel, High-Speed, Video Multiplexer/Amplifier	8-153*
MAX4259	275MHz, A_{VCL} = 2V/V, 2-Channel, High-Speed, Video Multiplexer/Amplifier	8-153*
MAX4277	350MHz, Gain of +2, High-Speed Buffer	8-155*
MAX4278	310MHz, Precision, Closed-Loop, Fixed Gain of +2 Buffer	8-157
MAX4308	225MHz, Ultra-Low-Distrortion Op Amp	8-169*
MAX4309	200MHz, Ultra-Low-Distortion Op Amp	8-169*

*Advance Information–first page of data sheet in preparation.

Video & High-Speed Products

Buffers

MAX4005
(950MHz, JFET)

MAX405
(180MHz,
0.998V/V gain)

MAX4178
(330MHz, AVCL = +1V/V)

☆ MAX4278
(310MHz, AVCL = +2V/V)

MAX460
(140MHz,
JFET input)

MAX467
(100MHz,
triple buffer)

MAX468
(100MHz, quad buffer)

MAX469
(90MHz,
AVCL = +2V/V,
triple buffer)

MAX470
(90MHz,
AVCL = +2V/V,
quad buffer)

☆ MAX496
(375MHz,
AVCL = +1V/V,
quad buffer)

☆ MAX497
(275MHz,
AVCL = +2V/V,
quad buffer)

† MAX4177
(380MHz,
AVCL = +1V/V)

† MAX4277
(350MHz,
AVCL = +2V/V)

RGB Switches

MAX463
(100MHz, output
drivers)

☆ MAX464
(100MHz, output
drivers)

MAX465
(90MHz, AVCL = +2V/V,
output drivers)

☆ MAX466
(90MHz, AVCL = +2V/V,
output drivers)

★MAX498
(310MHz, AVCL = +2V/V,
output drivers)

★MAX499
(310MHz, AVCL = +2V/V,
output drivers)

Crosspoint Switches

☆ MAX4111
(330MHz 1x1)

☆ MAX4121
(330MHz 2x1)

☆ MAX4141
(330MHz 4x1)

☆ MAX4221
(330MHz dual 2x1)

MAX456
(8x8)

☆ MAX458
(100MHz 8x4,
output drivers)

☆ MAX459
(90MHz 8x4,
AVCL = +2V/V,
output drivers)

Multiplexers

☆ MAX4111
(330MHz 1x1)

☆ MAX4121
(330MHz 2x1)

☆ MAX4141
(330MHz 4x1)

★☆ MAX4158
(330MHz,
2-ch mux + output amp)

★ MAX4159
(330MHz,
2-ch mux + output amp)

MAX4221
(330MHz dual 2x1)

★ MAX4258
(275MHz, AVCL = +2V/V
2-ch mux + output amp)

★ MAX4259
(275MHz, AVCL = +2V/V
2-ch mux + output amp)

MAX440
(160MHz, 8-ch mux
+ output amp)

MAX441
(160MHz, 4-ch mux
+ output amp)

MAX442
(160MHz, 2-ch mux
+ output amp)

MAX453
(50MHz, 2-ch mux
+ output amp)

MAX454
(50MHz, 4-ch mux
+ output amp)

MAX455
(50MHz, 8-ch mux
+ output amp)

Amplifiers

MAX404
(40MHz, AVCL = +2V/V)

MAX408
(33MHz, AVCL = +3V/V)

MAX4100/4101
(500MHz, low power)

★ MAX4102/4103
(250MHz, lowest DP/DG)

☆ MAX4106/4107
(350MHz, 0.75nV/√Hz)

☆ MAX4108/4109
(400MHz,1200V/µs)

☆ MAX4112/4113
(500MHz,1200V/µs)

★☆ MAX4117/4118
(Dual, 500MHz)

† MAX4119/4120
(Quad, 500MHz, 1200V/µs)

† MAX4180/4181
(SOT23-6, 400MHz, 1mA)

† MAX4182–MAX4185
(Dual, 400MHz, 1mA)

† MAX4186/4187
(Quad, 400MHz, 1mA)

† MAX4308/4309
(400MHz, -90dBc SFDR,
AVCL = +5V/V/+10V/V)

MAX428
(Dual MAX408)

MAX435
(275MHz, diff in/diff out)

MAX436
(200MHz, diff in/single out)

MAX448
(Quad MAX408)

MAX452
(50MHz)

CRT Driver

MAX445
(200MHz, 2.5ns tr/tf,
high-voltage output)

MAX453
(50MHz,
2-ch mux + amp)

MAX454
(50MHz,
4-ch mux + amp)

MAX455
(50MHz,
8-ch mux + amp)

MAX457
(70MHz dual)

† MAX476
(300MHz,
1100V/ms)

☆ MAX477
(300MHz,
1100V/ms)

Distribution Amplifiers

★☆ MAX4135
(185MHz, AVCL = +2V/V
1 input/6 output)

★☆ MAX4136
(140MHz, AVCL = +2V/V
1 input/6 output)

★☆ MAX4137
(185MHz, AVCL = +2V/V
1 input/4 output)

★☆ MAX4138
(140MHz, AVCL = +2V/V
1 input/4 output)

Differential Line Drivers

★☆ MAX4147
(350MHz, AVCL = +2V/V
high output drive)

High-Speed Line Receivers

★☆ MAX4144
(130MHz, AVCL = +2V/V)

†☆ MAX4146
(70MHz, AVCL = +10V/V)

★ New product
† Future product
☆ Evaluation kit available

Part Number	-3dB BW (MHz)	Min. Stable Gain (V/V)	0.1dB BW (MHz)	Slew Rate (V/µs)	V_{OUT} Swing/ Load (V/Ω)	DP/DG (deg./%)	Output Current (mA min)	Supply Voltage (V)	Supply Current per Ch. (mA)	Features	Price† 1000-up ($)
VIDEO/RF AMPLIFIERS											
MAX404	40	+2	–	500	±8/50	0.01/0.05	50	±5	30	Broadcast-quality, low DP/DG, symmetrical inputs, 70dB CMRR, 66dB A_{VOL}	2.68
MAX408/428/448	33	+3	–	90	±2.7/51	N/A	50/ op amp	±5	7/7.5 7.5	Single/dual/quad, high output drive	3.02/4.06/ 6.74
MAX435/436	275/200	+1	–	800	±3.5/500	N/A	10	±5	35	Ultra-fast differential input/output transconductance amp, no feedback required	2.75
MAX445	200		–	2.5ns tr/tf	75V (max)	N/A	80	±10, +75	70 (V+)	CRT video display driver for ultra-high-resolution monitors, single IC preamp and high-voltage (+75V) output stage	6.83
MAX452	50	+1	–	300	±3/150	0.2/0.5	14	±5	25	Unity-gain stable, drives 75Ω coaxial cable	2.40
MAX457	70	+1	–	300	±2.5/150	0.2/0.5	15	±5	17.5	Dual, unity-gain stable, drives 75Ω coaxial cable	4.45
MAX476	300	+1	130	1100	±3/100	0.01/0.01	70	±5	8	Voltage feedback, 130MHz 0.1dB gain flatness, drives 100pF C_{LOADS} w/enable	††
MAX477	300	+1	130	1100	±3/100	0.01/0.01	70	±5	8	Voltage feedback, 130MHz 0.1dB gain flatness, drives 100pF C_{LOADS}	2.40
MAX4100/4101	500/200	+1/+2	65/50	250	±3.5/100	0.04/0.06, 0.04/0.07	65	±5	5	Low power, low cost, voltage feedback	1.95
MAX4102/4103	250/180	+1/+2	130/80	350	±3.4/100	0.002/0.002, 0.003/0.008	65	±5	4.6	Ultra-low differential phase/gain, broadcast quality	1.95
MAX4106/4107	350/300	+5/+10	75/45	275/500	±3.5/100	0.02/0.04, 0.03/0.03	65	±5	15	0.75nV/$\sqrt{Hz}$, ultra-low noise, low distortion	3.88
MAX4108/4109	400/225	+1/+2	100/25	1200	+2.7 to -3.7/100	0.002/0.002, 0.002/0.008	65	±5	20	Ultra-low distortion: -81/-80dBc at 20MHz (SFDR)	3.88
MAX4112/4113	500/275	+2/+3	30/90	1200/ 1800	±3.5/100	0.03/0.02, 0.04/0.02	65	±5	5	Low power, low cost, current-mode feedback	1.95
MAX4117/4118	500/275	+2/+3	30/90	1200/ 1800	±3.5/100	0.03/0.02, 0.04/0.02	65	±5	5	Dual, low power, low cost, current-mode feedback, 300/275MHz full-power bandwidth	2.65
MAX4119/4120	500/275	+2/+3	30/90	1200/ 1800	±3.5/100	0.03/0.02, 0.04/0.02	65	±5	5	Quad, low-power, low-cost current-mode feedback	††
MAX4180/4181	340/400	+2/+1	80/60	1200	±3.2/150	0.04/0.02	50	±5/±5	1	Single, 1mA, high-speed SOT23 amplifiers	††
MAX4182/4183	340	+2	80	1200	±3.2/150	0.04/0.02	50	±5/±5	1	Dual, 1mA, high-speed amplifiers	††
MAX4184/4185	400	+1	60	1200	±3.2/150	0.04/0.02	50	±5/±5	1	Dual, 1mA, high-speed amplifiers	††
MAX4186/4187	340/400	+2/+1	80/60	1200	±3.2/150	0.04/0.02	50	±5/±5	1	Quad, 1mA, high-speed amplifiers	††
MAX4308/4309	225/200	+5/+10	100/25	1200	+2.7 to -3.7/100	0.008/0.002	65	±5	20	Ultra-low distortion: -81/-80dBc at 20MHz (SFDR)	††

Part Number	-3dB BW (MHz)	Gain (V/V)	0.1dB BW (MHz)	Slew Rate (V/µs)	V_{OUT} Swing/ Load (V/Ω)	DP/DG (deg./%)	Output Current (mA min)	Supply Voltage (V)	Supply Current per Ch. (mA)	Features	Price† 1000-up ($)
VIDEO/RF BUFFERS											
MAX4005	950	+1	60	1000	+0.8 to -0.65/75	0.03/0.11	75Ω output	±5	24	FET input buffer with 75Ω output to minimize reflections, low DP/DG, 60MHz 0.1dB gain flatness, 28dBm IP_3 (100MHz)	2.75
MAX405	180	+0.99	–	650	±3.4/50	0.01/0.03	60	±5	35	Closed loop, 0.99V gain guaranteed over temp	4.25
MAX4177	330	+1	150	1300	±2.5/50	0.01/0.04	70	±5	8	Closed loop, gain of +1 buffer, 150MHz 0.1dB gain flatness with enable	††
MAX4178	330	+1	150	1300	±2.5/50	0.01/0.04	70	±5	8	Closed loop, gain of +1 buffer, 150MHz 0.1dB gain flatness, low DP/DG	2.40
MAX4277	310	+2	150	1600	±2.5/50	0.01/0.04	70	±5	8	Closed loop, gain of +2 buffer, 150MHz 0.1dB gain flatness with enable	††
MAX4278	310	+2	150	1600	±2.5/50	0.01/0.04	70	±5	8	Closed loop, gain of +2 buffer, 150MHz 0.1dB gain flatness, low DP/DG	2.40
MAX460	140	+0.99	–	1500	±9.8/100	N/A	90	±15	19	FET input, EL2005/LH0033 upgrade	19.78
MAX467	100	+1	–	200	±2.4/75	0.03/0.01	20	±5	17	Triple (RGB) video buffer, low DP/DG	3.70
MAX468	100	+1	–	200	±2.4/75	0.03/0.01	20	±5	16	Quad, unity-gain video buffer, low DP/DG	4.20
MAX469	90	+2	–	300	±2.4/75	0.14/0.12	20	±5	17	Triple (RGB), gain of +2 video buffer, low DP/DG	3.70
MAX470	90	+2	–	300	±2.4/75	0.14/0.12	20	±5	16	Quad, gain of +2 (6dB) video buffer, low DP/DG	4.20
MAX496	375	+1	80	1600	±3.3/50	0.01/0.01	66	±5	8	Quad, gain of +1 (0dB) closed-loop buffer, low DP/DG	4.95
MAX497	275	+2	120	1500	±3.3/50	0.01/0.01	66	±5	8	Quad, gain of +2 (6dB) closed-loop buffer, low DP/DG	4.95

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†† Future product—contact factory for pricing and availability. Specifications are preliminary.

Part Number	-3dB BW (MHz)	Gain (V/V)	0.1dB BW (MHz)	Slew Rate (V/µs)	VOUT Swing/ Load (V/Ω)	DP/DG (deg./%)	Output Current (mA min)	Supply Voltage (V)	Supply Current per Ch. (mA)	Features	Price† 1000-up ($)
VIDEO MULTIPLEXERS/AMPLIFIERS											
MAX4111	330	+0.99	150	700	±2.5/5k	0.01/0.01	500µA	±5	4	1x1 video crosspoint building block, 150MHz 0.1dB gain flatness, low DP/DG	1.70
MAX4121	330	+0.99	150	700	±2.5/5k	0.01/0.01	500µA	±5	4	2x1 video crosspoint building block, 150MHz 0.1dB gain flatness, low DP/DG	2.10
MAX4141	330	+0.99	150	700	±2.5/5k	0.01/0.01	500µA	±5	4	4x1 video crosspoint building block, 150MHz 0.1dB gain flatness, low DP/DG	4.50
MAX4158	330	+1	90	1200	±3.5/50	0.02/0.02	80	±5	11	2 inputs/1 output, current-mode feedback, fixed gain of 1V/V	2.30
MAX4159	330	+1	90	1200	±3.5/50	0.02/0.02	80	±5	11	2 inputs/1 output, current-mode feedback, fixed gain of 1V/V, address latch and output enable	2.60
MAX4221	330	+0.99	150	700	±2.5/5k	0.01/0.01	500µA	±5	5	Dual 2x1 video crosspoint building block, 150MHz 0.1dB gain flatness, low DP/DG	4.50
MAX4258	275	+2	100	1200	±3.5/50	0.02/0.02	80	±5	11	2 inputs/1 output, current-mode feedback, fixed gain of 2V/V	2.30
MAX4259	275	+2	120	1200	±3.5/50	0.02/0.02	80	±5	11	2 inputs/1 output, current-mode feedback, fixed gain of 2V/V, address latch and output enable	2.60
MAX440	160	+1	–	370	±3/150	0.03/0.04	20	±5	40	Video amp with 8-channel mux, low DP/DG, 15ns switch time, high-Z output state	8.95
MAX441	160	+1	–	370	±3/150	0.03/0.04	20	±5	40	Video amp with 4-channel mux, low DP/DG, 15ns switch time	5.90
MAX442	140	+1	–	250	±3/75	0.09/0.07	33	±5	40	Video amp with 2-channel mux, 15ns switch time, 8-pin DIP/SO	4.45
MAX453	50	+1	–	300	±3/150	1.2/0.5	14	±5	25	Video amp with 2-channel video mux	3.94
MAX454	50	+1	–	300	±3/150	1.2/0.5	14	±5	25	Video amp with 4-channel video mux	5.25
MAX455	50	+1	–	300	±3/150	1.2/0.5	14	±5	25	Video amp with 8-channel video mux	8.75

Part Number	-3dB BW (MHz)	Buffer Amp Gain (V/V)	0.1dB BW (MHz)	Slew Rate (V/µs)	VOUT Swing/ Load (V/Ω)	Switching Time (ns)	Number of Inputs	Number of Outputs	Output Current (mA)	EV Kit	Features	Price† 1000-up ($)
RGB VIDEO SWITCHES												
MAX463/465	100/90	+1/+2	–	300	±2.4/75	20	6 (RGB$_A$, RGB$_B$)	3 (RGB)	20		RGB switch with 75Ω cable drivers	6.97
MAX464/466	100/90	+1/+2	–	300	±2.4/75	20	8 (RGB$_A$ + Sync, RGB$_B$ + Sync)	4 (RGB + Sync)	20	Yes	RGB + sync switch with 75Ω cable drivers	7.97
MAX498	310	+2	120	1250	±3/100	3	8 (RGB$_A$ + Sync, RGB$_B$ + Sync)	4 (RGB + Sync)	75		Drives back-terminated 75Ω cables	4.40
MAX499	310	+2	120	1250	±3/100	3	6 (RGB$_A$, RGB$_B$)	3 (RGB)	75		Drives back-terminated 75Ω cables	3.50

Part Number	-3dB BW (MHz)	Min. Gain Stable (V/V)	0.1dB BW (MHz)	Slew Rate (V/µs)	VOUT Swing/ Load (V/Ω)	DP/DG (deg./%)	Output Current (mA)	Supply Voltage (V)	Supply Current per Ch. (mA)	Features	Price† 1000-up ($)
DISTRIBUTION AMPLIFIERS											
MAX4135	185	+2	40	1000	+2.6 to -2.4 /150	0.02/0.09	70	±5	45	1 input/6 outputs, fixed gain of 2V/V, high-impedance outputs in shutdown. Outputs can be individually enabled/disabled.	5.90
MAX4136	140	+2	40	1000	+2.6 to -2.4 /150	0.03/0.12	70	±5	45	1 input/6 outputs, external gain set, high-impedance outputs in shutdown. Outputs can be individually enabled/disabled.	5.90
MAX4137	185	+2	40	1000	+2.6 to -2.4 /150	0.02/0.10	70	±5	30	1 input/4 outputs, fixed gain of 2V/V, high-impedance outputs in shutdown. Outputs can be individually enabled/disabled.	4.50
MAX4138	140	+2	40	1000	+2.6 to -2.4 /150	0.02/0.10	70	±5	30	1 input/4 outputs, external gain set, high-impedance outputs in shutdown. Outputs can be individually enabled/disabled.	4.50

Part Number	-3dB BW (MHz)	Gain (V/V)	0.1dB BW (MHz)	Slew Rate (V/µs)	VOUT Swing/ Load (V/Ω)	DP/DG (deg./%)	Output Current (mA)	Supply Voltage (V)	Supply Current per Ch. (mA)	Features	Price† 1000-up ($)
DIFFERENTIAL LINE DRIVERS											
MAX4147	350	+2	100	3600	±3.2/50	0.01/0.008	160	±5	11	Fixed gain of 2V/V, high output drive	2.50
HIGH-SPEED LINE RECEIVERS											
MAX4144	130	+2	30	1000	±2.6/150	0.03/0.03	50	±5	13	Fixed gain of 2V/V, differential input/single-ended output	3.35
MAX4146	70	+10	10	800	±2.6/150	0.07/0.12	50	±5	13	External gain set, low noise 3.5nV/Hz, differential input/single-ended output	††

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Part Number	-3dB BW (MHz)	Min. Stable Gain (V/V)	0.1dB BW (MHz)	Slew Rate (V/µs)	V_{OUT} Swing/ Load (V/Ω)	DP/DG (deg./%)	Off Isolation (dB)	Crosstalk (dB)	EV Kit	Features	Price† 1000-up ($)
VIDEO CROSSPOINT SWITCHES											
MAX4111	330	+0.99	150	700	±2.5/5k	0.01/0.01	86 (30MHz)	N/A	Yes	1x1 video crosspoint building block, 0.1dB gain flatness of 150MHz	1.70
MAX4121	330	+0.99	150	700	±2.5/5k	0.01/0.01	78 (30MHz)	-92 (30MHz)	Yes	2x1 video crosspoint building block, 0.1dB gain flatness of 150MHz	2.10
MAX4141	330	+0.99	150	700	±2.5/5k	0.01/0.01	74 (30MHz)	-66 (30MHz)	Yes	4x1 video crosspoint building block, 0.1dB gain flatness of 150MHz	2.95
MAX4221	330	+0.99	150	700	±2.5/5k	0.01/0.01	84 (30MHz)	-70 (30MHz)	Yes	Dual 2x1 video crosspoint building block, 0.1dB gain flatness of 150MHz	2.95
MAX456	35	+1	–	250	±1.3/0	1/0.5	80 (5MHz)	-70 (5MHz)		8x8 crosspoint switch array with eight output buffers, high-Z output capability	19.98
MAX458/459	100/90	+1/+2	–	200 /300	±3/150	0.05/0.01	60 (10MHz)	-55 (10MHz)	Yes	8x4 crosspoint switch array with four 75Ω cable drivers, high-Z output capability	21.85

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ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

10/96

MAXIM

300MHz High-Speed Op Amp

General Description

The MAX476 is a ±5V wide-bandwidth, fast-settling, unity-gain-stable op amp featuring low noise, low differential gain and phase errors, high slew rate, high precision, and high output current. The MAX476's architecture uses a standard voltage-feedback topology that can be configured into any desired gain setting, as with other general-purpose op amps.

Unlike high-speed amplifiers using current-mode feedback architectures, the MAX476 has a unique input stage that combines the benefits of the voltage-feedback design (flexibility in choice of feedback resistor, two high-impedance inputs) with those of the current-feedback design (high slew rate and full-power bandwidth). It also has the precision of voltage-feedback amplifiers, characterized by low input-offset voltage and bias current, low noise, and high common-mode and power-supply rejection.

The MAX476 is ideally suited for driving 50Ω or 75Ω loads. The device also features a shutdown mode that can be used to conserve power and to disable the output for multiplexer applications. The MAX476 is available in 8-pin DIP, SO, and µMAX packages.

Applications

Broadcast and High-Definition TV Systems

Video Switching and Routing

Communications

Medical Imaging

Precision DAC/ADC Buffer

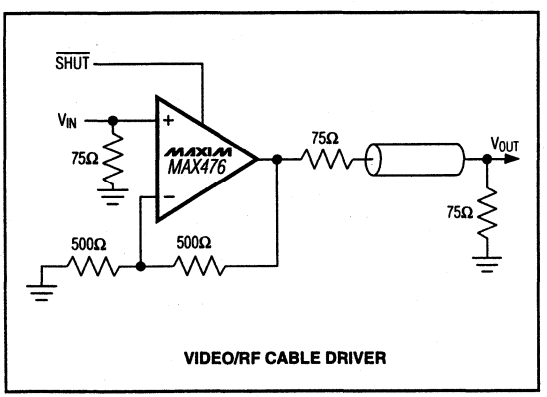
Features

- **High Speed:**
  300MHz -3dB Bandwidth (A_V = +1)
  200MHz Full-Power Bandwidth (A_V = +1, V_O = 2Vp-p)
  1100V/µs Slew Rate
  130MHz 0.1dB Gain Flatness
- **Drives 100pF Capacitive Loads Without Oscillation**
- **Low Differential Phase/Gain Error: 0.01°/0.01%**
- **8mA Quiescent Current**
- **Low Input-Referred Voltage Noise: 5nV/√Hz**
- **Low Input-Referred Current Noise: 2pA/√Hz**
- **Low Input Offset Voltage: 0.5mV**
- **High-Z Output in Shutdown Mode**
- **Voltage-Feedback Topology for Simple Design Configurations**
- **Short-Circuit Protected**
- **Available in µMAX Package**

Ordering Information

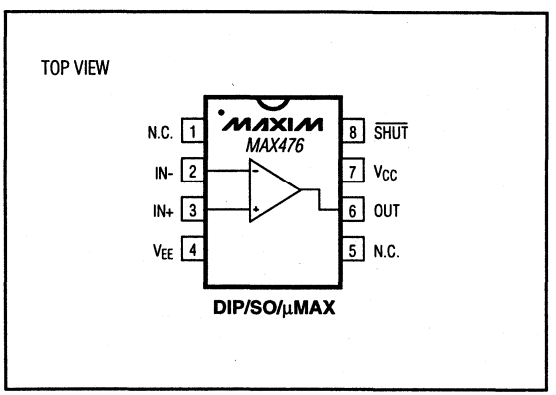
PART	TEMP. RANGE	PIN-PACKAGE
MAX476EPA	-40°C to +85°C	8 Plastic DIP
MAX476ESA	-40°C to +85°C	8 SO
MAX476EUA	-40°C to +85°C	8 µMAX
MAX476MJA	-55°C to +125°C	8 CERDIP

Typical Operating Circuit



VIDEO/RF CABLE DRIVER

Pin Configuration



DIP/SO/µMAX

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

19-0467; Rev 1; 10/96

MAXIM

300MHz High-Speed Op Amp

General Description

The MAX477 is a ±5V wide-bandwidth, fast-settling, unity-gain-stable op amp featuring low noise, low differential gain and phase errors, high slew rate, high precision, and high output current. The MAX477's architecture uses a standard voltage-feedback topology that can be configured into any desired gain setting, as with other general-purpose op amps.

Unlike high-speed amplifiers using current-mode feedback architectures, the MAX477 has a unique input stage that combines the benefits of the voltage-feedback design (flexibility in choice of feedback resistor, two high-impedance inputs) with those of the current-feedback design (high slew rate and full-power bandwidth). It also has the precision of voltage-feedback amplifiers, characterized by low input-offset voltage and bias current, low noise, and high common-mode and power-supply rejection.

The MAX477 is ideally suited for driving 50Ω or 75Ω loads. Packages include 8-pin DIP, SO, and µMAX.

Applications

Broadcast and High-Definition TV Systems
Video Switching and Routing
Communications
Medical Imaging
Precision DAC/ADC Buffer

Features

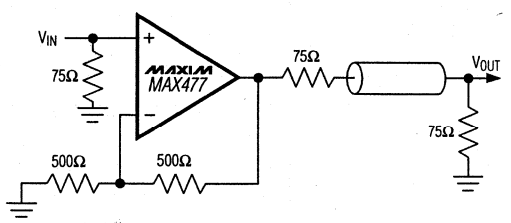
- **High Speed:**
  300MHz -3dB Bandwidth (A_V = +1)
  200MHz Full-Power Bandwidth (A_V = +1, V_O = 2Vp-p)
  1100V/µs Slew Rate
  130MHz 0.1dB Gain Flatness
- **Drives 100pF Capacitive Loads Without Oscillation**
- **Low Differential Phase/Gain Error: 0.01°/0.01%**
- **8mA Quiescent Current**
- **Low Input-Referred Voltage Noise: 5nV/√Hz**
- **Low Input-Referred Current Noise: 2pA/√Hz**
- **Low Input Offset Voltage: 0.5mV**
- **8000V ESD Protection**
- **Voltage-Feedback Topology for Simple Design Configurations**
- **Short-Circuit Protected**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX477EPA	-40°C to +85°C	8 Plastic DIP
MAX477ESA	-40°C to +85°C	8 SO
MAX477EUA	-40°C to +85°C	8 µMAX
MAX477MJA	-55°C to +125°C	8 CERDIP*

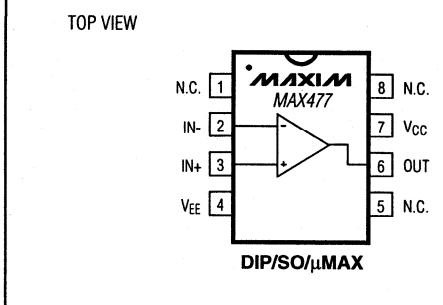
** Contact factory for availability.*

Typical Operating Circuit



VIDEO/RF CABLE DRIVER

Pin Configuration



DIP/SO/µMAX

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

300MHz High-Speed Op Amp

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to V_{EE}) 13V
Differential Input Voltage ..... (V_{CC} + 0.3V) to (V_{EE} - 0.3V)
Common-Mode Input Voltage ..... (V_{CC} + 0.3V) to (V_{EE} - 0.3V)
Output Short-Circuit Duration to GND ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C) 471mW
µMAX (derate 4.1mW/°C above +70°C) 330mW
CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges
MAX477E_A ..... -40°C to +85°C
MAX477MJA ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, V_{OUT} = 0V, R_L = ∞, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	T_A = +25°C			0.5	2.0	mV
		T_A = T_{MIN} to T_{MAX}				3.0	
Input Offset-Voltage Drift	TCV_{OS}				2		µV/°C
Input Bias Current	I_B	T_A = +25°C			1	3	µA
		T_A = T_{MIN} to T_{MAX}				5.0	
Input Offset Current	I_{OS}	T_A = +25°C			0.2	0.5	µA
		T_A = T_{MIN} to T_{MAX}				2.0	
Differential-Mode Input Resistance	$R_{IN(DM)}$	Either input			1		MΩ
Common-Mode Input Voltage Range	V_{CM}	T_A = +25°C		±3.0	±3.5		V
		T_A = T_{MIN} to T_{MAX}		±2.5			
Common-Mode Rejection Ratio	CMRR	T_A = +25°C	V_{CM} = ±3V	70	90		dB
		T_A = T_{MIN} to T_{MAX}	V_{CM} = ±2.5V	60			
Power-Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±5.5V		70	85		dB
Open-Loop Voltage Gain	A_{VOL}	V_{OUT} = ±2.0V, V_{CM} = 0V, R_L = 50Ω		55	65		dB
Output Voltage Swing	V_{OUT}	T_A = +25°C	R_L = ∞	±3.5	±3.9		V
		T_A = T_{MIN} to T_{MAX}	R_L = 100Ω	±3.0			
			R_L = 50Ω	±2.5			
Minimum Output Current	I_{OUT}	T_A = -40 °C to +85 °C		70	100		mA
Short-Circuit Output Current	I_{SC}	Short to ground			150		mA
Open-Loop Output Resistance	R_{OUT}	V_{OUT} = 0, f = DC			0.1		Ω
Quiescent Supply Current	I_{SY}	T_A = +25°C			8	10	mA
		MAX477E_A, T_A = T_{MIN} to T_{MAX}				12	mA
		MAX477MJA, T_A = T_{MIN} to T_{MAX}				14	

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, A_{VCL} = +1, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Small-Signal, -3dB Bandwidth	BW_{-3dB}	$V_{OUT} \le 0.1Vp\text{-}p$	MAX477ESA	220	300		MHz
			MAX477EPA/EUA/MJA		300		
Small-Signal, ±0.1dB Gain Flatness	$BW_{0.1dB}$	$V_{OUT} \le 0.1Vp\text{-}p$	MAX477ESA	30	130		MHz
			MAX477EPA/EUA/MJA		130		
Full-Power Bandwidth (Note 1)	FPBW	V_{OUT} = 2Vp-p			200		MHz
Slew Rate	SR	V_{OUT} = ±2Vp-p		900	1100		V/µs
Settling Time	t_S	V_{OUT} = 2V Step	to 0.1%		10		ns
			to 0.01%		12		
Rise Time, Fall Time	t_R, t_F	V_{OUT} = 2V Step			2		ns
Input Voltage Noise Density	e_n	f = 10MHz			5		$nV/\sqrt{Hz}$
Input Current Noise Density	i_n	f = 10MHz, either input			2		$pA/\sqrt{Hz}$
Differential Gain (Note 2)	DG	f = 3.58MHz			0.01		%
Differential Phase (Note 2)	DP	f = 3.58MHz			0.01		degrees
Differential-Mode Input Capacitance	$C_{IN(DM)}$	Either input			1		pF
Output Impedance	Z_{OUT}	f = 10MHz			2.5		Ω
Total Harmonic Distortion	THD	f_C = 10MHz, V_{OUT} = 2Vp-p			-58		dB
Spurious-Free Dynamic Range	SFDR	f = 5MHz, V_{OUT} = 2Vp-p			-74		dBc
Third-Order Intercept	IP3	f = 10MHz, V_{OUT} = 2Vp-p			36		dBm

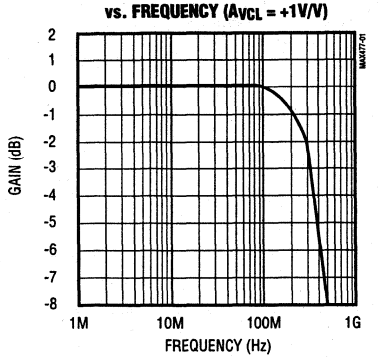
Note 1: Full-power bandwidth is inferred from slew-rate test.

Note 2: Tested with a 3.58MHz video test signal with an amplitude of 40IRE superimposed on a linear ramp (0 to 100IRE). An IRE is a unit of video-signal amplitude developed by the Institute of Radio Engineers. 140IRE = 1V.

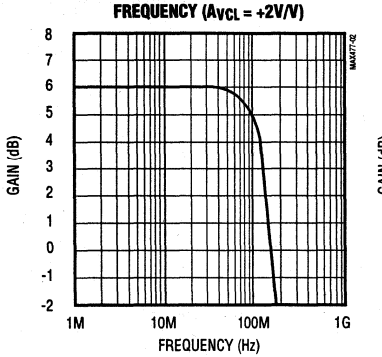
Typical Operating Characteristics

(V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, C_L = 0pF, T_A = +25°C, unless otherwise noted.)

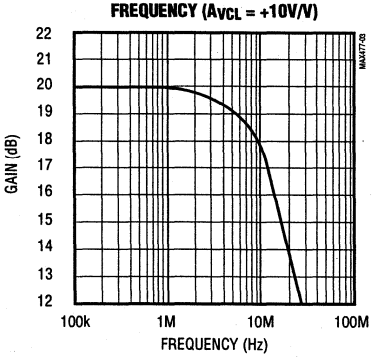
SMALL-SIGNAL GAIN vs. FREQUENCY (A_{VCL} = +1V/V)



SMALL-SIGNAL GAIN vs. FREQUENCY (A_{VCL} = +2V/V)



SMALL-SIGNAL GAIN vs. FREQUENCY (A_{VCL} = +10V/V)

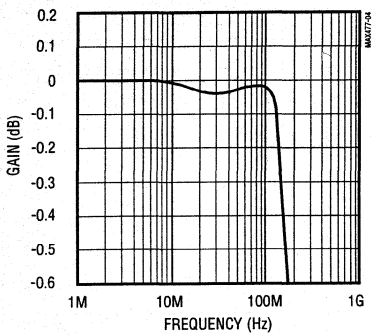


300MHz High-Speed Op Amp

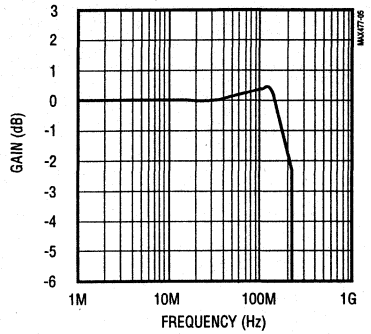
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, C_L = 0pF, T_A = +25°C, unless otherwise noted.)

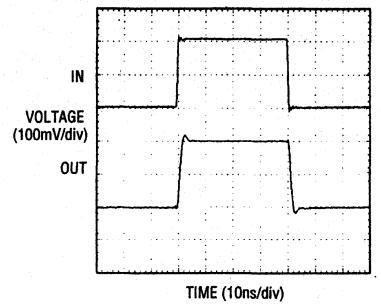
GAIN FLATNESS vs. FREQUENCY (A_{VCL} = +1V/V)



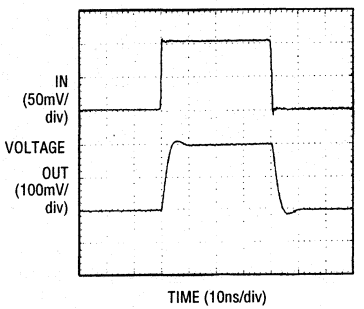
LARGE-SIGNAL GAIN vs. FREQUENCY (A_{VCL} = +1V/V)



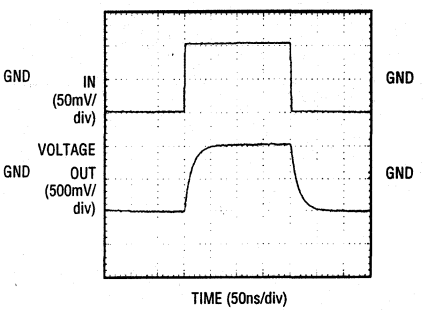
SMALL-SIGNAL PULSE RESPONSE (A_{VCL} = +1V/V)



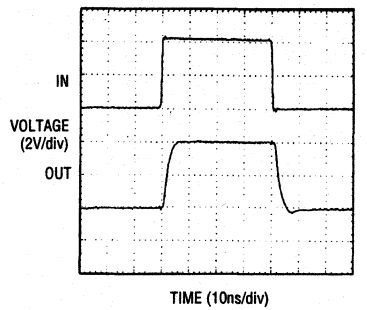
SMALL-SIGNAL PULSE RESPONSE (A_{VCL} = +2V/V)



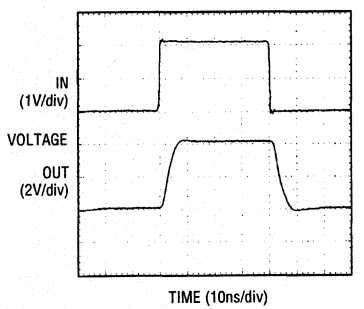
SMALL-SIGNAL PULSE RESPONSE (A_{VCL} = +10V/V)



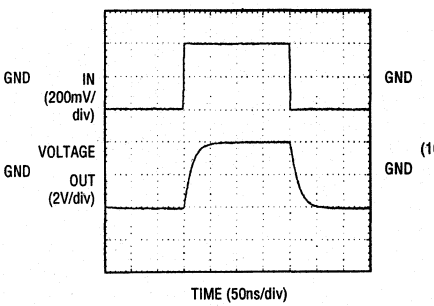
LARGE-SIGNAL PULSE RESPONSE (A_{VCL} = +1V/V)



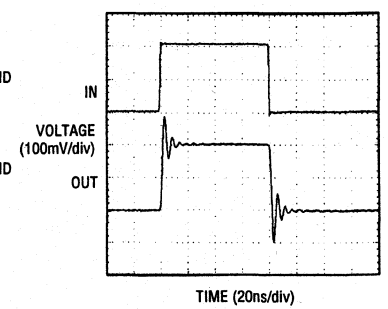
LARGE-SIGNAL PULSE RESPONSE (A_{VCL} = +2V/V)



LARGE-SIGNAL PULSE RESPONSE (A_{VCL} = +10V/V)



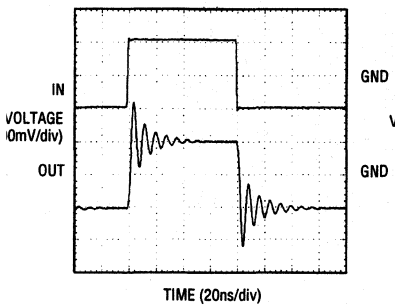
SMALL-SIGNAL PULSE RESPONSE (A_{VCL} = +1V/V, C_L = 50pF)



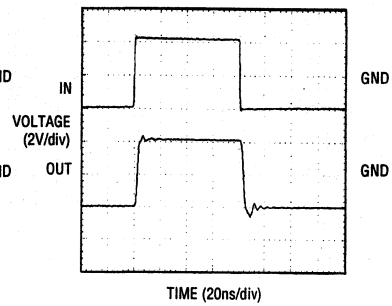
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, C_L = 0pF, T_A = +25°C, unless otherwise noted.)

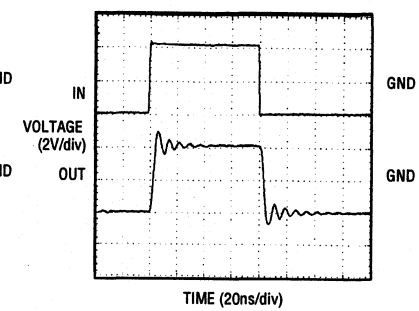
SMALL-SIGNAL PULSE RESPONSE (A_{VCL} = +1V/V, C_L = 100pF)



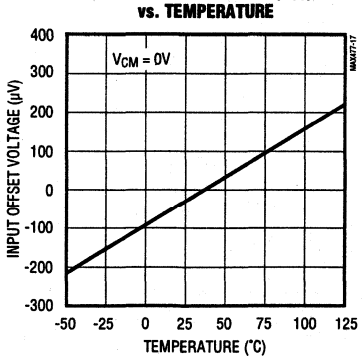
LARGE-SIGNAL PULSE RESPONSE (A_{VCL} = +1V/V, C_L = 50pF)



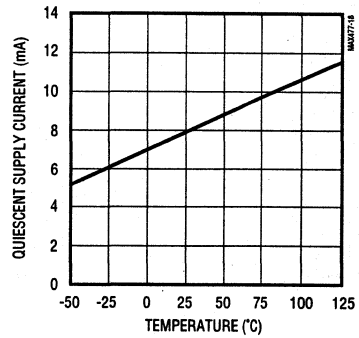
LARGE-SIGNAL PULSE RESPONSE (A_{VCL} = +1V/V, C_L = 100pF)



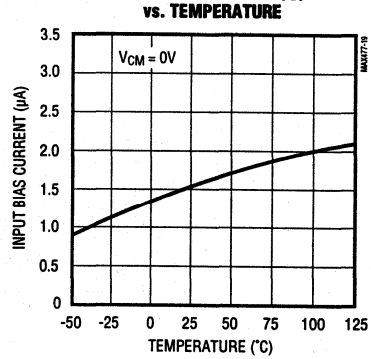
INPUT OFFSET VOLTAGE (V_{OS}) vs. TEMPERATURE



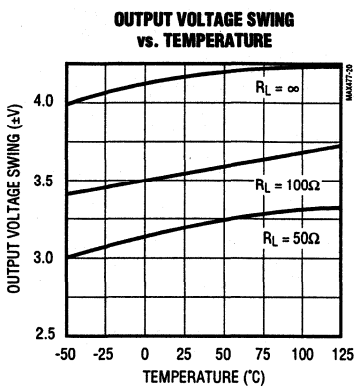
QUIESCENT SUPPLY CURRENT (I_{SY}) vs. TEMPERATURE



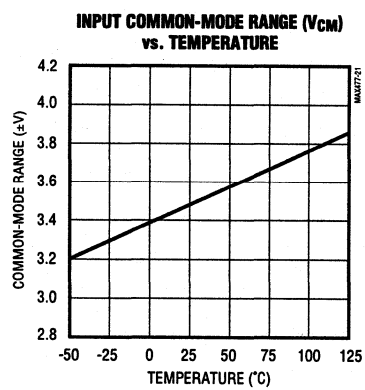
INPUT BIAS CURRENT (I_B) vs. TEMPERATURE



OUTPUT VOLTAGE SWING vs. TEMPERATURE



INPUT COMMON-MODE RANGE (V_{CM}) vs. TEMPERATURE

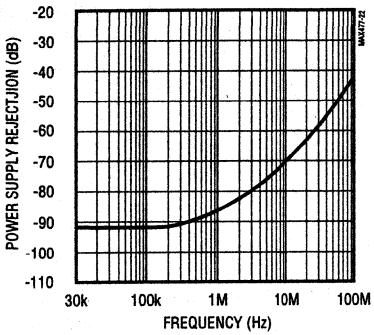


300MHz High-Speed Op Amp

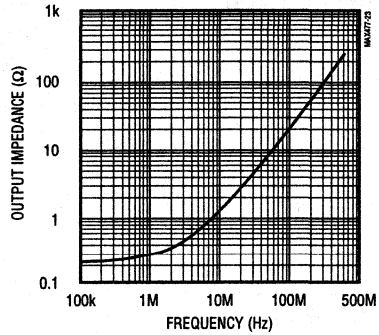
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, C_L = 0pF, T_A = +25°C, unless otherwise noted.)

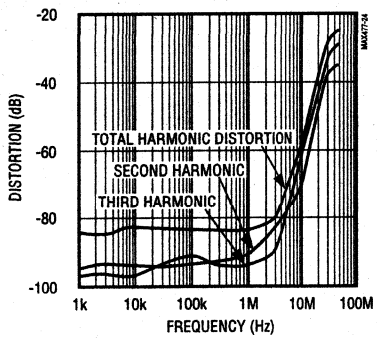
POWER-SUPPLY REJECTION vs. FREQUENCY



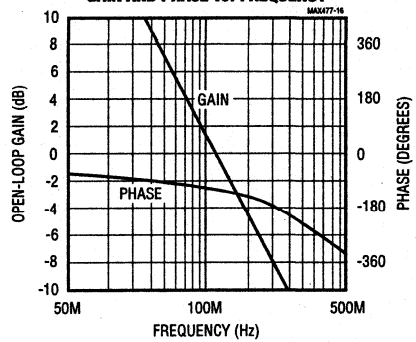
OUTPUT IMPEDANCE vs. FREQUENCY



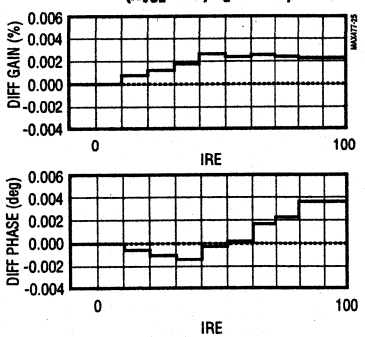
HARMONIC DISTORTION vs. FREQUENCY



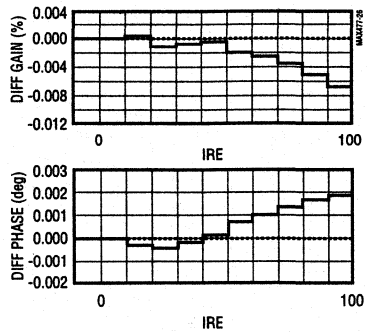
OPEN-LOOP GAIN AND PHASE vs. FREQUENCY



DIFFERENTIAL GAIN AND PHASE (A_{VCL} = +1, R_L = 150Ω)



DIFFERENTIAL GAIN AND PHASE (A_{VCL} = +2, R_L = 150Ω)



Pin Description

PIN	NAME	FUNCTION
1, 5, 8	N.C.	No Connect. Not internally connected.
2	IN-	Inverting Input
3	IN+	Noninverting Input
4	V_{EE}	Negative Power Supply
6	OUT	Amplifier Output
7	V_{CC}	Positive Power Supply

Detailed Description

The MAX477 allows the flexibility and ease of a classic voltage-feedback architecture while maintaining the high-speed benefits of current-mode feedback (CMF) amplifiers. Although the MAX477 is a voltage-feedback op amp, its internal architecture provides an 1100V/µs slew rate and a low 8mA supply current. CMF amplifiers offer high slew rates while maintaining low supply current, but use the feedback and load resistors as part of the amplifier's frequency compensation network. In addition, they have only one input with high impedance.

The MAX477 has speed and power specifications like those of current-feedback amplifiers, but has high input impedance at both input terminals. Like other voltage-feedback op amps, its frequency compensation is independent of the feedback and load resistors, and it exhibits a constant gain-bandwidth product. However, unlike standard voltage-feedback amplifiers, its large-signal slew rate is not limited by an internal current source, so the MAX477 exhibits a very high full-power bandwidth.

Output Short-Circuit Protection

Under short-circuit conditions, the output current is typically limited to 150mA. This is low enough that a short to ground of any duration will not cause permanent damage to the chip. However, a short to either supply will significantly increase the power dissipation and may cause permanent damage. The high output-current capability is an advantage in systems that transmit a signal to several loads. See *High-Performance Video Distribution Amplifier* in the *Applications Information* section.

Applications Information

Grounding, Bypassing, and PC Board Layout

To obtain the MAX477's full 300MHz bandwidth, Microstrip and Stripline techniques are recommended in most cases. To ensure the PC board does not degrade the amplifier's performance, design the board for a frequency greater than 1GHz. Even with very short traces, use these techniques at critical points, such as inputs and outputs. Whether you use a constant-impedance board or not, observe the following guidelines when designing the board:

- Do not use wire-wrap boards. They are too inductive.
- Do not use IC sockets. They increase parasitic capacitance and inductance.
- In general, surface-mount components have shorter leads and lower parasitic reactance, giving better high-frequency performance than through-hole components.
- The PC board should have at least two layers, with one side a signal layer and the other a ground plane.
- Keep signal lines as short and straight as possible. Do not make 90° turns; round all corners.
- The ground plane should be as free from voids as possible.

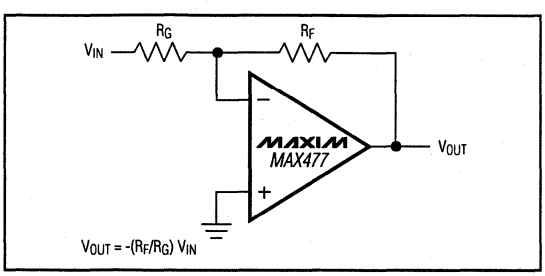


Figure 1a. Inverting Gain Configuration

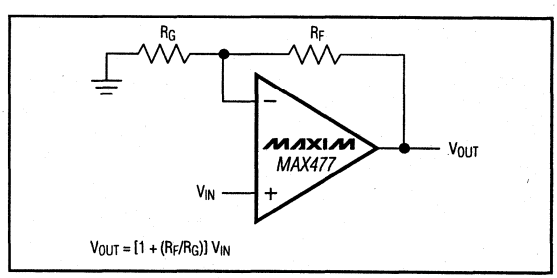


Figure 1b. Noninverting Gain Configuration

300MHz High-Speed Op Amp

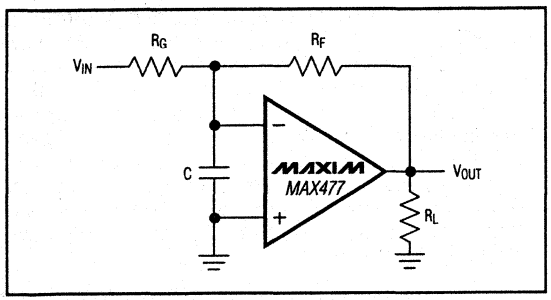


Figure 2. Effect of High-Feedback Resistor Values and Parasitic Capacitance on Bandwidth

Setting Gain

The MAX477 can be configured as an inverting or noninverting gain block in the same manner as any other voltage-feedback op amp. The gain is determined by the ratio of two resistors and does not affect amplifier frequency compensation. This is unlike CMF op amps, which have a limited range of feedback resistors, typically one resistor value for each gain and load setting. This is because the -3dB bandwidth of a CMF op amp is set by the feedback and load resistors. Figure 1a shows the inverting gain configuration and its gain equation, while Figure 1b shows the noninverting gain configuration.

Choosing Resistor Values

The feedback and input resistor values are not critical in the inverting or noninverting gain configurations (as with current-feedback amplifiers). However, be sure to select resistors that are small and noninductive.

Surface-mount resistors are best for high-frequency circuits. Their material is similar to that of metal-film resistors, but to minimize inductance, it is deposited in a flat, linear manner using a thick film. Their small size and lack of leads also minimize parasitic inductance and capacitance.

The MAX477's input capacitance is approximately 1pF. In either the inverting or noninverting configuration, excess phase resulting from the pole frequency formed by $R_f \parallel R_g$ and C can degrade amplifier phase margin and cause oscillations (Figure 2). Table 1 shows the recommended resistor combinations and measured bandwidth for several gain values.

DC and Noise Errors

The standard voltage-feedback topology of the MAX477 allows DC error and noise calculations to be done in the usual way. The following analysis shows

Table 1. Resistor and Bandwidth Values for Various Closed-Loop Gain Configurations

GAIN (V/V)	Rg (Ω)	Rf (Ω)	-3dB BANDWIDTH (MHz)
+1	Open	Short	300
+2	500	500	120
+5	125	500	25
+10	50	450	12
-1	300	300	114
-2	150	300	64
-5	100	500	42
-10	50	500	23

that the MAX477's voltage-feedback architecture provides a precision amplifier with significantly lower DC errors and lower noise compared to CMF amplifiers.

1) In Figure 3, total output offset error is given by:

$$V_{OUT} = \left[1 + \frac{R_f}{R_g}\right] \left[V_{OS} + I_B R_S - I_B\left(R_f \parallel R_g\right) + I_{OS}\left(R_S + \left(R_f \parallel R_g\right)\right)\right]$$

For the special case in which R_S is arranged to be equal to $R_f \parallel R_g$, the I_B terms cancel out. Note also, for I_{OS} ($R_S + (R_f \parallel R_g) << V_{OS}$, the I_{OS} term also drops out of the equation for total DC error. In practice, high-speed configurations for the MAX477 necessitate the use of low-value resistors for R_S, R_f, and R_g. In this case, the V_{OS} term is the dominant DC error source.

2) The MAX477's total input-referred noise in a closed-loop feedback configuration can be calculated by:

$$e_T = \sqrt{\left[e_n^2 + e_R^2 + \left(i_n R_{EQ}\right)^2\right]}$$

where e_n = input-referred noise voltage of the MAX477 ($5nV\sqrt{Hz}$)

i_n = input-referred noise current of the MAX477 ($2pA\sqrt{Hz}$)

R_{EQ} = total equivalent source resistance at the two inputs, i.e., $R_{EQ} = R_S + R_f \parallel R_g$

e_R = resistor noise voltage due to R_{EQ}, i.e.,

$$e_R = \sqrt{4KT\,R_{EQ}}$$

As an example, consider $R_S = 75\Omega$, $R_f = R_g = 500\Omega$. Then:

$$R_{EQ} = 75\Omega + (500\Omega \,||\, 500\Omega) = 325\Omega$$

$$e_R = \sqrt{4KT \times 325} = 2.3nV/\sqrt{Hz} \text{ at } 25°C$$

$$e_T = \sqrt{(5nV)^2 + (2.3nV)^2 + (2pA \times 325)^2} = 5.5nV\sqrt{Hz}$$

3) The MAX477's output-referred noise is simply total input-referred noise, e_T, multiplied by the gain factor:

$$e_{OUT} = e_T \left[1 + \frac{R_f}{R_g}\right]$$

In the above example, with $e_T = 5.5nV\sqrt{Hz}$, and assuming a signal bandwidth of 300MHz (471MHz noise bandwidth), total output noise in this bandwidth is:

$$e_{OUT} = 5.5nV \times \left[1 + \frac{500}{500}\right] \times \sqrt{471MHz} = 239\mu V_{RMS}$$

Note that for both DC and noise calculations, errors are dominated by offset voltage (V_{OS}) and input noise voltage (e_n). For a current-mode feedback amplifier with offset and noise errors significantly higher, the calculations are very different.

Driving Capacitive Loads

The MAX477 provides maximum AC performance with no output load capacitance. This is the case when the MAX477 is driving a correctly terminated transmission line (i.e., a back-terminated 75Ω cable). However, the MAX477 is capable of driving capacitive loads up to 100pF without oscillations, but with reduced AC performance.

Driving large capacitive loads increases the chance of oscillations in most amplifier circuits. This is especially true for circuits with high loop gain, such as voltage followers. The amplifier's output resistance and the load capacitor combine to add a pole and excess phase to the loop response. If the frequency of this pole is low enough and phase margin is degraded sufficiently, oscillations may occur.

A second problem when driving capacitive loads results from the amplifier's output impedance, which looks inductive at high frequency. This inductance forms an L-C resonant circuit with the capacitive load, which causes peaking in the frequency response and degrades the amplifier's gain margin.

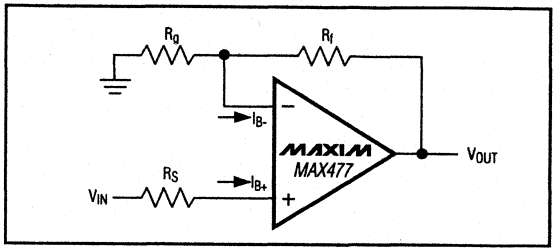


Figure 3. Output Offset Voltage

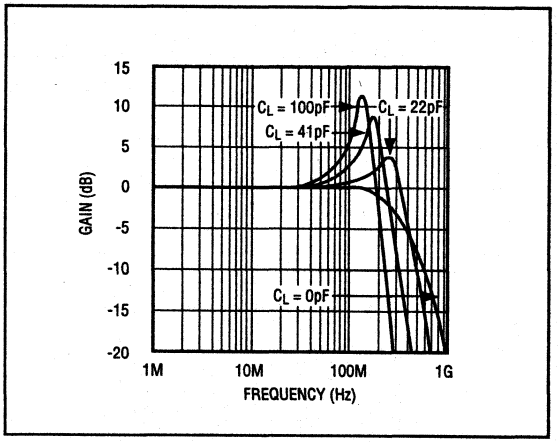


Figure 4. Effect of C_{LOAD} on Frequency Response (A_{VCL} = +1V/V)

The MAX477 drives capacitive loads up to 100pF without oscillation. However, some peaking (in the frequency domain) or ringing (in the time domain) may occur. This is shown in Figure 4 and the in the Small and Large-Signal Pulse Response graphs in the *Typical Operating Characteristics*.

To drive larger-capacitance loads or to reduce ringing, add an isolation resistor between the amplifier's output and the load, as shown in Figure 5.

The value of R_{ISO} depends on the circuit's gain and the capacitive load. Figure 6 shows the Bode plots that result when a 20Ω isolation resistor is used with a voltage follower driving a range of capacitive loads. At the higher capacitor values, the bandwidth is dominated by the RC network, formed by R_{ISO} and C_L; the bandwidth of the amplifier itself is much higher. Note that adding an isolation resistor degrades gain accuracy. The load and isolation resistor form a divider that decreases the voltage delivered to the load.

300MHz High-Speed Op Amp

Flash ADC Preamp

The MAX477's high output-drive capability and ability to drive capacitive loads make it well suited for buffering the low-impedance input of a high-speed flash ADC. With its low output impedance, the MAX477 can drive the inputs of the ADC while maintaining accuracy. Figure 7 shows a preamp for digitizing video, using the 250Msps MAX100 and the 500Msps MAX101 flash ADCs. Both of these ADCs have a 50Ω input resistance and a 1.2GHz input bandwidth.

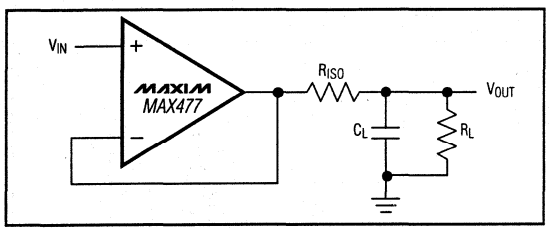


Figure 5. Capacitive-Load Driving Circuit

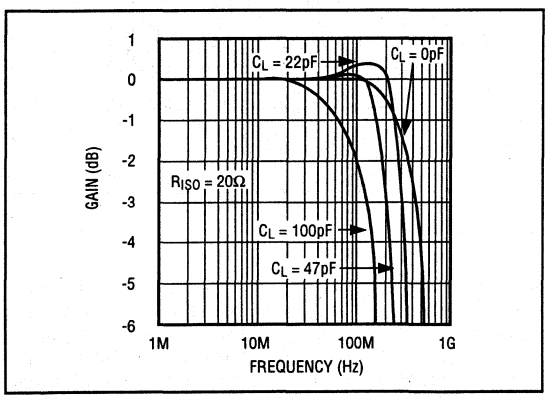


Figure 6. Effect of C_{LOAD} on Frequency Response With Isolation Resistor

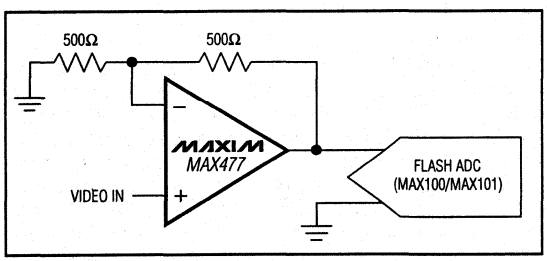


Figure 7. Preamp for Video Digitizer

High-Performance Video Distribution Amplifier

In a gain of +2 configuration, the MAX477 makes an excellent driver for back-terminated 75Ω video coaxial cables (Figure 8). The high output-current drive allows the attachment of up to six ±2Vp-p, 150Ω loads to the MAX477 at +25°C. With the output limited to ±1Vp-p, the number of loads may double. The MAX4278 is a similar amplifier configured for a gain of +2 without the need for external gain-setting resistors. For multiple gain-of-2 video line drivers in a single package, see the MAX496/MAX497 data sheet.

Wide-Bandwidth Bessel Filter

Two high-impedance inputs allow the MAX477 to be used in all standard active filter topologies. The filter design is straightforward because the component values can be chosen independently of op amp bias. Figure 9 shows a wide-bandwidth, second-order Bessel filter using a multiple feedback topology. The component values are chosen for a gain of +2, a -3dB bandwidth of 10MHz, and a 28ns delay. Figure 10a shows a square-wave pulse response, and Figure 10b shows the filter's frequency response and delay. Notice the flat delay in the passband, which is characteristic of the Bessel filter.

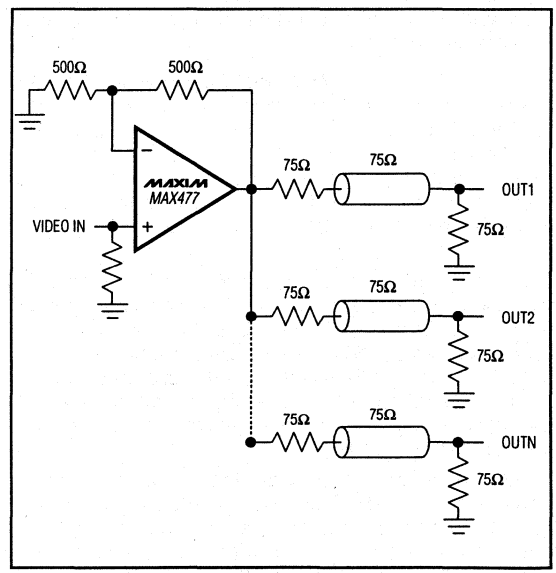


Figure 8. High-Performance Video Distribution Amplifier

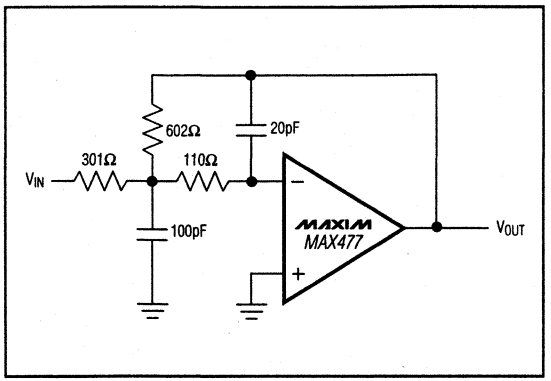


Figure 9. 8MHz Bessel Filter

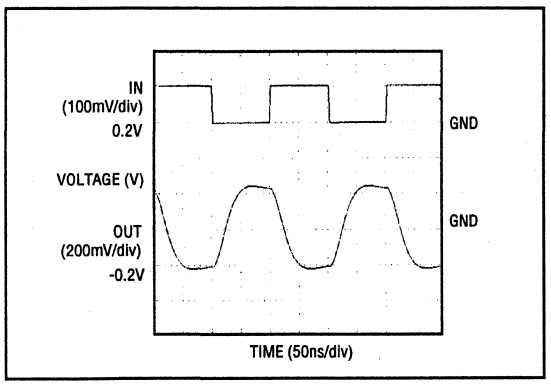


Figure 10a. 5MHz Square Wave Input

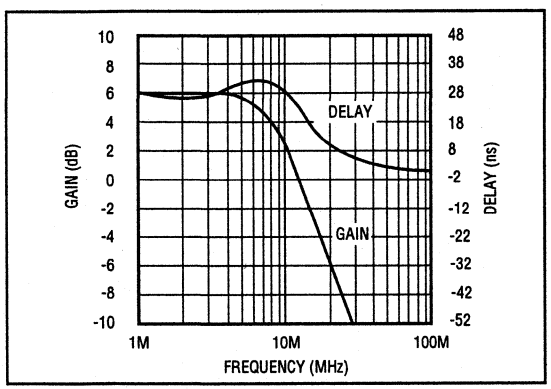


Figure 10b. Gain and Delay vs. Frequency

Chip Information

TRANSISTOR COUNT: 175

SUBSTRATE CONNECTED TO V_{EE}

19-0373; Rev 0; 12/95

EVALUATION KIT AVAILABLE

MAXIM

375MHz Quad Closed-Loop Video Buffers, AV = +1 and +2

General Description

The MAX496 and MAX497 are quad, closed-loop, ±5V video buffers that feature extremely high bandwidth and slew rate for both component video (RGB or YUV) and composite video (NTSC, PAL, SECAM). The MAX496 is a unity-gain (0dB) buffer with a 375MHz -3dB bandwidth and a 1600V/µs slew rate. The MAX497 gain of +2 (6dB) buffer, optimized for driving back-terminated coaxial cable, features a 275MHz -3dB bandwidth and a 1500V/µs slew rate. The MAX496/MAX497 are not slew-rate limited, thus providing a high full-power bandwidth of 230MHz and 215MHz, respectively.

The MAX496/MAX497 incorporate a unique two-stage architecture that combines the low offset and noise benefits of voltage feedback with the high bandwidth and slew-rate advantages of current-mode-feedback.

Applications

Computer Workstations

Surveillance Video

Broadcast and High-Definition TV Systems

Multimedia Products

Medical Imaging

High-Speed Signal Processing

Video Switching and Routing

Features

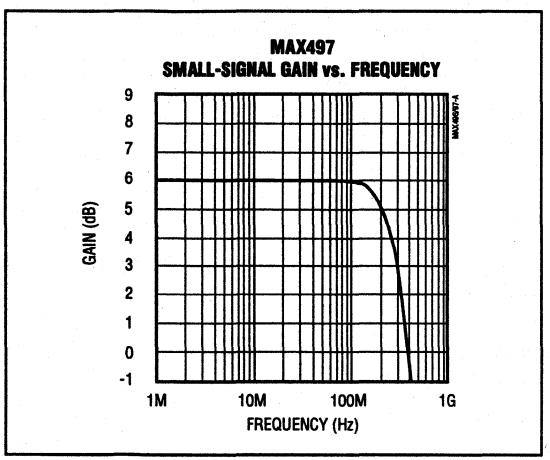
- **MAX496 Fixed Gain: +1V/V**
  MAX497 Fixed Gain: +2V/V
- **High Speed:**
  Small-Signal -3dB Bandwidth: 375MHz (MAX496)
  275MHz (MAX497)
  Full-Power -3dB Bandwidth: 230MHz (MAX496)
  215MHz (MAX497)
- **0.1dB Gain Flatness: 65MHz (MAX496)**
  120MHz (MAX497)
- **1600V/µs Slew Rate (MAX496)**
  1500V/µs Slew Rate (MAX497)
- **Fast Settling Time: 12ns to 0.1%**
- **Lowest Differential Phase/Gain Error: 0.01°/0.01%**
- **2pF Input Capacitance**
- **5.6nV/√Hz Input-Referred Voltage Noise**
- **Low Distortion: 64dBc (f = 10MHz)**
- **Directly Drives 50Ω or 75Ω Back-Terminated Cables**
- **High ESD Protection: 5000V**
- **Output Short-Circuit Protected**

Ordering Information

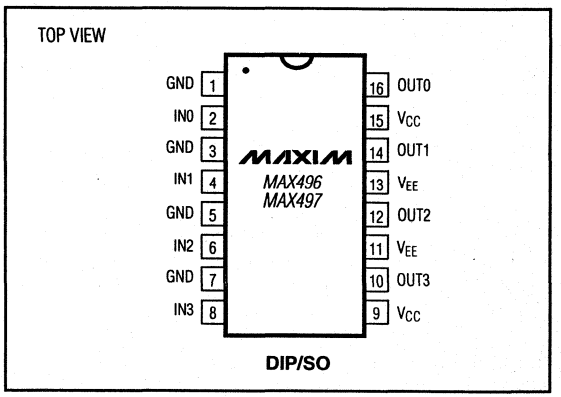
PART	TEMP. RANGE	PIN-PACKAGE
MAX496CPE	0°C to +70°C	16 Plastic DIP
MAX496CSE	0°C to +70°C	16 Narrow SO
MAX496C/D	0°C to +70°C	Dice*
MAX497CPE	0°C to +70°C	16 Plastic DIP
MAX497CSE	0°C to +70°C	16 Narrow SO
MAX497C/D	0°C to +70°C	Dice*

** Dice are specified at T_A = +25°C, DC parameters only.*

Frequency Response



Pin Configuration



8

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

375MHz Quad Closed-Loop Video Buffers, AV = +1 and +2

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to V_{EE}) 12V
Voltage on Any Input Pin to GND ....(V_{CC} + 0.3V) to (V_{EE} - 0.3V)
Output Short-Circuit Current Duration 60sec
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
Narrow SO (derate 8.70mW/°C above +70°C) 696mW

Operating Temperature Range.....0°C to +70°C
Storage Temperature Range.....-65°C to +150°C
Lead Temperature (soldering, 10sec).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, V_{IN} = 0V, R_L = 150Ω, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}	MAX496		±2.8	±3.2		V
		MAX497		±1.4	±1.6		
Input Offset Voltage	V_{OS}	V_{OUT} = 0V			±1	±3	mV
Input Offset Voltage Drift	TCV_{OS}	V_{OUT} = 0V			-10		µV/°C
Input Bias Current	I_B	V_{OUT} = 0V			±1	±5	µA
Input Resistance	R_{IN}	MAX496: -2V ≤ V_{IN} ≤ +2V, MAX497: -1V ≤ V_{IN} ≤ +1V		0.5	1.2		MΩ
Input Capacitance	C_{IN}				2		pF
Voltage Gain	A_V	MAX496 (Note 1)	R_L = 150Ω	0.988		1.00	V/V
			R_L = 50Ω	0.983		1.00	
		MAX497 (Note 2)	R_L = 150Ω	1.975		2.01	
			R_L = 50Ω	1.965		2.01	
Positive Power-Supply Rejection Ratio (Change in V_{OS})	PSRR+	V_{CC} = ±4.5V to ±5.5V, V_{EE} = -5.0V		55	74		dB
Negative Power-Supply Rejection Ratio (Change in V_{OS})	PSRR-	V_{EE} = ±4.5V to ±5.5V, V_{CC} = 5.0V		60	78		dB
Gain Linearity	A_{VLIN}	A_{VCL} = +2, V_{OUT} = ±1mV to ±2V			0.01		%
Positive Quiescent Supply Current (Total)	I_{SY+}	T_A = +25°C			31	36	mA
		T_A = T_{MIN} to T_{MAX}				45	
Negative Quiescent Supply Current (Total)	I_{SY-}	T_A = +25°C			32	37	mA
		T_A = T_{MIN} to T_{MAX}				45	
Operating Supply Voltage Range	V_S			±4.50		±5.50	V
Output Voltage Swing	V_{OUT}	R_L = 150Ω		±2.8	±3.7		V
		R_L = 50Ω		±2.5	±3.3		
Output Resistance	R_{OUT}	DC			0.1		Ω
Output Impedance	Z_{OUT}	f = 10MHz			1.5		Ω
Short-Circuit Output Current	I_{SC}	Short to ground or either supply voltage			170		mA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, V_{IN} = 0V, R_L = 100Ω, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Small-Signal -3dB Bandwidth	BW_{-3dB}	MAX496CSE		280	375		MHz
		MAX496CPE			375		
		MAX497CSE		280	275		
		MAX497CPE			275		
Full-Power Bandwidth	FPBW	V_{OUT} = ±2V	MAX496		230		MHz
			MAX497		215		
Slew Rate	SR	V_{OUT} = 4V step, MAX496		1150	1600		V/µs
		V_{OUT} = 4V step, MAX497		1100	1500		
Settling Time	t_S	0.1% (V_{OUT} = 2V step)			12		ns
Differential Gain Error	DG	f = 3.58MHz (Note 3)			0.01		%
Differential Phase Error	DP	f = 3.58MHz (Note 3)			0.01		degrees
Input Noise Voltage Density		f = 10MHz			5.6		$nV\sqrt{Hz}$
Input Noise Current Density		f = 10MHz			2		$pA\sqrt{Hz}$
Gain Flatness		±0.1dB	MAX496CPE		80		MHz
			MAX496CSE	50	80		
			MAX497CPE		100		
			MAX497CSE	55	120		
Adjacent Channel Crosstalk		(Note 4)	MAX496		78		dB
			MAX497		72		
All-Hostile Crosstalk		(Note 4)	MAX496		72		dB
			MAX497		65		
Total Harmonic Distortion	THD	f_C = 10MHz, V_{OUT} = 2Vp-p	MAX496		-64		dBc
			MAX497		-58		
Spurious-Free Dynamic Range	SFDR	f_C = 5MHz	MAX496		58		dBc
			MAX497		60		

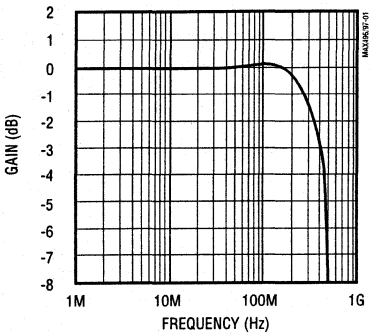
Note 1: Voltage Gain = (V_{OUT} - V_{OS}) / V_{IN}, measured at V_{IN} = ±1V.
Note 2: Voltage Gain = (V_{OUT} - V_{OS}) / V_{IN}, measured at V_{IN} = ±2V.
Note 3: Input test signal is a 3.58MHz sine wave of amplitude 40 IRE superimposed on a linear ramp (0 IRE to 100 IRE). R_L = 150Ω, see Figure 2.
Note 4: Input of channel under test grounded through 75Ω. Adjacent channel driven at f = 10MHz (Figure 4a). For All-Hostile Crosstalk, all inputs are driven except the channel under test (Figure 4b).

375MHz Quad Closed-Loop Video Buffers, AV = +1 and +2

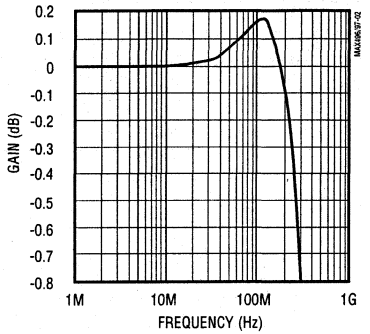
Typical Operating Characteristics

(V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

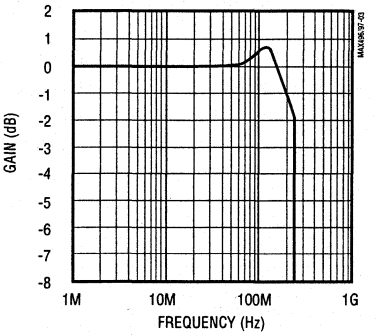
MAX496
SMALL-SIGNAL GAIN vs. FREQUENCY



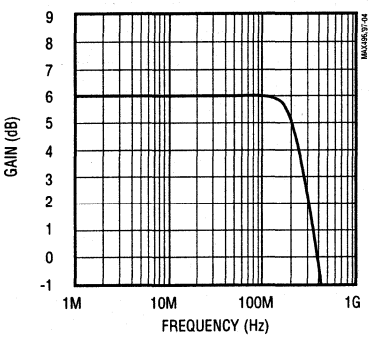
MAX496
GAIN FLATNESS vs. FREQUENCY



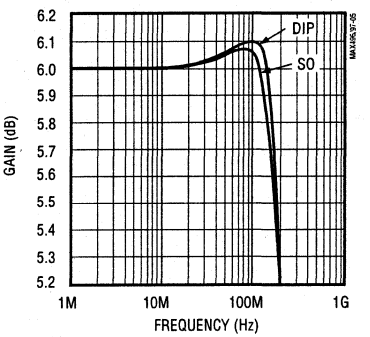
MAX496
LARGE-SIGNAL GAIN vs. FREQUENCY



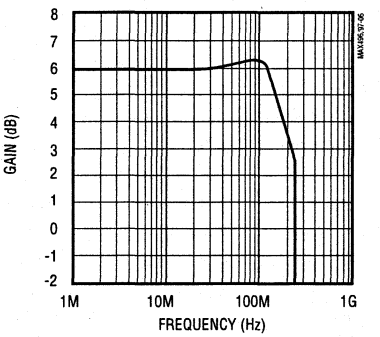
MAX497
SMALL-SIGNAL GAIN vs. FREQUENCY



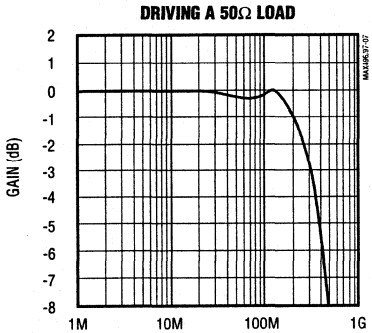
MAX497
GAIN FLATNESS vs. FREQUENCY



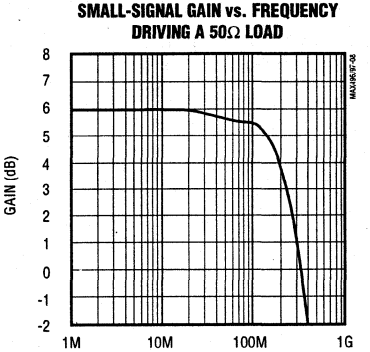
MAX497
LARGE-SIGNAL GAIN vs. FREQUENCY



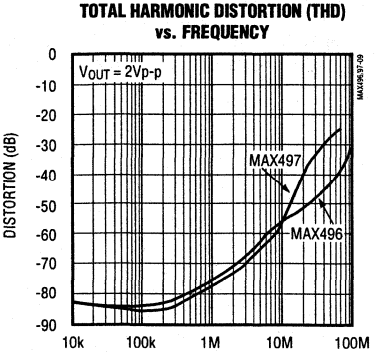
MAX496
SMALL-SIGNAL GAIN vs. FREQUENCY
DRIVING A 50Ω LOAD



MAX497
SMALL-SIGNAL GAIN vs. FREQUENCY
DRIVING A 50Ω LOAD



TOTAL HARMONIC DISTORTION (THD)
vs. FREQUENCY

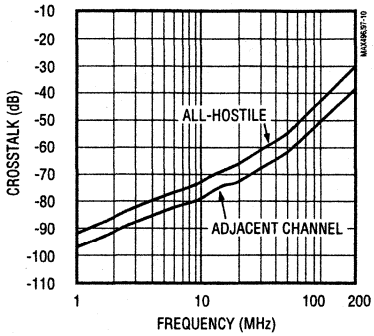


375MHz Quad Closed-Loop Video Buffers, AV = +1 and +2

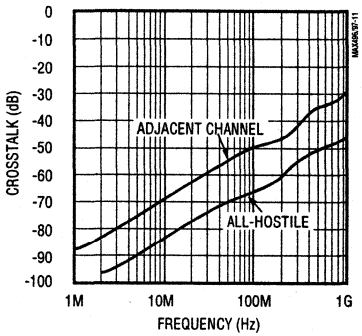
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

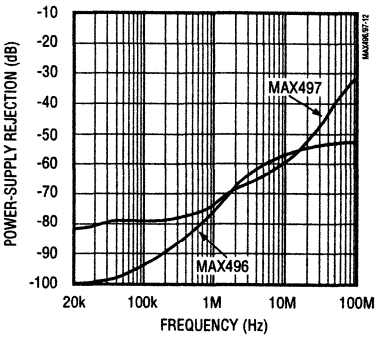
MAX496 CROSSTALK vs. FREQUENCY



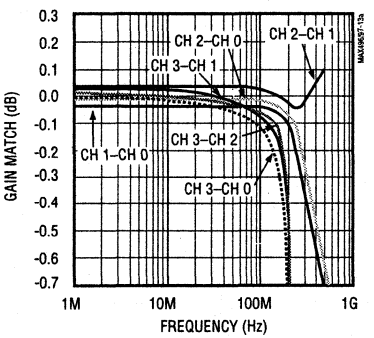
MAX497 CROSSTALK vs. FREQUENCY



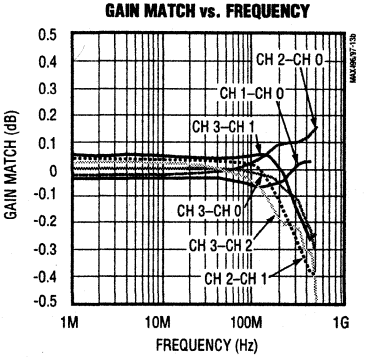
POWER-SUPPLY REJECTION (PSR) vs. FREQUENCY



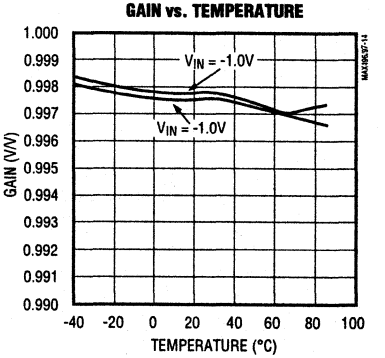
MAX496 GAIN MATCH vs. FREQUENCY



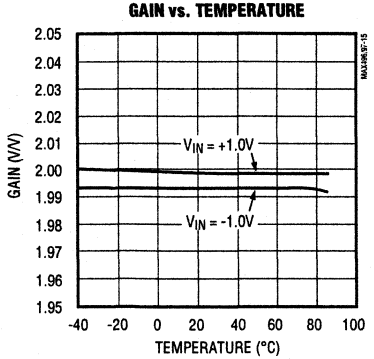
MAX497 GAIN MATCH vs. FREQUENCY



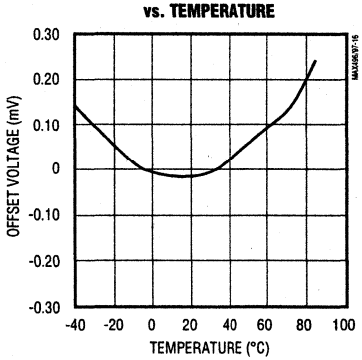
MAX496 GAIN vs. TEMPERATURE



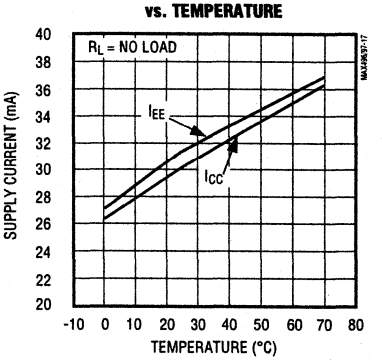
MAX497 GAIN vs. TEMPERATURE



INPUT OFFSET VOLTAGE vs. TEMPERATURE



SUPPLY CURRENT vs. TEMPERATURE



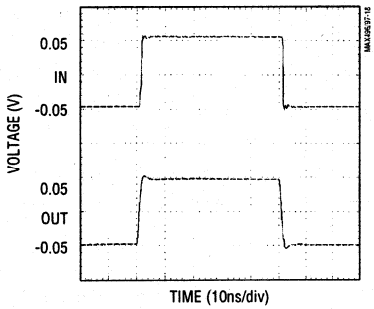
8

375MHz Quad Closed-Loop Video Buffers, AV = +1 and +2

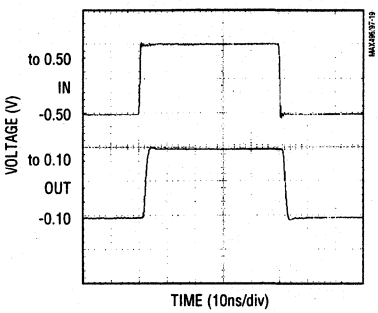
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

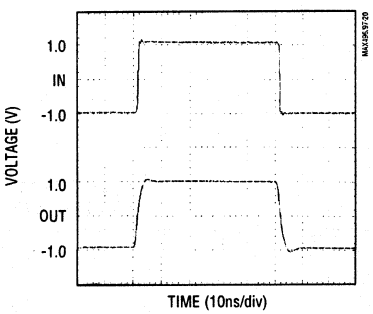
MAX496
SMALL-SIGNAL PULSE RESPONSE



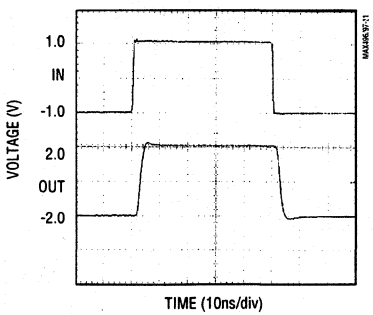
MAX497
SMALL-SIGNAL PULSE RESPONSE



MAX496
LARGE-SIGNAL PULSE RESPONSE



MAX497
LARGE-SIGNAL PULSE RESPONSE

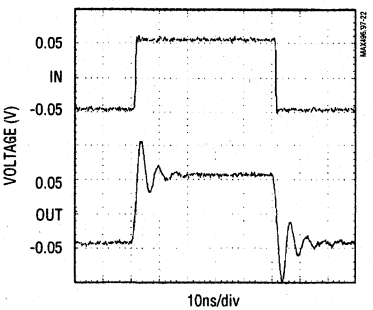


375MHz Quad Closed-Loop Video Buffers, AV = +1 and +2

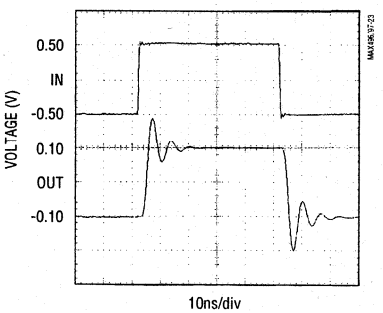
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

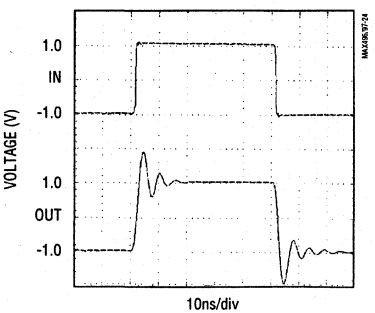
MAX496
SMALL-SIGNAL PULSE RESPONSE
(C_L = 47pF



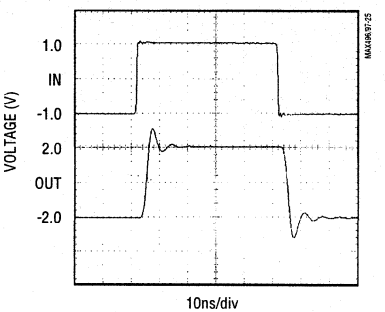
MAX497
SMALL-SIGNAL PULSE RESPONSE
(C_L = 47pF)



MAX496
LARGE-SIGNAL PULSE RESPONSE
(C_L = 47pF)



MAX497
LARGE-SIGNAL PULSE RESPONSE
(C_L = 47pF)



375MHz Quad Closed-Loop Video Buffers, AV = +1 and +2

Pin Description

PIN	NAME	FUNCTION
1, 3, 5, 7	GND	Ground. All ground pins are internally connected. Connect all ground pins externally to minimize the ground impedance.
2	IN0	Channel 0 Input
4	IN1	Channel 1 Input
6	IN2	Channel 2 Input
8	IN3	Channel 3 Input
9, 15	VCC	Positive Power Supply. Connect to +5V. VCC pins are internally connected. Connect both pins to +5V externally to minimize the supply impedance.
10	OUT3	Channel 3 Output
11, 13	VEE	Negative power supply. Connect to -5V. VEE pins are internally connected. Connect both pins to -5V externally to minimize the supply impedance.
12	OUT2	Channel 2 Output
14	OUT1	Channel 1 Output
16	OUT0	Channel 0 Output

Detailed Description

The MAX496/MAX497 are quad, high-speed, closed-loop voltage-feedback video amplifiers with fixed gain settings of +1 and +2, respectively (Figure 1). These amplifiers use a unique two-stage voltage-feedback architecture that combines the benefits of conventional voltage-feedback and current-mode-feedback topologies. They achieve wide bandwidths and high slew rates while maintaining precision. A resistively loaded first stage provides low input-referred noise even with low supply currents of 8mA per amplifier. The above features, along with the ability to drive 50Ω or 75Ω back-terminated cables to ±2.8V and low differential phase and gain errors, make these amplifiers ideal for the most demanding component and composite video applications.

Applications Information

The feedback elements of the MAX496/MAX497 are included internally in the device to set the closed-loop gain to AV = +1 and AV = +2, respectively. Closing the loop internally on the chip minimizes problems associated with the board and package parasitics influencing the amplifier's frequency response.

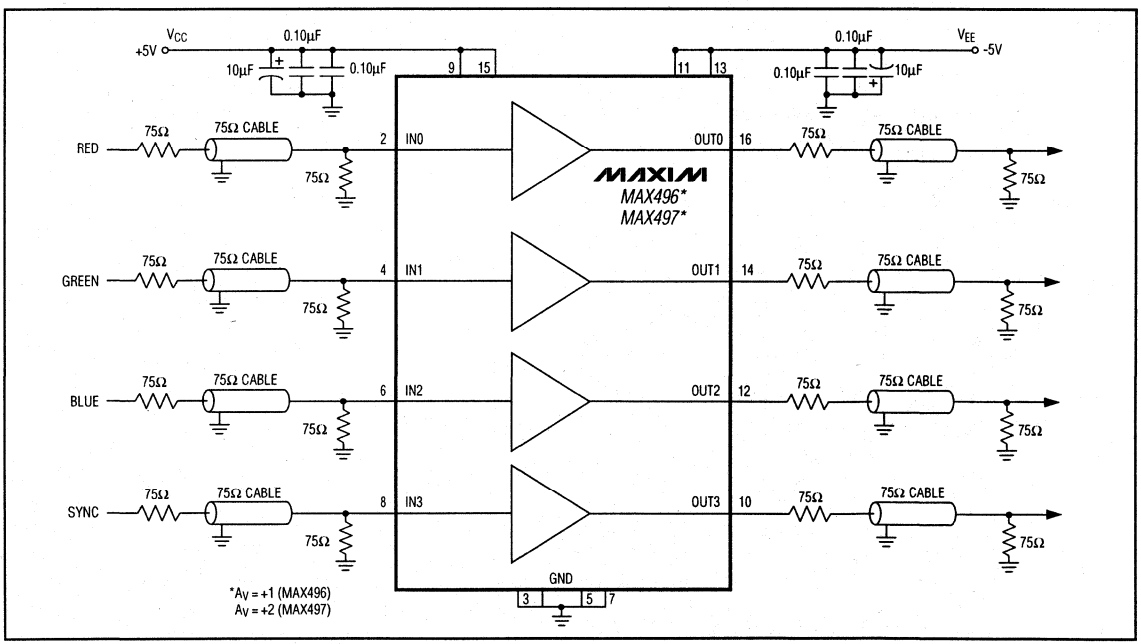


Figure 1. Typical Operating Circuit

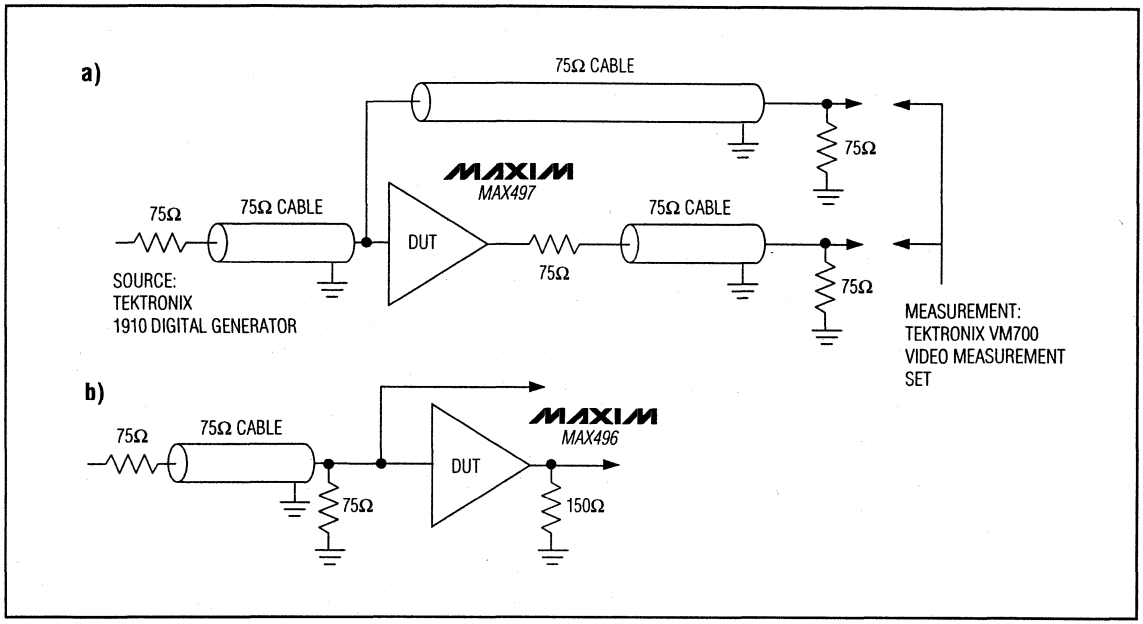


Figure 2. Differential Phase and Gain Error Test Circuits: a) MAX497, Gain of +2 Amplifier; b) MAX496 Unity-Gain Amplifier

Power Dissipation

The maximum output current of the MAX496/MAX497 is limited by the packages maximum allowable power dissipation. The maximum junction temperature should not exceed +150°C. The power dissipation increases with load, and this increase can be approximated by the following:

For $V_{OUT} > 0V$: $|V_{CC} - V_{OUT}| I_{LOAD}$

OR

For $V_{OUT} < 0V$: $|V_{EE} - V_{OUT}| I_{LOAD}$.

These devices can drive 100Ω loads connected to each of the outputs over the entire rated output swing and temperature range. When driving 50Ω loads with each of the four outputs simultaneously, the output swing must be limited to ±1.25V at T_A = +70°C. While the output is short-circuit protected to 170mA, this does not necessarily guarantee that, under all conditions, the maximum junction temperature will not be exceeded. Do not exceed the derating values given in the absolute maximum ratings.

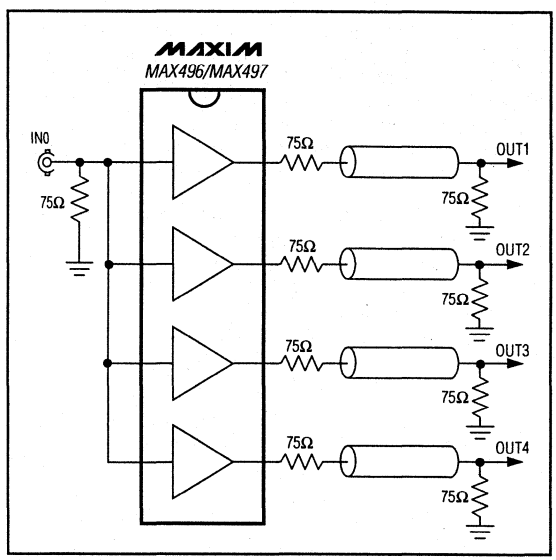


Figure 3. One-to-Four Distribution Amplifier

375MHz Quad Closed-Loop Video Buffers, AV = +1 and +2

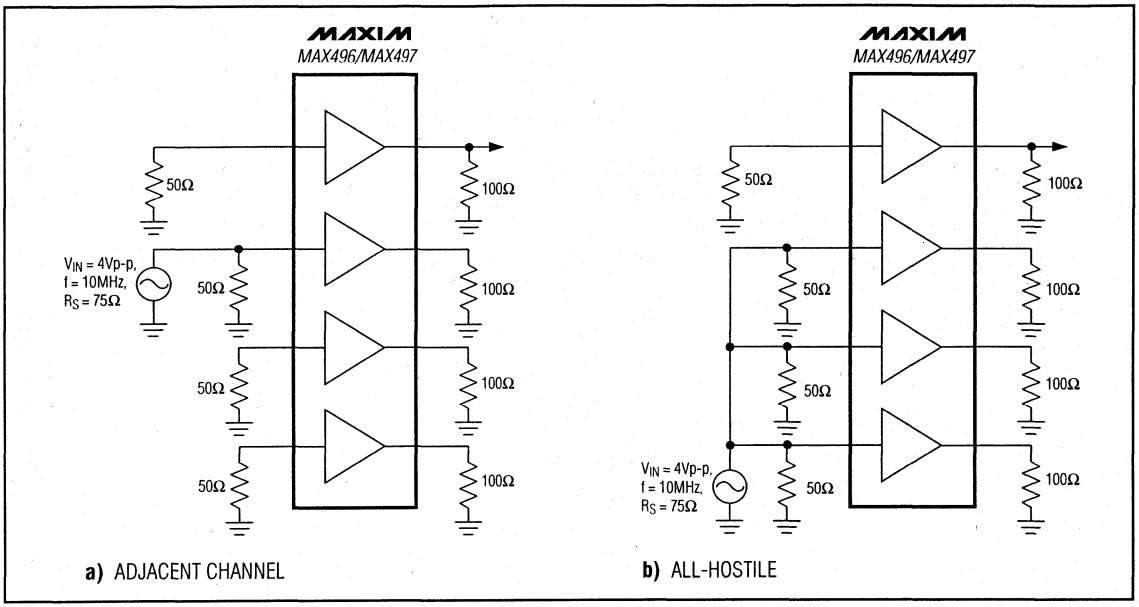


Figure 4. Crosstalk: a) Adjacent Channel; b) All-Hostile

Total Noise

The MAX496/MAX497's low input current noise of 2pA/√Hz and voltage noise of 5.6nV/√Hz provide for lower total noise compared to typical current-mode-feedback amplifiers, which usually have significantly higher input current noise. The input current noise multiplied by the feedback resistor is the dominant noise source of current-mode-feedback amplifiers.

Differential Gain and Phase Errors

Differential gain and phase errors are critical specifications for a buffer in composite (NTSC, PAL, SECAM) video applications, because these errors correspond directly to color changes in the displayed picture of composite video systems. The MAX496/MAX497's ultra-low differential gain and phase errors (0.01%/ 0.01°) make them ideal in broadcast-quality composite video applications.

Distribution Amplifier

The circuit in Figure 3 is a one-to-four distribution amplifier using a single MAX496 or MAX497 IC. A one-to-eight distribution amplifier can be implemented with a MAX496 or MAX497 by driving an additional cable from each of the four outputs. When driving more than four outputs from a single device, see the Continuous Power Dissipation specifications in the *Absolute Maximum Ratings*.

Coaxial Cable Drivers

High-speed performance, excellent output current capability, and an internally fixed gain of +2 make the MAX497 ideal for driving back-terminated 50Ω or 75Ω coaxial cables to ±2.8V.

In a typical application, the MAX497 drives a back-terminated 75Ω video cable (Figure 1). The back-termination resistor (at the MAX497's output) matches the impedance of the cable's driven end to the cable's impedance, to eliminate signal reflections. This, along with the load-termination resistor, forms a voltage divider with the load impedance, which attenuates the signal at the cable output by one-half. The MAX497 operates with an internal +2V/V closed-loop gain to provide unity gain at the cable's output.

Capacitive Load Driving

In most amplifier circuits, driving large capacitive loads increases the likelihood of oscillation. This is especially true for circuits with high loop gains, such as voltage followers. The amplifier's output resistance and the capacitive load form an RC filter that adds a pole to the loop response. If the pole frequency is low enough (as when driving a large capacitive load), the circuit phase margin is degraded and oscillation may occur.

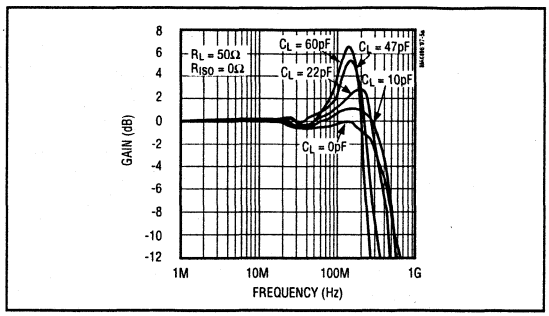


Figure 5a. MAX496 Small-Signal Gain vs. Frequency and Load Capacitor (R_L = 50Ω, R_{ISO} = 0Ω)

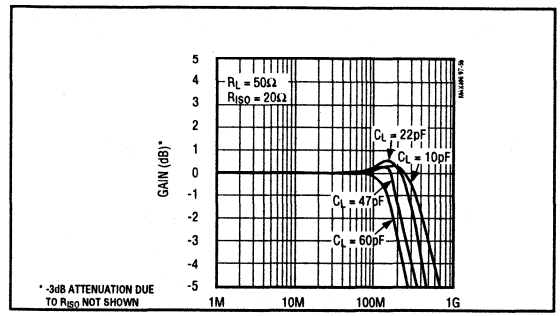


Figure 5b. MAX496 Small-Signal Gain vs. Frequency and Load Capacitor (R_L = 50Ω, R_{ISO} = 20Ω)

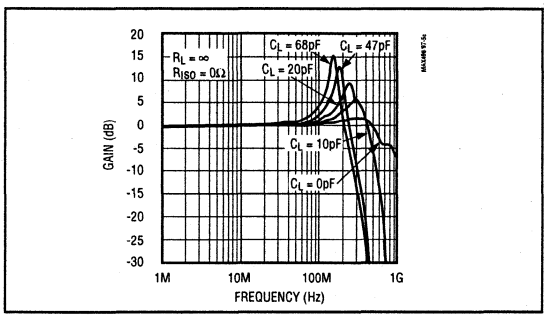


Figure 5c. MAX496 Small-Signal Gain vs. Frequency and Load Capacitor (R_L = ∞, R_{ISO} = 0Ω)

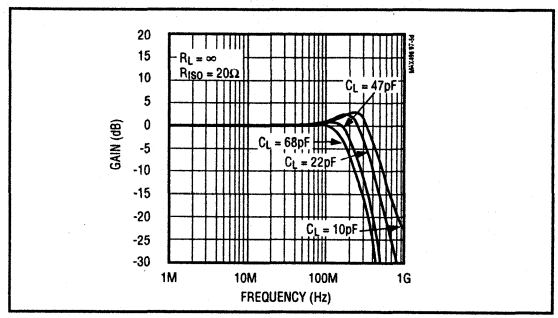


Figure 5d. MAX496 Small-Signal Gain vs. Frequency and Load Capacitor (R_L = ∞, R_{ISO} = 20Ω)

The MAX496/MAX497 drive capacitive loads up to 75pF without sustained oscillation, although some peaking may occur. When driving larger capacitive loads, or to reduce peaking, add an isolation resistor (R_{ISO}) between the output and the capacitive load (Figures 5a–5d).

Grounding and Layout

The MAX496/MAX497 bandwidths are in the RF frequency range. Depending on the size of the PC board used and the frequency of operation, it may be necessary to use Micro-strip or Stripline techniques.

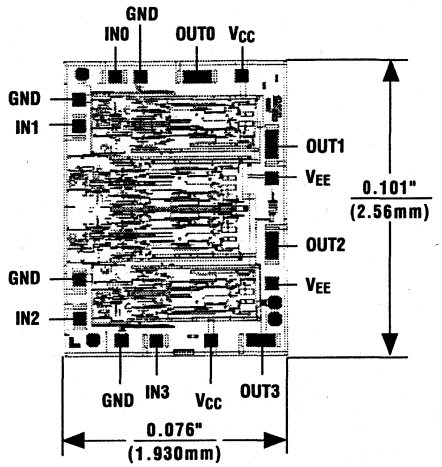
To realize the full AC performance of these high-speed buffers, pay careful attention to power-supply bypassing and board layout. The PC board should have at least two layers (wire-wrap boards are too inductive, bread boards are too capacitive), with one side a signal layer and the other a large, low-impedance ground plane. With multilayer boards, locate the ground plane on the layer that is not dedicated to a specific signal trace. The ground plane should be as free from voids as possible. Connect all ground pins to the ground plane.

Connect both positive power-supply pins together and bypass with a 0.10µF ceramic capacitor at each power supply pin, as close to the device as possible. Repeat the same for the negative power-supply pins. The capacitor lead lengths should be as short as possible to minimize lead inductance; surface-mount chip capacitors are ideal. A large-value (4.7µF or greater) tantalum or electrolytic bypass capacitor on each supply may be required for high-current loads. The location of this capacitor is not critical.

The MAX496/MAX497's analog input pins are isolated with ground pins to minimize parasitic coupling, which can degrade crosstalk and/or amplifier stability. Keep signal paths as short as possible to minimize inductance. Ensure that all input channel traces are the same length to maintain the phase relationship between the four channels. To further reduce crosstalk, connect the coaxial-cable shield to the ground side of the 75Ω terminating resistor at the ground plane, and terminate all unused inputs ground and outputs with a 100Ω or 150Ω resistor to ground.

375MHz Quad Closed-Loop Video Buffers, AV = +1 and +2

Chip Topography



TRANSISTOR COUNT: 544
SUBSTRATE CONNECTED TO V_{EE}

19-1143; Rev 0; 10/96

EVALUATION KIT AVAILABLE

MAXIM

Quad/Triple, SPDT, RGB Switches with 250MHz Video Buffer Amplifiers

General Description

The MAX498/MAX499 are high-speed, quad/triple, single-pole/double-throw video switches with on-board closed-loop buffer amplifiers. The buffer amplifiers feature +6dB gain (A_{VCL} = 2V/V), 250MHz -3dB bandwidth, 70MHz 0.1dB gain flatness, and 1250V/µs slew rate. Fast switching time (3ns) and fast settling time (12ns for a 4V step) make these devices excellent choices for a wide variety of video applications. The low differential gain/phase errors (0.03%/0.06°) and wide bandwidth make them ideal for both composite-video and RGB applications. The amplifiers are capable of delivering ±2.5V into back-terminated 50Ω or 75Ω cables, and they deliver ±2V to a 75Ω load, allowing multiple cables to be driven from a single output.

For implementation of large switch arrays, a low-power disable mode places the amplifier outputs in a high-impedance state. Channel selection and output enable/disable are controlled by four TTL/CMOS-compatible logic inputs. Each video input is isolated by an AC-ground pin, which minimizes channel-to-channel capacitance and reduces crosstalk to 90dB at 10MHz.

The four-channel MAX498 dissipates 390mW (typical) from ±5VDC power supplies with all output buffers enabled. Power consumption is reduced to 130mW with all buffers disabled. The corresponding dissipation for the three-channel MAX499 is 300mW enabled and 100mW disabled.

Applications

Video Switching and Routing
Broadcast-Quality Composite-Video Multiplexing
Workstations
Video Editing
Broadcast and High-Definition TV Systems
Multimedia Products
Medical Imaging

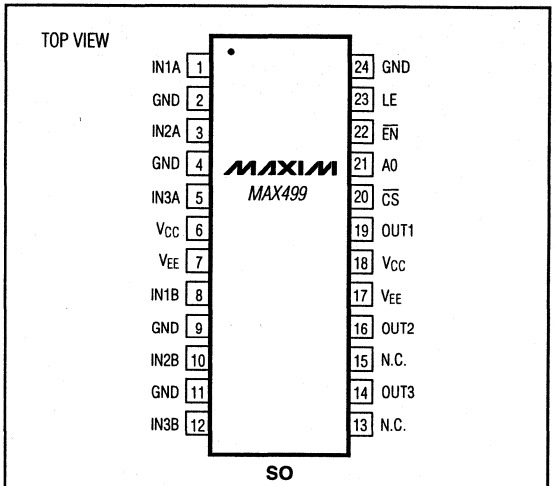
Features

- **High Speed:**
  250MHz Small-Signal -3dB Bandwidth
  135MHz Full-Power -3dB Bandwidth
- **70MHz 0.1dB Gain Flatness**
- **1250V/µs Slew Rate**
- **12ns to 0.1% Settling Time**
- **0.03°/0.06% Differential Phase/Gain Error**
- **2pF Input Capacitance**
- **3ns Channel-Switching Time**
- **120mVp-p Channel-Switching Transient**
- **Three-State Output Allows Large Switch Arrays**
- **Directly Drives 50Ω or 75Ω Back-Terminated Cables**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX498CWI	0°C to +70°C	28 SO
MAX499CWG	0°C to +70°C	24 SO

Pin Configurations



MAX498 appears at end of data sheet.

8

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Quad/Triple, SPDT, RGB Switches with 250MHz Video Buffer Amplifiers

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to V_{EE}).....+12V
Voltage on IN__ to GND .....(V_{EE} - 0.3V) to (V_{CC} + 0.3V)
Voltage on Digital Inputs
(LE, $\overline{EN}$, A0, $\overline{CS}$).....-0.3V to (V_{CC} + 0.3V)
Voltage on OUT_ (disabled) .....±4V
Output Short-Circuit Duration
to -4V ≤ OUT_ ≤ +4V .....Continuous

Continuous Power Dissipation (T_A = +70°C)
24-Pin SO (derate 11.76mW/°C above +70°C).....941mW
28-Pin SO (derate 12.5mW/°C above +70°C).....1W
Operating Temperature Range .....0°C to +70°
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, $V_{IN__}$ = 0V, R_L = 150Ω, LE = $\overline{EN}$ = $\overline{CS}$ = 0V, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}			±1.25	±1.70		V
Voltage Gain	A_V	R_L = 150Ω, -1.25V ≤ V_{IN} ≤ +1.25V		1.985		2.030	V/V
		R_L = 75Ω, -1.0V ≤ V_{IN} ≤ +1.0V		1.965		2.030	
Input Offset Voltage	V_{OS}				±2	±9	mV
Input Offset Voltage Drift	TCV_{OS}				±50		µV/°C
Input Bias Current	I_B				±1	±7	µA
Input Resistance	R_{IN}	-1.25V ≤ V_{IN} ≤ +1.25V		200	700		kΩ
Input Capacitance	C_{IN}	Channel on or off			2		pF
Output Short-Circuit Current	$I_{OUT(SC)}$	-3.5V ≤ OUT_ ≤ +3.5V (Note 1)			120		mA
Output Current	$I_{OUT_}$	-2.0V ≤ $V_{OUT_}$ ≤ +2.0V, R_L = 75Ω		±27	±40		mA
On Output Resistance	R_{OUT}				0.15		Ω
On Output Impedance		f = 10MHz			3.0		Ω
Off Output Resistance		-2.50V ≤ V_{OUT} ≤ +2.50V		1.0	1.2		kΩ
Operating Supply-Voltage Range				±4.50		±5.50	V
Positive Power-Supply Rejection	PSR+	4.50V ≤ V_{CC} ≤ 5.50V, V_{EE} = -5.0V		55	72		dB
Negative Power-Supply Rejection	PSR-	-5.50V ≤ V_{EE} ≤ -4.5V, V_{CC} = +5.0V		55	72		dB
Logic Low Voltage	V_{INLL}			0.8			V
Logic High Voltage	V_{INLH}					2	V
Logic Input Current	I_{INL}	0V ≤ V_{INL} ≤ V_{CC}		-10		130	µA
Positive Supply Current	I_{CC}	$\overline{EN}$ = 0	MAX498		40	52	mA
			MAX499		31	41	
		$\overline{EN}$ = 1	MAX498		14	17	
			MAX499		11	14	
Negative Supply Current	I_{EE}	$\overline{EN}$ = 0	MAX498		38	50	mA
			MAX499		29	39	
		$\overline{EN}$ = 1	MAX498		12	15	
			MAX499		9	12	

Note 1: Limited by package power dissipation.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, $V_{IN__}$ = 0V, R_L = 100Ω, LE = $\overline{EN}$ = $\overline{CS}$ = 0V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small-Signal, -3dB Bandwidth	BW_{-3dB}	V_{IN} ≤ 100mVp-p		250		MHz
±0.1dB Gain Flatness		V_{IN} ≤ 100mVp-p		70		MHz
Full-Power, -3dB Bandwidth	FPBW	V_{OUT} = ±2V		135		MHz
Slew Rate	SR	V_{OUT} = 4V step		1250		V/µs
Settling Time	t_S	0.1%, V_{OUT} = 4V step		12		ns
Input Voltage Noise Density		f = 100kHz		7.8		$nV/\sqrt{Hz}$
Input Current Noise Density		f = 100kHz		2.6		$pA/\sqrt{Hz}$
Total Harmonic Distortion	THD	f = 10MHz		-50		dB
Spurious-Free Dynamic Range	SFDR	f_C = 3MHz		-66		dBc
Adjacent-Channel Crosstalk		f = 10MHz (Note 2)		90		dB
All-Hostile Crosstalk		f = 10MHz (Note 3)		62		dB
Off-Isolation		$\overline{EN}$ = 1, f = 10MHz (Note 4)		81		dB
Differential Gain	Diff Gain	f = 3.58MHz (Note 5), R_L = 150Ω		0.03		%
Differential Phase	Diff Phase	f = 3.58MHz (Note 5), R_L = 150Ω		0.06		degrees

TIMING CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, $V_{IN__}$ = 0V, R_L = 150Ω, LE = $\overline{EN}$ = $\overline{CS}$ = 0V, T_A = 0°C to +70°C. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
A0/$\overline{EN}$ to $\overline{CS}$ Setup Time	t_{SU}	LE = high (Note 6)		8			ns
A0/$\overline{EN}$ to $\overline{CS}$ Hold Time	t_H	LE = high (Note 6)				4	ns
$\overline{CS}$ Pulse Width	t_{CS}	(Note 6)		15			ns
Channel-Switching Propagation Delay	t_{PD}	(Note 7)			20		ns
Channel-Switching Time	t_{SW}	(Note 8)			3		ns
Channel-Switching Transient		V_{INA} = V_{INB} = 0V	Positive		70		mV
			Negative		50		
Enable/Disable Switching Transient		V_{INA} = V_{INB} = 0V	Positive		10		mV
			Negative		150		
Amplifier-Disable Time	t_{OFF}	(Note 9)			16		ns
Amplifier-Enable Time	t_{ON}	(Note 10)			24		ns

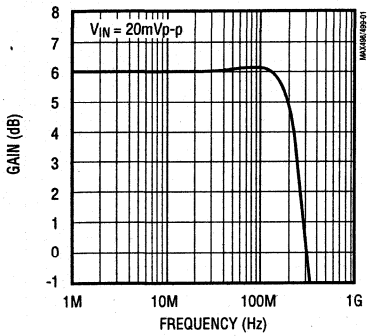
Note 2: Test-channel input grounded through a 50Ω resistor. Adjacent channel driven to a 2Vp-p output with a 10MHz sine wave (Figure 9).
Note 3: Same as Note 2, except all channels but the test channel are driven to a 2Vp-p output with a 10MHz sine wave (Figure 9).
Note 4: Test-channel input connected to a 2Vp-p sine wave at 10MHz. The test channel's output is measured with the outputs disabled (Figure 9).
Note 5: Input test signal is a 3.58MHz sine wave of 40IRE amplitude, superimposed on a 0IRE to 100IRE linear ramp (Figure 10).
Note 6: Guaranteed by design.
Note 7: V_{INA} = +1V, V_{INB} = -1V, delay from $\overline{CS}$ to 10% of V_{OUT}.
Note 8: V_{INA} = +1V, V_{INB} = -1V, delay from $\overline{CS}$ to 10% of V_{OUT}.
Note 9: Delay from $\overline{EN}$ to 90% of V_{OUT}.
Note 10: Delay from $\overline{EN}$ to 10% of V_{OUT}.

Quad/Triple, SPDT, RGB Switches with 250MHz Video Buffer Amplifiers

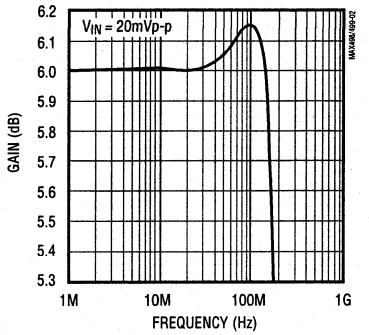
Typical Operating Characteristics

(V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

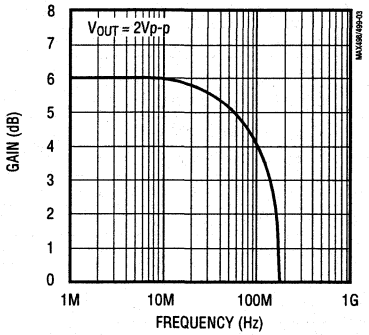
SMALL-SIGNAL GAIN vs. FREQUENCY



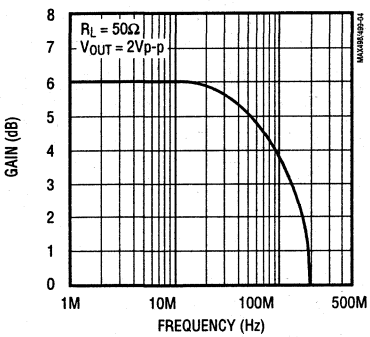
GAIN FLATNESS vs. FREQUENCY



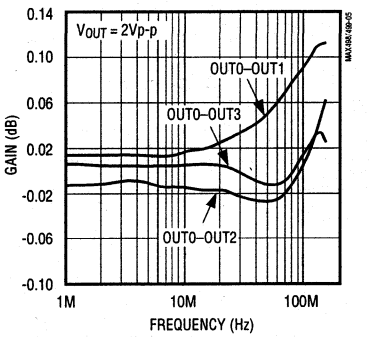
LARGE-SIGNAL GAIN vs. FREQUENCY



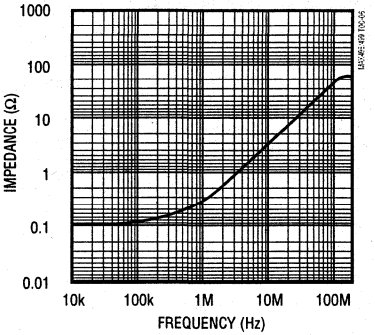
LARGE-SIGNAL GAIN vs. FREQUENCY



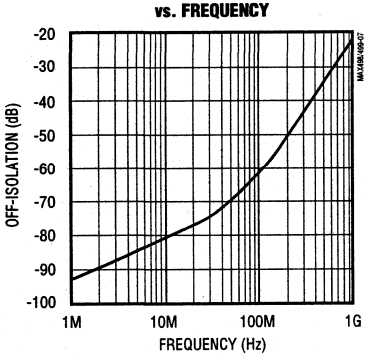
LARGE-SIGNAL GAIN vs. FREQUENCY



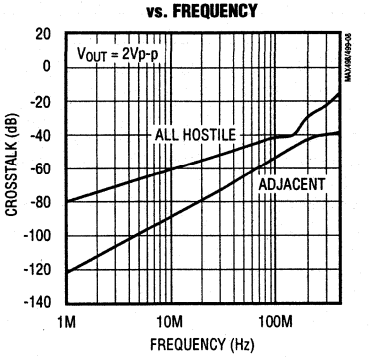
OUTPUT IMPEDANCE vs. FREQUENCY



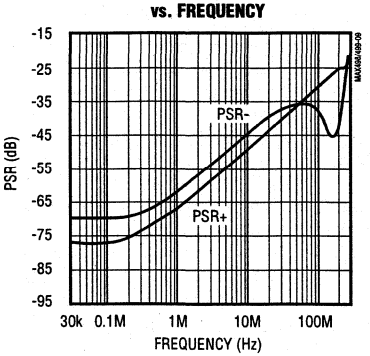
OFF-ISOLATION vs. FREQUENCY



CROSSTALK vs. FREQUENCY



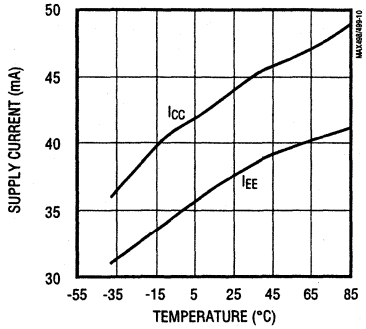
POWER-SUPPLY REJECTION vs. FREQUENCY



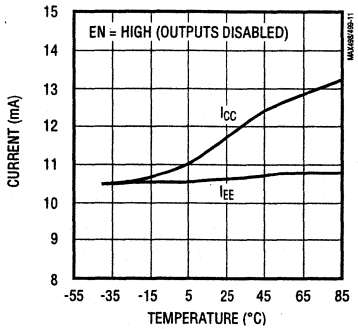
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

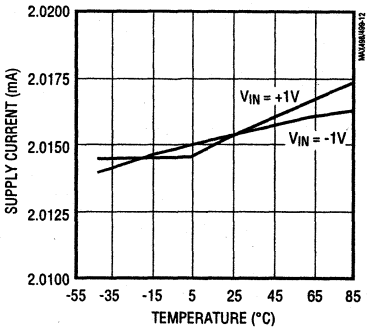
MAX498 SUPPLY CURRENT vs. TEMPERATURE



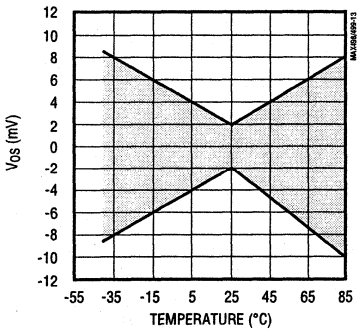
DISABLED SUPPLY CURRENT vs. TEMPERATURE



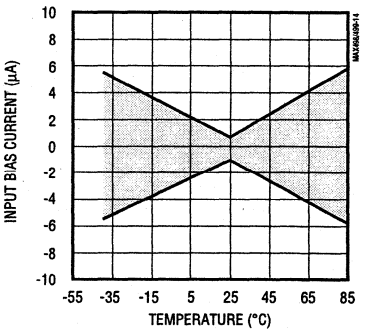
GAIN vs. TEMPERATURE



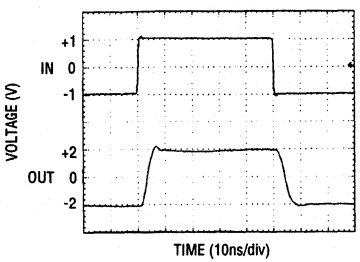
INPUT OFFSET VOLTAGE vs. TEMPERATURE



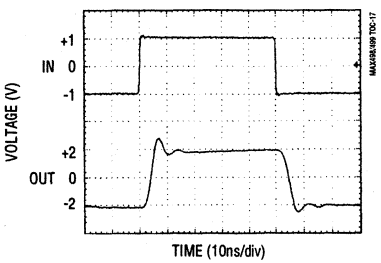
INPUT BIAS CURRENT vs. TEMPERATURE



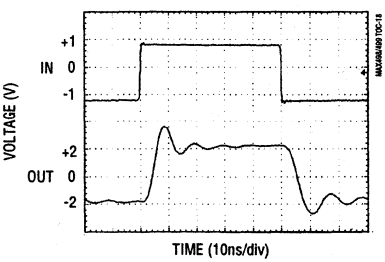
LARGE-SIGNAL PULSE RESPONSE



LARGE-SIGNAL PULSE RESPONSE (C_L = 47pF)



LARGE-SIGNAL PULSE RESPONSE (C_L = 100pF)

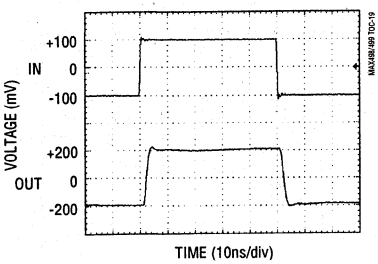


Quad/Triple, SPDT, RGB Switches with 250MHz Video Buffer Amplifiers

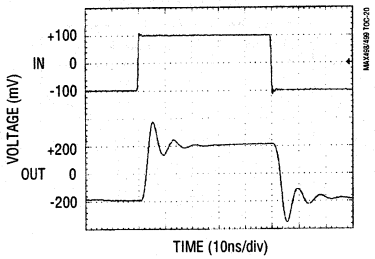
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

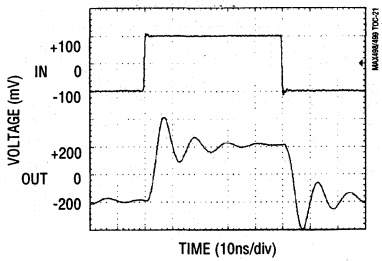
SMALL-SIGNAL PULSE RESPONSE



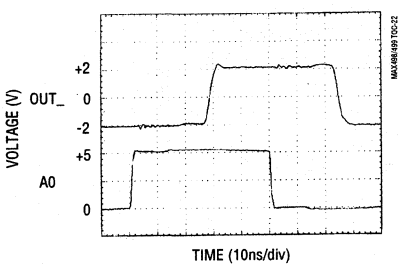
SMALL-SIGNAL PULSE RESPONSE (C_L = 47pF)



SMALL-SIGNAL PULSE RESPONSE (C_L = 100pF)

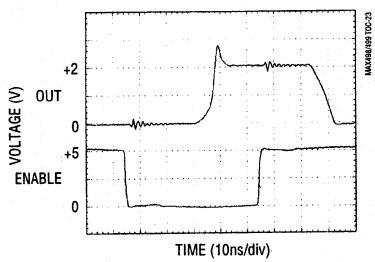


CHANNEL SWITCHING

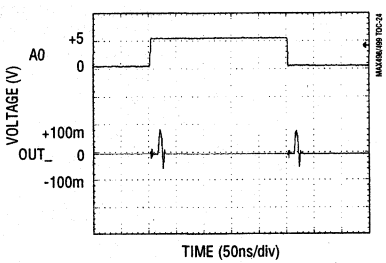


IN_A = -1V
IN_B = +1V

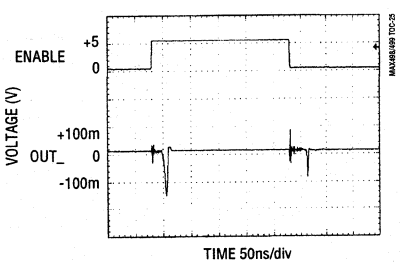
ENABLE/DISABLE SWITCHING



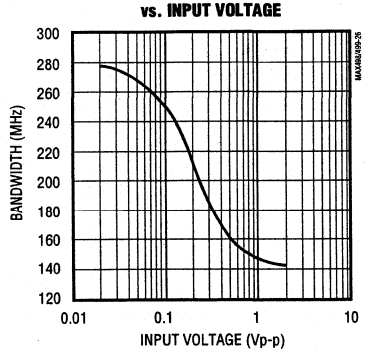
CHANNEL-SWITCHING TRANSIENT



ENABLE/DISABLE SWITCHING TRANSIENT



BANDWIDTH vs. INPUT VOLTAGE



Pin Description

PIN		NAME	FUNCTION
MAX498	MAX499		
1, 3, 5, 11, 13, 19	2, 4, 9, 11, 24	GND	Analog Ground. All ground pins are internally connected. Connect all ground pins externally to ground to minimize impedance.
2	1	IN1A	Signal Input 1, Channel A
4	3	IN2A	Signal Input 2, Channel A
6	5	IN3A	Signal Input 3, Channel A
7, 22	6, 18	V_{CC}	Positive Power-Supply Voltage. Connect V_{CC} to +5V. V_{CC} pins are internally connected. Connect both pins externally to +5V to minimize supply impedance. Bypass each pin to ground with a 0.1µF ceramic capacitor.
8	—	IN0B	Signal Input 0, Channel B
9, 21	7, 17	V_{EE}	Negative Power-Supply Voltage. Connect V_{EE} to -5V. V_{EE} pins are internally connected. Connect both pins to -5V externally to minimize supply impedance. Bypass each pin to ground with a 0.1µF ceramic capacitor.
10	8	IN1B	Signal Input 1, Channel B
12	10	IN2B	Signal Input 2, Channel B
14	12	IN3B	Signal Input 3, Channel B
15, 17	13, 15	N.C.	No Connect. Not internally connected; connect to GND.
16	14	OUT3	Output 3
18	16	OUT2	Output 2
20	19	OUT1	Output 1
23	—	OUT0	Output 0
24	20	$\overline{CS}$	Chip-Select Input. When $\overline{CS}$ is low, the A0 and $\overline{EN}$ latches are transparent. The data present at A0 is latched when $\overline{CS}$ goes high. LE's status determines whether $\overline{EN}$ is latched along with A0, or if the $\overline{EN}$ latch remains transparent independently of $\overline{CS}$.
25	21	A0	Address Input. A0 = 0 selects channel A, and A0 = 1 selects channel B if $\overline{CS}$ is low. A0 is latched on $\overline{CS}$'s low-to-high transition.
26	22	$\overline{EN}$	Output Buffer-Enable Input. $\overline{EN}$ = 0 enables the output buffer amplifiers, and $\overline{EN}$ = 1 disables the output buffers if $\overline{CS}$ is low. $\overline{EN}$ is latched during $\overline{CS}$'s low-to-high transition if LE is high. $\overline{EN}$ is not latched if LE is low.
27	23	LE	Latch-Enable Input. With LE = 1, $\overline{EN}$ is latched along with A0 when $\overline{CS}$ goes high. When LE = 0, the $\overline{EN}$ latch is transparent independently of $\overline{CS}$'s state.
28	—	IN0A	Signal Input 0, Channel A

Quad/Triple, SPDT, RGB Switches with 250MHz Video Buffer Amplifiers

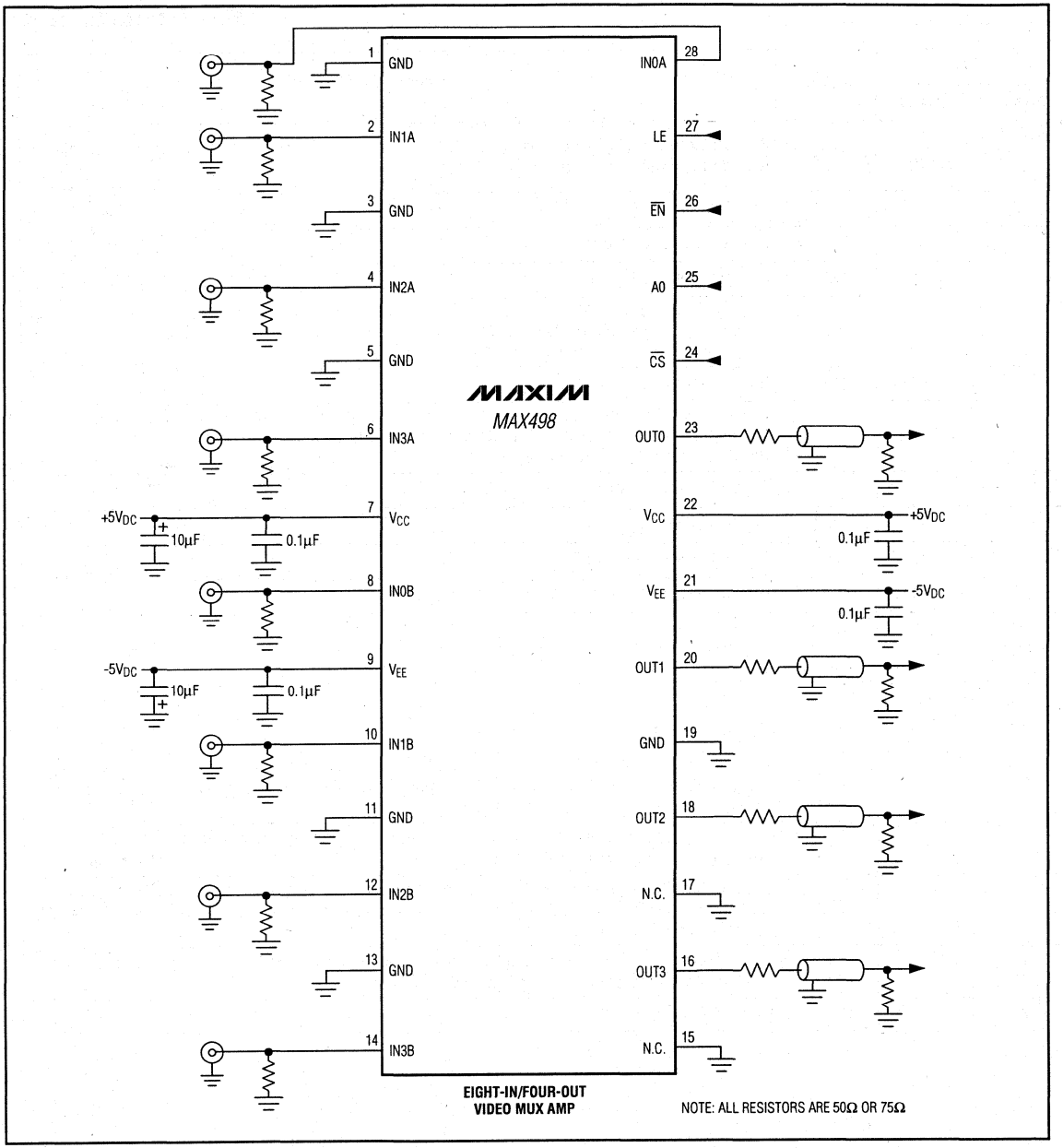


Figure 1a. MAX498 Typical Application Circuit

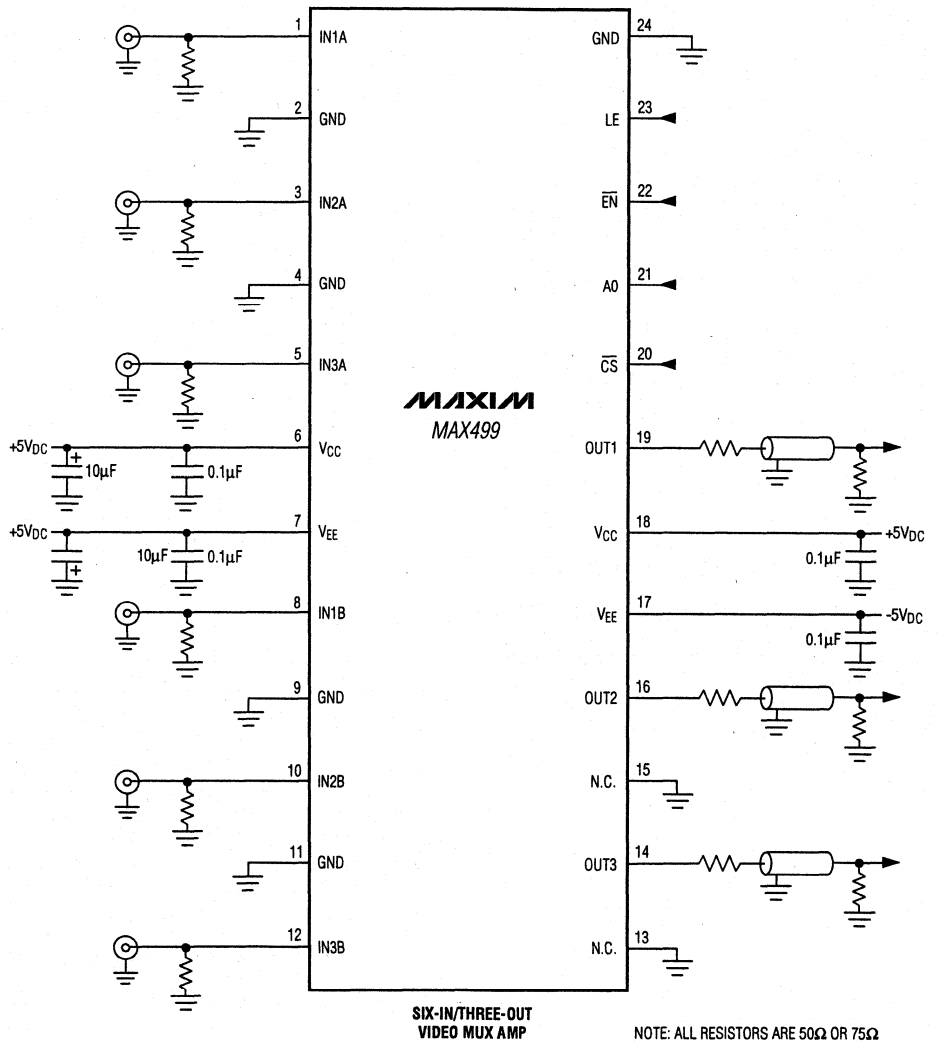


Figure 1b. MAX499 Typical Application Circuit

Quad/Triple, SPDT, RGB Switches with 250MHz Video Buffer Amplifiers

Detailed Description

The MAX498/MAX499 are quad/triple video switches with high-speed, closed-loop, voltage-feedback amplifiers set to a 2V/V gain. Figure 1 shows typical application circuits. The amplifiers use a unique two-stage, voltage-feedback architecture that combines the benefits of conventional voltage-feedback and current-feedback topologies to achieve wide bandwidths and high slew rates while maintaining precision.

Figure 2 is a simplified block diagram of the MAX498/MAX499. All four amplifier/switch blocks are identical to that shown for Ch_0. A common control logic block accepts external logic inputs A0, $\overline{EN}$, $\overline{CS}$, and LE, and controls the status of switches S1, S2, and S3 of each amplifier in parallel, as described in the *Digital Interface* section.

S3 is open in the enabled state, and if Ch_A is selected, S1 is connected to IN_A and S2 is connected to GND. If Ch_B is selected, S1 is connected to GND and S2 is connected to IN_B. Connecting the deselected GM_ block to GND ensures minimum feedthrough.

S3 is closed in the disabled state, and both S1 and S2 are connected to GND. Disconnecting both inputs and connecting the amplifier's inputs to GND significantly improves off-isolation.

Applications Information

Power Dissipation

The MAX498/MAX499's maximum output current is limited by the package's maximum allowable power dissipation. The maximum junction temperature should not exceed +150°C. Power dissipation increases with load, and this increase can be approximated by one of the following equations:

For $V_{OUT} > 0V$: $|V_{CC} - V_{OUT}| I_{LOAD}$

OR

For $V_{OUT} < 0V$: $|V_{EE} - V_{OUT}| I_{LOAD}$.

These devices can drive 100Ω loads connected to each of the outputs over the entire rated output swing and temperature range. While the output is short-circuit protected to 120mA, this does not necessarily guarantee that under all conditions, the maximum junction temperature will not be exceeded. Do not exceed the derating values given in the *Absolute Maximum Ratings* section.

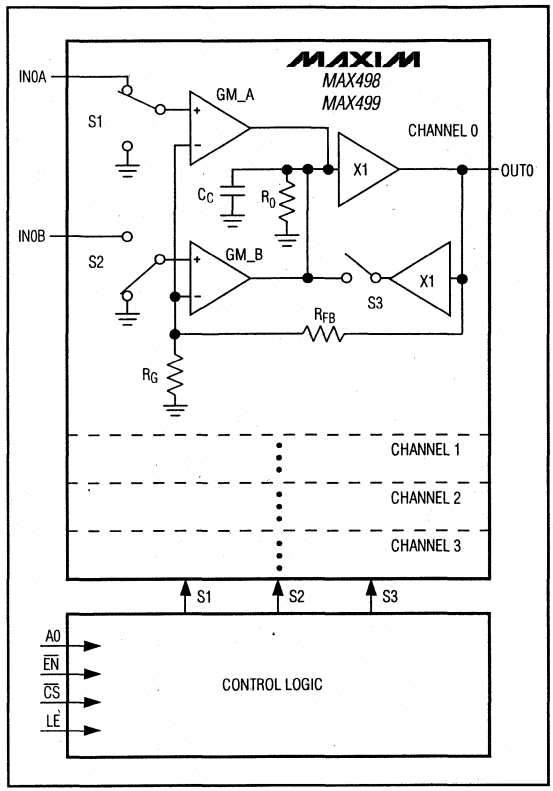


Figure 2. Block Diagram

Total Noise

The MAX498/MAX499's low 2.6pA/√Hz input current noise and 7.8nV/√Hz voltage noise provide for lower total noise compared to typical current-mode feedback amplifiers, which usually have significantly higher input current noise. The input current noise multiplied by the feedback resistor is the dominant noise source of current-mode feedback amplifiers.

Differential Gain and Phase Errors

Differential gain and phase errors are critical specifications for a buffer in composite (NTSC, PAL, SECAM) video applications, because these errors correspond directly to color changes in the displayed picture of composite video systems. The MAX498/MAX499's low differential gain and phase errors (0.03%/0.06°) make them ideal in broadcast-quality, composite video applications.

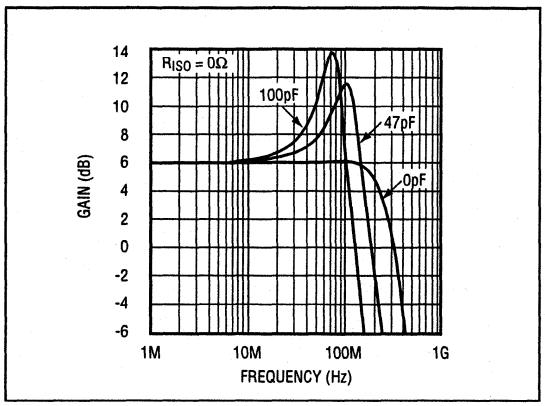


Figure 3a. Small-Signal Gain vs. Frequency and Load Capacitor (R_L = 100Ω, R_{ISO} = 0Ω)

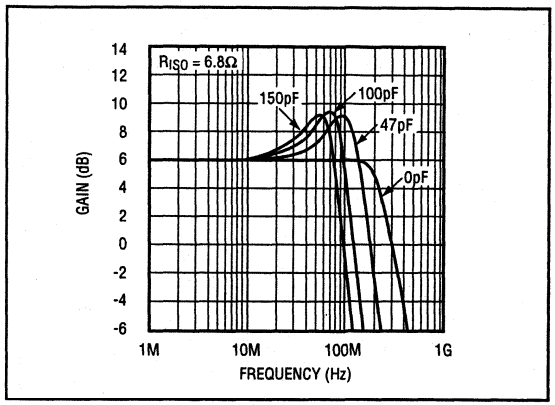


Figure 3b. Small-Signal Gain vs. Frequency and Load Capacitor (R_L = 100Ω, R_{ISO} = 6.8Ω)

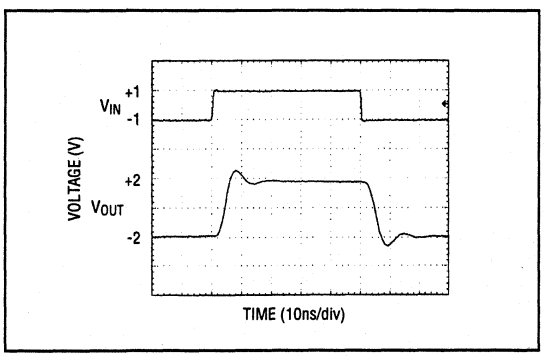


Figure 4a. Large-Signal Pulse Response with C_L = 100pF and R_{ISO} = 5.1Ω

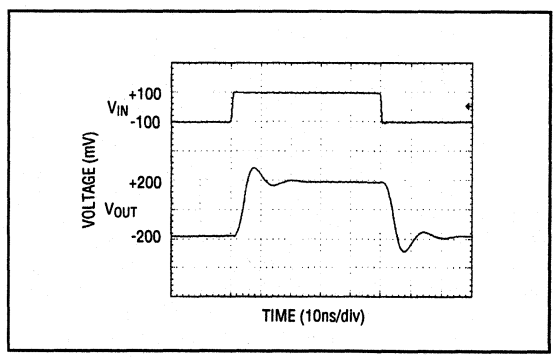


Figure 4b. Small-Signal Pulse Response with C_L = 100pF and R_{ISO} = 5.1Ω

Coaxial Cable Drivers

High-speed performance, excellent output current capability, and an internally fixed gain of +2 make the MAX498/MAX499 ideal for driving back-terminated 50Ω or 75Ω coaxial cables to ±2.5V.

In a typical application, the MAX498/MAX499 drive a back-terminated cable (Figure 1). The back-termination resistor, at the output, matches the impedance of the cable's driven end to the cable's impedance, eliminating signal reflections. This resistor, along with the load-termination resistor, forms a voltage divider with the load impedance, which attenuates the signal at the cable's output by one-half. The MAX498/MAX499 operate with an internal +2V/V closed-loop gain to provide unity gain at the cable's output.

Capacitive-Load Driving

In most amplifier circuits, driving large capacitive loads increases the likelihood of oscillation. This is especially true for circuits with high loop gains, such as voltage followers. The amplifier's output resistance and the capacitive load form an RC filter that adds a pole to the loop response. If the pole frequency is low enough (as when driving a large capacitive load), the circuit-phase margin is degraded and oscillation may occur.

The MAX498/MAX499 drive capacitive loads up to 100pF without sustained oscillation, although some peaking may occur (Figures 3a and 3b). When driving larger capacitive loads, or to reduce peaking, add an isolation resistor (R_{ISO}) between the output and the capacitive load (Figures 4a, 4b, and 5).

Quad/Triple, SPDT, RGB Switches with 250MHz Video Buffer Amplifiers

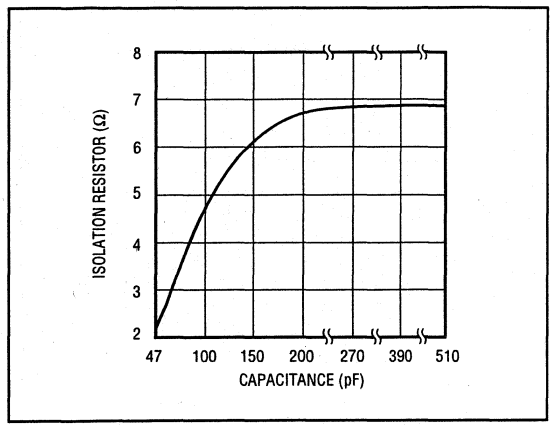


Figure 5. Isolation Resistor vs. Capacitive Load

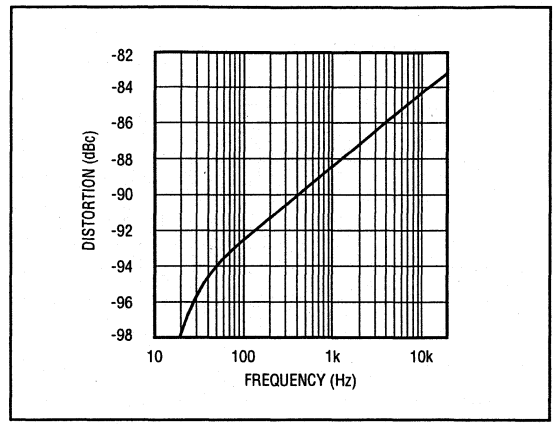


Figure 6. Total Harmonic Distortion (Audio) vs. Frequency

Switching Audio Signals (Audio-Distortion Measurement)

When switching audio signals, distortion is the prime consideration in performance. Figure 6 shows total harmonic distortion vs. frequency, in the audio range, for the MAX498/MAX499.

Large Switch Arrays

Large crosspoint switch arrays are possible with the MAX498/MAX499 using the enable function $\overline{EN}$. When the amplifiers are disabled, output impedance is typically 1.2kΩ, due to the feedback and gain resistors. This limits the number of outputs that can be paralleled without a buffer. Since each output can drive 100Ω, eight outputs can typically be connected together. If additional outputs must be connected in parallel, a MAX4178 (single), MAX496 (quad), or equivalent unity-gain buffer can be used.

Whether enabled or disabled, each input represents more than 200kΩ of resistance. Capacitance is the prime consideration limiting the number of inputs that can be connected to a single output. Since each output can drive 100pF of capacitance without an isolation resistor, 50 inputs (C_{IN} = 2pF, typical) can be driven by a single output. However, peaking will occur as inputs are added (Figure 3), which reduces the 0.1dB bandwidth.

Digital Interface

The MAX498/MAX499 multiplexer architecture ensures that no input channels are ever connected together. Select a channel by changing A0's state (A0 = 0 for channel A, and A0 = 1 for channel B) and pulsing $\overline{CS}$ low (see Tables 1a and 1b). Figure 7 shows the logic timing diagram.

When the enable input ($\overline{EN}$) is driven to a TTL low state, it enables the MAX498/MAX499 amplifier outputs. When $\overline{EN}$ is driven high, it disables the amplifier outputs. When disabled, the MAX498/MAX499 exhibit a 1.2kΩ disabled output resistance due to their internal feedback resistors.

LE determines whether $\overline{EN}$ is latched by $\overline{CS}$ or operates independently. When the latch-enable input (LE) is connected to V+, $\overline{CS}$ becomes the latch control for the $\overline{EN}$ input register. If $\overline{CS}$ is low, both the $\overline{EN}$ and A0 latches are transparent; once $\overline{CS}$ returns high, both A0 and $\overline{EN}$ are latched.

When LE is connected to ground, the $\overline{EN}$ latch is transparent and independent of $\overline{CS}$. This allows all MAX498/MAX499 devices to be shut down simultaneously, regardless of $\overline{CS}$'s input state. Simply connect LE to ground and connect all $\overline{EN}$ inputs together (Figure 8a). Hard wire LE to V+ or ground (rather than driving LE with a gate) to prevent crosstalk from the digital inputs to IN0A.

Another option for output disable is to connect LE to V+, parallel the outputs of several MAX498/MAX499s, and use $\overline{EN}$ to individually disable all devices but the one in use (Figure 8b).

When the outputs are disabled, off-isolation from the analog inputs to the amplifier outputs is typically 81dB at 10MHz.

Grounding and Layout

The MAX498/MAX499 bandwidths are in the RF frequency range. Depending on the size of the PC board used and the frequency of operation, it may be necessary to use Micro-strip or Stripline techniques.

To realize the full AC performance of these high-speed buffers, pay careful attention to power-supply bypassing and board layout. The PC board should have at least two layers (wire-wrap boards are too inductive, and bread boards are too capacitive), with one side a signal layer and the other a large, low-impedance ground plane. With multilayer boards, locate the ground plane on the layer that is not dedicated to a specific signal trace. The ground plane should be as free from voids as possible. Connect all ground pins to the ground plane.

Connect both positive power-supply pins together and bypass with a 0.10µF ceramic capacitor at each power-supply pin, as close to the device as possible. Repeat for the negative power-supply pins. The capacitor lead lengths should be as short as possible to minimize lead inductance; surface-mount chip capacitors are ideal. A large-value (10µF or greater) tantalum or electrolytic bypass capacitor on each supply may be required for high-current loads. The location of this capacitor is not critical.

The MAX498/MAX499's analog input pins are isolated with ground pins to minimize parasitic coupling, which can degrade crosstalk and/or amplifier stability. Keep signal paths as short as possible to minimize inductance. Ensure that all input channel traces are the same length, to maintain the phase relationship between the four channels. To further reduce crosstalk, connect the coaxial-cable shield to the ground side of the 75Ω terminating resistor at the ground plane, and terminate all unused inputs to ground and outputs with a 100Ω or 150Ω resistor to ground.

Table 1a. Amplifier and Channel Selection with LE = V+

$\overline{CS}$	$\overline{EN}$	A0	FUNCTION
0	0	0	Enables amplifier outputs. Selects channel A.
0	0	1	Enables amplifier outputs. Selects channel B.
0	1	X	Disables amplifiers. Outputs high-Z.
1	X	X	Latches A0, $\overline{EN}$. Outputs unchanged.

Table 1b. Amplifier and Channel Selection with LE = GND

$\overline{CE}$	$\overline{EN}$	$\overline{A0}$	FUNCTION
0	0	0	Enables amplifier outputs. Selects channel A.
1	0	X	Enables amplifier outputs. Latches A0 to output A or B, according to A0's state at $\overline{CS}$'s last edge.
X	1	X	Disables amplifiers. Outputs high-Z. A0 latch = channel A.
0	0	1	Enables amplifier outputs. Selects channel B.

Quad/Triple, SPDT, RGB Switches with 250MHz Video Buffer Amplifiers

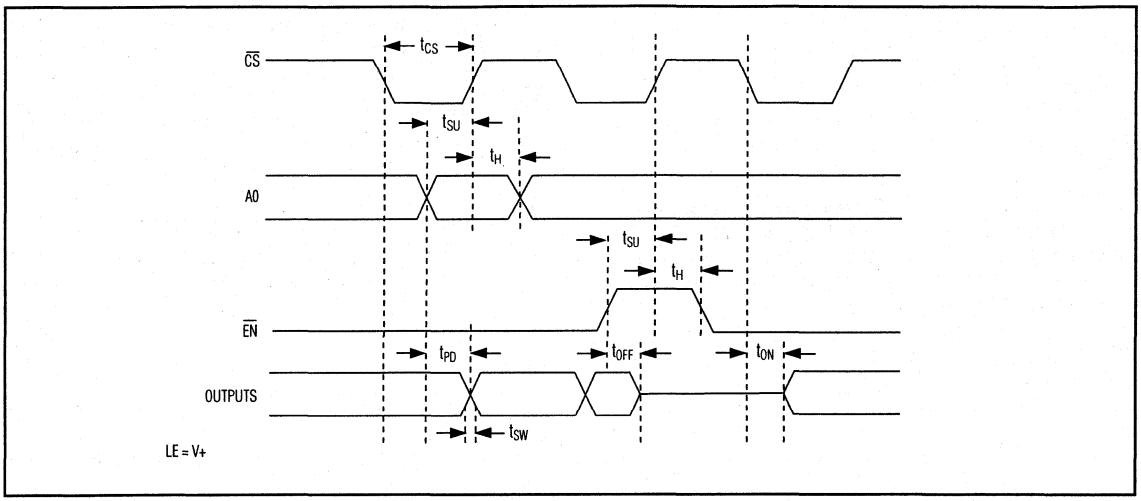


Figure 7. Logic Timing Diagram

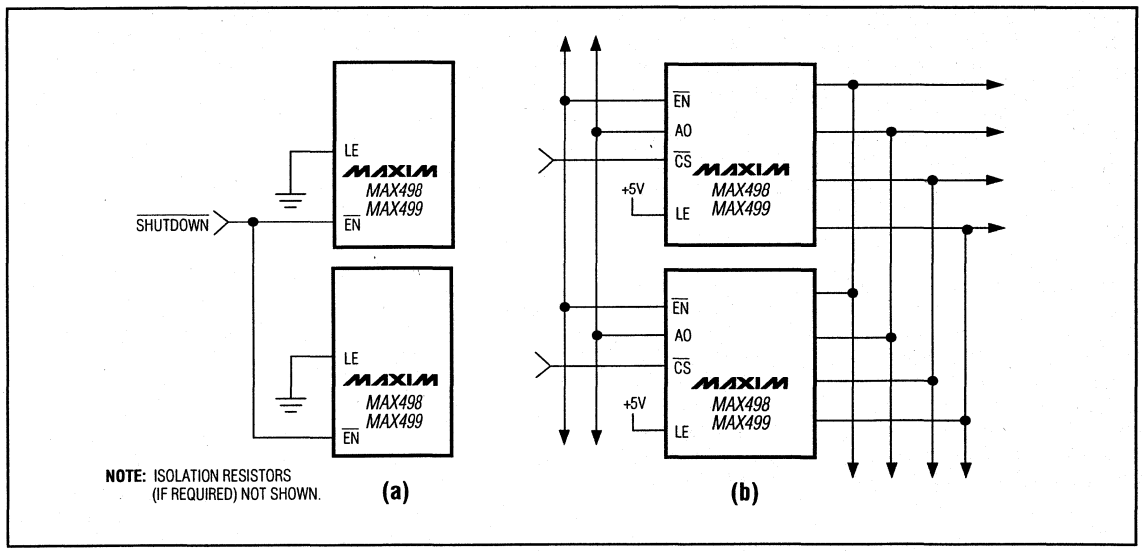


Figure 8. (a) Simultaneous Shutdown of all MAX498/MAX499s; (b) Enable ($\overline{EN}$) Register Latched by $\overline{CS}$

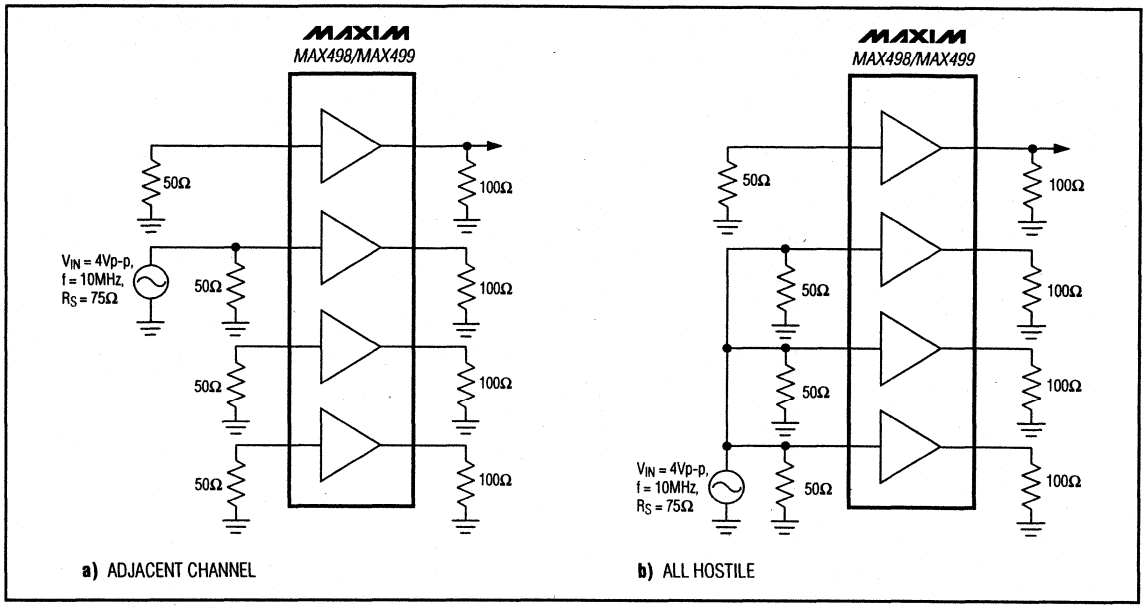


Figure 9. Test Circuits for Measuring Crosstalk: a) Adjacent Channel; b) All Hostile

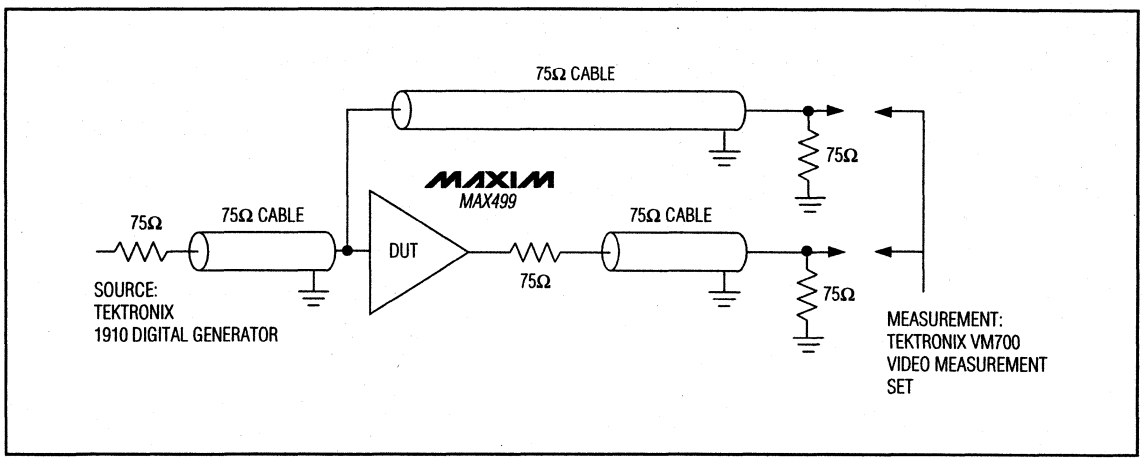
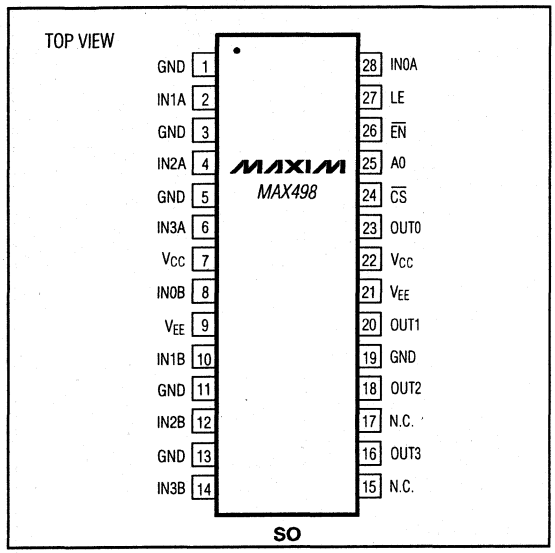


Figure 10. Differential Phase and Gain Error Test Circuit

Quad/Triple, SPDT, RGB Switches with 250MHz Video Buffer Amplifiers

Pin Configurations (continued)



Chip Information

SUBSTRATE CONNECTED TO: V_{EE}
TRANSISTOR COUNT: 813

19-0436; Rev 1; 3/96

EVALUATION KIT AVAILABLE

MAXIM

500MHz, Low-Power Op Amps

General Description

The MAX4100/MAX4101 op amps combine ultra-high-speed performance with low-power operation. The MAX4100 is compensated for unity-gain stability, while the MAX4101 is compensated for stability in applications with a closed-loop gain (A_{VCL}) of 2V/V or greater.

The MAX4100/MAX4101 require only 5mA of supply current while delivering a 500MHz unity-gain bandwidth (MAX4100) or a 200MHz -3dB bandwidth (MAX4101) with a 250V/µs slew rate.

These high-speed op amps have a wide output voltage swing of ±3.5V and a high current-drive capability of 80mA.

Applications

Video Cable Driver

Ultrasound

Gamma Cameras

Portable Instruments

Active Filters

ADC Buffers

Features

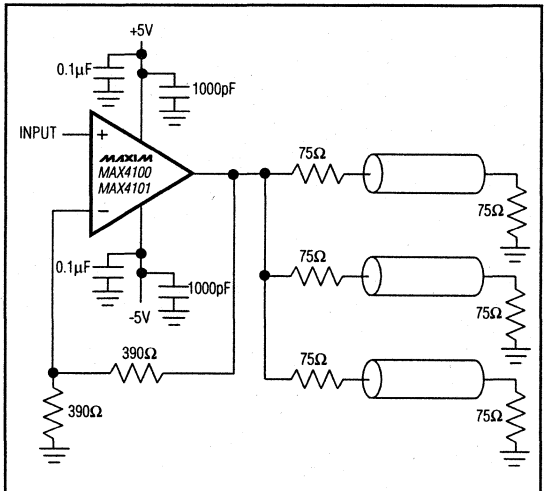
- **500MHz Unity-Gain Bandwidth (MAX4100)**
  200MHz -3dB Bandwidth (A_{VCL} = 2V/V, MAX4101)
- **65MHz 0.1dB Gain Flatness (MAX4100)**
- **250V/µs Slew Rate**
- **0.06%/0.04° Differential Gain/Phase**
- **High Output Drive: 80mA**
- **Low Power: 5mA Supply Current**
- **Fast Settling Time:**
  18ns to 0.1%
  35ns to 0.01%

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4100ESA	-40°C to +85°C	8 SO
MAX4100EUA	-40°C to +85°C	8 µMAX*
MAX4101ESA	-40°C to +85°C	8 SO

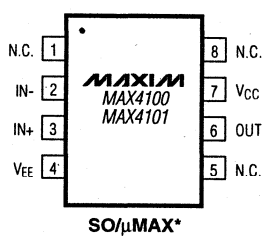
** Contact factory for availability of µMAX package.*

Typical Application Circuit



VIDEO/RF DISTRIBUTION AMPLIFIER

Pin Configuration



SO/µMAX*

** Contact factory for availability of MAX4100 µMAX package.*

8

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

500MHz, Low-Power Op Amps

ABSOLUTE MAXIMUM RATINGS

Power-Supply Voltage (V_{CC}, V_{EE}) ..... ±6V
Voltage on Any Pin to Ground or Any Other Pin ..... V_{CC} to V_{EE}
Short-Circuit Duration (V_{OUT} to GND) ..... Indefinite
Continuous Power Dissipation (T_A = +70°C)
SO (derate 5.88mW/°C above +70°C) 471mW
µMAX (derate 4.10mW/°C above +70°C) 330mW

Operating Temperature Ranges
MAX4100E_A/MAX4101E_A ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, V_{EE} = -5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC SPECIFICATIONS							
Input Offset Voltage	V_{OS}	V_{OUT} = 0V			1	8	mV
Input Offset Voltage Drift	TCV_{OS}	V_{OUT} = 0V			15		µV/°C
Input Bias Current	I_B	V_{OUT} = 0V, V_{IN} = -V_{OS}			3	9	µA
Input Offset Current	I_{OS}	V_{OUT} = 0V, V_{IN} = -V_{OS}			0.05	0.5	µA
Common-Mode Input Resistance	R_{INCM}	Either input			5		MΩ
Common-Mode Input Capacitance	C_{INCM}	Either input			1		pF
Input Voltage Noise	e_n	f = 100kHz	MAX4100		8		nV/√Hz
			MAX4101		6		
Integrated Voltage Noise		f = 1MHz to 100MHz	MAX4100		100		$µV_{RMS}$
			MAX4101		75		
Input Current Noise	i_n	f = 100kHz	MAX4100		0.8		pA/√Hz
			MAX4101		0.8		
Integrated Current Noise		f = 1MHz to 100MHz	MAX4100		10		nA_{RMS}
			MAX4101		10		
Common-Mode Input Voltage	V_{CM}			-2.5		2.5	V
Common-Mode Rejection	CMR	V_{CM} = ±2.5V		75	90		dB
Power-Supply Rejection	PSR	V_S = ±4.5V to ±5.5V		55	60		dB
Open-Loop Voltage Gain	A_{OL}	V_{OUT} = ±2.0V, V_{CM} = 0V	R_L = ∞	53	58		dB
			R_L = 100Ω	51	56		
Quiescent Supply Current	I_{SY}	V_{IN} = 0V			5	6	mA
Output Voltage Swing	V_{OUT}	R_L = ∞		±3.5	±3.8		V
		R_L = 100Ω		±3.1	±3.5		
Output Current		R_L = 30Ω, T_A = 0°C to +85°C		65	80		mA
Short-Circuit Output Current	I_{SC}	Short to ground or either supply voltage			90		mA

ELECTRICAL CHARACTERISTICS (continued)

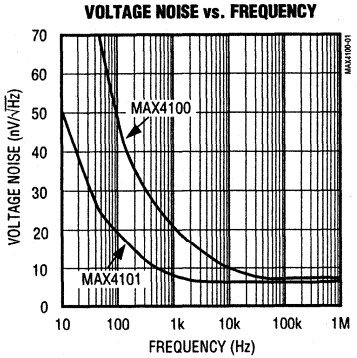
(V_{CC} = 5V, V_{EE} = -5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
AC SPECIFICATIONS							
-3dB Bandwidth	BW	$V_{OUT} \le 0.1V_{RMS}$	MAX4100		500		MHz
			MAX4101		200		
0.1dB Bandwidth		MAX4100, A_{VCL} = +1			65		MHz
		MAX4100, A_{VCL} = +2			50		
Slew Rate	SR	-2V ≤ V_{OUT} ≤ 2V			250		V/µs
Settling Time	t_S	-1V ≤ V_{OUT} ≤ 1V, R_L = 100Ω	to 0.1%		18		ns
			to 0.01%		35		
Rise/Fall Times	t_R, t_F	10% to 90%, -2V ≤ V_{OUT} ≤ 2V, R_L = 100Ω			13		ns
		10% to 90%, -50mV ≤ V_{OUT} ≤ 50mV, R_L = 100Ω			1.5		
Differential Gain	DG	f = 3.58MHz	MAX4100, A_{VCL} = +1		0.06		%
			MAX4101, A_{VCL} = +2		0.07		
Differential Phase	DP	f = 3.58MHz	MAX4100, A_{VCL} = +1		0.04		degrees
			MAX4101, A_{VCL} = +2		0.04		
Input Capacitance	C_{IN}				2		pF
Output Resistance	R_{OUT}	f = 10MHz	MAX4100, A_{VCL} = +1		0.8		Ω
			MAX4101, A_{VCL} = +2		0.3		
Spurious-Free Dynamic Range	SFDR	f_C = 5MHz, V_{OUT} = $2V_{p-p}$	MAX4100, A_{VCL} = +1		-70		dBc
			MAX4101, A_{VCL} = +2		-65		
Third-Order Intercept		f_C = 10MHz, A_{VCL} = +2			36		dBm

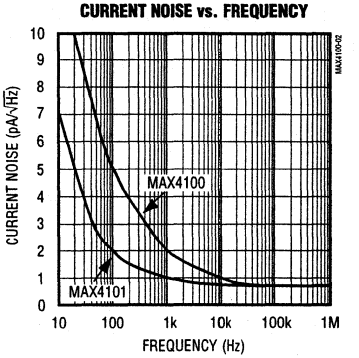
Typical Operating Characteristics

(V_{CC} = 5V, V_{EE} = -5V, T_A = +25°C, unless otherwise noted.)

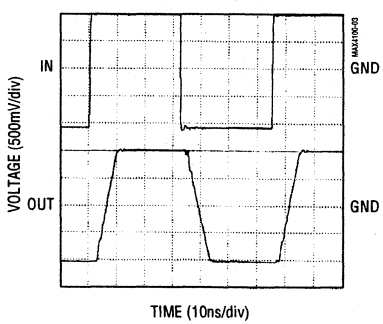
VOLTAGE NOISE vs. FREQUENCY



CURRENT NOISE vs. FREQUENCY



MAX4100 LARGE-SIGNAL PULSE RESPONSE (A_{VCL} = +1)

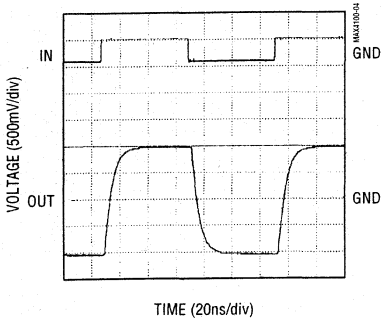


500MHz, Low-Power Op Amps

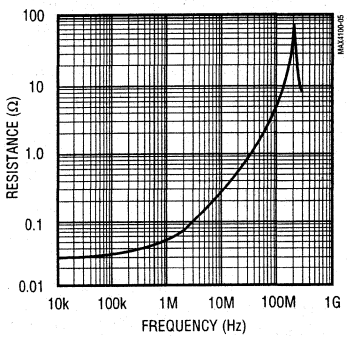
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{EE} = -5V, T_A = +25°C, unless otherwise noted.)

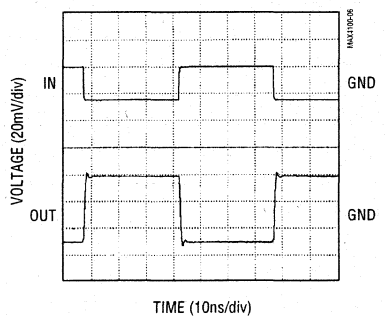
MAX4100
LARGE-SIGNAL PULSE RESPONSE
(A_{VCL} = +5)



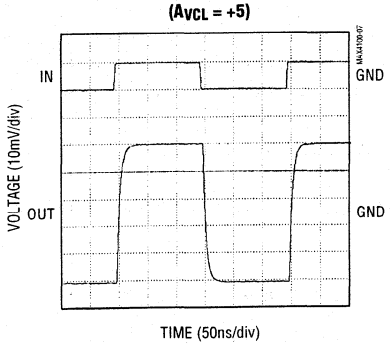
MAX4100
OUTPUT RESISTANCE vs. FREQUENCY



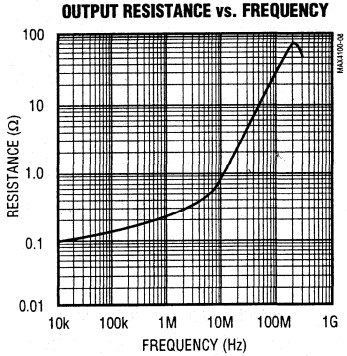
MAX4100
SMALL-SIGNAL PULSE RESPONSE
(A_{VCL} = +1)



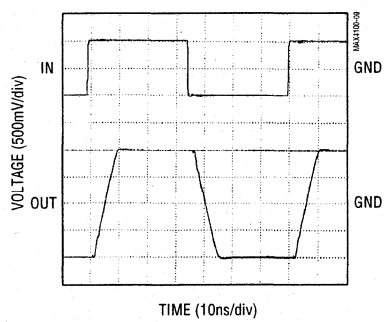
MAX4100
SMALL-SIGNAL PULSE RESPONSE
(A_{VCL} = +5)



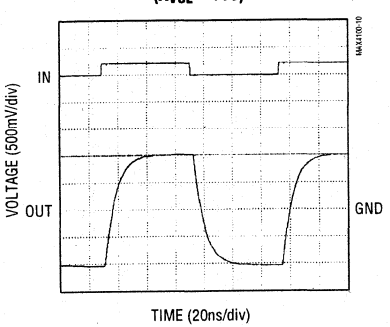
MAX4101
OUTPUT RESISTANCE vs. FREQUENCY



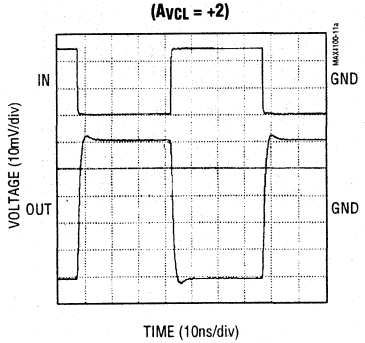
MAX4101
LARGE-SIGNAL PULSE RESPONSE
(A_{VCL} = +2)



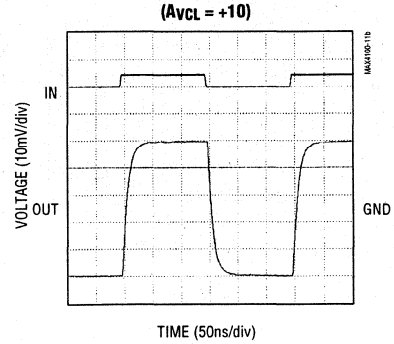
MAX4101
LARGE-SIGNAL PULSE RESPONSE
(A_{VCL} = +10)



MAX4101
SMALL-SIGNAL PULSE RESPONSE
(A_{VCL} = +2)



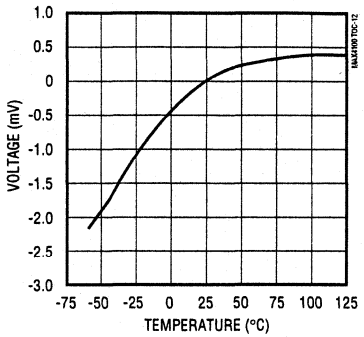
MAX4101
SMALL-SIGNAL PULSE RESPONSE
(A_{VCL} = +10)



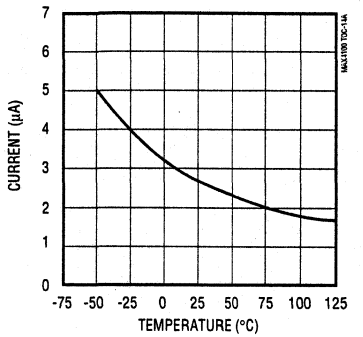
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{EE} = -5V, T_A = +25°C, unless otherwise noted.)

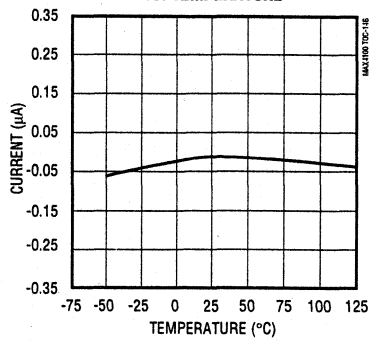
INPUT OFFSET VOLTAGE vs. TEMPERATURE



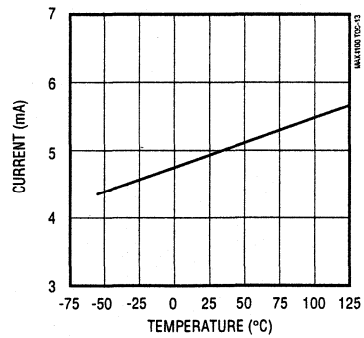
INPUT BIAS CURRENT vs. TEMPERATURE



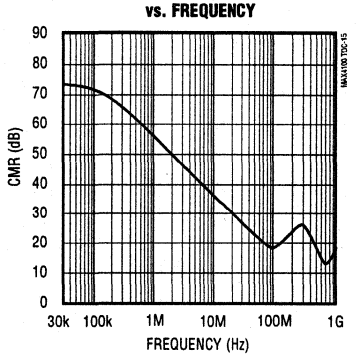
INPUT OFFSET CURRENT vs. TEMPERATURE



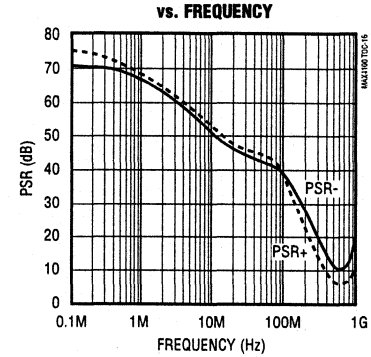
POWER-SUPPLY CURRENT vs. TEMPERATURE



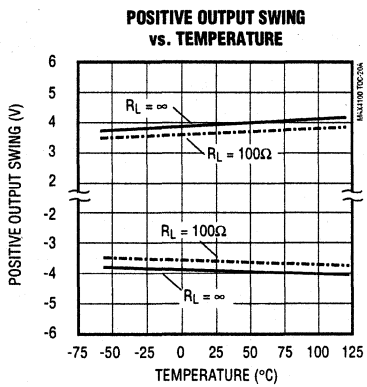
MAX4100 COMMON-MODE REJECTION vs. FREQUENCY



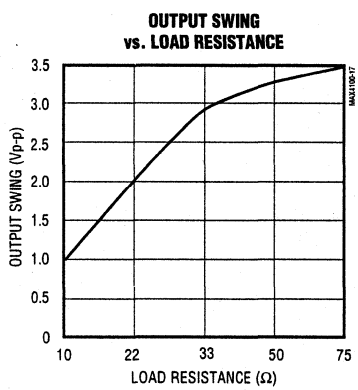
MAX4100 POWER-SUPPLY REJECTION vs. FREQUENCY



POSITIVE OUTPUT SWING vs. TEMPERATURE



OUTPUT SWING vs. LOAD RESISTANCE



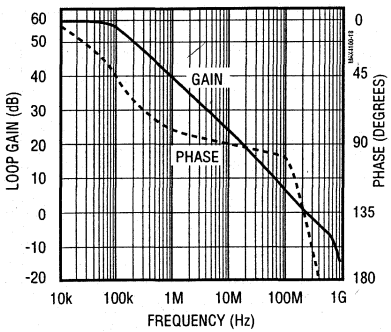
8

500MHz, Low-Power Op Amps

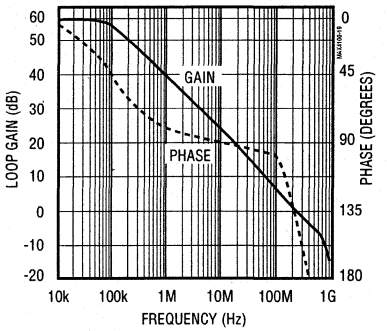
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{EE} = -5V, T_A = +25°C, unless otherwise noted.)

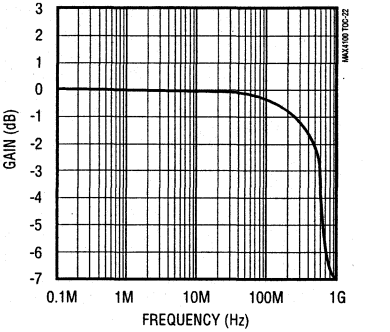
MAX4100 OPEN-LOOP GAIN AND PHASE vs. FREQUENCY



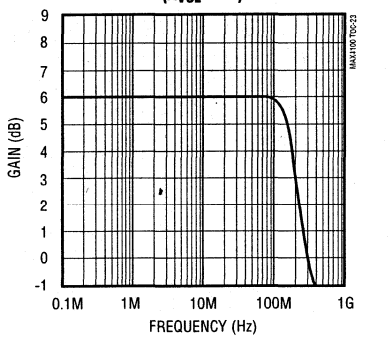
MAX4101 OPEN-LOOP GAIN AND PHASE vs. FREQUENCY



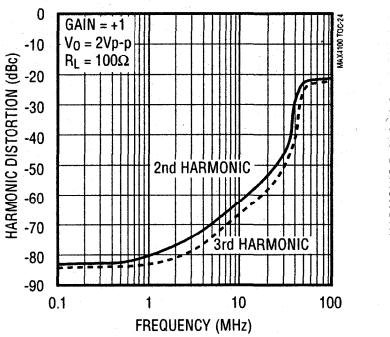
MAX4100 CLOSED-LOOP RESPONSE (A_{VCL} = +1)



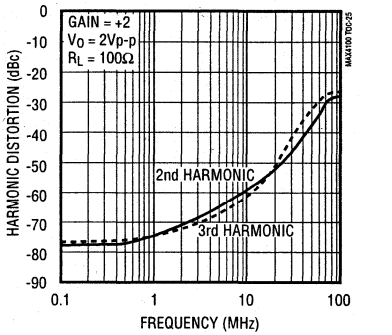
MAX4101 CLOSED-LOOP RESPONSE (A_{VCL} = +2)



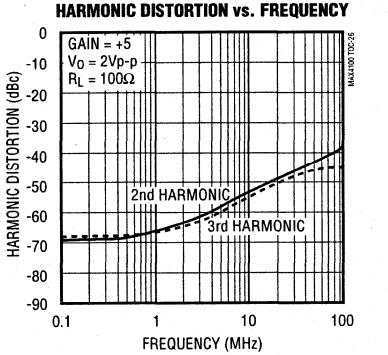
MAX4100 HARMONIC DISTORTION vs. FREQUENCY



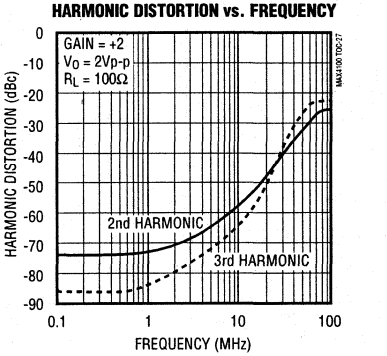
MAX4100 HARMONIC DISTORTION vs. FREQUENCY



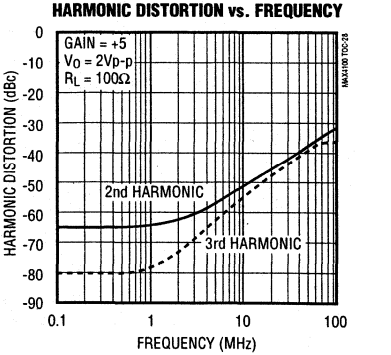
MAX4100 HARMONIC DISTORTION vs. FREQUENCY



MAX4101 HARMONIC DISTORTION vs. FREQUENCY



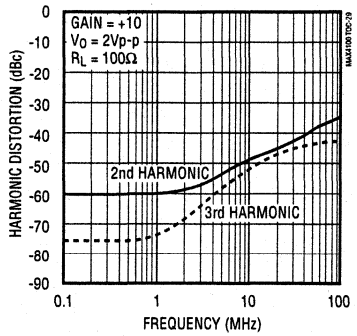
MAX4101 HARMONIC DISTORTION vs. FREQUENCY



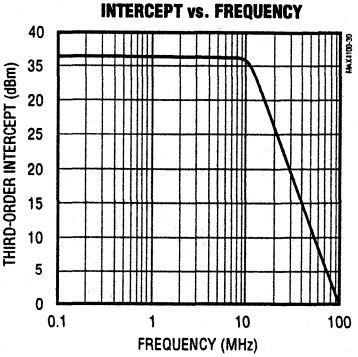
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{EE} = -5V, T_A = +25°C, unless otherwise noted.)

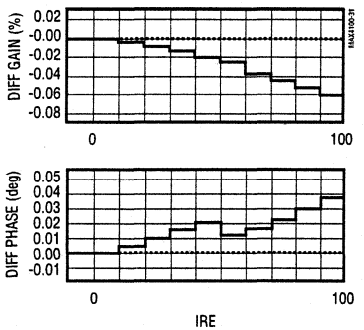
MAX4101
HARMONIC DISTORTION vs. FREQUENCY



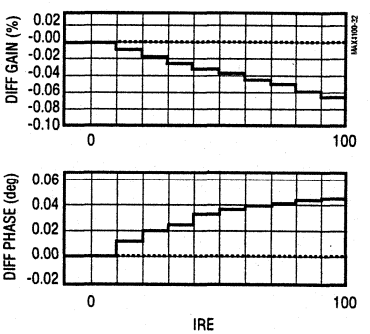
TWO-TONE THIRD-ORDER
INTERCEPT vs. FREQUENCY



MAX4100
DIFFERENTIAL GAIN AND PHASE



MAX4101
DIFFERENTIAL GAIN AND PHASE



8

Pin Description

PIN	NAME	FUNCTION
1, 5, 8	N.C.	No Connection, not internally connected
2	IN-	Inverting Input
3	IN+	Noninverting Input
4	V_{EE}	Negative Power Supply, connected to -5V
6	OUT	Amplifier Output
7	V_{CC}	Positive Power Supply, connected to +5V

500MHz, Low-Power Op Amps

Detailed Description

The MAX4100/MAX4101 are low-power, high-bandwidth operational amplifiers optimized for driving back-terminated cables in composite video, RGB, and RF systems. The MAX4100 is unity-gain stable, and the MAX4101 is optimized for closed-loop gains greater than or equal to 2V/V ($A_{VCL} \geq 2V/V$). While consuming only 5mA (6mA max) supply current, both devices can drive 50Ω back-terminated cables to ±3.1V minimum.

The MAX4100 features a bandwidth in excess of 500MHz and a 0.1dB gain flatness of 65MHz. It offers differential gain and phase errors of 0.06%/0.04°, respectively. The MAX4101 features a -3dB bandwidth of 200MHz, a 0.1dB bandwidth of 50MHz, and 0.07%/0.04° differential gain and phase.

Available in small 8-pin SO and µMAX packages, these ICs are ideally suited for use in portable systems (in RGB, broadcast, or consumer video applications) that benefit from low power consumption.

Applications Information

Layout and Power-Supply Bypassing

The MAX4100/MAX4101 have an RF bandwidth and, consequently, require careful board layout. Depending on the size of the PC board used and the frequency of operation, it may be desirable to use constant-impedance microstrip or stripline techniques.

To realize the full AC performance of this high-speed amplifier, pay careful attention to power-supply bypassing and board layout. The PC board should have at least two layers: a signal and power layer on one side, and a large, low-impedance ground plane on the other side. The ground plane should be as free of voids as possible. With multilayer boards, locate the ground plane on a layer that incorporates no signal or power traces.

Regardless of whether a constant-impedance board is used, it is best to observe the following guidelines when designing the board. Wire-wrap boards are much too inductive, and breadboards are much too capacitive; neither should be used. IC sockets increase parasitic capacitance and inductance, and should not be used. In general, surface-mount components give better high-frequency performance than through-hole components. They have shorter leads and lower parasitic reactances. Keep lines as short and as straight as possible. Do not make 90° turns; round all corners.

High-frequency bypassing techniques must be observed to maintain the amplifier accuracy. The bypass capacitors should include a 1000pF ceramic capacitor between each supply pin and the ground plane, located as close to the package as possible. Next, place a 0.01µF to 0.1µF ceramic capacitor in parallel with each 1000pF capacitor, and as close to each as possible. Then place a 10µF to 15µF low-ESR tantalum at the point of entry (to the PC board) of the power-supply pins. The power-supply trace should lead directly from the tantalum capacitor to the V_{CC} and V_{EE} pins. To minimize parasitic inductance, keep PC traces short and use surface-mount components.

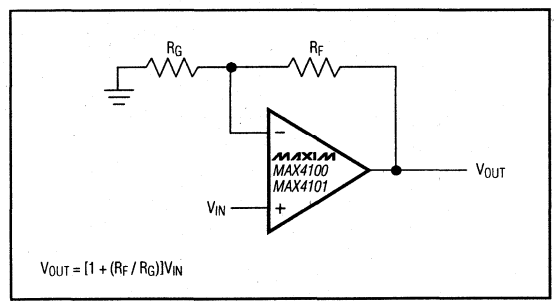


Figure 1b. Noninverting Gain Configuration

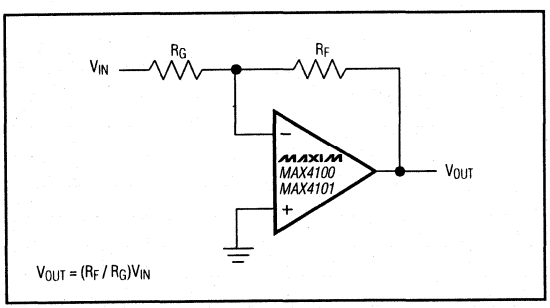


Figure 1a. Inverting Gain Configuration

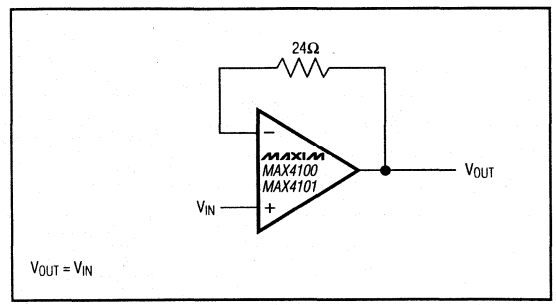


Figure 1c. MAX4100 Unity-Gain Buffer Configuration

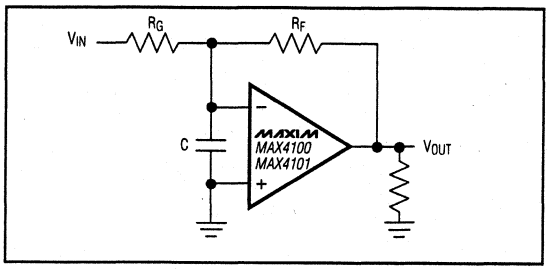


Figure 2. Effect of Feedback Resistor Values and Parasitic Capacitance on Bandwidth

Setting Gain

The MAX4100/MAX4101 are voltage-feedback op amps that can be configured as an inverting or noninverting gain block, as shown in Figures 1a and 1b. The gain is determined by the ratio of two resistors and does not affect amplifier frequency compensation.

In the unity-gain configuration (as shown in Figure 1c), maximum bandwidth and stability is achieved with the MAX4100 when a small feedback resistor is included. This resistor suppresses the negative effects of parasitic inductance and capacitance. A value of 24Ω provides the best combination of wide bandwidth, low peaking, and fast settling time. In addition, this resistor reduces the errors from input bias currents.

Choosing Resistor Values

The values of feedback and input resistors used in the inverting or noninverting gain configurations are not critical (as is the case with current feedback amplifiers). However, take care when selecting because the ohmic values need to be kept small and noninductive for practical reasons.

The input capacitance of the MAX4100/MAX4101 is approximately 2pF. In either the inverting or noninverting configuration, the bandwidth limit caused by the package capacitance and resistor time constant is $f_{3dB} = 1 / (2\Pi RC)$, where R is the parallel combination of the input and feedback resistors (R_F and R_G in Figure 2) and C is the package and board capacitance at the inverting input. Table 1 shows the bandwidth limit for several values of R_F and R_G, assuming 4pF total capacitance (2pF for the MAX4100/MAX4101 and 2pF of PC board parasitics).

Table 1. Resistor and Bandwidth Values for Various Gain Configurations

GAIN (V/V)	R_G (Ω)	R_F (Ω)	BANDWIDTH LIMIT* (MHz)
+1	∞	24	1659
+2	200	200	398
+5	50	200	995
+10	30	270	1474
-1	200	200	398
-2	75	150	796
-5	50	250	955
-10	50	500	875

** Assuming an infinite bandwidth amplifier.*

Resistor Types

Surface-mount resistors are the best choice for high-frequency circuits. They are of similar material to the metal film resistors, but are deposited using a thick-film process in a flat, linear manner so that inductance is minimized. Their small size and lack of leads also minimize parasitic inductance and capacitance, thereby yielding more predictable performance.

DC and Noise Errors

There are several major error sources to be considered in any operational amplifier. These apply equally to the MAX4100/MAX4101. Offset-error terms are given by the equation below. Voltage and current noise errors are root-square summed, so are computed separately. Using the circuit in Figure 3, the total output offset voltage is determined by:

a) The input offset voltage (V_{OS}) times the closed-loop gain ($1 + R_F / R_G$)

b) The positive input bias current (I_{B+}) times the source resistor (R_S) minus the negative input bias current (I_{B-}) times the parallel combination of R_G and R_F. I_{OS} (offset current) is the difference between the two bias currents. If $R_G \,||\, R_F = R_S$, this part of the expression becomes $I_{OS} \times R_S$.

The equation for total DC error is:

$$V_{OUT} = (I_{OS}R_S + V_{OS})\left(1 + \frac{R_F}{R_G}\right)$$

500MHz, Low-Power Op Amps

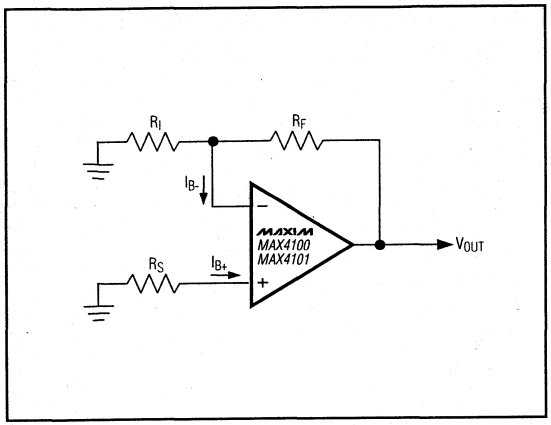


Figure 3. Output Offset Voltage

c) Total output-referred noise voltage is shown by the equation below ($e_{n(OUT)}$):

$$e_{n(OUT)} = \left(1+\frac{R_F}{R_G}\right)\sqrt{(2i_nR_S)^2+(e_N)^2}$$

The MAX4100/MAX4101, with two high-impedance inputs, have low 8nV/√Hz voltage noise and only 0.8pA/√Hz current noise.

An example of DC error calculations, using the MAX4100/MAX4101 typical data and the typical operating circuit with $R_F = R_G = 200\Omega$ ($R_S = 100\Omega$), gives:

$$V_{OUT} = (I_{OS}R_S + V_{OS})\left(1+\frac{R_F}{R_G}\right)$$

$$V_{OUT} = \left(3\times10^{-6}\times10^{2}+1\times10^{-3}\right)(1+1)$$

$$V_{OUT} = 2.6mV$$

Calculating total output-referred noise in a similar manner yields:

$$e_{n(OUT)} = (1+1)\sqrt{\left(2\times0.8\times10^{-12}\times100\right)^2+\left(8\times10^{-9}\right)^2}$$

$$e_{n(OUT)} = 8nV/\sqrt{Hz}$$

With a 200MHz system bandwidth, this calculates to 133μV_{RMS} (approximately 679μV_{p-p}).

In both DC and noise calculations, errors are dominated by offset voltage and noise voltage (rather than by input bias current or noise current).

Metal-film resistors with leads are manufactured using a thin-film process, where resistive material is deposited in a spiral layer around a ceramic rod. Although the materials used are noninductive, the spiral winding presents a small inductance (about 5nH) that may have an adverse effect on high-frequency circuits.

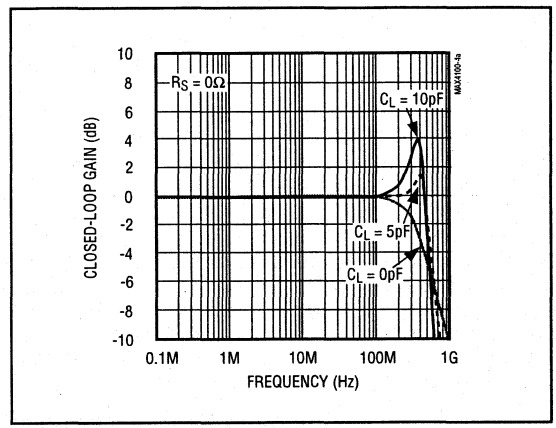


Figure 4a. MAX4100 Bandwidth vs. Capacitive Load

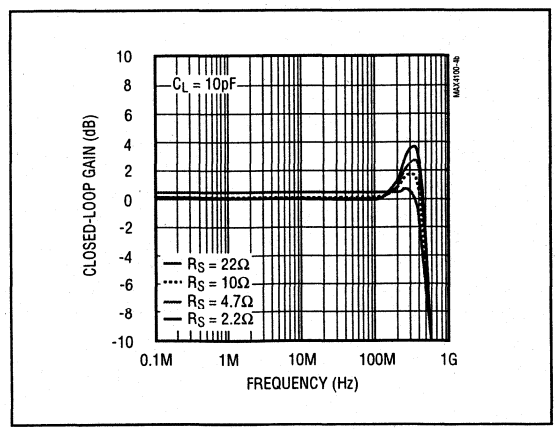


Figure 4b. MAX4100 Bandwidth vs. Capacitive Load and Isolation Resistor

Carbon composition resistors with leads are manufactured by pouring the resistor material into a mold. This process yields a relatively low-inductance resistor that is very useful in high-frequency applications, although they tend to cost more and have more thermal noise than other types. The ability of carbon composition resistors to self-heal after a large current overload makes them useful in high-power RF applications.

For general-purpose use, surface-mount metal-film resistors seem to have the best overall performance for low cost, low inductance, and low noise.

Driving Capacitive Loads

When driving 50Ω or 75Ω back-terminated transmission lines, capacitive loading is not an issue; therefore an isolation resistor is not required. For other applications where the ability to drive capacitive loads is required, the MAX4100/MAX4101 can typically drive 5pF and 20pF, respectively. Figure 4a illustrates how a capacitive load influences the amplifier's peaking without an isolation resistor (R_S). Figure 4b shows how an isolation resistor decreases the amplifier's peaking.

The MAX4100/MAX4101 can drive capacitive loads up to 5pF. By using a small isolation resistor between the amplifier output and the load, large capacitance values may be driven without oscillation (Figure 5a). In most cases, less than 50Ω is sufficient. Use Figure 5b to determine the value needed in your application. Determine the worst-case maximum capacitive load you may encounter and select the appropriate resistor from the graph.

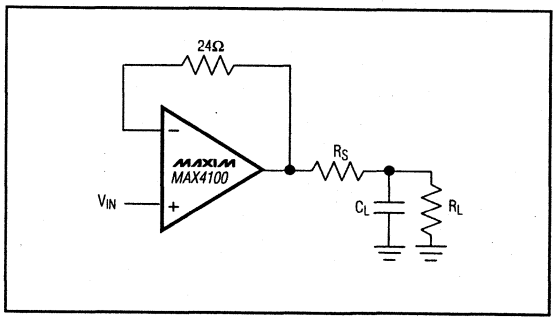


Figure 5a. Using an Isolation Resistor for High Capacitive Loads (MAX4100)

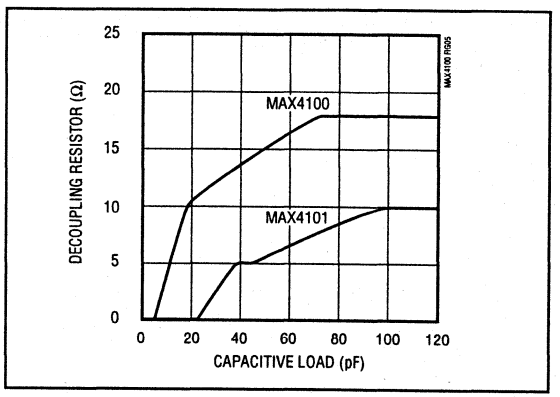


Figure 5b. Isolation vs. Capacitive Load

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19-0471; Rev 0; 2/96

EVALUATION KIT AVAILABLE

MAXIM

250MHz, Broadcast-Quality, Low-Power Video Op Amps

General Description

The MAX4102/MAX4103 op amps combine high-speed performance and ultra-low differential gain and phase while drawing only 5mA of supply current. The MAX4102 is compensated for unity-gain stability, while the MAX4103 is compensated for a closed-loop gain (A_{VCL}) of 2V/V or greater.

The MAX4102/MAX4103 deliver a 250MHz -3dB bandwidth (MAX4102) or a 180MHz -3dB bandwidth (MAX4103). Differential gain and phase are an ultra-low 0.002%/0.002° (MAX4102) and 0.008%/0.003° (MAX4103), making these amplifiers ideal for composite video applications.

These high-speed op amps have a wide output voltage swing of ±3.4V (R_L = 100Ω) and 80mA current-drive capability.

Applications

Broadcast and High-Definition TV Systems

Pulse/RF Amplifier

ADC/DAC Amplifier

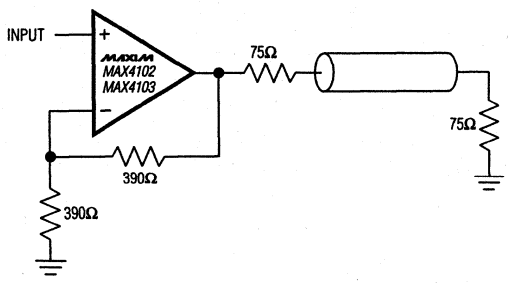
Features

- **250MHz -3dB Bandwidth (MAX4102)**
  180MHz -3dB Bandwidth (MAX4103)
- **Unity-Gain Stable (MAX4102)**
- **350V/µs Slew Rate**
- **Lowest Differential Gain/Phase (R_L = 150Ω)**
  MAX4102: 0.002%/0.002°
  MAX4103: 0.008%/0.003°
- **Low Distortion (SFDR 5MHz): -78dBc**
- **100dB Open-Loop Gain**
- **High Output Drive: 80mA**
- **Low Power: 5mA Supply Current**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4102ESA	-40°C to +85°C	8 SO
MAX4103ESA	-40°C to +85°C	8 SO

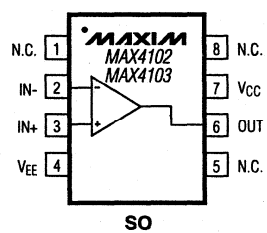
Typical Application Circuit



VIDEO CABLE DRIVER

Pin Configuration

TOP VIEW



SO

8

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

250MHz, Broadcast-Quality, Low-Power Video Op Amps

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to V_{EE}) 12V
Voltage on Any Pin to Ground or Any Other Pin ..... V_{CC} to V_{EE}
Short-Circuit Duration (V_{OUT} to GND) ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
SO (derate 5.88mW/°C above +70°C) 471mW

Operating Temperature Range
MAX4102ESA/MAX4103ESA ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, V_{EE} = -5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC SPECIFICATIONS							
Input Offset Voltage	V_{OS}	V_{OUT} = 0V			0.5	8	mV
Input Offset Voltage Drift	TCV_{OS}	V_{OUT} = 0V			5		µV/°C
Input Bias Current	I_B	V_{OUT} = 0V, V_{IN} = -V_{OS}			3	9	µA
Input Offset Current	I_{OS}	V_{OUT} = 0V, V_{IN} = -V_{OS}			0.04	0.5	µA
Common-Mode Input Resistance	R_{INCM}	Either input			5		MΩ
Common-Mode Input Capacitance	C_{INCM}	Either input			1		pF
Input Voltage Noise	e_n	f = 100kHz	MAX4102		7		nV/√Hz
			MAX4103		5		
Integrated Voltage Noise		f = 1MHz to 100MHz	MAX4102		88		$µV_{RMS}$
			MAX4103		63		
Input Current Noise	i_n	f = 100kHz	MAX4102		1.0		pA/√Hz
			MAX4103		1.0		
Integrated Current Noise		f = 1MHz to 100MHz	MAX4102		12.5		nA_{RMS}
			MAX4103		12.5		
Common-Mode Input Voltage	V_{CM}			-2.5		2.5	V
Common-Mode Rejection	CMR	V_{CM} = ±2.5V		75	100		dB
Power-Supply Rejection	PSR	V_S = ±4.5V to ±5.5V		70	100		dB
Open-Loop Voltage Gain	A_{VOL}	V_{OUT} = ±2.0V, V_{CM} = 0V	R_L = ∞	66	96		dB
			R_L = 100Ω	70	100		
Quiescent Supply Current	I_{SY}	V_{IN} = 0V			4.6	6	mA
Output Voltage Swing	V_{OUT}	R_L = ∞		±3.3	±3.7		V
		R_L = 100Ω		±3.1	±3.4		
Output Current		R_L = 30Ω, T_A = 0°C to +85°C		65	80		mA
Short-Circuit Output Current	I_{SC}	Short to ground or either supply voltage			90		mA

250MHz, Broadcast-Quality, Low-Power Video Op Amps

AC ELECTRICAL CHARACTERISTICS

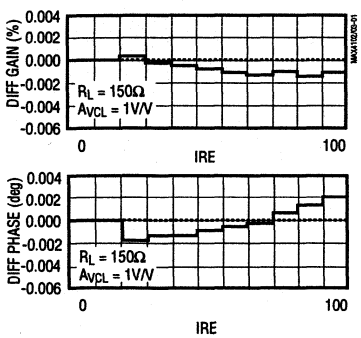
(V_{CC} = 5V, V_{EE} = -5V, R_L = 100Ω, A_{VCL} = +1 (MAX4102), A_{VCL} = +2 (MAX4103), T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
AC SPECIFICATIONS							
-3dB Bandwidth	BW	$V_{OUT} \le 0.1V_{RMS}$	MAX4102		250		MHz
			MAX4103		180		
0.1dB Bandwidth		MAX4102			130		MHz
		MAX4103			80		
Slew Rate	SR	$-2V \le V_{OUT} \le 2V$			350		V/µs
Settling Time	t_S	$-1V \le V_{OUT} \le 1V$	to 0.1%		18		ns
			to 0.01%		30		
Rise/Fall Times	t_R, t_F	10% to 90%, $-2V \le V_{OUT} \le 2V$			13		ns
		10% to 90%, $-50mV \le V_{OUT} \le 50mV$			1.5		
Differential Gain	DG	f = 3.58MHz, R_L = 150Ω	MAX4102		0.002		%
			MAX4103		0.008		
Differential Phase	DP	f = 3.58MHz, R_L = 150Ω	MAX4102		0.002		degrees
			MAX4103		0.003		
Input Capacitance	C_{IN}				2		pF
Output Resistance	R_{OUT}	f = 10MHz	MAX4102		0.7		Ω
			MAX4103		0.7		
Spurious-Free Dynamic Range	SFDR	f_C = 5MHz, $V_{OUT} = 2V_{p-p}$	MAX4102		-78		dBc
			MAX4103		-76		

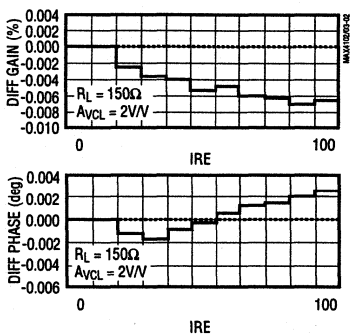
Typical Operating Characteristics

(V_{CC} = 5V, V_{EE} = -5V, R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

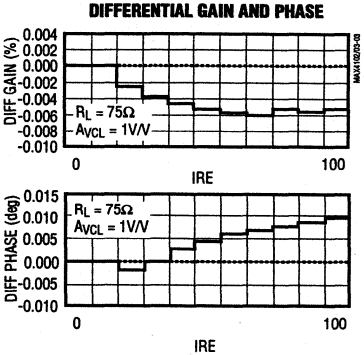
MAX4102
DIFFERENTIAL GAIN AND PHASE



MAX4103
DIFFERENTIAL GAIN AND PHASE



MAX4102
DIFFERENTIAL GAIN AND PHASE

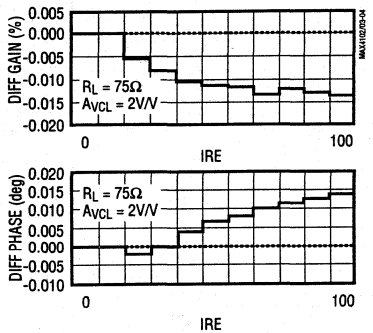


250MHz, Broadcast-Quality, Low-Power Video Op Amps

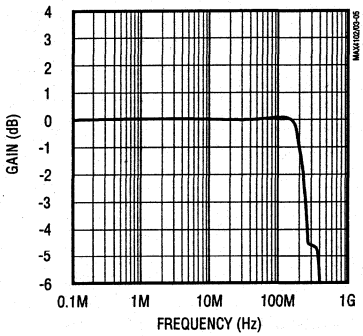
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{EE} = -5V, R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

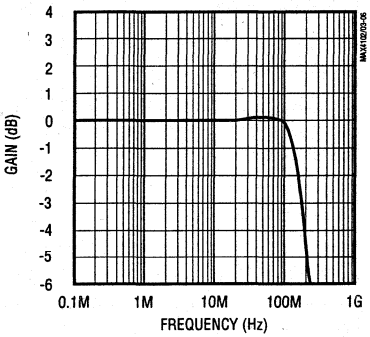
MAX4103
DIFFERENTIAL GAIN AND PHASE



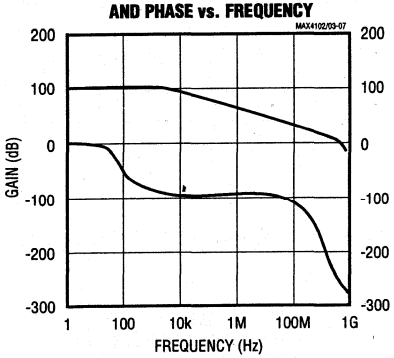
MAX4102
SMALL-SIGNAL GAIN vs. FREQUENCY (A_{VCL} = +1)



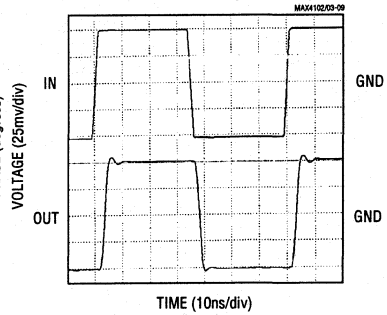
MAX4103
SMALL-SIGNAL GAIN vs. FREQUENCY (A_{VCL} = +2)



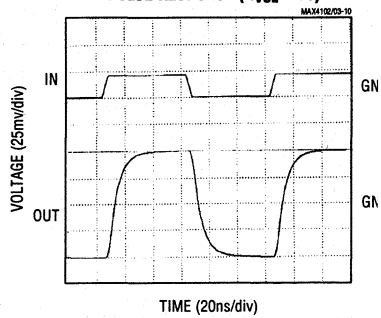
MAX4102/MAX4103
OPEN-LOOP GAIN AND PHASE vs. FREQUENCY



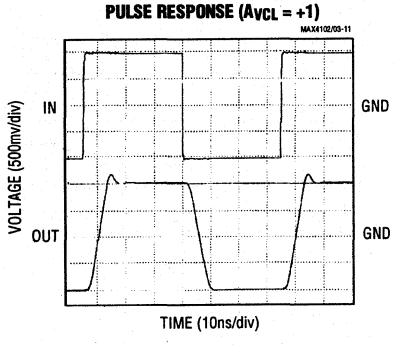
MAX4102
SMALL-SIGNAL PULSE RESPONSE (A_{VCL} = +1)



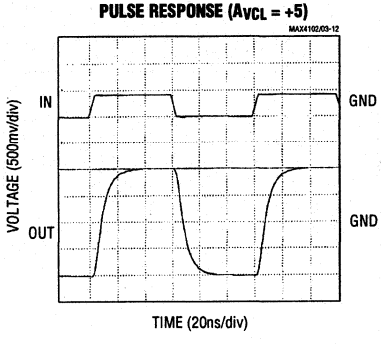
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SMALL-SIGNAL PULSE RESPONSE (A_{VCL} = +5)



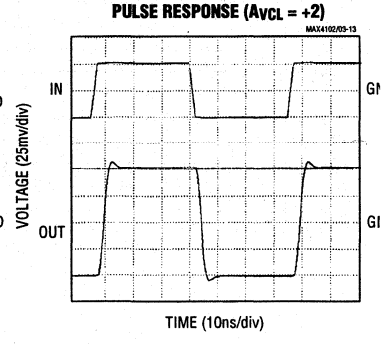
MAX4102
LARGE-SIGNAL PULSE RESPONSE (A_{VCL} = +1)



MAX4102
LARGE-SIGNAL PULSE RESPONSE (A_{VCL} = +5)



MAX4103
SMALL-SIGNAL PULSE RESPONSE (A_{VCL} = +2)

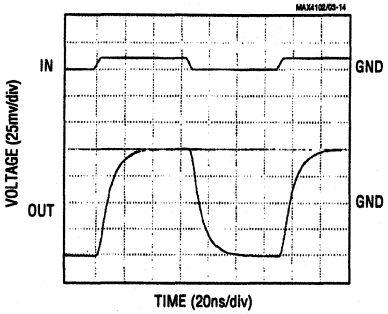


250MHz, Broadcast-Quality, Low-Power Video Op Amps

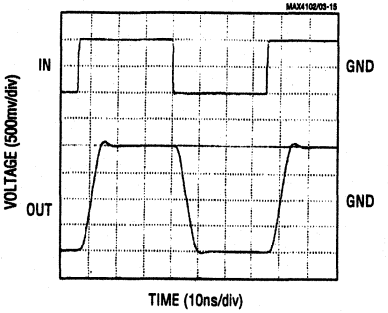
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{EE} = -5V, R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

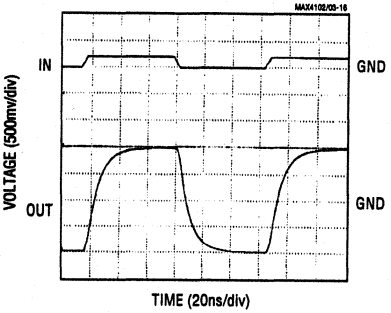
MAX4103 SMALL-SIGNAL PULSE RESPONSE (A_{VCL} = +10)



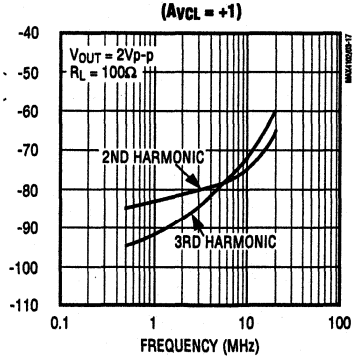
MAX4103 LARGE-SIGNAL PULSE RESPONSE (A_{VCL} = +2)



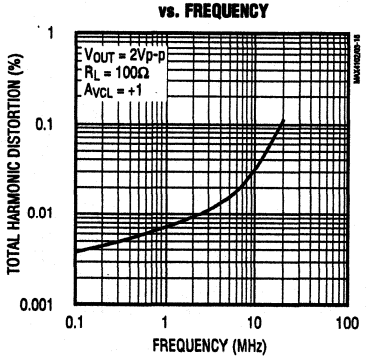
MAX4103 LARGE-SIGNAL PULSE RESPONSE (A_{VCL} = +10)



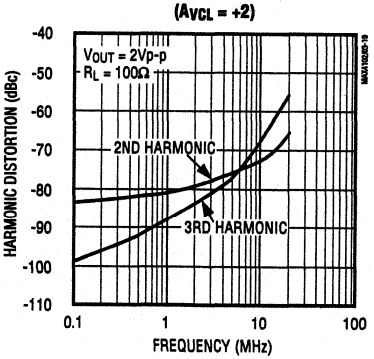
MAX4102 DISTORTION vs. FREQUENCY (A_{VCL} = +1)



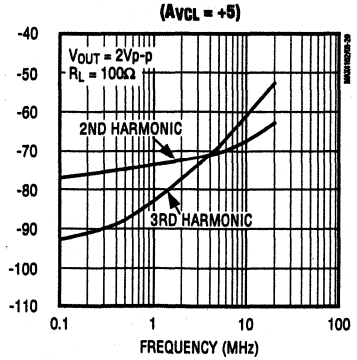
MAX4102 TOTAL HARMONIC DISTORTION vs. FREQUENCY



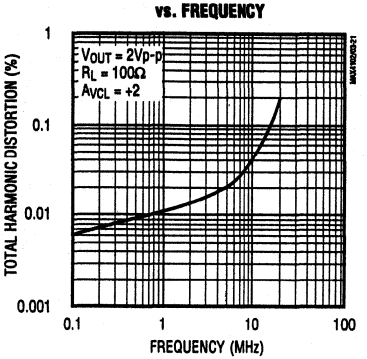
MAX4103 DISTORTION vs. FREQUENCY (A_{VCL} = +2)



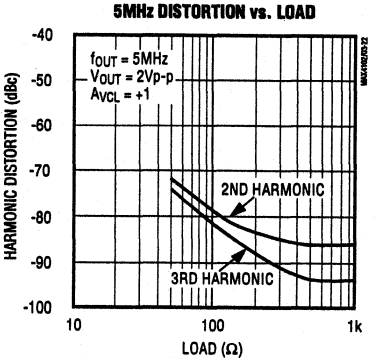
MAX4103 DISTORTION vs. FREQUENCY (A_{VCL} = +5)



MAX4103 TOTAL HARMONIC DISTORTION vs. FREQUENCY



MAX4102 5MHz DISTORTION vs. LOAD



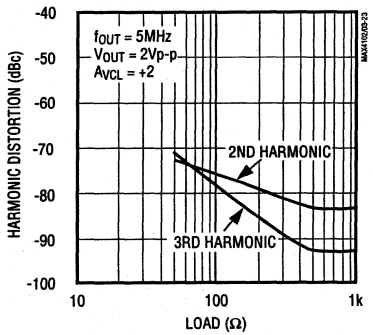
8

250MHz, Broadcast-Quality, Low-Power Video Op Amps

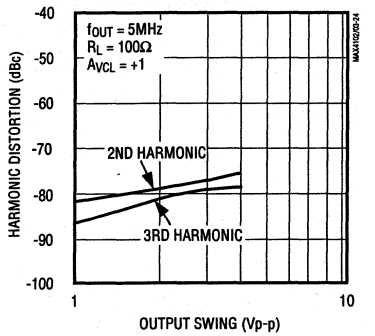
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{EE} = -5V, R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

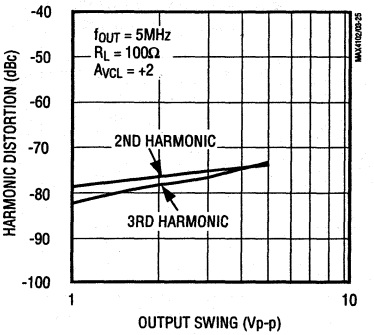
MAX4103
5MHz DISTORTION vs. LOAD



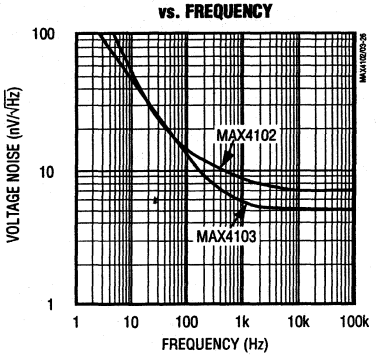
MAX4102
5MHz DISTORTION vs. OUTPUT SWING



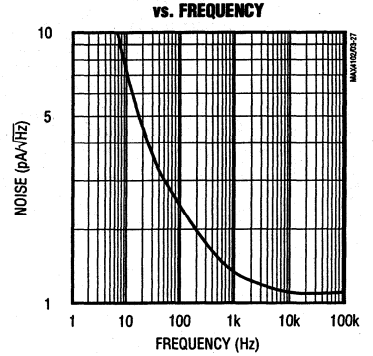
MAX4103
5MHz DISTORTION vs. OUTPUT SWING



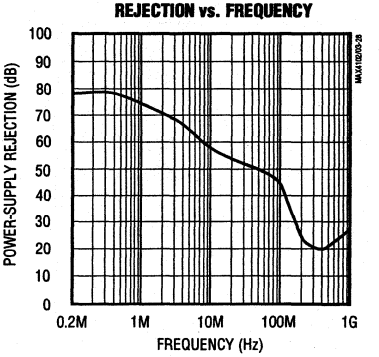
INPUT VOLTAGE NOISE
vs. FREQUENCY



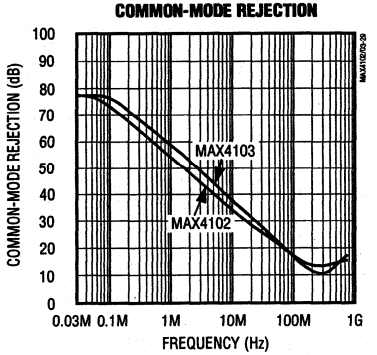
INPUT CURRENT NOISE
vs. FREQUENCY



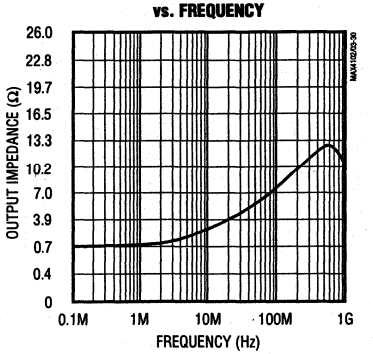
POWER-SUPPLY
REJECTION vs. FREQUENCY



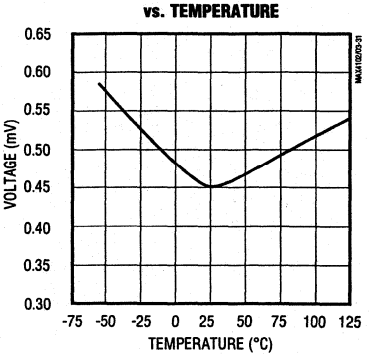
COMMON-MODE REJECTION



OUTPUT RESISTANCE
vs. FREQUENCY



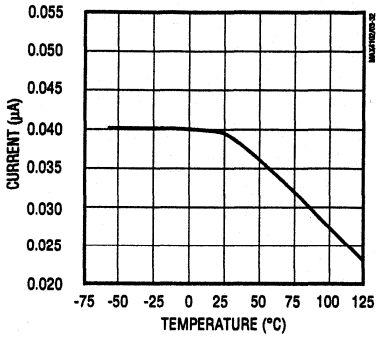
INPUT OFFSET VOLTAGE
vs. TEMPERATURE



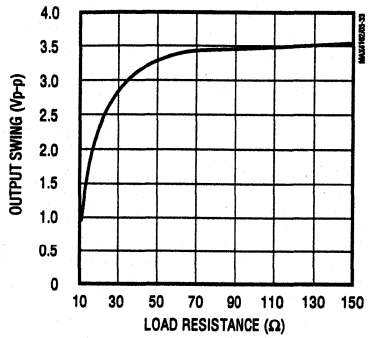
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{EE} = -5V, R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

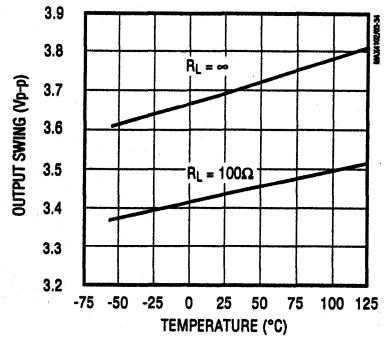
INPUT OFFSET CURRENT vs. TEMPERATURE



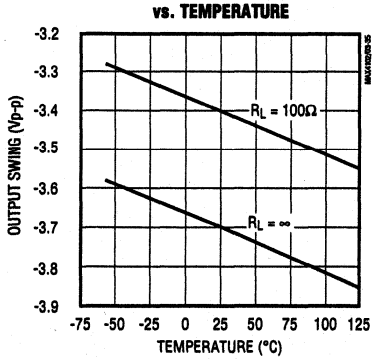
OUTPUT SWING vs. LOAD RESISTANCE



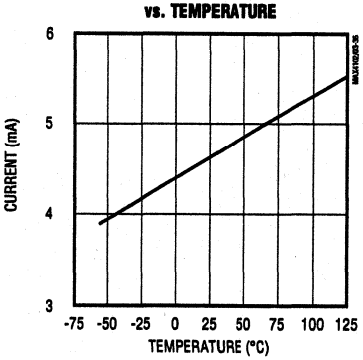
POSITIVE OUTPUT SWING vs. TEMPERATURE



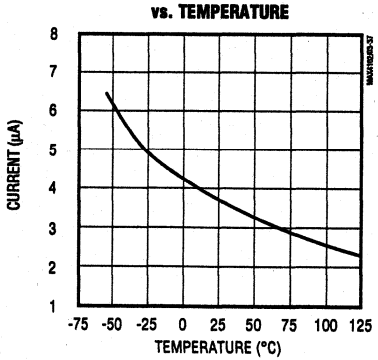
NEGATIVE OUTPUT SWING vs. TEMPERATURE



POWER-SUPPLY CURRENT vs. TEMPERATURE



INPUT BIAS CURRENT vs. TEMPERATURE



250MHz, Broadcast-Quality, Low-Power Video Op Amps

Pin Description

PIN	NAME	FUNCTION
1	N.C.	Not internally connected
2	IN-	Inverting Input
3	IN+	Noninverting Input
4	V_{EE}	Negative Power Supply. Connect to -5V
5	N.C.	Not internally connected
6	OUT	Amplifier Output
7	V_{CC}	Positive Power Supply. Connect to +5V
8	N.C.	Not internally connected

Detailed Description

The MAX4102/MAX4103 low-power, high-speed op amps feature ultra-low differential gain and phase, and are optimized for the highest quality video applications. Differential gain and phase errors are 0.002%/0.002° for the MAX4102 and 0.008%/0.003° for the MAX4103. The MAX4102 also features a -3dB bandwidth of over 250MHz and 0.1dB gain-flatness of 130MHz. The MAX4103 features a -3dB bandwidth of 180MHz and a 0.1dB bandwidth of 80MHz.

The MAX4102 is unity-gain stable, and the MAX4103 is optimized for closed-loop gains of 2V/V (6dB) and higher. Both devices drive back-terminated 50Ω or 75Ω cables to ±3.1V (min) and deliver an output current of 80mA.

Available in a small 8-pin SO package, the MAX4102/MAX4103 are ideal for high-definition TV systems (in RGB, broadcast, or consumer video applications) that benefit from low power consumption and superior differential gain and phase characteristics.

Applications Information

Grounding, Bypassing, and PC Board Layout

In order to achieve the full bandwidth, Microstrip and Stripline techniques are recommended in most cases. To ensure your PC board does not degrade the amp's performance, it's wise to design the board for a frequency greater than 1GHz. Even with very short runs, it's good practice to use this technique at critical points, such as inputs and outputs. Whether you use a constant-impedance board or not, observe the following guidelines when designing the board:

- Do not use wire-wrap boards, because they are too inductive.
- Do not use IC sockets. They increase parasitic capacitance and inductance.
- In general, surface-mount components have shorter leads and lower parasitic reactance, and give better high-frequency performance than through-hole components.
- The PC board should have at least two layers, with one side a signal layer and the other a ground plane.
- Keep signal lines as short and as straight as possible. Do not make 90° turns; round all corners.
- The ground plane should be as free from voids as possible.

On Maxim's evaluation kit, the ground plane has been removed from areas where keeping the trace capacitance to a minimum is more important than maintaining ground continuity. For example, the ground plane has been removed from beneath the IC to minimize pin capacitance.

The bypass capacitors should include a 0.1µF at each supply pin and the ground plane, located as close to the package as possible. Then place a 10µF to 15µF low-ESR tantalum at the point of entry (to the PC board) of the power-supply pins. The power-supply trace should lead directly from the tantalum capacitor to the V_{CC} and V_{EE} pins to maintain the low differential gain and phase of these devices.

Setting Gain

The MAX4102/MAX4103 are voltage-feedback op amps that can be configured as an inverting or noninverting gain block, as shown in Figures 1a and 1b. The gain is determined by the ratio of two resistors and does not affect amplifier frequency compensation.

In the unity-gain configuration (Figure 1c), maximum bandwidth and stability are achieved with the MAX4102 when a small feedback resistor is included. This resistor suppresses the negative effects of parasitic inductance and capacitance. A value of 24Ω provides the best combination of wide bandwidth, low peaking, and fast settling time. In addition, this resistor reduces the errors from input bias currents.

Choosing Resistor Values

The values of feedback and input resistors used in the inverting or noninverting gain configurations are not critical (as is the case with current-feedback amplifiers), but should be kept small and noninductive.

The input capacitance of the MAX4102/MAX4103 is approximately 2pF. In either the inverting or noninverting configuration, the bandwidth limit caused by the package capacitance and resistor time constant is $f_{3dB} = 1 / (2\Pi RC)$, where R is the parallel combination of the input and feedback resistors (R_F and R_G in Figure 2) and C is the package and board capacitance at the inverting input. R_{S1} and R_{S2} represent the input termination resistors. Table 1 shows the typical bandwidth and resistor values for several gain configurations.

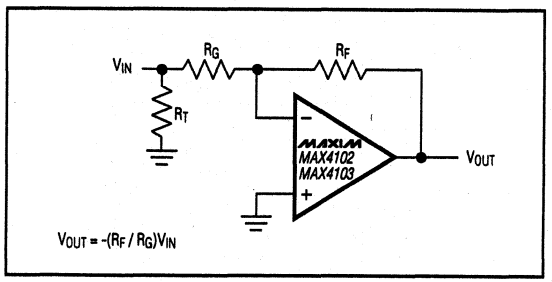


Figure 1a. Inverting Gain Configuration

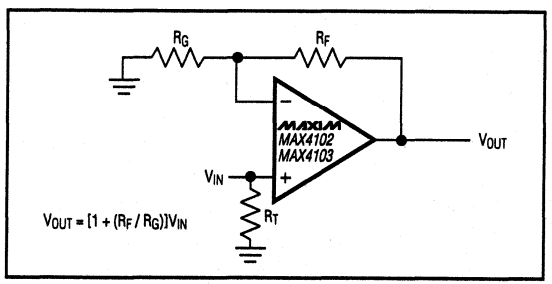


Figure 1b. Noninverting Gain Configuration

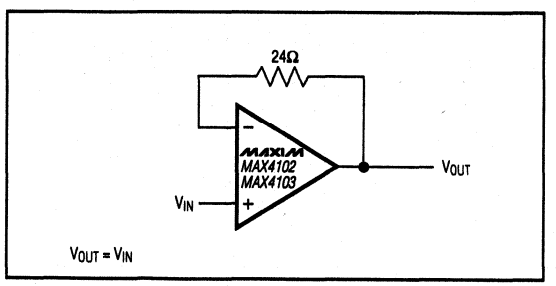


Figure 1c. MAX4102 Unity-Gain Buffer Configuration

Table 1. Resistor and Bandwidth Values for Various Gain Configurations

DEVICE	GAIN (V/V)	R_G (Ω)	R_F (Ω)	R_T (Ω)	BANDWIDTH (MHz)
MAX4102	1	∞	24	50	250
MAX4102	2	200	200	50	100
MAX4103	2	200	200	50	180
MAX4103	5	50	200	50	40
MAX4103	10	30	270	50	20
MAX4103	-1	200	200	56	180
MAX4103	-2	75	150	150	140
MAX4103	-5	50	250	∞	75
MAX4103	-10	50	500	∞	35

Note: Refer to Figure 1a for inverting gain configurations and Figure 1b for noninverting gain configurations. R_T is calculated for 50Ω systems.

Resistor Types

Surface-mount resistors are the best choice for high-frequency circuits. They are of similar material to the metal-film resistors, but are deposited using a thick-film process in a flat, linear manner so that inductance is minimized. Their small size and lack of leads also minimize parasitic inductance and capacitance, thereby yielding more predictable performance.

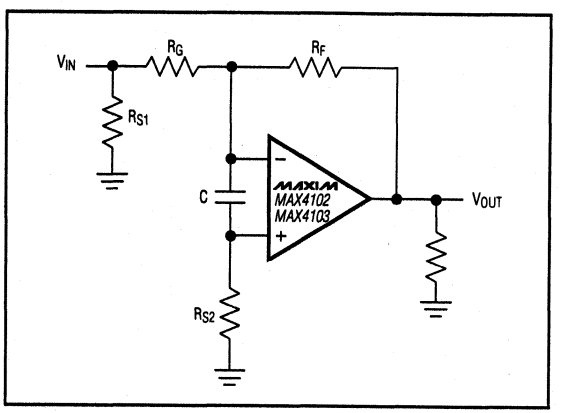


Figure 2. Effect of Feedback Resistor Values and Parasitic Capacitance on Bandwidth

250MHz, Broadcast-Quality, Low-Power Video Op Amps

Driving Capacitive Loads

When driving 50Ω or 75Ω back-terminated transmission lines, capacitive loading is not an issue. The MAX4102/MAX4103 can typically drive 5pF and 20pF, respectively. Figure 3a illustrates how a capacitive load influences the amplifier's peaking without an isolation resistor (R_S). Figure 3b shows how an isolation resistor decreases the amplifier's peaking. By using a small isolation resistor between the amplifier output and the load, large capacitance values may be driven without oscillation (Figure 4a). In most cases, less than 50Ω is sufficient. Use Figure 4b to determine the value needed in your application. Determine the worst-case maximum capacitive load you may encounter and select the appropriate resistor from the graph.

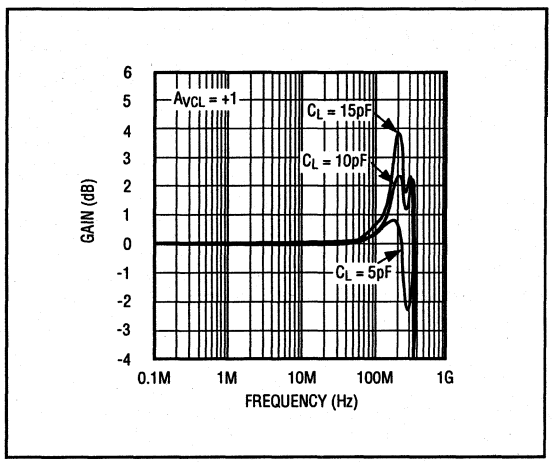


Figure 3a. MAX4102 Bandwidth vs. Capacitive Load (No Isolation Resistor (R_S))

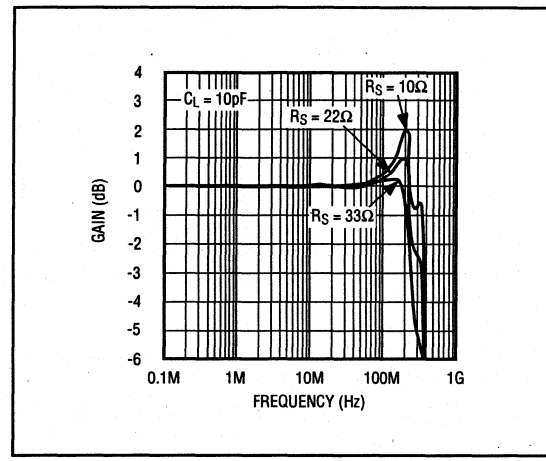


Figure 3b. MAX4102 Bandwidth vs. 10pF Capacitive Load and Isolation Resistor

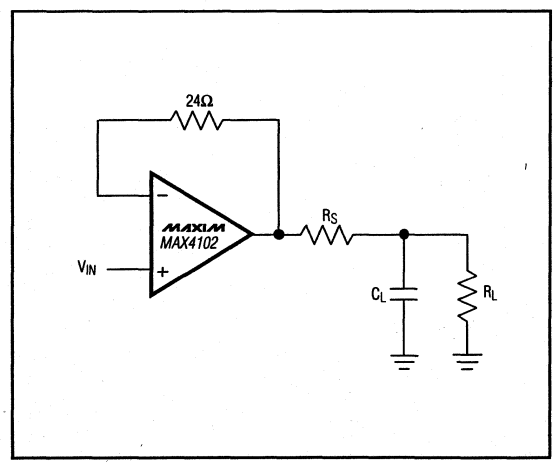


Figure 4a. Using an Isolation Resistor (R_S) for Large Capacitive Loads (MAX4102)

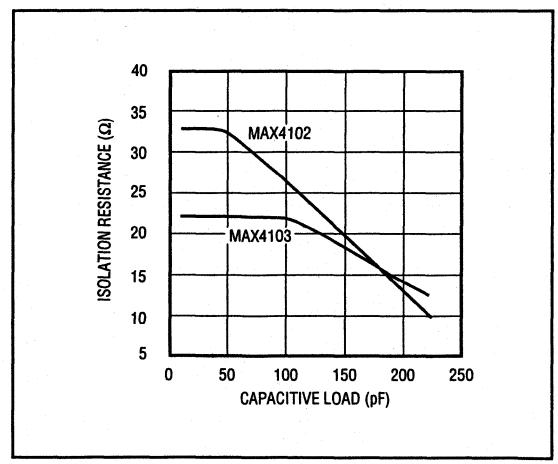


Figure 4b. Isolation vs. Capacitive Load

Chip Information

TRANSISTOR COUNT: 51

SUBSTRATE CONNECTED TO: V_{EE}

19-0442; Rev 1; 11/95

EVALUATION KIT AVAILABLE

MAXIM

350MHz, Ultra-Low-Noise Op Amps

General Description

The MAX4106/MAX4107 op amps combine high-speed performance with ultra-low-noise performance. The MAX4106 is compensated for closed-loop gains of 5V/V, while the MAX4107 is stable in closed-loop gains of 10V/V or greater.

The MAX4106/MAX4107 require only 15mA of supply current while delivering a 350MHz or a 300MHz bandwidth, respectively. Voltage noise is an ultra-low 0.75nV/√Hz, while a low-distortion architecture provides a spurious-free dynamic range (SFDR) of 63dB at 5MHz.

These high-speed op amps have a wide output voltage swing of ±3.2V and a high current-drive capability of 80mA.

Applications

Ultra-Low-Noise ADC Preamp

Ultrasound

Low-Noise Preamplifier

High-Performance Receivers

Active Filters

Pulse/RF Amplifier

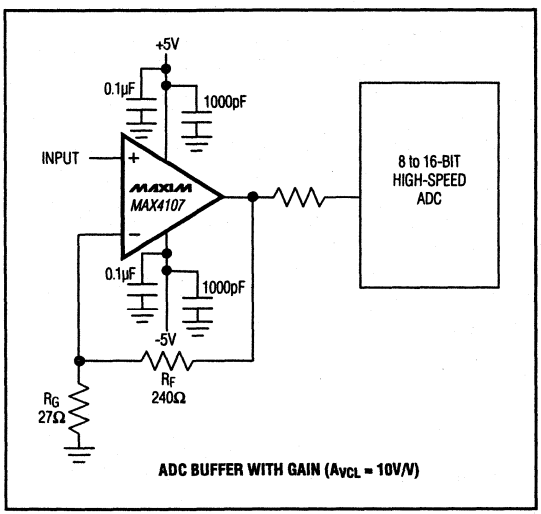
Features

- **350MHz -3dB Bandwidth (MAX4106)**
- **275V/µs Slew Rate (MAX4106)**
  500V/µs Slew Rate (MAX4107)
- **18ns Settling Time to 0.01%**
- **0.75nV/√Hz Voltage Noise**
- **High Output Drive: 80mA**

Ordering Information

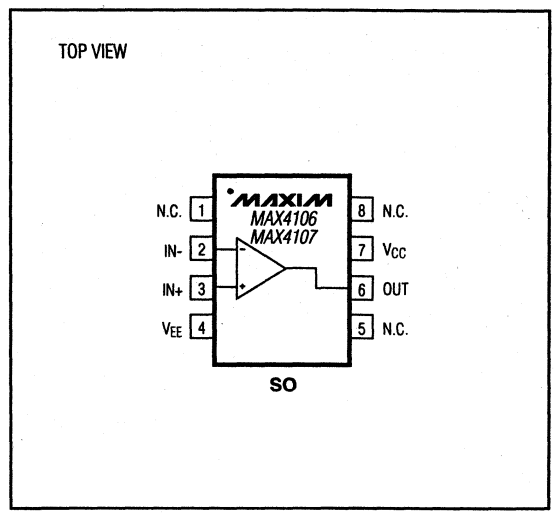
PART	TEMP. RANGE	PIN-PACKAGE
MAX4106ESA	-40°C to +85°C	8 SO
MAX4107ESA	-40°C to +85°C	8 SO

Typical Application Circuit



ADC BUFFER WITH GAIN (A_{VCL} = 10V/V)

Pin Configuration



8

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

350MHz, Ultra-Low-Noise Op Amps

ABSOLUTE MAXIMUM RATINGS

Power-Supply Voltage (V_{CC} to V_{EE}) 12V
Voltage on Any Pin to Ground or Any Other Pin ..... V_{CC} to V_{EE}
Short-Circuit Duration (V_{OUT} to GND) ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
SO (derate 5.88mW/°C above +70°C) 471mW

Operating Temperature Range
MAX4106ESA/MAX4107ESA ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Junction Temperature ..... +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, V_{EE} = -5V, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC SPECIFICATIONS							
Input Offset Voltage	V_{OS}	V_{OUT} = 0V			0.250	3	mV
Input Offset Voltage Drift	TCV_{OS}	V_{OUT} = 0V			1.0		µV/°C
Input Bias Current	I_B	V_{OUT} = 0V, V_{IN} = -V_{OS}			18	26	µA
Input Offset Current	I_{OS}	V_{OUT} = 0V, V_{IN} = -V_{OS}			0.05	2	µA
Common-Mode Input Resistance	R_{INCM}	Either input			1		MΩ
Common-Mode Input Capacitance	C_{INCM}	Either input			1		pF
Input Voltage Noise	e_n	f = 10kHz			0.75		nV/√Hz
Integrated Voltage Noise	E_{nRMS}	f = 1MHz to 100MHz			9.5		$µV_{RMS}$
Input Current Noise	I_n	f = 10kHz			2.5		pA/√Hz
Integrated Current Noise	I_{nRMS}	f = 1MHz to 100MHz			31		nA_{RMS}
Common-Mode Input Voltage	V_{CM}			-2.5		2.5	V
Common-Mode Rejection	CMR	V_{CM} = ±2.5V		70	100		dB
Power-Supply Rejection	PSR	V_S = ±4.5V to ±5.5V		75	100		dB
Open-Loop Voltage Gain	A_{VOL}	V_{OUT} = ±2.0V, V_{CM} = 0V	R_L = ∞	80	100		dB
			R_L = 100Ω	80	100		
Supply Current	I_S	V_{IN} = 0V			15	19	mA
Output Voltage Swing	V_{OUT}	R_L = ∞		±3.2	±3.8		V
		R_L = 100Ω		±3.0	±3.5		
Output Current Drive	I_{OUT}	R_L = 30Ω, T_A = 0°C to +85°C		65	80		mA
Short-Circuit Output Current	I_{SC}	Short to ground			90		mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5V, V_{EE} = -5V, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C, unless otherwise noted.)

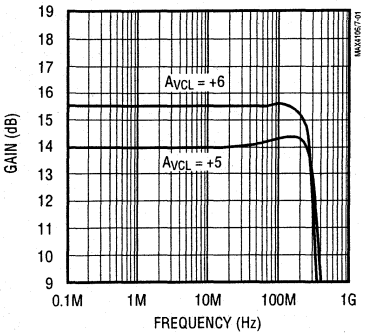
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
AC SPECIFICATIONS							
-3dB Bandwidth	BW_{-3dB}	$V_{OUT} \le 0.1V_{RMS}$	MAX4106		350		MHz
			MAX4107		300		
0.1dB Bandwidth	$BW_{0.1dB}$	MAX4106, A_{VCL} = +5			75		MHz
		MAX4107, A_{VCL} = +10			45		
Slew Rate	SR	-2V ≤ V_{OUT} ≤ 2V	MAX4106		275		V/µs
			MAX4107		500		
Settling Time	t_S	-1V ≤ V_{OUT} ≤ 1V, R_L = 100Ω, to 0.1%	MAX4106		13		ns
			MAX4107		13		
		-1V ≤ V_{OUT} ≤ 1V, R_L = 100Ω, to 0.01%	MAX4106		18		
			MAX4107		18		
Rise/Fall Times	t_R, t_F	10% to 90%, -2V ≤ V_{OUT} ≤ 2V, R_L = 100Ω	MAX4106		13		ns
			MAX4107		6		
		10% to 90%, -50mV ≤ V_{OUT} ≤ 50mV, R_L = 100Ω	MAX4106		1		
			MAX4107		1		
Differential Gain	DG	f = 3.58MHz	MAX4106, A_{VCL} = +5		0.04		%
			MAX4107, A_{VCL} = +10		0.03		
Differential Phase	DP	f = 3.58MHz	MAX4106, A_{VCL} = +5		0.02		degrees
			MAX4107, A_{VCL} = +10		0.03		
Input Capacitance	C_{IN}				2		pF
Output Impedance	Z_{OUT}	f = 10MHz			0.7		Ω
Spurious-Free Dynamic Range	SFDR	f_C = 5MHz, V_{OUT} = 2Vp-p	MAX4106, A_{VCL} = +5		63		dBc
			MAX4107, A_{VCL} = +10		60		
Two-Tone Third-Order Intercept	IP3	f_C = 10MHz			24		dBm

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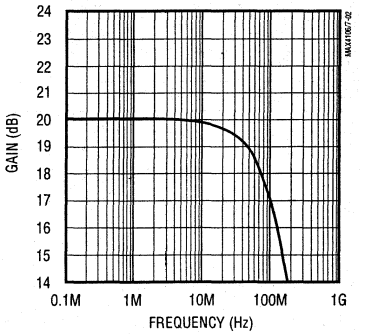
Typical Operating Characteristics

(V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

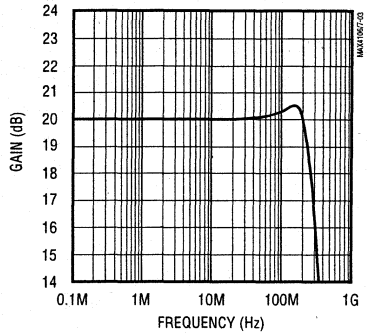
MAX4106
SMALL-SIGNAL GAIN vs. FREQUENCY
(A_{VCL} = +5, +6)



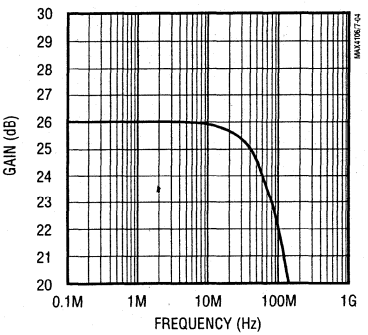
MAX4106
SMALL-SIGNAL GAIN vs. FREQUENCY
(A_{VCL} = +10)



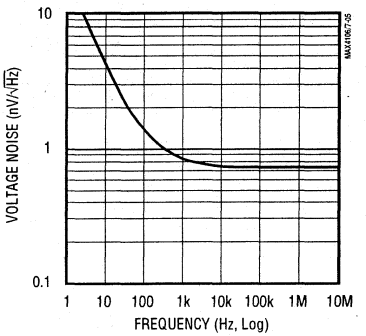
MAX4107
SMALL-SIGNAL GAIN vs. FREQUENCY
(A_{VCL} = +10)



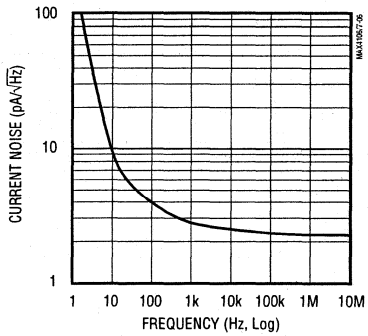
MAX4107
SMALL-SIGNAL GAIN vs. FREQUENCY
(A_{VCL} = +20)



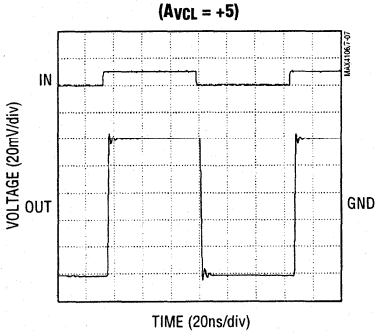
VOLTAGE NOISE
vs. FREQUENCY



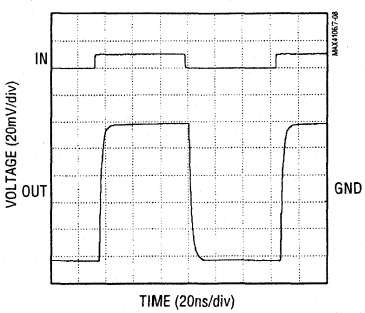
CURRENT NOISE
vs. FREQUENCY



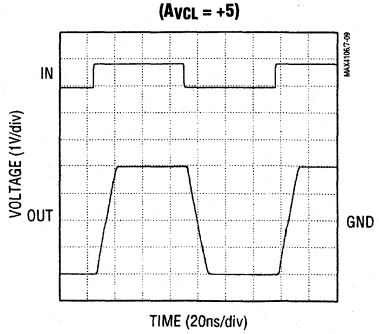
MAX4106
SMALL-SIGNAL PULSE RESPONSE
(A_{VCL} = +5)



MAX4106
SMALL-SIGNAL PULSE RESPONSE
(A_{VCL} = +10)



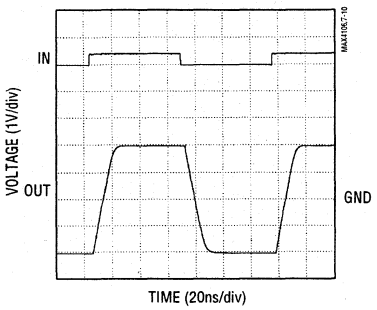
MAX4106
LARGE-SIGNAL PULSE RESPONSE
(A_{VCL} = +5)



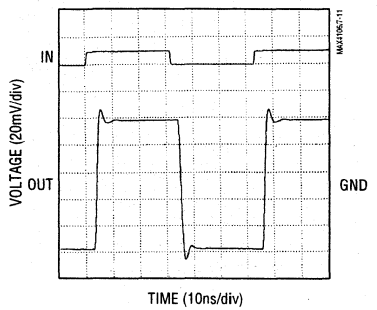
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

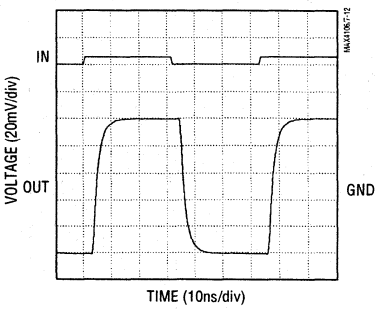
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LARGE-SIGNAL PULSE RESPONSE
(A_{VCL} = +10)



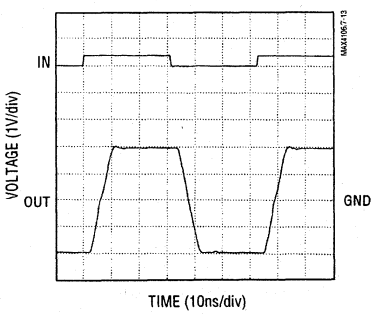
MAX4107
SMALL-SIGNAL PULSE RESPONSE
(A_{VCL} = +10)



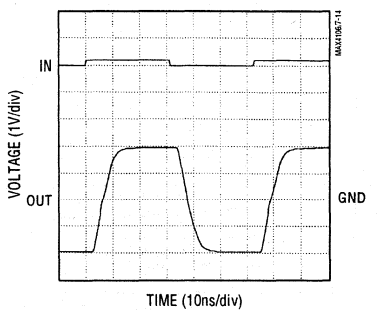
MAX4107
SMALL-SIGNAL PULSE RESPONSE
(A_{VCL} = +20)



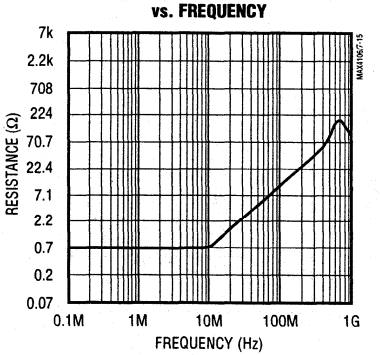
MAX4107
LARGE-SIGNAL PULSE RESPONSE
(A_{VCL} = +10)



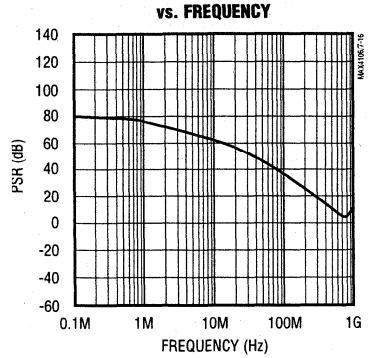
MAX4107
LARGE-SIGNAL PULSE RESPONSE
(A_{VCL} = +20)



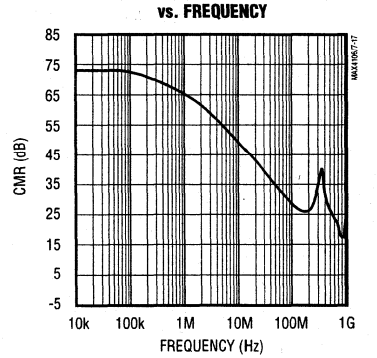
CLOSED-LOOP OUTPUT IMPEDANCE
vs. FREQUENCY



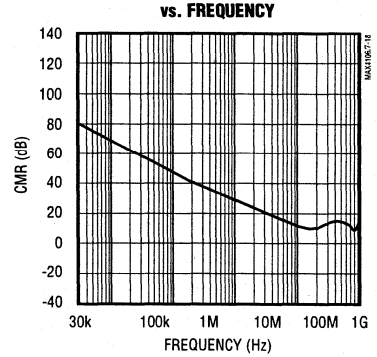
POWER-SUPPLY REJECTION
vs. FREQUENCY



MAX4106
COMMON-MODE REJECTION
vs. FREQUENCY



MAX4107
COMMON-MODE REJECTION
vs. FREQUENCY



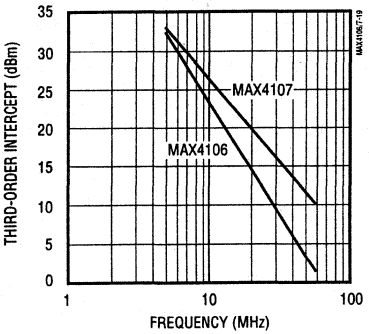
8

350MHz, Ultra-Low-Noise Op Amps

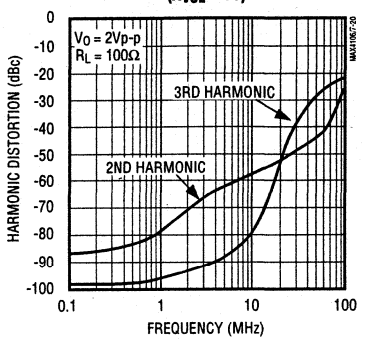
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

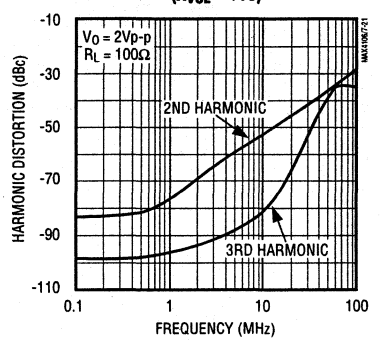
TWO-TONE THIRD-ORDER INTERCEPT vs. FREQUENCY



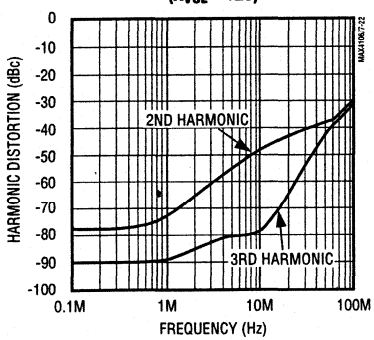
MAX4106 HARMONIC DISTORTION vs. FREQUENCY (A_{VCL} = +5)



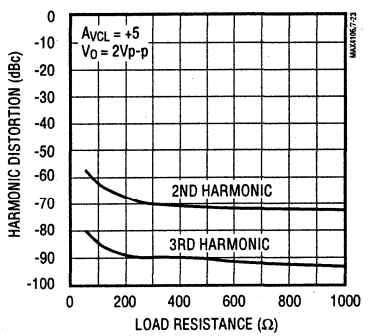
MAX4107 HARMONIC DISTORTION vs. FREQUENCY (A_{VCL} = +10)



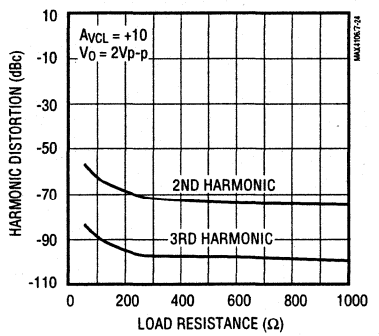
MAX4107 HARMONIC DISTORTION vs. FREQUENCY (A_{VCL} = +20)



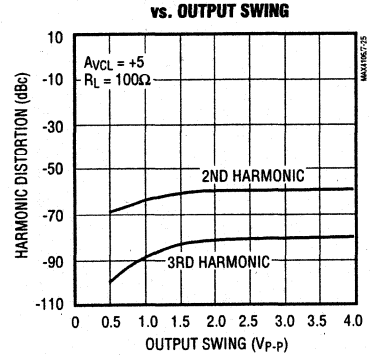
MAX4106 5MHz HARMONIC DISTORTION vs. LOAD RESISTANCE



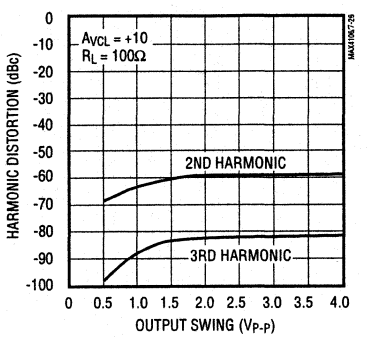
MAX4107 5MHz HARMONIC DISTORTION vs. LOAD RESISTANCE



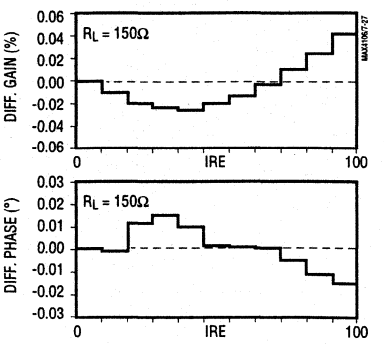
MAX4106 5MHz HARMONIC DISTORTION vs. OUTPUT SWING



MAX4107 5MHz HARMONIC DISTORTION vs. OUTPUT SWING



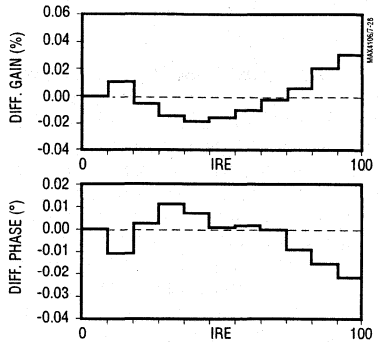
MAX4106 DIFFERENTIAL GAIN AND PHASE



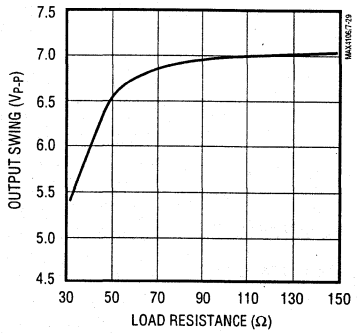
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

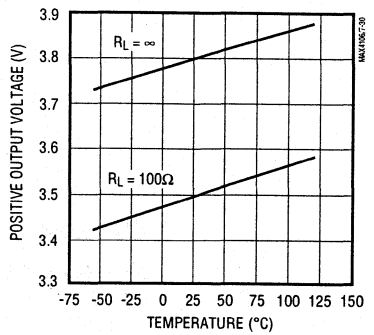
MAX4107 DIFFERENTIAL GAIN AND PHASE



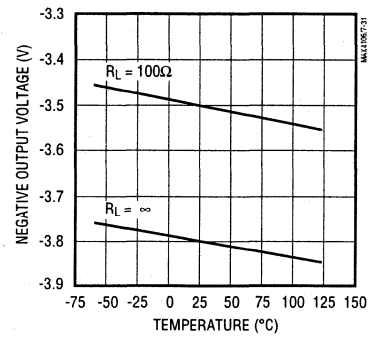
OUTPUT SWING vs. LOAD RESISTANCE



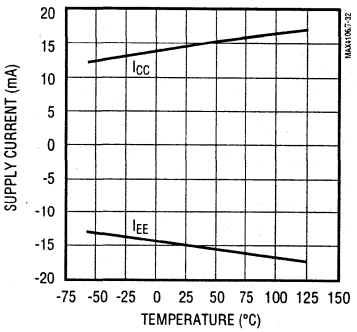
POSITIVE OUTPUT VOLTAGE SWING vs. TEMPERATURE



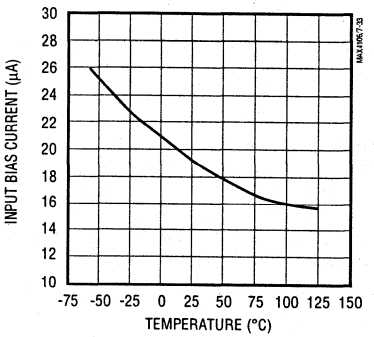
NEGATIVE OUTPUT VOLTAGE SWING vs. TEMPERATURE



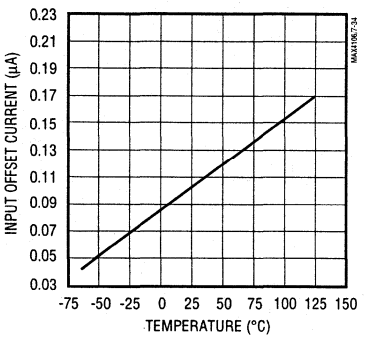
POWER-SUPPLY CURRENT vs. TEMPERATURE



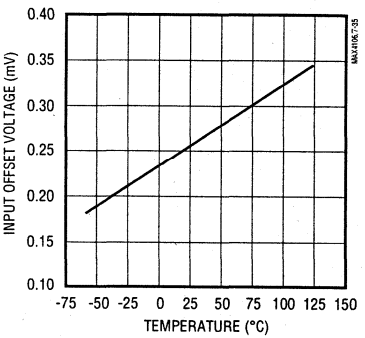
INPUT BIAS CURRENT vs. TEMPERATURE



INPUT OFFSET CURRENT vs. TEMPERATURE



INPUT OFFSET VOLTAGE vs. TEMPERATURE



350MHz, Ultra-Low-Noise Op Amps

Pin Description

PIN	NAME	FUNCTION
1, 5, 8	N.C.	No Connection, not internally connected
2	IN-	Inverting Input
3	IN+	Noninverting Input
4	V_{EE}	Negative Power Supply, connect to -5V
6	OUT	Amplifier Output
7	V_{CC}	Positive Power Supply, connect to +5V

General Description

Choosing Resistor Values

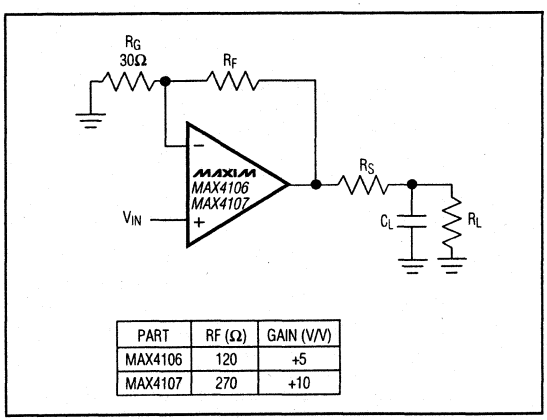
The values of the gain-setting feedback and input resistors are important design considerations. Large resistor values will increase voltage noise, and will interact with the amplifier's input and PC board capacitance to generate undesirable poles and zeros, which can decrease bandwidth or cause oscillations. For example, a noninverting gain of +5 (MAX4106), using a 1kΩ feedback resistor combined with 2pF of input capacitance and 0.5pF of board capacitance, will cause a feedback pole at 318MHz. If this pole is within the anticipated amplifier bandwidth, it will jeopardize stability. Reducing the 1kΩ feedback resistor to 40Ω will extend the pole frequency to 8GHz, but could limit output swing by adding 50Ω in parallel with the amplifier's load. Clearly the selection of resistor values must be tailored to the specific application.

The MAX4106/MAX4107 are ultra-low-noise, high-bandwidth op amps. The output noise voltage can be dominated by resistor thermal noise, so keep the feedback and input resistors small. Setting the input resistor to 30Ω and choosing the feedback resistor to suit the gain will provide excellent AC performance without significantly degrading noise performance.

Driving Capacitive Loads

The MAX4106/MAX4107 are optimized for AC performance. They are not designed to drive highly reactive loads. Reactive loads will decrease phase margin and may produce excessive ringing and oscillation. Figure 1a shows a circuit that eliminates this problem, and Figure 1b is a graph of the optimal isolation resistor (R_S) vs. capacitive load. Figures 2a and 2b show how a capacitive load causes excessive peaking of the amplifier's bandwidth if the capacitive load is not isolated (R_S) from the amplifier. A small isolation resistor (usually 10Ω to 20Ω) placed before the reactive load prevents ringing and oscillation. At higher capacitive loads, AC performance will be controlled by the interaction of the load capacitance and isolation resistor. Figures 3a and 3b show the effect of an isolation resistor on the MAX4106/MAX4107 closed-loop response.

Coaxial cable and other transmission lines are easily driven when terminated at both ends with their characteristic impedance. When driving back-terminated transmission lines, the capacitance of the transmission line is essentially eliminated.



PART	RF (Ω)	GAIN (V/V)
MAX4106	120	+5
MAX4107	270	+10

Figure 1a. Using an Isolation Resistor for High Capacitive Loads

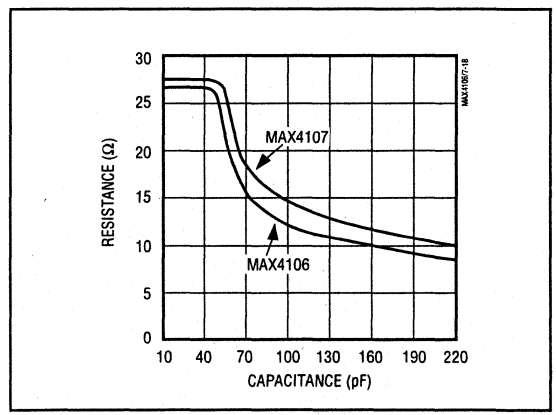


Figure 1b. Optimal Isolation Resistor (R_S) vs. Capacitive Load

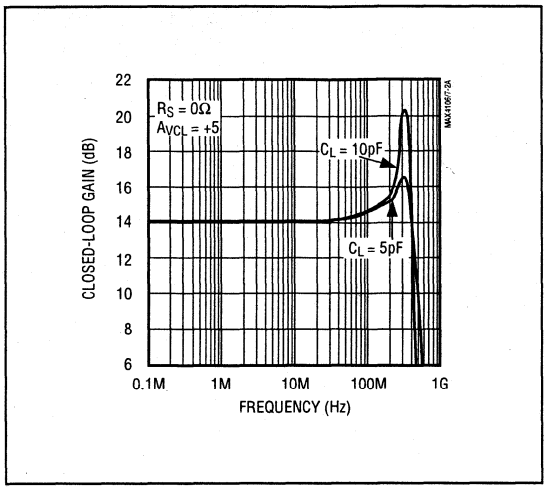


Figure 2a. MAX4106 Response vs. Capacitive Load—No Resistive (R_S) Isolation (circuit shown in Figure 1)

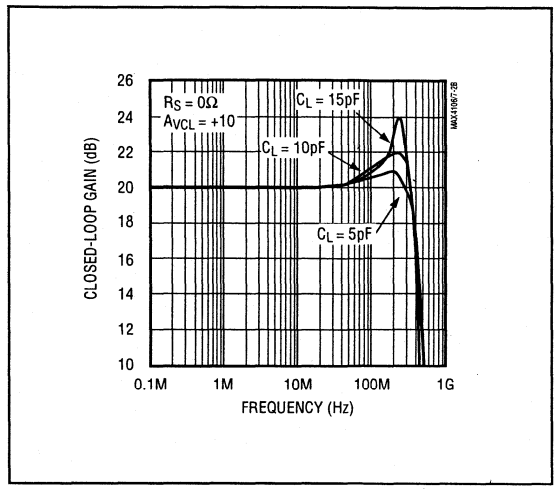


Figure 2b. MAX4107 Response vs. Capacitive Load—No Isolation (R_S) Resistor (circuit shown in Figure 1)

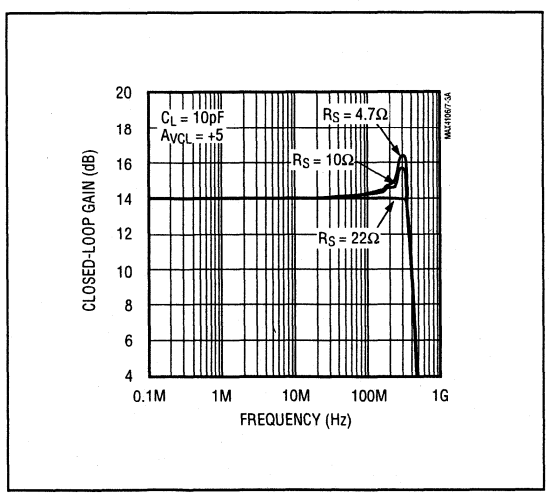


Figure 3a. MAX4106 Response vs. Capacitive Load with Resistive (R_S) Isolation (circuit shown in Figure 1)

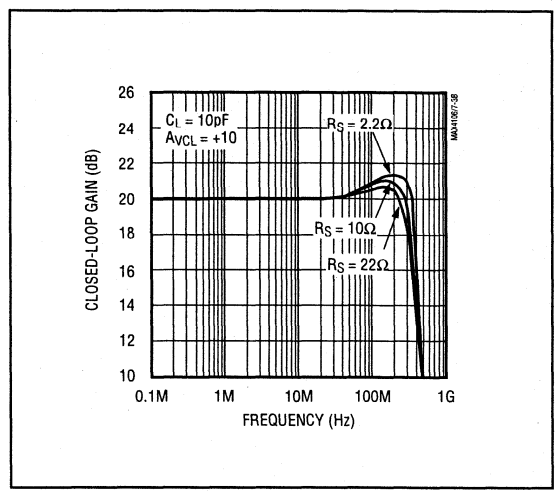


Figure 3b. MAX4107 Response vs. Capacitive Load with Resistive (R_S) Isolation (circuit shown in Figure 1)

Chip Information

TRANSISTOR COUNT: 55

19-0461; Rev 1; 3/96

EVALUATION KIT AVAILABLE

400MHz, Ultra-Low-Distortion Op Amps

General Description

The MAX4108/MAX4109 op amps combine ultra-high-speed performance with low-distortion operation. The MAX4108 is compensated for unity-gain stability, while the MAX4109 is compensated for a closed-loop gain (A_{VCL}) of 2V/V or greater.

The MAX4108 delivers a 400MHz unity-gain bandwidth with a 1200V/µs slew rate, while the MAX4109 provides a 225MHz gain bandwidth with a 1200V/µs slew rate. The low-distortion design provides an unprecedented spurious-free dynamic range of -81dBc and -80dBc, respectively, at 20MHz (V_O = 2Vp-p, R_L = 100Ω), making these amplifiers ideal for high-performance RF signal processing.

These high-speed op amps have a wide output voltage swing and a high current-drive capability of 90mA.

Features

- **400MHz Unity-Gain Bandwidth (MAX4108)**
  225MHz -3dB Bandwidth (MAX4109)
- **1200V/µs Slew Rate**
- **-81dBc SFDR at f_C = 20MHz (MAX4108)**
  -80dBc SFDR at f_C = 20MHz (MAX4109)
- **300MHz Full-Power Bandwidth**
  (MAX4108, V_O = 2Vp-p)
  200MHz Full-Power Bandwidth
  (MAX4109, V_O = 2Vp-p)
- **Voltage Feedback Architecture**
- **High Output Drive: 90mA**
- **Output Short-Circuit Protected**

Applications

RGB and Composite Video

High-Performance Receivers

Pulse/RF Amplifier

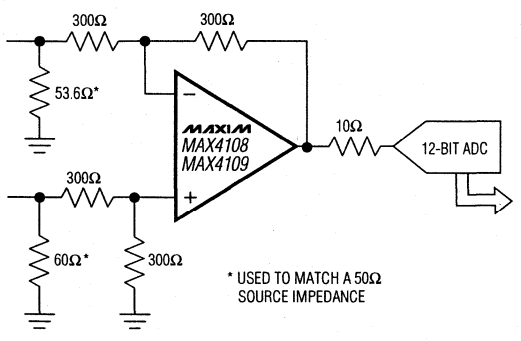
ADC/DAC Preamp

Active Filters

Ordering Information

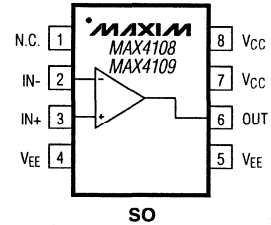
PART	TEMP. RANGE	PIN-PACKAGE
MAX4108ESA	-40°C to +85°C	8 SO
MAX4109ESA	-40°C to +85°C	8 SO

Typical Application Circuit



DIFFERENCE AMPLIFIER/ADC PREAMPLIFIER

Pin Configuration



SO

8

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

400MHz, Ultra-Low-Distortion Op Amps

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to V_{EE}) 12V
Voltage on Any Pin to Ground or Any Other Pin ..... V_{CC} to V_{EE}
Short-Circuit Duration (V_{OUT} to GND) ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
SO (derate 5.88mW/°C above +70°C) 471mW

Operating Temperature Range
MAX4108ESA/MAX4109ESA ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Junction Temperature ..... +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, V_{EE} = -5V, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC SPECIFICATIONS							
Input Offset Voltage	V_{OS}	V_{OUT} = 0V			1	8	mV
Input Offset Voltage Drift	TCV_{OS}	V_{OUT} = 0V			13		µV/°C
Input Bias Current	I_B	V_{OUT} = 0V, V_{IN} = $-V_{OS}$			12	25	µA
Input Offset Current	I_{OS}	V_{OUT} = 0V, V_{IN} = $-V_{OS}$			0.05	1.0	µA
Common-Mode Input Resistance	R_{INCM}	Either input			1.5		MΩ
Common-Mode Input Capacitance	C_{INCM}	Either input			1		pF
Input Voltage Noise	e_n	f_O = 10kHz	MAX4108		8		$nV/\sqrt{Hz}$
			MAX4109		6		
Integrated Voltage Noise	E_{nRMS}	f_B = 1MHz to 100MHz	MAX4108		100		μV_{RMS}
			MAX4109		75		
Input Current Noise	I_n	f_O = 10kHz	MAX4108		2		$pA/\sqrt{Hz}$
			MAX4109		2		
Integrated Current Noise	I_{nRMS}	f_B = 1MHz to 100MHz	MAX4108		25		nA_{RMS}
			MAX4109		25		
Common-Mode Input Voltage	V_{CM}			-2.5		2.5	V
Common-Mode Rejection	CMR	V_{CM} = ±2.5V		70	100		dB
Power-Supply Rejection	PSR	V_S = ±4.5V to ±5.5V		70	90		dB
Open-Loop Voltage Gain	A_{OL}	V_{OUT} = ±2.0V, V_{CM} = 0V, R_L = 100Ω		70	100		dB
Quiescent Supply Current	I_{SY}	V_{IN} = 0V			20	25	mA
Output Voltage Swing	V_{OUT}	R_L = ∞		2.5 to -3.1	2.9 to -3.8		V
		R_L = 100Ω		2.5 to -3.1	2.7 to -3.7		
Output Current Drive	I_{OUT}	R_L = 33Ω, T_A = 0°C to +85°C		65	90		mA
Short-Circuit Output Current	I_{SC}	Short to ground			100		mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5V, V_{EE} = -5V, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C, unless otherwise noted.)

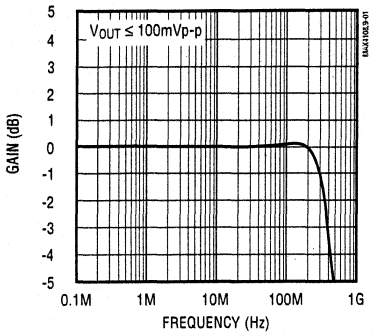
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
AC SPECIFICATIONS							
-3dB Bandwidth	BW_{-3dB}	$V_{OUT} \le 0.1V_{RMS}$	MAX4108		400		MHz
			MAX4109		225		
Full-Power Bandwidth	FPBW	V_{OUT} = 2Vp-p	MAX4108		300		MHz
			MAX4109		200		
0.1dB Bandwidth	$BW_{0.1dB}$	MAX4108, A_{VCL} = +1			100		MHz
		MAX4109, A_{VCL} = +2			25		
Slew Rate	SR	-2V ≤ V_{OUT} ≤ 2V	MAX4108		1200		V/µs
			MAX4109		1200		
Settling Time	t_S	to 0.1%, -1V ≤ V_{OUT} ≤ 1V, R_L = 100Ω	MAX4108		8		ns
			MAX4109		8		
		to 0.01%, -1V ≤ V_{OUT} ≤ 1V, R_L = 100Ω	MAX4108		12		
			MAX4109		12		
Rise/Fall Times	t_R, t_F	-2V ≤ V_{OUT} ≤ 2V, 10% to 90%, R_L = 100Ω	MAX4108		3		ns
			MAX4109		3		
		-50mV ≤ V_{OUT} ≤ 50mV, 10% to 90%, R_L = 100Ω	MAX4108		2		
			MAX4109		2		
Differential Gain	DG	f = 3.58MHz	MAX4108, A_{VCL} = +1		0.002		%
			MAX4109, A_{VCL} = +2		0.008		
Differential Phase	DP	f = 3.58MHz	MAX4108, A_{VCL} = +1		0.002		degrees
			MAX4109, A_{VCL} = +2		0.002		
Input Capacitance	C_{IN}				2		pF
Output Resistance	R_{OUT}	f = 10MHz			1		Ω
Spurious-Free Dynamic Range	SFDR	MAX4108, A_{VCL} = +1, V_{OUT} = 2Vp-p	f_C = 5MHz		-93		dBc
			f_C = 20MHz		-81		
		MAX4109, A_{VCL} = +2, V_{OUT} = 2Vp-p	f_C = 5MHz		-90		
			f_C = 20MHz		-80		
Third-Order Intercept	IP3	f_C = 10MHz	MAX4108, A_{VCL} = +1		39		dBm
			MAX4109, A_{VCL} = +2		36		

400MHz, Ultra-Low-Distortion Op Amps

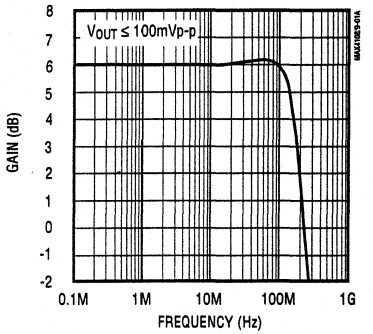
Typical Operating Characteristics

(V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

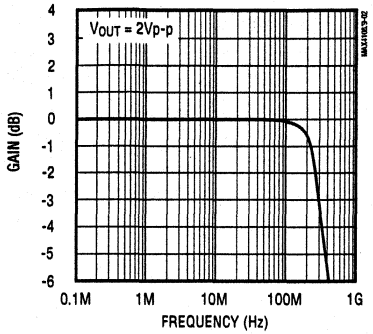
MAX4108
SMALL-SIGNAL GAIN vs. FREQUENCY
(A_{VCL} = +1)



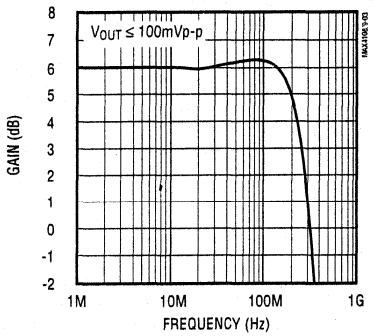
MAX4108
SMALL-SIGNAL GAIN vs. FREQUENCY
(A_{VCL} = +2)



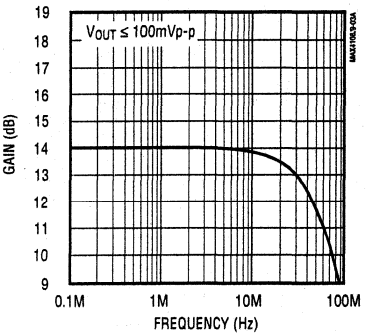
MAX4108
LARGE-SIGNAL GAIN vs. FREQUENCY
(A_{VCL} = +1)



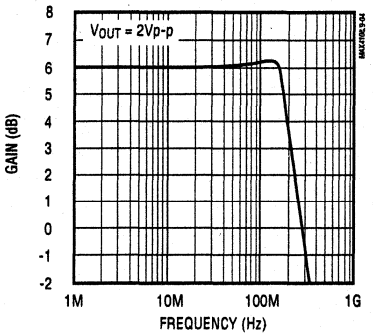
MAX4109
SMALL-SIGNAL GAIN vs. FREQUENCY
(A_{VCL} = +2)



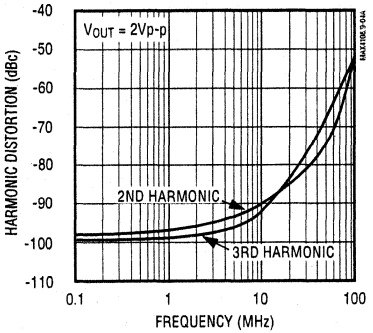
MAX4109
SMALL-SIGNAL GAIN vs. FREQUENCY
(A_{VCL} = +5)



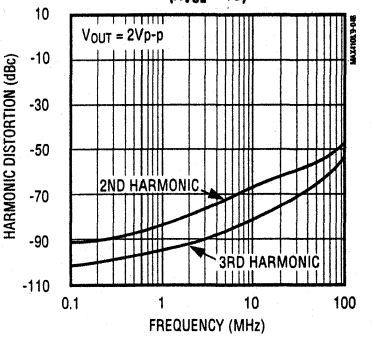
MAX4109
LARGE-SIGNAL GAIN vs. FREQUENCY
(A_{VCL} = +2)



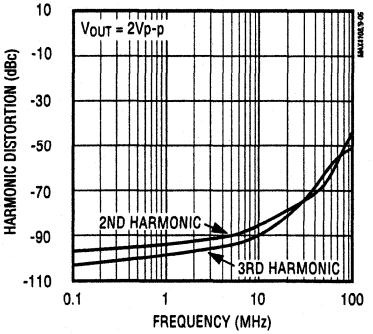
MAX4108
HARMONIC DISTORTION vs. FREQUENCY
(A_{VCL} = +1)



MAX4108
HARMONIC DISTORTION vs. FREQUENCY
(A_{VCL} = +5)



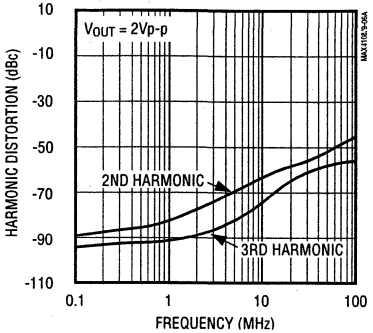
MAX4109
HARMONIC DISTORTION vs. FREQUENCY
(A_{VCL} = +2)



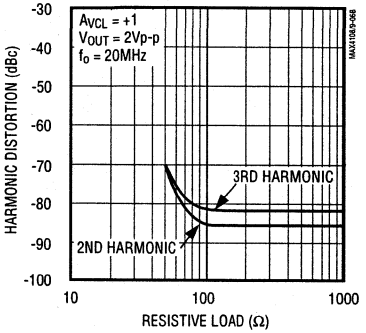
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

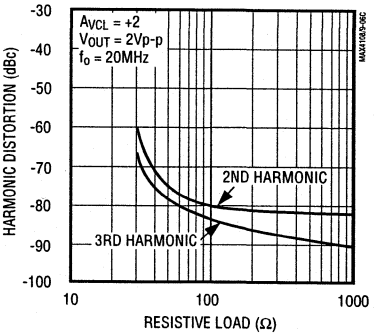
MAX4109
HARMONIC DISTORTION vs. FREQUENCY
(A_{VCL} = +10)



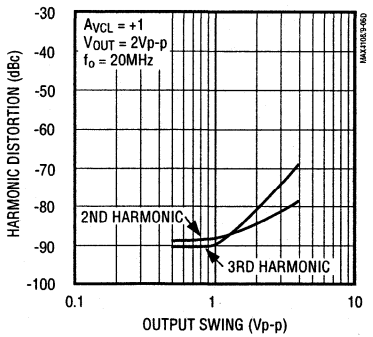
MAX4108
HARMONIC DISTORTION vs. LOAD



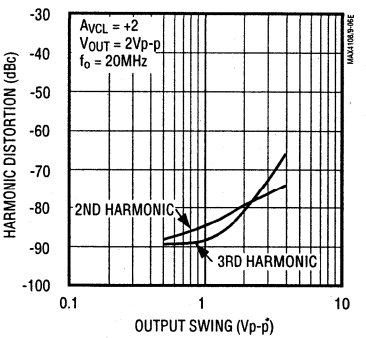
MAX4109
HARMONIC DISTORTION vs. LOAD



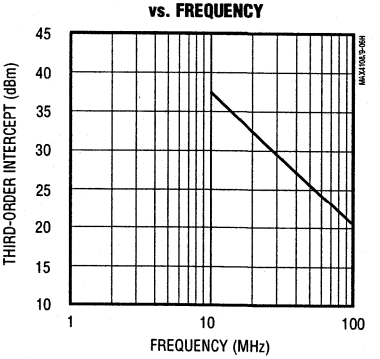
MAX4108
HARMONIC DISTORTION vs. OUTPUT SWING



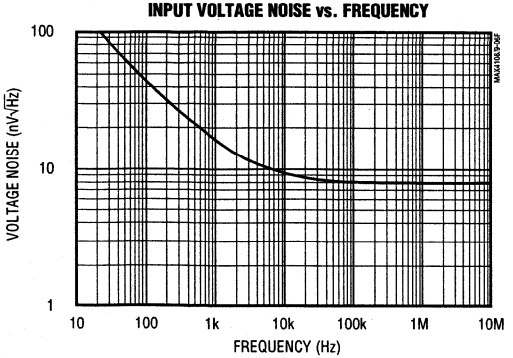
MAX4109
HARMONIC DISTORTION vs. OUTPUT SWING



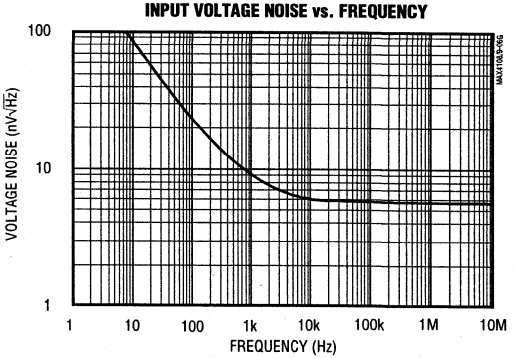
MAX4109
TWO-TONE THIRD-ORDER INTERCEPT
vs. FREQUENCY



MAX4108
INPUT VOLTAGE NOISE vs. FREQUENCY



MAX4109
INPUT VOLTAGE NOISE vs. FREQUENCY

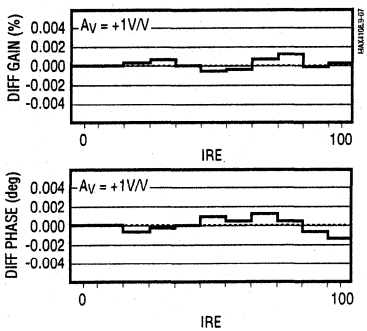


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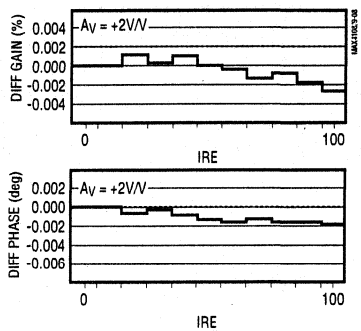
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

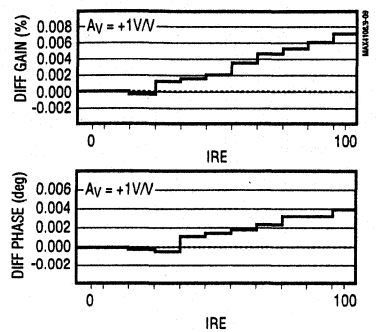
MAX4108
DIFFERENTIAL GAIN AND PHASE
(R_L = 150Ω)



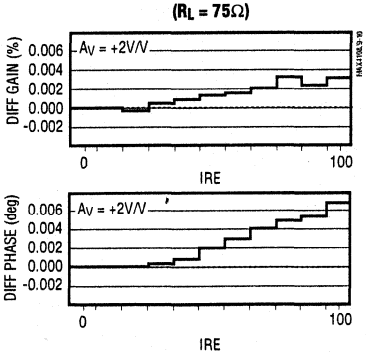
MAX4109
DIFFERENTIAL GAIN AND PHASE
(R_L = 150Ω)



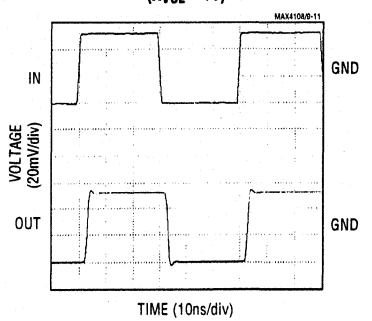
MAX4108
DIFFERENTIAL GAIN AND PHASE
(R_L = 75Ω)



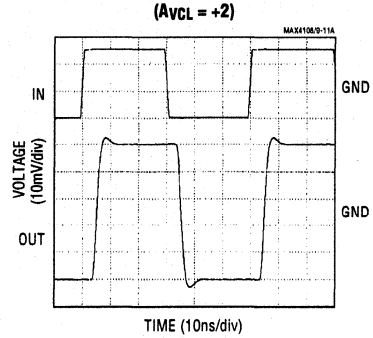
MAX4109
DIFFERENTIAL GAIN AND PHASE
(R_L = 75Ω)



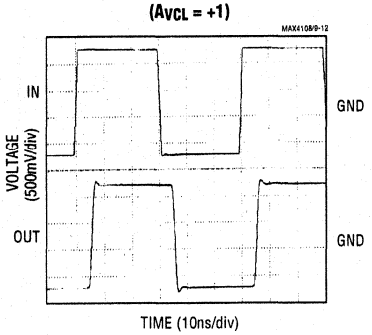
MAX4108
SMALL-SIGNAL PULSE RESPONSE
(A_{VCL} = +1)



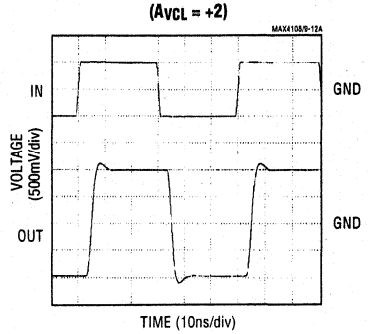
MAX4108
SMALL-SIGNAL PULSE RESPONSE
(A_{VCL} = +2)



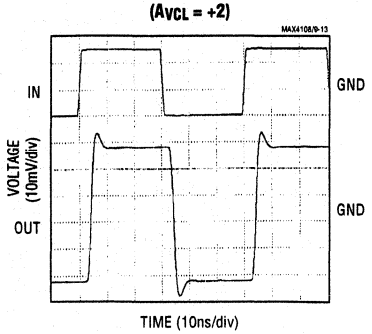
MAX4108
LARGE-SIGNAL PULSE RESPONSE
(A_{VCL} = +1)



MAX4108
LARGE-SIGNAL PULSE RESPONSE
(A_{VCL} = +2)

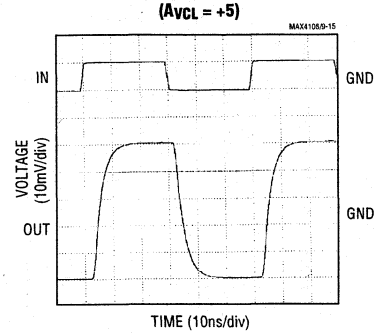


MAX4109
SMALL-SIGNAL PULSE RESPONSE
(A_{VCL} = +2)

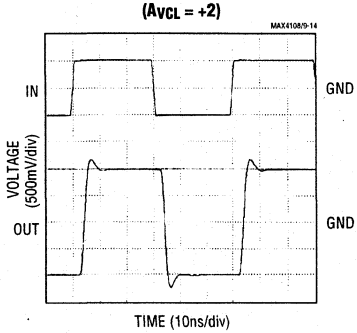


Typical Operating Characteristics (continued)

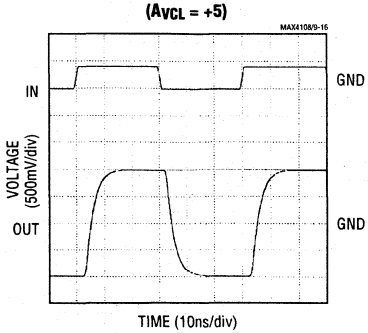
MAX4109
SMALL-SIGNAL PULSE RESPONSE
(A_{VCL} = +5)



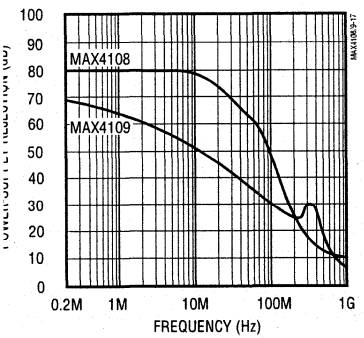
MAX4109
LARGE-SIGNAL PULSE RESPONSE
(A_{VCL} = +2)



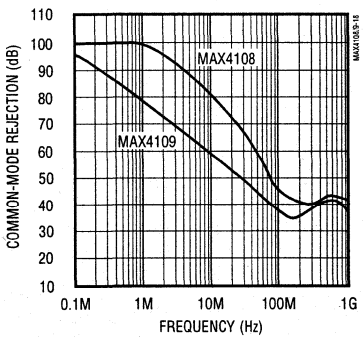
MAX4109
LARGE-SIGNAL PULSE RESPONSE
(A_{VCL} = +5)



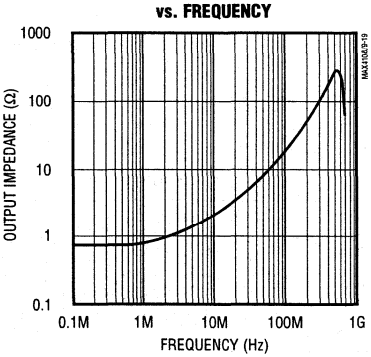
POWER-SUPPLY REJECTION
vs. FREQUENCY



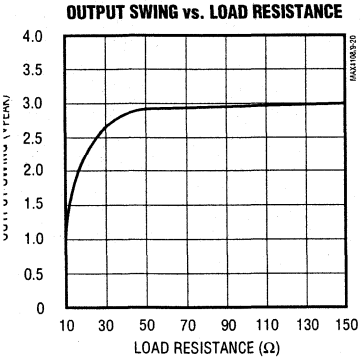
COMMON-MODE REJECTION
vs. FREQUENCY



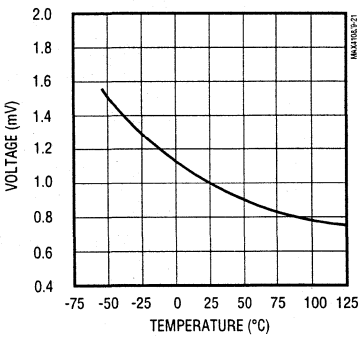
CLOSED-LOOP OUTPUT IMPEDANCE
vs. FREQUENCY



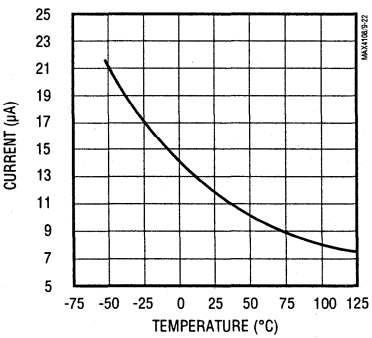
MAX4108
OUTPUT SWING vs. LOAD RESISTANCE



INPUT OFFSET VOLTAGE
vs. TEMPERATURE



INPUT BIAS CURRENT
vs. TEMPERATURE



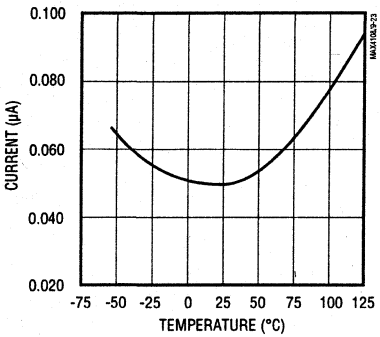
8

400MHz, Ultra-Low-Distortion Op Amps

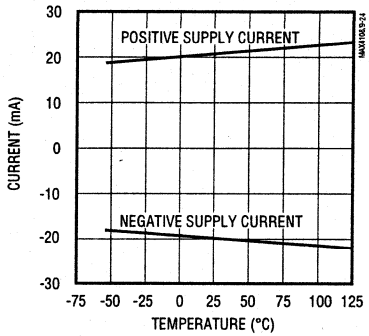
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

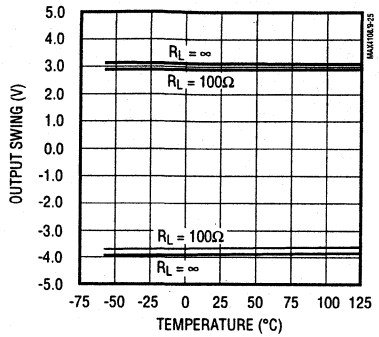
INPUT OFFSET CURRENT vs. TEMPERATURE



POWER SUPPLY CURRENT vs. TEMPERATURE



OUTPUT SWING vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1	N.C.	No Connection. Not internally connected.
2	IN-	Inverting Input
3	IN+	Noninverting Input
4, 5	V_{EE}	Negative Power Supply, connect to -5V
6	OUT	Amplifier Output
7, 8	V_{CC}	Positive Power Supply, connect to +5V

Detailed Description

Choosing Resistor Values

Unity-Gain Configuration

The MAX4108 is internally compensated for unity gain. When configured for unity gain, the device requires a small resistor (typically 24Ω) in series with the feedback path. This resistor provides better AC response by reducing the Q of the tank circuit formed by parasitic feedback inductance and capacitance.

Inverting and Noninverting Configurations

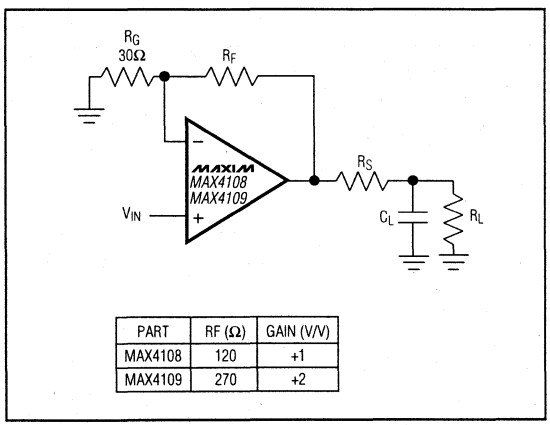
The values of the gain-setting feedback and input resistors are important design considerations. Large resistor values will increase voltage noise, and will interact with the amplifier's input and PC board capacitance to generate undesirable poles and zeros, which can decrease bandwidth or cause oscillations. For example, a noninverting gain of +2, using 1kΩ resistors combined with 2pF of input capacitance and 0.5pF of board capacitance, will cause a feedback pole at 128MHz. If this pole is within the anticipated amplifier bandwidth, it will jeopardize stability. Reducing these 1kΩ resistors to 100Ω will extend the pole frequency to 1.28GHz, but could limit output swing by adding 200Ω in parallel with the amplifier's load. Clearly, the selection of resistor values must be tailored to the specific application.

The MAX4108/MAX4109 are ultra-low-distortion, high-bandwidth op amps. The output distortion will be degraded as the total load resistance seen by the amplifier decreases. To minimize distortion products, keep the input and gain-setting resistors relatively large. A 500Ω feedback resistor combined with an appropriate input resistor to set the gain will provide excellent AC performance without significantly increasing distortion.

Driving Capacitive Loads

The MAX4108/MAX4109 are optimized for AC performance. They are not designed to drive highly reactive loads. Reactive loads will decrease phase margin and may produce excessive ringing and oscillation. Figure 1a shows a circuit that eliminates this problem, and Figure 1b is a graph of the optimal isolation resistor (R_S) vs. capacitive load. Figures 2a and 2b show how a capacitive load causes excessive peaking of the amplifier's bandwidth if the capacitive load is not isolated (R_S) from the amplifier. A small isolation resistor (usually 10Ω to 20Ω) placed before the reactive load prevents ringing and oscillation. At higher capacitive loads, AC performance will be controlled by the interaction of the load capacitance and isolation resistor. Figures 3a and 3b show the effect of an isolation resistor on the MAX4108/MAX4109 closed-loop response.

Coaxial cable and other transmission lines are easily driven when terminated at both ends with their characteristic impedance. When driving back-terminated transmission lines, the capacitance of the transmission line is essentially eliminated.



PART	RF (Ω)	GAIN (V/V)
MAX4108	120	+1
MAX4109	270	+2

Figure 1a. Using an Isolation Resistor for High Capacitive Loads

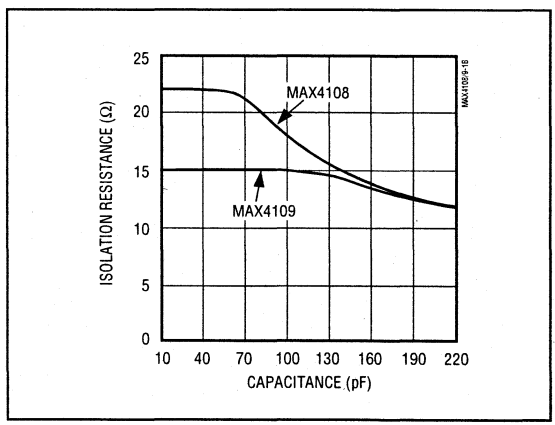


Figure 1b. Optimal Isolation Resistor (RS) vs. Capacitive Load

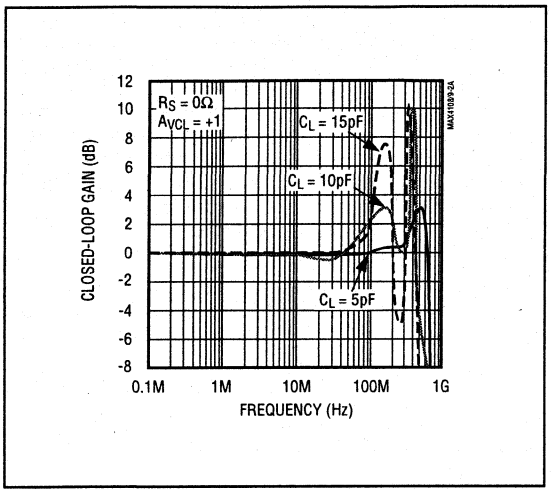


Figure 2a. MAX4108 Response vs. Capacitive Load—No Resistive (R_S) Isolation (circuit shown in Figure 1)

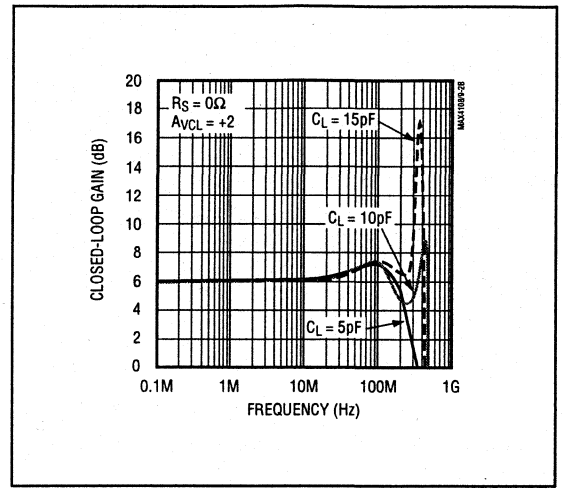


Figure 2b. MAX4109 Response vs. Capacitive Load—No Isolation (R_S) Resistor (circuit shown in Figure 1)

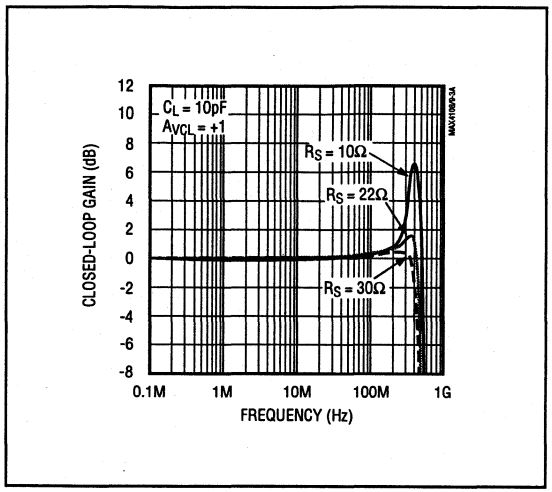


Figure 3a. MAX4108 Response vs. Capacitive Load with Resistive (R_S) Isolation (circuit shown in Figure 1)

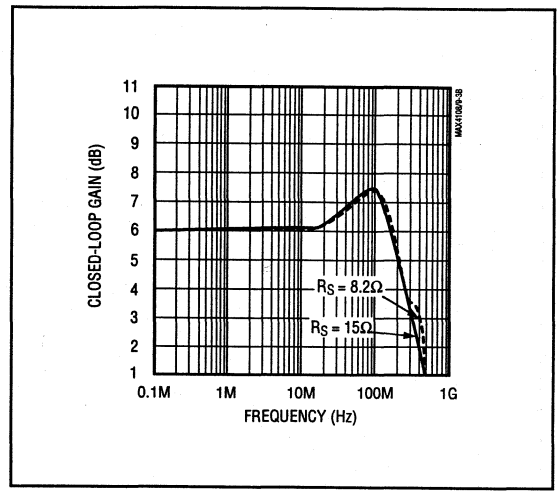


Figure 3b. MAX4109 Response vs. Capacitive Load with Resistive (R_S) Isolation (circuit shown in Figure 1)

Chip Information

TRANSISTOR COUNT: 57

SUBSTRATE CONNECTED TO V_{EE}

19-0440; Rev 1; 8/96

EVALUATION KIT AVAILABLE

MAXIM

Single/Dual, 500MHz, Low-Power, Current-Mode Feedback Amplifiers

General Description

The single MAX4112/MAX4113 and the dual MAX4117/MAX4118 current-mode feedback amplifiers combine high-speed performance with low-power operation. The MAX4112/MAX4117 are optimized for closed-loop gains of 2V/V or greater, while the MAX4113/MAX4118 are optimized for gains of 8V/V or greater.

The MAX4112/MAX4117 and MAX4113/MAX4118 require only 5mA of supply current per channel, and deliver bandwidths of 500MHz ($A_V \geq 2V/V$) and 275MHz ($A_V \geq 8V/V$), respectively. Their high slew rates (1200V/µs and 1800V/µs) provide exceptional full-power bandwidths (300MHz and 250MHz), making these amplifiers ideal for high-performance pulse and RGB video applications.

These high-speed op amps have a wide output voltage swing of ±3.5V into 100Ω and high current-drive capability of 80mA.

Applications

Broadcast and High-Definition TV Systems

RGB Video

Pulse/RF Amplifier

Ultrasound

Active Filters

ADC Buffers

Features

- **500MHz -3dB Bandwidth (MAX4112/MAX4117)**
  275MHz -3dB Bandwidth (MAX4113/MAX4118)
- **0.1dB Gain Flatness to 30MHz (MAX4112/MAX4117)**
- **1200V/µs Slew Rate (MAX4112/MAX4117)**
  1800V/µs Slew Rate (MAX4113/MAX4118)
- **300MHz Full-Power Bandwidth**
  (V_O = 2Vp-p, MAX4112/MAX4117)
  250MHz Full-Power Bandwidth
  (V_O = 2Vp-p, MAX4113/MAX4118)
- **High Output Drive: 80mA**
- **Low Power: 5mA Supply Current per Channel**

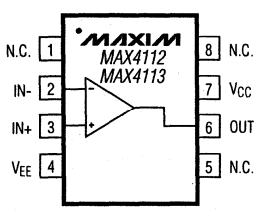
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4112ESA	-40°C to +85°C	8 SO
MAX4112EUA	-40°C to +85°C	8 µMAX*
MAX4113ESA	-40°C to +85°C	8 SO
MAX4117ESA	-40°C to +85°C	8 SO
MAX4118ESA	-40°C to +85°C	8 SO

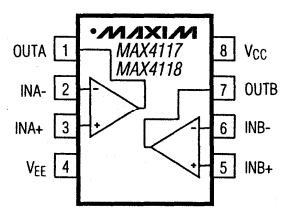
** Contact factory for µMAX package availability.*

Pin Configurations

TOP VIEW



SO/µMAX*



SO

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Single/Dual, 500MHz, Low-Power, Current-Mode Feedback Amplifiers

ABSOLUTE MAXIMUM RATINGS

Power-Supply Voltage (V_{CC} to V_{EE}) 12V
Input Voltage (IN+, IN-, IN_+, IN_-) ..... (V_{CC} + 0.3V) to (V_{EE} - 0.3V)
IN- Current (Note 1) ..... ±10mA
Short-Circuit Duration (V_{OUT} to GND)
V_{IN} < 1.5V ..... Continuous
V_{IN} > 1.5V 0sec

Continuous Power Dissipation (T_A = +70°C)
SO (derate 5.88mW/°C above +70°C) 471mW
µMAX (derate 4.10mW/°C above +70°C) 330mW
Operating Temperature Range
MAX411_E_A ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Specifications apply to MAX411_ESA. V_{CC} = +5V, V_{EE} = -5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A =

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC SPECIFICATIONS							
Input Offset Voltage	V_{OS}	V_{OUT} = 0V			1	8	mV
Input Offset Voltage Drift	TCV_{OS}	V_{OUT} = 0V			10		µV/°C
Positive Input Bias Current	I_{B+}	V_{OUT} = 0V, V_{IN} = -V_{OS}			3.5	20	µA
Negative Input Bias Current	I_{B-}	V_{OUT} = 0V, V_{IN} = -V_{OS}			3.5	20	µA
Input Resistance		IN+			500		kΩ
		IN-			30		Ω
Input Voltage Noise	e_n	f = 10kHz			2.2		nV/√Hz
Integrated Voltage Noise	E_{nRMS}	f = 1MHz to 100MHz			27		µVRMS
Positive Input Current Noise	i_{n+}	f = 10kHz	MAX4112/MAX4117		13		pA/√Hz
			MAX4113/MAX4118		9		
Negative Input Current Noise	i_{n-}	f = 10kHz			14		pA/√Hz
Common-Mode Input Voltage	V_{CM}			-2.5		2.5	V
Common-Mode Rejection	CMR	V_{CM} = ±2.5V		45	50		dB
Power-Supply Rejection	PSR	V_S = ±4.5V to ±5.5V		60	80		dB
Open-Loop Transimpedance	Z_{OL}	V_{OUT} = ±2.0V, V_{CM} = 0V, R_L = 100Ω		250	500		kΩ
Quiescent Supply Current per Amplifier	I_{SY}	MAX4112/MAX4113, V_{IN} = 0V			5	6	mA
Output Voltage Swing	V_{OUT}	R_L = ∞		±3.5	±3.8		V
		R_L = 100Ω		±3.1	±3.5		
Output Current Drive	I_{OUT}	R_L = 30Ω, T_A = 0°C to +85°C		65	80		mA

Note 1: The MAX4112/MAX4113/MAX4117/MAX4118 are designed to operate in a closed-loop configuration in which the IN- pin is driven by the OUT pin through an external feedback network. If an external voltage source is connected to IN-, current into or out of IN- must be limited to ±10mA; otherwise, irreversible damage to the part will occur.

ELECTRICAL CHARACTERISTICS (continued)

(Specifications apply to MAX411_ESA. V_{CC} = +5V, V_{EE} = -5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A =

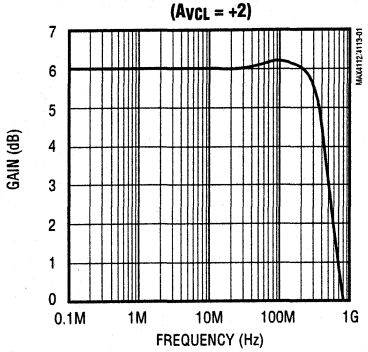
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
AC SPECIFICATIONS							
-3dB Bandwidth	BW_{-3dB}	$V_{OUT} \le 0.1V_{RMS}$	MAX4112/MAX4117		500		MHz
			MAX4113/MAX4118		275		
0.1dB Bandwidth	$BW_{0.1dB}$	MAX4112/MAX4117, A_{VCL} = +2			30		MHz
		MAX4113/MAX4118, A_{VCL} = +8			90		
Full-Power Bandwidth	FPBW	V_O = 2Vp-p	MAX4112/MAX4117		300		MHz
			MAX4113/MAX4118		250		
Slew Rate	SR	-2V ≤ V_{OUT} ≤ 2V	MAX4112/MAX4117		1200		V/µs
			MAX4113/MAX4118		1800		
Settling Time	t_S	to 0.1%, -1V ≤ V_{OUT} ≤ 1V, R_L = 100Ω	MAX4112/MAX4117		15		ns
			MAX4113/MAX4118		10		
		to 0.01%, -1V ≤ V_{OUT} ≤ 1V, R_L = 100Ω	MAX4112/MAX4117		35		
			MAX4113/MAX4118		25		
Rise/Fall Times	t_R, t_F	10% to 90%, -2V ≤ V_{OUT} ≤ 2V, R_L = 100Ω			3		ns
		10% to 90%, -50mV ≤ V_{OUT} ≤ 50mV, R_L = 100Ω			0.8		
Differential Gain	DG	f = 3.58MHz	MAX4112/MAX4117, A_{VCL} = +2		0.02		%
			MAX4113/MAX4118, A_{VCL} = +8		0.02		
Differential Phase	DP	f = 3.58MHz	MAX4112/MAX4117, A_{VCL} = +2		0.03		degrees
			MAX4113/MAX4118, A_{VCL} = +8		0.04		
Input Capacitance	C_{IN}				2		pF
Output Impedance	Z_{OUT}	f = 10MHz, A_{VCL} = +2			0.9		Ω
Spurious-Free Dynamic Range	SFDR	f_C = 5MHz, V_{OUT} = 2Vp-p	MAX4112/MAX4117, A_{VCL} = +2		-68		dBc
			MAX4113/MAX4118, A_{VCL} = +8		-62		
Two-Tone Third-Order Intercept	IP3	MAX4112/MAX4117, f_C = 10MHz, A_{VCL} = +2			36		dB
Crosstalk		V_{IN} = $1V_{p-p}$, f = 10MHz			-75		dB

Single/Dual, 500MHz, Low-Power, Current-Mode Feedback Amplifiers

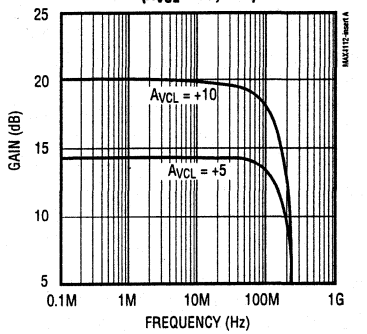
Typical Operating Characteristics

(V_{CC} = +5V, V_{EE} = -5V, R_F = 499Ω, R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

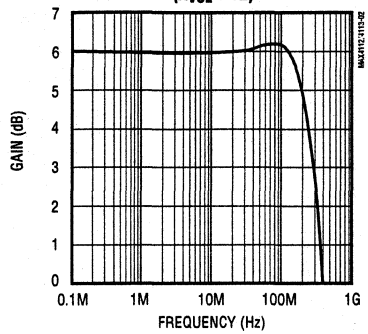
MAX4112/MAX4117
SMALL-SIGNAL GAIN vs. FREQUENCY
(A_{VCL} = +2)



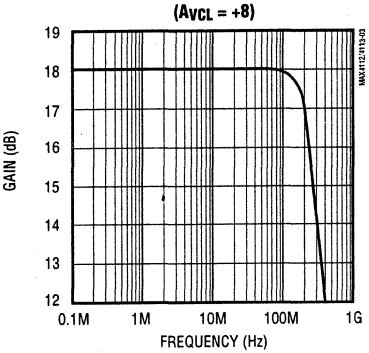
MAX4112/MAX4117
SMALL-SIGNAL GAIN vs. FREQUENCY
(A_{VCL} = +5, +10)



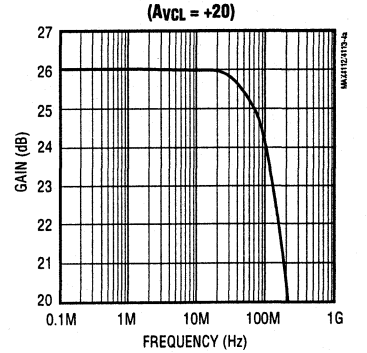
MAX4112/MAX4117
LARGE-SIGNAL GAIN vs. FREQUENCY
(A_{VCL} = +2)



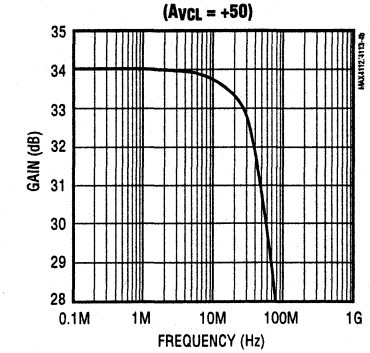
MAX4113/MAX4118
SMALL-SIGNAL GAIN vs. FREQUENCY
(A_{VCL} = +8)



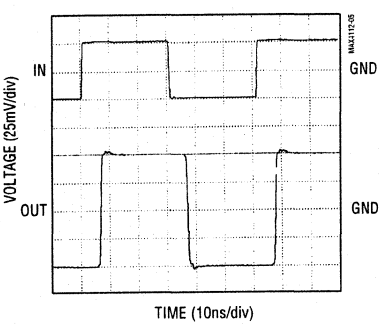
MAX4113/MAX4118
SMALL-SIGNAL GAIN vs. FREQUENCY
(A_{VCL} = +20)



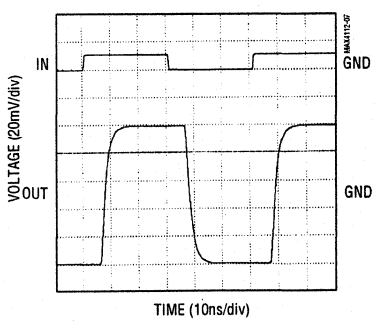
MAX4113/MAX4118
SMALL-SIGNAL GAIN vs. FREQUENCY
(A_{VCL} = +50)



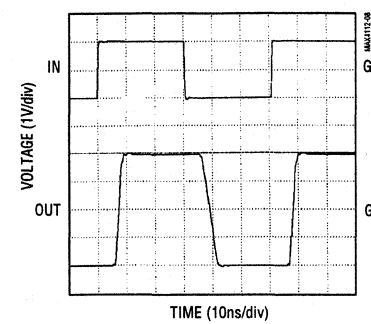
MAX4112/MAX4117
SMALL-SIGNAL PULSE RESPONSE
(A_{VCL} = +2)



MAX4112/MAX4117
SMALL-SIGNAL PULSE RESPONSE
(A_{VCL} = +10)



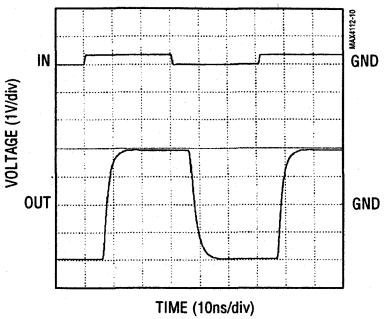
MAX4112/MAX4117
LARGE-SIGNAL PULSE RESPONSE
(A_{VCL} = +2)



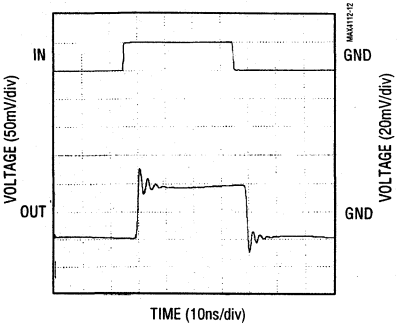
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, R_F = 499Ω, R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

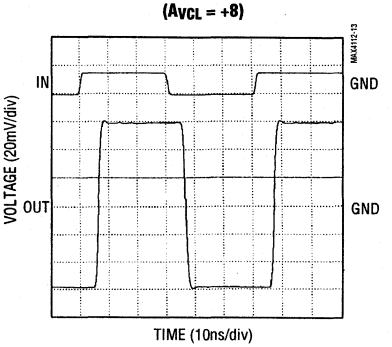
MAX4112/MAX4117
LARGE-SIGNAL PULSE RESPONSE
(A_{VCL} = +10)



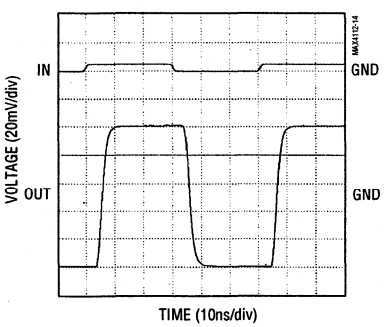
MAX4112/MAX4117
SMALL-SIGNAL PULSE RESPONSE
(A_{VCL} = +2, C_L = 10pF)



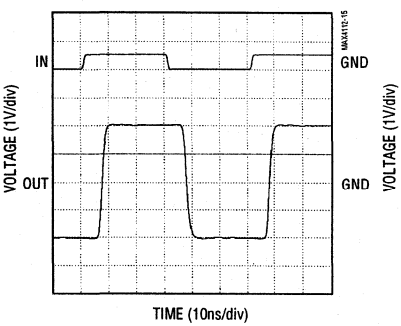
MAX4113/MAX4118
SMALL-SIGNAL PULSE RESPONSE
(A_{VCL} = +8)



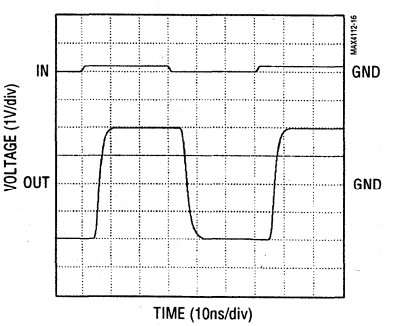
MAX4113/MAX4118
SMALL-SIGNAL PULSE RESPONSE
(A_{VCL} = +20)



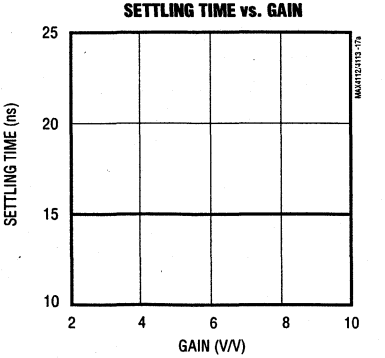
MAX4113/MAX4118
LARGE-SIGNAL PULSE RESPONSE
(A_{VCL} = +8)



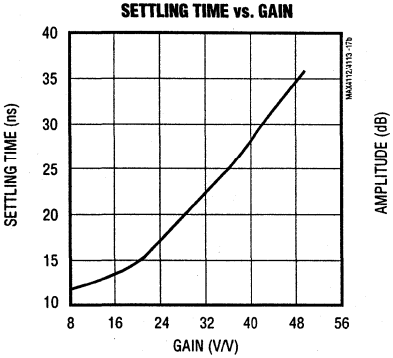
MAX4113/MAX4118
LARGE-SIGNAL PULSE RESPONSE
(A_{VCL} = +20)



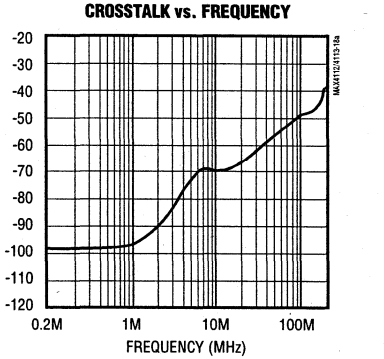
MAX4112/MAX4117
SETTLING TIME vs. GAIN



MAX4113/MAX4118
SETTLING TIME vs. GAIN



MAX4117/MAX4118
CROSSTALK vs. FREQUENCY

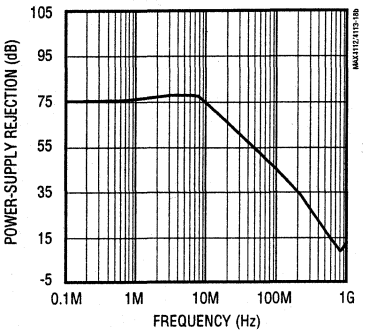


Single/Dual, 500MHz, Low-Power, Current-Mode Feedback Amplifiers

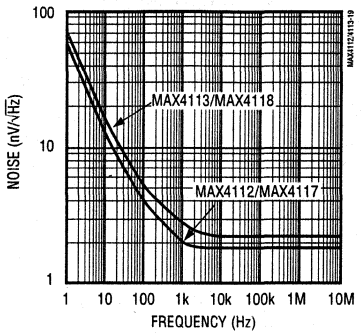
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, R_F = 499Ω, R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

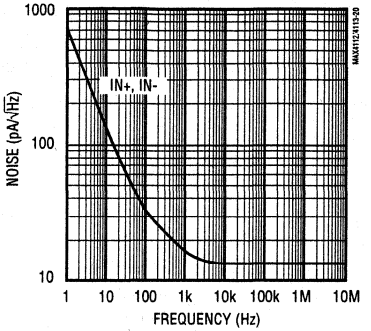
POWER-SUPPLY REJECTION



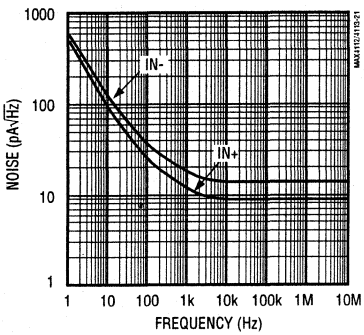
INPUT VOLTAGE NOISE vs. FREQUENCY



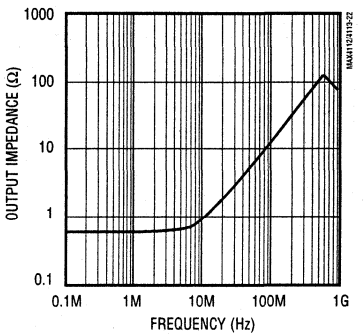
MAX4112/MAX4117 INPUT CURRENT NOISE vs. FREQUENCY



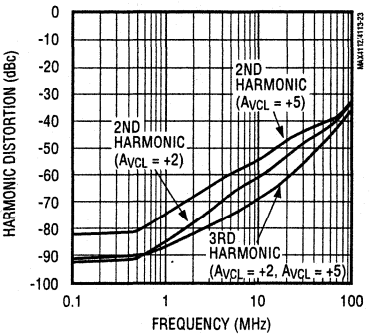
MAX4113/MAX4118 INPUT CURRENT NOISE vs. FREQUENCY



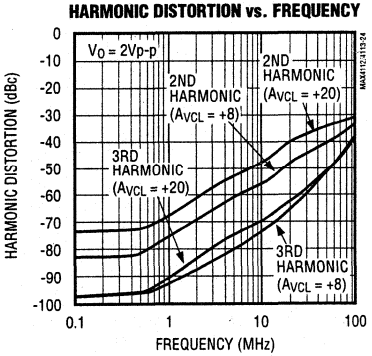
CLOSED-LOOP OUTPUT IMPEDANCE



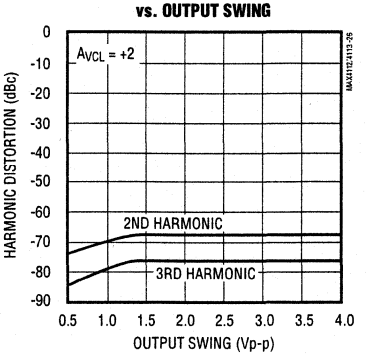
MAX4112/MAX4117 HARMONIC DISTORTION vs. FREQUENCY



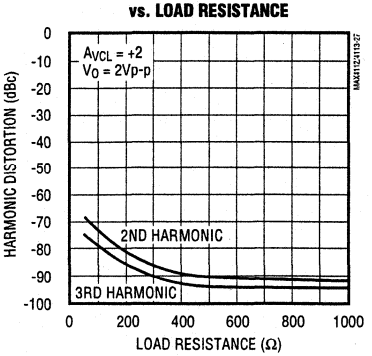
MAX4113/MAX4118 HARMONIC DISTORTION vs. FREQUENCY



MAX4112/MAX4117 5MHz HARMONIC DISTORTION vs. OUTPUT SWING



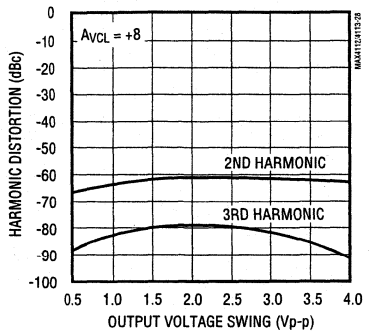
MAX4112/MAX4117 5MHz HARMONIC DISTORTION vs. LOAD RESISTANCE



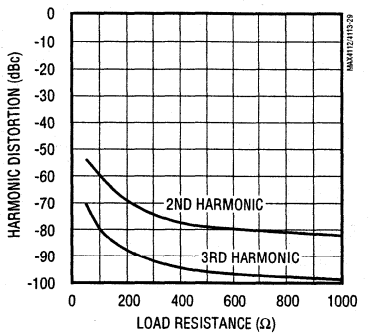
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, R_F = 499Ω, R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

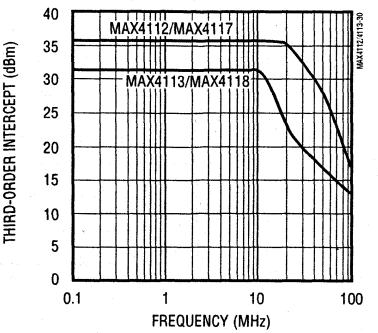
MAX4113/MAX4118 5MHz HARMONIC DISTORTION vs. OUTPUT SWING



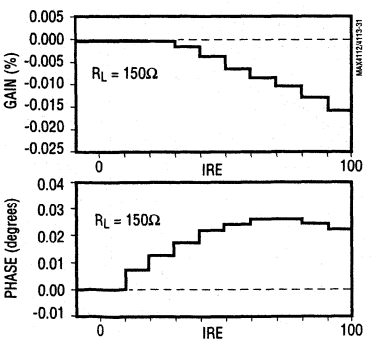
MAX4113/MAX4118 5MHz HARMONIC DISTORTION vs. LOAD RESISTANCE



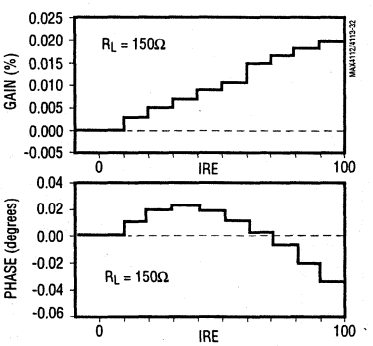
TWO-TONE THIRD-ORDER INTERCEPT vs. FREQUENCY



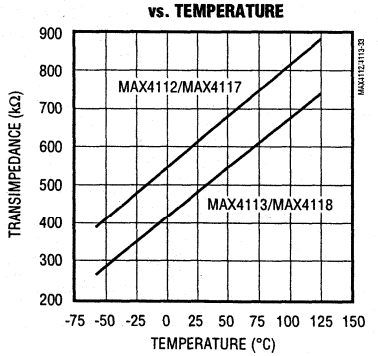
MAX4112/MAX4117 DIFFERENTIAL GAIN and PHASE



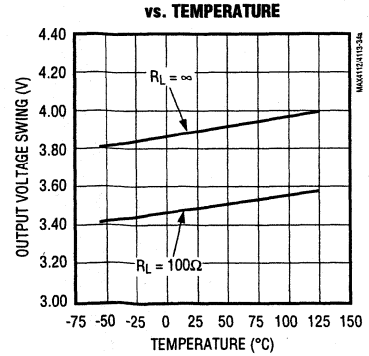
MAX4113/MAX4118 DIFFERENTIAL GAIN and PHASE



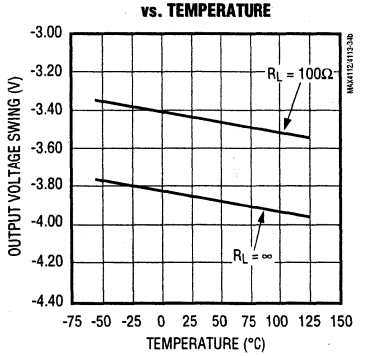
OPEN-LOOP TRANSIMPEDANCE vs. TEMPERATURE



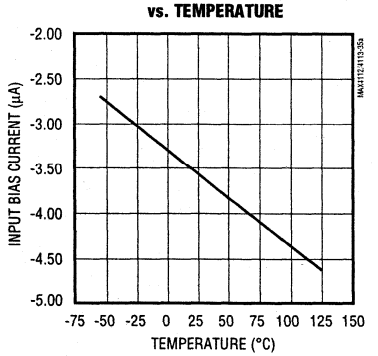
POSITIVE OUTPUT VOLTAGE SWING vs. TEMPERATURE



NEGATIVE OUTPUT VOLTAGE SWING vs. TEMPERATURE



POSITIVE INPUT BIAS CURRENT vs. TEMPERATURE

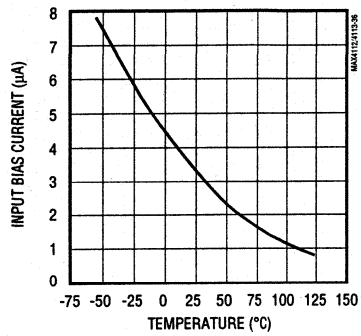


Single/Dual, 500MHz, Low-Power, Current-Mode Feedback Amplifiers

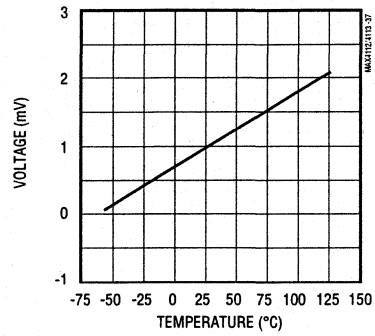
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, R_F = 499Ω, R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

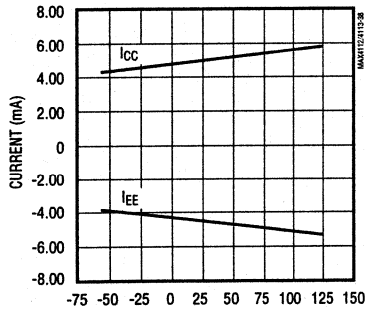
NEGATIVE INPUT BIAS (I_{B-}) CURRENT vs. TEMPERATURE



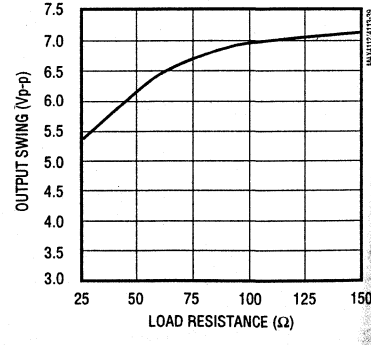
INPUT OFFSET VOLTAGE vs. TEMPERATURE



POWER-SUPPLY CURRENT vs. TEMPERATURE (PER AMPLIFIER)



OUTPUT SWING vs. LOAD RESISTANCE



Single/Dual, 500MHz, Low-Power, Current-Mode Feedback Amplifiers

Pin Description

PIN		NAME	FUNCTION
MAX4112/MAX4113	MAX4117/MAX4118		
1, 5, 8	—	N.C.	No Connection. Not internally connected.
—	1	OUTA	Amplifier A Output
2	—	IN-	Inverting Input
—	2	INA-	Amplifier A Inverting Input
3	—	IN+	Noninverting Input
—	3	INA+	Amplifier A Noninverting Input
4	4	V_{EE}	Negative Power Supply. Connect to -5V.
—	5	INB+	Amplifier B Noninverting Input
6	—	OUT	Amplifier Output
—	6	INB-	Amplifier B Inverting Input
—	7	OUTB	Amplifier B Output
7	8	V_{CC}	Positive Power Supply. Connect to +5V.

Detailed Description

The MAX4112/MAX4117 are optimized for closed-loop gains (A_{VCL}) of 2V/V or greater, while the MAX4113/MAX4118 are optimized for closed-loop gains of 8V/V or greater. These low-power, high-speed, current-mode feedback amplifiers operate from ±5V supplies. They are designed to drive video loads with excellent distortion characteristics. The MAX4112/MAX4117's differential gain and phase are 0.02% and 0.03°, respectively; the MAX4113/MAX4118 exhibit gain/phase error specifications of 0.02% and 0.04°, respectively. These characteristics, plus a wide 0.1dB bandwidth, make the MAX4112/MAX4113/MAX4117/MAX4118 ideal for use in broadcast and graphics video systems. The combination of ultra-high speed and low power makes these parts ideal for use in general-purpose, high-speed applications, such as medical imaging, industrial instrumentation, and communications systems.

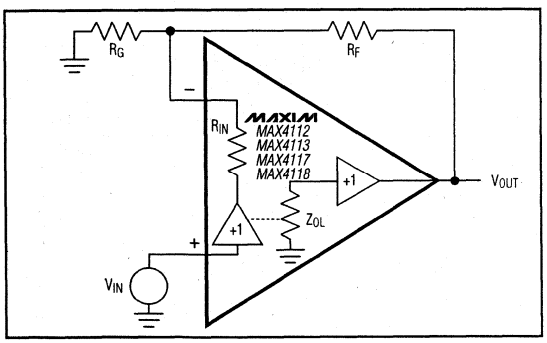


Figure 1. Current Feedback Amplifier

Applications Information

Theory of Operation

Since these devices are current-feedback amplifiers, their open-loop transfer function is expressed as a transimpedance, $\Delta V_{OUT}/\Delta I_{IN}$, or Z_{OL}. The frequency behavior of the open-loop transimpedance is similar to the open-loop gain of a voltage-mode feedback amplifier. That is, it has a large DC value and decreases at approximately 6dB/octave.

Analyzing the follower with gain, as shown in Figure 1, yields the following transfer function:

$$\frac{V_{OUT}}{V_{IN}} = G \times \frac{Z_{OL(S)}}{Z_{OL(S)} + G \times R_{IN} + R_F}$$

where $G = A_{VCL} = 1 + R_F / R_G$, and $R_{IN} = 1 / g_M \cong 30\Omega$.

At low gains, $G \times R_{IN} << R_F$. Therefore, the closed-loop bandwidth is essentially independent of closed-loop gain. Similarly $Z_{OL} >> R_F$ at low frequencies, so that:

$$\frac{V_{OUT}}{V_{IN}} = G = 1 + R_F / R_G$$

Layout and Power-Supply Bypassing

MAX4112/MAX4113/MAX4117/MAX4118 have an RF bandwidth and consequently require careful board layout, including the possible use of constant-impedance Microstrip or Stripline techniques.

To realize the full AC performance of these high-speed amplifiers, pay careful attention to power-supply

Single/Dual, 500MHz, Low-Power, Current-Mode Feedback Amplifiers

bypassing and board layout. The PC board should have at least two layers: a signal and power layer on one side, and a large, low-impedance ground plane on the other side. The ground plane should be as free of voids as possible. With multilayer boards, locate the ground plane on a layer that incorporates no signal or power traces.

Regardless of whether a constant-impedance board is used, observe the following guidelines when designing the board. Wire-wrap boards are much too inductive, and breadboards are much too capacitive; neither should be used. IC sockets increase parasitic capacitance and inductance, and should not be used. In general, surface-mount components give better high-frequency performance than through-hole components. They have shorter leads and lower parasitic reactances. Keep lines as short and as straight as possible. Do not make 90° turns; round all corners.

Observe high-frequency bypassing techniques to maintain the amplifier's accuracy. The bypass capacitors should include a 1000pF ceramic capacitor between each supply pin and the ground plane, located as close to the package as possible. Next, place a 0.01µF to 0.1µF ceramic capacitor in parallel with each 1000pF capacitor, and as close to them as possible. Then place a 10µF to 15µF low-ESR tantalum at the point of entry (to the PC board) of the power-supply pins. The power-supply trace should lead directly from the tantalum capacitor to the V_{CC} and V_{EE} pins. To minimize parasitic inductance, keep PC traces short and use surface-mount components.

Choosing Feedback and Gain Resistors

The MAX4112/MAX4113/MAX4117/MAX4118 are current-mode feedback amplifiers optimized for a 499Ω feedback resistor. Although a standard 5% value is sufficient, a 1% value is preferred to maintain consistency

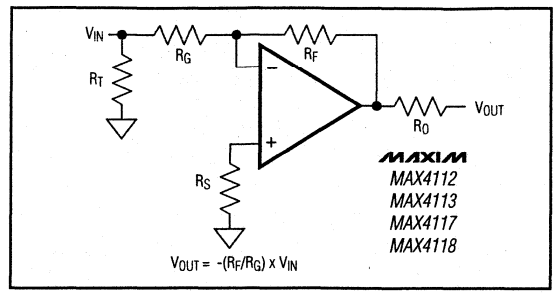


Figure 2a. Inverting Gain Configuration

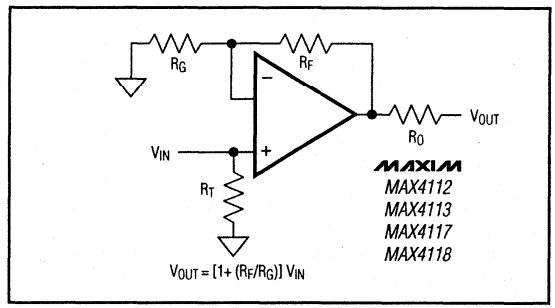


Figure 2b. Noninverting Gain Configuration

over a wide range of production lots. Changing feedback resistor value will reduce the bandwidth or cause excessive peaking. Use the input resistor (R_F) to change the magnitude of the gain. Figure 2 shows the standard inverting and noninverting configurations. Notice that the gain of the noninverting circuit (Figure 2b) is 1 plus the magnitude of the inverting closed-loop gain. Otherwise the two circuits are identical and equivalent (see Table 1).

Table 1. Recommended Component Values

COMPONENT	MAX4112/MAX4117 GAIN (V/V)				MAX4113/MAX4118 GAIN (V/V)				
	-2	+2	+10	+25	-8	+8	+10	+50	+100
R_F (Ω)	499	499	499	499	499	499	499	499	499
R_G (Ω)	247	499	56	20	62.5	69	56	10	5
R_O (Ω)	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9
R_S (Ω)	0	—	—	—	—	0	—	—	—
R_T (Ω)	62.5	49.9	49.9	49.9	250	49.9	49.9	49.9	49.9
Small-Signal Bandwidth (MHz)	180	500	100	50	325	275	235	50	23
0.1dB Flatness (MHz)	40	30	15	8	90	90	79	8	4

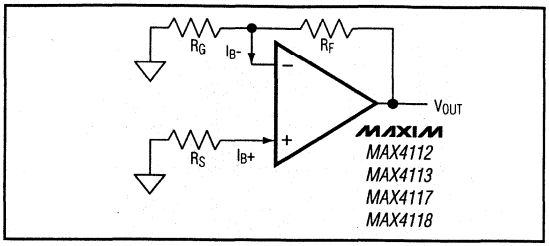


Figure 3. Output Offset Voltage

DC and Noise Errors

There are several major error sources to consider in any operational amplifier. These apply equally to the MAX4112/MAX4113/MAX4117/MAX4118. Offset-error terms are given by the equation below. Voltage and current noise errors are root-square summed and therefore computed separately. In Figure 3, the total output offset voltage is determined by:

a) The input offset voltage (V_{OS}) times the closed-loop gain ($1 + R_F / R_G$).

b) The positive input bias current (I_{B+}) times the source resistor (R_S) (usually 50Ω or 75Ω), plus the negative input bias current (I_{B-}), times the parallel combination of R_G and R_F. In current-mode feedback amplifiers, the input bias currents may flow into or out of the device. For this reason, there is no benefit to matching the resistance at both inputs.

The equation for total DC error is:

$$V_{OUT} = \left[(I_{B+})R_S + (I_{B-})(R_F \,||\, R_G) + V_{OS}\right]\left(1\frac{R_F}{R_G}\right)$$

c) The total output-referred noise voltage is:

$$e_{n(OUT)} = \left(1+\frac{R_F}{R_G}\right)\sqrt{\left[(i_{n+})R_S\right]^2 + \left[(i_{n-})R_F \,||\, R_G\right]^2 + (e_n)^2}$$

The MAX4112/MAX4117 have a very low, 2nV/√Hz noise voltage. The current noise at the positive input (i_{n+}) is 13pA/√Hz, and the current noise at the inverting input is 14pA/√Hz.

An example of the DC error calculations, using the MAX4112 typical data and the typical operating circuit where $R_F = R_G = 500\Omega$ ($R_F \,||\, R_G = 250\Omega$) and $R_S = 50\Omega$, gives the following:

$V_{OUT} = (3.5 \times 10^{-6} \times 50 + 3.5 \times 10^{-6} \times 250 + 10^{-3})(1 + 1)$

$V_{OUT} = 4.1mV$

Calculating total output noise in a similar manner yields:

$$e_{n(OUT)} = (1+1)\sqrt{\left(13x10^{-12}x50\right)^2 + \left(14x10^{-12}x250\right)^2 + \left(2x10^{-9}\right)^2}$$

$$e_{n(OUT)} = 4nV/\sqrt{Hz}$$

With a 200MHz system bandwidth, this calculates to 56.6μVRMS (approximately 340μVp-p, choosing the six-sigma value).

Resistor Types

Surface-mount resistors are the best choice for high-frequency circuits. They are of similar material to metal-film resistors, but are deposited using a thick-film process in a flat, linear manner that minimizes inductance. Their small size and lack of leads also minimizes parasitic inductance and capacitance, yielding more predictable performance.

Metal-film resistors with leads are manufactured using a thin-film process where resistive material is deposited in a spiral layer around a ceramic rod. Although the materials used are noninductive, the spiral winding presents a small inductance (about 5nH) that may have an adverse effect on high-frequency circuits.

Carbon composition resistors with leads are manufactured by pouring the resistor material into a mold. This process yields relatively low-inductance resistors that are very useful in high-frequency applications, although they tend to cost more and have more thermal noise than other types. The ability of carbon composition resistors to self-heal after a large current overload makes them useful in high-power RF applications.

For general-purpose use, surface-mount metal-film resistors seem to have the best overall performance for low cost, low inductance, and low noise.

Video Line Driver

The MAX4112/MAX4113/MAX4117/MAX4118 are optimized (gain flatness) to drive coaxial transmission lines when the cable is terminated at both ends, as shown in Figure 4. Cable frequency response can cause variations in the flatness of the signal.

Driving Capacitive Loads

The MAX4112/MAX4113/MAX4117/MAX4118 are optimized for AC performance. They are not designed to drive highly capacitive loads. Reactive loads decrease phase margin and can produce excessive ringing and oscillation. Figure 5 shows a circuit that eliminates this problem. The small (usually 5Ω to 20Ω) isolation resistor, R_S, placed before the reactive load prevents ringing and oscillation. At higher capacitive loads, AC performance is controlled by the interaction of the load capacitance and isolation resistor.

Single/Dual, 500MHz, Low-Power, Current-Mode Feedback Amplifiers

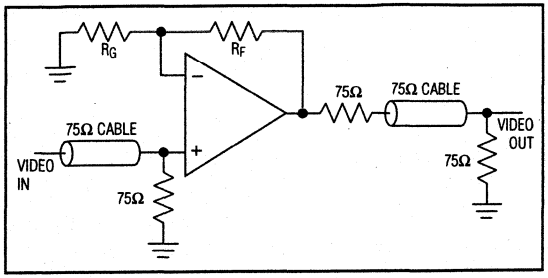


Figure 4. Video Line Driver

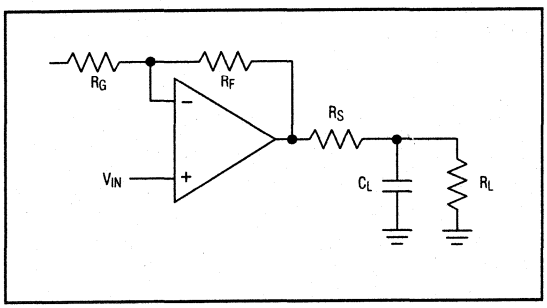


Figure 5a. Using an Isolation Resistor (R_S) for High Capacitive Loads

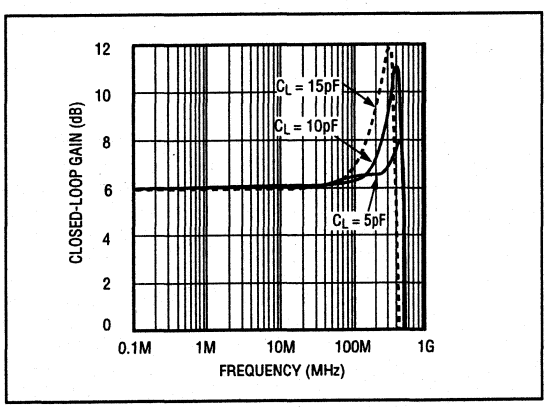


Figure 5b. Frequency Response vs. Capacitive Load—No Isolation Resistor

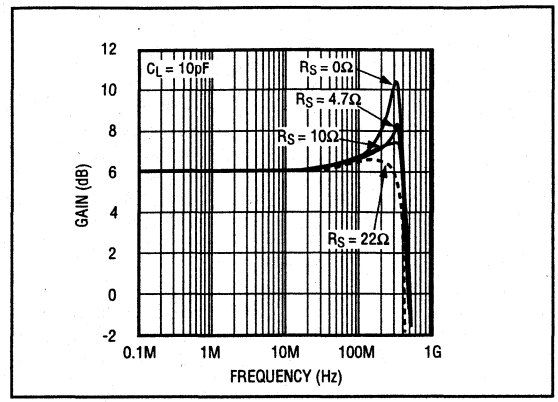


Figure 5c. Frequency Response vs. Isolation Resistance (see Figure 5a for circuit)

Chip Information

TRANSISTOR COUNT: 53 (MAX4112/MAX4113)
112 (MAX4117/MAX4118)

SUBSTRATE CONNECTED TO V_{EE}

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

10/96

MAXIM

Quad, 500MHz, Low-Power, Current-Mode Feedback Amplifiers

General Description

The quad MAX4119/MAX4120 current-mode feedback amplifiers combine high-speed performance with low-power operation. The MAX4119 is optimized for closed-loop gains of 2V/V or greater, while the MAX4120 is optimized for gains of 8V/V or greater.

These devices require only 5mA of supply current per channel, and deliver bandwidths of 500MHz ($A_V \geq 2V/V$) and 275MHz ($A_V \geq 8V/V$), respectively. Their high slew rates (1200V/µs and 1800V/µs) provide exceptional full-power bandwidths (300MHz and 250MHz), making these amplifiers ideal for high-performance pulse and RGB video applications.

These high-speed op amps have a wide output voltage swing of ±3.5V into 100Ω and high current-drive capability of 80mA.

Applications

Broadcast and High-Definition TV Systems

RGB Video

Pulse/RF Amplifier

Ultrasound

Active Filters

ADC Buffers

Features

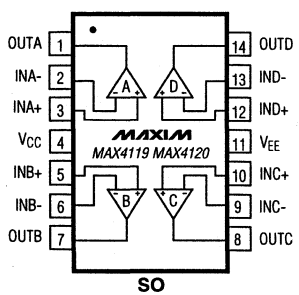
- **500MHz -3dB Bandwidth (MAX4119)**
  275MHz -3dB Bandwidth (MAX4120)
- **1200V/µs Slew Rate (MAX4119)**
  1800V/µs Slew Rate (MAX4120)
- **300MHz Full-Power Bandwidth**
  (V_O = 2Vp-p, MAX4119)
  250MHz Full-Power Bandwidth
  (V_O = 2Vp-p, MAX4120)
- **High Output Drive: 80mA**
- **Low Power: 5mA Supply Current per Channel**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4119ESD	-40°C to +85°C	14 SO
MAX4120ESD	-40°C to +85°C	14 SO

Pin Configuration

TOP VIEW



SO

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

19-1092; Rev 0; 6/96

EVALUATION KIT AVAILABLE

MAXIM

1-Input/6-Output Video Distribution Amplifiers

General Description

The MAX4135/MAX4136 are 1-input/6-output voltage-feedback amplifiers that combine high speed with fast switching for video distribution applications. The MAX4135 is internally set for a closed-loop gain of 2V/V, while the MAX4136 can be externally set for gains of 2V/V or greater.

The MAX4135 achieves a -3dB bandwidth of 185MHz, with 0.1dB gain flatness to 40MHz. The MAX4136's -3dB bandwidth is 140MHz. Both devices deliver a 1000V/µs slew rate, as well as exceptional full-power bandwidths of 185MHz and 140MHz, respectively.

A 25ns channel switching time enables rapid multiplexing for picture-in-picture applications, yet maintains a high off-isolation of 75dB and all-hostile crosstalk of -50dB (f = 30MHz). The MAX4135/MAX4136's on-board logic selects any combination of the six signal outputs. Each output is capable of swinging ±2V and delivering 65mA.

For applications that require a 1-input/4-output distribution amplifier, see the MAX4137/MAX4138 data sheet.

Selector Guide

PART	No. OF OUTPUTS	GAIN (V/V)	-3dB BANDWIDTH (MHz)
MAX4135	6	Fixed 2	185
MAX4136	6	≥2	140
MAX4137	4	Fixed 2	185
MAX4138	4	≥2	140

Applications

Video Switching and Distribution
High-Resolution RGB CRT Monitors
High-Speed Analog Bus Drivers
RF Signal Processing
Composite Video Preamplifiers

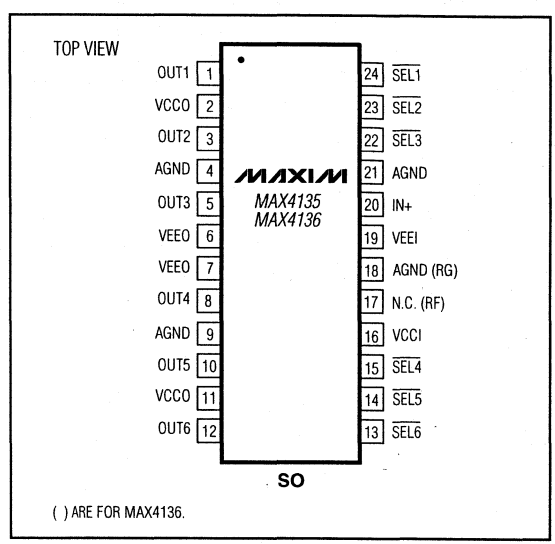
Features

- ♦ **Fixed Gain of 2V/V (MAX4135)**
  External Gain Set (MAX4136)
- ♦ **High Speed:**
  185MHz -3dB Bandwidth (MAX4135)
  140MHz -3dB Bandwidth (MAX4136)
  1000V/µs Slew Rate
- ♦ **High Full-Power Bandwidths (V_{OUT} = 2Vp-p):**
  185MHz (MAX4135)
  140MHz (MAX4136)
- ♦ **0.1dB Gain Flatness to 40MHz**
- ♦ **Low Differential Gain/Phase Error: 0.10%/0.02°**
- ♦ **High-Impedance Output Disable**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4135EWG	-40°C to +85°C	24 Wide SO
MAX4136EWG	-40°C to +85°C	24 Wide SO

Pin Configurations



8

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

1-Input/6-Output Video Distribution Amplifiers

ABSOLUTE MAXIMUM RATINGS

Power-Supply Voltage (V_{CC} to V_{EE}) 12V
Voltage on Any Input Pin to GND ..... (V_{CC} + 0.3V) to (V_{EE} - 0.3V)
Short-Circuit Duration to GND ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
Wide SO (derate 19.3mW/°C above +70°C) 1.54W

Operating Temperature Range
MAX4135EWG/MAX4136EWG ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	V_{OUT} = 0V, R_L = ∞			1	8	mV
Input Offset Voltage Match Between Channels		V_{OUT} = 0V, R_L = ∞			1	6	mV
Input Offset Voltage Drift	TCV_{OS}	V_{OUT} = 0V, R_L = 150Ω			30		µV/°C
Input Bias Current	I_B	V_{OUT} = 0V, R_L = 150Ω, V_{CM} = 0V			4.5	10	µA
Common-Mode Input Resistance	$R_{IN(CM)}$	MAX4136, either input			5		MΩ
Common-Mode Input Capacitance	$C_{IN(CM)}$	MAX4136, either input			2		pF
Input Voltage Noise	e_n	f = 1MHz			7		$nV/\sqrt{Hz}$
		f = 1MHz to 100MHz			88		μV_{RMS}
Input Current Noise	i_n	f = 1MHz			2.4		$pA/\sqrt{Hz}$
		f = 1MHz to 100MHz			30		nA_{RMS}
Input Capacitance	C_{IN}				2		pF
Common-Mode Input Voltage Range	V_{CM}	MAX4136			±2.5		V
Common-Mode Rejection Ratio	CMRR	MAX4136, V_{CM} = ±2.5V			60		dB
Power-Supply Rejection Ratio	PSRR	V_S = ±4.75V to ±5.25V		55	65		dB
Quiescent Supply Current	I_{SY}	V_{IN} = 0V	All channels off		45	55	mA
			All channels on		70	80	
Output Voltage Swing	V_{OUT}	R_L = 150Ω	Positive	+2.2	+2.6		V
			Negative	-2.0	-2.5		
Output Current Drive	I_{OUT}	R_L = 30Ω		45	65		mA
$\overline{SEL}$ High Threshold	V_{IH}					2.0	V
$\overline{SEL}$ Low Threshold	V_{IL}			0.8			V
$\overline{SEL}$ Input Current	$I_{\overline{SEL}}$				1	5	µA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, A_{VCL} = 2V/V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

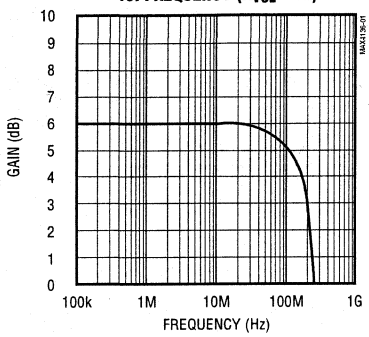
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
-3dB Bandwidth	BW_{-3dB}	$V_{OUT} \le 0.1V_{RMS}$, A_{VCL} = 2V/V	MAX4135		185		MHz
			MAX4136		140		
Full-Power Bandwidth	FPBW	V_{OUT} = 2Vp-p, A_{VCL} = 2V/V	MAX4135		185		MHz
			MAX4136		140		
0.1dB Bandwidth		A_{VCL} = 2V/V			40		MHz
Slew Rate	SR	-2V ≤ V_{OUT} ≤ 2V			1000		V/µs
Settling Time	t_S	-1V ≤ V_{OUT} ≤ 1V/V, R_L = 150Ω, A_{VCL} = 2V/V	to 0.1%		17		ns
			to 0.01%		40		
Differential Gain	DG	f = 3.58MHz, A_{VCL} = 2V/V	MAX4135		0.10		%
			MAX4136		0.10		
Differential Phase	DP	f = 3.58MHz, A_{VCL} = 2V/V	MAX4135		0.02		degrees
			MAX4136		0.02		
All-Hostile Crosstalk		V_{IN} = 1Vp-p, f = 30MHz			-50		dB
Off Isolation		V_{IN} = 1Vp-p, f = 30MHz			75		dB
Channel Switching Off Time	t_{OFF}				25		ns
Channel Switching On Time	t_{ON}				25		ns
Digital Switching Feedthrough		V_{IN} = $0V_{DC}$			±1		mV
Spurious-Free Dynamic Range	SFDR	f_C = 5MHz, A_{VCL} = 2V/V, V_{OUT} = 2Vp-p, R_L = 100Ω			-72		dBc
Output On-Resistance	R_{OUT}	f = DC, A_{VCL} = 2V/V			1		Ω
Output Off-Resistance	R_{OUT}	f = DC, A_{VCL} = 2V/V			200		kΩ
Output On-Capacitance	$C_{OUT(ON)}$				2		pF
Output Off-Capacitance	$C_{OUT(OFF)}$				3.5		pF

1-Input/6-Output Video Distribution Amplifiers

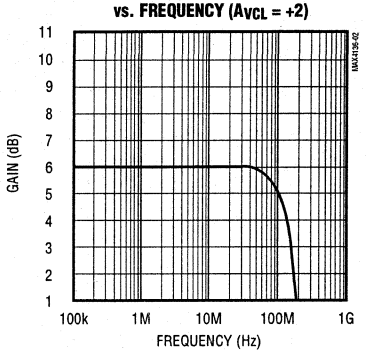
Typical Operating Characteristics

(V_{CC} = +5V, V_{EE} = -5V, R_L = 150Ω, T_A = +25°C, unless otherwise noted.)

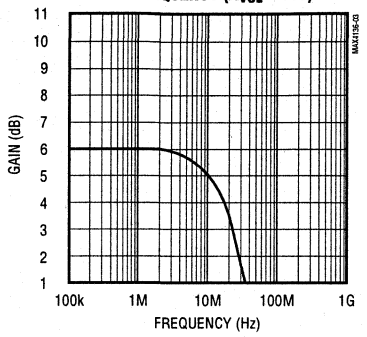
MAX4135 SMALL-SIGNAL GAIN vs. FREQUENCY (A_{VCL} = +2)



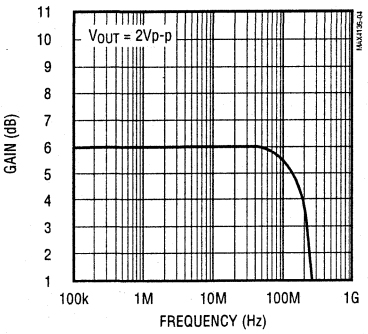
MAX4136 SMALL-SIGNAL GAIN vs. FREQUENCY (A_{VCL} = +2)



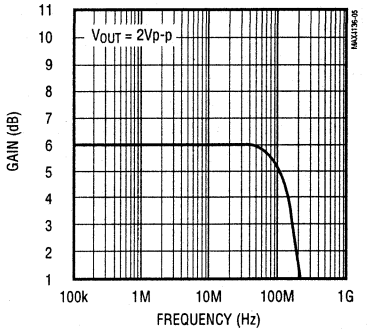
MAX4136 SMALL-SIGNAL GAIN vs. FREQUENCY (A_{VCL} = +10)



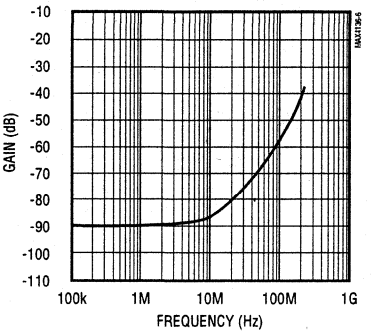
MAX4135 LARGE-SIGNAL GAIN vs. FREQUENCY (A_{VCL} = +2)



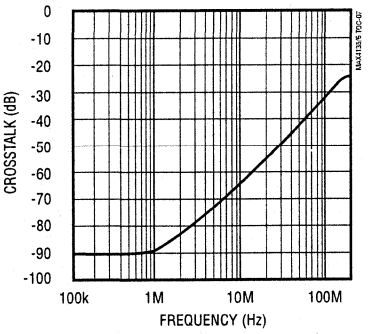
MAX4136 LARGE-SIGNAL GAIN vs. FREQUENCY (A_{VCL} = +2)



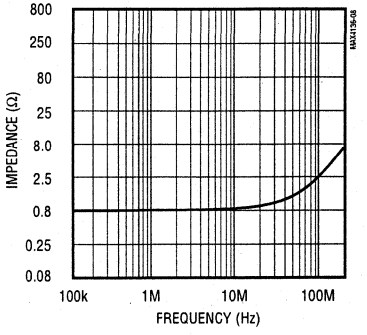
OFF-ISOLATION vs. FREQUENCY



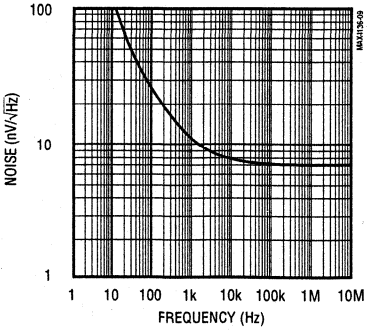
ALL-HOSTILE CROSSTALK vs. FREQUENCY



CLOSED-LOOP OUTPUT IMPEDANCE vs. FREQUENCY



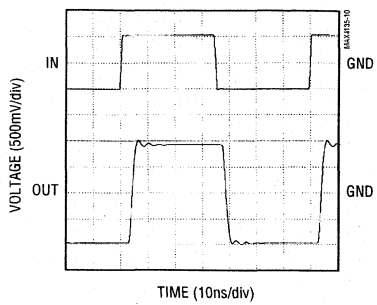
INPUT VOLTAGE NOISE vs. FREQUENCY



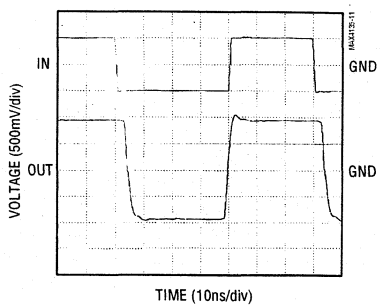
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, R_L = 150Ω, T_A = +25°C, unless otherwise noted.)

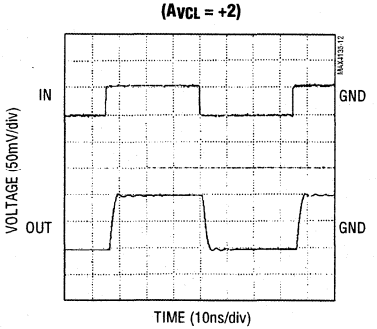
MAX4135
LARGE-SIGNAL PULSE RESPONSE
(A_{VCL} = +2)



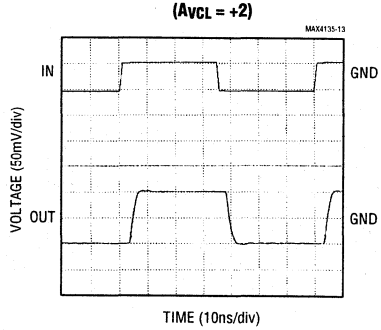
MAX4136
LARGE-SIGNAL PULSE RESPONSE
(A_{VCL} = +2)



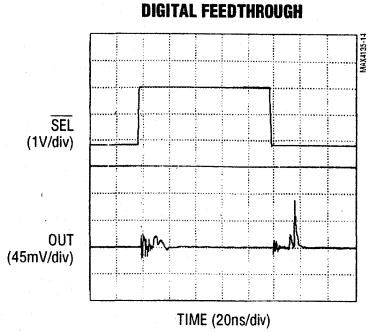
MAX4135
SMALL-SIGNAL PULSE RESPONSE
(A_{VCL} = +2)



MAX4136
SMALL-SIGNAL PULSE RESPONSE
(A_{VCL} = +2)



DIGITAL FEEDTHROUGH



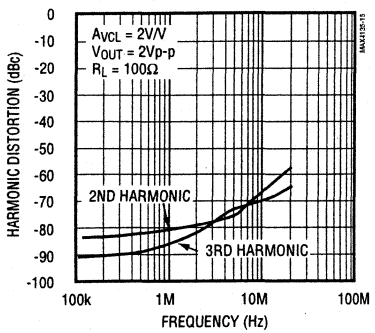
8

1-Input/6-Output Video Distribution Amplifiers

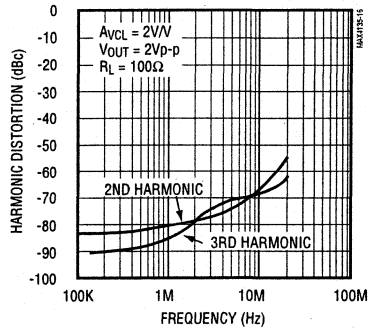
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, R_L = 150Ω, T_A = +25°C, unless otherwise noted.)

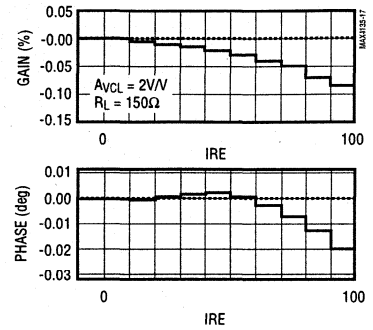
MAX4135
HARMONIC DISTORTION vs. FREQUENCY



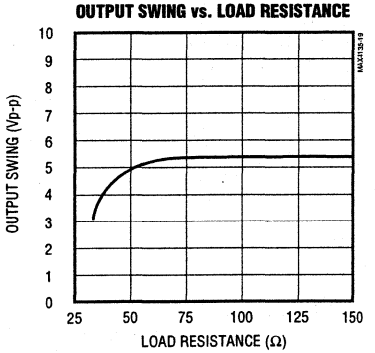
MAX4136
HARMONIC DISTORTION vs. FREQUENCY



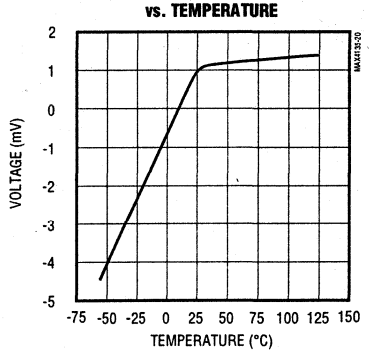
DIFFERENTIAL GAIN AND PHASE



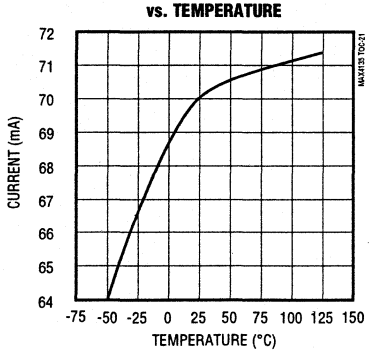
MAX4135
OUTPUT SWING vs. LOAD RESISTANCE



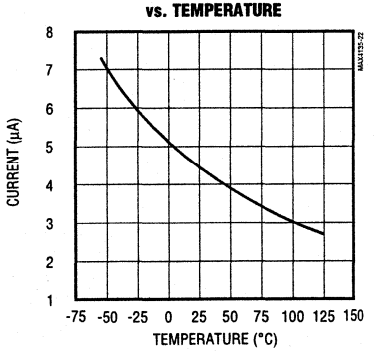
INPUT OFFSET VOLTAGE vs. TEMPERATURE



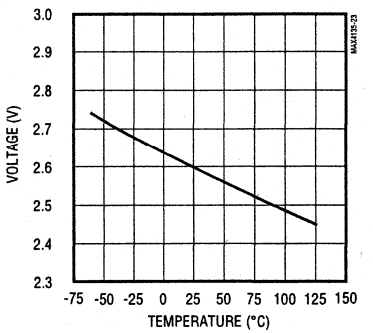
MAX4135/6 POWER SUPPLY CURRENT vs. TEMPERATURE



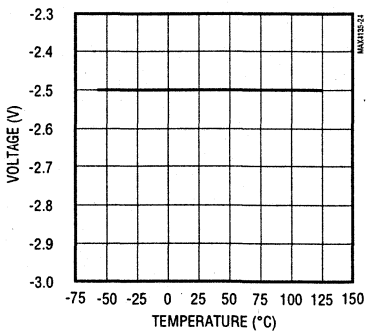
INPUT BIAS CURRENT vs. TEMPERATURE



POSITIVE OUTPUT VOLTAGE SWING vs. TEMPERATURE



NEGATIVE OUTPUT VOLTAGE SWING vs. TEMPERATURE



1-Input/6-Output Video Distribution Amplifiers

Pin Description

PIN		NAME	FUNCTION
MAX4135	MAX4136		
1	1	OUT1	Output 1
2, 11	2, 11	VCCO	Positive Supply for Output Amplifiers. Connect to +5V.
3	3	OUT2	Output 2
4, 9, 18, 21	4, 9, 21	AGND	Analog Ground
5	5	OUT3	Output 3
6, 7	6, 7	VEEO	Negative Supply for Output Amplifiers. Connect to -5V.
8	8	OUT4	Output 4
10	10	OUT5	Output 5
12	12	OUT6	Output 6
13	13	$\overline{SEL6}$	When low, enables output channel OUT6. When high, disables output channel OUT6.
14	14	$\overline{SEL5}$	When low, enables output channel OUT5. When high, disables output channel OUT5.
15	15	$\overline{SEL4}$	When low, enables output channel OUT4. When high, disables output channel OUT4.
16	16	VCCI	Positive Supply for Input Amplifier. Connect to +5V.
17	—	N.C.	No Connect. Not internally connected.
—	17	RF	Output of Input Amplifier
—	18	RG	Inverting Input
19	19	VEEI	Negative Supply for Input Amplifier. Connect to -5V.
20	20	IN+	Noninverting Input
22	22	$\overline{SEL3}$	When low, enables output channel OUT3. When high, disables output channel OUT3.
23	23	$\overline{SEL2}$	When low, enables output channel OUT2. When high, disables output channel OUT2.
24	24	$\overline{SEL1}$	When low, enables output channel OUT1. When high, disables output channel OUT1.

Detailed Description

The MAX4135/MAX4136 are 1-input/6-output video distribution amplifiers. The MAX4135 is configured for a fixed gain of +2, while the MAX4136 features external gain control (feedback) for closed-loop gains of 2V/V or greater.

Each output provides sufficient current to drive five 150Ω loads. However, distortion will increase when driving multiple loads. The TTL/CMOS-compatible digital control ($\overline{SEL_}$) enables or disables each output amplifier. When the $\overline{SEL_}$ control input is low, the amplifier is enabled; when it is high, the amplifier is disabled and presents a high-impedance output. The enable/disable or disable/enable time is under 25ns, which is useful in multiplexing, pixel switching, or picture-in-picture applications.

Each device has an input amplifier, which buffers the input from any switching glitches that may occur at the output stage, and provides a high-impedance, low-capacitance input. The separate input buffer allows a true high output impedance when an amplifier is disabled.

The outputs are protected against short circuits to ground. However, power-dissipation limits preclude shorting all output channels to ground. See the *Power-Dissipation Considerations* section for details.

1-Input/6-Output Video Distribution Amplifiers

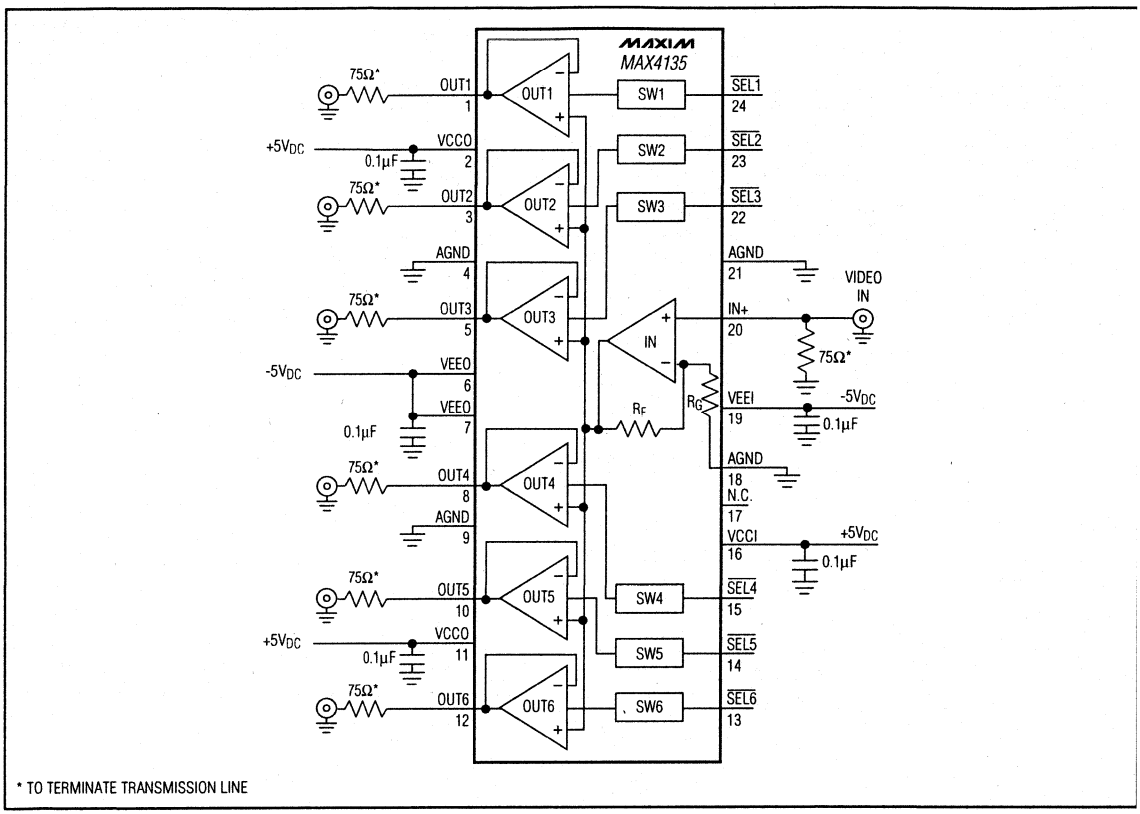


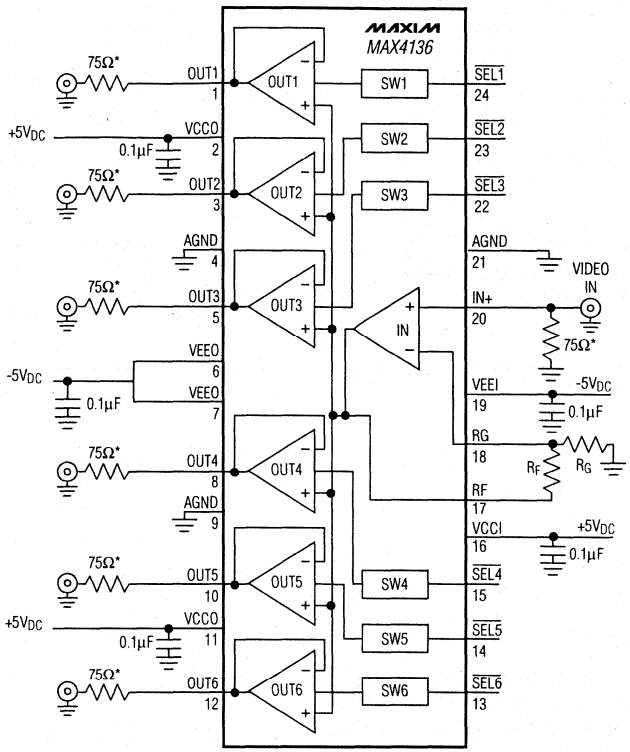
Figure 1. MAX4135 Typical Operating Circuit

Applications Information

Grounding, Bypassing, and PC Board Layout

To obtain the MAX4135/MAX4136's full 185MHz bandwidth, Microstrip and Stripline techniques are recommended in most cases. To ensure that the PC board does not degrade the amplifier's performance, design the board for a frequency greater than 1GHz. Even with very short traces, use these techniques at critical points, such as inputs and outputs. Whether you use a constant-impedance board or not, observe the following guidelines when designing the board:

- Do not use wire-wrap boards. They are too inductive.
- Do not use IC sockets. They increase parasitic capacitance and inductance.
- In general, surface-mount components have shorter leads and lower parasitic reactance, giving better high-frequency performance than through-hole components.
- The PC board should have at least two layers, with one side a signal layer and the other a ground plane.
- Keep signal lines as short and straight as possible. Do not make 90° turns; round all corners.
- The ground plane should be as free from voids as possible.



* TO TERMINATE TRANSMISSION LINE

Figure 2. MAX4136 Typical Operating Circuit

8

Driving Capacitive Loads

The MAX4135/MAX4136 provide maximum AC performance with no output load capacitance. This is the case when they are driving a correctly terminated transmission line (i.e., a back-terminated 75Ω cable). However, the MAX4135/MAX4136 are capable of driving capacitive loads up to 10pF without oscillations, but with reduced AC performance.

Driving large capacitive loads increases the chance of oscillations in most amplifier circuits. This is especially true for circuits with high loop gain, such as voltage followers. The amplifier's output resistance and the load capacitor combine to add a pole and excess phase to the loop response. If the frequency of this pole is low enough and phase margin is degraded sufficiently, oscillations may occur.

A second problem when driving capacitive loads results from the amplifier's output impedance, which looks inductive at high frequencies. This inductance forms an L-C resonant circuit with the capacitive load, which causes peaking in the frequency response and degrades the amplifier's gain margin.

The MAX4135/MAX4136 drive capacitive loads up to 10pF without oscillation. However, some peaking (in the frequency domain) or ringing (in the time domain) may occur (Figure 3).

1-Input/6-Output Video Distribution Amplifiers

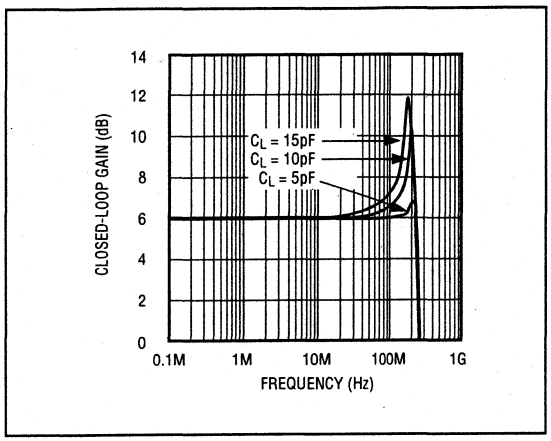


Figure 3. Effect of C_{LOAD} on Frequency Response (without R_{ISO})

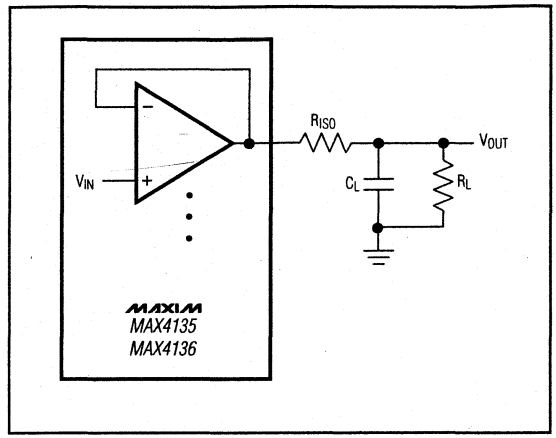


Figure 4. Capacitive-Load Driving Circuit

To drive larger-capacitance loads or to reduce ringing, add an isolation resistor between the amplifier's output and the load, as shown in Figure 4.

The value of R_{ISO} depends on the circuit's gain and the capacitive load. Figure 5 shows the optimal isolation resistor (R_{ISO}) vs. capacitive load (C_L). At the higher capacitor values, the bandwidth is dominated by the RC network, formed by R_{ISO} and C_L.

Power-Dissipation Considerations

The MAX4135/MAX4136 can drive up to six outputs simultaneously. Quiescent power dissipation is typically 750mW and 800mW maximum, respectively, with all channels enabled. The maximum package power dissipation is rated at 1540mW.

In a typical application, six outputs drive a standard video signal into a 150Ω load. The amount of power added to the quiescent dissipation is minimal and no special precautions are necessary.

However, each output driving the maximum 65mA into 30Ω will cause a power-dissipation increase of approximately 200mW. Therefore, you should not allow more than three outputs to deliver that load simultaneously. Similarly, one output shorted to ground will cause a power-dissipation increase of 650mW. Only one output can be shorted to ground without violating the package power rating.

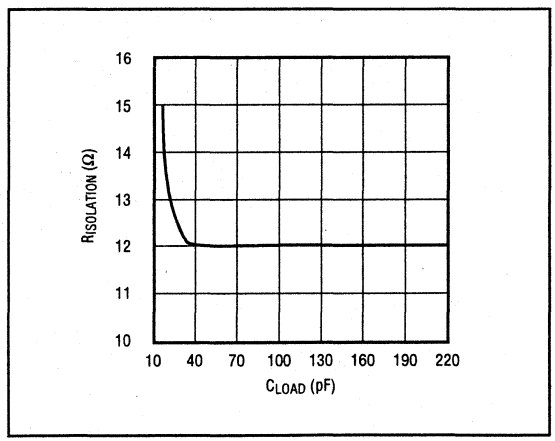


Figure 5. Optimal Isolation Resistor (R_{ISO}) vs. C_{LOAD}

In conclusion, during normal operation in a matched-load environment, the total power dissipation is well within the package's dissipation rating. The maximum power dissipation is violated only if multiple channels are driving the maximum current into minimum loads at the same time.

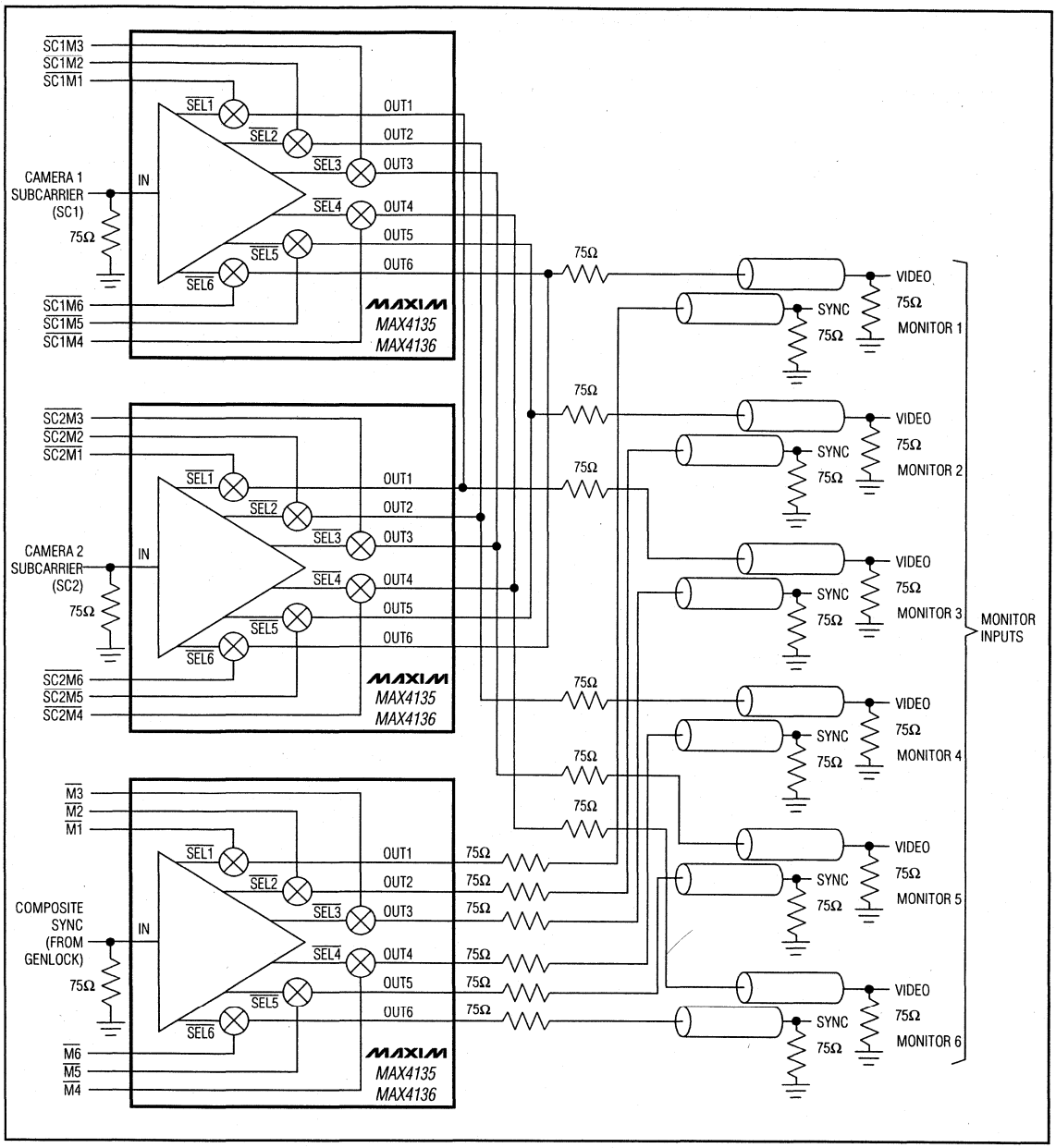


Figure 6. Two Cameras to Six Monitors Distribution Amplifier

1-Input/6-Output Video Distribution Amplifiers

Chip Information

TRANSISTOR COUNT: 901

SUBSTRATE CONNECTED TO V_{EE}

19-2001; Rev 0; 6/96

EVALUATION KIT AVAILABLE

MAXIM

1-Input/4-Output Video Distribution Amplifiers

General Description

The MAX4137/MAX4138 are 1-input/4-output voltage-feedback amplifiers that combine high speed with fast switching for video distribution applications. The MAX4137 is internally set for a closed-loop gain of 2V/V, while the MAX4138 can be externally set for gains of 2V/V or greater.

The MAX4137 achieves a -3dB bandwidth of 185MHz, with 0.1dB gain flatness to 40MHz. The MAX4138's -3dB bandwidth is 140MHz, with 0.1dB gain flatness to 40MHz. Both devices deliver a 1000V/µs slew rate, as well as exceptional full-power bandwidths of 185MHz and 140MHz, respectively.

A 25ns channel switching time enables rapid multiplexing for picture-in-picture applications, yet maintains a high off-isolation of 75dB and all-hostile crosstalk of -50dB (f = 30MHz). The MAX4137/MAX4138's on-board logic selects any combination of the four signal outputs. Each output is capable of swinging ±2V and delivering up to 65mA of current.

For applications that require a 1-input/6-output distribution amplifier, see the MAX4135/MAX4136 data sheet.

Selector Guide

PART	No. OF OUTPUTS	GAIN (V/V)	-3dB BANDWIDTH (MHz)
MAX4135	6	Fixed 2	185
MAX4136	6	≥2	140
MAX4137	4	Fixed 2	185
MAX4138	4	≥2	140

Applications

Video Switching and Distribution
High-Resolution RGB CRT Monitors
High-Speed Analog Bus Drivers
RF Signal Processing
Composite Video Preamplifiers

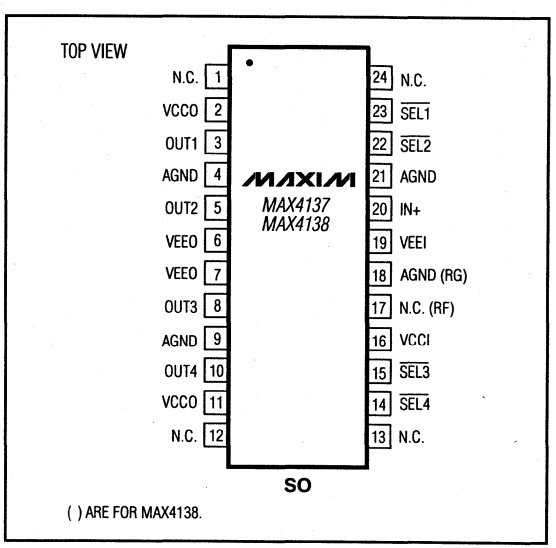
Features

- **Fixed Gain of 2V/V (MAX4137)**
  External Gain Set (MAX4138)
- **High Speed:**
  185MHz -3dB Bandwidth (MAX4137)
  140MHz -3dB Bandwidth (MAX4138)
  1000V/µs Slew Rate
- **High Full-Power Bandwidths (V_{OUT} = 2Vp-p):**
  185MHz (MAX4137)
  140MHz (MAX4138)
- **0.1dB Gain Flatness to 40MHz**
- **Low Differential Gain/Phase Error: 0.10%/0.02°**
- **High-Impedance Output Disable**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4137EWG	-40°C to +85°C	24 Wide SO
MAX4138EWG	-40°C to +85°C	24 Wide SO

Pin Configurations



8

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

1-Input/4-Output Video Distribution Amplifiers

ABSOLUTE MAXIMUM RATINGS

Power-Supply Voltage (V_{CC} to V_{EE}).....12V
Voltage on Any Input Pin to GND .....(V_{CC} + 0.3V) to (V_{EE} - 0.3V)
Short-Circuit Duration to GND.....Continuous
Continuous Power Dissipation (T_A = +70°C)
Wide SO (derate 19.3mW/°C above +70°C).....1.54W

Operating Temperature Range
MAX4137EWG/MAX4138EWG .....-40°C to +85°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	V_{OUT} = 0V, R_L = 150Ω			1	8.0	mV
Input Offset Voltage Match Between Channels		V_{OUT} = 0V, R_L = 150Ω			1	6	mV
Input Offset Voltage Drift	TCV_{OS}	V_{OUT} = 0V, R_L = ∞			30		µV/°C
Input Bias Current	I_B	V_{OUT} = 0V, R_L = ∞, V_{IN} = $-V_{OS}$			4.5	10	µA
Common-Mode Input Resistance	$R_{IN(CM)}$	MAX4138, either input			5		MΩ
Common-Mode Input Capacitance	$C_{IN(CM)}$	MAX4138, either input			2		pF
Input Voltage Noise	e_n	f = 1MHz			7		$nV/\sqrt{Hz}$
		f = 1MHz to 100MHz			88		μV_{RMS}
Input Current Noise	i_n	f = 1MHz			2.4		$pA/\sqrt{Hz}$
		f = 1MHz to 100MHz			30		nA_{RMS}
Input Capacitance	C_{IN}				2		pF
Common-Mode Input Voltage Range	V_{CM}				±2.5		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±2.5V			60		dB
Power-Supply Rejection Ratio	PSRR	V_S = ±4.75V to ±5.25V		55	65		dB
Quiescent Supply Current	I_{SY}	V_{IN} = 0V	All channels off		30	40	mA
			All channels on		47	60	
Output Voltage Swing	V_{OUT}	R_L = 150Ω	Positive	2.2	2.6		V
			Negative	-2.0	-2.5		
Output Current Drive	I_{OUT}	R_L = 30Ω		45	65		mA
$\overline{SEL}$ High Threshold	V_{IH}					2.0	V
$\overline{SEL}$ Low Threshold	V_{IL}			0.8			V
$\overline{SEL}$ Input Current	$I_{\overline{SEL}}$				1	5	µA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, A_{VCL} = 2V/V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = 25°C.)

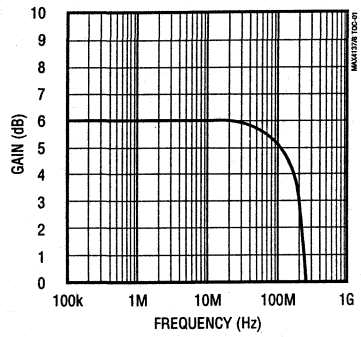
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
-3dB Bandwidth	BW_{-3dB}	$V_{OUT} \le 0.1V_{RMS}$, A_{VCL} = 2V/V	MAX4137		185		MHz
			MAX4138		140		
Full-Power Bandwidth	FPBW	V_{OUT} = 2Vp-p, A_{VCL} = 2V/V	MAX4137		185		MHz
			MAX4138		140		
0.1dB Bandwidth		A_{VCL} = 2V/V			40		MHz
Slew Rate	SR	$-2V \le V_{OUT} \le +2V$			1000		V/µs
Settling Time	t_S	$-1V \le V_{OUT} \le +1V$, R_L=150Ω, A_{VCL}=2V/V	to 0.1%		17		ns
			to 0.01%		40		
Differential Gain	DG	f = 3.58MHz, A_{VCL} = 2V/V	MAX4137		0.10		%
			MAX4138		0.10		
Differential Phase	DP	f = 3.58MHz, A_{VCL} = 2V/V	MAX4137		0.02		degrees
			MAX4138		0.02		
All-Hostile Crosstalk		V_{IN} = 1Vp-p, f = 30MHz			-50		dB
Off Isolation		V_{IN} = 1Vp-p, f = 30MHz			75		dB
Channel Switching Off Time	t_{OFF}				25		ns
Channel Switching On Time	t_{ON}				25		ns
Digital Switching Feedthrough		V_{IN} = 0V_{DC}			±1		mV
Spurious-Free Dynamic Range	SFDR	f_C = 5MHz, A_{VCL} = 2V/V, V_{OUT} = 2Vp-p, R_L = 100Ω			-72		dBc
Output On-Resistance	R_{OUT}	f = DC, A_{VCL} = 2V/V			1		Ω
Output Off-Resistance	R_{OUT}	f = DC, A_{VCL} = 2V/V			200		kΩ
Output On-Capacitance	$C_{OUT(ON)}$				2		pF
Output Off-Capacitance	$C_{OUT(OFF)}$				3.5		pF

1-Input/4-Output Video Distribution Amplifiers

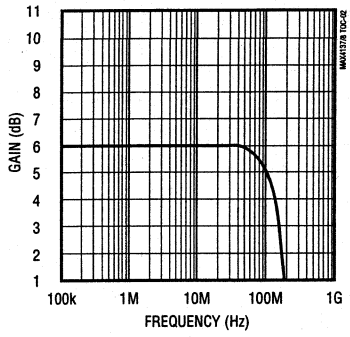
Typical Operating Characteristics

(V_{CC} = +5V, V_{EE} = -5V, R_L = 150Ω, T_A = +25°C, unless otherwise noted.)

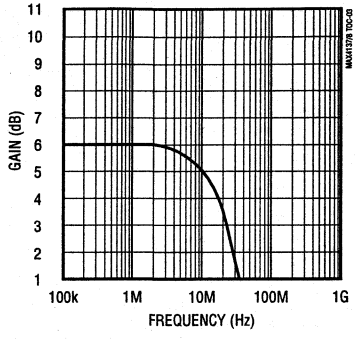
MAX4137 SMALL-SIGNAL GAIN vs. FREQUENCY (A_{VCL} = +2)



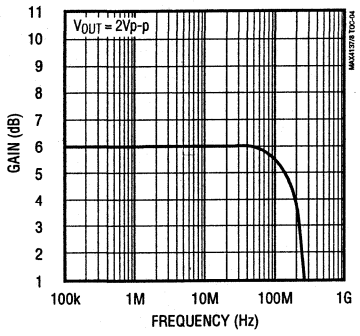
MAX4138 SMALL-SIGNAL GAIN vs. FREQUENCY (A_{VCL} = +2)



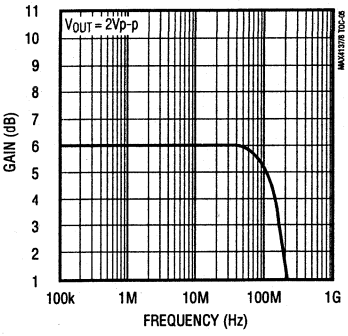
MAX4138 SMALL-SIGNAL GAIN vs. FREQUENCY (A_{VCL} = +10)



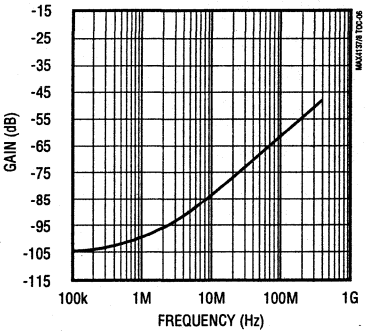
MAX4137 LARGE-SIGNAL GAIN vs. FREQUENCY (A_{VCL} = +2)



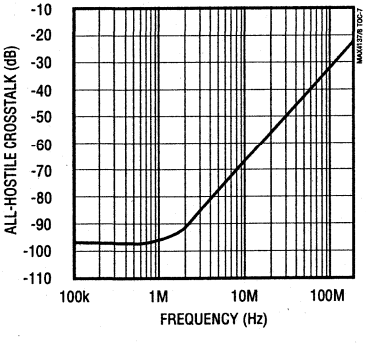
MAX4138 LARGE-SIGNAL GAIN vs. FREQUENCY (A_{VCL} = +2)



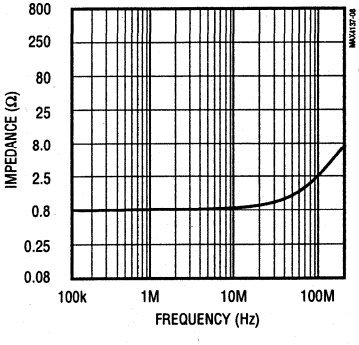
OFF-ISOLATION vs. FREQUENCY



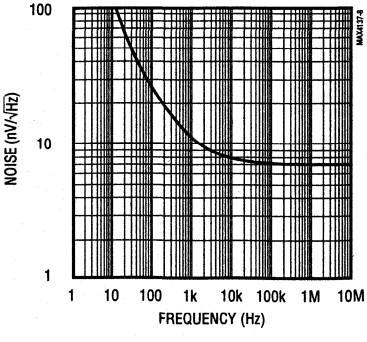
ALL-HOSTILE CROSSTALK vs. FREQUENCY



CLOSED-LOOP OUTPUT IMPEDANCE vs. FREQUENCY



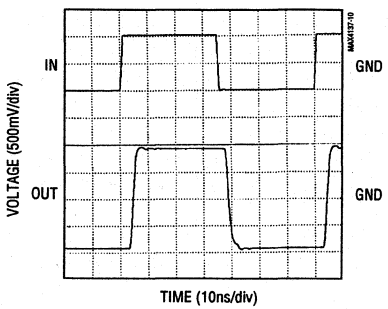
INPUT VOLTAGE NOISE vs. FREQUENCY



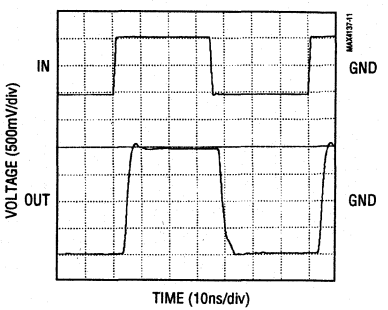
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, R_L = 150Ω, T_A = +25°C, unless otherwise noted.)

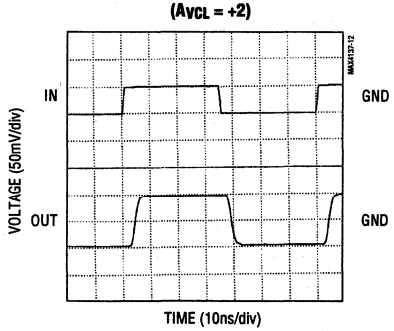
MAX4137
LARGE-SIGNAL PULSE RESPONSE
(A_{VCL} = +2)



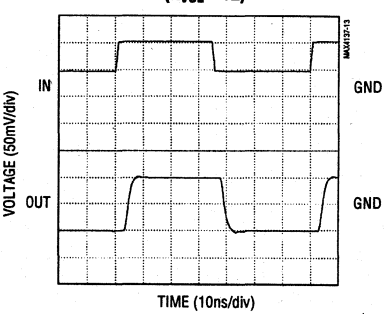
MAX4138
LARGE-SIGNAL PULSE RESPONSE
(A_{VCL} = +2)



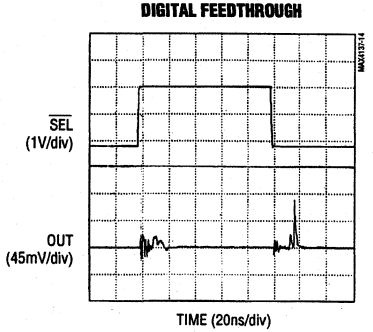
MAX4137
SMALL-SIGNAL PULSE RESPONSE
(A_{VCL} = +2)



MAX4138
SMALL-SIGNAL PULSE RESPONSE
(A_{VCL} = +2)



DIGITAL FEEDTHROUGH

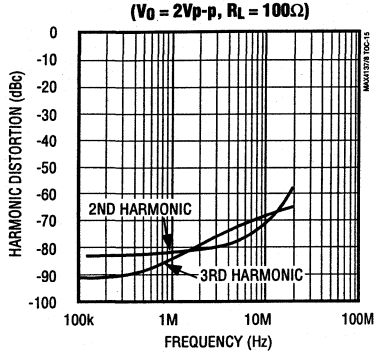


1-Input/4-Output Video Distribution Amplifiers

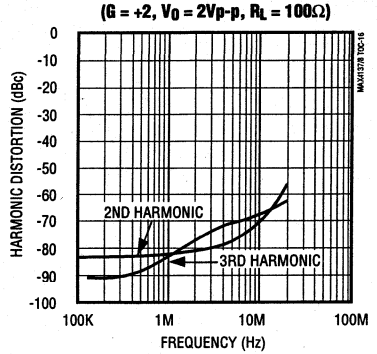
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, R_L = 150Ω, T_A = +25°C, unless otherwise noted.)

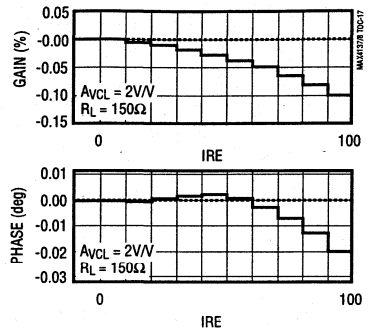
MAX4137
HARMONIC DISTORTION vs. FREQUENCY
(V_O = 2Vp-p, R_L = 100Ω)



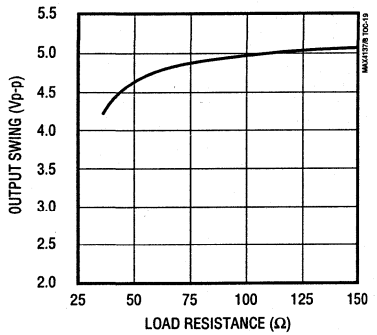
MAX4138
HARMONIC DISTORTION vs. FREQUENCY
(G = +2, V_O = 2Vp-p, R_L = 100Ω)



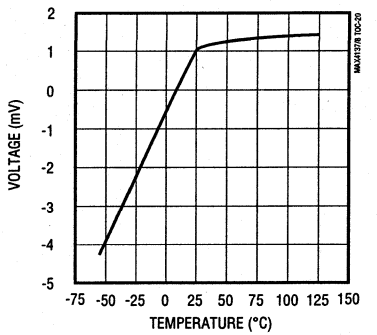
DIFFERENTIAL GAIN AND PHASE



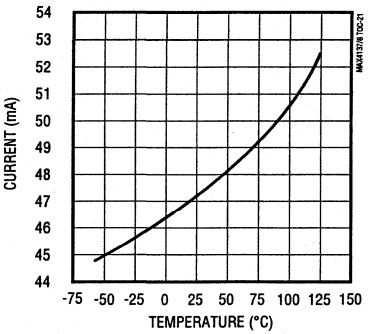
MAX4137
OUTPUT SWING vs. LOAD RESISTANCE



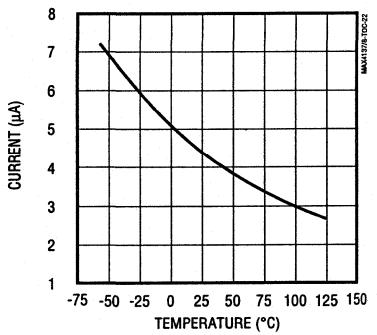
INPUT OFFSET VOLTAGE vs. TEMPERATURE



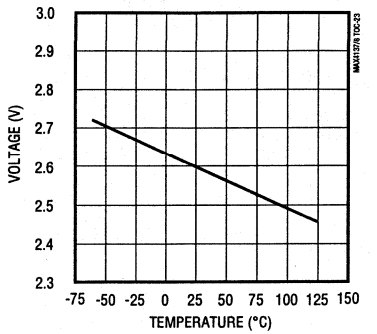
POWER SUPPLY CURRENT vs. TEMPERATURE



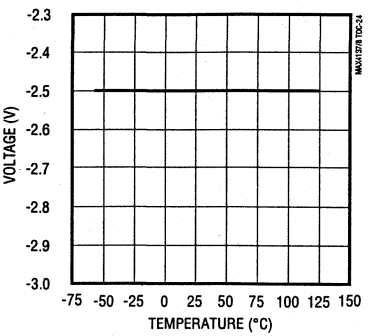
INPUT BIAS CURRENT vs. TEMPERATURE



POSITIVE OUTPUT VOLTAGE SWING vs. TEMPERATURE



NEGATIVE OUTPUT VOLTAGE SWING vs. TEMPERATURE



1-Input/4-Output Video Distribution Amplifiers

Pin Description

PIN		NAME	FUNCTION
MAX4137	MAX4138		
1, 12, 13, 17, 24	1, 12, 13, 24	N.C.	No Connect. Not internally connected.
2, 11	2, 11	VCCO	Positive Supply for Output Amplifiers. Connect to +5V.
3	3	OUT1	Output 1
4, 9, 18, 21	4, 9, 21	AGND	Analog Ground
5	5	OUT2	Output 2
6, 7	6, 7	VEEO	Negative Supply for Output Amplifiers. Connect to -5V.
8	8	OUT3	Output 3
10	10	OUT4	Output 4
14	14	$\overline{SEL4}$	When low, enables output channel OUT4. When high, disables output channel OUT4.
15	15	$\overline{SEL3}$	When low, enables output channel OUT3. When high, disables output channel OUT3.
16	16	VCCI	Positive Supply for Input Amplifier. Connect to +5V.
—	17	RF	Output of Input Amplifier
—	18	RG	Inverting Input
19	19	VEEI	Negative Supply for Input Amplifier. Connect to -5V.
20	20	IN+	Noninverting Input
22	22	$\overline{SEL2}$	When low, enables output channel OUT2. When high, disables output channel OUT2.
23	23	$\overline{SEL1}$	When low, enables output channel OUT1. When high, disables output channel OUT1.

Detailed Description

The MAX4137/MAX4138 are 1-input/4-output video distribution amplifiers. The MAX4137 is configured for a fixed gain of +2, while the MAX4138 features external gain control (feedback) for closed-loop gains of 2V/V or greater.

Each output provides sufficient current to drive five 50Ω loads. However, distortion will increase when driving multiple loads. The TTL/CMOS-compatible digital control ($\overline{SEL_}$) enables or disables each output amplifier. When the $\overline{SEL_}$ control input is low, the amplifier is enabled; when it is high, the amplifier is disabled and presents a high-impedance output. The enable/disable or disable/enable time is under 25ns, which is useful in multiplexing, pixel switching, or picture-in-picture applications.

Each device has an input amplifier, which buffers the input from any switching glitches that may be taking place at the output stage, and provides a high-impedance, low-capacitance input. The separate input buffer allows a true high output impedance when an amplifier is disabled.

The outputs are protected against short circuits to ground. However, power-dissipation limits preclude shorting all output channels to ground. See the *Power-Dissipation Considerations* section for details.

1-Input/4-Output Video Distribution Amplifiers

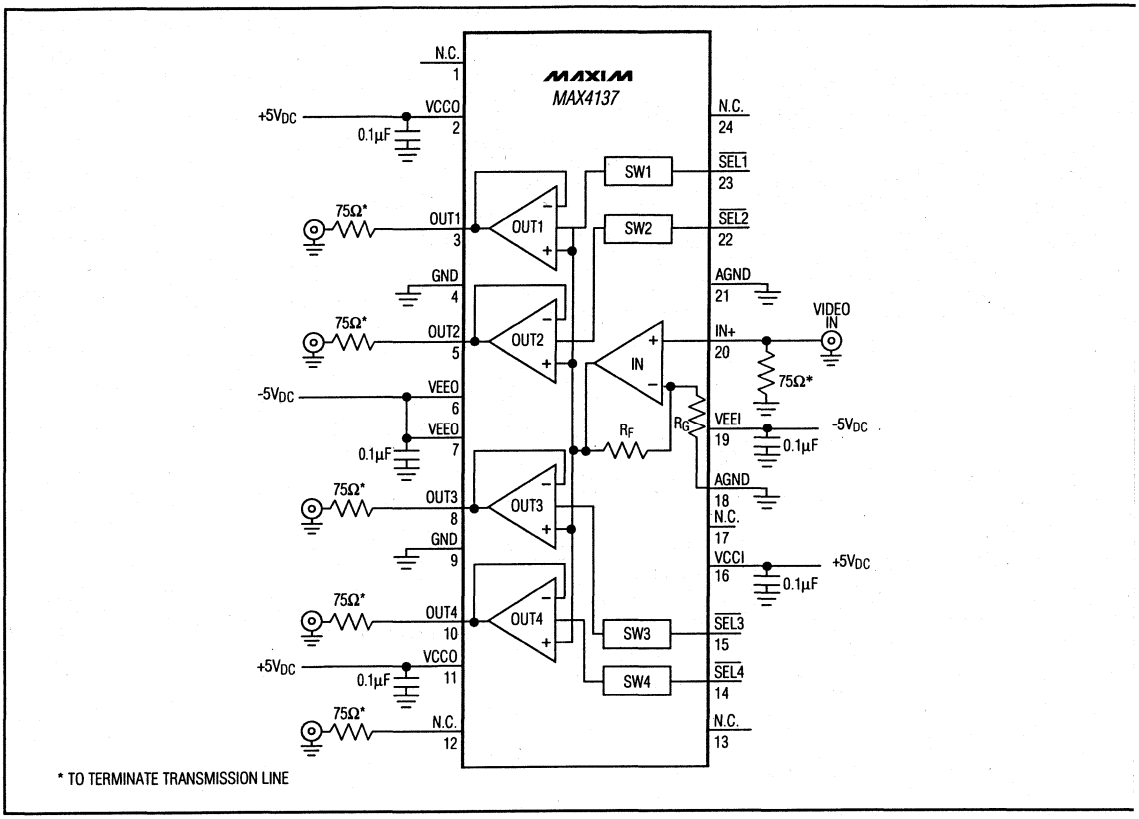


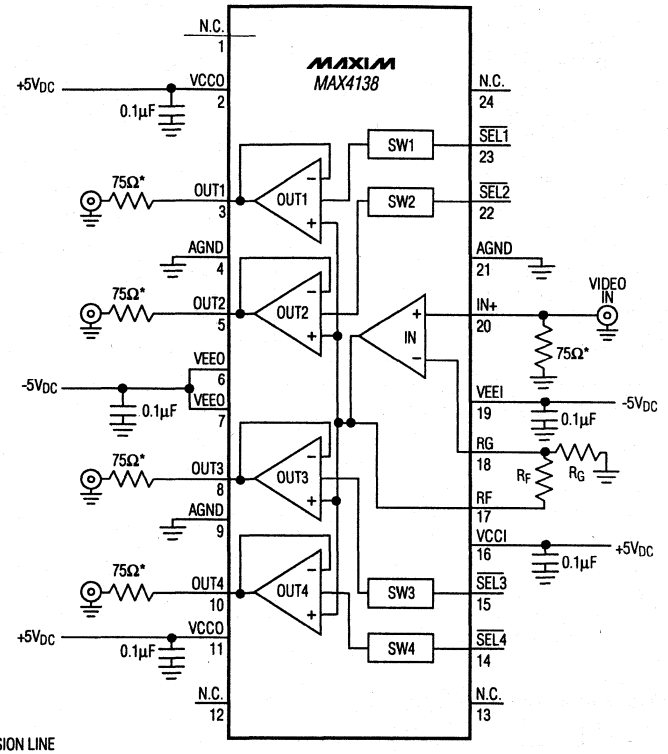
Figure 1. MAX4137 Typical Operating Circuit

Applications Information

Grounding, Bypassing, and PC Board Layout

To obtain the MAX4137/MAX4138's full 185MHz bandwidth, Microstrip and Stripline techniques are recommended in most cases. To ensure the PC board does not degrade the amplifier's performance, design the board for a frequency greater than 1GHz. Even with very short traces, use these techniques at critical points, such as inputs and outputs. Whether you use a constant-impedance board or not, observe the following guidelines when designing the board:

- Do not use wire-wrap boards. They are too inductive.
- Do not use IC sockets. They increase parasitic capacitance and inductance.
- In general, surface-mount components have shorter leads and lower parasitic reactance, giving better high-frequency performance than through-hole components.
- The PC board should have at least two layers, with one side a signal layer and the other a ground plane.
- Keep signal lines as short and straight as possible. Do not make 90° turns; round all corners.
- The ground plane should be as free from voids as possible.



* TO TERMINATE TRANSMISSION LINE

igure 2. MAX4138 Typical Operating Circuit

Driving Capacitive Loads

he MAX4137/MAX4138 provide maximum AC perfor- ıance with no output load capacitance. This is the ase when they are driving a correctly terminated trans- ıission line (i.e., a back-terminated 75Ω cable). lowever, the MAX4137/MAX4138 are capable of riving capacitive loads up to 10pF without oscillations, ut with reduced AC performance.

ıriving large capacitive loads increases the chance of scillations in most amplifier circuits. This is especially ue for circuits with high loop gain, such as voltage fol- ıwers. The amplifier's output resistance and the load apacitor combine to add a pole and excess phase to the loop response. If the frequency of this pole is low enough and phase margin is degraded sufficiently, oscillations may occur.

A second problem when driving capacitive loads results from the amplifier's output impedance, which looks inductive at high frequencies. This inductance forms an L-C resonant circuit with the capacitive load, which causes peaking in the frequency response and degrades the amplifier's gain margin.

The MAX4137/MAX4138 drive capacitive loads up to 10pF without oscillation. However, some peaking (in the frequency domain) or ringing (in the time domain) may occur (Figure 3).

1-Input/4-Output Video Distribution Amplifiers

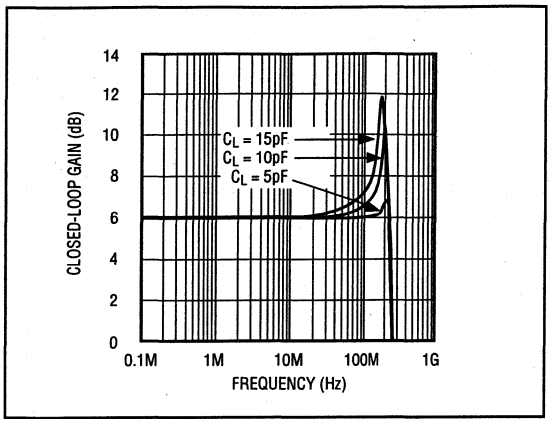


Figure 3. Effect of C_{LOAD} on Frequency Response (without R_{ISO})

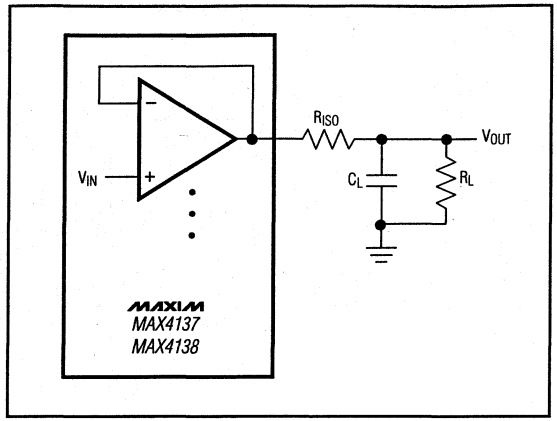


Figure 4. Capacitive-Load Driving Circuit

To drive larger-capacitance loads or to reduce ringing, add an isolation resistor between the amplifier's output and the load, as shown in Figure 4.

The value of R_{ISO} depends on the circuit's gain and the capacitive load. Figure 5 shows the optional isolation resistor (R_{ISO}) vs. capacitive load (C_L). At the higher capacitor values, the bandwidth is dominated by the RC network, formed by R_{ISO} and C_L.

Power-Dissipation Considerations

The MAX4137/MAX4138 can drive up to four outputs simultaneously. Quiescent power dissipation is typically 520mW and 650mW maximum, respectively, with all channels enabled. The maximum package power dissipation is rated at 1540mW.

In a typical application, four outputs drive a standard video signal into a 150Ω load. The amount of power added to the quiescent dissipation is minimal and no special precautions are necessary.

However, each output driving the maximum 65mA into 30Ω will cause a power-dissipation increase of approximately 200mW. Therefore, you should not allow more than three outputs to deliver that load simultaneously. Similarly, one output shorted to ground will cause a power-dissipation increase of 650mW. Only one output can be shorted to ground without violating the package power rating.

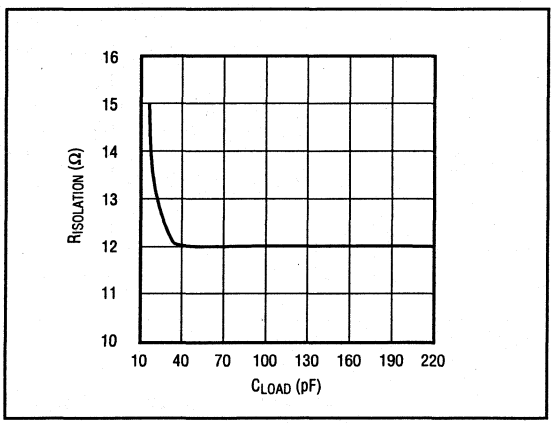


Figure 5. Optimal Isolation Resistor (R_{ISO}) vs. C_{LOAD}

In conclusion, during normal operation in a matched-load environment, the total power dissipation is well within the package's dissipation rating. The maximum power dissipation is violated only if multiple channels are driving the maximum current into minimum loads at the same time.

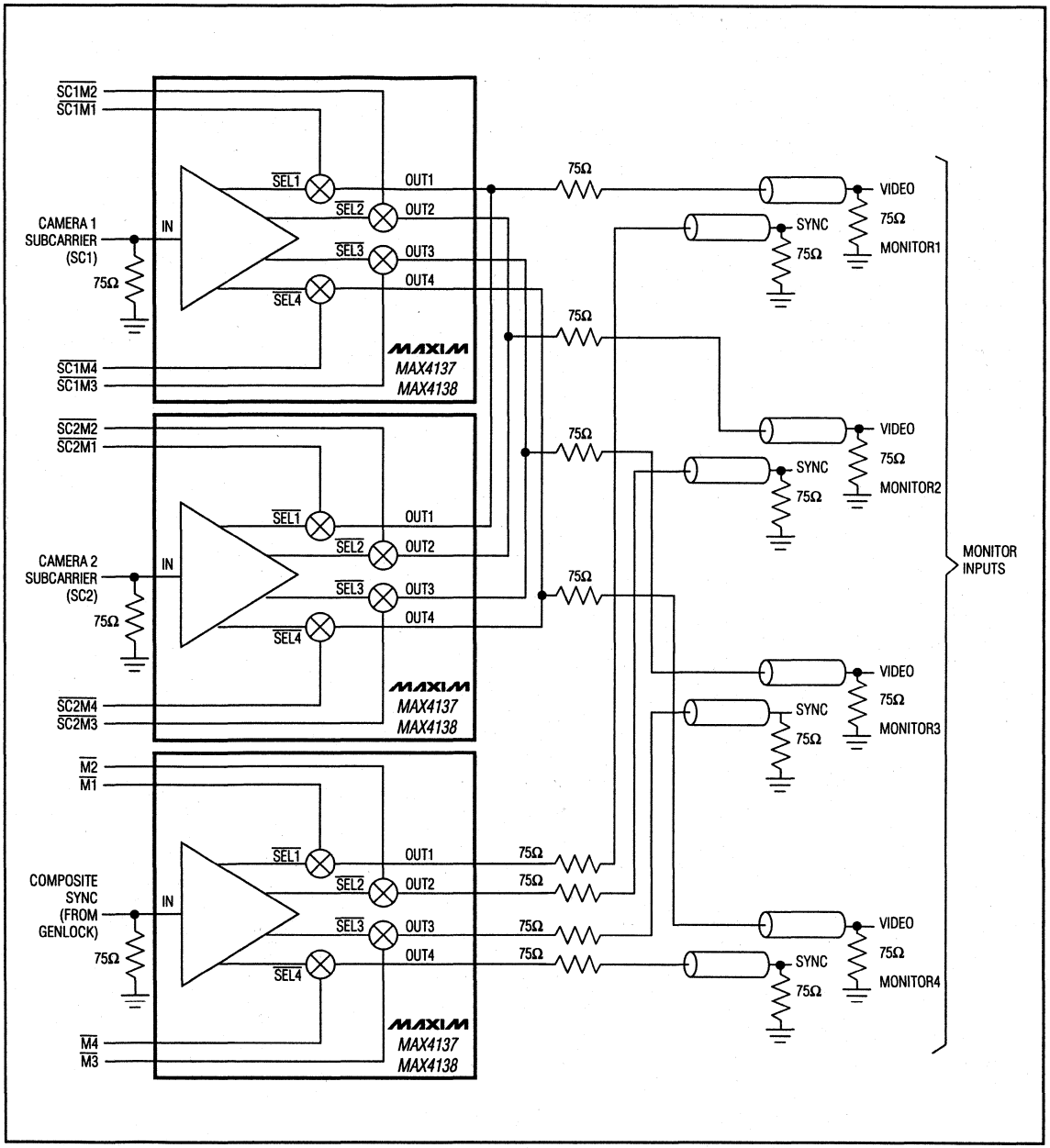


Figure 6. Two Cameras to Four Monitors Distribution Amplifier

1-Input/4-Output Video Distribution Amplifiers

Chip Information

TRANSISTOR COUNT: 625

SUBSTRATE CONNECTED TO V_{EE}

19-1147; Rev 0; 9/96

EVALUATION KIT AVAILABLE

MAXIM

High-Speed Differential Line Receivers

General Description

The MAX4144/MAX4146 differential line receivers offer unparalleled high-speed performance. Utilizing a three-op-amp instrumentation amplifier architecture, these ICs have fully symmetrical differential inputs and a single-ended output. The devices drive ±3.5V into a 150Ω load. The MAX4144 is internally set for a 2V/V closed-loop gain, while the MAX4146 can be externally set to gains from 10V/V to 100V/V.

These amplifiers use laser-trimmed, matched thin-film resistors to deliver a 70dB CMR at 10MHz. Using current-feedback techniques, the MAX4144 achieves a 130MHz bandwidth and 1000V/µs slew rate, while the MAX4146 maintains a 70MHz bandwidth at G = 10V/V and an 800V/µs slew rate. Excellent differential gain/phase and noise specifications make these amplifiers ideal in a variety of video and RF signal-processing applications.

For a complete differential transmission link, use the MAX4144/MAX4146 with the MAX4147 differential line driver (see the MAX4147 data sheet for more information).

Applications

Differential-to-Single-Ended Conversion

Twisted-Pair-to-Coax Converter

High-Speed Instrumentation Amplifier

Data Acquisition

Medical Instrumentation

Features

MAX4144:

- **2V/V Fixed Gain**
- **130MHz Bandwidth**
- **1000V/µs Slew Rate**
- **70dB CMR at 10MHz**
- **-90 dBc SFDR (f_C = 10kHz)**
- **Low Differential Gain/Phase: 0.03%/0.03°**
- **800µA Shutdown**

MAX4146:

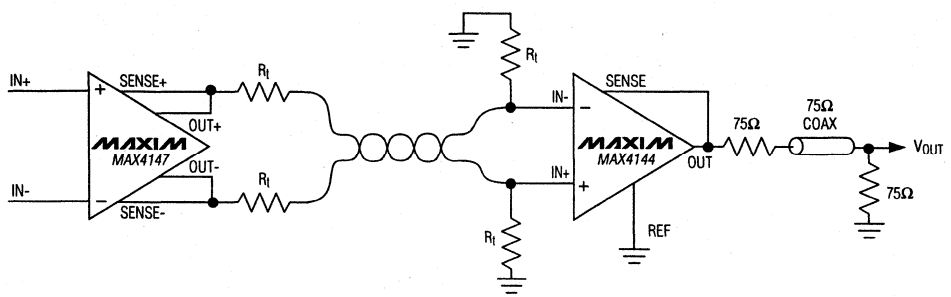
- **External Gain Selection**
- **70MHz Bandwidth (A_V = 10V/V)**
- **800V/µs Slew Rate**
- **90dB CMR at 10MHz**
- **-82dBc SFDR (f_C = 10kHz)**
- **Very Low Noise: 3.5nV/√Hz (G = 100V/V)**
- **800µA Shutdown**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4144ESD	-40°C to +85°C	14 SO
MAX4146ESD	-40°C to +85°C	14 SO

Pin Configurations appear on last page.

Typical Application Circuit



TWISTED-PAIR-TO-COAX CABLE CONVERTER

8

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High-Speed Differential Line Receivers

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to V_{EE}) 12V
Voltage on IN_, SHDN, REF, OUT, SENSE, RG_ ..... (V_{CC} + 0.3V) to (V_{EE} - 0.3V)
Continuous Power Dissipation (T_A = +70°C)
SO (derate 8.33mW/°C above +70°C) 667mW
Short-Circuit Duration to Ground 10sec
Input Current (IN_, RG_) ..... ±10mA
Output Current ..... ±120mA
Operating Temperature Range
MAX414_ESD ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	V_{OUT} = 0V, R_L = ∞				0.6	8	mV
Input Offset Voltage Drift	TCV_{OS}	V_{OUT} = 0V, R_L = ∞				5		µV/°C
Input Bias Current	I_B	V_{OUT} = 0V, R_L = ∞, V_{IN} = -V_{OS}				9	20	µA
Input Offset Current	I_{OS}	V_{OUT} = 0V, R_L = ∞, V_{IN} = -V_{OS}				0.1	2.5	µA
Input Voltage Noise	e_n	f = 1MHz		MAX4144		12		nV/√Hz
				MAX4146		2.1 + (135 / G)		
Input Current Noise	i_n	f = 1MHz				1.7		pA/√Hz
Input Capacitance	C_{IN}					1		pF
Differential Input Resistance						1		MΩ
Differential Input Voltage Range		R_L = 150Ω		MAX4144	-1.55		1.55	V
				MAX4146	-3.1 / G		3.1 / G	
Common-Mode Input Voltage Range	V_{CM}	R_L = ∞			-2.8		2.8	V
Gain	A_V	-1V ≤ V_{OUT} ≤ +1V, R_L = 150Ω		MAX4144		2		V/V
				MAX4146		10 + (14kΩ / R_G)		
Gain Error		-1V ≤ V_{OUT} ≤ +1V, R_L = 150Ω	MAX4144			0.02	2	%
			MAX4146	AV = 10V/V		0.5	2	
				AV = 100V/V		1.5	5	
Gain Drift		-1V ≤ V_{OUT} ≤ +1V, R_L = 150Ω		MAX4144		20		ppm/°C
				MAX4146		14 + 0.9G		
Common-Mode Rejection	CMR	V_C = ±2.8V	0°C ≤ T_A ≤ 85°C		70	80		dB
			-40°C ≤ T_A < 0°C		60			
Power-Supply Rejection	PSR	V_S = ±4.50V to ±5.50V			70	85		dB
Quiescent Supply Current	I_{SY}	R_L = ∞				11	16	mA
Shutdown Supply Current	I_{SHDN}	R_L = ∞				0.8	1	mA
Shutdown Output Impedance		V_{SHDN} ≥ 2.0V		MAX4144		1.4		kΩ
				MAX4146		2.0		
Output Voltage Swing	V_{OUT}	R_L = ∞			±3.4	±3.8		V
		R_L = 150Ω			±3.1	±3.5		
Output Current Drive	I_{OUT}	V_{OUT} = ±1.7V	0°C ≤ T_A ≤ 85°C		80	100		mA
			-40°C ≤ T_A < 0°C		60			

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V, V_{EE} = -5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SHDN High Threshold	V_{IH}				2.0	V
SHDN Low Threshold	V_{IL}		0.8			V
SHDN Input Current (Note 1)	I_{SHDN}	$V_{SHDN} \le 0.8V$		-75	-150	µA
		$V_{SHDN} \ge 2.0V$		±0.06	±2	

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
-3dB Bandwidth	$BW_{(-3dB)}$	$V_{OUT} \le 0.1V_{RMS}$	MAX4144			130		MHz
			MAX4146	A_{VCL} = 10V/V		70		MHz
				A_{VCL} = 100V/V		30		MHz
Full-Power Bandwidth	FPBW	V_{OUT} = 2Vp-p	MAX4144			110		MHz
			MAX4146	A_{VCL} = 10V/V		70		MHz
				A_{VCL} = 100V/V		30		MHz
0.1dB Bandwidth	$BW_{(0.1dB)}$	$V_{OUT} \le 0.1V_{RMS}$		MAX4144		30		MHz
				MAX4146		10		
Common-Mode Rejection	CMR	f = 10MHz		MAX4144		70		dB
				MAX4146		90		
Slew Rate	SR	-2V ≤ V_{OUT} ≤ +2V		MAX4144		1000		V/µs
				MAX4146		800		
Settling Time	t_S	-1V ≤ V_{OUT} ≤ +1V	to 0.1%	MAX4144		23		ns
				MAX4146		17		
			to 0.01%	MAX4144		36		
				MAX4146		40		
Differential Gain	DG	f = 3.58MHz, R_L = 150Ω		MAX4144		0.03		%
				MAX4146		0.12		
Differential Phase	DP	f = 3.58MHz, R_L = 150Ω		MAX4144		0.03		degrees
				MAX4146		0.07		
Spurious-Free Dynamic Range	SFDR	f_C = 10kHz, V_{OUT} = 2Vp-p, R_L = 150Ω	MAX4144	A_V = 2V/V		-90		dBc
			MAX4146	A_V = 10V/V		-82		
		f_C = 5MHz, V_{OUT} = 2Vp-p, R_L = 150Ω	MAX4144	A_V = 2V/V		-66		
			MAX4146	A_V = 10V/V		-48		

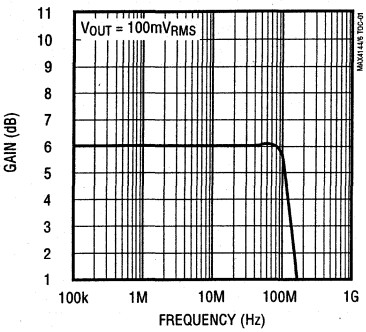
Note 1: The negative sign indicates that current is flowing out of the SHDN pin.
Note 2: Differential gain and phase are tested using a modulated ramp, 100 IRE (0.714V).

High-Speed Differential Line Receivers

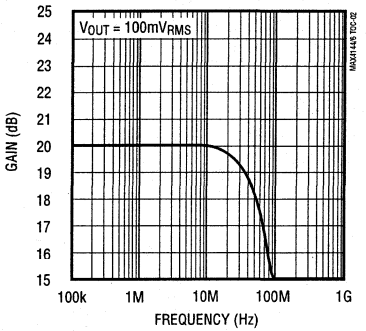
Typical Operating Characteristics

(T_A = +25°C, R_L = 150Ω, unless otherwise noted.)

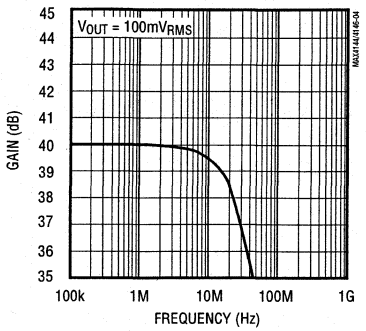
MAX4144
SMALL-SIGNAL GAIN
vs. FREQUENCY (Av = +2)



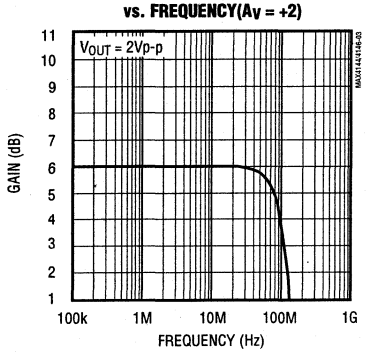
MAX4146
SMALL-SIGNAL GAIN
vs. FREQUENCY (Av = +10)



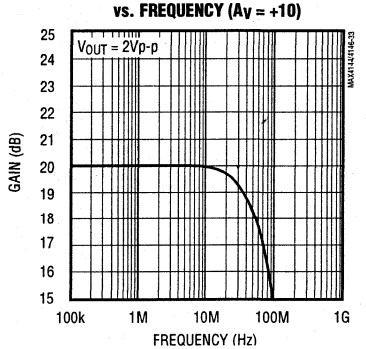
MAX4146
SMALL-SIGNAL GAIN
vs. FREQUENCY (Av = +100)



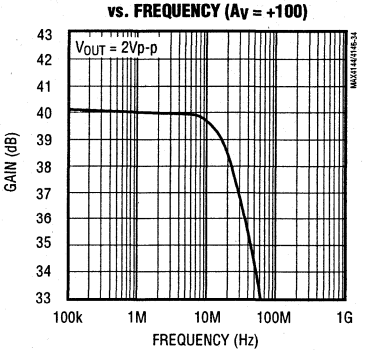
MAX4144
LARGE-SIGNAL GAIN
vs. FREQUENCY(Av = +2)



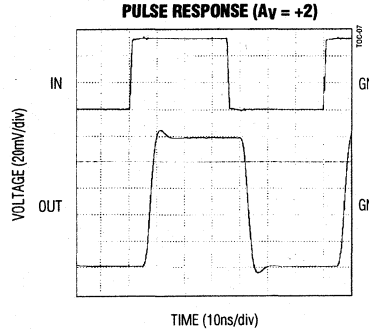
MAX4146
LARGE-SIGNAL GAIN
vs. FREQUENCY (Av = +10)



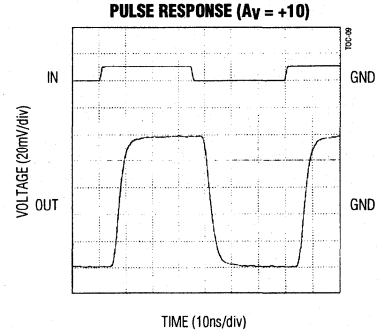
MAX4146
LARGE-SIGNAL GAIN
vs. FREQUENCY (Av = +100)



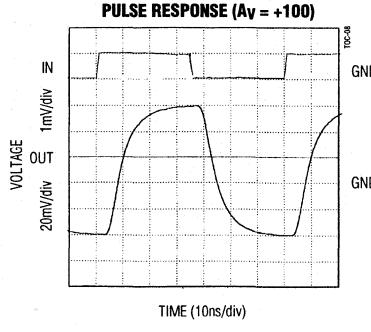
MAX4144
SMALL-SIGNAL
PULSE RESPONSE (Av = +2)



MAX4146
SMALL-SIGNAL
PULSE RESPONSE (Av = +10)



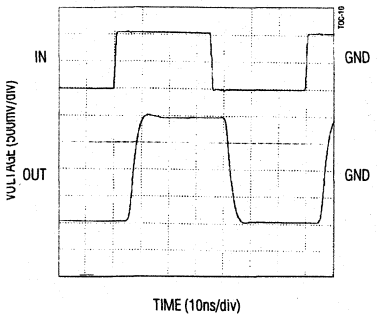
MAX4146
SMALL-SIGNAL
PULSE RESPONSE (Av = +100)



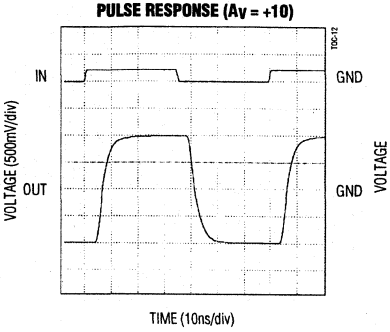
Typical Operating Characteristics (continued)

(T_A = +25°C, R_L = 150Ω, unless otherwise noted.)

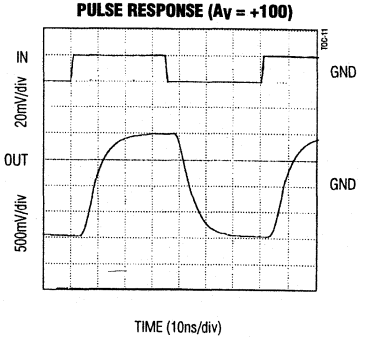
MAX4144 LARGE-SIGNAL PULSE RESPONSE (Av = +2)



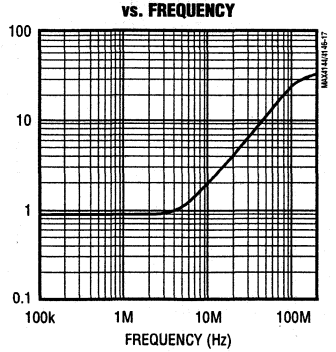
MAX4146 LARGE-SIGNAL PULSE RESPONSE (Av = +10)



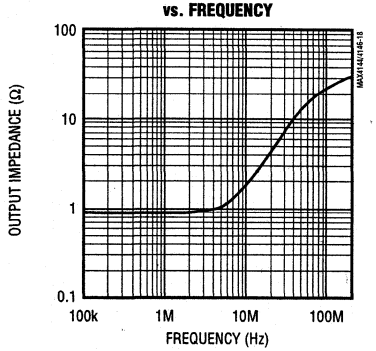
MAX4146 LARGE-SIGNAL PULSE RESPONSE (Av = +100)



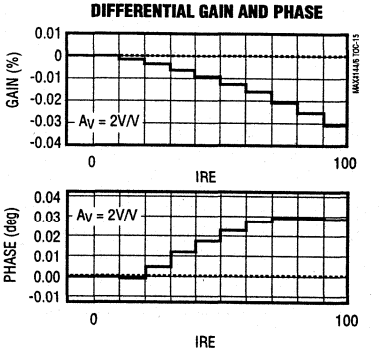
MAX4144 OUTPUT IMPEDANCE vs. FREQUENCY



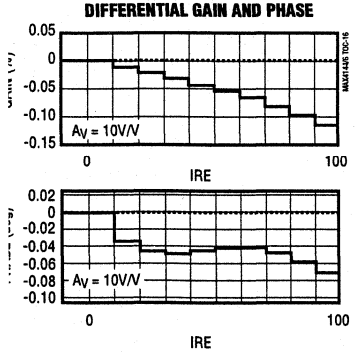
MAX4146 OUTPUT IMPEDANCE vs. FREQUENCY



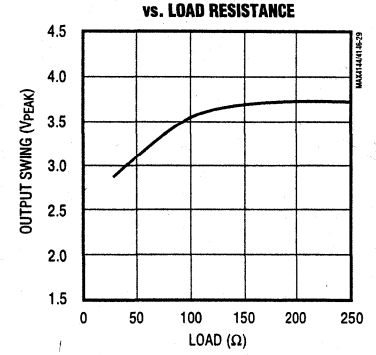
MAX4144 DIFFERENTIAL GAIN AND PHASE



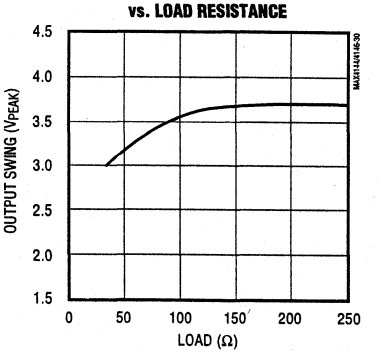
MAX4146 DIFFERENTIAL GAIN AND PHASE



MAX4144 OUTPUT SWING vs. LOAD RESISTANCE



MAX4146 OUTPUT SWING vs. LOAD RESISTANCE



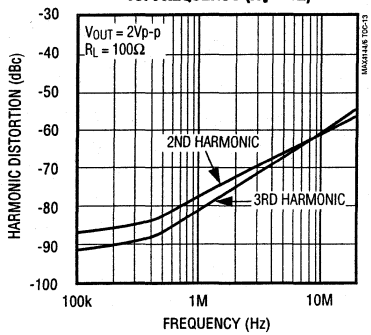
8

High-Speed Differential Line Receivers

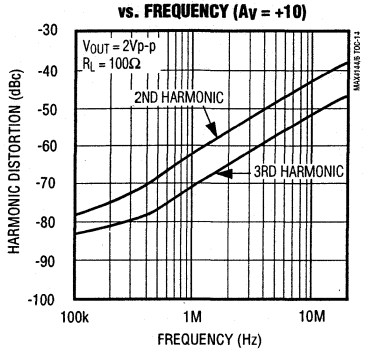
Typical Operating Characteristics (continued)

(T_A = +25°C, R_L = 150Ω, unless otherwise noted.)

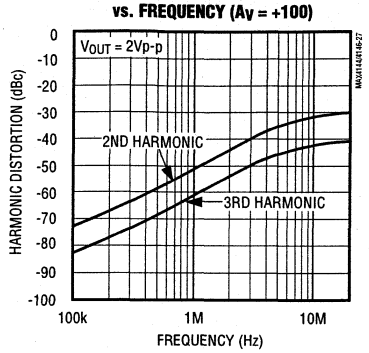
MAX4144
HARMONIC DISTORTION vs. FREQUENCY (A_V = +2)



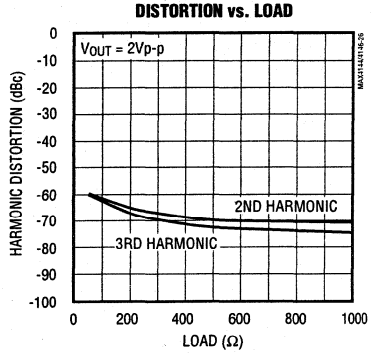
MAX4146
HARMONIC DISTORTION vs. FREQUENCY (A_V = +10)



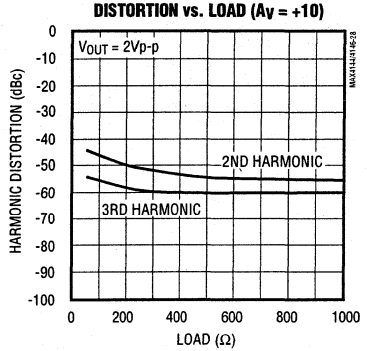
MAX4146
HARMONIC DISTORTION vs. FREQUENCY (A_V = +100)



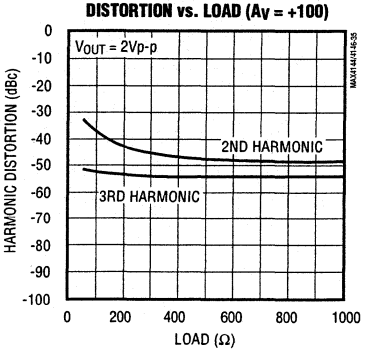
MAX4144
5MHz HARMONIC DISTORTION vs. LOAD



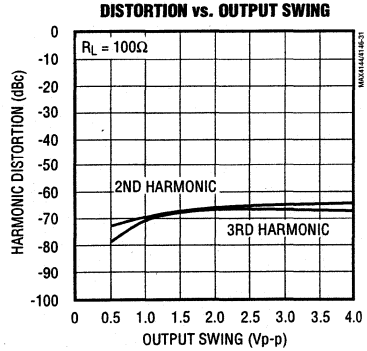
MAX4146
5MHz HARMONIC DISTORTION vs. LOAD (A_V = +10)



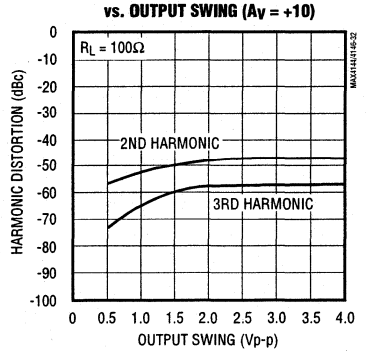
MAX4146
5MHz HARMONIC DISTORTION vs. LOAD (A_V = +100)



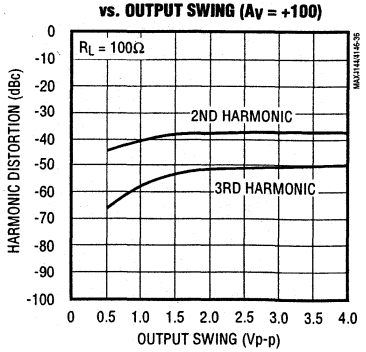
MAX4144
5MHz HARMONIC DISTORTION vs. OUTPUT SWING



MAX4146
5MHz HARMONIC DISTORTION vs. OUTPUT SWING (A_V = +10)



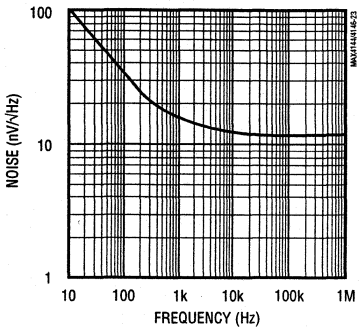
MAX4146
5MHz HARMONIC DISTORTION vs. OUTPUT SWING (A_V = +100)



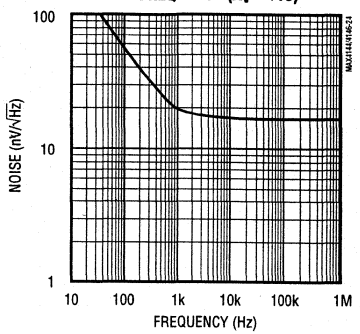
Typical Operating Characteristics (continued)

(T_A = +25°C, R_L = 150Ω, unless otherwise noted.)

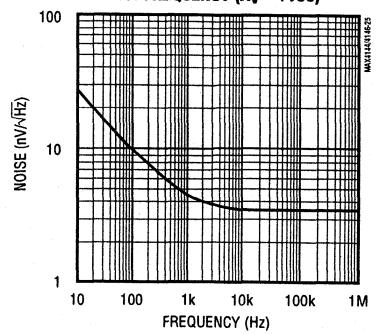
MAX4144
VOLTAGE NOISE
vs. FREQUENCY



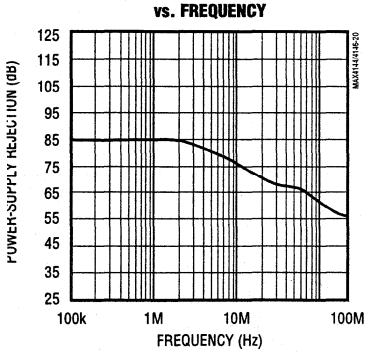
MAX4146
VOLTAGE NOISE
vs. FREQUENCY (Av = +10)



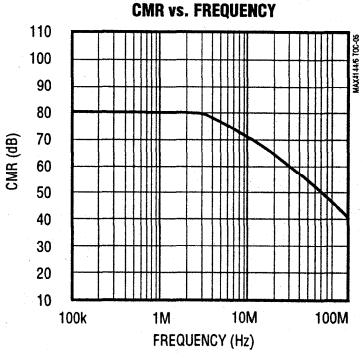
MAX4146
VOLTAGE NOISE
vs. FREQUENCY (Av = +100)



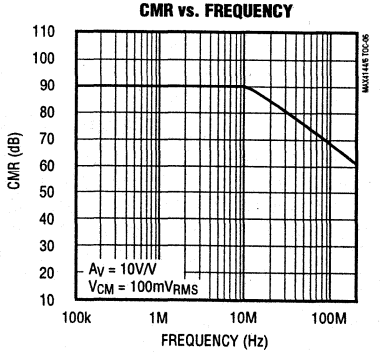
MAX4144 (Av = 2)
MAX4146 (Av = 10)
POWER-SUPPLY REJECTION
vs. FREQUENCY



MAX4144
CMR vs. FREQUENCY



MAX4146
CMR vs. FREQUENCY



High-Speed Differential Line Receivers

Pin Description

PIN		NAME	FUNCTION
MAX4144	MAX4146		
1, 7	1, 7	V_{EE}	Negative Power Supply. Connect to -5V.
2	2	IN-	Inverting Input
3, 5, 10, 12	10, 12	N.C.	No Connect. Not internally connected.
—	3	RG-	Inverting Input for Gain-Set Resistor. A gain-setting resistor (R_G) between RG+ and RG- sets the gain (in V/V) according to the following equation: $G = 10 + \frac{14k\Omega}{R_G}$
4	4	SHDN	Logic Input for Shutdown Circuitry. A logic low enables the amplifier. A logic high disables the amplifier.
—	5	RG+	Non-Inverting Input for Gain-Set Resistor
6	6	IN+	Non-Inverting Input
8, 14	8, 14	V_{CC}	Positive Power Supply. Connect to +5V.
9	9	REF	Output Reference. Connect to ground for normal operation.
11	11	OUT	Output
13	13	SENSE	Output Sense. Connect to OUT close to the pin for normal operation.

Detailed Description

The MAX4144/MAX4146 differential line receivers feature 130MHz and 70MHz (A_V = 10V/V) bandwidth, respectively, and 70dB and 90dB common-mode rejection (CMR) at 10MHz. The parts feature a 1000V/µs slew rate, and power dissipation is a mere 110mW. The MAX4144 is internally set for a 2V/V closed-loop gain, while the MAX4146 can be set to gains from 10V/V to 100V/V using a single resistor. The amplifiers are ideal as line receivers. They have fully symmetrical differential inputs and a single-ended output, and can drive ±3.5V into a 150Ω load.

The differential inputs make the MAX4144/MAX4146 ideal for applications with high common-mode noise such as receiving T1 or XDSL transmissions over a twisted-pair cable. Excellent gain and phase, along with low noise, also suit them to video applications and RF signal processing.

For a complete differential transmission link, use the MAX4144/MAX4146 amplifiers with the MAX4147 line driver, as shown in the *Applications Information* section.

Applications Information

Grounding, Bypassing, and PC Board Layout

High-frequency design techniques must be followed when designing the PC board for the MAX4144/MAX4146.

- The printed circuit board should have at least two layers: the signal layer and the ground plane.
- Do not use wire-wrap boards—they are too inductive.
- Do not use IC sockets—they increase parasitic capacitance and inductance.
- Use surface-mount power-supply bypass capacitors instead of through-hole capacitors. Their shorter lead lengths reduce parasitic inductance, leading to superior high-frequency performance.
- Keep signal lines as short and as straight as possible. Do not make 90° turns; round all corners.
- The ground plane should be as free from voids as possible.

Output Short-Circuit Protection

Under short-circuit conditions to ground, the output current is typically limited to 100mA. This level is low enough that a moderate-duration short to ground will not cause permanent damage to the chip. However, a short to either supply will significantly increase power dissipation, and will cause permanent damage. The high output current capability is an advantage in systems that transmit a signal to several loads.

Input State Circuitry

The MAX4144/MAX4146 include internal protection circuitry that prevents damage to the precision input stage from large differential input voltages. This protection circuitry consists of five back-to-back Schottky protection diodes between IN+ and R_G+, and IN- and R_G- (Figure 1). The diodes limit the differential voltage applied to the amplifiers' internal circuitry to no more than $10V_F$, where V_F is the diode's forward voltage drop (about 0.4V at +25°C).

For a large differential input voltage (exceeding 4V), the MAX4146 input bias current (at IN+ and IN-) increases according to the following equation:

$$\text{Input Current} = \frac{(V_{IN+} - V_{IN-}) - 10V_F}{R_G}$$

The MAX4144 has an internal gain-setting resistor equal to 1.4kΩ. A differential input voltage as high as 10V will cause only 4.3mA to flow—much less than the absolute maximum rating of 10mA. However, in the MAX4146, R_G can be as low as 150Ω. Under this condition, the absolute maximum input current rating might be exceeded if the differential input voltage exceeds 5.5V (10mA x 150Ω + $10V_F$). In that case, 510Ω resistors can be placed at IN+ and IN- to limit the current without degrading performance.

Shutdown Mode

The MAX4144/MAX4146 can be put into low-power shutdown mode by bringing SHDN high. The amplifier output is high impedance in this mode; thus the impedance at OUT is that of the feedback resistors (1.4kΩ and 2kΩ, respectively, for the MAX4144/MAX4146).

Setting Gain (MAX4146)

The MAX4146's gain is determined by a single external resistor, R_G. The minimum gain is 10V/V (R_G = open), and the maximum practical gain is 100V/V. The gain (in V/V) is given in the following equation:

$$G = 10 + \frac{14k\Omega}{R_G}$$

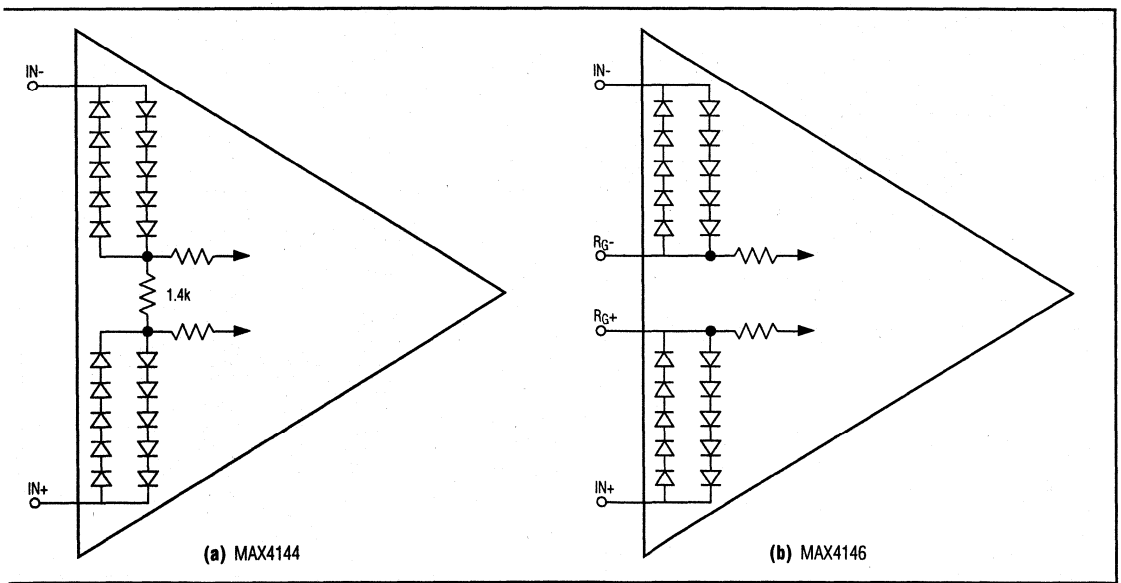


Figure 1. MAX4144/MAX4146 Input Protection Circuit

High-Speed Differential Line Receivers

Figure 2 shows the connection for R_G. R_G might simply be a resistor, or it can be a complex pole-zero pair for filter and shaping applications (Figure 9). Use surface-mount gain-setting components to ensure stability.

Using REF and SENSE

The MAX4144/MAX4146 have a REF pin (normally connected to ground) and a SENSE pin (normally connected to OUT). In some long-line applications, it may be desirable to connect SENSE and OUT together at the load, instead of the typical connection at the part (Figure 3). This compensates for the long line's resistance, which otherwise leads to an IR voltage error.

When using this technique, keep the sense lines' impedance low to minimize gain errors. Also, keep capacitance low to maximize frequency response. The gain of the MAX4144/MAX4146 output stage is approximated by the following equation:

$$A_V = \frac{1}{2}\left[\frac{700\Omega + \Delta R_{SENSE}}{R}\left(1 + \frac{700\Omega + \Delta R_{REF}}{R + 700\Omega + \Delta R_{REF}}\right) + \frac{700\Omega + \Delta R_{REF}}{R + 700\Omega + \Delta R_{REF}}\right]$$

where ΔR_{SENSE} and ΔR_{REF} are the SENSE and REF trace impedances, respectively. R is 700Ω for the MAX4144 and 70Ω for the MAX4146.

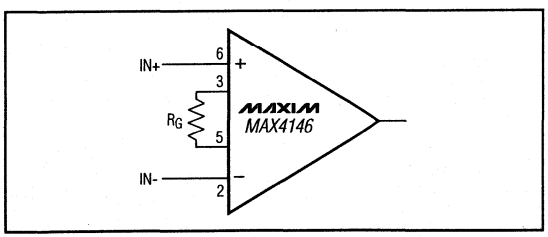


Figure 2. Connection of R_G in MAX4146

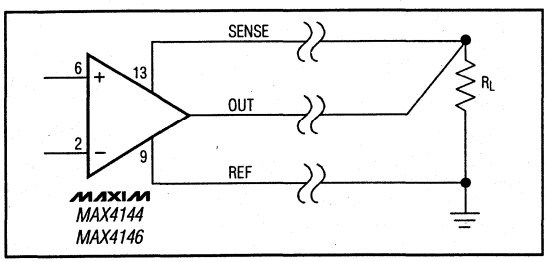


Figure 3. Connection of SENSE and REF to a Remote Load

Additionally, mismatches in the SENSE and REF traces lead to common-mode gain errors. Common-mode gain is approximated by the following equation:

$$AVCM = \frac{\Delta R_{REF} - \Delta R_{SENSE}}{R + 700}$$

Substituting numbers for ΔR_{REF} and ΔR_{SENSE} into this equation, we can see that if changes in ΔR_{REF} and ΔR_{SENSE} are equal, CMR is not degraded.

Driving Capacitive Loads

The MAX4144/MAX4146 provide maximum AC performance when driving no output load capacitance. This is the case when driving a correctly terminated transmission line (i.e., a back-terminated cable).

In most amplifier circuits, driving large load capacitance increases the chance of oscillations. The amplifier's output impedance and the load capacitor combine to add a pole and excess phase to the loop response. If the pole's frequency is low enough and phase margin is degraded sufficiently, oscillations may occur.

A second concern when driving capacitive loads results from the amplifier's output impedance, which looks inductive at high frequencies. This inductance forms an L-C resonant circuit with the capacitive load. This causes peaking in the frequency response and degrades the amplifier's phase margin.

The MAX4144/MAX4146 drive capacitive loads up to 25pF without oscillation. However, some peaking may occur in the frequency domain (Figure 4).

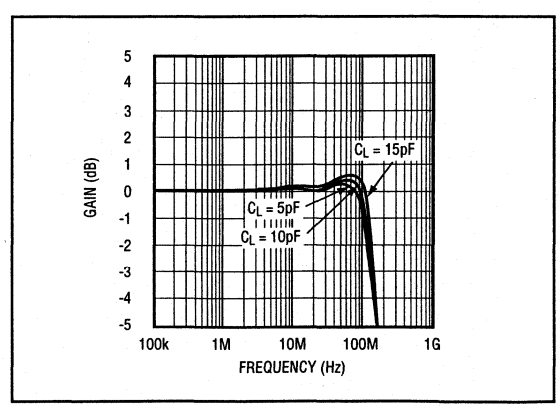


Figure 4. MAX4144 Small-Signal Response with Capacitative Load

To drive larger capacitance loads or to reduce ringing, add an isolation resistor between the amplifier's output and the load (Figure 5).

The value of R_{ISO} depends on the circuit's gain and the capacitive load (Figures 6 and 7). With higher capacitive values, bandwidth is dominated by the RC network formed by R_{ISO} and C_L; the bandwidth of the amplifier itself is much higher. Also note that the isolation resistor forms a divider that decreases the voltage delivered to the load.

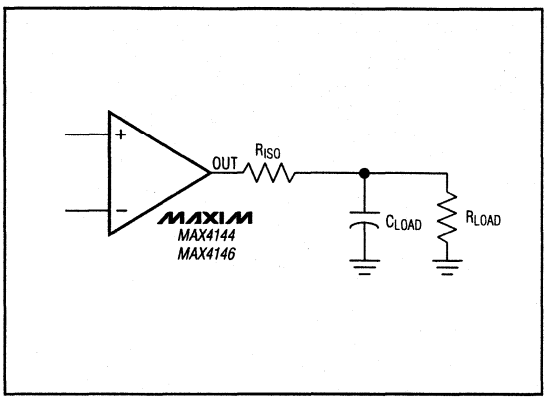


Figure 5. Addition of R_{ISO} to Amplifier Output

Twisted-Pair Line Receiver

The MAX4144/MAX4146 are well suited as receivers in twisted-pair XDSL or NTSC/PAL video applications. The standard 24AWG telephone wire widely used in these applications is a lossy medium for high-frequency signals. The losses in NTSC video applications are almost 15dB per 1,000 feet (Figure 8). Losses are higher at higher frequencies, contributing to severe pulse-edge rounding in digital applications. The nominal impedance of twisted pair telephone wire is 110Ω.

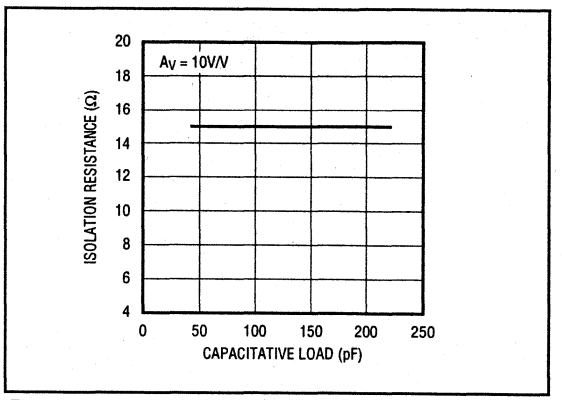


Figure 7. MAX4146 Isolation Resistance vs. Capacitative Load

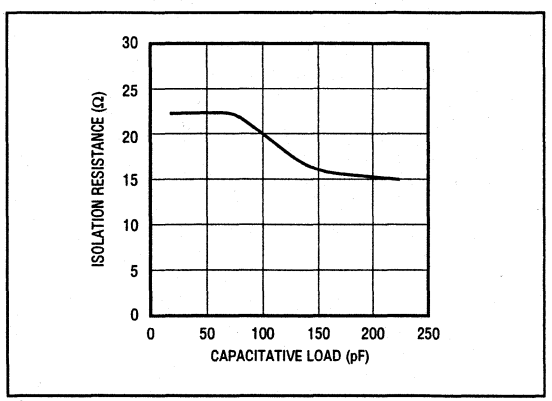


Figure 6. MAX4144 Isolation Resistance vs. Capacitative Load

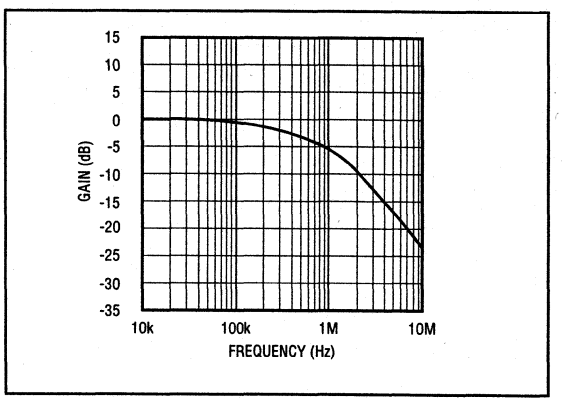


Figure 8. 1000 Feet of AWG24 Twisted-Pair Telephone Cable (Gain vs. Frequency)

High-Speed Differential Line Receivers

The MAX4146, with variable gain up to 100V/V, can be used to compensate for cable losses. In the circuit of Figure 8, the cable characteristics are such that the video-chroma frequency loss is almost 15dB greater than the low-frequency loss. The losses can be compensated for by using the RC-shaping network (Figure 9). A 560Ω resistance and a 100pF capacitance shape the MAX4146 gain to inversely match the frequency of the 1000 feet of telephone cable. The differential gain and phase, using the circuit of Figure 8, is 0.55% and 0.18°, respectively.

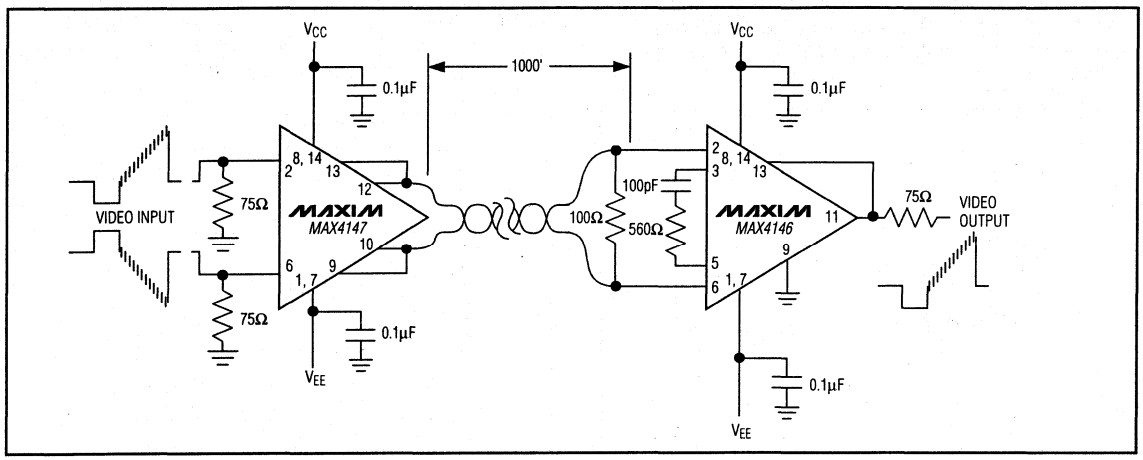
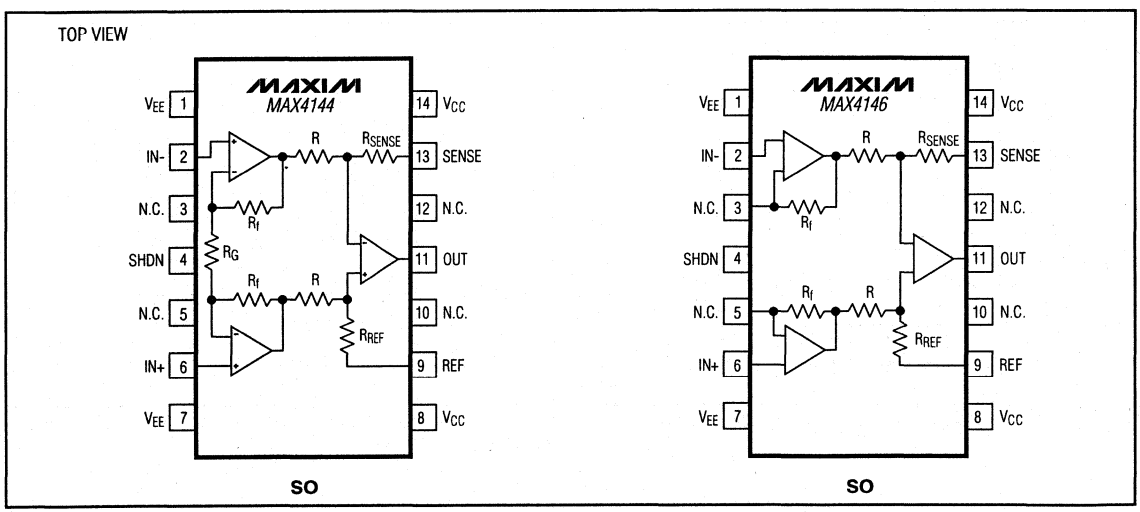


Figure 9. Circuit for Transmitting NTSC/PAL Video Over 1000 Feet of Twisted-Pair Telephone Line

Pin Configurations



19-1106; Rev 0; 8/96

EVALUATION KIT AVAILABLE

MAXIM

300MHz, Low-Power, High-Output-Current, Differential Line Driver

General Description

The MAX4147 differential line driver offers high-speed performance while consuming only 100mW of power. Its amplifier has fully symmetrical inputs and outputs and uses laser-trimmed, matched, thin-film resistors to deliver 70dB CMR at 10MHz. Using current-feedback techniques, the MAX4147 achieves a 300MHz bandwidth and a 2000V/µs slew rate.

Optimized for differential, high-output-current applications such as transformer drivers, the MAX4147 drives ±2.6V into a 26.5Ω load (single-ended) or ±5.6V into a 53Ω load (differential). This device is preset for a closed-loop gain of 2V/V. Its ultra-low 0.008%/0.03° differential gain/phase allow for a variety of video and RF signal-processing applications.

For power-sensitive applications, the MAX4147 has a shutdown function that reduces supply current to less than 1mA. In addition, superior SFDR (-82dBc at 10kHz, R_L = 33Ω) makes it ideal as a transformer driver for HDSL applications.

For a complete differential transmission link, use the MAX4147 with the MAX4144 line receiver (see the MAX4144 data sheet for more information).

Applications

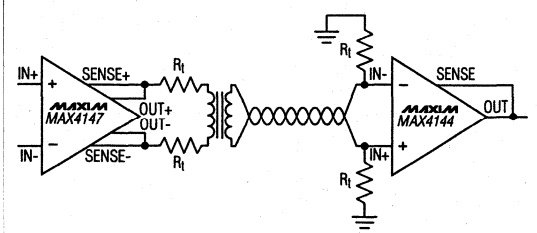
VDSL, ADSL, HDSL

Video Twisted-Pair Driver

Differential Pulse Amplifier

Differential ADC Driver

Typical Application Circuit



VDSL
TRANSFORMER ISOLATION

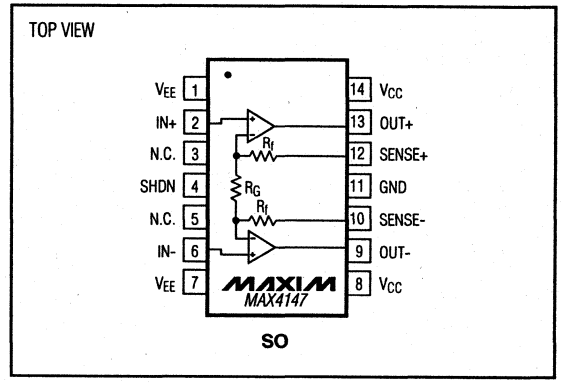
Features

- ♦ 2V/V Fixed Gain
- ♦ 300MHz -3dB Bandwidth
- ♦ 2000V/µs Slew Rate
- ♦ 82dBc SFDR at 10kHz
- ♦ 70dB CMR at 10MHz
- ♦ Low Differential Gain/Phase: 0.008%/0.03°
- ♦ High Output Drive: ±5.6V into 53Ω
- ♦ Low Power: 100mW

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4147ESD	-40°C to +85°C	14 SO

Pin Configuration



SO

8

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

300MHz, Low-Power, High-Output-Current, Differential Line Driver

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to V_{EE}) 12V
Voltage on Any Input to Ground ..... (V_{CC} + 0.3V) to (V_{EE} - 0.3V)
Continuous Power Dissipation (T_A = +70°C)
SO (derate 8.33mW/°C above +70°C) 667mW
Short-Circuit Duration 10sec

Operating Temperature Range
MAX4147ESD ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC SPECIFICATIONS						
Input Offset Voltage	V_{OS}	V_{OUT} = 0V, R_L = ∞		0.5	6	mV
Input Offset Voltage Drift	TCV_{OS}	V_{OUT} = 0V, R_L = ∞		30		µV/°C
Input Bias Current	I_B	V_{OUT} = 0V, R_L = ∞, V_{IN} = -V_{OS}		9	20	µA
Input Offset Current	I_{OS}	V_{OUT} = 0V, R_L = ∞, V_{IN} = -V_{OS}		0.03	2	µA
Input Voltage Noise	e_n	f = 10kHz		8		$nV/\sqrt{Hz}$
		f = 1MHz to 100MHz		80		μV_{RMS}
Input Current Noise	I_n	f = 10kHz		1.7		$pA/\sqrt{Hz}$
		f = 1MHz to 100MHz		17		nA_{RMS}
Input Capacitance	C_{IN}			1		pF
Differential Input Resistance				1		MΩ
Differential Input Voltage Range		R_L = ∞	-3.6		3.6	V
Common-Mode Input Voltage Range	V_{CM}	R_L = ∞	-2.8		2.8	V
Gain	A_V	-1V ≤ V_{OUT} ≤ +1V, R_L = 53Ω		2		V/V
Gain Error		-1V ≤ V_{OUT} ≤ +1V, R_L = 53Ω		0.3	1	%
Common-Mode Rejection	CMR	V_{CM} = ±2.8V	70	100		dB
Power-Supply Rejection	PSR	V_S = ±4.5V to ±5.5V	70	100		dB
Quiescent Supply Current	I_{SY}	V_{IN} = 0, R_L = ∞		10	13	mA
Shutdown Supply Current	I_{SHDN}	V_{IN} = 0, R_L = ∞		0.6	1	mA
Output Voltage Swing	$\lvert V_{OUT} \rvert$	Single-ended, R_L = ∞	3.2	3.8		V
		Differential, R_L = ∞	7.2	7.8		
		Single-ended, R_L = 26.5Ω	2.2	2.6		
		Differential, R_L = 53Ω	5.0	5.6		
Output Current Drive	I_{OUT}	V_{OUT} = ±2.2V	110	160		mA
SHDN High Threshold	V_{IH}				2.0	V
SHDN Low Threshold	V_{IL}		0.8			V
SHDN Input Current	I_{SHDN}	V_{SHDN} = 0V		75	150	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V, V_{EE} = -5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
AC SPECIFICATIONS							
-3dB Bandwidth	$BW_{(-3dB)}$	$V_{OUT} \le 0.1V_{RMS}$			300		MHz
Full-Power Bandwidth	FPBW	V_{OUT} = 2Vp-p			250		MHz
0.1dB Bandwidth	$BW_{(0.1dB)}$	$V_{OUT} \le 0.1V_{RMS}$			70		MHz
Common-Mode Rejection	CMR	f = 10MHz			70		dB
Slew Rate	SR	Differential, -2V ≤ V_{OUT} ≤ +2V			2000		V/µs
Settling Time	t_S	1V ≤ V_{OUT} ≤ +1V, R_L = 150Ω, A_{VCL} = +2	to 0.1%		10		ns
			to 0.01%		30		
Differential Gain	DG	f = 3.58MHz, R_L = 150Ω			0.008		%
Differential Phase	DP	f = 3.58MHz, R_L = 150Ω			0.03		degrees
Spurious-Free Dynamic Range	SFDR	f_C = 10kHz, V_{OUT} = 4.0Vp-p, R_L = 33Ω single-ended, R_S = 50Ω, Figure 1			-82		dBc
		f_C = 5MHz, V_{OUT} = 2Vp-p, R_L = 150Ω differential, Figure 2			-75		

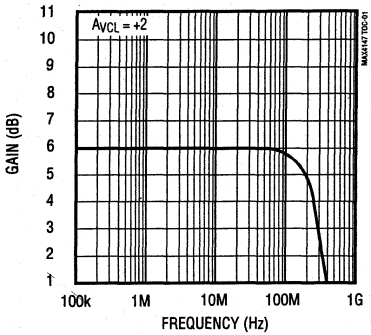
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300MHz, Low-Power, High-Output-Current, Differential Line Driver

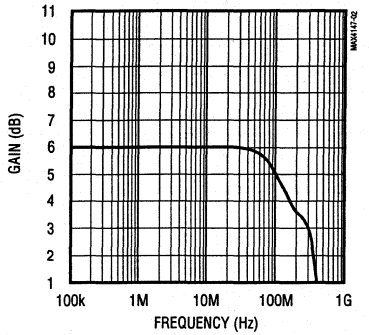
Typical Operating Characteristics

(V_{CC} = +5V, V_{EE} = -5V, R_L = 150Ω, T_A = +25°C, unless otherwise noted.)

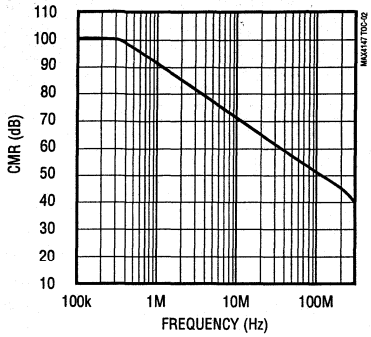
SMALL-SIGNAL GAIN vs. FREQUENCY



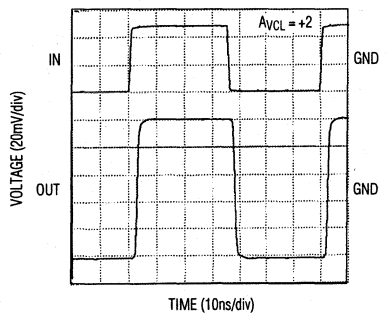
LARGE-SIGNAL GAIN vs. FREQUENCY



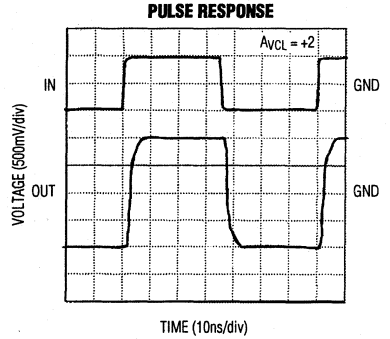
COMMON-MODE REJECTION vs. FREQUENCY



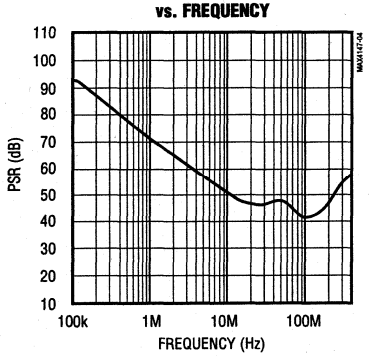
SMALL-SIGNAL PULSE RESPONSE



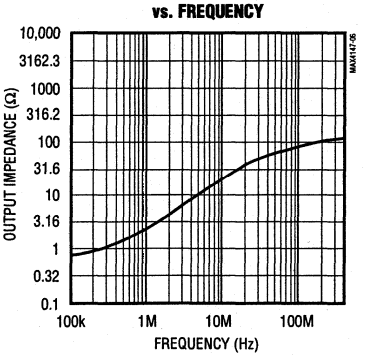
LARGE-SIGNAL PULSE RESPONSE



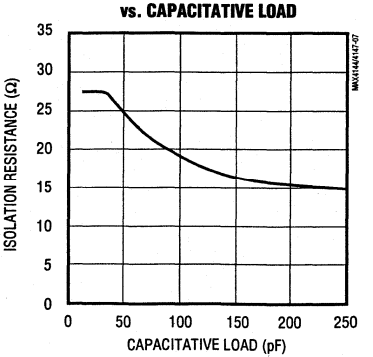
POWER-SUPPLY REJECTION vs. FREQUENCY



CLOSED-LOOP OUTPUT IMPEDANCE vs. FREQUENCY



ISOLATION RESISTANCE vs. CAPACITATIVE LOAD

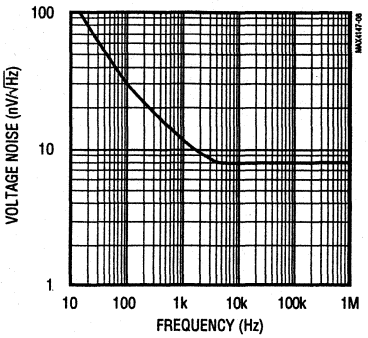


300MHz, Low-Power, High-Output-Current, Differential Line Driver

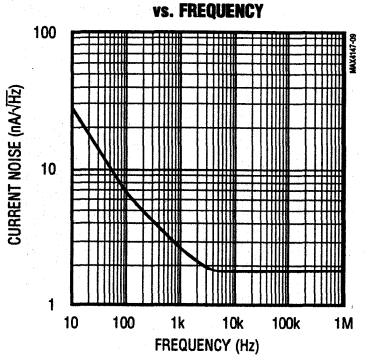
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, R_L = 150Ω, T_A = +25°C, unless otherwise noted.)

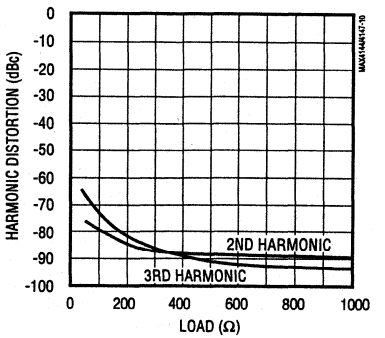
VOLTAGE NOISE vs. FREQUENCY



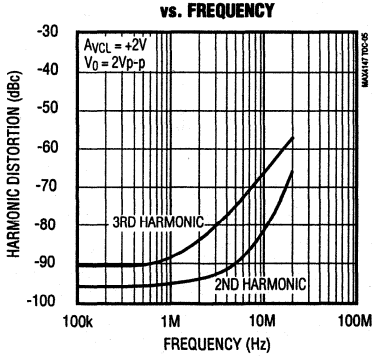
CURRENT NOISE vs. FREQUENCY



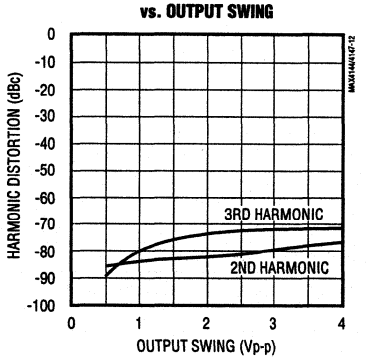
5MHz HARMONIC DISTORTION vs. LOAD



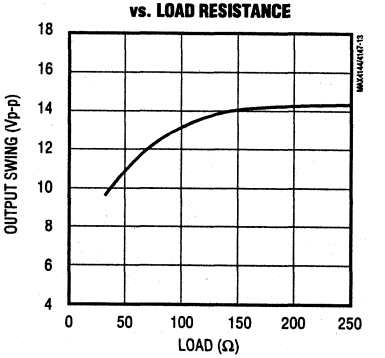
HARMONIC DISTORTION vs. FREQUENCY



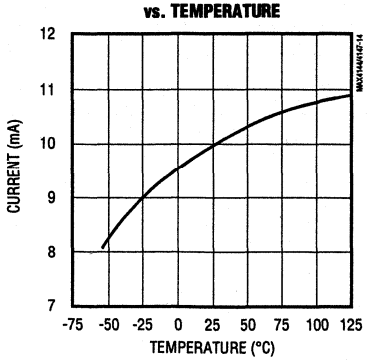
5MHz HARMONIC DISTORTION vs. OUTPUT SWING



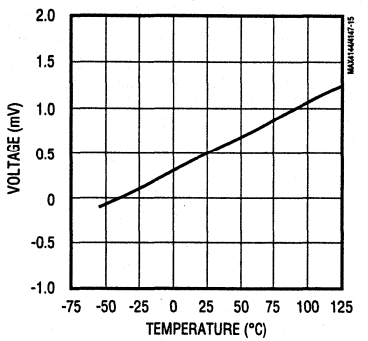
OUTPUT SWING vs. LOAD RESISTANCE



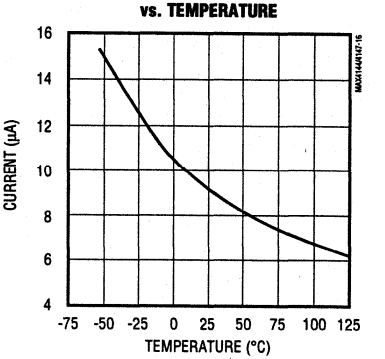
POWER-SUPPLY CURRENT vs. TEMPERATURE



INPUT OFFSET VOLTAGE vs. TEMPERATURE



INPUT BIAS CURRENT vs. TEMPERATURE

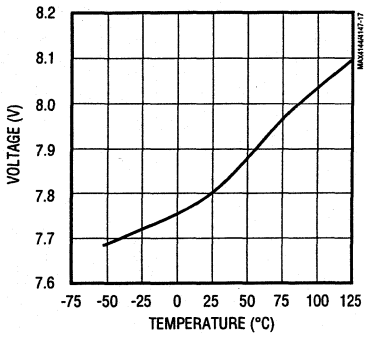


300MHz, Low-Power, High-Output-Current, Differential Line Driver

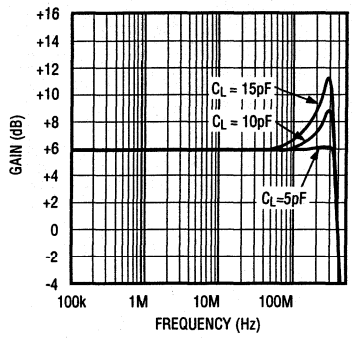
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, R_L = 150Ω, T_A = +25°C, unless otherwise noted.)

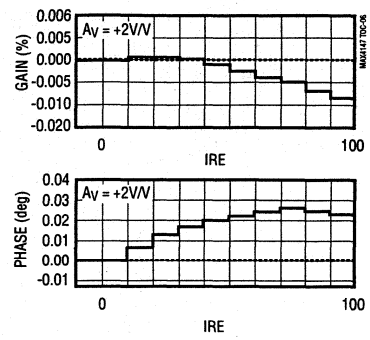
DIFFERENTIAL OUTPUT VOLTAGE SWING vs. TEMPERATURE



SMALL-SIGNAL GAIN vs. FREQUENCY AND CAPACITIVE LOAD



DIFFERENTIAL GAIN AND PHASE



Pin Description

PIN	NAME	FUNCTION
1, 7	V_{EE}	Negative Power Supply. Connect to -5V.
2	IN+	Noninverting Input
3, 5	N.C.	No Connect. Not internally connected.
4	SHDN	Logic Input for Shutdown Circuitry. A logic low enables the amplifier. A logic high disables the amplifier.
6	IN-	Inverting Input
8, 14	V_{CC}	Positive Power Supply
9	OUT-	Inverting Output
10	SENSE-	Sense Line for the Inverting Output. Connect to OUT-, close to the pin.
11	GND	Ground
12	SENSE+	Sense Line for the Noninverting Output. Connect to OUT+, close to the pin.
13	OUT+	Noninverting Output

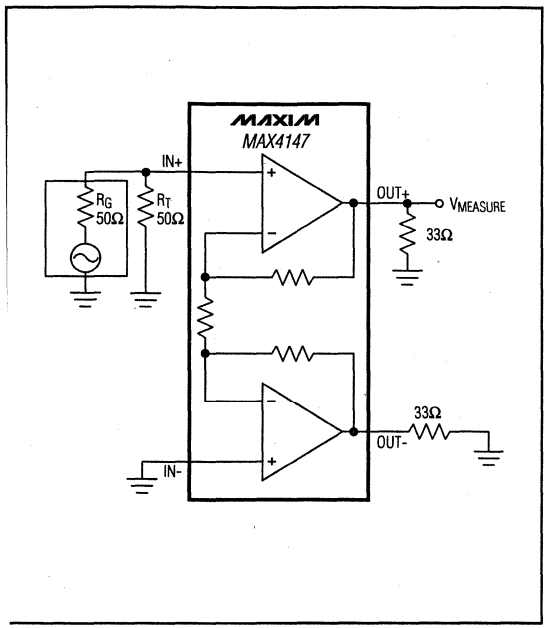


Figure 1. Single-Ended Distortion Setup

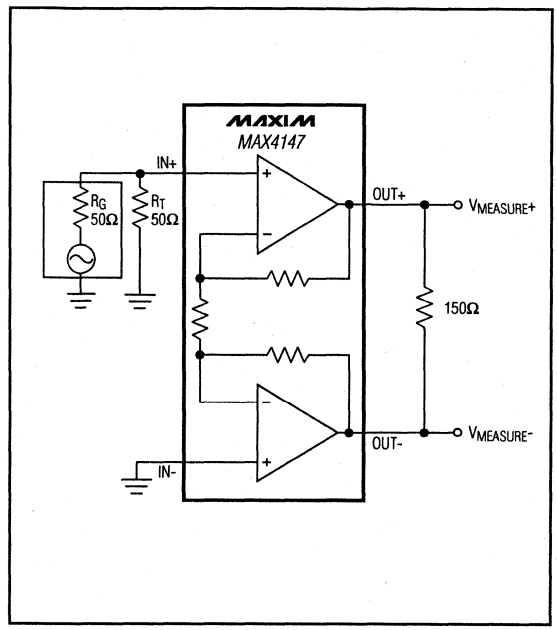


Figure 2. Differential Distortion Setup

ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
11/96

MAXIM

350MHz/250MHz, 2-Channel Video Multiplexer-Amplifiers

General Description

The MAX4158/MAX4159/MAX4258/MAX4259 are wideband, 2-channel, noninverting video amplifiers with input multiplexing, capable of driving ±2.5V signals into 50Ω or 75Ω loads. These devices are current-mode feedback amplifiers; gain is set by external feedback resistors. The MAX4158/MAX4159 are optimized for unity gain (0dB) with a -3dB bandwidth of 350MHz. The MAX4258/MAX4259 are optimized for gains of two (6dB) or more with a 250MHz -3dB bandwidth. All four devices have low (0.02%/0.02°) differential gain and phase errors and operate from ±5V supplies.

These devices are ideal for use in broadcast and graphics video systems because of their low, 2pF input capacitance, channel-to-channel switching time of only 20ns, and wide, 100MHz 0.1dB bandwidth. In addition, the combination of ultra-high speed and low power makes them suitable for use in general-purpose high-speed applications, such as medical imaging, industrial instrumentation, and communications systems.

The MAX4159/MAX4259 have address latching and high-impedance output disabling, allowing them to be incorporated into large switching arrays. They are available in 14-pin SO and 16-pin QSOP packages. The MAX4158/MAX4258 have no address latching or output disabling, but are available in space-saving 8-pin µMAX and SO packages.

Applications

Video-Signal Multiplexing
Video Crosspoint Switches
Pixel Switching
Coaxial Cable Drivers
Workstations
High-Definition TV (HDTV)
Broadcast Video
Multimedia Products
High-Speed Signal Processing

Features

- **Excellent Video Specifications:**
  0.1dB Gain Flatness to 100MHz
  0.02%/0.02° Differential Gain/Phase Error
- **High Speed:**
  350MHz -3dB Bandwidth (Av = 0dB, MAX4158/4159)
  250MHz -3dB Bandwidth (Av = 6dB, MAX4258/4259)
  155MHz Full-Power Bandwidth (Av = 0dB, MAX4158/4159)
  200MHz Full-Power Bandwidth (Av = 6dB, MAX4258/4259)
  700V/µs Slew Rate (MAX4158/4159)
  1000V/µs Slew Rate (MAX4258/4259)
  20ns Settling Time to 0.1%
- **Fast Switching:**
  20ns Channel-Switching Time
  <120mVp-p Switching Transient
- **Low Power: 100mW**
- **Directly Drives 75Ω or 50Ω Cables**
- **High Output Current Drive: >70mA**
- **Address Latch and High-Z Output Disable (MAX4159/4259)**
- **2pF On/Off Input Capacitance**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4158EUA	-40°C to +85°C	8 µMAX
MAX4158ESA	-40°C to +85°C	8 SO
MAX4159EEE	-40°C to +85°C	16 QSOP
MAX4159ESD	-40°C to +85°C	14 SO
MAX4258EUA	-40°C to +85°C	8 µMAX
MAX4258ESA	-40°C to +85°C	8 SO
MAX4259EEE	-40°C to +85°C	16 QSOP
MAX4259ESD	-40°C to +85°C	14 SO

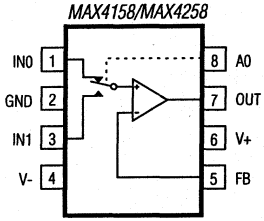
For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

350MHz/250MHz, 2-Channel Video Multiplexer-Amplifiers

Pin Configurations/Functional Diagrams/Truth Tables

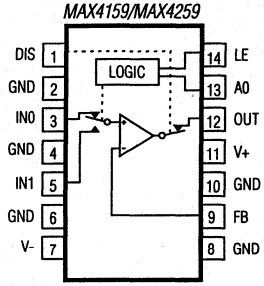
TOP VIEW

MAXIM
MAX4158/MAX4258



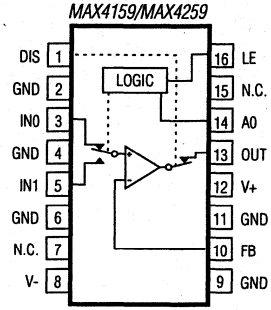
SO/μMAX

MAXIM
MAX4159/MAX4259



SO

MAXIM
MAX4159/MAX4259



QSOP

MAX4158/MAX4258	
A0	INPUT
0	IN0
1	IN1

X = DON'T CARE

MAX4159/MAX4259		
LE	A0	INPUT
0	0	IN0
0	1	IN1
1	X	LAST

N.C. = NOT INTERNALLY CONNECTED

MAX4159/MAX4259	
DIS	OUTPUT
0	ON
1	OFF (HI-Z)

ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
10/96

MAXIM

330MHz, Gain of +1/Gain of +2 Closed-Loop Buffers

General Description

The MAX4177/MAX4277 are ±5V, wide-bandwidth, fast-settling, closed-loop buffers featuring high slew rate, high precision, high output current, low noise, and low differential gain and phase errors. The MAX4177, with a -3dB bandwidth of 330MHz, is preset for unity voltage gain (0dB). The MAX4277 is preset for a voltage gain of +2 (6dB) and has a 310MHz -3dB bandwidth.

The MAX4177/MAX4277 feature the high slew rate and low power that are characteristic of current-mode feedback amplifiers. However, unlike conventional current-mode feedback amplifiers, these devices have a unique input stage that combines the benefits of current-feedback topology with those of the traditional voltage-feedback topology. This combination results in low input offset voltage and bias current, low noise, and high gain precision and power-supply rejection.

The MAX4177/MAX4277 are ideally suited for driving 50Ω or 75Ω loads. They are the perfect choice for high-speed cable-driving applications, such as video routing. The devices also feature a shutdown mode that can be used to conserve power and to disable the output for multiplexer applications. The MAX4177/MAX4277 are available in 8-pin DIP, SO, and µMAX packages.

Applications

Broadcast and High-Definition TV Systems
Video Switching and Routing
High-Speed Cable Drivers
Communications
Medical Imaging
Precision High-Speed DAC/ADC Buffers

Features

- **High Speed:**
  330MHz -3dB Bandwidth (MAX4177)
  310MHz -3dB Bandwidth (MAX4277)
  250MHz Full-Power Bandwidth (V_{OUT} = 2Vp-p)
  150MHz 0.1dB Flatness Bandwidth
  1300V/µs Slew Rate (MAX4177)
  1600V/µs Slew Rate (MAX4277)
- **Low Differential Phase/Gain Error: 0.01°/0.04%**
- **8mA Supply Current**
- **1µA Input Bias Current**
- **0.5mV Input Offset Voltage**
- **5nV/√Hz Input-Referred Voltage Noise**
- **2pA/√Hz Input-Referred Current Noise**
- **1.0% Max Gain Error with 100Ω Load**
- **90dB PSRR**
- **Short-Circuit Protected**
- **High-Z Output in Shutdown Mode**
- **Available in µMAX Package**

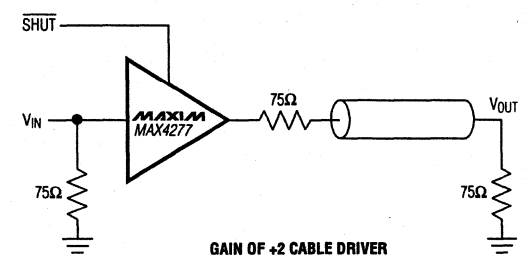
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4177EPA	-40°C to +85°C	8 Plastic DIP
MAX4177ESA	-40°C to +85°C	8 SO
MAX4177EUA	-40°C to +85°C	8 µMAX
MAX4177MJA	-55°C to +125°C	8 CERDIP

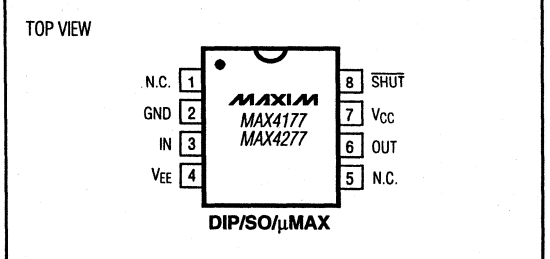
Ordering Information continued on next page.

8

Typical Operating Circuit



Pin Configuration



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330MHz, Gain of +1/Gain of +2 Closed-Loop Buffers

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX4277EPA	-40°C to +85°C	8 Plastic DIP
MAX4277ESA	-40°C to +85°C	8 SO
MAX4277EUA	-40°C to +85°C	8 µMAX
MAX4277MJA	-55°C to +125°C	8 CERDIP

19-0468; Rev 0; 2/96

EVALUATION KIT AVAILABLE

MAXIM

330MHz, Gain of +1/Gain of +2 Closed-Loop Buffers

General Description

The MAX4178/MAX4278 are ±5V, wide-bandwidth, fast-settling, closed-loop buffers featuring high slew rate, high precision, high output current, low noise, and low differential gain and phase errors. The MAX4178, with a -3dB bandwidth of 330MHz, is preset for unity voltage gain (0dB). The MAX4278 is preset for a voltage gain of +2 (6dB) and has a 310MHz -3dB bandwidth.

The MAX4178/MAX4278 feature the high slew rate and low power that are characteristic of current-mode feedback amplifiers. However, unlike conventional current-mode feedback amplifiers, these devices have a unique input stage that combines the benefits of current-feedback topology with those of the traditional voltage-feedback topology. This combination results in low input offset voltage and bias current, low noise, and high gain precision and power-supply rejection.

The MAX4178/MAX4278 are ideally suited for driving 50Ω or 75Ω loads. They are the perfect choice for high-speed cable-driving applications, such as video routing. The MAX4178/MAX4278 are available in 8-pin DIP, SO, and µMAX packages.

Applications

Broadcast and High-Definition TV Systems
Video Switching and Routing
High-Speed Cable Drivers
Communications
Medical Imaging
Precision High-Speed DAC/ADC Buffers

Features

- **High Speed:**
  - **330MHz -3dB Bandwidth (MAX4178)**
  - **310MHz -3dB Bandwidth (MAX4278)**
  - **250MHz Full-Power Bandwidth (V_{OUT} = 2Vp-p)**
  - **150MHz 0.1dB Flatness Bandwidth**
  - **1300V/µs Slew Rate (MAX4178)**
  - **1600V/µs Slew Rate (MAX4278)**
- **Low Differential Phase/Gain Error: 0.01°/0.04%**
- **8mA Supply Current**
- **1µA Input Bias Current**
- **0.5mV Input Offset Voltage**
- **5nV/√Hz Input-Referred Voltage Noise**
- **2pA/√Hz Input-Referred Current Noise**
- **1.0% Max Gain Error with 100Ω Load**
- **90dB PSRR**
- **Short-Circuit Protected**
- **8000V ESD Protection**

Ordering Information

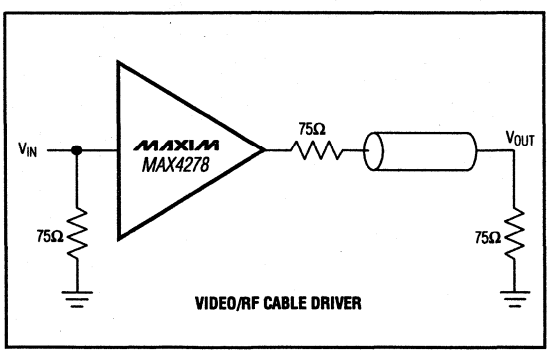
PART	TEMP. RANGE	PIN-PACKAGE
MAX4178EPA	-40°C to +85°C	8 Plastic DIP
MAX4178ESA	-40°C to +85°C	8 SO
MAX4178EUA	-40°C to +85°C	8 µMAX*
MAX4178MJA	-55°C to +125°C	8 CERDIP

Ordering Information continued at end of data sheet.

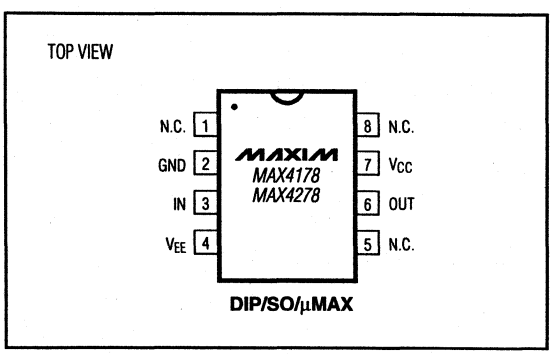
** Contact factory for availability.*

8

Typical Operating Circuit



Pin Configuration



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

330MHz, Gain of +1/Gain of +2 Closed-Loop Buffers

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to V_{EE}) 13V
Input Voltage ..... (V_{CC} + 0.3V) to (V_{EE} - 0.3V)
Output Short-Circuit Duration (to GND) ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C) 471mW
µMAX (derate 4.10mW/°C above +70°C) 330mW
CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges
MAX4178E_A/MAX4278E_A ..... -40°C to +85°C
MAX4178MJA/MAX4278MJA ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, V_{OUT} = 0V, R_L = ∞, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}	MAX4178		±2.5	±3.0		V
		MAX4278		±1.25	±1.5		
Input Offset Voltage	V_{OS}	T_A = +25°C			0.5	2.0	mV
		T_A = T_{MIN} to T_{MAX}				3.0	
Input Offset Voltage Drift	TCV_{OS}				2		µV/°C
Input Bias Current	I_B	T_A = +25°C			1	3	µA
		T_A = T_{MIN} to T_{MAX}				5	
Input Resistance	R_{IN}				1		MΩ
Power-Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±5.5V		70	90		dB
Voltage Gain	A_V	MAX4178 (Note 1)	R_L = 100Ω	0.990		1.000	V/V
			R_L = 50Ω	0.985		1.000	
		MAX4278 (Note 2)	R_L = 100Ω	1.98		2.01	
			R_L = 50Ω	1.97		2.01	
Gain Linearity	$A_{V(LIN)}$	V_{OUT} = ±1mV to ±2V			0.01		%
Output Resistance	R_{OUT}	f = DC			0.1		Ω
Minimum Output Current	I_{OUT}	T_A = -40°C to +85°C		70	100		mA
Short-Circuit Output Current	I_{SC}	Short to GND			150		mA
Output Voltage Swing	V_{OUT}	R_L = 100Ω		±2.5	±3.0		V
		R_L = 50Ω		±2.0	±2.5		
Quiescent Supply Current	I_{SY}	T_A = +25°C			8	10	mA
		T_A = T_{MIN} to T_{MAX}	MAX4_78E_A			12	
			MAX4_78MJA			14	

Note 1: Voltage Gain = (V_{OUT} - V_{OS}) / V_{IN} measured at V_{IN} = ±2.5V.
Note 2: Voltage Gain = (V_{OUT} - V_{OS}) / V_{IN} measured at V_{IN} = ±1.25V.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Small-Signal, -3dB Bandwidth	BW	V_{OUT} ≤ 0.1Vp-p	MAX4178ESA	260	330		MHz
			MAX4178EPA/EUA/MJA		330		
			MAX4278ESA	240	310		
			MAX4278EPA/EUA/MJA		310		
Small-Signal, ±0.1dB Bandwidth	$BW_{(0.1dB)}$	V_{OUT} ≤ 0.1Vp-p	MAX4178ESA	50	150		MHz
			MAX4178EPA/EUA/MJA		150		
			MAX4278ESA	50	150		
			MAX4278EPA/EUA/MJA		150		
Full-Power Bandwidth	FPBW	V_{OUT} = 2Vp-p	MAX4178		250		MHz
			MAX4278		250		
Slew Rate	SR	V_{OUT} = ±2V	MAX4178ESA	1000	1300		V/µs
			MAX4178EPA/EUA/MJA		1300		
			MAX4278ESA	1000	1600		
			MAX4278EPA/EUA/MJA		1600		
Settling Time	t_S	V_{OUT} = 2V step	to 0.1%		10		ns
			to 0.01%		12		
Rise/Fall Times	t_R, t_F	V_{OUT} = 2V step			2		ns
Input Capacitance	C_{IN}				1		pF
Input Voltage Noise Density	e_n	f = 10MHz			5		nV/√Hz
Input Current Noise Density	i_n	f = 10MHz			2		pA/√Hz
Differential Gain (Note 3)	DG	f = 3.58MHz	MAX4178		0.04		%
			MAX4278		0.04		
Differential Phase (Note 3)	DP	f = 3.58MHz	MAX4178		0.01		degrees
			MAX4278		0.01		
Total Harmonic Distortion	THD	f_C = 10MHz, V_{OUT} = 2Vp-p	MAX4178		-58		dB
			MAX4278		-59		
Spurious-Free Dynamic Range	SFDR	f = 5MHz, V_{OUT} = 2Vp-p	MAX4178		-81		dBC
			MAX4278		-74		
Third-Order Intercept	IP3	f_C = 10MHz, V_{OUT} = 2Vp-p	MAX4178		36		dBm
			MAX4278		31		

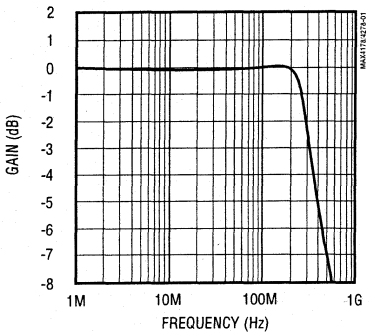
Note 3: Tested with a 3.58MHz video test signal with an amplitude of 40IRE superimposed on a linear ramp (0 to 100IRE). An IRE is a unit of video signal amplitude developed by the Institute of Radio Engineers. 140IRE = 1V in color systems.

330MHz, Gain of +1/Gain of +2 Closed-Loop Buffers

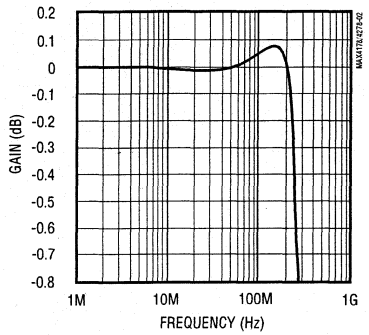
Typical Operating Characteristics

(V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, C_L = 0pF, T_A = +25°C, unless otherwise noted.)

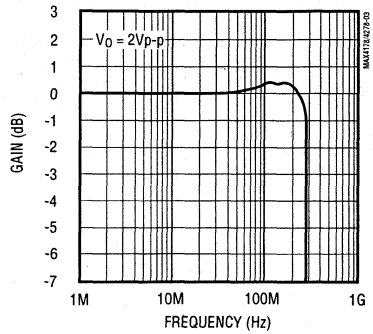
MAX4178 SMALL-SIGNAL GAIN vs. FREQUENCY



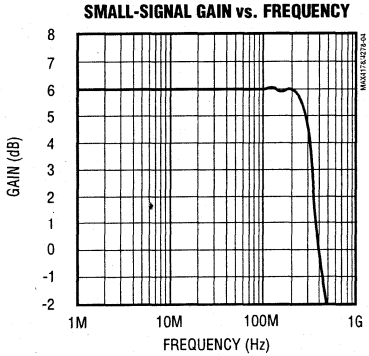
MAX4178 GAIN FLATNESS vs. FREQUENCY



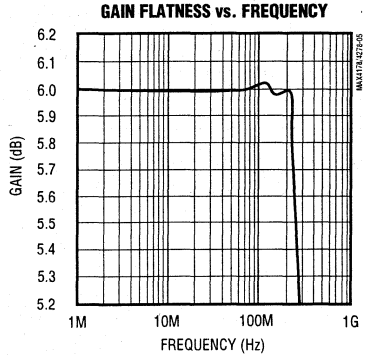
MAX4178 LARGE-SIGNAL GAIN vs. FREQUENCY



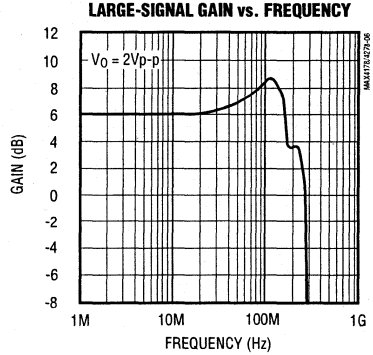
MAX4278 SMALL-SIGNAL GAIN vs. FREQUENCY



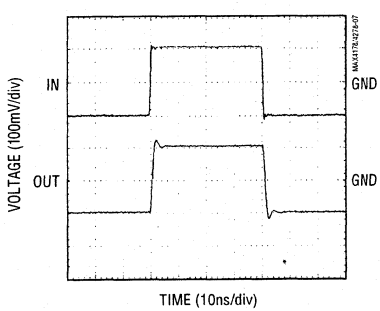
MAX4278 GAIN FLATNESS vs. FREQUENCY



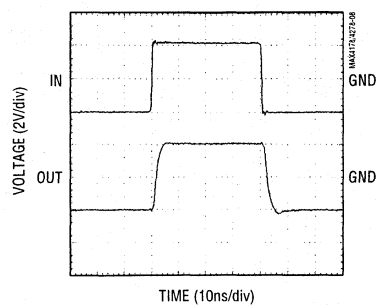
MAX4278 LARGE-SIGNAL GAIN vs. FREQUENCY



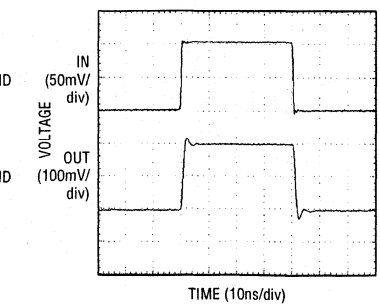
MAX4178 SMALL-SIGNAL PULSE RESPONSE (C_L = 0pF)



MAX4178 LARGE-SIGNAL PULSE RESPONSE (C_L = 0pF)



MAX4278 SMALL-SIGNAL PULSE RESPONSE (C_L = 0pF)

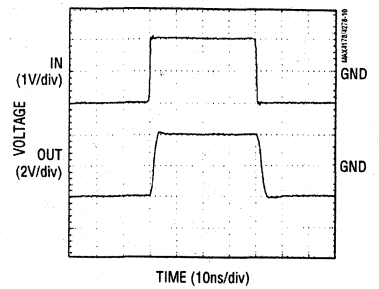


330MHz, Gain of +1/Gain of +2 Closed-Loop Buffers

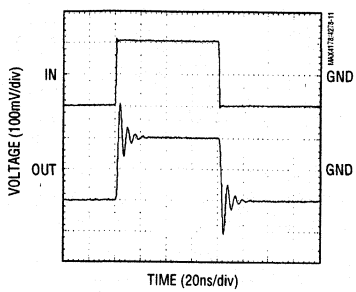
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, C_L = 0pF, T_A = +25°C, unless otherwise noted.)

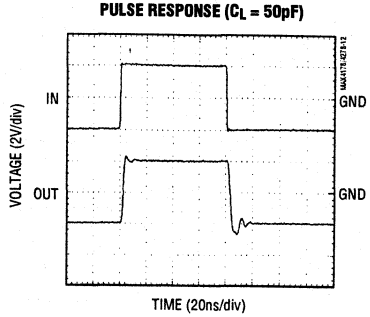
MAX4278 LARGE-SIGNAL PULSE RESPONSE (C_L = 0pF)



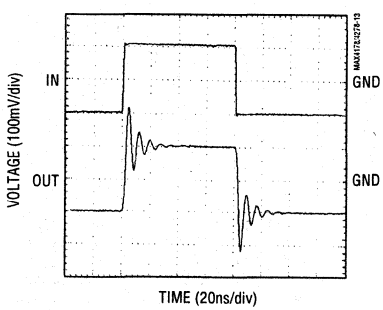
MAX4178 SMALL-SIGNAL PULSE RESPONSE (C_L = 50pF)



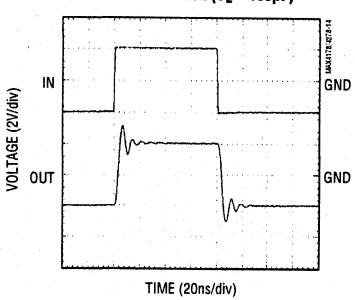
MAX4178 LARGE-SIGNAL PULSE RESPONSE (C_L = 50pF)



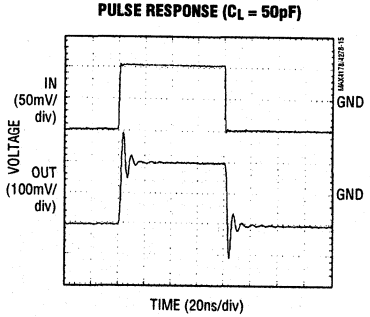
MAX4178 SMALL-SIGNAL PULSE RESPONSE (C_L = 100pF)



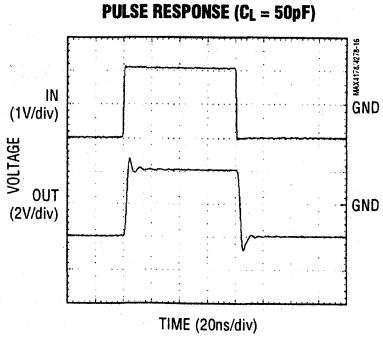
MAX4178 LARGE-SIGNAL PULSE RESPONSE (C_L = 100pF)



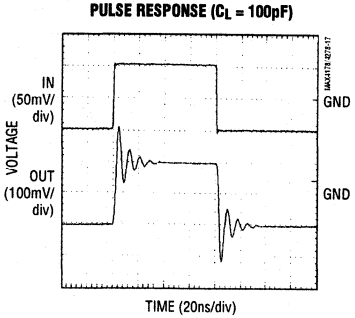
MAX4278 SMALL-SIGNAL PULSE RESPONSE (C_L = 50pF)



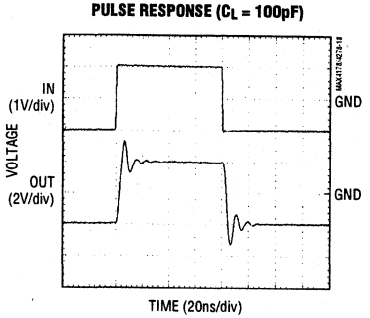
MAX4278 LARGE-SIGNAL PULSE RESPONSE (C_L = 50pF)



MAX4278 SMALL-SIGNAL PULSE RESPONSE (C_L = 100pF)



MAX4278 LARGE-SIGNAL PULSE RESPONSE (C_L = 100pF)



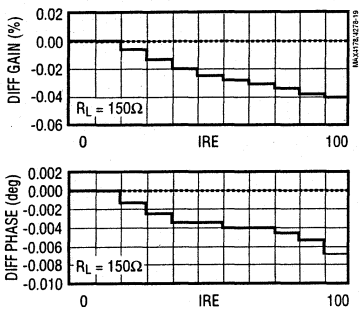
8

330MHz, Gain of +1/Gain of +2 Closed-Loop Buffers

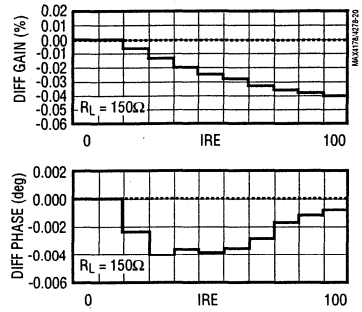
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, C_L = 0pF, T_A = +25°C, unless otherwise noted.)

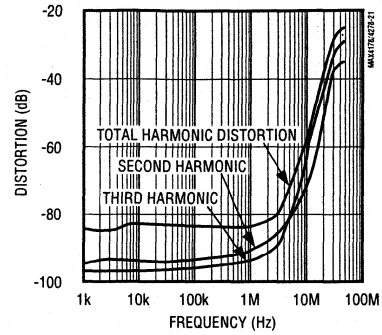
MAX4178 DIFFERENTIAL PHASE/GAIN



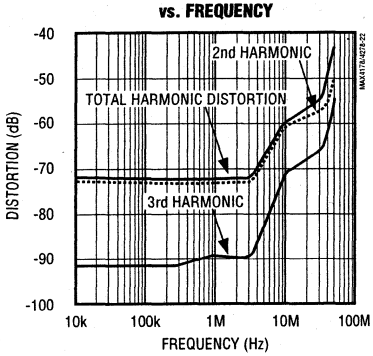
MAX4278 DIFFERENTIAL PHASE/GAIN



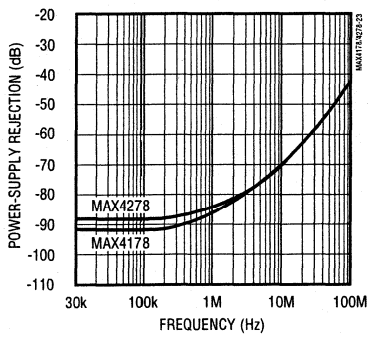
MAX4178 HARMONIC DISTORTION vs. FREQUENCY



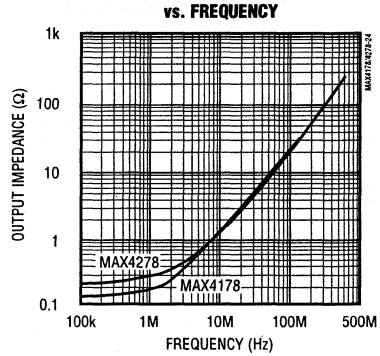
MAX4278 HARMONIC DISTORTION vs. FREQUENCY



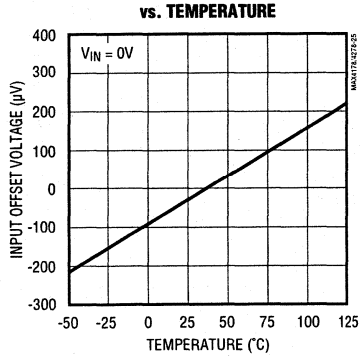
POWER-SUPPLY REJECTION vs. FREQUENCY



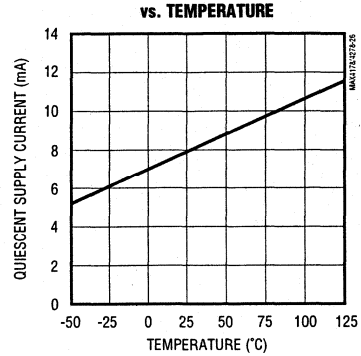
OUTPUT IMPEDANCE vs. FREQUENCY



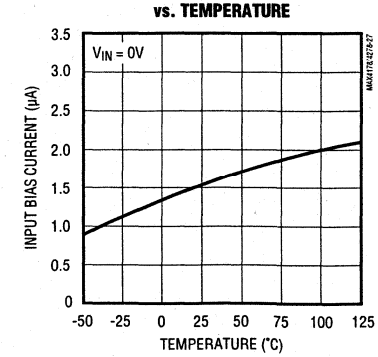
INPUT OFFSET VOLTAGE (V_{OS}) vs. TEMPERATURE



QUIESCENT SUPPLY CURRENT (I_{SY}) vs. TEMPERATURE



INPUT BIAS CURRENT (I_B) vs. TEMPERATURE

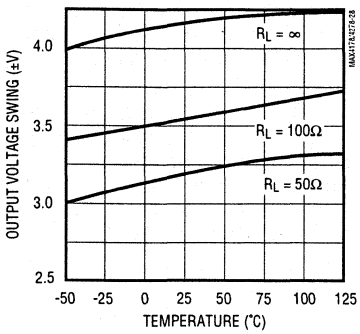


330MHz, Gain of +1/Gain of +2 Closed-Loop Buffers

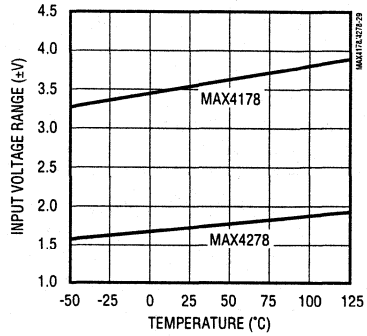
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, C_L = 0pF, T_A = +25°C, unless otherwise noted.)

OUTPUT VOLTAGE SWING vs. TEMPERATURE



INPUT VOLTAGE RANGE vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1, 5, 8	N.C.	No Connection
2	GND	Ground
3	IN	Input
4	V_{EE}	Negative Power Supply. Connect to -5V.
6	OUT	Output
7	V_{CC}	Positive Power Supply. Connect to +5V.

Detailed Description

The MAX4178/MAX4278 are ±5V, wide-bandwidth, fast-settling, closed-loop buffers featuring high slew rate, high precision, high output current, low noise, and low differential gain and phase errors. The MAX4178, with a -3dB bandwidth of 330MHz, is preset for unity voltage gain (0dB). The MAX4278 is preset for a voltage gain of +2 (6dB) and has a 310MHz -3dB bandwidth.

These devices have a unique input stage that combines the benefits of a current-mode-feedback topology (high slew rate and low power) with those of a traditional voltage-feedback topology. This combination of architectures results in low input offset voltage and bias current, and high gain precision and power-supply rejection.

Under short-circuit conditions, the output current is typically limited to 150mA. This is low enough that a short to ground of any duration will not cause permanent damage to the chip. However, a short to either supply will create double the allowable power dissipation and may cause permanent damage if allowed to exist for longer than approximately 10 seconds. The high output-current capability is an advantage in systems that transmit a signal to several loads. See *High-Performance Video Distribution Amplifier* in the *Applications Information* section.

330MHz, Gain of +1/Gain of +2 Closed-Loop Buffers

Applications Information

Grounding, Bypassing, and PC Board Layout

In order to obtain the MAX4178/MAX4278's full 330MHz/310MHz bandwidths, Micro-Strip and Stripline techniques are recommended in most cases. To ensure that the PC board does not degrade the amplifier's performance, it's a good idea to design the board for a frequency greater than 1GHz. Even with very short traces, it's good practice to use these techniques at critical points, such as inputs and outputs. Whether you use a constant-impedance board or not, observe the following guidelines when designing the board:

- Do not use wire-wrap boards. They are too inductive.
- Do not use IC sockets. They increase parasitic capacitance and inductance.
- In general, surface-mount components have shorter leads and lower parasitic reactance, giving better high-frequency performance than through-hole components.
- The PC board should have at least two layers, with one side a signal layer and the other a ground plane.
- Keep signal lines as short and straight as possible. Do not make 90° turns; round all corners.
- The ground plane should be as free from voids as possible.

On Maxim's evaluation kit, the ground plane has been removed from areas where keeping the trace capacitance to a minimum is more important than maintaining ground continuity.

Driving Capacitive Loads

The MAX4178/MAX4278 provide maximum AC performance with no output load capacitance. This is the case when the MAX4178/MAX4278 are driving a correctly terminated transmission line (e.g., a back-terminated 75Ω cable). However, the MAX4178/MAX4278 are capable of driving capacitive loads up to 100pF without oscillations, but with reduced AC performance

Driving large capacitive loads increases the chance of oscillations in most amplifier circuits. This is especially true for circuits with high loop gains, such as voltage followers. The amplifier's output resistance and the load capacitor combine to add a pole and excess phase to the loop response. If the frequency of this pole is low enough and if phase margin is degraded sufficiently, oscillations may occur.

A second problem when driving capacitive loads results from the amplifier's output impedance, which looks inductive at high frequency. This inductance forms an L-C resonant circuit with the capacitive load, which causes peaking in the frequency response and degrades the amplifier's gain margin.

The MAX4178/MAX4278 drive capacitive loads up to 100pF without oscillation. However, some peaking (in the frequency domain) or ringing (in the time domain) may occur. This is shown in Figures 2a and 2b and the in the Small- and Large-Signal Pulse Response graphs in the *Typical Operating Characteristics*.

To drive larger-capacitance loads or to reduce ringing, add an isolation resistor between the amplifier's output and the load, as shown in Figure 1.

The value of R_{ISO} depends on the circuit's gain and the capacitive load. Figures 3a and 3b show the Bode plots that result when a 20Ω isolation resistor is used with a voltage follower driving a range of capacitive loads. At the higher capacitor values, the bandwidth is dominated by the RC network, formed by R_{ISO} and C_L; the bandwidth of the amplifier itself is much higher. Note that adding an isolation resistor degrades gain accuracy. The load and isolation resistor form a divider that decreases the voltage delivered to the load.

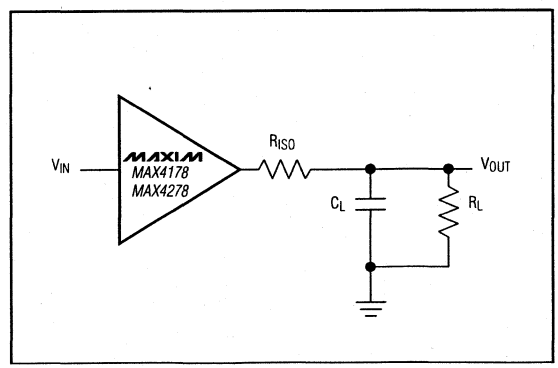


Figure 1. Capacitive-Load Driving Circuit

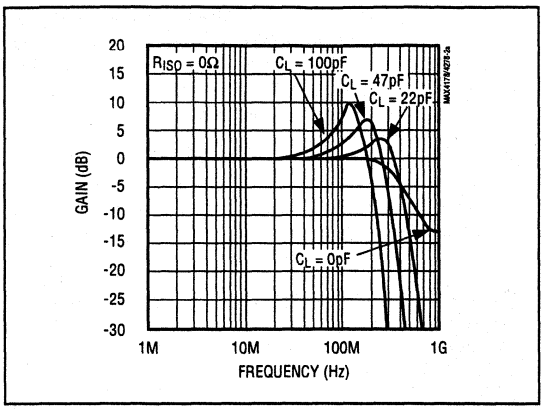


Figure 2a. MAX4178 Small-Signal Gain vs. Frequency with Capacitive Load

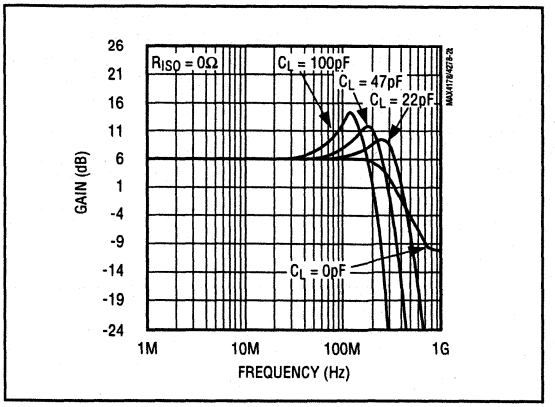


Figure 2b. MAX4278 Small-Signal Gain vs. Frequency with Capacitive Load

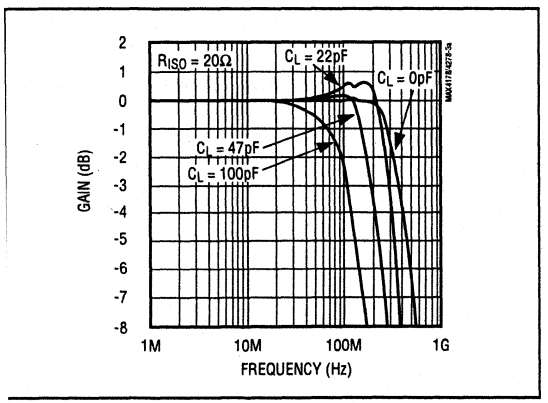


Figure 3a. MAX4178 Small-Signal Gain vs. Frequency with Capacitive Load and Isolation Resistor (R_{ISO})

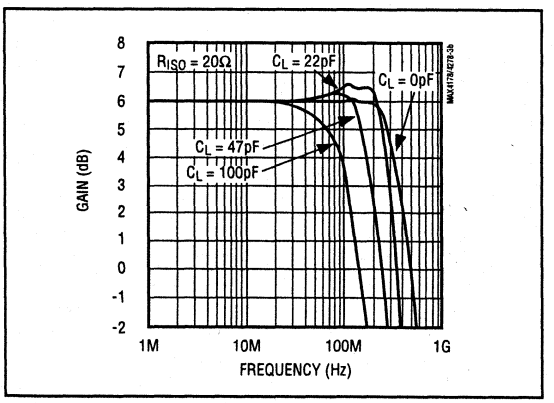


Figure 3b. MAX4278 Small-Signal Gain vs. Frequency with Capacitive Load and Isolation Resistor (R_{ISO})

330MHz, Gain of +1/Gain of +2 Closed-Loop Buffers

Flash ADC Preamp

The MAX4178/MAX4278's high current-drive capability makes them well suited for buffering the low-impedance input of a high-speed flash ADC. With their low output impedance, these buffers can drive the inputs of the ADC with no loss of accuracy. Figure 4 shows a preamp for digitizing video, using the 250Msps MAX100 and the 500Msps MAX101 flash ADCs. Both of these ADCs have a 50Ω input resistance and a 1.2GHz input bandwidth.

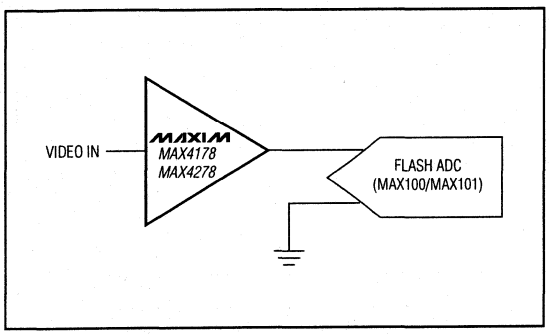


Figure 4. Preamp for Video Digitizer

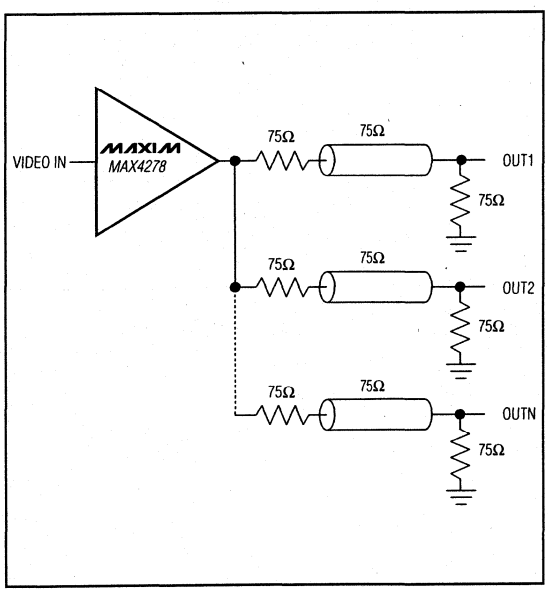


Figure 5. High-Performance Video Distribution Amplifier

High-Performance Video Distribution Amplifier

The MAX4278 (A_V = +2) makes an excellent driver for multiple back-terminated 75Ω video coaxial cables (Figure 5). The high current-output capability allows the attachment of up to six ±2Vp-p, 150Ω loads to the MAX4278 at +25°C. With the output limited to ±1Vp-p, the number of loads may double. For multiple gain-of-2 video line drivers in a single package, see the MAX496/MAX497data sheet

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX4278EPA	-40°C to +85°C	8 Plastic DIP
MAX4278ESA	-40°C to +85°C	8 SO
MAX4278EUA	-40°C to +85°C	8 µMAX*
MAX4278MJA	-55°C to +125°C	8 CERDIP

** Contact factory for availability.*

_____Chip Information

TRANSISTOR COUNT: 175

SUBSTRATE CONNECTED TO V_{EE}

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

11/96

MAXIM

Low-Power, High-Speed SOT23 Amplifiers

General Description

The MAX4180–MAX4187 current-mode feedback amplifiers combine high-speed performance, low distortion, and excellent video specifications with ultra-low-power operation. They operate with dual supplies ranging from ±2.25V to ±5.5V or a single +5V supply, and require only 1mA of supply current per amp. The MAX4180/MAX4181 are single amplifiers, the MAX4182–MAX4185 are dual amplifiers, and the MAX4186/MAX4187 are quad amplifiers. The MAX4180/MAX4182/MAX4183/MAX4186 are optimized for applications with a closed-loop gain of +2 (6dB) or greater and provide a -3dB bandwidth of 275MHz. The MAX4181/MAX4184/MAX4185/MAX4187 are optmized for applications with a gain of +1 (0dB) or greater and have a -3dB bandwidth of 325MHz.

The MAX4180–MAX4187 feature 0.02%/0.04° differential gain and phase errors, a fast 16ns settling time to 0.1%, and a 1000V/µs slew rate, making them ideal for high-performance video applications. The single MAX4180/MAX4181 are offered in space-saving 6-pin SOT23 packages.

Applications

Broadcast and High-Definition Video Systems
Multimedia Products
High-Speed A/D Buffers
Medical Imaging
Professional Cameras
CCD Imaging Systems
RGB Video
Pulse/RF Amplifier

Features

- ♦ **Low Supply Current: 1mA/Amplifier**
- ♦ **High Speed:**
  - **325MHz -3dB Small-Signal Bandwidth (MAX4181/84/85/87)**
  - **275MHz -3dB Small-Signal Bandwidth (MAX4180/82/83/86)**
- ♦ **1000V/µs Slew Rate**
- ♦ **Fast Settling Time: 16ns to 0.1%**
- ♦ **Excellent Video Specifications:**
  - **60MHz -0.1dB Gain Flatness (MAX4181/84/85/87)**
  - **80MHz -0.1dB Gain Flatness (MAX4180/82/83/86)**
  - **0.04° Differential Phase**
  - **0.02% Differential Gain**
- ♦ **Low Distortion: 75dB SFDR (at f_C = 5MHz, V_O = 2Vp-p)**
- ♦ **2pF Input Capacitance**
- ♦ **Available in 6-pin SOT23 Package (MAX4180/81)**

Ordering Information

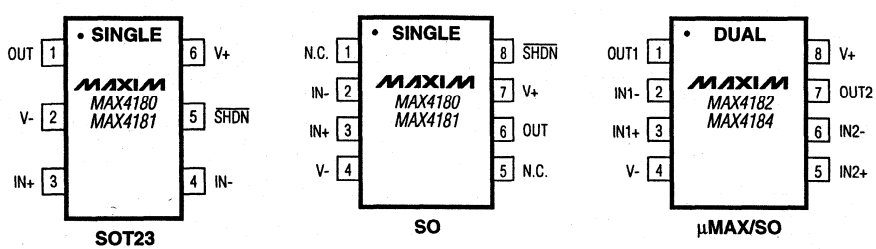
PART	TEMP. RANGE	PIN-PACKAGE
MAX4180ESA	-40°C to +85°C	8 SO
MAX4180EUT	-40°C to +85°C	6 SOT23-6
MAX4181ESA	-40°C to +85°C	8 SO
MAX4181EUT	-40°C to +85°C	6 SOT23-6

Ordering Information continued on next page.

8

Pin Configurations

TOP VIEW



N.C. = NO CONNECTION (NOT INTERNALLY CONNECTED)

Pin Configurations continued on next page.

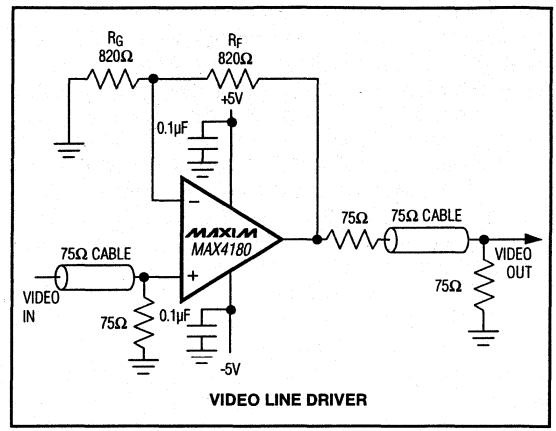
For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Low-Power, High-Speed SOT23 Amplifiers

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX4182ESA	-40°C to +85°C	8 SO
MAX4182EUA	-40°C to +85°C	8 µMAX
MAX4183ESD	-40°C to +85°C	14 SO
MAX4183EEE	-40°C to +85°C	16 QSOP
MAX4184ESA	-40°C to +85°C	8 SO
MAX4184EUA	-40°C to +85°C	8 µMAX
MAX4185ESD	-40°C to +85°C	14 SO
MAX4185EEE	-40°C to +85°C	16 QSOP
MAX4186ESD	-40°C to +85°C	14 SO
MAX4186EEE	-40°C to +85°C	16 QSOP
MAX4187ESD	-40°C to +85°C	14 SO
MAX4187EEE	-40°C to +85°C	16 QSOP

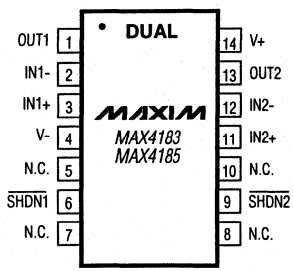
Typical Application Circuit



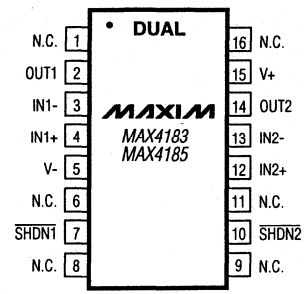
VIDEO LINE DRIVER

Pin Configurations (continued)

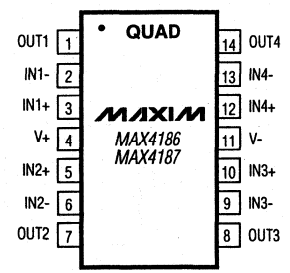
TOP VIEW



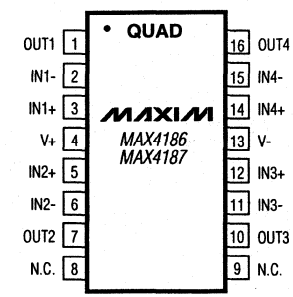
SO



QSOP



SO



QSOP

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

10/96

MAXIM

225MHz, Ultra-Low-Distortion Op Amps

General Description

The MAX4308/MAX4309 op amps combine ultra-high-speed performance with low-distortion operation. The MAX4308 is compensated for stability at closed-loop gains (A_{VCL}) of 5V/V or greater, while the MAX4309 is compensated for A_{VCL} greater than or equal to 10V/V.

The MAX4308 delivers a 225MHz bandwidth with a 1200V/µs slew rate, while the MAX4309 provides a 200MHz bandwidth with a 1200V/µs slew rate. The low-distortion design provides an unprecedented spurious-free dynamic range of -90dBc at 5MHz (V_O = 2Vp-p, R_L = 100Ω), making these amplifiers ideal for high-performance RF signal processing.

These high-speed op amps have a wide output voltage swing and a high current-drive capability of 90mA.

Features

- **225MHz Unity-Gain Bandwidth (MAX4308)**
  200MHz -3dB Bandwidth (MAX4309)
- **1200V/µs Slew Rate**
- **-90dBc SFDR at f_C = 5MHz**
- **200MHz Full-Power Bandwidth (V_O = 2Vp-p)**
- **Voltage Feedback Architecture**
- **High Output Drive: 90mA**
- **Output Short-Circuit Protected**

Applications

RGB and Composite Video

High-Performance Receivers

Pulse/RF Amplifier

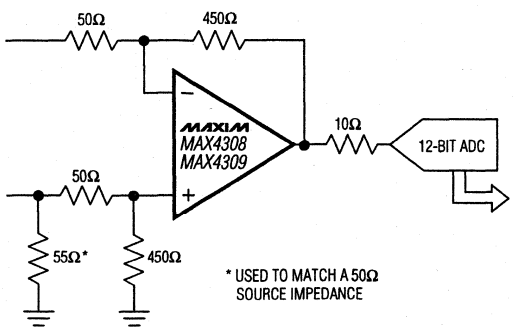
ADC/DAC Preamp

Active Filters

Ordering Information

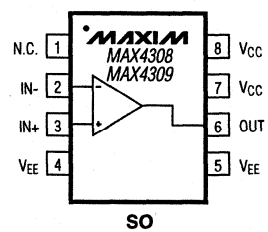
PART	TEMP. RANGE	PIN-PACKAGE
MAX4308ESA	-40°C to +85°C	8 SO
MAX4309ESA	-40°C to +85°C	8 SO

Typical Application Circuit



DIFFERENCE AMPLIFIER/ADC PREAMPLIFIER

Pin Configuration



SO

8

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

MAXIM

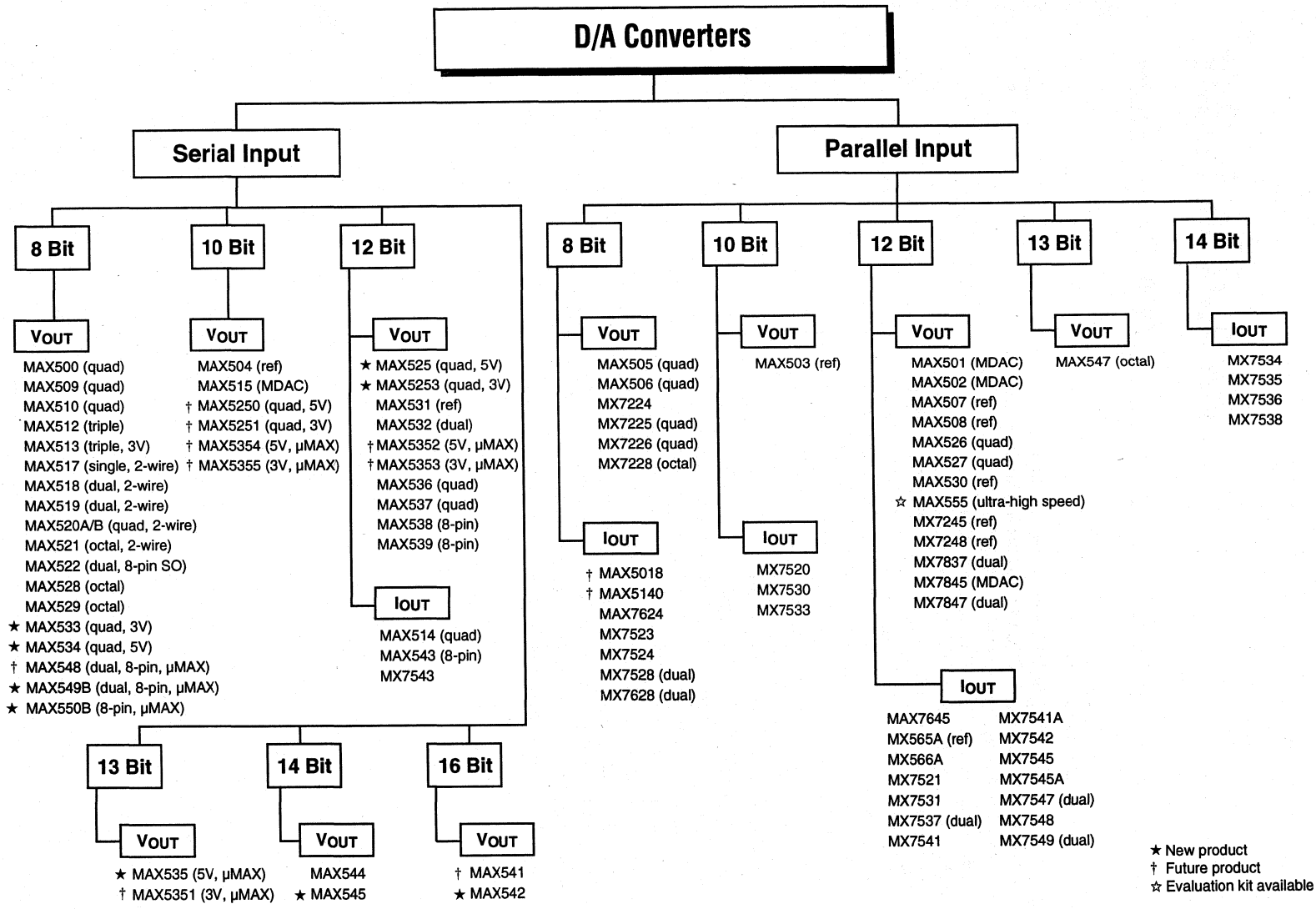
D/A Converters

D/A Converters, Product Tables and Trees 9-2

MAX520A/B	Quad, 2-Wire, Serial, 8-Bit DAC with Unbuffered Outputs	9-7
MAX521	Octal, 2-Wire, Serial, 8-Bit DAC with Rail-to-Rail Outputs	9-7
MAX525	Lowest Power, +5V, Serial, Quad 12-Bit DAC	9-25
MAX533	+3V, Serial, Quad 8-Bit DAC in QSOP Package	9-41
MAX534	+5V, Serial, Quad 8-Bit DAC in QSOP Package	9-57
MAX535	+5V, 13-Bit, Serial, Voltage-Output DAC in 8-Pin µMAX Package	9-71
MAX541	+5V, 16-Bit, Serial, Voltage-Output DAC in 8-Pin Package	9-83
MAX542	+5V, 16-Bit, Serial, Voltage-Output DAC with Bipolar Output Configuration	9-83
MAX544	+5V, 14-Bit, Serial, Voltage-Output DAC in 8-Pin Package	9-95
MAX545	+5V, 14-Bit, Serial, Voltage-Output DAC with Bipolar Output Configuration	9-95
MAX549	2.7V to 5.5V, 8-Bit, Dual, Voltage-Output DAC in 8-Pin Package	9-107
MAX550B	2.7V to 5.5V, 8-Bit, Single, Serial, Voltage-Output DAC in 8-Pin Package	9-115
MAX5018	165/275Msps Video DAC with Controls	9-125*
MAX5140	400Msps High-Resolution Video DAC	9-127*
MAX5250	+5V, Quad, 10-Bit Voltage-Output DAC with Serial Interface	9-129*
MAX5251	+3V, Quad, 10-Bit Voltage-Output DAC with Serial Interface	9-131*
MAX5253	+3V, Quad, 12-Bit Voltage-Output DAC with Serial Interface	9-133
MAX5351	+3.3V, Low-Power, 13-Bit Voltage-Output DAC with Serial Interface	9-149*
MAX5352	+5V, 12-Bit Voltage-Output DAC with Serial Interface	9-151*
MAX5353	+3.3V, 12-Bit Voltage-Output DAC with Serial Interface	9-151*
MAX5354	+5V, 10-Bit Voltage-Output DAC with Serial Interface	9-153*
MAX5355	+3.3V, 10-Bit Voltage-Output DAC with Serial Interface	9-153*

*Advance Information–first page of data sheet in preparation.

D/A Converters



Part Number	Resolution (Bits)	Output Type*	Settling Time (µs)	Reference**	Data-Bus Interface (Bits)	Supply Voltage (V)	Features	Price† 1000-up ($)
MX7224	8	V	5.0	Ext	µP/8	+12 to +15 & -5	Single or dual supplies	3.16
MAX517	8	V	6.0	Ext	Serial, 2-wire	+5	2-wire interface	2.10
MAX550	8	V	***	Ext	Serial	+2.5 to +5.5	8-pin µMAX, 2.5V, <0.7mW	1.45
MAX5018	8	I	4.5ns	Ext	Parallel	-5.2	165/275Msps video DAC with controls	††
MAX5140	8	I	3ns	Ext	Parallel	-5.2	400Msps high-resolution video DAC	††
MX7523	8	I	0.15	MDAC	Logic	+15	Low-cost 8-bit DAC	2.60
MAX7624	8	I	0.25	MDAC	µP/8	+12 to +15	Improved MX7524	2.26
MX7524	8	I	0.4	MDAC	µP/8	+5 to +15	Low-cost 8-bit DAC	2.52
MAX5354	10	V	20.0	Ext	Serial	+5	+5V, 10-bit, 8-pin µMAX	††
MAX5355	10	V	20.0	Ext	Serial	+3.3	+3.3V, 10-bit, 8-pin µMAX	††
MAX503	10	V	25.0	Int/MDAC	µP/8	+5 or ±5	Ultra-low power, complete DAC	2.95
MAX504	10	V	25.0	Int/MDAC	Serial	+5 or ±5	Serial version of MAX503	2.80
MAX515	10	V	25.0	Ext	Serial	+5	Ultra-low power, 8-pin DIP/SO	2.50
MX7520	10	I	0.5	MDAC	Logic	+15	Low-cost 10-bit DAC	2.80
MX7530	10	I	0.5	MDAC	Logic	+15	Low-cost 10-bit DAC	2.80
MX7533	10	I	0.6	MDAC	Logic	+15	Low-cost 10-bit DAC	2.84
MAX555	12	V	0.5ns	Ext/MDAC	Parallel	-5.2	300Msps update rate, 72dB SFDR	‡
MAX501	12	V	5.0	MDAC	µP/8	±12 to ±15	4-quadrant multiplying DAC	5.65
MAX502	12	V	5.0	MDAC	µP/12	±12 to ±15	4-quadrant multiplying DAC	5.65
MAX507	12	V	5.0	Int	µP/12	±12 to ±15	Complete 12-bit DAC with reference	7.65
MAX508	12	V	5.0	Int	µP/8	±12 to ±15	Complete 12-bit DAC with reference	7.65
MX7845	12	V	5.0	MDAC	µP/12	±15	4-range, 4-quadrant multiplying DAC	6.26
MX7245	12	V	10.0	Int	µP/12	±15 or +12 to +15	Single or dual supplies with reference	8.33
MX7248	12	V	10.0	Int	µP/8	±15 or +12 to +15	8-bit interface MX7245	8.33
MAX5352	12	V	20.0	Ext	Serial	+5	+5V, 12-bit, 8-pin µMAX, 1.5mW	††
MAX5353	12	V	20.0	Ext	Serial	+3.3	+3.3V, 12-bit, 8-pin µMAX, 0.9mW	††
MAX530	12	V	25.0	Int/MDAC	µP/8	+5 or ±5	Ultra-low power, flexible output range	5.45
MAX531	12	V	25.0	Int/MDAC	Serial	+5 or ±5	Serial version of MAX530	5.45
MAX538	12	V	25.0	Ext	Serial	+5	8-pin DIP/SO, ultra-low power, 0V to 2V output	4.85
MAX539	12	V	25.0	Ext	Serial	+5	8-pin DIP/SO, ultra-low power, 0V to 5V output	4.85
MX565A	12	I	0.25	Int	Logic	±15	10V buried-zener reference	9.68
MX566A	12	I	0.35	Ext	Logic	-15	No internal reference	9.04
MX7521	12	I	0.5	MDAC	Logic	+15	Low-cost 12-bit DAC	5.00
MX7531	12	I	0.5	MDAC	Logic	+15	Low-cost 12-bit DAC	5.08
MX7541A	12	I	0.6	MDAC	Logic	+15	12-bit data bus	5.72
MAX543	12	I	1.0	MDAC	Serial	+5 to +15	12-bit multiplying DAC in 8-pin DIP/SO	4.80
MAX7645	12	I	1.0	MDAC	µP/12	+15	Improved MX7545	5.60
MX7541	12	I	1.0	MDAC	Logic	+15	12-bit data bus	5.07
MX7545A	12	I	1.0	MDAC	µP/12	+5 to +15	Improved MX7545	6.03
MX7548	12	I	1.0	MDAC	µP/8	+5 to +15	8-bit data bus with latches	6.06
MX7542	12	I	2.0	MDAC	µP/4	+5	4-bit data bus with latches	7.52
MX7543	12	I	2.0	MDAC	Serial	+5	12-bit multiplying DAC	7.52
MX7545	12	I	2.0	MDAC	µP/12	+5 to +15	12-bit data bus with latches	5.00
MAX535	13	V	20.0	Ext	Serial	+5	13-bit, 8-pin µMAX, 1.5mW	4.95
MAX5351	13	V	20.0	Ext	Serial	+3.3	+3.3V, 13-bit, 8-pin µMAX, 0.9mW	††

* V = voltage, I = current

** MDAC = 4-quadrant multiplying capability, Int = internal reference, Ext = external reference

*** Settling time depends on internal resistive ladder and external load impedance.

† Prices provided are for design guidance and are FOB USA.
International prices will differ due to local duties, taxes, and exchange rates.

†† Future product—contact factory for pricing and availability. Specifications are preliminary.

‡ Contact factory for pricing.

Single D/A Converters (continued)

Part Number	Resolution (Bits)	Output Type*	Settling Time (µs)	Reference**	Data-Bus Interface (Bits)	Supply Voltage (V)	Features	Price† 1000-up ($)
MAX544	14	V	***	Ext	Serial	+5	5V, 14-bit, low power, 8-pin SO	††
MAX545	14	V	***	Ext	Serial	+5	5V, unipolar or bipolar, low power, 14-pin DIP/SO	7.90
MX7534	14	I	1.5	MDAC	µP/8	+12 to +15	Double-buffered inputs	13.37
MX7535	14	I	1.5	MDAC	µP/8 or 14	+12 to +15	Double-buffered inputs	15.00
MX7536	14	I	1.5	MDAC	µP/8 or 14	+12 to +15	No external resistors needed	14.66
MX7538	14	I	1.5	MDAC	µP/14	+12 to +15	Low-cost 14-bit DAC	8.88
MAX541	16	V	***	Ext	Serial	+5	5V, 16-bit, low power, 8-pin DIP/SO	††
MAX542	16	V	***	Ext	Serial	+5	5V, 16-bit, unipolar or bipolar, low power, 14-pin DIP/SO	9.95

Multiple D/A Converters

Part Number	Resolution (Bits)	Output Type*	Settling Time (µs)	Reference**	Data-Bus Interface (Bits)	Supply Voltage (V)	Features	Price† 1000-up ($)
DUAL								
MAX518	8	V	6.0	Int (V_{DD})	Serial, 2-wire	+5	2-wire interface, 8-pin SO	2.25
MAX519	8	V	6.0	Ext	Serial, 2-wire	+5	2-wire interface, separate reference inputs	2.35
MAX522	8	V	70.0	MDAC	Serial	+2.7 to +5.5	Low-power dual in 8-pin SO	2.25
MAX548	8	V	***	Int (V_{DD})	Serial	+2.5 to +5.5	2.5V, 8-pin µMAX, low power	††
MAX549	8	V	***	Ext	Serial	+2.5 to +5.5	2.5V, 8-pin µMAX, low power	1.65
MX7528	8	I	0.18	MDAC	µP/8	+5 to +15	Data latches for both DACs	3.79
MX7628	8	I	0.35	MDAC	µP/8	+12 to +15	Data latches for both DACs	3.80
MAX532	12	V	4.0	MDAC	Serial	±12 to ±15	16-pin DIP/SO	8.45
MX7837	12	V	4.0	Ext	µP/8	±12 to ±15	Dual V_{OUT} DAC with 8-bit data bus	12.18
MX7847	12	V	4.0	Ext	µP/12	±12 to ±15	Dual V_{OUT} DAC with 12-bit data bus	12.18
MX7537	12	I	1.5	MDAC	µP/8	+12 to +15	Dual DAC with 8-bit data bus	11.23
MX7547	12	I	1.5	MDAC	µP/12	+12 to +15	Dual DAC with 12-bit data bus	11.40
MX7549	12	I	1.5	MDAC	µP/4	+15	Dual DAC with 4-bit data bus	12.97
TRIPLE								
MAX512	8	V	60.0	MDAC	Serial	+5 or ±5	Low-power with shutdown, 14-pin narrow SO	2.85
MAX513	8	V	70.0	MDAC	Serial	+2.7 to ±3.6	For 3V systems	2.85
QUAD								
MAX500	8	V	4.0	Ext	Serial	+12 to +15 & -5	16-pin DIP/SO, three reference inputs	5.70
MX7225	8	V	4.0	Ext	µP/8	+12 to +15 & -5	Double buffered, separate reference inputs	14.14
MX7226	8	V	4.0	Ext	µP/8	+12 to +15 & -5	Single buffered, single reference input	11.80
MAX505	8	V	6.0	MDAC	µP/8	+5 or ±5	Rail-to-rail outputs, separate reference inputs	5.95
MAX506	8	V	6.0	MDAC	µP/8	+5 or ±5	Rail-to-rail outputs; single reference input	6.10
MAX509	8	V	6.0	MDAC	Serial	+5 or ±5	Rail-to-rail outputs, four reference inputs	5.35
MAX510	8	V	6.0	MDAC	Serial	+5 or ±5	Rail-to-rail outputs, one reference input	5.19
MAX520	8	V	***	Ext	Serial, 2-wire	+5	2-wire interface, separate reference inputs	3.50
MAX533	8	V	6	Ext	Serial	+2.7 to +3.6	2.7V, low-power (1.9mW), serial, 16-pin QSOP	2.80
MAX534	8	V	6	Ext	Serial	+5	Low-power, +5V, quad DAC in 16-pin QSOP	2.80

* V = voltage, I = current

** MDAC = 4-quadrant multiplying capability, Int = internal reference, Ext = external reference

*** Settling time depends on internal resistive ladder and external load impedance.

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†† Future product—contact factory for pricing and availability. Specifications are preliminary.

‡ Contact factory for pricing.

Multiple D/A Converters (continued)

Part Number	Resolution (Bits)	Output Type*	Settling Time (µs)	Reference**	Data-Bus Interface (Bits)	Supply Voltage (V)	Features	Price† 1000-up ($)
MAX5250	10	V	20.0	Ext	Serial	+5	5V, 1mW/DAC, serial, 20µA power-down, 20-pin DIP/SSOP	††
MAX5251	10	V	20.0	Ext	Serial	+3 to +3.6	3V, 0.6mW/DAC, serial, 20µA power-down	††
MAX526	12	V	3.0	Ext	µP/8	+12 to +15 & -5	Quad voltage-output DACs, available in DIP/SO	19.44
MAX527	12	V	3.0	Ext	µP/8	±5	±5V version of MAX526	16.56
MAX536	12	V	3.0	Ext	Serial	+12 to +15 & -5	Serial version of MAX526	15.95
MAX537	12	V	3.0	Ext	Serial	±5	Serial version of MAX527	15.95
MAX525	12	V	20.0	Ext	Serial	+5	<1mW/DAC, serial, 20µA power-down, 20-pin DIP/SSOP	11.95
MAX5253	12	V	16.0	Ext	Serial	+3 to +3.6	3V, 0.6mW/DAC, serial, 20µA power-down	11.35
MAX514	12	I	1.0	MDAC	Serial	+5	Quad current-output DACs, available in DIP/SO	14.25
OCTAL								
MAX528	8	V	5.0	Ext	Serial	+5 to +15, +15 & -5 or +5 & -15	µP-selected buffered and unbuffered output	6.90
MAX529	8	V	5.0	Ext	Serial	+5 or ±5	Single +5V supply MAX528	5.65
MX7228	8	V	5.0	Ext	µP/8	+5 to +15 & -5 or +15	Single or dual supplies	11.95
MAX521	8	V	6.0	Ext	Serial, 2-wire	+5	2-wire interface, five reference inputs	4.95
MAX547	13	V	5.0	Ext	µP/13	±5	Unipolar or bipolar, four reference inputs	29.60

Serial D/A Converters

Part Number	Resolution (Bits)	Output Type*	DACs in Package	Reference**	Settling Time (µs)	Data-Bus Interface (Bits)	Supply Voltage (V)	Features	Price† 1000-up ($)
MAX517	8	V	1	Ext	6.0	Serial, 2-wire	+5	2-wire interface	2.10
MAX550B	8	V	1	Ext	***	Serial	+2.5 to +5.5	8-pin µMAX, 2.5V, <0.7mW	1.45
MAX518	8	V	2	Int (V_{DD})	6.0	Serial, 2-wire	+5	2-wire interface, 8-pin SO	2.25
MAX519	8	V	2	Ext	6.0	Serial, 2-wire	+5	2-wire interface, two reference inputs	2.35
MAX522	8	V	2	MDAC	6.0	Serial	+2.7 to +5.5	Low-power dual in 8-pin SO	2.25
MAX548	8	V	2	Int (V_{DD})	***	Serial	+2.5 to +5.5	2.5V, 8-pin µMAX, low power	††
MAX549B	8	V	2	Ext	***	Serial	+2.5 to +5.5	2.5V, 8-pin µMAX, low power	1.65
MAX512	8	V	3	MDAC	60.0	Serial	+5 or ±5	Low-power with shutdown, 14-pin narrow SO	2.85
MAX513	8	V	3	MDAC	70.0	Serial	+2.7 to ±3.6	MAX512 for 3V systems	2.85
MAX500	8	V	4	Ext	4.0	Serial	+12 to +15 & -5	16-pin DIP/SO, three reference inputs	5.70
MAX509	8	V	4	MDAC	6.0	Serial	+5 or ±5	Rail-to-rail outputs, four reference inputs	5.35
MAX510	8	V	4	MDAC	6.0	Serial	+5 or ±5	Rail-to-rail outputs, one reference input	5.19
MAX520	8	V	4	Ext	***	Serial, 2-wire	+5	2-wire interface, four reference inputs	3.50
MAX533	8	V	4	Ext	6.0	Serial	+2.7 to +3.6	2.7V, low-power (1.9mW), 16-pin QSOP	2.80
MAX534	8	V	4	Ext	6.0	Serial	+5	Low-power, +5V, quad DAC in 16-pin QSOP	2.80
MAX521	8	V	8	Ext	6.0	Serial, 2-wire	+5	2-wire interface, five reference inputs	4.95
MAX528	8	V	8	Ext	5.0	Serial	+5 to +15, +15 & -5 or +5 & -15	µP-selected buffered and unbuffered output	6.90
MAX529	8	V	8	Ext	5.0	Serial	+5 or ±5	Single +5V supply MAX528	5.65

* V = voltage, I = current

** MDAC = 4-quadrant multiplying capability, Int = internal reference, Ext = external reference

*** Settling time depends on internal resistive ladder and external load impedance.

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Serial D/A Converters (continued)

Part Number	Resolution (Bits)	Output Type*	DACs in Package	Reference**	Settling Time (µs)	Data-Bus Interface (Bits)	Supply Voltage (V)	Features	Price† 1000-up ($)
MAX504	10	V	1	Int/MDAC	25.0	Serial	+5 or ±5	Ultra-low power, rail to rail	2.80
MAX515	10	V	1	Ext	25.0	Serial	+5	Ultra-low power, 8-pin SO/DIP	2.50
MAX5250	10	V	1	Ext	20.0	Serial	+5	5V, 1mW/DAC, serial, 20µA power-down	††
MAX5251	10	V	1	Ext	16.0	Serial	+3	3V, 0.6mW/DAC, serial, 20µA power-down	††
MAX5354	10	V	1	Ext	20.0	Serial	+5	5V, 10-bit 8-pin µMAX	††
MAX5355	10	V	1	Ext	20.0	Serial	+3.3	3.3V, 10-bit 8-pin µMAX	††
MAX531	12	V	1	Int/MDAC	25.0	Serial	+5 or ±5	Ultra-low power, flexible output range	5.45
MAX5352	12	V	1	Ext	20.0	Serial	+5	5V, 12-bit, 8-pin µMAX	††
MAX5353	12	V	1	Ext	20.0	Serial	+3.3	3.3V, 12-bit, 8-pin µMAX	††
MAX538	12	V	1	Ext	25.0	Serial	+5	8-pin DIP/SO, ultra-low power, 0V to 2V output	4.85
MAX539	12	V	1	Ext	25.0	Serial	+5	8-pin DIP/SO, ultra-low power, 0V to 5V output	4.85
MAX532	12	V	2	MDAC	4.0	Serial	±12 to ±15	16-pin DIP/SO	8.45
MAX525	12	V	4	Ext	20.0	Serial	+5	<1mW/DAC, 20µA power-down, 20-pin DIP/SSOP	11.95
MAX5253	12	V	4	Ext	16.0	Serial	+3 to +3.6	3V, 0.6mW/DAC, 20µA power-down	11.35
MAX536	12	V	4	Ext	3.0	Serial	+12 to +15 & -5	Serial version of MAX526	15.95
MAX537	12	V	4	Ext	3.0	Serial	±5	Serial version of MAX527	15.95
MAX543	12	I	1	MDAC	1.0	Serial	+5 to +15	12-bit multiplying DAC in 8-pin DIP/SO	4.80
MX7543	12	I	1	MDAC	2.0	Serial	+5	12-bit multiplying DAC	7.52
MAX514	12	I	4	MDAC	1.0	Serial	+5	Quad current-output DACs, available in DIP/SO	14.25
MAX535	13	V	1	Ext	20.0	Serial	+5	13-bit, 8-pin µMAX, 1.5mW	4.95
MAX5351	13	V	1	Ext	20.0	Serial	+3.3	3.3V, 13-bit, 8-pin µMAX	††
MAX544	14	V	1	Ext	***	Serial	+5	5V, 14-bit, low power, 8-pin DIP/SO	††
MAX545	14	V	1	Ext	***	Serial	+5	5V, unipolar or bipolar, low power, 14-pin DIP SO	7.90
MAX541	16	V	1	Ext	***	Serial	+5	5V, 16-bit, low power, 8-pin DIP/SO	††
MAX542	16	V	1	Ext	***	Serial	+5	5V, 16-bit, unipolar or bipolar, low power, 14-pin DIP/SO	9.95

* V = voltage, I = current

** MDAC = 4-quadrant multiplying capability, Int = internal reference, Ext = external reference

*** Settling time depends on internal resistive ladder and external load impedance.

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†† Future product—contact factory for pricing and availability. Specifications are preliminary.

19-0378; Rev 3; 9/96

MAXIM

Quad/Octal, 2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

General Description

The MAX520/MAX521 are quad/octal, 8-bit voltage-output digital-to-analog converters (DACs) with simple 2-wire serial interfaces that allow communication between multiple devices. They operate from a single +5V supply and their reference input range includes both supply rails.

The MAX521 includes rail-to-rail output buffer amplifiers for reduced system size and component count when driving loads. The MAX520's unbuffered voltage outputs reduce the device's total supply current to 4µA and provide increased accuracy at low output currents.

The MAX520/MAX521 feature a serial interface and internal software protocol, allowing communication at data rates up to 400kbps. The interface, combined with the double-buffered input configuration, allows the DAC registers to be updated individually or simultaneously. In addition, the devices can be put into a low-power shutdown mode that reduces supply current to 4µA. Power-on reset ensures the DAC outputs are at 0V when power is initially applied.

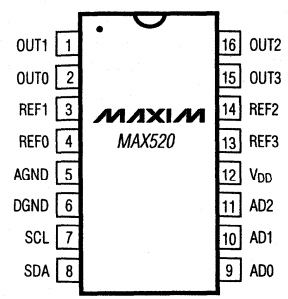
The MAX520 is available in 16-pin DIP and wide SO packages, as well as a space-saving 20-pin SSOP. The MAX521 comes in 20-pin DIP and 24-pin SO packages, as well as a space-saving 24-pin SSOP.

Applications

Minimum Component Analog Systems
Digital Offset/Gain Adjustment
Industrial Process Control
Automatic Test Equipment
Programmable Attenuators

Pin Configurations

TOP VIEW



DIP/SO

Pin Configurations continued at end of data sheet.

Features

- **Single +5V Supply**
- **Simple 2-Wire Serial Interface**
- **I²C Compatible**
- **Outputs Swing Rail to Rail:**
  Unbuffered Outputs (MAX520)
  Buffered Outputs (MAX521)
- **1%-Accurate Trimmed Output Resistance (MAX520A)**
- **Ultra-Low 4µA Supply Current (MAX520)**
- **Individual DACs Have Separate Reference Inputs**
- **Power-On Reset Clears All Latches**
- **4µA Power-Down Mode**

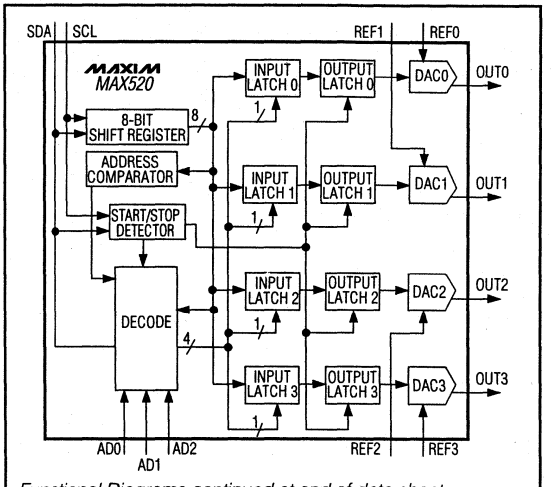
Ordering Information

PART†	TEMP. RANGE	PIN-PACKAGE	TUE (LSB)
MAX520ACPE	0°C to +70°C	16 Plastic DIP	1
MAX520BCPE	0°C to +70°C	16 Plastic DIP	1
MAX520ACWE	0°C to +70°C	16 Wide SO	1
MAX520BCWE	0°C to +70°C	16 Wide SO	1

Ordering Information continued at end of data sheet.

†*MAX520 "A" grade parts include a 1%-accurate, factory-trimmed output resistance.*

Functional Diagrams



Functional Diagrams continued at end of data sheet.

9

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Quad/Octal, 2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND .....-0.3V to +6V
V_{DD} to AGND.....-0.3V to +6V
OUT_ .....-0.3V to (V_{DD} + 0.3V)
REF_.....-0.3V to (V_{DD} + 0.3V)
AD0, AD1, AD2.....-0.3V to (V_{DD} + 0.3V)
SCL, SDA to DGND .....-0.3V to +6V
AGND to DGND.....-0.3V to +0.3V
Maximum Current into Any Pin.....50mA
Continuous Power Dissipation (T_A = +70°C)
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C)....842mW
20-Pin Plastic DIP (derate 11.11mW/°C above +70°C)....889mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) 762mW
24-Pin Wide SO (derate 11.76mW/°C above +70°C) 941mW
20-Pin SSOP (derate 8.00mW/°C above +70°C) 640mW
24-Pin SSOP (derate 8.00mW/°C above +70°C) 640mW
16-Pin CERDIP (derate 10.00mW/°C above +70°C)....800mW
20-Pin CERDIP (derate 11.11mW/°C above +70°C)....889mW
Operating Temperature Ranges
MAX520_C_ _/MAX521_C_ _.....0°C to +70°C
MAX520_E_ _/MAX521_E_ _ .....-40°C to +85°C
MAX520_MJE/MAX521BMJP .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ±10%, $V_{REF_}$ = 4V, R_L = ∞ (MAX520), R_L = 10kΩ (MAX521), C_L = 0pF (MAX520), C_L = 100pF (MAX521), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC ACCURACY							
Resolution				8			Bits
Total Unadjusted Error	TUE		MAX520_			±1	LSB
			MAX521A			±1.5	
			MAX521B			±2	
Differential Nonlinearity	DNL	Guaranteed monotonic				±1.0	LSB
Zero-Code Error	ZCE	Code = 00 hex	MAX520_			8	mV
			MAX521_C			18	
			MAX521_E			20	
			MAX521BM			20	
Zero-Code-Error Supply Rejection		Code = 00 hex			±1		mV
Zero-Code-Error Temperature Coefficient		Code = 00 hex			±10		µV/°C
Full-Scale Error		Code = FF hex	MAX520_			8	mV
			MAX521_C			18	
			MAX521_E			20	
			MAX521BM			20	
Full-Scale-Error Supply Rejection		Code = FF hex, V_{DD} = 5V ±10%			±1		mV
Full-Scale-Error Temperature Coefficient					±10		µV/°C

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V ±10%, $V_{REF_}$ = 4V, R_L = ∞ (MAX520), R_L = 10kΩ (MAX521), C_L = 0pF (MAX520), C_L = 100pF (MAX521), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
REFERENCE INPUTS								
Input Voltage Range					0		V_{DD}	V
Input Resistance	R_{IN}	Code = 55 hex (Note 1)	MAX520_		8	12		kΩ
			MAX521_	REF4	4	6		
				REF0–REF3	16	24		
Input Current		PD = 1					±10	µA
Input Capacitance		Code = FF hex (Note 2)	MAX520_			30		pF
			MAX521_	REF4		120		
				REF0–REF3		30		
Channel-to-Channel Isolation		(Note 3)	MAX520_			-70		dB
			MAX521_			-60		
AC Feedthrough		(Note 4)				-70		dB
DAC OUTPUTS								
Full-Scale Output Voltage					0		V_{DD}	V
Output Resistance (Note 5)		MAX520A	T_A = +25°C		15.8	16	16.2	kΩ
			T_A = T_{MIN} to T_{MAX}		15.6	16	16.4	
		MAX520B			8.4		16.4	
Output Load Regulation		MAX521_, OUT_ = 4V, 0mA to 2.5mA				0.25		LSB
		MAX521_C/E, $V_{REF_}$ = V_{DD}, code = FF hex, 0µA to 500µA				1.5		
		MAX521BM, $V_{REF_}$ = V_{DD}, code = FF hex, 0µA to 500µA				2.0		
Output Leakage Current		MAX521_, OUT_ = 0V to V_{DD}, PD = 1					±10	µA
DIGITAL INPUTS SCL, SDA								
Input High Voltage	V_{IH}				0.7V_{DD}			V
Input Low Voltage	V_{IL}						0.3V_{DD}	V
Input Current	I_{IN}	0V ≤ V_{IN} ≤ V_{DD}					±10	µA
Input Hysteresis	V_{HYST}	(Note 5)			0.05V_{DD}			V
Input Capacitance	C_{IN}	(Note 5)					10	pF
DIGITAL INPUTS AD0, AD1								
Input High Voltage	V_{IH}				2.4			V
Input Low Voltage	V_{IL}						0.8	V
Input Leakage	I_{IN}	V_{IN} = 0V to V_{DD}					±10	µA
DIGITAL OUTPUT SDA (Note 6)								
Output Low Voltage	V_{OL}	I_{SINK} = 3mA					0.4	V
		I_{SINK} = 6mA					0.6	
Three-State Leakage Current	I_L	V_{IN} = 0V to V_{DD}					±10	µA
Three-State Output Capacitance	C_{OUT}	(Note 5)					10	pF

Quad/Octal, 2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V ±10%, $V_{REF_}$ = 4V, R_L = ∞ (MAX520), R_L = 10kΩ (MAX521), C_L = 0pF (MAX520), C_L = 100pF (MAX521), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE							
Voltage Output Slew Rate		Positive and negative	MAX521_C		1.0		V/µs
			MAX521_E		0.7		
			MAX521BM		0.5		
Output Settling Time		MAX520_, to 1/2LSB, no load			2		µs
		MAX521_, to 1/2LSB, 10kΩ and 100pF load (Note 7)			6		
Digital Feedthrough		Code = 00 hex, all digital inputs from 0V to V_{DD}			5		nV-s
Digital-Analog Glitch Impulse		Code 128 to 127			12		nV-s
Signal to Noise + Distortion Ratio	SINAD	$V_{REF_}$ = 4Vp-p at 1kHz, V_{DD} = 5V, code = FF hex			87		dB
Multiplying Bandwidth		$V_{REF_}$ = 4Vp-p, 3dB bandwidth			1		MHz
Wideband Amplifier Noise		MAX521_			60		μV_{RMS}
POWER REQUIREMENTS							
Supply Voltage	V_{DD}			4.5		5.5	V
Supply Current	I_{DD}	Operating mode, output unloaded, all digital inputs 0V or V_{DD}	MAX520_		4	20	µA
			MAX521_C		10	20	mA
			MAX521_E/BM		10	24	
		Power-down mode (PD = 1)			4	20	µA

Note 1: Input resistance is code dependent. The lowest input resistance occurs at code = 55 hex.
Note 2: Input capacitance is code dependent. The highest input capacitance occurs at code = FF hex.
Note 3: $V_{REF_}$ = 4Vp-p, 10kHz. Channel-to-channel isolation is measured by setting the code of one DAC to FF hex and setting the code of all other DACs to 00 hex.
Note 4: $V_{REF_}$ = 4Vp-p, 10kHz, DAC code = 00 hex.
Note 5: Guaranteed by design.
Note 6: I^2C-compatible mode.
Note 7: Output settling time is measured by taking the code from 00 hex to FF hex, and from FF hex to 00 hex.

TIMING CHARACTERISTICS

(V_{DD} = 5V ±10%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between a STOP and a START Condition	t_{BUF}		1.3			µs
Hold Time, (Repeated) Start Condition	$t_{HD, STA}$		0.6			µs
Low Period of the SCL Clock	t_{LOW}		1.3			µs
High Period of the SCL Clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU, STA}$		0.6			µs
Data Hold Time	$t_{HD, DAT}$	(Note 8)	0		0.9	µs
Data Setup Time	$t_{SU, DAT}$		100			ns
Rise Time of Both SDA and SCL Signals, Receiving	t_R	(Note 9)	20 + 0.1Cb		300	ns
Fall Time of Both SDA and SCL Signals, Receiving	t_F	(Note 9)	20 + 0.1Cb		300	ns
Fall Time of SDA Transmitting (Note 6)	t_F	I_{SINK} ≤ 6mA (Note 9)	20 + 0.1Cb		250	ns
Setup Time for STOP Condition	$t_{SU, STO}$		0.6			µs
Capacitive Load for Each Bus Line	Cb				400	pF
Pulse Width of Spike Suppressed	t_{SP}	(Notes 10, 11)	0		50	ns

Note 8: A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) in order to bridge the undefined region of SCL's falling edge.

Note 9: Cb = total capacitance of one bus line in pF. t_R and t_f measured between 0.3V_{DD} and 0.7V_{DD}.

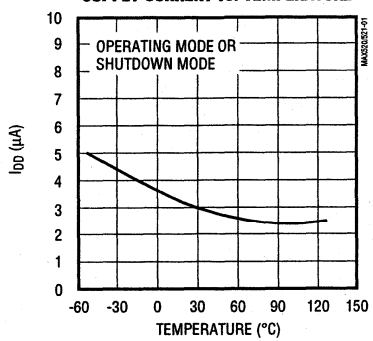
Note 10: An input filter on the SDA and SCL input suppresses noise spikes less than 50ns.

Note 11: Guaranteed by design.

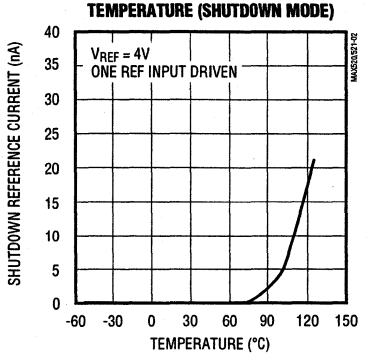
Typical Operating Characteristics

(V_{DD} = 5V, DAC outputs unloaded, T_A = +25°C, unless otherwise noted.)

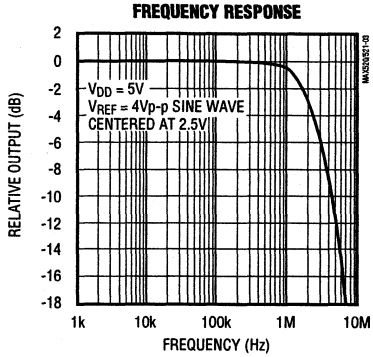
MAX520
SUPPLY CURRENT vs. TEMPERATURE



MAX520
REFERENCE INPUT CURRENT vs. TEMPERATURE (SHUTDOWN MODE)



MAX520
REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE

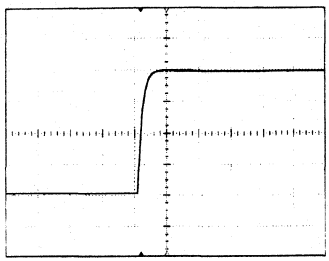


Quad/Octal, 2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

Typical Operating Characteristics (continued)

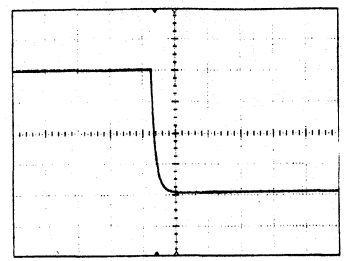
(V_{DD} = 5V, DAC outputs unloaded, T_A = +25°C, unless otherwise noted.)

MAX520
POSITIVE SETTLING TIME



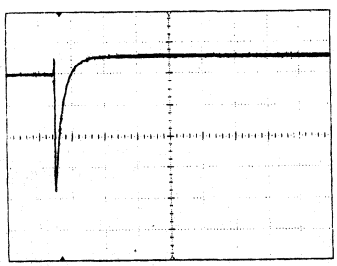
OUT2 = NO LOAD, REF2 = 4V,
DAC CODE = 00 HEX to FF HEX

MAX520
NEGATIVE SETTLING TIME



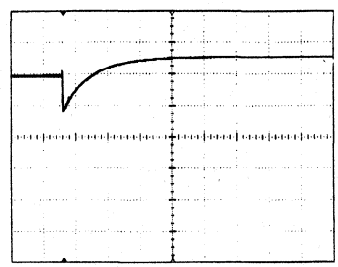
OUT2 = NO LOAD, REF2 = 4V,
DAC CODE = FF HEX to 00 HEX

MAX520
WORST-CASE 1LSB DIGITAL STEP CHANGE
(CAPACITIVE LOAD < 5pF)



REF2 = 4V, DAC CODE = 7F HEX to 80 HEX

MAX520
WORST-CASE 1LSB DIGITAL STEP CHANGE
(CAPACITIVE LOAD = 25pF)



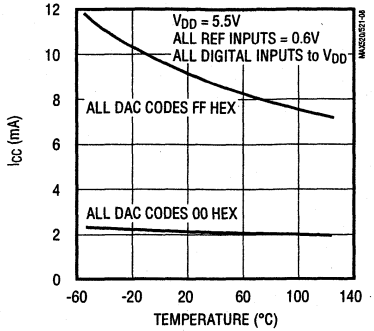
REF2 = 4V, DAC CODE = 7F HEX to 80 HEX

Quad/Octal, 2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

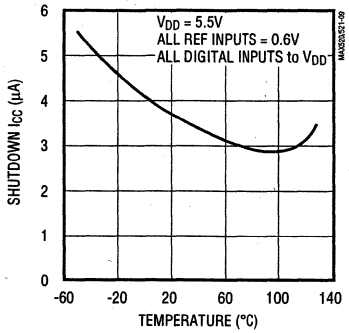
Typical Operating Characteristics

(V_{DD} = 5V, DAC outputs unloaded, T_A = +25°C, unless otherwise noted.)

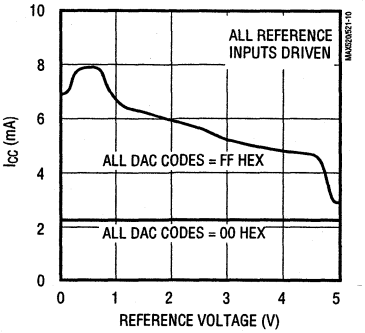
MAX521
SUPPLY CURRENT vs. TEMPERATURE



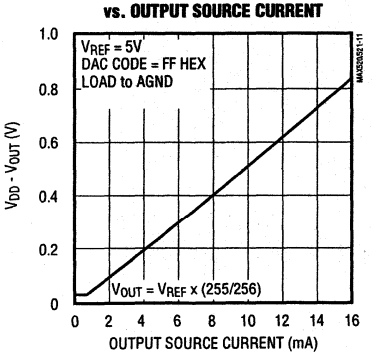
MAX521
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



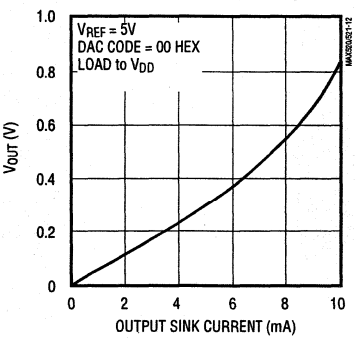
MAX521
SUPPLY CURRENT vs. REFERENCE VOLTAGE



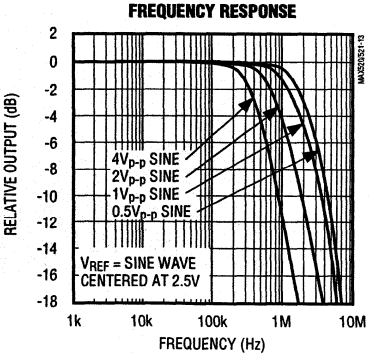
MAX521
DAC OUTPUT HIGH VOLTAGE vs. OUTPUT SOURCE CURRENT



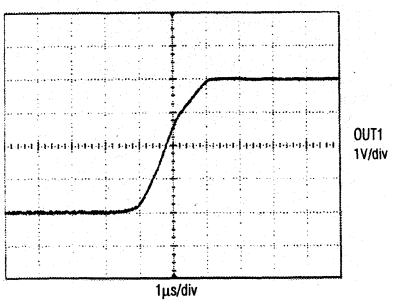
MAX521
DAC OUTPUT LOW VOLTAGE vs. OUTPUT SINK CURRENT



MAX521
REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE

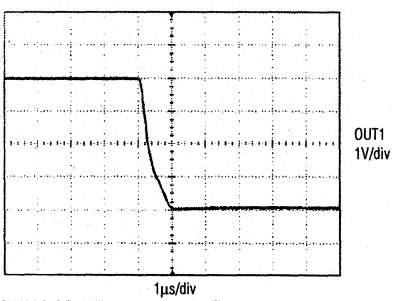


MAX521
POSITIVE SETTLING TIME



OUT1 LOADED WITH 10kΩ II 100pF, REF1 = 4V,
DAC CODE = 00 HEX to FF HEX

MAX521
NEGATIVE SETTLING TIME



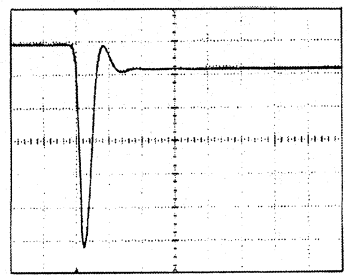
OUT1 LOADED WITH 10kΩ II 100pF, REF1 = 4V,
DAC CODE = FF HEX to 00 HEX

Quad/Octal, 2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

Typical Operating Characteristics (continued)

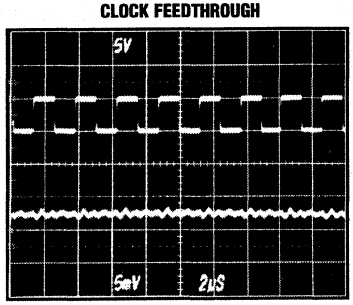
(V_{DD} = 5V, DAC outputs unloaded, T_A = +25°C, unless otherwise noted.)

MAX521
WORST-CASE 1LSB DIGITAL STEP CHANGE



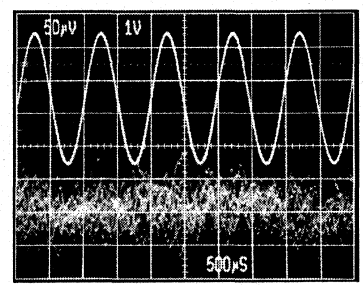
REF1 = 5V, DAC CODE = 80 HEX to 7F HEX

CLOCK FEEDTHROUGH



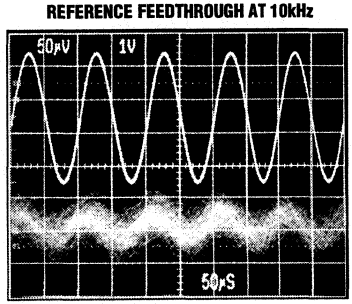
A = SCL, 400kHz, 5V/div
B = OUT1, 5mV/div
REF1 = 5V, DAC CODE = 7F HEX

REFERENCE FEEDTHROUGH AT 1kHz



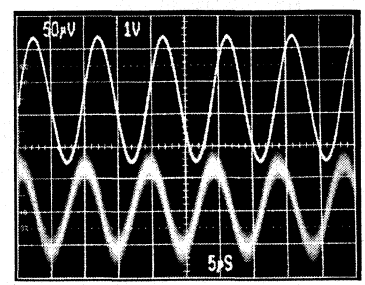
A = REF1, 1V/div ($4V_{P-P}$)
B = OUT1, 50µV/div, UNLOADED
FILTER PASSBAND = 100Hz to 10kHz, DAC CODE = 00 HEX

REFERENCE FEEDTHROUGH AT 10kHz



A = REF1, 1V/div ($4V_{P-P}$)
B = OUT1, 50µV/div, UNLOADED
FILTER PASSBAND = 1kHz to 100kHz, DAC CODE = 00 HEX

REFERENCE FEEDTHROUGH AT 100kHz



A = REF1, 1V/div ($4V_{P-P}$)
B = OUT1, 50µV/div, UNLOADED
FILTER PASSBAND = 10kHz to 1MHz, DAC CODE = 00 HEX

Pin Description

PIN				NAME	FUNCTION
MAX520		MAX521			
DIP/SO	SSOP	DIP	SO/SSOP		
1	1	1	1	OUT1	DAC1 Voltage Output
2	2	2	2	OUT0	DAC0 Voltage Output
3	3	3	3	REF1	Reference Voltage Input for DAC1
4	5	4	4	REF0	Reference Voltage Input for DAC0
—	4, 7, 14, 17	—	7, 9, 16, 20	N.C.	No Connect—not internally connected
6	8	5	5	DGND	Digital Ground
5	6	6	6	AGND	Analog Ground
7	9	7	8	SCL	Serial Clock Input
8	10	8	10	SDA	Serial Data Input
—	—	9	11	OUT4	DAC4 Voltage Output
—	—	10	12	OUT5	DAC5 Voltage Output
—	—	11	13	OUT6	DAC6 Voltage Output
—	—	12	14	OUT7	DAC7 Voltage Output
9	11	13	15	AD0	Address Input 0; sets IC's slave address
10	12	14	17	AD1	Address Input 1; sets IC's slave address
11	13	—	—	AD2	Address Input 2; sets IC's slave address
12	15	15	18	V_{DD}	Power Supply, +5V
—	—	16	19	REF4	Reference Voltage Input for DACs 4, 5, 6, and 7
13	16	17	21	REF3	Reference Voltage Input for DAC3
14	18	18	22	REF2	Reference Voltage Input for DAC2
15	19	19	23	OUT3	DAC3 Voltage Output
16	20	20	24	OUT2	DAC2 Voltage Output

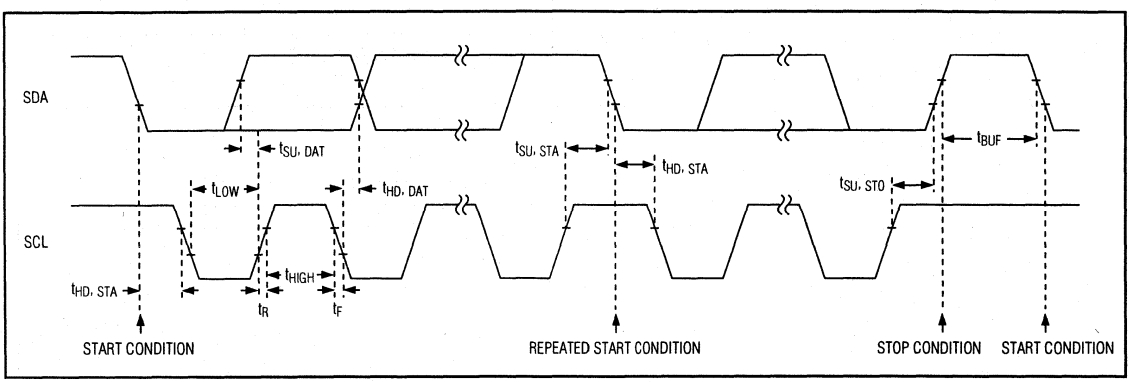


Figure 1. 2-Wire Serial-Interface Timing Diagram

Quad/Octal, 2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

Detailed Description

Serial Interface

The MAX520/MAX521 use a simple 2-wire serial interface requiring only two I/O lines (2-wire bus) of a standard microprocessor (µP) port. Figure 1 shows the timing diagram for signals on the 2-wire bus. Figure 2 shows the typical application of the MAX520/MAX521. The 2-wire bus can have several devices (in addition to the MAX520/MAX521) attached. The two bus lines (SDA and SCL) must be high when the bus is not in use. When in use, the port bits are toggled to generate the appropriate signals for SDA and SCL. External pull-up resistors are not required on these lines. The MAX520/MAX521 can be used in applications where pull-up resistors are required (such as in I²C systems) to maintain compatibility with the existing circuitry.

The MAX520/MAX521 are receive-only devices and must be controlled by a bus master device. They operate at SCL rates up to 400kHz. A master device sends information to the devices by transmitting their address over the bus and then transmitting the desired information. Each transmission consists of a START condition, the MAX520/MAX521's programmable slave-address, one or more command-byte/output-byte pairs (or a command byte alone, if it is the last byte in the transmission), and finally, a STOP condition (Figure 3).

The address byte and pairs of command and output bytes are transmitted between the START and STOP conditions. The SDA state is allowed to change only while SCL is low. SDA's state is sampled, and therefore must remain stable while SCL is high. The only exceptions to this are the START and STOP conditions. Data is transmitted in 8-bit bytes. Nine clock cycles are required to transfer the data bits to the MAX520/MAX521. Set SDA low during the 9th clock cycle as the MAX520/MAX521 pull SDA low during this time. R_C (Figure 2) limits the current that flows during this time if SDA stays high for short periods of time.

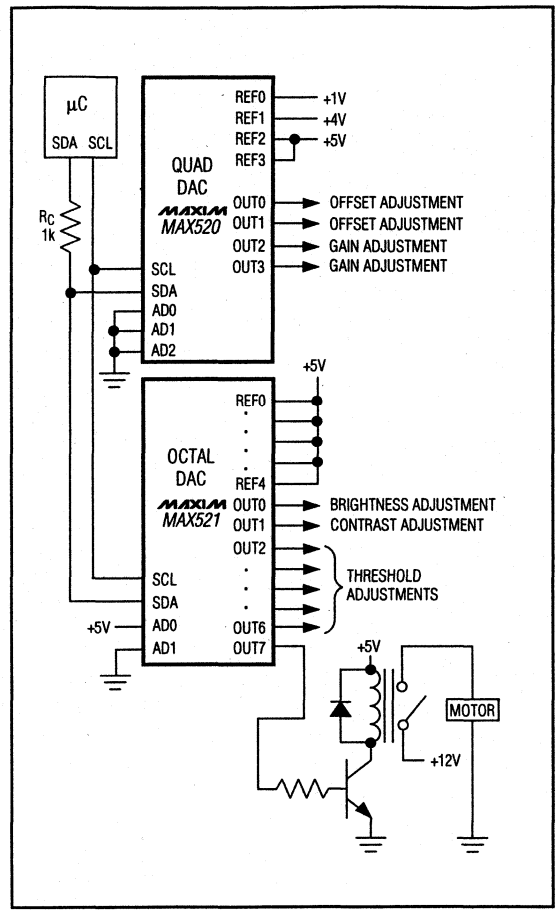


Figure 2. Typical Application Circuit

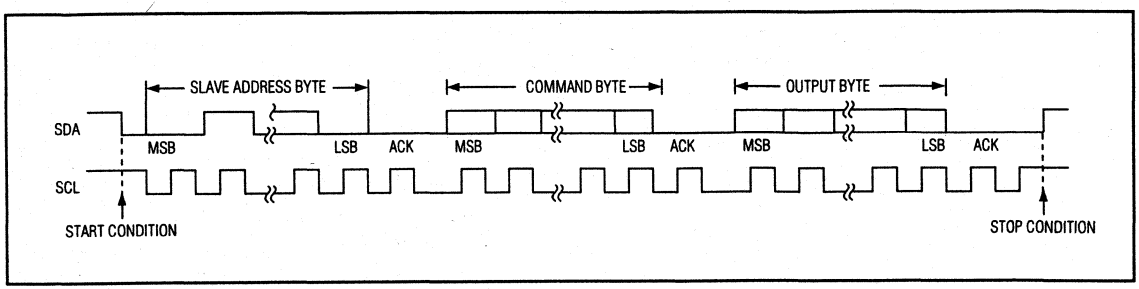


Figure 3. A Complete Serial Transmission

START and STOP Conditions

When the bus is not in use, both SCL and SDA must be high. A bus master signals the beginning of a transmission with a START condition by transitioning SDA from high to low while SCL is high (Figure 4). When the master has finished communicating with the slave, it issues a STOP condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

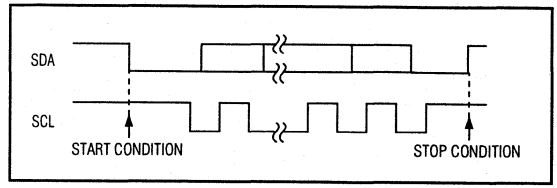


Figure 4. All communications begin with a START condition and end with a STOP condition, both generated by a bus master.

Slave Address

The MAX520/MAX521 each have a 7-bit-long slave address (Figure 5). The first four bits (MSBs) of the slave address have been factory programmed and are always 0101. In addition, the MAX521 has the next bit factory programmed to 0. The logic state of the address input pins (AD0, AD1, and AD2 of the MAX520; AD0 and AD1 of the MAX521) determine the least significant bits of the 7-bit slave address. These input pins may be connected to V_{DD} or DGND, or they may be actively driven by TTL or CMOS logic levels. There are four possible slave addresses for the MAX521, and therefore a maximum of four such devices may be on the bus at one time. The MAX520 has eight possible slave addresses. The eighth bit (LSB) in the slave address byte should be low when writing to the MAX520/MAX521.

The MAX520/MAX521 monitor the bus continuously, waiting for a START condition followed by its slave address. When a device recognizes its slave address, it is ready to accept data.

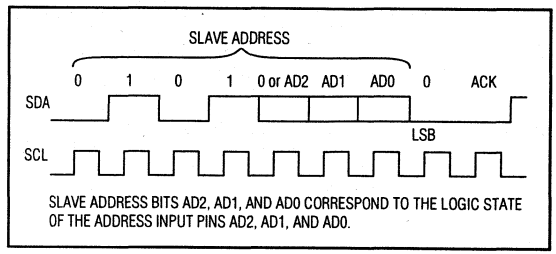


Figure 5. Address Byte

Command Byte and Output Byte

A command byte follows the slave address. Figure 6 shows the format for the command byte. A command byte is usually followed by an output byte unless it is the last byte in the transmission. If it is the last byte, all bits except PD and RST are ignored. If an output byte follows the command byte, A0–A2 of the command byte indicate the digital address of the DAC whose input data latch receives the digital output data. The data is transferred to the DAC's output latch during the STOP condition following the transmission. This allows all DACs to be updated and the new outputs to appear simultaneously (Figure 7).

Setting the PD bit high powers down the MAX520/MAX521 following a STOP condition (Figure 8a). If a command byte with PD set high is followed by an output byte, the addressed DAC's input latch will be updated and the data will be transferred to the DAC's output latch following the STOP condition (Figure 8b). If the transmission's last command byte has PD high, the voltage outputs will not reflect the newly entered data because the DAC will enter power-down mode when

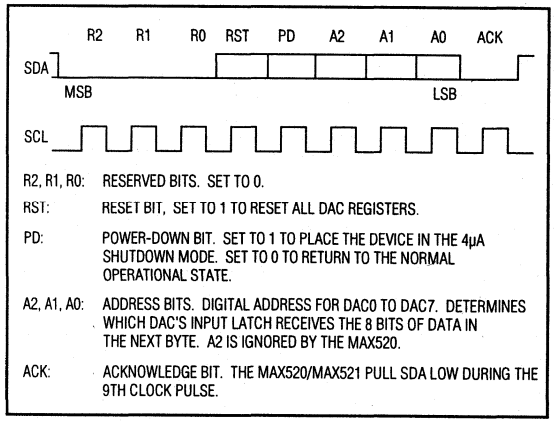


Figure 6. Command Byte

the STOP condition is detected. When in power-down, the MAX521's DAC outputs float, and the MAX520's unbuffered outputs look like a 16kΩ resistor to AGND. In this mode, the supply current is a maximum of 20µA. A command byte with the PD bit low returns the MAX520/MAX521 to normal operation following a STOP condition, and the voltage outputs reflect the current output-latch contents (Figures 9a and 9b). Because each subsequent command byte overwrites the previous PD bit, only the last command byte of a transmission affects the power-down state.

Quad/Octal, 2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

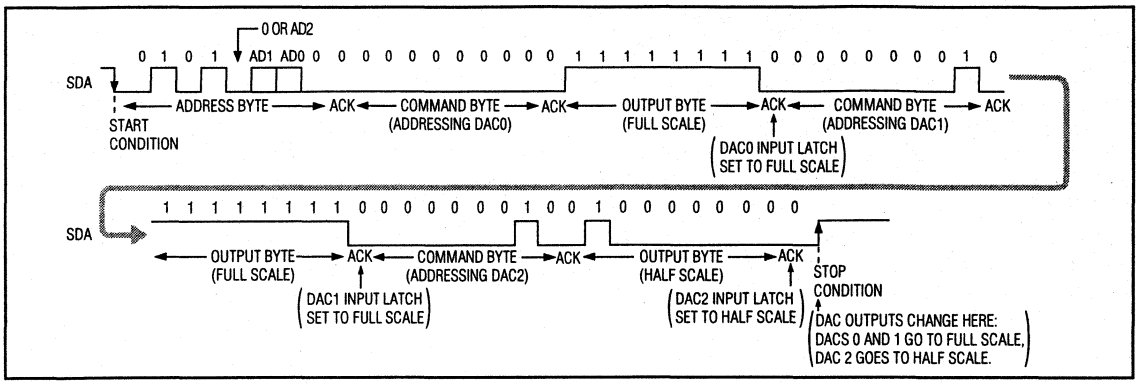


Figure 7. Setting DAC Outputs

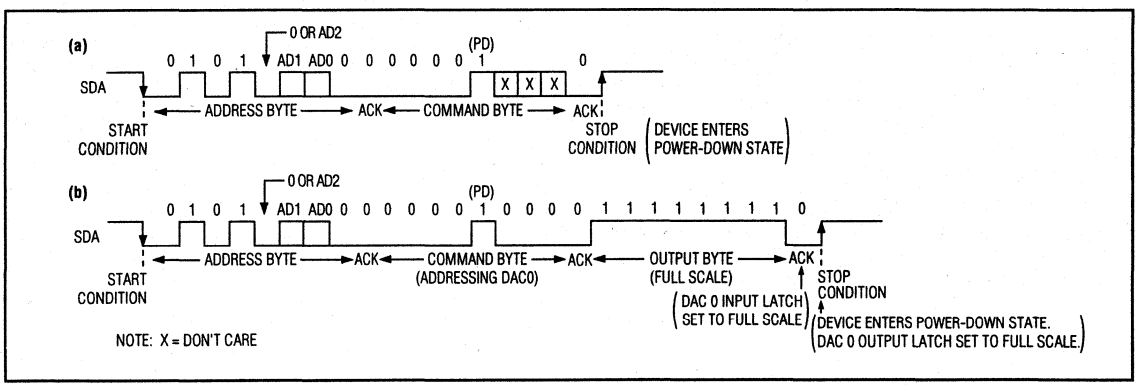


Figure 8. Entering the Power-Down State

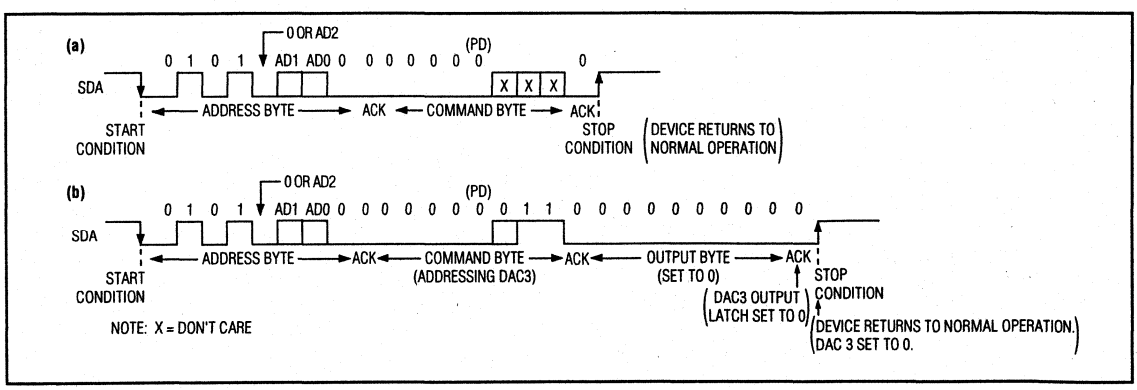


Figure 9. Returning to Normal Operation from Power-Down

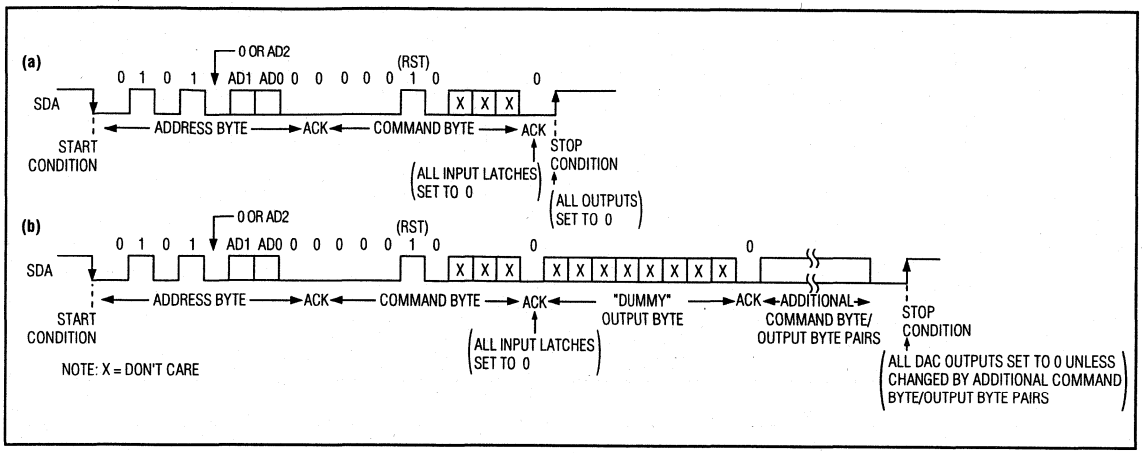


Figure 10. Resetting DAC Outputs

Setting the RST bit high clears all DAC input latches. The DAC outputs remain unchanged until a STOP condition is detected (Figure 10a). If a reset is issued, the following output byte is ignored. Subsequent pairs of command/output bytes overwrite the input latches (Figure 10b).

All changes made during a transmission affect the MAX520/MAX521's outputs only when the transmission ends and a STOP has been recognized. The R0, R1, and R2 bits are reserved bits that must be set to zero.

I²C Compatibility

The MAX520/MAX521 are fully compatible with existing I²C systems. SCL and SDA are high-impedance inputs; SDA has an open drain which pulls the data line low during the 9th clock pulse. Figure 11 shows a typical I²C application.

Additional START Conditions

It is possible to interrupt a transmission to a MAX520/MAX521 with a new START (repeated start) condition (perhaps addressing another device), which leaves the input latches with data that has not been transferred to the output latches (Figure 12). Only the currently addressed device will recognize a STOP condition and transfer data to its output latches. If the device is left with data in its input latches, the data can be transferred to the output latches the next time the device is addressed, as long as it receives at least one command byte and a STOP condition.

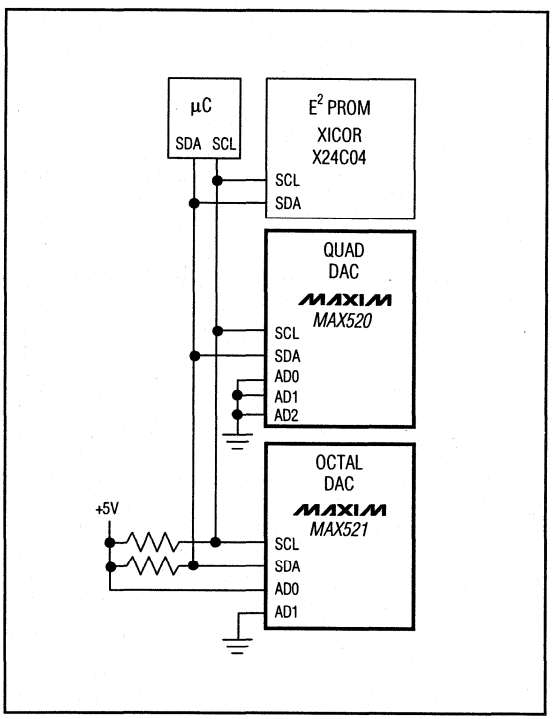


Figure 11. Typical I²C Application Circuit

Quad/Octal, 2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

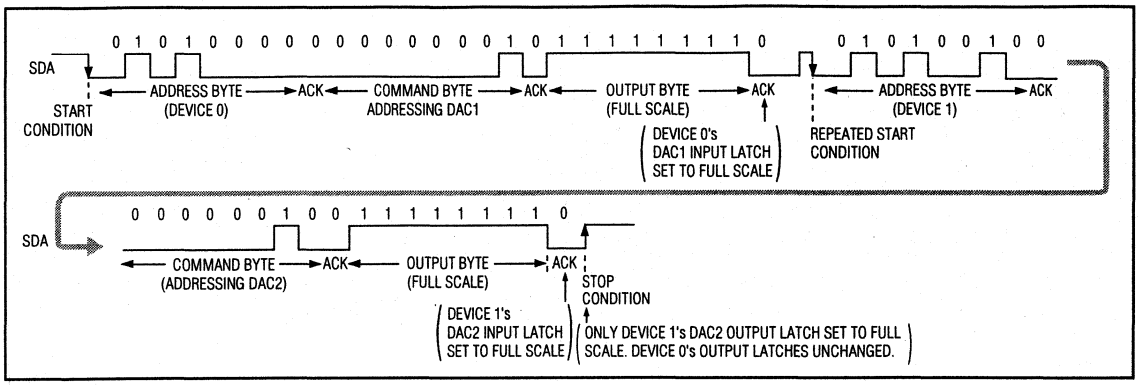


Figure 12. Repeated START Conditions

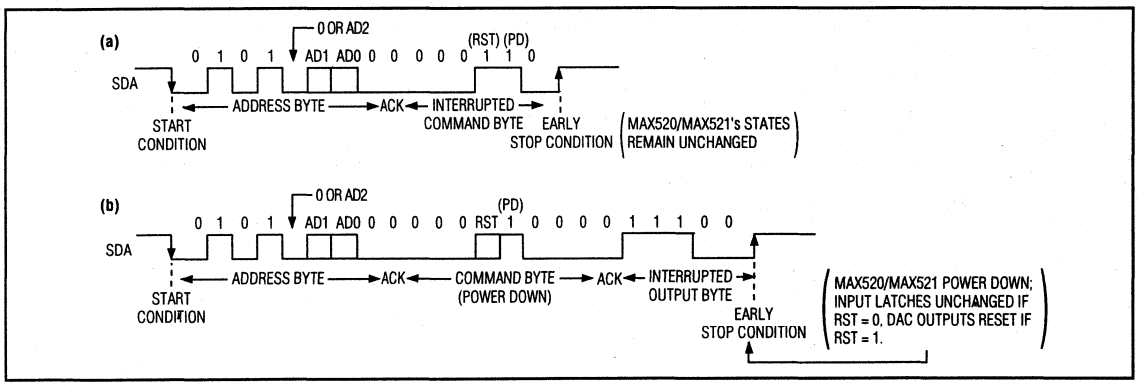


Figure 13. Early STOP Conditions

Early Stop Conditions

The addressed device recognizes a STOP condition at any point in a transmission. If the STOP occurs during a command byte, all previous uninterrupted command and output byte pairs are accepted, the interrupted command byte is ignored, and the transmission ends (Figure 13a). If the STOP occurs during an output byte, all previous uninterrupted command and output byte pairs are accepted, the final command byte's PD and RST bits are accepted, the interrupted output byte is ignored, and the transmission ends (Figure 13b).

Analog Section

DAC Operation

The MAX520 contains four matched voltage-output DACs, and the MAX521 contains eight. The DACs are inverted R-2R ladder networks that convert 8-bit digital words into equivalent analog output voltages in proportion to the applied reference voltages. For both devices, DAC0–DAC3 each have separate reference inputs, while the MAX521's DAC4–DAC7 all share a common reference input. Figure 14 shows a simplified diagram of one DAC.

Reference Inputs

The MAX520/MAX521 can be used for multiplying applications. The reference accepts a 0V to V_{DD} voltage, both DC and AC signals. The voltage at each REF input sets the full-scale output voltage for its respective DAC(s). The reference voltage must be positive. The DAC's input impedance is code dependent, with the lowest value occurring when the input code is 55 hex or 0101 0101, and the maximum value occurring when the input code is 00 hex. Since the REF input resistance

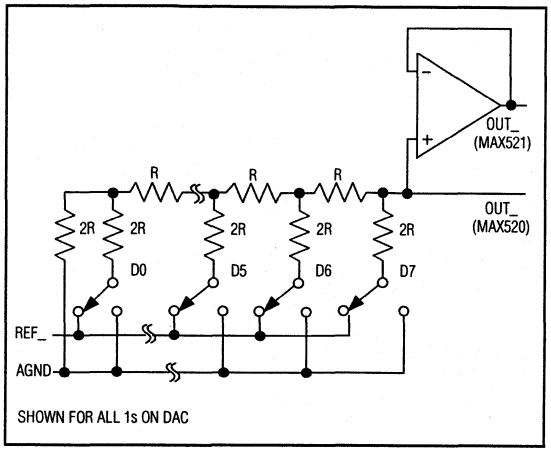


Figure 14. DAC Simplified Circuit Diagram

(R_{IN}) is code dependent, it must be driven by a circuit with low output impedance (no more than $R_{IN} \div 2000$) to maintain output linearity. The REF input capacitance is also code dependent, with the maximum value occurring at code FF hex (typically 30pF for the MAX520/MAX521's REF0–REF3, and 120pF for the MAX521's REF4). The output voltage for any DAC can be represented by a digitally programmable voltage source as: $V_{OUT} = (N \times V_{REF}) / 256$, where N is the numerical value of the DAC's binary input code. Table 1 shows the unipolar code.

Table 1. Unipolar Code Table

DAC CONTENTS	ANALOG OUTPUT
11111111	$+ V_{REF}\left(\frac{255}{256}\right)$
10000001	$+ V_{REF}\left(\frac{129}{256}\right)$
10000000	$+ V_{REF}\left(\frac{128}{256}\right) = \frac{V_{REF}}{2}$
01111111	$+ V_{REF}\left(\frac{127}{256}\right)$
00000001	$+ V_{REF}\left(\frac{1}{256}\right)$
00000000	0V

MAX520 Unbuffered DAC Outputs

The unbuffered DAC outputs (OUT0–OUT3) connect directly to the internal 16kΩ R-2R network. The outputs swing from 0V to V_{DD}.

The MAX520 has no output buffer amplifiers, giving it very low supply current. The output-offset voltage is lower without the output buffer, and the output can also slew and settle faster if capacitive loading is minimized. Resistive loading should be very light for highest accuracy. Any output loading generates some gain error, increasing full-scale error. The R-2R ladder's output resistance is 16kΩ, so a 1µA output current creates a 16mV error. Linearity is not affected because the ladder output resistance does not change with DAC code. Ladder-resistance changes with temperature are also very small.

DACs are often used in trimming applications to replace hardware potentiometers. Figure 15a shows a typical application, which requires a buffered output so that a precise current can be injected into the summing node through precision resistor R_T. For this application, the MAX520A features a precise ±1% (T_A = +25°C, ±2.5% over temperature) factory-trimmed output resistance. Because the MAX520A's output resistance is precisely trimmed, there is no need for an internal buffer or external precision resistor (Figure 15b). For applications where the output resistance value is not critical, use the MAX520B.

All DACs exhibit output glitches during code transitions. An output filter is sometimes used to reduce these glitches in sensitive applications. The MAX520 simplifies output filtering because its internal resistive ladder network serves as the "R" in an RC filter. Simply connect a small capacitor from the DAC output to ground. See the *Typical Operating Characteristics* for oscilloscope photos of the worst-case 1LSB step change both without and with 25pF of capacitance on the MAX520's output.

MAX521 Output Buffer Amplifiers

The MAX521 voltage outputs (OUT0–OUT7) are internally buffered precision unity-gain followers that slew up to 1V/µs. The outputs can swing from 0V to V_{DD}. With a 0V to 4V (or 4V to 0V) output transition, the amplifier outputs typically settle to 1/2LSB in 6µs when loaded with 10kΩ in parallel with 100pF. The buffer amplifiers are stable with any combination of resistive loads ≥2kΩ and capacitive loads ≤300pF.

Quad/Octal, 2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

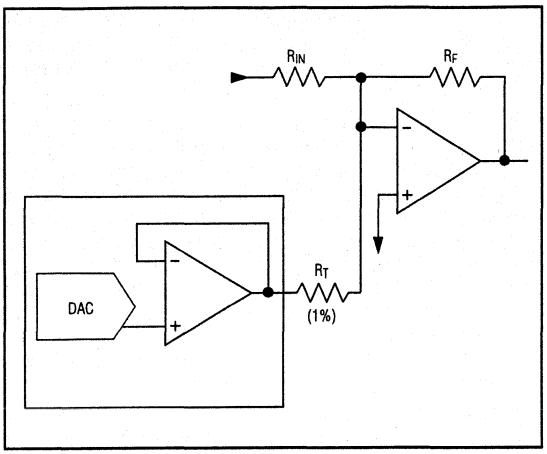


Figure 15a. Typical Trimming Circuit

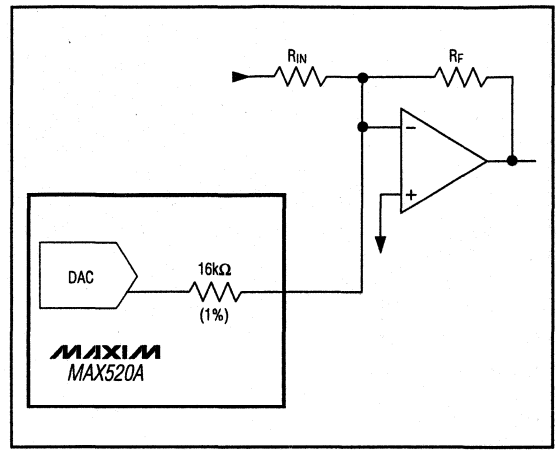


Figure 15b. MAX520A Trimming Circuit

Applications Information

Shutdown Mode

In shutdown mode, the MAX520/MAX521 reference inputs are disconnected from the R-2R ladder inputs, which saves power when the reference is not powered down. In addition, the MAX521's output buffers are disabled, greatly reducing the supply current. The MAX520's operating supply current does not change in shutdown mode. The *Command Byte and Output Byte* section describes how to enter and exit shutdown mode.

Power-Supply Bypassing and Ground Management

Bypass V_{DD} with a 0.1µF capacitor, located as close to V_{DD} and DGND as possible. The analog ground (AGND) and digital ground (DGND) pins should be connected in a "star" configuration to the highest quality ground available, which should be located as close to the MAX521 as possible.

Careful PC board layout minimizes crosstalk among DAC outputs, reference inputs, and digital inputs. Figure 16 shows the suggested PC board layout to minimize crosstalk.

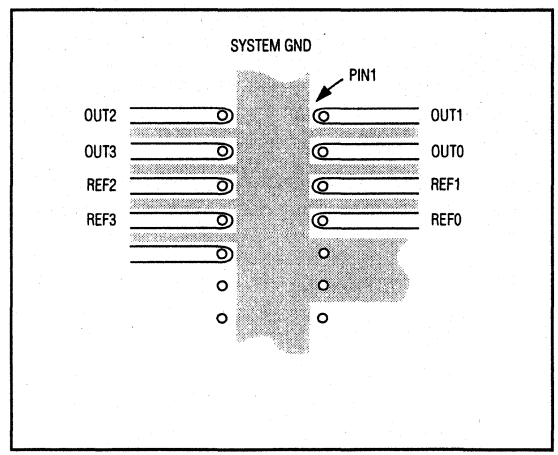
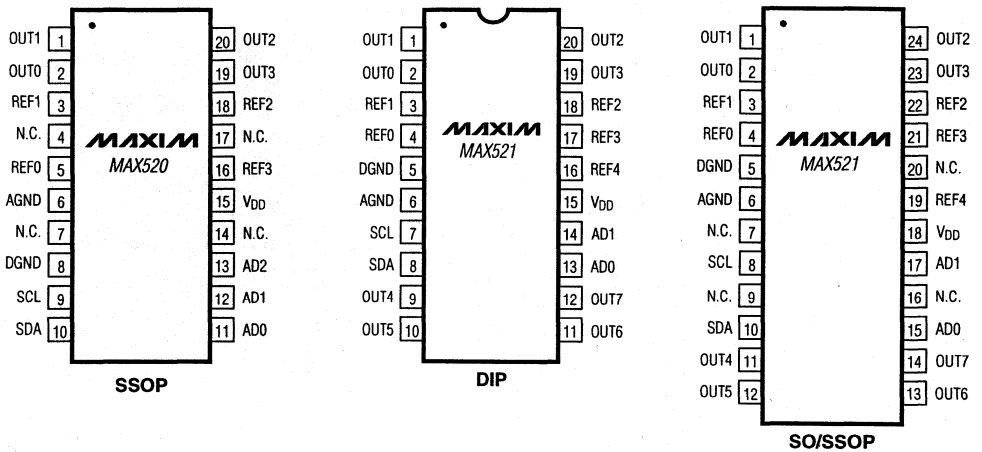


Figure 16. PC Board Layout for Minimizing Crosstalk (MAX521 bottom view, DIP package)

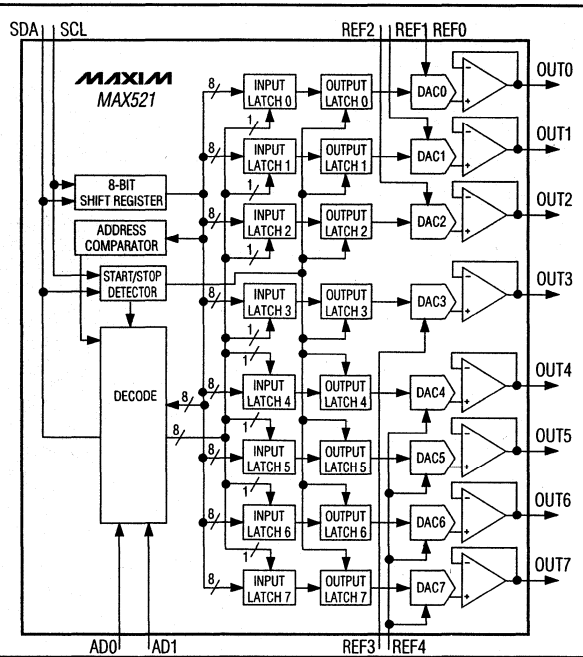
Quad/Octal, 2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

Pin Configurations (continued)

TOP VIEW



Functional Diagrams (continued)



Quad/Octal, 2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

Ordering Information (continued)

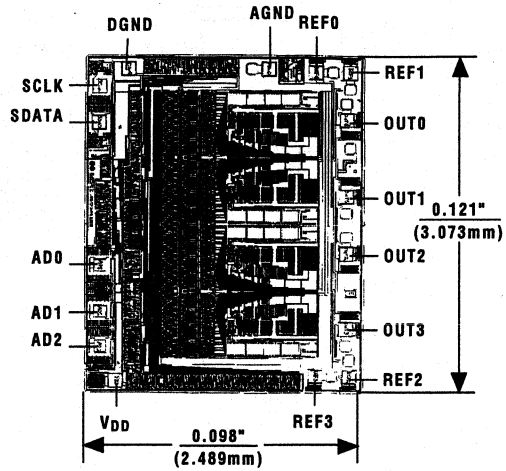
PART†	TEMP. RANGE	PIN-PACKAGE	TUE (LSB)
MAX520ACAP	0°C to +70°C	20 SSOP	1
MAX520BCAP	0°C to +70°C	20 SSOP	1
MAX520AC/D	0°C to +70°C	Dice*	1
MAX520BC/D	0°C to +70°C	Dice*	1
MAX520AEPE	-40°C to +85°C	16 Plastic DIP	1
MAX520BEPE	-40°C to +85°C	16 Plastic DIP	1
MAX520AEWE	-40°C to +85°C	16 Wide SO	1
MAX520BEWE	-40°C to +85°C	16 Wide SO	1
MAX520AEAP	-40°C to +85°C	20 SSOP	1
MAX520BEAP	-40°C to +85°C	20 SSOP	1
MAX520AMJE	-55°C to +125°C	16 CERDIP	1
MAX520BMJE	-55°C to +125°C	16 CERDIP	1
MAX521ACPP	0°C to +70°C	20 Plastic DIP	1
MAX521BCPP	0°C to +70°C	20 Plastic DIP	2
MAX521ACWG	0°C to +70°C	24 Wide SO	1
MAX521BCWG	0°C to +70°C	24 Wide SO	2
MAX521ACAG	0°C to +70°C	24 SSOP	1
MAX521BCAG	0°C to +70°C	24 SSOP	2
MAX521BC/D	0°C to +70°C	Dice*	2
MAX521AEPP	-40°C to +85°C	20 Plastic DIP	1
MAX521BEPP	-40°C to +85°C	20 Plastic DIP	2
MAX521AEWG	-40°C to +85°C	24 Wide SO	1
MAX521BEWG	-40°C to +85°C	24 Wide SO	2
MAX521AEAG	-40°C to +85°C	24 SSOP	1
MAX521BEAG	-40°C to +85°C	24 SSOP	2
MAX521BMJP	-55°C to +125°C	20 CERDIP	2

** Dice are specified at T_A = +25°C, DC parameters only.*

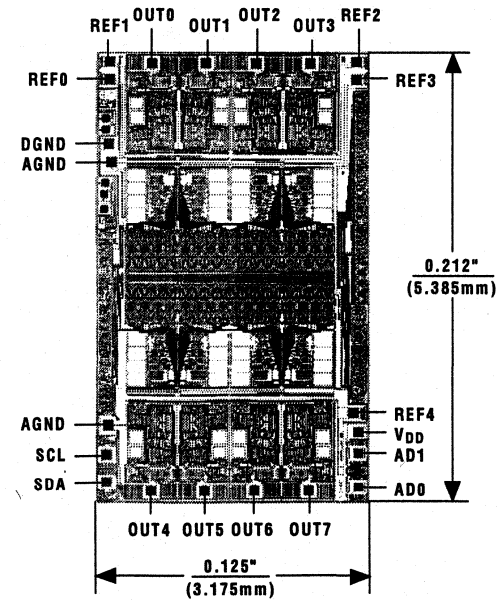
† MAX520 "A" grade parts include a 1%-accurate, factory-trimmed output resistance.

Chip Topographies

MAX520



MAX521



TRANSISTOR COUNT: 4518
SUBSTRATE CONNECTED TO V_{DD}

19-1098; Rev 0; 6/96

MAXIM

Low-Power, Quad, 12-Bit Voltage-Output DAC with Serial Interface

General Description

The MAX525 combines four low-power, voltage-output, 12-bit digital-to-analog converters (DACs) and four precision output amplifiers in a space-saving, 20-pin package. In addition to the four voltage outputs, each amplifier's negative input is also available to the user. This facilitates specific gain configurations, remote sensing, and high output drive capacity, making the MAX525 ideal for industrial-process-control applications. Other features include software shutdown, hardware shutdown lockout, an active-low reset which clears all registers and DACs to zero, a user-programmable logic output, and a serial-data output.

Each DAC has a double-buffered input organized as an input register followed by a DAC register. A 16-bit serial word loads data into each input/DAC register. The serial interface is compatible with SPI™/QSPI™ and Microwire™. It allows the input and DAC registers to be updated independently or simultaneously with a single software command. The DAC registers can be simultaneously updated via the 3-wire serial interface. All logic inputs are TTL/CMOS-logic compatible.

Applications

Industrial Process Controls
Automatic Test Equipment
Digital Offset and Gain Adjustment
Motion Control
Remote Industrial Controls
Microprocessor-Controlled Systems

Features

- ♦ **Four 12-Bit DACs with Configurable Output Amplifiers**
- ♦ **+5V Single-Supply Operation**
- ♦ **Low Supply Current: 0.85mA Normal Operation**
  10µA Shutdown Mode
- ♦ **Available in 20-Pin SSOP**
- ♦ **Power-On Reset Clears all Registers and DACs to Zero**
- ♦ **Capable of Recalling Last State Prior to Shutdown**
- ♦ **SPI/QSPI and Microwire Compatible**
- ♦ **Simultaneous or Independent Control of DACs via 3-Wire Serial Interface**
- ♦ **User-Programmable Digital Output**

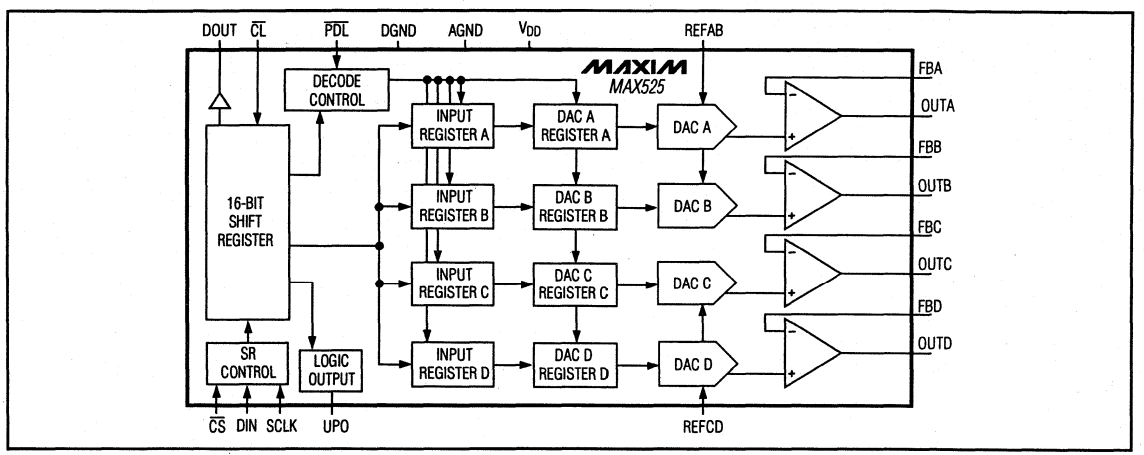
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX525ACPP	0°C to +70°C	20 Plastic DIP	±1/2
MAX525BCPP	0°C to +70°C	20 Plastic DIP	±1
MAX525ACAP	0°C to +70°C	20 SSOP	±1/2
MAX525BCAP	0°C to +70°C	20 SSOP	±1

Ordering Information continued on last page.

Pin Configuration appears at end of data sheet.

Functional Diagram



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Low-Power, Quad, 12-Bit Voltage-Output DAC with Serial Interface

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND .....-0.3V, +6V
V_{DD} to DGND .....-0.3V, +6V
AGND to DGND .....±0.3V
REFAB, REFCD to AGND .....-0.3V to (V_{DD} + 0.3V)
OUT_, FB_ to AGND .....-0.3V to (V_{DD} + 0.3V)
Digital Inputs to DGND .....-0.3V to (V_{DD} + 0.3V)
DOUT, UPO to DGND .....-0.3V to (V_{DD} + 0.3V)
Continuous Current into Any Pin .....±20mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 8.00mW/°C above +70°C) 640mW
SSOP (derate 8.00mW/°C above +70°C) 640mW
CERDIP (derate 11.11mW/°C above +70°C) 889mW

Operating Temperature Ranges
MAX525_C_P .....0°C to +70°C
MAX525_E_P .....-40°C to +85°C
MAX525_MJP .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±10%, AGND = DGND = 0V, REFAB = REFCD = 2.5V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 9).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE—ANALOG SECTION						
Resolution	N		12			Bits
Integral Nonlinearity (Note 1)	INL	MAX525A		±0.25	±0.5	LSB
		MAX525B			±1.0	
Differential Nonlinearity	DNL	Guaranteed monotonic			±1.0	LSB
Offset Error	V_{OS}	T_A = +25°C			±6.0	mV
Offset-Error Tempco				6		ppm/°C
Gain Error (Note 1)	GE			-0.8	±2.0	LSB
Gain-Error Tempco				1		ppm/°C
Power-Supply Rejection Ratio	PSRR	4.5V ≤ V_{DD} ≤ 5.5V		100	600	µV/V
MATCHING PERFORMANCE (T_A = +25°C)						
Gain Error	GE			-0.8	±2.0	LSB
Offset Error				±1.0	±6.0	mV
Integral Nonlinearity	INL			±0.35	±1.0	LSB
REFERENCE INPUT						
Reference Input Range	V_{REF}		0		V_{DD} - 1.4	V
Reference Input Resistance	R_{REF}	Code-dependent, minimum at code 555 hex	10			kΩ
Reference Current in Shutdown				0.01	±1	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±10%, AGND = DGND = 0V, REFAB = REFCD = 2.5V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 9).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MULTIPLYING-MODE PERFORMANCE						
Reference -3dB Bandwidth		V_{REF} = 0.67Vp-p		650		kHz
Reference Feedthrough		Input code = all 0s, V_{REF} = 3.6Vp-p at 1kHz		-84		dB
Signal-to-Noise Plus Distortion Ratio	SINAD	V_{REF} = 1Vp-p at 25kHz		72		dB
DIGITAL INPUTS						
Input High Voltage	V_{IH}		2.4			V
Input Low Voltage	V_{IL}				0.8	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}		0.01	±1.0	µA
Input Capacitance	C_{IN}			8		pF
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}	I_{SOURCE} = 2mA	V_{DD} - 0.5			V
Output Low Voltage	V_{OL}	I_{SINK} = 2mA		0.13	0.4	V
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate	SR			0.6		V/µs
Output Settling Time		To ±1/2LSB, V_{STEP} = 2.5V		12		µs
Output Voltage Swing		Rail to rail (Note 2)		0 to V_{DD}		V
Current into FB_				0	0.1	µA
OUT_ Leakage Current in Shutdown		R_L = ∞		0.01	±1	µA
Start-Up Time Exiting Shutdown Mode				15		µs
Digital Feedthrough		$\overline{CS}$ = V_{DD}, DIN = 100kHz		5		nV-s
Digital Crosstalk				5		nV-s
POWER SUPPLIES						
Supply Voltage	V_{DD}		4.5		5.5	V
Supply Current	I_{DD}	(Note 3)		0.85	0.98	mA
Supply Current in Shutdown		(Note 3)		10	20	µA
Reference Current in Shutdown				0.01	±1	µA

Note 1: Guaranteed from code 11 to code 4095 in unity-gain configuration.
Note 2: Full-scale error is less than 0.5LSB for V_{OUT} = 6mV to V_{DD} - 60mV.
Note 3: R_L = ∞, digital inputs at DGND or V_{DD}.

Low-Power, Quad, 12-Bit Voltage-Output DAC with Serial Interface

ELECTRICAL CHARACTERISTICS (continued)

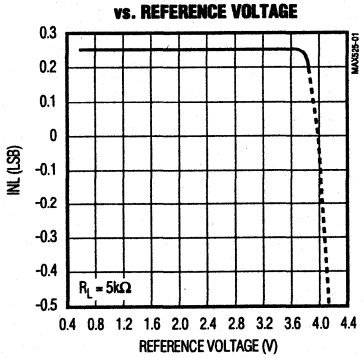
(V_{DD} = +5V ±10%, AGND = DGND = 0V, REFAB = REFCD = 2.5V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 9).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS						
SCLK Clock Period	t_{CP}		100			ns
SCLK Pulse Width High	t_{CH}		40			ns
SCLK Pulse Width Low	t_{CL}		40			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		40			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
DIN Setup Time	t_{DS}		40			ns
DIN Hold Time	t_{DH}		0			ns
SCLK Rise to DOUT Valid Propagation Delay	t_{D01}	C_{LOAD} = 200pF			80	ns
SCLK Fall to DOUT Valid Propagation Delay	t_{D02}	C_{LOAD} = 200pF			80	ns
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CS0}		40			ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	t_{CS1}		40			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		100			ns

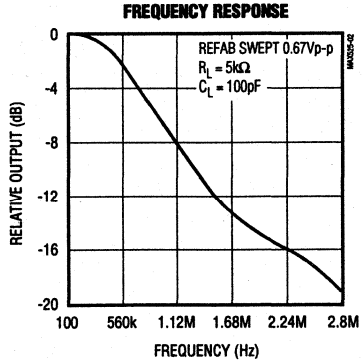
Typical Operating Characteristics

(V_{DD} = +5V, T_A = +25°C, unless otherwise noted.)

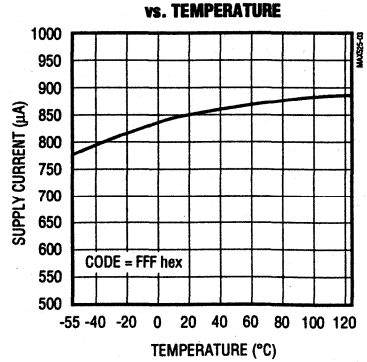
INTEGRAL NONLINEARITY vs. REFERENCE VOLTAGE



REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE



SUPPLY CURRENT vs. TEMPERATURE

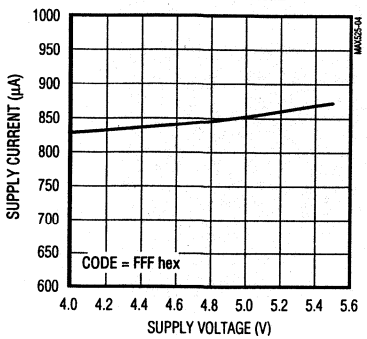


Low-Power, Quad, 12-Bit Voltage-Output DAC with Serial Interface

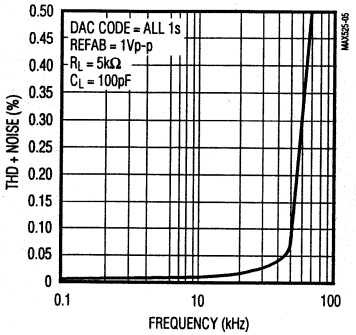
Typical Operating Characteristics (continued)

(V_{DD} = +5V, T_A = +25°C, unless otherwise noted.)

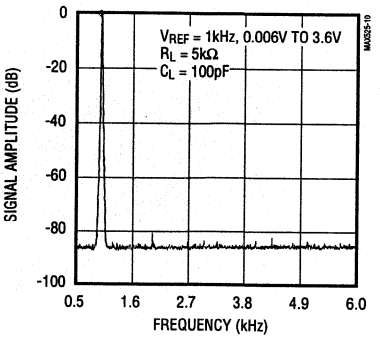
SUPPLY CURRENT vs. SUPPLY VOLTAGE



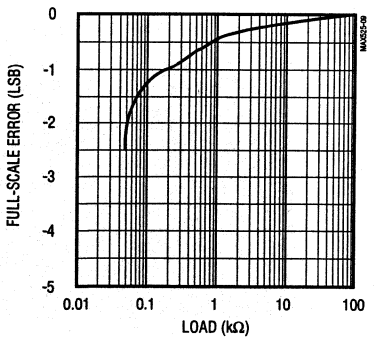
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



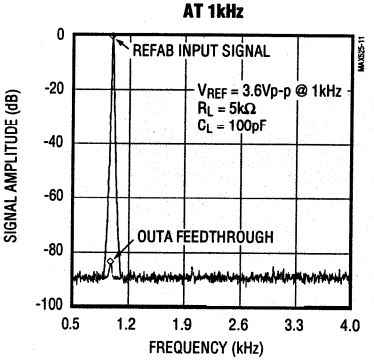
OUTPUT FFT PLOT



FULL-SCALE ERROR vs. LOAD



REFERENCE FEEDTHROUGH AT 1kHz

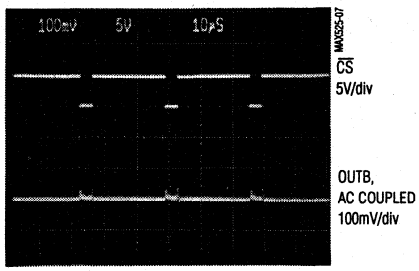


Low-Power, Quad, 12-Bit Voltage-Output DAC with Serial Interface

Typical Operating Characteristics (continued)

(V_{DD} = +5V, T_A = +25°C, unless otherwise noted.)

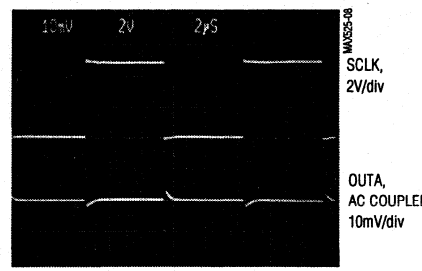
MAJOR-CARRY TRANSITION



10µs/div

V_{REF} = 2.5V, R_L = 5kΩ, C_L = 100pF

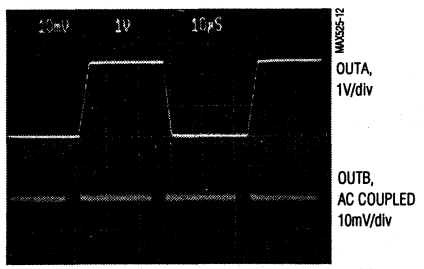
DIGITAL FEEDTHROUGH (SCLK = 100kHz)



2µs/div

V_{REF} = 2.5V, R_L = 5kΩ, C_L = 100pF
$\overline{CS}$ = $\overline{PDL}$ = $\overline{CL}$ = 5V, DIN = 0V
DAC A CODE SET TO 800 hex

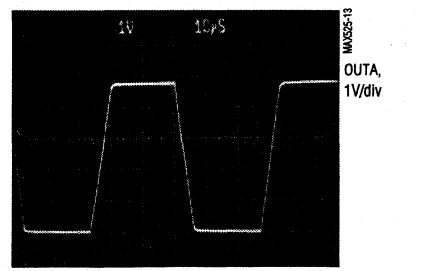
ANALOG CROSSTALK



10µs/div

V_{REF} = 2.5V, R_L = 5kΩ, C_L = 100pF
DAC A CODE SWITCHING FROM 00B hex TO FFF hex
DAC B CODE SET TO 800 hex

DYNAMIC RESPONSE



10µs/div

V_{REF} = 2.5V, R_L = 5kΩ, C_L = 100pF
SWITCHING FROM CODE 000 hex TO FB4 hex
OUTPUT AMPLIFIER GAIN = +2

Pin Description

PIN	NAME	FUNCTION
1	AGND	Analog Ground
2	FBA	DAC A Output Amplifier Feedback
3	OUTA	DAC A Output Voltage
4	OUTB	DAC B Output Voltage
5	FBB	DAC B Output Amplifier Feedback
6	REFAB	Reference Voltage Input for DAC A and DAC B
7	$\overline{CL}$	Clear All DACs and Registers. Resets all outputs (OUT_, UPO, DOUT) to 0, active low.
8	$\overline{CS}$	Chip-Select Input. Active low.
9	DIN	Serial-Data Input
10	SCLK	Serial Clock Input
11	DGND	Digital Ground
12	DOUT	Serial-Data Output
13	UPO	User-Programmable Logic Output
14	$\overline{PDL}$	Power-Down Lockout. Active low. Locks out software shutdown if low.
15	REFCD	Reference Voltage Input for DAC C and DAC D
16	FBC	DAC C Output Amplifier Feedback
17	OUTC	DAC C Output Voltage
18	OUTD	DAC D Output Voltage
19	FBD	DAC D Output Amplifier Feedback
20	V_{DD}	Positive Power Supply

Low-Power, Quad, 12-Bit Voltage-Output DAC with Serial Interface

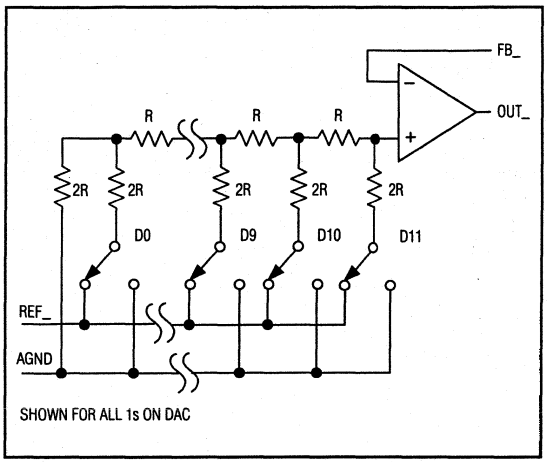


Figure 1. Simplified DAC Circuit Diagram

Detailed Description

The MAX525 contains four 12-bit, voltage-output digital-to-analog converters (DACs) that are easily addressed using a simple 3-wire serial interface. It includes a 16-bit data-in/data-out shift register, and each DAC has a doubled-buffered input composed of an input register and a DAC register (see *Functional Diagram*). In addition to the four voltage outputs, each amplifier's negative input is available to the user.

The DACs are inverted R-2R ladder networks that convert 12-bit digital inputs into equivalent analog output voltages in proportion to the applied reference voltage inputs. DACs A and B share the REFAB reference input, while DACs C and D share the REFCD reference input. The two reference inputs allow different full-scale output voltage ranges for each pair of DACs. Figure 1 shows a simplified circuit diagram of one of the four DACs.

Reference Inputs

The two reference inputs accept positive DC and AC signals. The voltage at each reference input sets the full-scale output voltage for its two corresponding DACs. The reference input voltage range is 0V to (V_{DD} - 1.4V). The output voltages ($V_{OUT_}$) are represented by a digitally programmable voltage source as:

$$V_{OUT_} = (V_{REF} \times NB / 4096) \times Gain$$

where NB is the numeric value of the DAC's binary input code (0 to 4095), V_{REF} is the reference voltage, and Gain is the externally set voltage gain.

The impedance at each reference input is code-dependent, ranging from a low value of 10kΩ when both DACs connected to the reference have an input code of 555 hex, to a high value exceeding several gigohms (leakage currents) with an input code of 000 hex. Because the input impedance at the reference pins is code-dependent, load regulation of the reference source is important.

The REFAB and REFCD reference inputs have a 10kΩ guaranteed minimum input impedance. When the two reference inputs are driven from the same source, the effective minimum impedance is 5kΩ. A voltage reference with a load regulation of 6ppm/mA, such as the MAX873, would typically deviate by 0.025LSB (0.061LSB worst case) when driving both MAX525 reference inputs simultaneously at 2.5V. Driving the REFAB and REFCD pins separately improves reference accuracy.

In shutdown mode, the MAX525's REFAB and REFCD inputs enter a high-impedance state with a typical input leakage current of 0.01µA.

The reference input capacitance is also code dependent and typically ranges from 20pF with an input code of all 0s to 100pF with an input code of all 1s.

Output Amplifiers

All MAX525 DAC outputs are internally buffered by precision amplifiers with a typical slew rate of 0.6V/µs. Access to the inverting input of each output amplifier provides the user greater flexibility in output gain setting/signal conditioning (see the *Applications Information* section).

With a full-scale transition at the MAX525 output, the typical settling time to ±1/2LSB is 12µs when loaded with 5kΩ in parallel with 100pF (loads less than 2kΩ degrade performance).

The MAX525 output amplifier's output dynamic responses and settling performances are shown in the *Typical Operating Characteristics.*

Power-Down Mode

The MAX525 features a software-programmable shutdown that reduces supply current to a typical value of 10µA. The power-down lockout ($\overline{PDL}$) pin must be high to enable the shutdown mode. Writing 1100XXXXXXXXXXXX as the input-control word puts the MAX525 in power-down mode (Table 1).

In power-down mode, the MAX525 output amplifiers and the reference inputs enter a high-impedance state. The serial interface remains active. Data in the input registers is retained in power-down, allowing the MAX525 to recall the output states prior to entering shutdown. Start up from power-down either by recalling the previous configuration or by updating the DACs with new data. When powering up the device or bringing it out of shutdown, allow 15µs for the outputs to stabilize.

Serial-Interface Configurations

The MAX525's 3-wire serial interface is compatible with both Microwire™ (Figure 2) and SPI™/QSPI™ (Figure 3). The serial input word consists of two address bits and two control bits followed by 12 data bits (MSB first), as shown in Figure 4. The 4-bit address/control code determines the MAX525's response outlined in Table 1. The connection between DOUT and the serial-interface port is not necessary, but may be used for data echo. Data held in the MAX525's shift register can be shifted out of DOUT and returned to the microprocessor (µP) for data verification.

The MAX525's digital inputs are double buffered. Depending on the command issued through the serial interface, the input register(s) can be loaded without affecting the DAC register(s), the DAC register(s) can be loaded directly, or all four DAC registers can be updated simultaneously from the input registers (Table 1).

Serial-Interface Description

The MAX525 requires 16 bits of serial data. Table 1 lists the serial-interface programming commands. For certain commands, the 12 data bits are "don't cares." Data is sent MSB first and can be sent in two 8-bit packets or one 16-bit word ($\overline{CS}$ must remain low until 16 bits are transferred). The serial data is composed of two DAC address bits (A1, A0) and two control bits (C1, C0), followed by the 12 data bits D11...D0 (Figure 4). The 4-bit address/control code determines:

- The register(s) to be updated
- The clock edge on which data is to be clocked out via the serial-data output (DOUT)
- The state of the user-programmable logic output (UPO)
- If the part is to go into shutdown mode (assuming $\overline{PDL}$ is high)
- How the part is configured when coming out of shutdown mode.

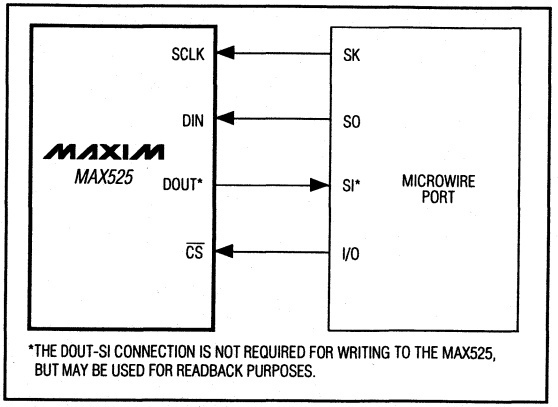


Figure 2. Connections for Microwire

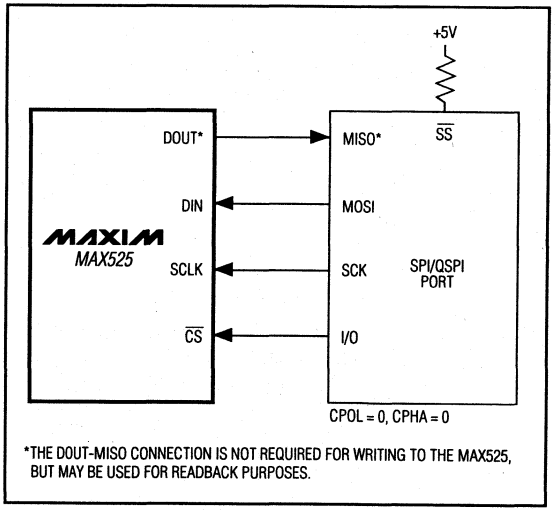


Figure 3. Connections for SPI/QSPI

MSB ..... LSB			
← 16 Bits of Serial Data →			
Address Bits		Control Bits	Data Bits
A1	A0	C1 C0	MSB ..... LSB
			D11 ..... D0
← 4 Address/Control Bits →			← 12 Data Bits →

Figure 4. Serial-Data Format

Low-Power, Quad, 12-Bit Voltage-Output DAC with Serial Interface

Table 1. Serial-Interface Programming Commands

16-BIT SERIAL WORD					FUNCTION
A1	A0	C1	C0	D11.....D0 MSB LSB	
0	0	0	1	12-bit DAC data	Load input register A; DAC registers unchanged.
0	1	0	1	12-bit DAC data	Load input register B; DAC registers unchanged.
1	0	0	1	12-bit DAC data	Load input register C; DAC registers unchanged.
1	1	0	1	12-bit DAC data	Load input register D; DAC registers unchanged.
0	0	1	1	12-bit DAC data	Load input register A; all DAC registers updated.
0	1	1	1	12-bit DAC data	Load input register B; all DAC registers updated.
1	0	1	1	12-bit DAC data	Load input register C; all DAC registers updated.
1	1	1	1	12-bit DAC data	Load input register D; all DAC registers updated.
0	1	0	0	XXXXXXXXXXXX	Update all DAC registers from their respective input registers (start-up).
1	0	0	0	12-bit DAC data	Load all DAC registers from shift register (start-up).
1	1	0	0	XXXXXXXXXXXX	Shutdown (provided $\overline{PDL}$ = 1)
0	0	1	0	XXXXXXXXXXXX	UPO goes low (default)
0	1	1	0	XXXXXXXXXXXX	UPO goes high
0	0	0	0	XXXXXXXXXXXX	No operation (NOP) to DAC registers
1	1	1	0	XXXXXXXXXXXX	Mode 1, DOUT clocked out on SCLK's rising edge. All DAC registers updated.
1	0	1	0	XXXXXXXXXXXX	Mode 0, DOUT clocked out on SCLK's falling edge. All DAC registers updated (default).

"X" = Don't care

Figure 5 shows the serial-interface timing requirements. The chip-select pin ($\overline{CS}$) must be low to enable the DAC's serial interface. When $\overline{CS}$ is high, the interface control circuitry is disabled. $\overline{CS}$ must go low at least t_{CSS} before the rising serial clock (SCLK) edge to properly clock in the first bit. When $\overline{CS}$ is low, data is clocked into the internal shift register via the serial-data input pin (DIN) on SCLK's rising edge. The maximum guaranteed clock frequency is 10MHz. Data is latched into the appropriate MAX525 input/DAC registers on $\overline{CS}$'s rising edge.

The programming command Load-All-DACs-From-Shift-Register allows all input and DAC registers to be simultaneously loaded with the same digital code from the input shift register. The no operation (NOP) command leaves the register contents unaffected and is useful when the MAX525 is configured in a daisy chain (see the *Daisy Chaining Devices* section). The command to change the clock edge on which serial data is shifted out of DOUT also loads data from all input registers to their respective DAC registers.

Serial-Data Output (DOUT)

The serial-data output, DOUT, is the internal shift register's output. The MAX525 can be programmed so that data is clocked out of DOUT on SCLK's rising edge (Mode 1) or falling edge (Mode 0). In Mode 0, output data at DOUT lags input data at DIN by 16.5 clock cycles, maintaining compatibility with Microwire, SPI/QSPI, and other serial interfaces. In Mode 1, output data lags input data by 16 clock cycles. On power-up, DOUT defaults to Mode 0 timing.

User-Programmable Logic Output (UPO)

The user-programmable logic output, UPO, allows an external device to be controlled via the MAX525 serial interface (Table 1).

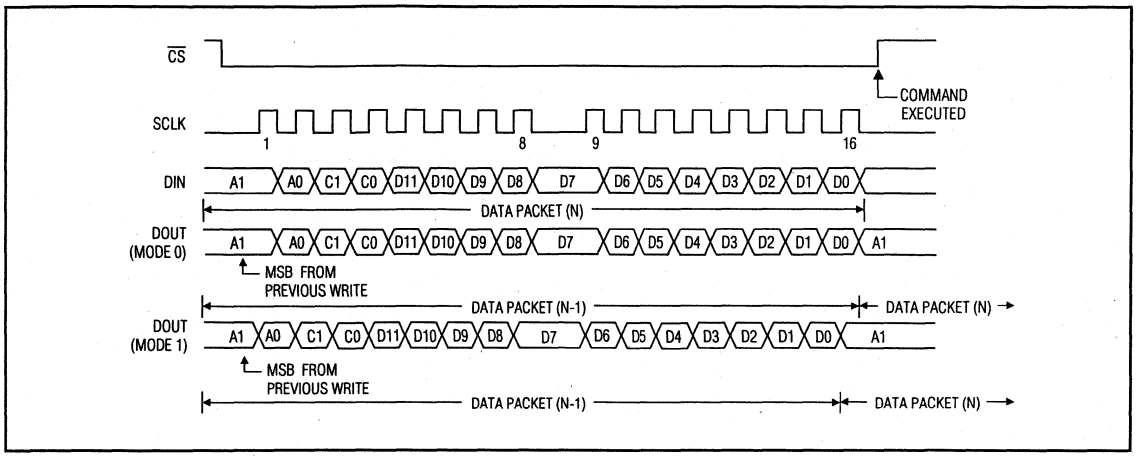


Figure 5. Serial-Interface Timing Diagram

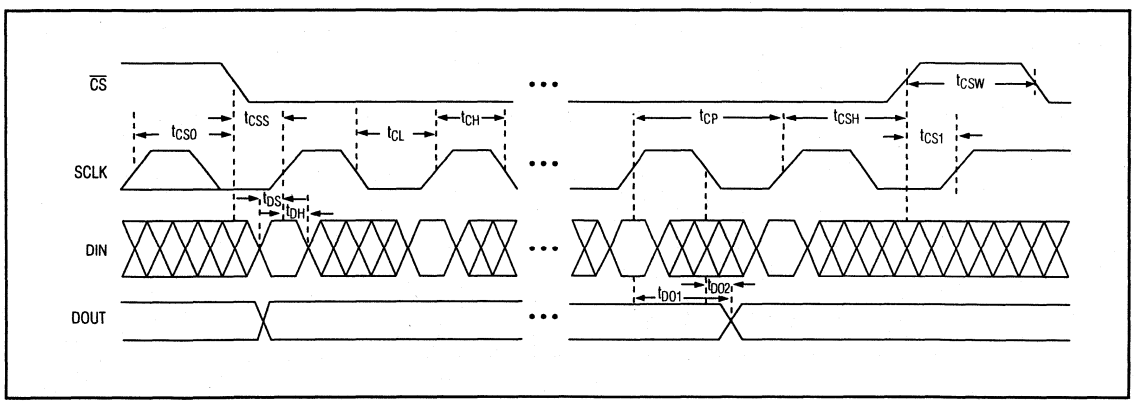


Figure 6. Detailed Serial-Interface Timing Diagram

Power-Down Lockout (PDL)

The power-down lockout pin PDL disables software shutdown when low. When in shutdown, transitioning PDL from high to low wakes up the part with the output set to the state prior to shutdown. PDL could also be used to asynchronously wake up the device.

Daisy Chaining Devices

Any number of MAX525s can be daisy chained by connecting the DOUT pin of one device to the DIN pin of the following device in the chain (Figure 7).

Since the MAX525's DOUT pin has an internal active pull-up, the DOUT sink/source capability determines the time required to discharge/charge a capacitive load. Refer to the serial-data-out V_{OH} and V_{OL} specifications in the *Electrical Characteristics.*

Figure 8 shows an alternate method of connecting several MAX525s. In this configuration, the data bus is common to all devices; data is not shifted through a daisy chain. More I/O lines are required in this configuration because a dedicated chip-select input (CS) is required for each IC.

Low-Power, Quad, 12-Bit Voltage-Output DAC with Serial Interface

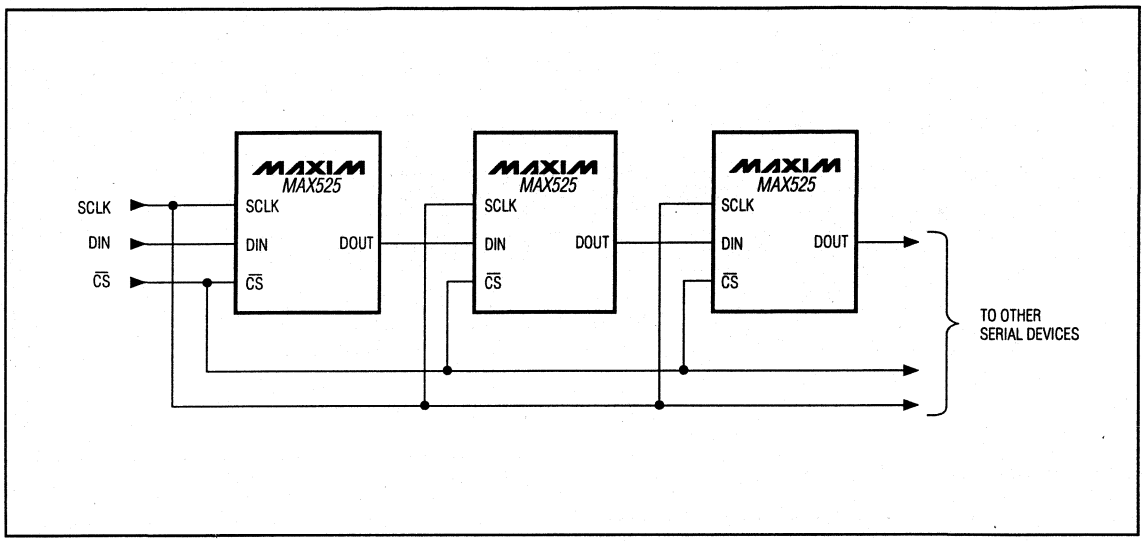


Figure 7. Daisy-Chaining MAX525s

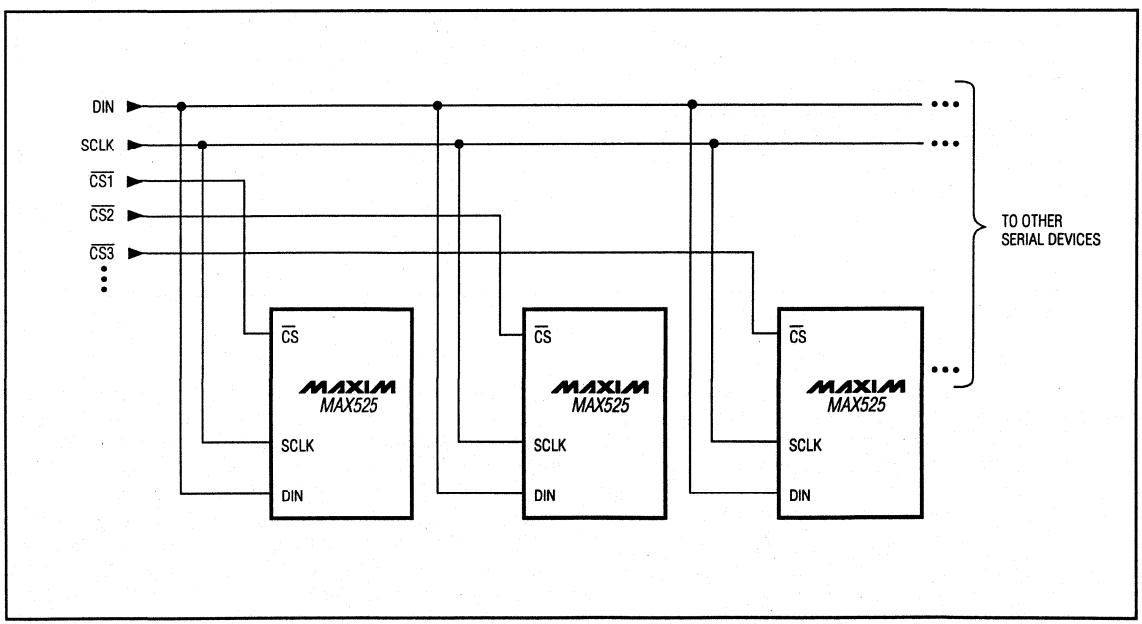


Figure 8. Multiple MAX525s Sharing a Common DIN Line

Applications Information

Unipolar Output

For a unipolar output, the output voltages and the reference inputs have the same polarity. Figure 9 shows the MAX525 unipolar output circuit, which is also the typical operating circuit. Table 2 lists the unipolar output codes.

For rail-to-rail outputs, see Figure 10. This circuit shows the MAX525 with the output amplifiers configured with a closed-loop gain of +2 to provide 0V to 5V full-scale range when a 2.5V reference is used.

Table 2. Unipolar Code Table

DAC CONTENTS MSB		LSB	ANALOG OUTPUT
1111	1111	1111	$+V_{REF}\left(\frac{4095}{4096}\right)$
1000	0000	0001	$+V_{REF}\left(\frac{2049}{4096}\right)$
1000	0000	0000	$+V_{REF}\left(\frac{2048}{4096}\right)=\frac{+V_{REF}}{2}$
0111	1111	1111	$+V_{REF}\left(\frac{2047}{4096}\right)$
0000	0000	0001	$+V_{REF}\left(\frac{1}{4096}\right)$
0000	0000	0000	0V

Table 3. Bipolar Code Table

DAC CONTENTS MSB		LSB	ANALOG OUTPUT
1111	1111	1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000	0000	0001	$+V_{REF}\left(\frac{1}{2048}\right)$
1000	0000	0000	0V
0111	1111	1111	$-V_{REF}\left(\frac{1}{2048}\right)$
0000	0000	0001	$-V_{REF}\left(\frac{2047}{2048}\right)$
0000	0000	0000	$-V_{REF}\left(\frac{2048}{2048}\right)=-V_{REF}$

Note: $1LSB = (V_{REF})\left(\frac{1}{4096}\right)$

Bipolar Output

The MAX525 outputs can be configured for bipolar operation using Figure 11's circuit.

$$V_{OUT} = V_{REF}[(2NB / 4096) - 1]$$

where NB is the numeric value of the DAC's binary input code. Table 3 shows digital codes (offset binary) and corresponding output voltages for Figure 11's circuit.

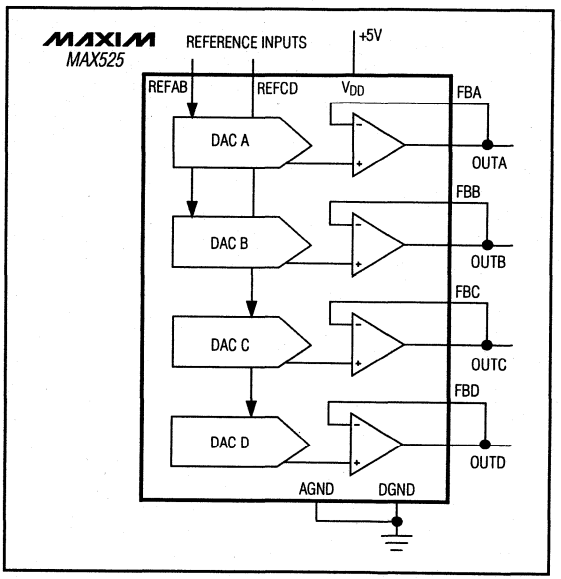


Figure 9. Unipolar Output Circuit

Low-Power, Quad, 12-Bit Voltage-Output DAC with Serial Interface

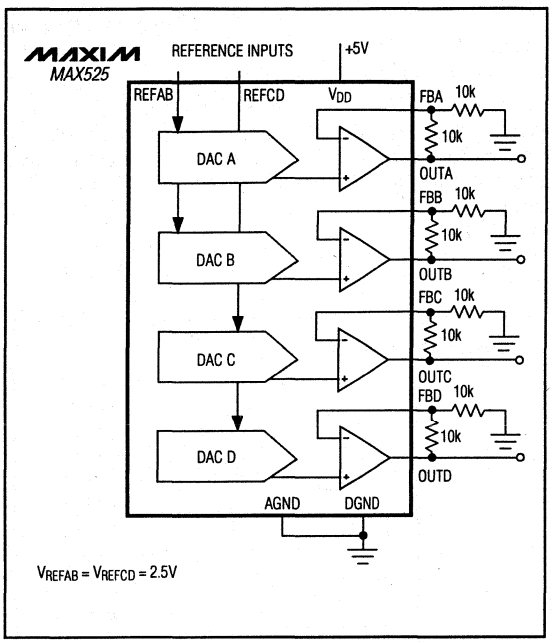


Figure 10. Unipolar Rail-to-Rail Output Circuit

Using an AC Reference

In applications where the reference has AC signal components, the MAX525 has multiplying capability within the reference input range specifications. Figure 12 shows a technique for applying a sine-wave signal to the reference input where the AC signal is offset before being applied to REFAB/REFCD. The reference voltage must never be more negative than DGND.

The MAX525's total harmonic distortion plus noise (THD + N) is typically less than -72dB, given a 1Vp-p signal swing and input frequencies up to 25kHz. The typical -3dB frequency is 650kHz, as shown in the *Typical Operating Characteristics* graphs.

Digitally Programmable Current Source

The circuit of Figure 13 places an NPN transistor (2N3904 or similar) within the op-amp feedback loop to implement a digitally programmable, unidirectional current source. This circuit can be used to drive 4mA to 20mA current loops, which are commonly used in industrial-control applications. The output current is calculated with the following equation:

$$I_{OUT} = (V_{REF} / R) \times (NB / 4096)$$

where NB is the numeric value of the DAC's binary input code and R is the sense resistor shown in Figure 13.

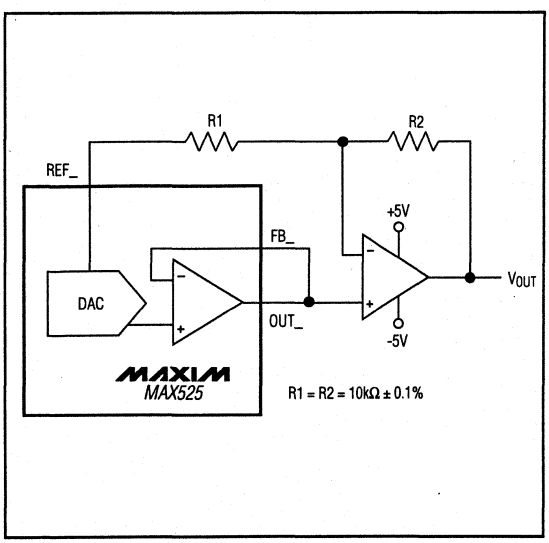


Figure 11. Bipolar Output Circuit

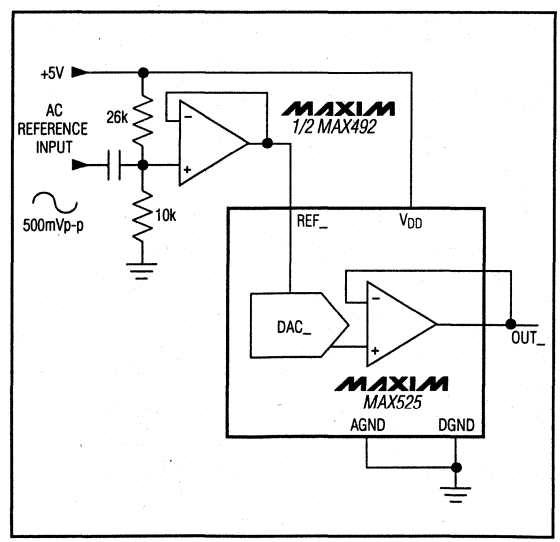


Figure 12. AC Reference Input Circuit

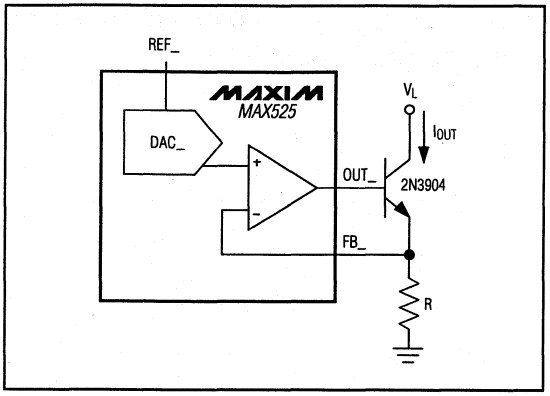


Figure 13. Digitally Programmable Current Source

Power-Supply Considerations

On power-up, all input and DAC registers are cleared (set to zero code) and DOUT is in Mode 0 (serial data is shifted out of DOUT on the clock's falling edge).

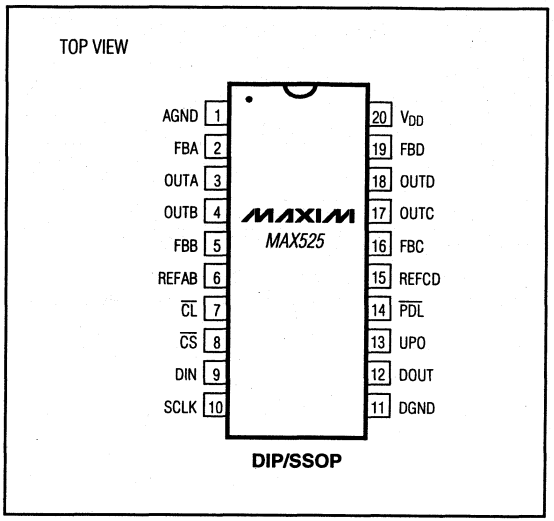
For rated MAX525 performance, limit REFAB/REFCD to less than 1.4V below V_{DD}. Bypass V_{DD} with a 4.7µF capacitor in parallel with a 0.1µF capacitor to AGND. Use short lead lengths and place the bypass capacitors as close to the supply pins as possible.

Grounding and Layout Considerations

Digital or AC transient signals between AGND and DGND can create noise at the analog outputs. Tie AGND and DGND together at the DAC, then tie this point to the highest-quality ground available.

Good printed circuit board ground layout minimizes crosstalk between DAC outputs, reference inputs, and digital inputs. Reduce crosstalk by keeping analog lines away from digital lines. Wire-wrapped boards are not recommended.

Pin Configuration



Low-Power, Quad, 12-Bit Voltage-Output DAC with Serial Interface

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSBs)
MAX525BC/D	0°C to +70°C	Dice*	±1
MAX525AEPP	-40°C to +85°C	20 Plastic DIP	±1/2
MAX525BEPP	-40°C to +85°C	20 Plastic DIP	±1
MAX525AEAP	-40°C to +85°C	20 SSOP	±1/2
MAX525BEAP	-40°C to +85°C	20 SSOP	±1
MAX525AMJP	-55°C to +125°C	20 CERDIP**	±1/2
MAX525BMJP	-55°C to +125°C	20 CERDIP**	±1

** Dice are specified at T_A = +25°C, DC parameters only.*
***Contact factory for availability and processing to MIL-STD-883.*

_____Chip Information

TRANSISTOR COUNT: 4337

19-1080; Rev 0; 6/96

MAXIM

2.7V, Low-Power, 8-Bit Quad DAC with Rail-to-Rail Output Buffers

General Description

The MAX533 serial-input, voltage-output, 8-bit quad digital-to-analog converter (DAC) operates from a single +2.7V to +3.6V supply. Internal precision buffers swing rail to rail, and the reference input range includes both ground and the positive rail. The MAX533 features a 1µA shutdown mode.

The serial interface is double buffered: a 12-bit input shift register is followed by four 8-bit buffer registers and four 8-bit DAC registers. The 12-bit serial word consists of eight data bits and four control bits (for DAC selection and special programming commands). Both the input and DAC registers can be updated independently or simultaneously with a single software command. Two additional asynchronous control pins, $\overline{LDAC}$ and $\overline{CLR}$, provide simultaneous updating or clearing of the input and DAC registers.

The interface is compatible with SPI™, QSPI™ (CPOL = CPHA = 0 or CPOL = CPHA = 1), and Microwire™. A buffered data output allows daisy chaining of serial devices.

In addition to 16-pin DIP and CERDIP packages, the MAX533 is available in a 16-pin QSOP that occupies the same area as an 8-pin SO.

Applications

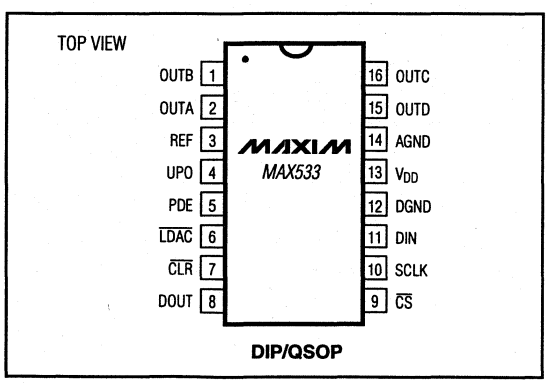
Digital Gain and Offset Adjustments

Programmable Attenuators

Programmable Current Sources

Portable Instruments

Pin Configuration



Features

- ♦ **+2.7V to +3.6V Single-Supply Operation**
- ♦ **Ultra-Low Supply Current:**
  0.7mA while Operating
  1µA in Shutdown Mode
- ♦ **Ultra-Small 16-Pin QSOP Package**
- ♦ **Ground to V_{DD} Reference Input Range**
- ♦ **Output Buffer Amplifiers Swing Rail to Rail**
- ♦ **10MHz Serial Interface, Compatible with SPI, QSPI (CPOL = CPHA = 0 or CPOL = CPHA = 1), and Microwire**
- ♦ **Double-Buffered Registers for Synchronous Updating**
- ♦ **Serial Data Output for Daisy Chaining**
- ♦ **Power-On Reset Clears Serial Interface and Sets All Registers to Zero**
- ♦ **Software Shutdown**
- ♦ **Software-Programmable Logic Output**
- ♦ **Asynchronous Hardware Clear Resets All Internal Registers to Zero**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX533ACPE	0°C to +70°C	16 Plastic DIP	±1
MAX533BCPE	0°C to +70°C	16 Plastic DIP	±2
MAX533ACEE	0°C to +70°C	16 QSOP	±1
MAX533BCEE	0°C to +70°C	16 QSOP	±2
MAX533BC/D	0°C to +70°C	Dice*	±2
MAX533AEPE	-40°C to +85°C	16 Plastic DIP	±1
MAX533BEPE	-40°C to +85°C	16 Plastic DIP	±2
MAX533AEEE	-40°C to +85°C	16 QSOP	±1
MAX533BEEE	-40°C to +85°C	16 QSOP	±2
MAX533AMJE	-55°C to +125°C	16 CERDIP**	±1
MAX533BMJE	-55°C to +125°C	16 CERDIP**	±2

Dice are tested at T_A = +25°C.

***Contact factory for availability and processing to MIL-STD-883.*

Functional Diagram appears at end of data sheet.

SPI and QSPI are trademarks of Motorola, Inc. Microwire is a trademark of National Semiconductor Corp.

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2.7V, Low-Power, 8-Bit Quad DAC with Rail-to-Rail Output Buffers

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND .....-0.3V, +6V
V_{DD} to AGND.....-0.3V, +6V
Digital Input Voltage to DGND .....-0.3V, +6V
Digital Output Voltage to DGND.....-0.3V, (V_{DD} + 0.3V)
AGND to DGND.....±0.3V
REF.....-0.3V, (V_{DD} + 0.3V)
OUT_.....-0.3V, V_{DD}
Maximum Current into Any Pin.....50mA

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
QSOP (derate 8.3mW/°C above +70°C).....667mW
CERDIP (derate 10.00mW/°C above +70°C).....800mW
Operating Temperature Ranges
MAX533 _ C_ E.....0°C to +70°C
MAX533 _ E_ E.....-40°C to +85°C
MAX533 _ MJE.....-55°C to +125°C
Storage Temperature Range.....-65°C to +150°C
Lead Temperature (soldering, 10sec).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +3.6V, V_{REF} = 2.5V, AGND = DGND = 0V, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +3V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC ACCURACY						
Resolution					8	Bits
Integral Nonlinearity (Note 1)	INL	MAX533A			±1	LSB
		MAX533B			±2	
Differential Nonlinearity (Note 1)	DNL	Guaranteed monotonic (all codes)			±1.0	LSB
Zero-Code Error	ZCE	Code = 00 hex			±20	mV
Zero-Code-Error Supply Rejection		Code = 00 hex, V_{DD} = 2.7V to 3.6V			1	LSB
Zero-Code Temperature Coefficient		Code = 00 hex		±10		µV/°C
Full-Scale Error		Code = FF hex			±30	mV
Full-Scale Error Supply Rejection		Code = FF hex, V_{DD} = 2.7V to 3.6V			1	LSB
Full-Scale Temperature Coefficient		Code = FF hex		±10		µV/°C
REFERENCE INPUTS						
Input Voltage Range			0		V_{DD}	V
Input Resistance			322	460	598	kΩ
Input Capacitance				10		pF
Channel-to-Channel Isolation		(Note 2)		-60		dB
AC Feedthrough		(Note 3)		-70		dB
DAC OUTPUTS						
Output Voltage Range		R_L = open	0		V_{REF}	V
Load Regulation		Code = FF hex, R_L from 10kΩ to ∞			0.25	LSB

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +3.6V, V_{REF} = 2.5V, AGND = DGND = 0V, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +3V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS						
Input High Voltage	V_{IH}		0.7V_{DD}			V
Input Low Voltage	V_{IL}				0.3V_{DD}	V
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}			±1.0	µA
Input Capacitance	C_{IN}	(Note 4)			10	pF
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}	I_{SOURCE} = TBDmA	V_{DD} - 0.5			V
Output Low Voltage	V_{OL}	I_{SINK} = 1.6mA			0.4	V
DYNAMIC PERFORMANCE						
Voltage-Output Slew Rate		CODE = FF hex		0.6		V/µs
Output Settling Time		To 1/2LSB, from code 00 to code FF hex (Note 5)		6		µs
Digital Feedthrough and Crosstalk		VREF = 0V, code 00 to code FF hex (Note 6)		5		nV-s
Digital-to-Analog Glitch Impulse		Code 80 hex to code 7F hex		50		nV-s
Signal-to-Noise Plus Distortion Ratio	SINAD	V_{REF} = 2.5Vp-p at 1kHz, V_{DD} = 3V, code = FF hex		-70		dB
		V_{REF} = 2.5Vp-p at 10kHz		-62		
Multiplying Bandwidth		V_{REF} = 0.5Vp-p, 3dB bandwidth		380		kHz
Wideband Amplifier Noise				60		µV_{RMS}
POWER SUPPLIES						
Power-Supply Voltage	V_{DD}		2.7		3.6	V
Supply Current	I_{DD}	MAX533C/E		0.68	1.3	mA
		MAX533M		0.68	1.5	
Shutdown Current				1	10	µA

TIMING CHARACTERISTICS

(V_{DD} = +2.7V to +3.6V, V_{REF} = 2.5V, AGND = DGND = 0V, C_{DOUT} = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +3V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD} Rise to $\overline{CS}$ Fall Setup Time (Note 4)	t_{VDCS}	MAX533C/E			50	µs
		MAX533M			60	
$\overline{LDAC}$ Pulse Width Low	t_{LDAC}	MAX533C/E	40	20		ns
		MAX533M	50	25		
$\overline{CS}$ Rise to $\overline{LDAC}$ Fall Setup Time (Note 7)	t_{CLL}	MAX533C/E	40			ns
		MAX533M	50			
$\overline{CLR}$ Pulse Width Low	t_{CLW}	MAX533C/E	40	20		ns
		MAX533M	50	25		
$\overline{CS}$ Pulse Width High	t_{CSW}	MAX533C/E	90			ns
		MAX533M	100			

2.7V, Low-Power, 8-Bit Quad DAC with Rail-to-Rail Output Buffers

TIMING CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +3.6V, V_{REF} = 2.5V, AGND = DGND = 0V, C_{DOUT} = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +3V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SERIAL-INTERFACE TIMING						
SCLK Clock Frequency (Note 8)	f_{CLK}	MAX533C/E			10	MHz
		MAX533M			8.3	
SCLK Pulse Width High	t_{CH}	MAX533C/E	40			ns
		MAX533M	50			
SCLK Pulse Width Low	t_{CL}	MAX533C/E	40			ns
		MAX533M	50			
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}	MAX533C/E	40			ns
		MAX533M	50			
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
DIN to SCLK Rise to Setup Time	t_{DS}	MAX533C/E	40			
		MAX533M	50			
DIN to SCLK Rise to Hold Time	t_{DH}		0			ns
SCLK Rise to DOUT Valid Propagation Delay (Note 9)	t_{DO1}	MAX533C/E			200	ns
		MAX533M			230	
SCLK Fall to DOUT Valid Propagation Delay (Note 10)	t_{DO2}	MAX533C/E			210	ns
		MAX533M			250	
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CS0}	MAX533C/E	40			ns
		MAX533M	50			
$\overline{CS}$ Rise to SCLK Rise Setup Time	t_{CS1}	MAX533C/E	40			ns
		MAX533M	50			

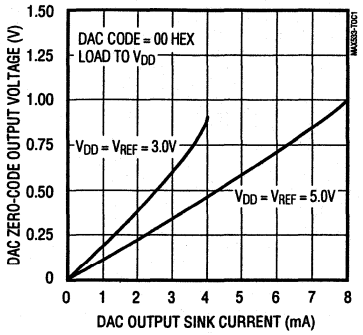
Note 1: INL and DNL are measured with R_L referenced to ground. Nonlinearity is measured from the first code that is greater than or equal to the maximum offset specification to code FF hex (full scale). See *DAC Linearity and Voltage Offset* section.
Note 2: V_{REF} = 2.5Vp-p, 10kHz. Channel-to-channel isolation is measured by setting one DAC's code to FF hex and setting all other DAC's codes to 00 hex.
Note 3: V_{REF} = 2.5Vp-p, 10kHz. DAC code = 00 hex.
Note 4: Guaranteed by design, not production tested.
Note 5: Output settling time is measured from the 50% point of the rising edge of $\overline{CS}$ to 1/2LSB of V_{OUT}'s final value.
Note 6: Digital crosstalk is defined as the glitch energy at any DAC output in response to a full-scale step change on any other DAC.
Note 7: If $\overline{LDAC}$ is activated prior to $\overline{CS}$'s rising edge, it must stay low for t_{LDAC} or longer after $\overline{CS}$ goes high.
Note 8: When DOUT is not used. If DOUT is used, f_{CLK} max is 4MHz, due to the SCLK to DOUT propagation delay.
Note 9: Serial data clocked out at SCLK's rising edge (measured from 50% of the clock edge to 20% or 80% of V_{DD}).
Note 10: Serial data clocked out at SCLK's falling edge (measured from 50% of the clock edge to 20% or 80% of V_{DD}).

2.7V, Low-Power, 8-Bit Quad DAC with Rail-to-Rail Output Buffers

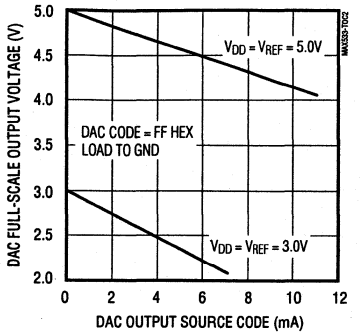
Typical Operating Characteristics

(V_{DD} = +3V, T_A = +25°C, unless otherwise noted.)

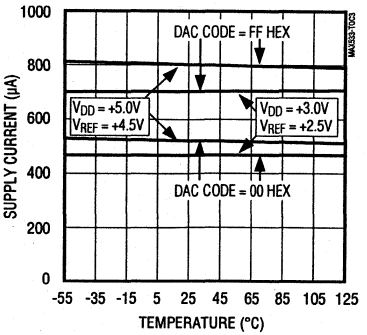
DAC ZERO-CODE OUTPUT VOLTAGE vs. OUTPUT SINK CURRENT



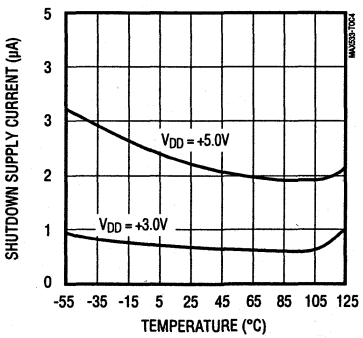
DAC FULL-SCALE OUTPUT VOLTAGE vs. OUTPUT SOURCE CURRENT



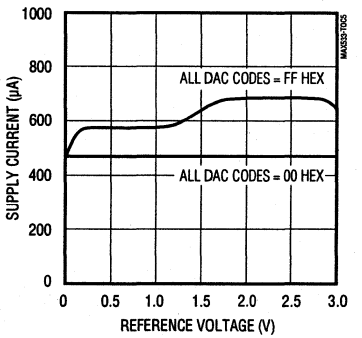
SUPPLY CURRENT vs. TEMPERATURE



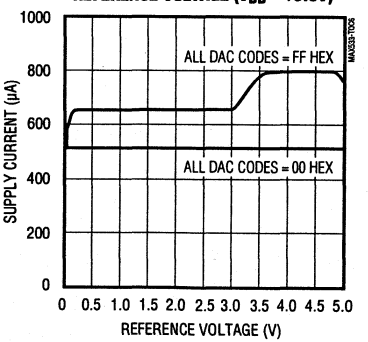
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



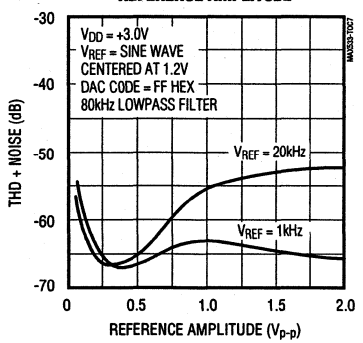
SUPPLY CURRENT vs. REFERENCE VOLTAGE (V_{DD} = +3.0V)



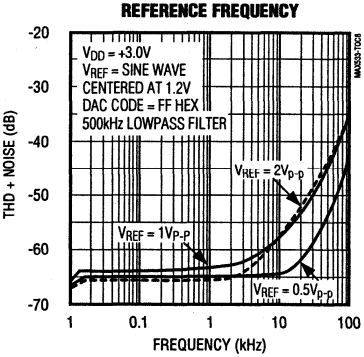
SUPPLY CURRENT vs. REFERENCE VOLTAGE (V_{DD} = +5.0V)



THD + NOISE AT DAC OUTPUT vs. REFERENCE AMPLITUDE



THD + NOISE AT DAC OUTPUT vs. REFERENCE FREQUENCY

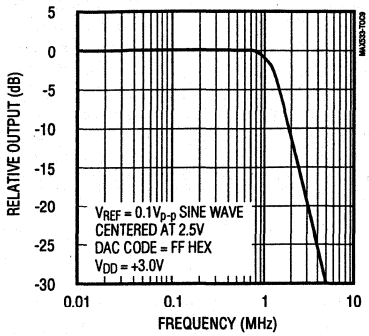


2.7V, Low-Power, 8-Bit Quad DAC with Rail-to-Rail Output Buffers

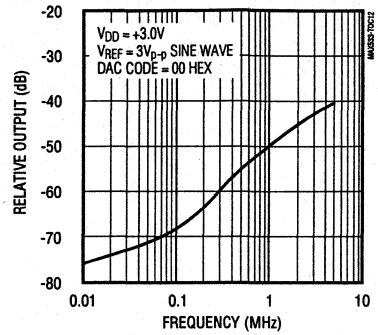
Typical Operating Characteristics (continued)

(V_{DD} = +3V, T_A = +25°C, unless otherwise noted.)

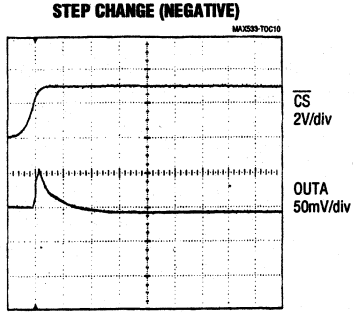
REFERENCE INPUT FREQUENCY RESPONSE



REFERENCE FEEDTHROUGH vs. FREQUENCY

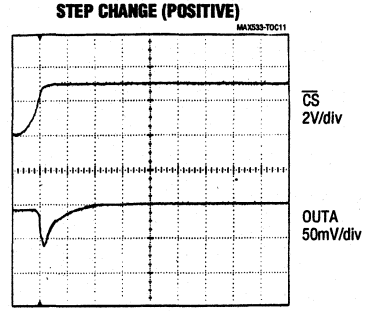


WORST-CASE 1LSB DIGITAL STEP CHANGE (NEGATIVE)



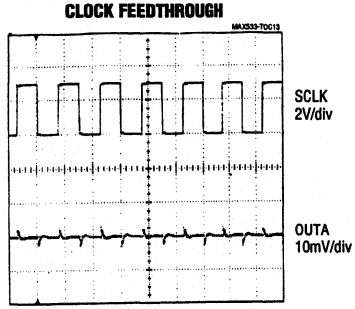
V_{DD} = 3.0V
V_{REF} = 2.5V
DAC CODE = 80 TO 7F hex
NO LOAD

WORST-CASE 1LSB DIGITAL STEP CHANGE (POSITIVE)



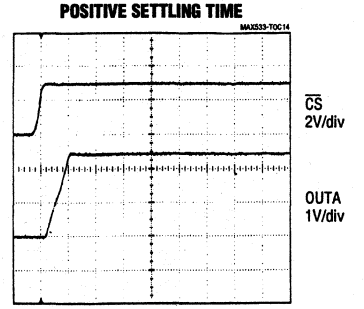
V_{DD} = 3.0V
V_{REF} = 2.5V
DAC CODE = 7F TO 80 hex
NO LOAD

CLOCK FEEDTHROUGH



SCLK = 333kHz
SCLK $t_R = t_F$ = 25ns
V_{DD} = 3.0V
V_{REF} = 2.5V
DAC CODE = 80 hex
NO LOAD

POSITIVE SETTLING TIME



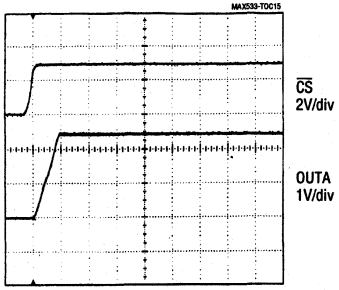
V_{DD} = 3.0V
V_{REF} = 2.5V
DAC CODE = 00 TO FF hex
NO LOAD

2.7V, Low-Power, 8-Bit Quad DAC with Rail-to-Rail Output Buffers

Typical Operating Characteristics (continued)

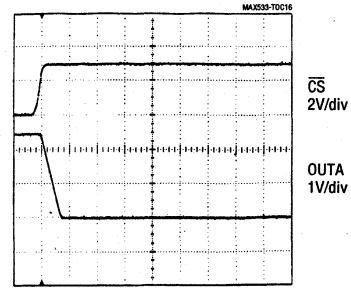
(V_{DD} = +3V, T_A = +25°C, unless otherwise noted.)

POSITIVE SETTLING TIME



V_{DD} = 3.0V
V_{REF} = 2.5V
DAC CODE = 01 TO FF hex
NO LOAD

NEGATIVE SETTLING TIME



V_{DD} = 3.0V
V_{REF} = 2.5V
DAC CODE = FF TO 00 hex
NO LOAD

Pin Description

PIN	NAME	FUNCTION
1	OUTB	DAC B Voltage Output
2	OUTA	DAC A Voltage Output
3	REF	Reference-Voltage Input
4	UPO	Software-Programmable Logic Output
5	PDE	Power-Down Enable. Must be high to enter software shutdown mode.
6	$\overline{LDAC}$	Load DAC Input (active low). Driving this asynchronous input low (level sensitive) transfers the contents of each input latch to its respective DAC latch.
7	$\overline{CLR}$	Clear DAC Input (active low). Driving $\overline{CLR}$ low asynchronously clears the input and DAC registers, and sets all DAC outputs to zero.
8	DOUT	Serial Data Output. Sinks and sources current. Data at DOUT can be clocked out on the rising or falling edge of SCLK (Table 1).
9	$\overline{CS}$	Chip-Select Input (active low). Data is shifted in and out when $\overline{CS}$ is low. Programming commands are executed when $\overline{CS}$ returns high.
10	SCLK	Serial Clock Input. Data is clocked in on the rising edge and clocked out on the falling (default) or rising edge (A0 = A1 = 1, see Table 1).
11	DIN	Serial Data Input. Data is clocked in on the rising edge of SCLK.
12	DGND	Digital Ground
13	V_{DD}	Power Supply, +2.7V to +3.6V
14	AGND	Analog Ground
15	OUTD	DAC D Voltage Output
16	OUTC	DAC C Voltage Output

2.7V, Low-Power, 8-Bit Quad DAC with Rail-to-Rail Output Buffers

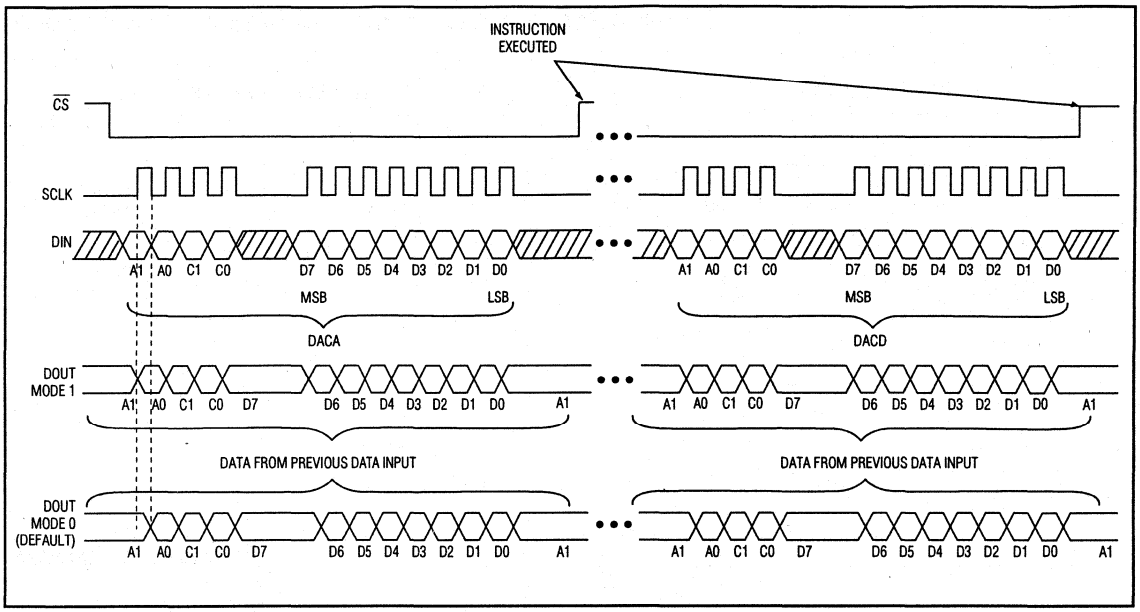


Figure 1. 3-Wire Interface Timing

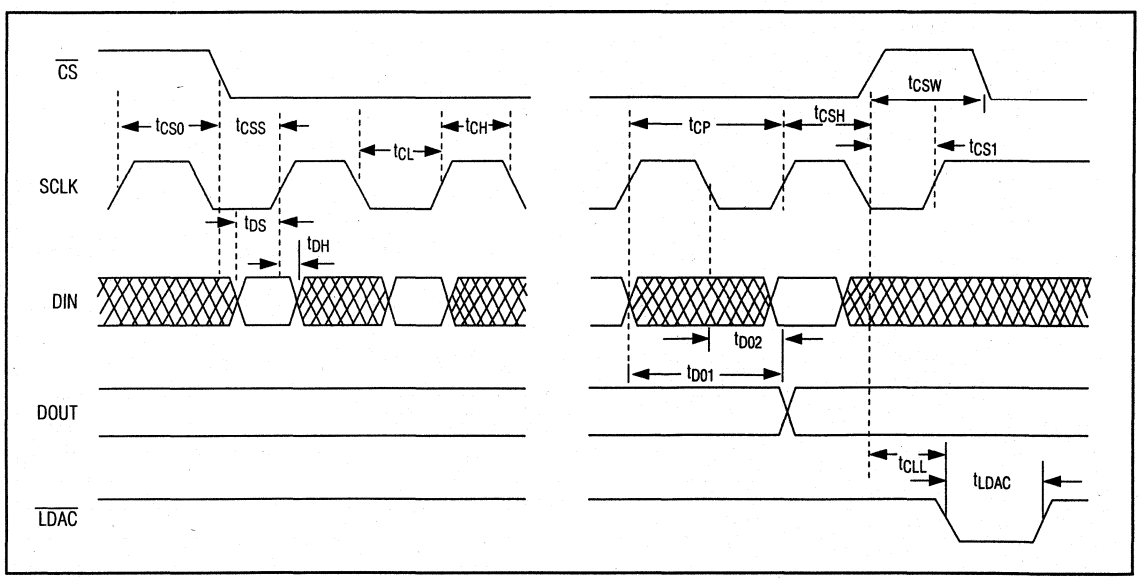


Figure 2. Detailed Serial-Interface Timing Diagram

Detailed Description

Serial Interface

At power-on, the serial interface and all digital-to-analog converters (DACs) are cleared and set to code zero. The serial data output (DOUT) is set to transition on SCLK's falling edge.

The MAX533 communicates with microprocessors through a synchronous, full-duplex, 3-wire interface (Figure 1). Data is sent MSB first and can be transmitted in one 4-bit and one 8-bit (byte) packet or in one 12-bit word. If a 16-bit word is used, the first four bits are ignored. A 4-wire interface adds a line for $\overline{LDAC}$ and allows asynchronous updating. The serial clock (SCLK) synchronizes the data transfer. Data is transmitted and received simultaneously.

Figure 2 shows the detailed serial-interface timing. Please note that the clock should be low if it is stopped between updates. DOUT does not go into a high-impedance state if the clock idles or $\overline{CS}$ is high.

Serial data is clocked into the data registers in MSB-first format, with the address and configuration information preceding the actual DAC data. Data is clocked in on SCLK's rising edge while $\overline{CS}$ is low. Data at DOUT is clocked out 12 clock cycles later, either at SCLK's falling edge (default or mode 0) or rising edge (mode 1).

Chip select ($\overline{CS}$) must be low to enable the DAC. If $\overline{CS}$ is high, the interface is disabled and DOUT remains unchanged. $\overline{CS}$ must go low at least 40ns before the first rising edge of the clock pulse to properly clock in the first bit. With $\overline{CS}$ low, data is clocked into the MAX533's internal shift register on the rising edge of the external serial clock. Always clock in the full 12 bits because each time $\overline{CS}$ goes high the bits currently in the input shift register are interpreted as a command. SCLK can be driven at rates up to 10MHz.

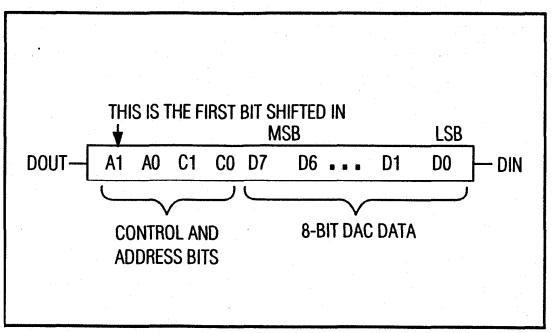


Figure 3. Serial Input Format

Serial Input Data Format and Control Codes

The 12-bit serial input format shown in Figure 3 comprises two DAC address bits (A1, A0), two control bits (C1, C0), and eight bits of data (D7...D0).

The 4-bit address/control code configures the DAC as shown in Table 1.

Load Input Register, DAC Registers Unchanged (Single Update Operation)

A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
Address		0	1	8-Bit Data							

($\overline{LDAC}$ = H)

When performing a single update operation, A1 and A0 select the respective input register. At the rising edge of $\overline{CS}$, the selected input register is loaded with the current shift-register data. All DAC outputs remain unchanged. This preloads individual data in the input register without changing the DAC outputs.

Load Input and DAC Registers

A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
Address		1	1	8-Bit Data							

($\overline{LDAC}$ = H)

This command directly loads the selected DAC register at $\overline{CS}$'s rising edge. A1 and A0 set the DAC address. Current shift-register data is placed in the selected input and DAC registers.

For example, to load all four DAC registers simultaneously with individual settings (DAC A = 0.5V, DAC B = 1V, DAC C = 1.5V, and DAC D = 2V), four commands are required. First, perform three single input register update operations for DACs A, B, and C (C1 = 0). The final command loads input register D and updates all four DAC registers from their respective input registers.

Software "$\overline{LDAC}$" Command

A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	x	x	x	x	x	x	x	x

($\overline{LDAC}$ = 1)

All DAC registers are updated with the contents of their respective input registers at $\overline{CS}$'s rising edge. With the exception of using $\overline{CS}$ to execute, this performs the same function as the asynchronous $\overline{LDAC}$.

2.7V, Low-Power, 8-Bit Quad DAC with Rail-to-Rail Output Buffers

Table 1. Serial-Interface Programming Commands

12-BIT SERIAL WORD					LDAC	FUNCTION
A1	A0	C1	C0	D7 ..... D0		
0	0	0	1	8-bit DAC data	1	Load input register A; all DAC outputs unchanged.
0	1	0	1	8-bit DAC data	1	Load input register B; all DAC outputs unchanged.
1	0	0	1	8-bit DAC data	1	Load input register C; all DAC outputs unchanged.
1	1	0	1	8-bit DAC data	1	Load input register D; all DAC outputs unchanged.
0	0	1	1	8-bit DAC data	1	Load input register A; all DAC outputs updated
0	1	1	1	8-bit DAC data	1	Load input register B; all DAC outputs updated
1	0	1	1	8-bit DAC data	1	Load input register C; all DAC outputs updated
1	1	1	1	8-bit DAC data	1	Load input register D; all DAC outputs updated.
0	1	0	0	XXXXXXXX	1	Software $\overline{LDAC}$ commands. Update all DACs from their respective input registers. Also bring the part out of shutdown mode.
1	0	0	0	8-bit DAC data	X	Load all DACs with shift-register data. Also bring the part out of shutdown mode.
1	1	0	0	XXXXXXXX	X	Software shutdown (provided PDE is high)
0	0	1	0	XXXXXXXX	X	UPO goes low.
0	1	1	0	XXXXXXXX	X	UPO goes high.
0	0	0	0	XXXXXXXX	X	No operation (NOP); shift data in shift registers.
1	1	1	0	XXXXXXXX	X	Set DOUT phase—SCLK rising (mode 1). DOUT clocked out on rising edge of SCLK. All DACs updated from their respective input registers.
1	0	1	0	XXXXXXXX	X	Set DOUT phase—SCLK falling (mode 0). DOUT clocked out on falling edge of SCLK. All DACs updated from their respective registers (default).

Load All DACs with Shift-Register Data

A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	8-Bit Data							

($\overline{LDAC}$ = X)

All four DAC registers are updated with shift-register data. This command allows all DACs to be set to any analog value within the reference range. This command can be used to substitute $\overline{CLR}$ if code 00 hex is programmed, which clears all DACs.

Software Shutdown

A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	x	x	x	x	x	x	x	x

($\overline{LDAC}$ = X, PDE = H)

Shuts down all output buffer amplifiers, reducing supply current to 10µA max.

User-Programmable Output (UPO)

A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0	UPO Output
0	0	1	0	x	x	x	x	x	x	x	x	Low
0	1	1	0	x	x	x	x	x	x	x	x	High

($\overline{LDAC}$ = X)

User-programmable logic output for controlling another device across an isolated interface. Example devices are gain control of an amplifier, a 4mA to 20mA amplifier, and a polarity output for a motor speed control.

No Operation (NOP)

A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	x	x	x	x	x	x	x	x

($\overline{LDAC}$ = X)

The NOP command (no operation) allows data to be shifted through the MAX533 shift register without affecting the input or DAC registers. This is useful in daisy chaining (also see the *Daisy Chaining Devices* section).

For this command, the data bits are "Don't Cares." As an example, three MAX533s are daisy chained (A, B, and C), and devices A and C need to be updated. The 36-bit-wide command would consist of one 12-bit word for device C, followed by an NOP instruction for device B and a third 12-bit word with data for device A. At $\overline{CS}$'s rising edge, device B will not change state.

Set DOUT Phase—SCLK Rising (Mode 1)

A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	0	x	x	x	x	x	x	x	x

($\overline{LDAC}$ = x)

Mode 1 resets the serial-output DOUT to transition at SCLK's rising edge. Once this command is issued, DOUT's phase is latched and will not change except on power-up or if the specific command to set the phase to falling edge is issued.

This command also loads all DAC registers with the contents of their respective input registers, and is identical to the "$\overline{LDAC}$" command.

Set DOUT Phase—SCLK Falling (Mode 0, Default)

A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	x	x	x	x	x	x	x	x

($\overline{LDAC}$ = x)

This command resets DOUT to transition at SCLK's falling edge. The same command also updates all DAC registers with the contents of their respective input registers, identical to the "$\overline{LDAC}$" command.

LDAC Operation (Hardware)

$\overline{LDAC}$ is typically used in 4-wire interfaces (Figure 7). This command is level sensitive, and it allows asynchronous hardware control of the DAC outputs. With $\overline{LDAC}$ low, the DAC registers are transparent, and any time an input register is updated, the DAC output immediately follows.

Clear DACs with $\overline{CLR}$

Strobing the $\overline{CLR}$ pin low causes an asynchronous clear of input and DAC registers and sets all DAC outputs to zero. Similar to the $\overline{LDAC}$ pin, $\overline{CLR}$ can be invoked at any time, typically when the device is not selected ($\overline{CS}$ = H). When the DAC data is all zeros, this function is equivalent to the "Update all DACs from Shift Registers" command.

Serial Data Output

DOUT is the internal shift register's output. DOUT can be programmed to clock out data on SCLK's falling edge (mode 0) or rising edge (mode 1). In mode 0, output data lags input data by 12.5 clock cycles, maintaining compatibility with Microwire and SPI. In mode 1, output data lags input data by 12 clock cycles. On power-up, DOUT defaults to mode 0 timing. DOUT never three-states; it always actively drives either high or low and remains unchanged when $\overline{CS}$ is high.

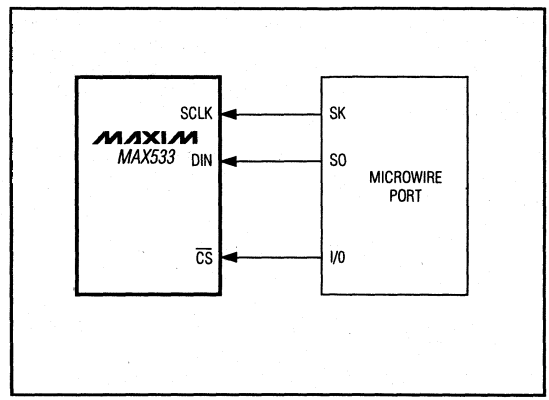


Figure 4. Connections for Microwire

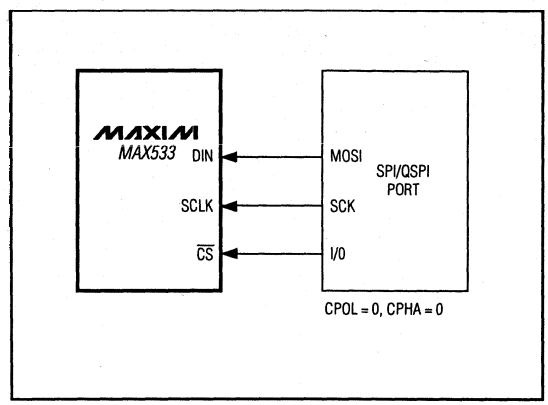


Figure 5. Connections for SPI/QSPI

9

2.7V, Low-Power, 8-Bit Quad DAC with Rail-to-Rail Output Buffers

Interfacing to the Microprocessor

The MAX533 is Microwire™ and SPI™/QSPI™ compatible. For SPI and QSPI, clear the CPOL and CPHA configuration bits (CPOL = CPHA = 0). The SPI/QSPI CPOL = CPHA = 1 configuration can also be used if the DOUT output is ignored.

The MAX533 can interface with Intel's 80C5X/80C3X family in mode 0 if the SCLK clock polarity is inverted. More universally, if a serial port is not available, three lines from one of the parallel ports can be used for bit manipulation.

Digital feedthrough at the voltage outputs is greatly minimized by operating the serial clock only to update the registers. Also see the Clock Feedthrough photo in the *Typical Operating Characteristics* section. The clock idle state is low.

Daisy-Chaining Devices

Any number of MAX533s can be daisy-chained by connecting DOUT of one device to DIN of the following device in the chain. The NOP instruction (Table 1) allows data to be passed from DIN to DOUT without changing the input or DAC registers of the passing device. A 3-wire interface updates daisy-chained or individual MAX533s simultaneously by bringing $\overline{CS}$ high (Figure 6).

Analog Section

DAC Operation

The MAX533 uses a matrix decoding architecture for the DACs, which saves power in the overall system. The external reference voltage is divided down by a resistor string placed in a matrix fashion. Row and column decoders select the appropriate tab from the resistor string to provide the needed analog voltages. The resistor string presents a code-independent input impedance to the reference and guarantees a monotonic output. Figure 8 shows a simplified diagram of the four DACs.

Reference Input

The voltage at REF sets the full-scale output voltage for all four DACs. The 460kΩ typical input impedance at REF is code independent. The output voltage for any DAC can be represented by a digitally programmable voltage source as follows:

$$V_{OUT} = (NB \times V_{REF}) / 256$$

where NB is the numerical value of the DAC's binary input code.

SPI and QSPI are trademarks of Motorola, Inc. Microwire is a trademark of National Semiconductor Corp.

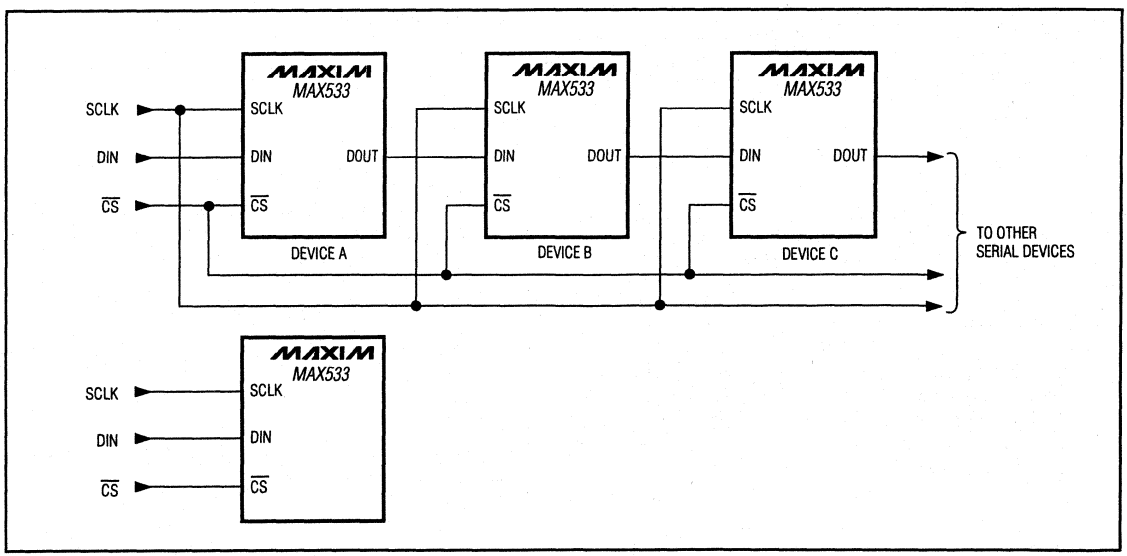


Figure 6. Daisy-chained or individual MAX533s are simultaneously updated by bringing $\overline{CS}$ high. Only three wires are required.

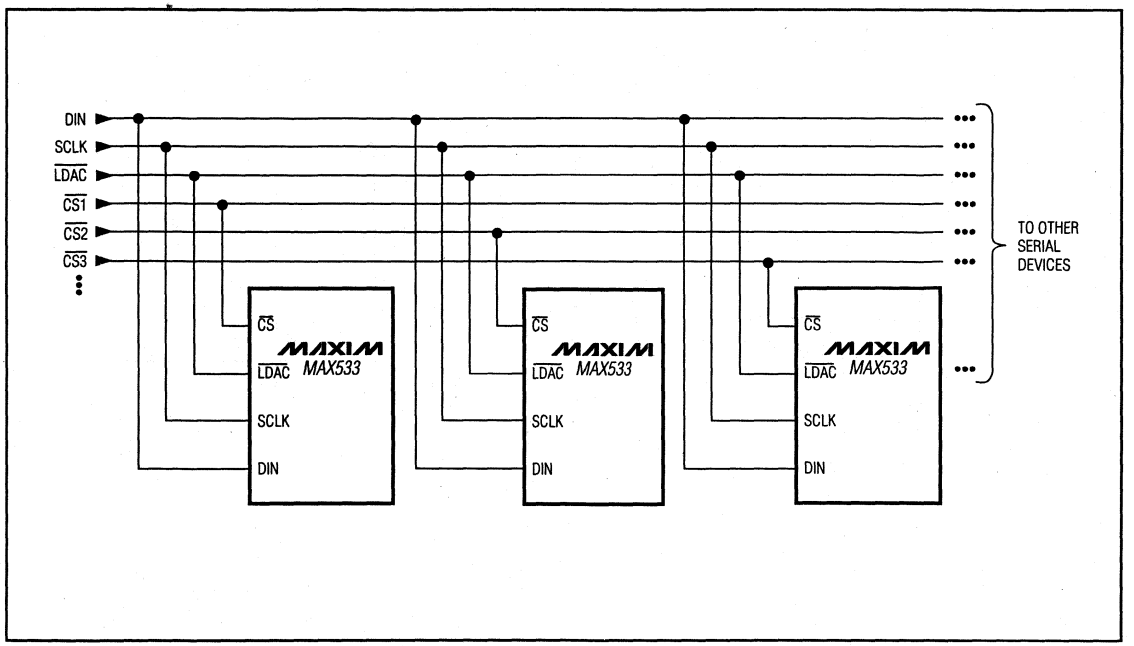


Figure 7. Multiple MAX533s sharing one DIN line. Simultaneously update by strobing LDAC, or specifically update by enabling an individual CS.

Output Buffer Amplifiers

All MAX533 voltage outputs are internally buffered by precision unity-gain followers that slew at about 0.6V/µs. The outputs can swing from GND to V_{DD}. With a 0V to +2.5V (or +2.5V to 0V) output transition, the amplifier outputs will typically settle to 1/2LSB in 6µs when loaded with 10kΩ in parallel with 100pF.

The buffer amplifiers are stable with any combination of resistive (≥10kΩ) or capacitive loads.

Applications Information

DAC Linearity and Voltage Offset

The output buffer can have a negative input offset voltage that would normally drive the output negative, but since there is no negative supply the output stays at 0V (Figure 9). When linearity is determined using the endpoint method, it is measured between zero code (all inputs 0) and full-scale code (all inputs 1) after offset and gain error are calibrated out. However, in single-supply operation the next code after zero may not change the output (Figure 9), so the lowest code that produces a positive output is the lower endpoint.

2.7V, Low-Power, 8-Bit Quad DAC with Rail-to-Rail Output Buffers

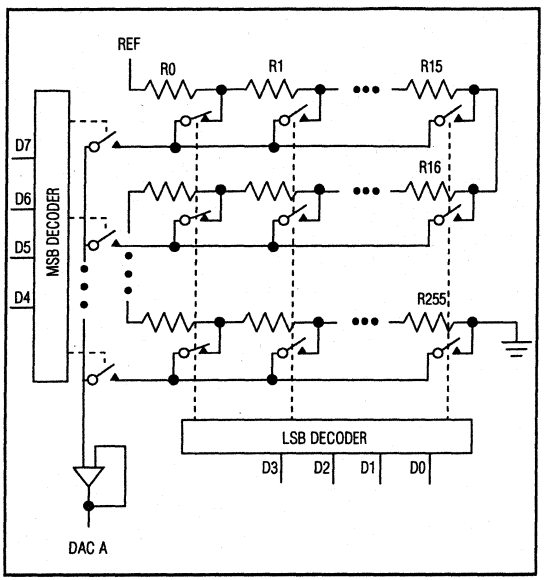


Figure 8. DAC Simplified Circuit Diagram

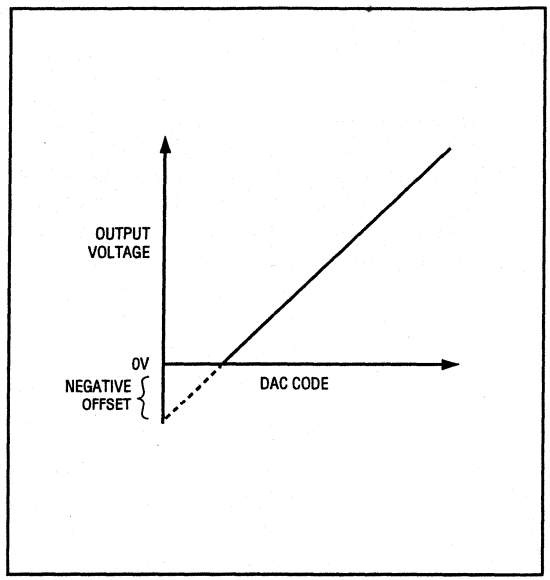


Figure 9. Effect of Negative Offset (Single Supply)

Power Sequencing

The voltage applied to REF should not exceed V_{DD} at any time. If proper power sequencing is not possible, connect an external Schottky diode between REF and V_{DD} to ensure compliance with the absolute maximum ratings. Do not apply signals to the digital inputs before the device is fully powered up.

Power-Supply Bypassing and Ground Management

Connect AGND and DGND together at the IC. This ground should then return to the highest-quality ground available. Bypass V_{DD} with a 0.1µF capacitor, located as close to V_{DD} and DGND as possible.

Careful PC board layout minimizes crosstalk among DAC outputs and digital inputs. Figure 10 shows suggested circuit board layout to minimize crosstalk.

Unipolar-Output, Two-Quadrant Multiplication

In unipolar operation, the output voltages and the reference input are the same polarity. Figure 11 shows the MAX533 unipolar configuration, and Table 2 shows the unipolar code.

Table 2. Unipolar Code Table

DAC CONTENTS		ANALOG OUTPUT
MSB	LSB	
1111	1111	$+V_{REF}\left(\frac{255}{256}\right)$
1000	0001	$+V_{REF}\left(\frac{129}{256}\right)$
1000	0000	$+V_{REF}\left(\frac{128}{256}\right) = +\frac{V_{REF}}{2}$
0111	1111	$+V_{REF}\left(\frac{127}{256}\right)$
0000	0001	$+V_{REF}\left(\frac{1}{256}\right)$
0000	0000	0V

Note: $1LSB = (V_{REF})(2^{-8}) = +V_{REF}\left(\frac{1}{256}\right)$

2.7V, Low-Power, 8-Bit Quad DAC with Rail-to-Rail Output Buffers

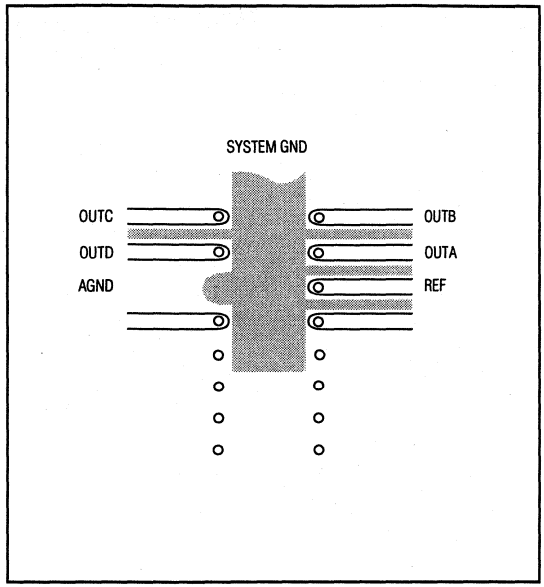


Figure 10. Suggested PC Board Layout for Minimizing Crosstalk (Bottom View)

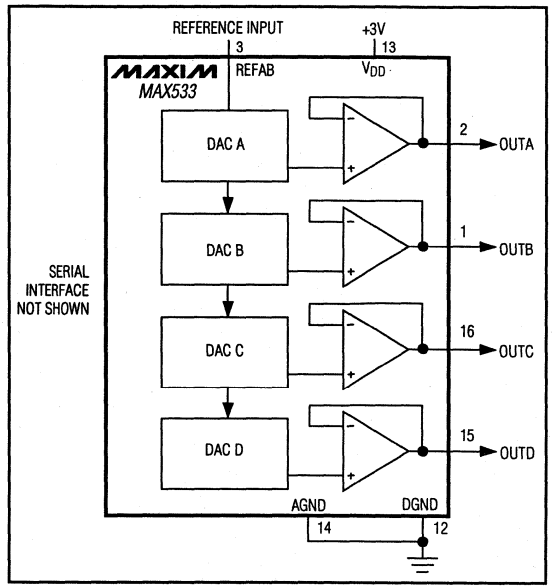
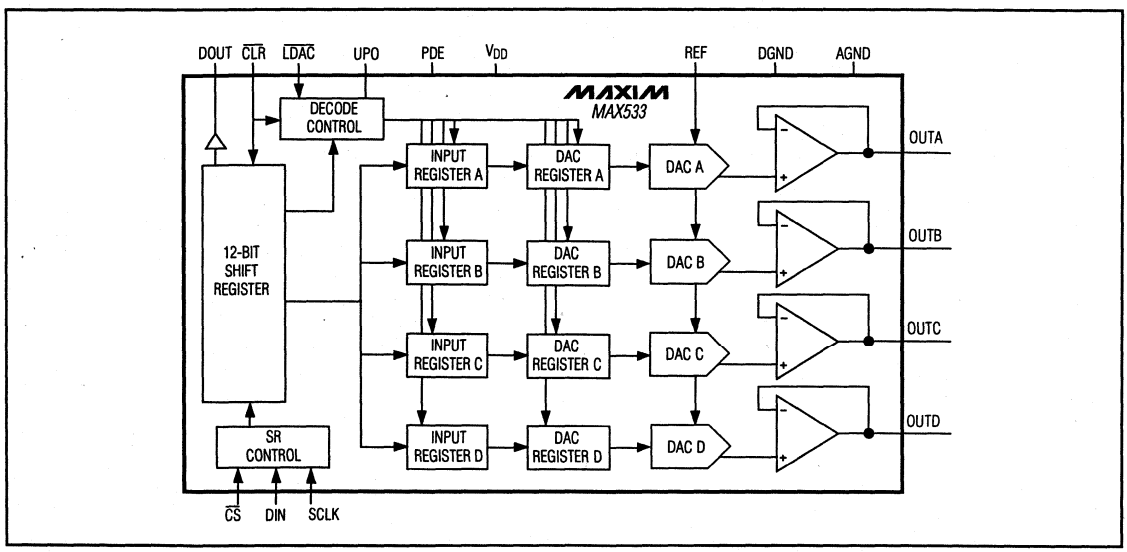


Figure 11. Unipolar Output Circuit

Functional Diagram



2.7V, Low-Power, 8-Bit Quad DAC with Rail-to-Rail Output Buffers

Chip Information

TRANSISTOR COUNT: 6821

19-1105; Rev 0; 8/96

MAXIM

+5V, Low-Power, 8-Bit Quad DAC with Rail-to-Rail Output Buffers

General Description

The MAX534 serial-input, voltage-output, 8-bit quad digital-to-analog converter (DAC) operates from a single +4.5V to +5.5V supply. Internal precision buffers swing rail to rail, and the reference input range includes both ground and the positive rail. The MAX534 features a 2.5µA shutdown mode.

The serial interface is double buffered: a 12-bit input shift register is followed by four 8-bit buffer registers and four 8-bit DAC registers. The 12-bit serial word consists of eight data bits and four control bits (for DAC selection and special programming commands). Both the input and DAC registers can be updated independently or simultaneously with a single software command. Two additional asynchronous control pins, $\overline{LDAC}$ and $\overline{CLR}$, provide simultaneous updating or clearing of the input and DAC registers.

The interface is compatible with SPI™, QSPI™ (CPOL = CPHA = 0 or CPOL = CPHA = 1), and Microwire™. A buffered data output allows daisy chaining of serial devices.

In addition to 16-pin DIP and CERDIP packages, the MAX534 is available in a 16-pin QSOP that occupies the same area as an 8-pin SO.

For operation guaranteed to 2.7V, see the MAX533 data sheet.

Applications

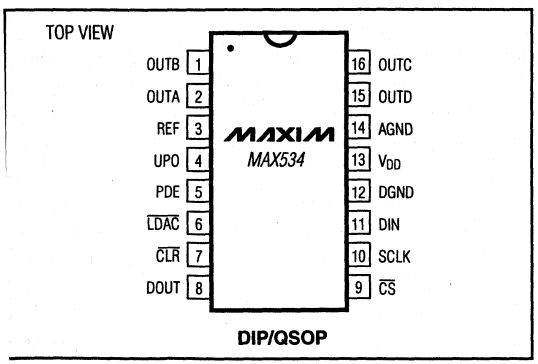
Digital Gain and Offset Adjustments

Programmable Attenuators

Programmable Current Sources

Portable Instruments

Pin Configuration



Features

- ♦ **+4.5V to +5.5V Single-Supply Operation**
- ♦ **Ultra-Low Supply Current:**
  0.8mA while Operating
  2.5µA in Shutdown Mode
- ♦ **Ultra-Small 16-Pin QSOP Package**
- ♦ **Ground to V_{DD} Reference Input Range**
- ♦ **Output Buffer Amplifiers Swing Rail to Rail**
- ♦ **10MHz Serial Interface Compatible with SPI, QSPI (CPOL = CPHA = 0 or CPOL = CPHA = 1), and Microwire**
- ♦ **Double-Buffered Registers for Synchronous Updating**
- ♦ **Serial Data Output for Daisy Chaining**
- ♦ **Power-On Reset Clears Serial Interface and Sets All Registers to Zero**
- ♦ **Software Shutdown**
- ♦ **Software-Programmable Logic Output (µC I/O Extender)**
- ♦ **Asynchronous Hardware Clear Resets All Internal Registers to Zero**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX534ACPE	0°C to +70°C	16 Plastic DIP	±1
MAX534BCPE	0°C to +70°C	16 Plastic DIP	±2
MAX534ACEE	0°C to +70°C	16 QSOP	±1
MAX534BCEE	0°C to +70°C	16 QSOP	±2
MAX534BC/D	0°C to +70°C	Dice*	±2
MAX534AEPE	-40°C to +85°C	16 Plastic DIP	±1
MAX534BEPE	-40°C to +85°C	16 Plastic DIP	±2
MAX534AEEE	-40°C to +85°C	16 QSOP	±1
MAX534BEEE	-40°C to +85°C	16 QSOP	±2
MAX534AMJE	-55°C to +125°C	16 CERDIP**	±1
MAX534BMJE	-55°C to +125°C	16 CERDIP**	±2

*Dice are tested at T_A = +25°C.
**Contact factory for availability and processing to MIL-STD-883.

Functional Diagram appears at end of data sheet.

9

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+5V, Low-Power, 8-Bit Quad DAC with Rail-to-Rail Output Buffers

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND .....-0.3V, +6V
V_{DD} to AGND.....-0.3V, +6V
Digital Input Voltage to DGND .....-0.3V, +6V
Digital Output Voltage to DGND.....-0.3V, (V_{DD} + 0.3V)
AGND to DGND .....±0.3V
REF.....-0.3V, (V_{DD} + 0.3V)
OUT_ .....-0.3V, V_{DD}
Maximum Current into Any Pin.....50mA

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
QSOP (derate 8.3mW/°C above +70°C).....667mW
CERDIP (derate 10.00mW/°C above +70°C).....800mW
Operating Temperature Ranges
MAX534 _ C_ E .....0°C to +70°C
MAX534 _ E_ E .....-40°C to +85°C
MAX534 _ MJE .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +4.5V to +5.5V, V_{REF} = 4.096V, AGND = DGND = 0V, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +5V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC ACCURACY						
Resolution					8	Bits
Integral Nonlinearity (Note 1)	INL	MAX534A			±1	LSB
		MAX534B			±2	
Differential Nonlinearity (Note 1)	DNL	Guaranteed monotonic (all codes)			±1.0	LSB
Zero-Code Error	ZCE	Code = 00 hex			±20	mV
Zero-Code-Error Supply Rejection		Code = 00 hex, V_{DD} = 4.5V to 5.5V			1	LSB
Zero-Code Temperature Coefficient		Code = 00 hex		±10		µV/°C
Full-Scale Error		Code = FF hex			±30	mV
Full-Scale Error Supply Rejection		Code = FF hex, V_{DD} = 4.5V to 5.5V			1	LSB
Full-Scale Temperature Coefficient		Code = FF hex		±10		µV/°C
REFERENCE INPUTS						
Input Voltage Range			0		V_{DD}	V
Input Resistance			322	460	598	kΩ
Input Capacitance				10		pF
Channel-to-Channel Isolation		(Note 2)		-60		dB
AC Feedthrough		(Note 3)		-60		dB
DAC OUTPUTS						
Output Voltage Range		R_L = open	0		V_{REF}	V
Load Regulation		Code = FF hex, measured with I_L = 0mA to 1.6mA			0.156	LSB/mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +4.5V to +5.5V, V_{REF} = 4.096V, AGND = DGND = 0V, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +5V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS						
Input High Voltage	V_{IH}		0.7V_{DD}			V
Input Low Voltage	V_{IL}				0.3V_{DD}	V
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}			±1.0	µA
Input Capacitance	C_{IN}	(Note 4)			10	pF
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}	I_{SOURCE} = 0.2mA	V_{DD} - 0.5			V
Output Low Voltage	V_{OL}	I_{SINK} = 1.6mA			0.4	V
DYNAMIC PERFORMANCE						
Voltage-Output Slew Rate		CODE = FF hex		0.6		V/µs
Output Settling Time		To 1/2LSB, from code 00 to code FF hex (Note 5)		8		µs
Digital Feedthrough and Crosstalk		VREF = 0V, code 00 to code FF hex (Note 6)		5		nV-s
Digital-to-Analog Glitch Impulse		Code 80 hex to code 7F hex		50		nV-s
Signal-to-Noise Plus Distortion Ratio	SINAD	V_{REF} = 4Vp-p at 1kHz, code = FF hex		80		dB
		V_{REF} = 4Vp-p at 10kHz		70		
Multiplying Bandwidth		V_{REF} = 0.5Vp-p, 3dB bandwidth		380		kHz
Wideband Amplifier Noise				60		µV_{RMS}
POWER SUPPLIES						
Power-Supply Voltage	V_{DD}		4.5		5.5	V
Supply Current	I_{DD}	MAX534C/E		0.8	1.3	mA
		MAX534M		0.8	1.5	
Shutdown Current				2.5	10	µA

TIMING CHARACTERISTICS

(V_{DD} = +4.5V to +5.5V, V_{REF} = 4.096V, AGND = DGND = 0V, C_{DOUT} = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +5V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD} Rise to $\overline{CS}$ Fall Setup Time (Note 4)	t_{VDCS}	MAX534C/E			50	µs
		MAX534M			60	
$\overline{LDAC}$ Pulse Width Low	t_{LDAC}	MAX534C/E	40	20		ns
		MAX534M	50	25		
$\overline{CS}$ Rise to $\overline{LDAC}$ Fall Setup Time (Note 7)	t_{CLL}	MAX534C/E	40			ns
		MAX534M	50			
$\overline{CLR}$ Pulse Width Low	t_{CLW}	MAX534C/E	40	20		ns
		MAX534M	50	25		
$\overline{CS}$ Pulse Width High	t_{CSW}	MAX534C/E	90			ns
		MAX534M	100			

+5V, Low-Power, 8-Bit Quad DAC with Rail-to-Rail Output Buffers

TIMING CHARACTERISTICS (continued)

(V_{DD} = +4.5V to +5.5V, V_{REF} = 4.096V, AGND = DGND = 0V, C_{DOUT} = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +5V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SERIAL-INTERFACE TIMING						
SCLK Clock Frequency (Note 8)	f_{CLK}	MAX534C/E			10	MHz
		MAX534M			8.3	
SCLK Pulse Width High	t_{CH}	MAX534C/E	40			ns
		MAX534M	50			
SCLK Pulse Width Low	t_{CL}	MAX534C/E	40			ns
		MAX534M	50			
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}	MAX534C/E	40			ns
		MAX534M	50			
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
DIN to SCLK Rise to Setup Time	t_{DS}	MAX534C/E	40			ns
		MAX534M	50			
DIN to SCLK Rise to Hold Time	t_{DH}		0			ns
SCLK Rise to DOUT Valid Propagation Delay (Note 9)	t_{DO1}	MAX534C/E			200	ns
		MAX534M			230	
SCLK Fall to DOUT Valid Propagation Delay (Note 10)	t_{DO2}	MAX534C/E			210	ns
		MAX534M			250	
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CS0}	MAX534C/E	40			ns
		MAX534M	50			
$\overline{CS}$ Rise to SCLK Rise Setup Time	t_{CS1}	MAX534C/E	40			ns
		MAX534M	50			

Note 1: INL and DNL are measured with R_L referenced to ground. Nonlinearity is measured from the first code that is greater than or equal to the maximum offset specification to code FF hex (full scale). See *DAC Linearity and Voltage Offset* section.

Note 2: V_{REF} = 4Vp-p, 10kHz. Channel-to-channel isolation is measured by setting one DAC's code to FF hex and setting all other DAC's codes to 00 hex.

Note 3: V_{REF} = 4Vp-p, 10kHz. DAC code = 00 hex.

Note 4: Guaranteed by design, not production tested.

Note 5: Output settling time is measured from the 50% point of the rising edge of $\overline{CS}$ to 1/2LSB of V_{OUT}'s final value.

Note 6: Digital crosstalk is defined as the glitch energy at any DAC output in response to a full-scale step change on any other DAC.

Note 7: If $\overline{LDAC}$ is activated prior to $\overline{CS}$'s rising edge, it must stay low for t_{LDAC} or longer after $\overline{CS}$ goes high.

Note 8: When DOUT is not used. If DOUT is used, f_{CLK} max is 4MHz, due to the SCLK to DOUT propagation delay.

Note 9: Serial data clocked out at SCLK's rising edge (measured from 50% of the clock edge to 20% or 80% of V_{DD}).

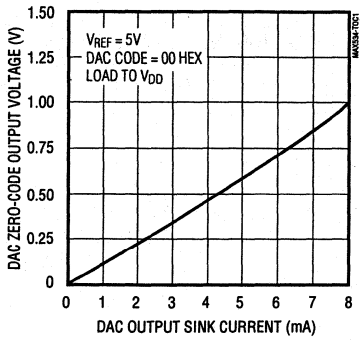
Note 10: Serial data clocked out at SCLK's falling edge (measured from 50% of the clock edge to 20% or 80% of V_{DD}).

+5V, Low-Power, 8-Bit Quad DAC with Rail-to-Rail Output Buffers

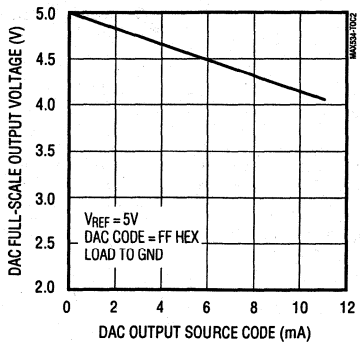
Typical Operating Characteristics

(V_{DD} = +5V, T_A = +25°C, unless otherwise noted.)

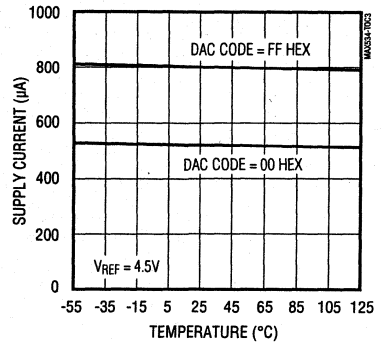
DAC ZERO-CODE OUTPUT VOLTAGE vs. OUTPUT SINK CURRENT



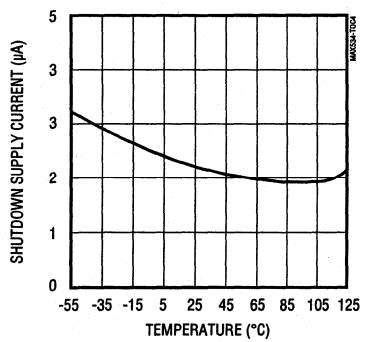
DAC FULL-SCALE OUTPUT VOLTAGE vs. OUTPUT SOURCE CURRENT



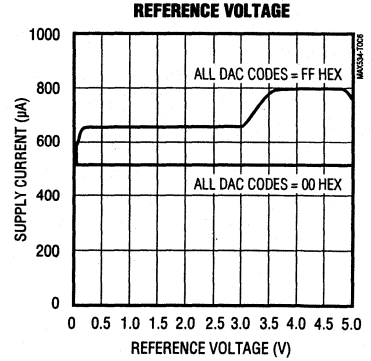
SUPPLY CURRENT vs. TEMPERATURE



SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



SUPPLY CURRENT vs. REFERENCE VOLTAGE



+5V, Low-Power, 8-Bit Quad DAC with Rail-to-Rail Output Buffers

Pin Description

PIN	NAME	FUNCTION
1	OUTB	DAC B Voltage Output
2	OUTA	DAC A Voltage Output
3	REF	Reference-Voltage Input
4	UPO	Software-Programmable Logic Output
5	PDE	Power-Down Enable. Must be high to allow software shutdown mode.
6	$\overline{LDAC}$	Load DAC Input (active low). Driving this asynchronous input low (level sensitive) transfers the contents of each input latch to its respective DAC latch.
7	$\overline{CLR}$	Clear DAC Input (active low). Driving $\overline{CLR}$ low asynchronously clears the input and DAC registers, and sets all DAC outputs to zero.
8	DOUT	Serial Data Output. Sinks and sources current. Data at DOUT can be clocked out on the rising or falling edge of SCLK (Table 1).
9	$\overline{CS}$	Chip-Select Input (active low). Data is shifted in and out when $\overline{CS}$ is low. Programming commands are executed when $\overline{CS}$ returns high.
10	SCLK	Serial Clock Input. Data is clocked in on the rising edge and clocked out on the falling (default) or rising edge (A0 = A1 = 1, see Table 1).
11	DIN	Serial Data Input. Data is clocked in on the rising edge of SCLK.
12	DGND	Digital Ground
13	V_{DD}	Power Supply, +4.5V to +5.5V
14	AGND	Analog Ground
15	OUTD	DAC D Voltage Output
16	OUTC	DAC C Voltage Output

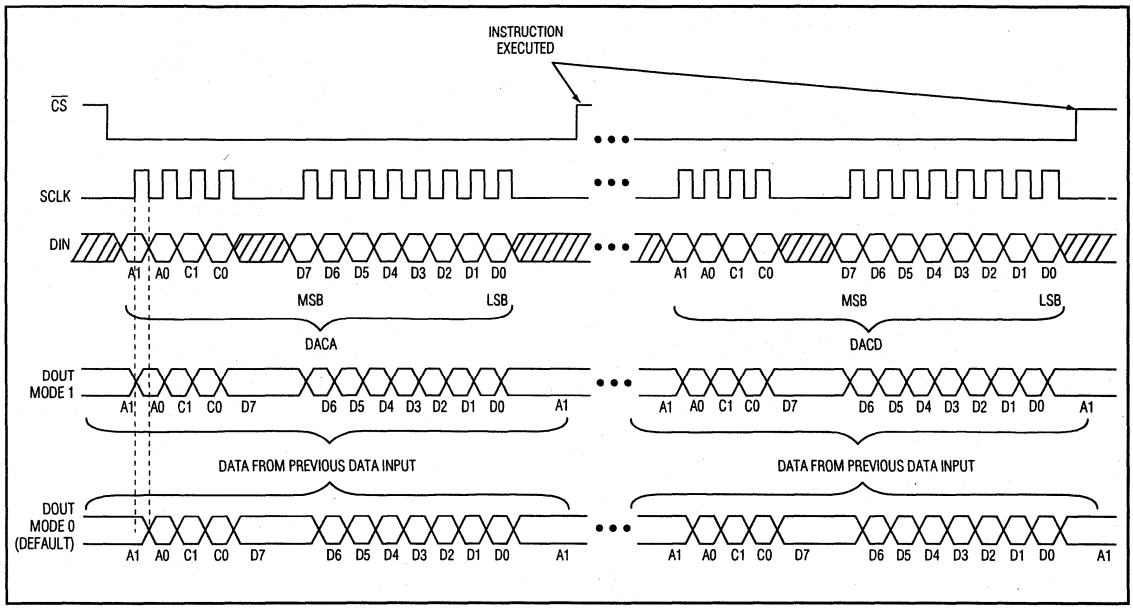


Figure 1. 3-Wire Interface Timing

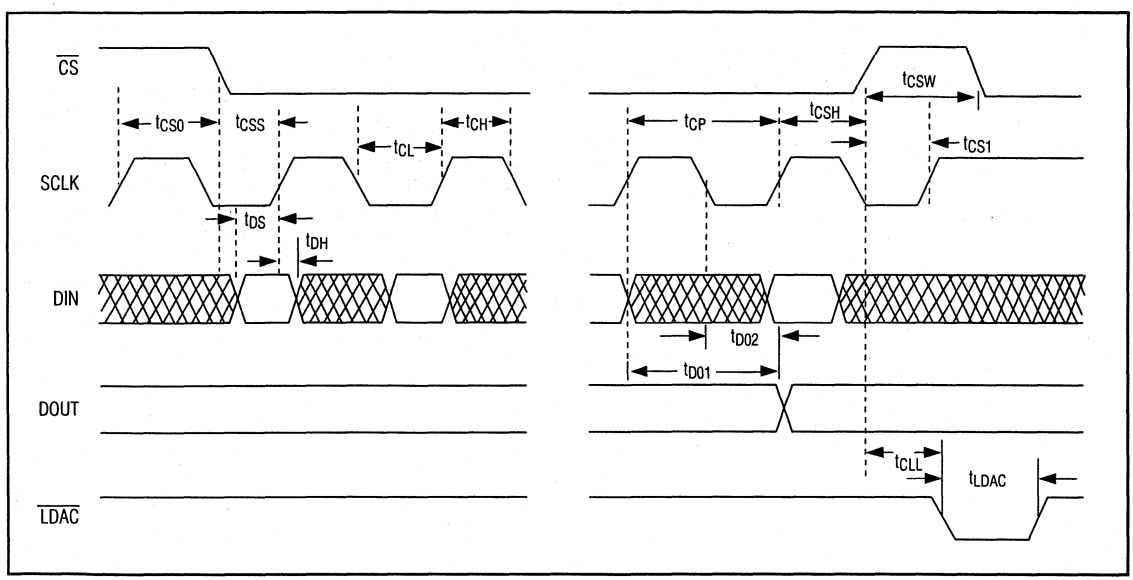


Figure 2. Detailed Serial-Interface Timing Diagram

+5V, Low-Power, 8-Bit Quad DAC with Rail-to-Rail Output Buffers

Detailed Description

Serial Interface

At power-on, the serial interface and all digital-to-analog converters (DACs) are cleared and set to code zero. The serial data output (DOUT) is set to transition on SCLK's falling edge.

The MAX534 communicates with microprocessors through a synchronous, full-duplex, 3-wire interface (Figure 1). Data is sent MSB first and can be transmitted in one 4-bit and one 8-bit (byte) packet or in one 12-bit word. If a 16-bit word is used, the first four bits are ignored. A 4-wire interface adds a line for $\overline{LDAC}$ and allows asynchronous updating. The serial clock (SCLK) synchronizes the data transfer. Data is transmitted and received simultaneously.

Figure 2 shows the detailed serial-interface timing. Please note that the clock should be low if it is stopped between updates. DOUT does not go into a high-impedance state if the clock idles or $\overline{CS}$ is high.

Serial data is clocked into the data registers in MSB-first format, with the address and configuration information preceding the actual DAC data. Data is clocked in on SCLK's rising edge while $\overline{CS}$ is low. Data at DOUT is clocked out 12 clock cycles later, either at SCLK's falling edge (default or mode 0) or rising edge (mode 1).

Chip select ($\overline{CS}$) must be low to enable the DAC. If $\overline{CS}$ is high, the interface is disabled and DOUT remains unchanged. $\overline{CS}$ must go low at least 40ns before the first rising edge of the clock pulse to properly clock in the first bit. With $\overline{CS}$ low, data is clocked into the MAX534's internal shift register on the rising edge of the external serial clock. Always clock in the full 12 bits because each time $\overline{CS}$ goes high the bits currently in the input shift register are interpreted as a command. SCLK can be driven at rates up to 10MHz.

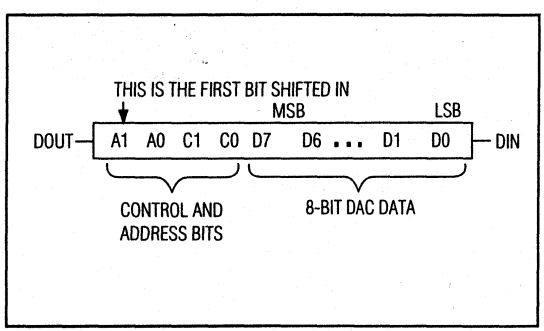


Figure 3. Serial Input Format

Serial Input Data Format and Control Codes

The 12-bit serial input format shown in Figure 3 comprises two DAC address bits (A1, A0), two control bits (C1, C0), and eight bits of data (D7...D0).

The 4-bit address/control code configures the DAC as shown in Table 1.

Load Input Register, DAC Registers Unchanged (Single Update Operation)

A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
Address		0	1	8-Bit Data							

($\overline{LDAC}$ = H)

When performing a single update operation, A1 and A0 select the respective input register. At the rising edge of $\overline{CS}$, the selected input register is loaded with the current shift-register data. All DAC outputs remain unchanged. This preloads individual data in the input register without changing the DAC outputs.

Load Input and DAC Registers

A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
Address		1	1	8-Bit Data							

($\overline{LDAC}$ = H)

This command directly loads the selected DAC register at $\overline{CS}$'s rising edge. A1 and A0 set the DAC address. Current shift-register data is placed in the selected input and DAC registers.

For example, to load all four DAC registers simultaneously with individual settings (DAC A = 1V, DAC B = 2V, DAC C = 3V, and DAC D = 4V), four commands are required. First, perform three single input register update operations for DACs A, B, and C (C1 = 0). The final command loads input register D and updates all four DAC registers from their respective input registers.

Software "$\overline{LDAC}$" Command

A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	x	x	x	x	x	x	x	x

($\overline{LDAC}$ = 1)

When this command is initiated, all DAC registers are updated with the contents of their respective input registers at $\overline{CS}$'s rising edge. With the exception of using $\overline{CS}$ to execute, this performs the same function as the asynchronous $\overline{LDAC}$.

Table 1. Serial-Interface Programming Commands

12-BIT SERIAL WORD					LDAC	FUNCTION
A1	A0	C1	C0	D7 ..... D0		
0	0	0	1	8-bit DAC data	1	Load input register A; all DAC outputs unchanged.
0	1	0	1	8-bit DAC data	1	Load input register B; all DAC outputs unchanged.
1	0	0	1	8-bit DAC data	1	Load input register C; all DAC outputs unchanged.
1	1	0	1	8-bit DAC data	1	Load input register D; all DAC outputs unchanged.
0	0	1	1	8-bit DAC data	1	Load input register A; all DAC outputs updated
0	1	1	1	8-bit DAC data	1	Load input register B; all DAC outputs updated
1	0	1	1	8-bit DAC data	1	Load input register C; all DAC outputs updated
1	1	1	1	8-bit DAC data	1	Load input register D; all DAC outputs updated.
0	1	0	0	XXXXXXXX	1	Software $\overline{LDAC}$ commands. Update all DACs from their respective input registers. Also bring the part out of shutdown mode.
1	0	0	0	8-bit DAC data	X	Load all DACs with shift-register data. Also bring the part out of shutdown mode.
1	1	0	0	XXXXXXXX	X	Software shutdown (provided PDE is high)
0	0	1	0	XXXXXXXX	X	UPO goes low.
0	1	1	0	XXXXXXXX	X	UPO goes high.
0	0	0	0	XXXXXXXX	X	No operation (NOP); shift data in shift registers.
1	1	1	0	XXXXXXXX	X	Set DOUT phase—SCLK rising (mode 1). DOUT clocked out on rising edge of SCLK. All DACs updated from their respective input registers.
1	0	1	0	XXXXXXXX	X	Set DOUT phase—SCLK falling (mode 0). DOUT clocked out on falling edge of SCLK. All DACs updated from their respective registers (default).

Load All DACs with Shift-Register Data

A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	8-Bit Data							

($\overline{LDAC}$ = X)

When this command is initiated, all four DAC registers are updated with shift-register data. This command allows all DACs to be set to any analog value within the reference range. It can be used to substitute $\overline{CLR}$ if code 00 hex is programmed, which clears all DACs.

Software Shutdown

A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	x	x	x	x	x	x	x	x

($\overline{LDAC}$ = X, PDE = H)

This command shuts down all output buffer amplifiers, reducing supply current to 10µA max.

User-Programmable Output (UPO)

A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0	UPO Output
0	0	1	0	x	x	x	x	x	x	x	x	Low
0	1	1	0	x	x	x	x	x	x	x	x	High

($\overline{LDAC}$ = X)

This command initiates the user-programmable logic output for controlling another device across an isolated interface. Example devices are gain control of an amplifier and a polarity output for a motor speed control.

No Operation (NOP)

A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	x	x	x	x	x	x	x	x

($\overline{LDAC}$ = X)

The NOP command (no operation) allows data to be shifted through the MAX534 shift register without affecting the input or DAC registers. This is useful in daisy chaining (also see the *Daisy Chaining Devices* section).

+5V, Low-Power, 8-Bit Quad DAC with Rail-to-Rail Output Buffers

For this command, the data bits are "Don't Cares." As an example, three MAX534s are daisy chained (A, B, and C), and devices A and C need to be updated. The 36-bit-wide command would consist of one 12-bit word for device C, followed by an NOP instruction for device B and a third 12-bit word with data for device A. At $\overline{CS}$'s rising edge, device B will not change state.

Set DOUT Phase—SCLK Rising (Mode 1)

A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	0	x	x	x	x	x	x	x	x

($\overline{LDAC}$ = x)

The mode 1 command resets the serial-output DOUT to transition at SCLK's rising edge. Once this command is issued, DOUT's phase is latched and will not change except on power-up or if the specific command to set the phase to falling edge is issued.

This command also loads all DAC registers with the contents of their respective input registers, and is identical to the "$\overline{LDAC}$" command.

Set DOUT Phase—SCLK Falling (Mode 0, Default)

A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	x	x	x	x	x	x	x	x

($\overline{LDAC}$ = x)

This command resets DOUT to transition at SCLK's falling edge. The same command also updates all DAC registers with the contents of their respective input registers, identical to the "$\overline{LDAC}$" command.

$\overline{LDAC}$ Operation (Hardware)

$\overline{LDAC}$ is typically used in 4-wire interfaces (Figure 7). This command is level sensitive, and allows asynchronous hardware control of the DAC outputs. With $\overline{LDAC}$ low the DAC registers are transparent, and any time an input register is updated, the DAC output immediately follows.

Clear DACs with $\overline{CLR}$

Strobing the $\overline{CLR}$ pin low causes an asynchronous clear of input and DAC registers and sets all DAC outputs to zero. Similar to the $\overline{LDAC}$ pin, $\overline{CLR}$ can be invoked at any time, typically when the device is not selected ($\overline{CS}$ = H). When the DAC data is all zeros, this function is equivalent to the "Update all DACs from Shift Registers" command.

Serial Data Output

DOUT is the internal shift register's output. DOUT can be programmed to clock out data on SCLK's falling edge (mode 0) or rising edge (mode 1). In mode 0, output data lags input data by 12.5 clock cycles, maintaining compatibility with Microwire and SPI. In mode 1, output data lags input data by 12 clock cycles. On power-up, DOUT defaults to mode 0 timing. DOUT never three-states; it always actively drives either high or low and remains unchanged when $\overline{CS}$ is high.

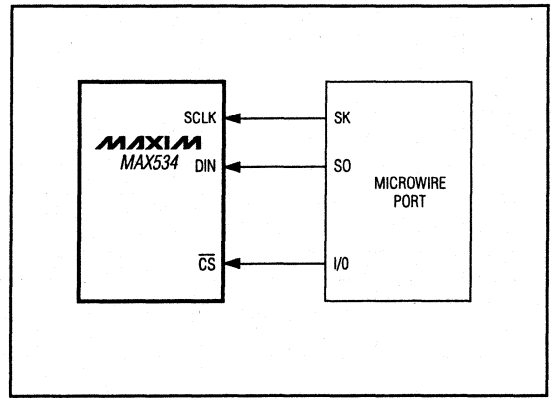


Figure 4. Connections for Microwire

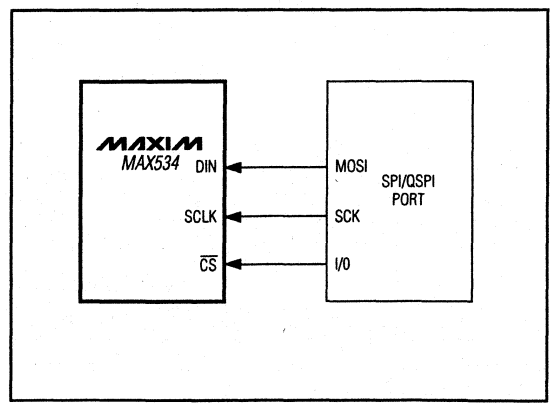


Figure 5. Connections for SPI/QSPI

+5V, Low-Power, 8-Bit Quad DAC with Rail-to-Rail Output Buffers

Interfacing to the Microprocessor

The MAX534 is Microwire™ and SPI™/QSPI™ compatible (Figures 4 and 5). For SPI and QSPI, clear the CPOL and CPHA configuration bits (CPOL = CPHA = 0). The SPI/QSPI CPOL = CPHA = 1 configuration can also be used if the DOUT output is ignored.

The MAX534 can interface with Intel's 80C5X/80C3X family in mode 0 if the SCLK clock polarity is inverted. More universally, if a serial port is not available, three lines from one of the parallel ports can be used for bit manipulation.

Digital feedthrough at the voltage outputs is greatly minimized by operating the serial clock only to update the registers. The clock idle state is low.

Daisy-Chaining Devices

Any number of MAX534s can be daisy-chained by connecting DOUT of one device to DIN of the following device in the chain. The NOP instruction (Table 1) allows data to be passed from DIN to DOUT without changing the input or DAC registers of the passing device. A 3-wire interface updates daisy-chained or individual MAX534s simultaneously by bringing $\overline{CS}$ high (Figure 6).

Analog Section

DAC Operation

The MAX534 uses a matrix decoding architecture for the DACs, which saves power in the overall system. The external reference voltage is divided down by a resistor string placed in a matrix fashion. Row and column decoders select the appropriate tab from the resistor string to provide the needed analog voltages. The resistor string presents a code-independent input impedance to the reference and guarantees a monotonic output. Figure 8 shows a simplified diagram of the four DACs.

Reference Input

The voltage at REF sets the full-scale output voltage for all four DACs. The 460kΩ typical input impedance at REF is code independent. The output voltage for any DAC can be represented by a digitally programmable voltage source as follows:

$$V_{OUT} = (NB \times V_{REF}) / 256$$

where NB is the numerical value of the DAC's binary input code.

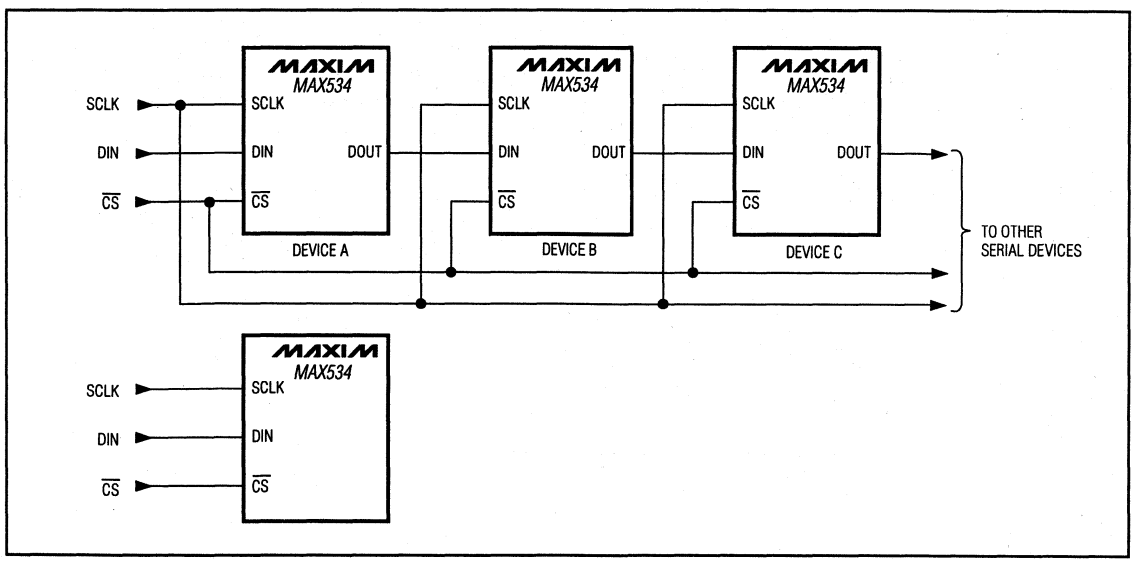


Figure 6. Daisy-chained or individual MAX534s are simultaneously updated by bringing $\overline{CS}$ high. Only three wires are required.

+5V, Low-Power, 8-Bit Quad DAC with Rail-to-Rail Output Buffers

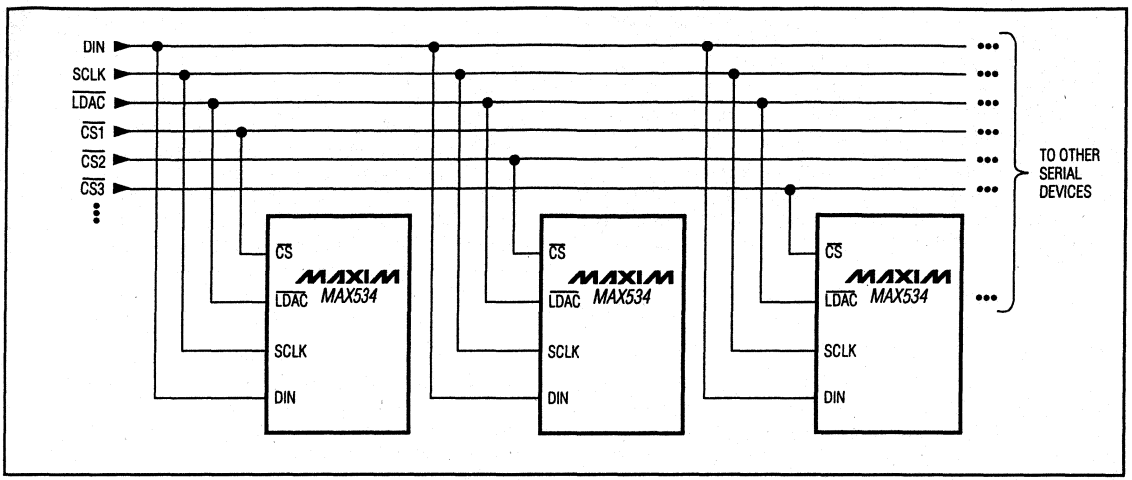


Figure 7. Multiple MAX534s sharing one DIN line. Simultaneously update by strobing LDAC, or specifically update by enabling an individual CS.

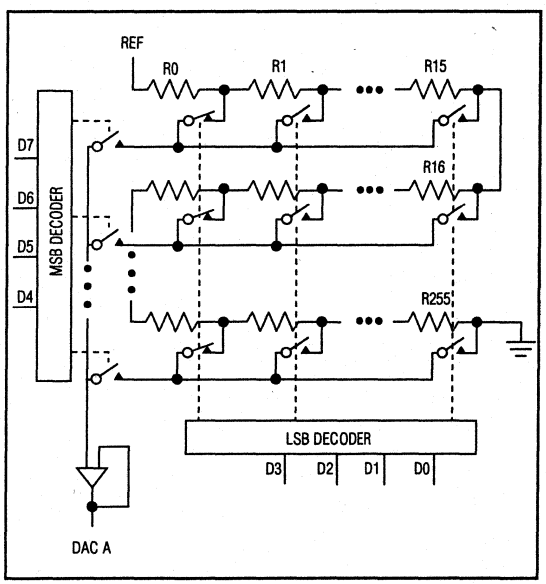


Figure 8. DAC Simplified Circuit Diagram

Output Buffer Amplifiers

All MAX534 voltage outputs are internally buffered by precision unity-gain followers that slew at about 0.6V/µs. The outputs can swing from GND to V_{DD}. With a 0V to +4V (or +4V to 0V) output transition, the amplifier outputs will typically settle to 1/2LSB in 8µs when loaded with 10kΩ in parallel with 100pF.

The buffer amplifiers are stable with any combination of resistive (≥10kΩ) or capacitive loads.

Applications Information

DAC Linearity and Voltage Offset

The output buffer can have a negative input offset voltage that would normally drive the output negative, but since there is no negative supply the output stays at 0V (Figure 9). When linearity is determined using the endpoint method, it is measured between zero code (all inputs 0) and full-scale code (all inputs 1) after offset and gain error are calibrated out. However, in single-supply operation the next code after zero may not change the output, so the lowest code that produces a positive output is the lower endpoint.

Power Sequencing

The voltage applied to REF should not exceed V_{DD} at any time. If proper power sequencing is not possible, connect an external Schottky diode between REF and V_{DD} to ensure compliance with the absolute maximum ratings. Do not apply signals to the digital inputs before the device is fully powered up.

Power-Supply Bypassing and Ground Management

Connect AGND and DGND together at the IC. This ground should then return to the highest-quality ground available. Bypass V_{DD} with a 0.1µF capacitor, located as close to V_{DD} and DGND as possible.

Careful PC board layout minimizes crosstalk among DAC outputs and digital inputs. Figure 10 shows suggested circuit board layout to minimize crosstalk.

Unipolar-Output, Two-Quadrant Multiplication

In unipolar operation, the output voltages and the reference input are the same polarity. Figure 11 shows the MAX534 unipolar configuration, and Table 2 shows the unipolar code.

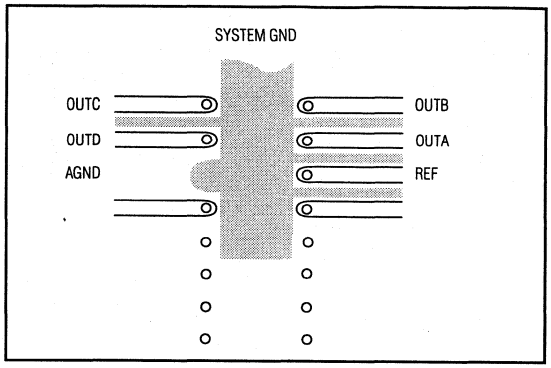


Figure 10. Suggested PC Board Layout for Minimizing Crosstalk (Bottom View)

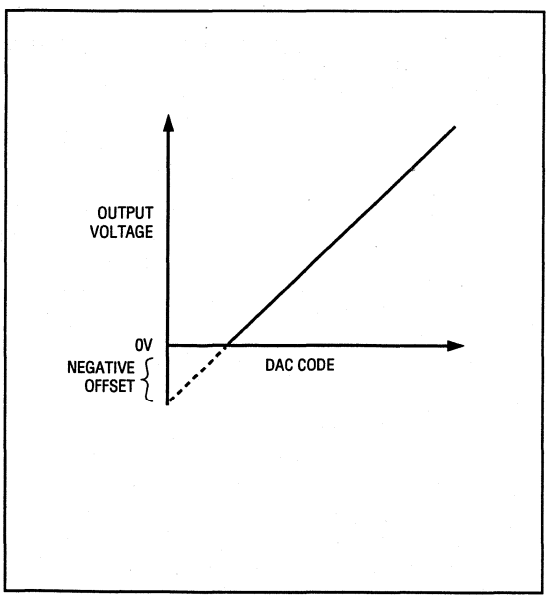


Figure 9. Effect of Negative Offset (Single Supply)

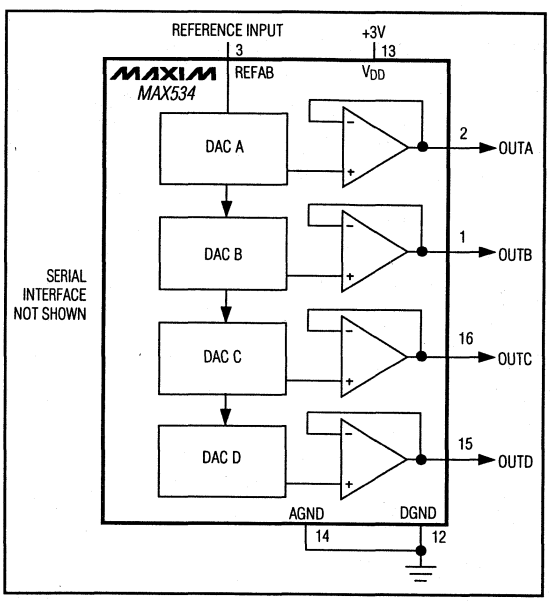


Figure 11. Unipolar Output Circuit

+5V, Low-Power, 8-Bit Quad DAC with Rail-to-Rail Output Buffers

Functional Diagram

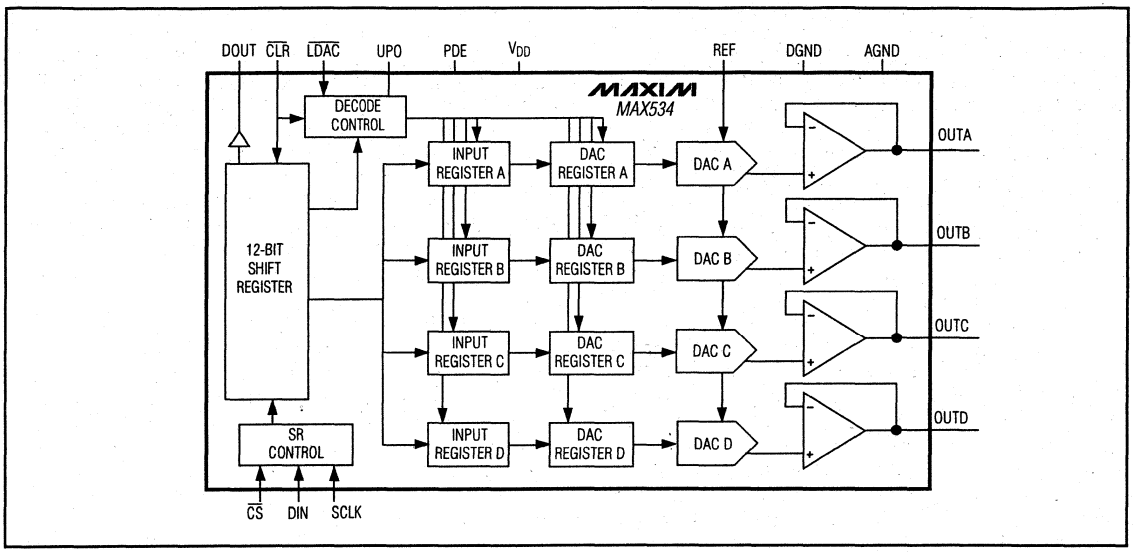


Table 2. Unipolar Code Table

DAC CONTENTS		ANALOG OUTPUT
MSB	LSB	
1111	1111	$+V_{REF}\left(\frac{255}{256}\right)$
1000	0001	$+V_{REF}\left(\frac{129}{256}\right)$
1000	0000	$+V_{REF}\left(\frac{128}{256}\right) = +\frac{V_{REF}}{2}$
0111	1111	$+V_{REF}\left(\frac{127}{256}\right)$
0000	0001	$+V_{REF}\left(\frac{1}{256}\right)$
0000	0000	0V

Note: 1LSB = $(V_{REF})(2^{-8}) = +V_{REF}\left(\frac{1}{256}\right)$

Chip Information

TRANSISTOR COUNT: 6821

19-1124; Rev 0; 9/96

MAXIM

Low-Power, 13-Bit Voltage-Output DAC with Serial Interface

General Description

The MAX535 combines a low-power, voltage-output, 13-bit digital-to-analog converter (DAC) and a precision output amplifier in an 8-pin package. The amplifier's output and inverting input are both available to the user. This provides specific gain configurations, remote sensing, and high output drive capacity, making the MAX535 ideal for a wide range of applications, including industrial-process-control. Other features include software shutdown and power-on reset to zero.

The serial interface is compatible with either SPI™/QSPI™ or Microwire™. The DAC has a double-buffered input organized as an input register followed by a DAC register. A 16-bit serial word loads data into the input registers. The DAC register can be updated independently or simultaneously with the input register. All logic inputs are TTL/CMOS-logic compatible and buffered with Schmitt triggers to allow direct interfacing to optocouplers.

Applications

Industrial Process Controls

Automatic Test Equipment

Digital Offset and Gain Adjustment

Motion Control

Remote Industrial Controls

Microprocessor-Controlled Systems

Features

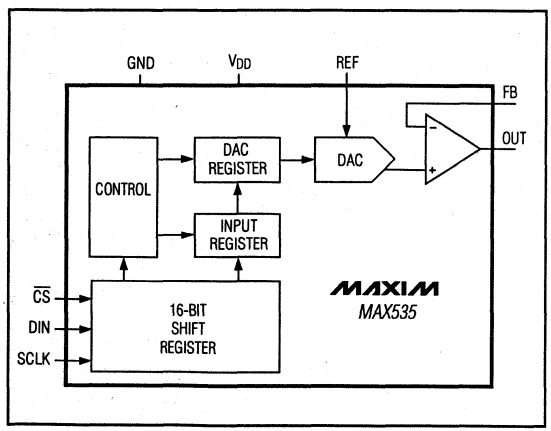
- ♦ **13-Bit DAC with Configurable Output Amplifier**
- ♦ **+5V Single-Supply Operation**
- ♦ **Low Supply Current: 0.28mA Normal Operation**
  4µA Shutdown Mode
- ♦ **Available in 8-Pin µMAX**
- ♦ **Power-On Reset Clears DAC Output to 0V**
- ♦ **SPI/QSPI and Microwire Compatible**
- ♦ **Schmitt-Trigger Digital Inputs for Direct Optocoupler Interface**

Ordering Information

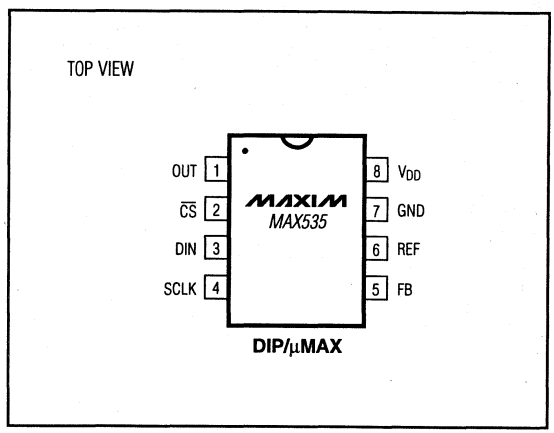
PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX535ACPA	0°C to +70°C	8 Plastic DIP	±1/2
MAX535BCPA	0°C to +70°C	8 Plastic DIP	±1
MAX535ACUA	0°C to +70°C	8 µMAX†	±1/2
MAX535BCUA	0°C to +70°C	8 µMAX	±1
MAX535BC/D	0°C to +70°C	Dice*	±1

**Dice are tested at +25°C, DC parameters only.*
†Contact factory for availability.
Ordering Information continued on last page.

Functional Diagram



Pin Configuration



DIP/µMAX

SPI and QSPI are trademarks of Motorola, Inc. Microwire is a trademark of National Semiconductor Corp.

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Low-Power, 13-Bit Voltage-Output DAC with Serial Interface

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V, +6V
REF, OUT, FB to GND .....-0.3V to (V_{DD} + 0.3V)
Digital Inputs to GND .....-0.3V to (V_{DD} + 0.3V)
Continuous Current into Any Pin.....±20mA
Continuous Power Dissipation (T_A = +70°C)
8 Plastic DIP (derate 6.90mW/°C above +70°C).....552mW
8 µMAX (derate 4.00mW/°C above +70°C).....330mW
8 CERDIP (derate 8.00mW/°C above +70°C).....640mW

Operating Temperature Ranges
MAX535_C_A.....0°C to +70°C
MAX535_E_A.....-40°C to +85°C
MAX535BMJA.....-55°C to +125°C
Storage Temperature Range.....-65°C to +150°C
Lead Temperature (soldering, 10sec).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±10%, REF = +2.5V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 8).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE—ANALOG SECTION						
Resolution	N		13			Bits
Integral Nonlinearity (Note 1)	INL	MAX535A			±0.5	LSB
		MAX535B			±1.0	
		MAX535MJA			±2.0	
Differential Nonlinearity	DNL	Guaranteed monotonic			±1.0	LSB
Offset Error	V_{OS}			±0.3	±8	mV
Offset-Error Tempco	TCV_{OS}			6		ppm/°C
Gain Error (Note 1)	GE			-0.5	±6	LSB
Gain-Error Tempco				1		ppm/°C
Power-Supply Rejection Ratio	PSRR	4.5V ≤ V_{DD} ≤ 5.5V			600	µV/V
REFERENCE INPUT						
Reference Input Range	V_{REF}		0		V_{DD} - 1.4	V
Reference Input Resistance	R_{REF}	Code dependent, minimum at code 1 555 hex	14	20		kΩ
MULTIPLYING-MODE PERFORMANCE						
Reference -3dB Bandwidth		V_{REF} = 0.67Vp-p		650		kHz
Reference Feedthrough		Input Code = all 0s, V_{REF} = 3.6Vp-p at 1kHz		-84		dB
Signal-to-Noise Plus Distortion Ratio	SINAD	V_{REF} = 1Vp-p at 25kHz		78		dB
DIGITAL INPUTS						
Input High Voltage	V_{IH}		2.4			V
Input Low Voltage	V_{IL}				0.8	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}		0.001	±0.5	µA
Input Capacitance	C_{IN}			8		pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±10%, GND = 0V, REF = +2.5V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 8).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate	SR			0.6		V/µs
Output Settling Time		To ±1/2LSB, V_{STEP} = 2.5V		16		µs
Output Voltage Swing		Rail-to-rail (Note 2)		0 to V_{DD}		V
Current into FB				0.001	0.1	µA
Time to Valid Operation on Start-Up				20		µs
Digital Feedthrough		$\overline{CS}$ = V_{DD}, DIN = 100kHz		5		nV-s
POWER SUPPLIES						
Supply Voltage	V_{DD}		4.5		5.5	V
Supply Current	I_{DD}	Note 3		0.28	0.4	mA
Supply Current in Shutdown		Note 3		4	20	µA
Reference Current in Shutdown				0.01	±0.5	µA
TIMING CHARACTERISTICS						
SCLK Clock Period	t_{CP}		100			ns
SCLK Pulse Width High	t_{CH}		40			ns
SCLK Pulse Width Low	t_{CL}		40			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		40			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
DIN Setup Time	t_{DS}		40			ns
DIN Hold Time	t_{DH}		0			ns
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CS0}		40			ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	t_{CS1}		40			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		100			ns

Note 1: Guaranteed from code 22 to code 8191 in unity-gain configuration.

Note 2: Accuracy is better than 0.5LSB for V_{OUT} = 8mV to V_{DD} - 100mV, guaranteed by a power-supply rejection test at the end points.

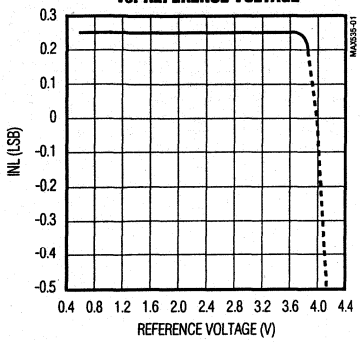
Note 3: R_L = ∞, digital inputs at GND or V_{DD}.

Low-Power, 13-Bit Voltage-Output DAC with Serial Interface

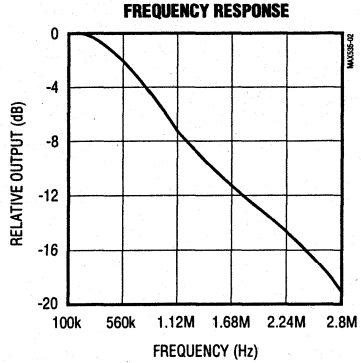
Typical Operating Characteristics

(V_{DD} = +5V, R_L = 5kΩ, C_L = 100pF, T_A = +25°C, unless otherwise noted.)

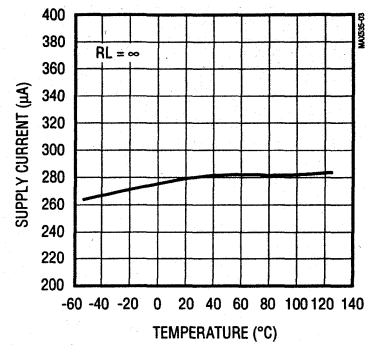
INTEGRAL NONLINEARITY vs. REFERENCE VOLTAGE



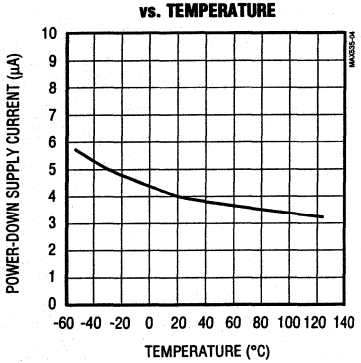
REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE



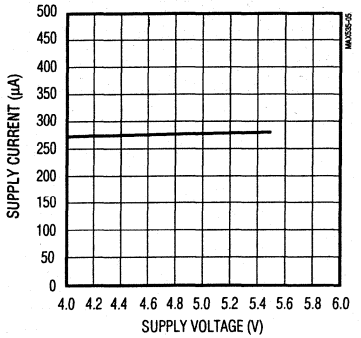
SUPPLY CURRENT vs. TEMPERATURE



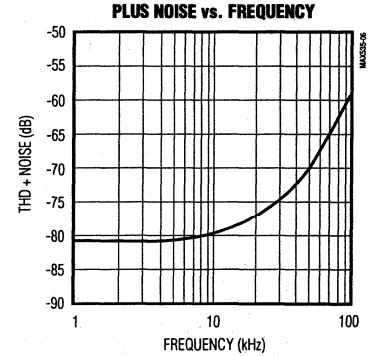
POWER-DOWN SUPPLY CURRENT vs. TEMPERATURE



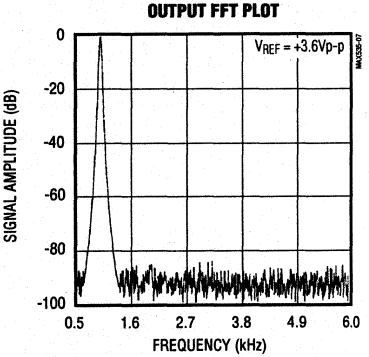
SUPPLY CURRENT vs. SUPPLY VOLTAGE



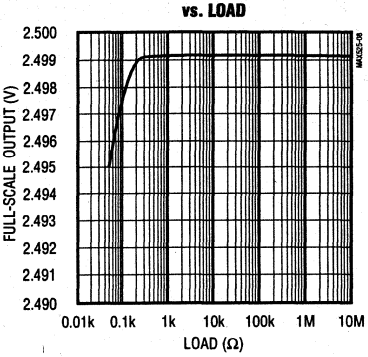
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



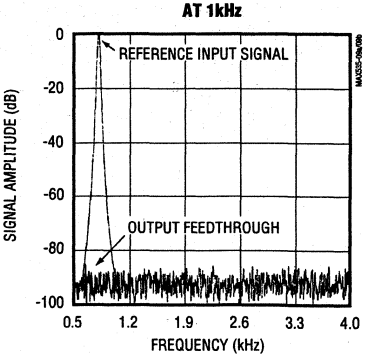
OUTPUT FFT PLOT



FULL-SCALE OUTPUT vs. LOAD



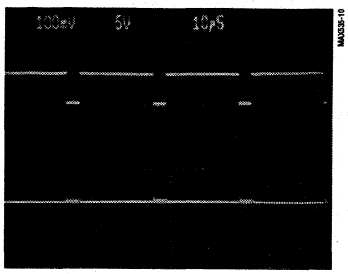
REFERENCE FEEDTHROUGH AT 1kHz



Typical Operating Characteristics (continued)

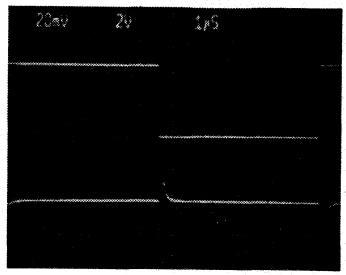
(V_{DD} = +5V, R_L = 5kΩ, C_L = 100pF, T_A = +25°C, unless otherwise noted.)

MAJOR-CARRY TRANSITION



10µs/div

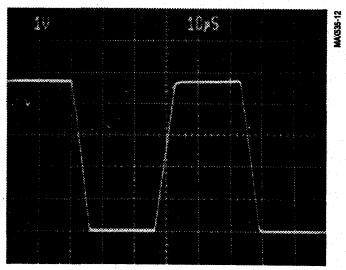
DIGITAL FEEDTHROUGH (f_{SCLK} = 100kHz)



2µs/div

CS = 5V

DYNAMIC RESPONSE



10µs/div

GAIN = 2 SWITCHING FROM CODE 0 TO 8040

Low-Power, 13-Bit Voltage-Output DAC with Serial Interface

Pin Description

PIN	NAME	FUNCTION
1	OUT	DAC Output Voltage
2	$\overline{CS}$	Chip-Select Input. Active low.
3	DIN	Serial-Data Input
4	SCLK	Serial-Clock Input
5	FB	DAC Output Amplifier Feedback
6	REF	Reference Voltage Input
7	GND	Ground
8	V_{DD}	Positive Power Supply

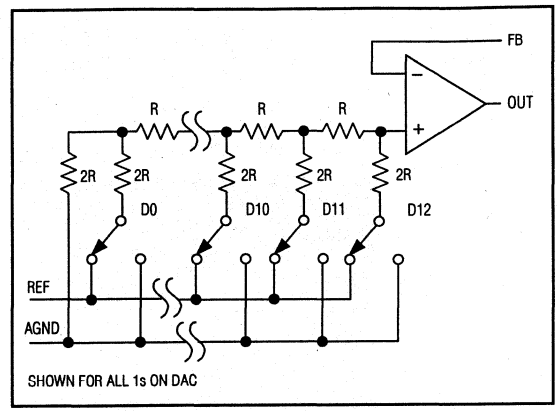


Figure 1. Simplified DAC Circuit Diagram

Detailed Description

The MAX535 contains a 13-bit, voltage-output digital-to-analog converter (DAC) that is easily addressed using a simple 3-wire serial interface. It includes a 16-bit shift register, and has a doubled-buffered input composed of an input register and a DAC register (see *Functional Diagram*). In addition to the voltage output, the amplifier's negative input is available to the user.

The DAC is an inverted R-2R ladder network that converts a 13-bit digital input into an equivalent analog output voltage in proportion to the applied reference voltage input. Figure 1 shows a simplified circuit diagram of the DAC.

Reference Inputs

The reference input accepts positive DC and AC signals. The voltage at the reference input sets the full-scale output voltage for the DAC. The reference input voltage range is 0V to (V_{DD} - 1.4V). The output voltage (V_{OUT}) is represented by a digitally programmable voltage source as:

$$V_{OUT} = (V_{REF} \times NB / 8192) \times Gain$$

where NB is the numeric value of the DAC's binary input code (0 to 8191), V_{REF} is the reference voltage, and Gain is the externally set voltage gain.

The impedance at the reference input is code dependent, ranging from a low value of 14kΩ when the DAC has an input code of 1555 hex, to a high value exceeding several giga ohms (leakage currents) with an input code of 0000 hex. Because the input impedance at the reference pin is code dependent, load regulation of the reference source is important.

The REF reference input has a 14kΩ guaranteed minimum input impedance. A voltage reference with a load regulation of 6ppm/mA, such as the MAX873, would typically deviate by 0.0062LSB (0.009LSB worst case) when driving the MAX535 reference input at 2.5V.

In shutdown mode, the MAX535's REF input enters a high-impedance state with a typical input leakage current of 0.01µA.

The reference input capacitance is also code dependent and typically ranges from 15pF (with an input code of all 0s) to 50pF (with an input code of all 1s).

Output Amplifier

The MAX535 DAC output is internally buffered by a precision amplifier with a typical slew rate of 0.6V/µs. Access to the output amplifier's inverting input provides the user greater flexibility in output gain setting/signal conditioning (see the *Applications Information* section).

With a full-scale transition at the MAX535 output, the typical settling time to ±1/2LSB is 16µs when loaded with 5kΩ in parallel with 100pF (loads less than 2kΩ degrade performance).

The MAX535 output amplifier's output dynamic responses and settling performances are shown in the *Typical Operating Characteristics*.

Low-Power, 13-Bit Voltage-Output DAC with Serial Interface

Shutdown Mode

The MAX535 features a software-programmable shutdown that reduces supply current to a typical value of 4µA. Writing 111XXXXXXXXXXXX as the input-control word puts the MAX535 in shutdown mode (Table 1).

In shutdown mode, the MAX535 output amplifiers and the reference inputs enter a high-impedance state. The serial interface remains active. Data in the input registers is retained in shutdown, allowing the MAX535 to recall the output states prior to entering shutdown. Exit shutdown mode by either recalling the previous configuration or by updating the DACs with new data. When powering up the device or bringing it out of shutdown, allow 20µs for the outputs to stabilize.

Serial-Interface Configurations

The MAX535's 3-wire serial interface is compatible with both Microwire™ (Figure 2) and SPI™/QSPI™ (Figure 3). The serial input word consists of three control bits followed by 13 data bits (MSB first), as shown in Figure 4. The 3-bit control code determines the MAX535's response outlined in Table 1.

The MAX535's digital inputs are double buffered. Depending on the command issued through the serial interface, the input register can be loaded without affecting the DAC register, the DAC register can be loaded directly, or the DAC register can be updated from the input register (Table 1).

Serial-Interface Description

The MAX535 requires 16 bits of serial data. Table 1 lists the serial-interface programming commands. For certain commands, the 13 data bits are "don't cares." Data is sent MSB first and can be sent in two 8-bit packets or one 16-bit word ($\overline{CS}$ must remain low until 16 bits are transferred). The serial data is composed of three control bits (C2, C1, C0), followed by the 13 data bits D12...D0 (Figure 4). The 3-bit control code determines:

- The register to be updated
- Configuration when exiting shutdown

Figure 5 shows the serial-interface timing requirements. The chip-select pin ($\overline{CS}$) must be low to enable the DAC's serial interface. When $\overline{CS}$ is high, the interface control circuitry is disabled. $\overline{CS}$ must go low at least t_{CSS} before the rising serial clock (SCLK) edge to properly clock in the first bit. When $\overline{CS}$ is low, data is clocked into the internal shift register via the serial-data input pin (DIN) on SCLK's rising edge. The maximum guaranteed clock frequency is 10MHz. Data is latched into the MAX535 input/DAC register on $\overline{CS}$'s rising edge.

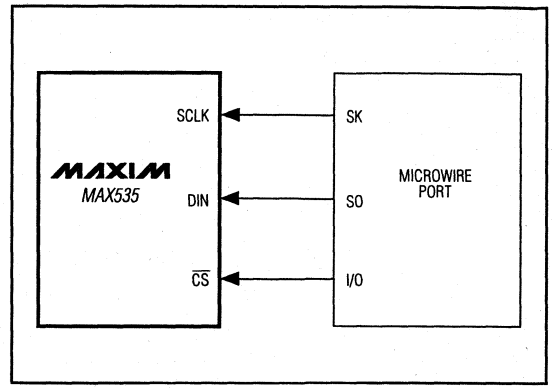


Figure 2. Connections for Microwire

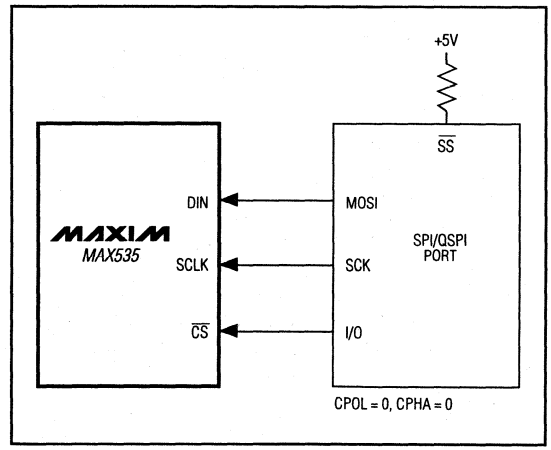


Figure 3. Connections for SPI/QSPI

MSB ..... LSB	
◄ 16 Bits of Serial Data ►	
Control Bits	Data Bits MSB ..... LSB
C2 .....C1 .....C0	D12 ..... D0
◄ 3 Control Bits ►	◄ 13 Data Bits ►

Figure 4. Serial-Data Format

Low-Power, 13-Bit Voltage-Output DAC with Serial Interface

Table 1. Serial-Interface Programming Commands

16-BIT SERIAL WORD				FUNCTION
C2	C1	C0	D12.....D0 MSB LSB	
X	0	0	13 bits of data	Load input register; DAC register immediately updated (exit shutdown).
X	0	1	13 bits of data	Load input register; DAC register unchanged.
X	1	0	XXXXXXXXXXXXX	Update DAC register from input register (exit shutdown; recall previous state).
1	1	1	XXXXXXXXXXXXX	Shutdown
0	1	1	XXXXXXXXXXXXX	No operation (NOP)

"X" = Don't care

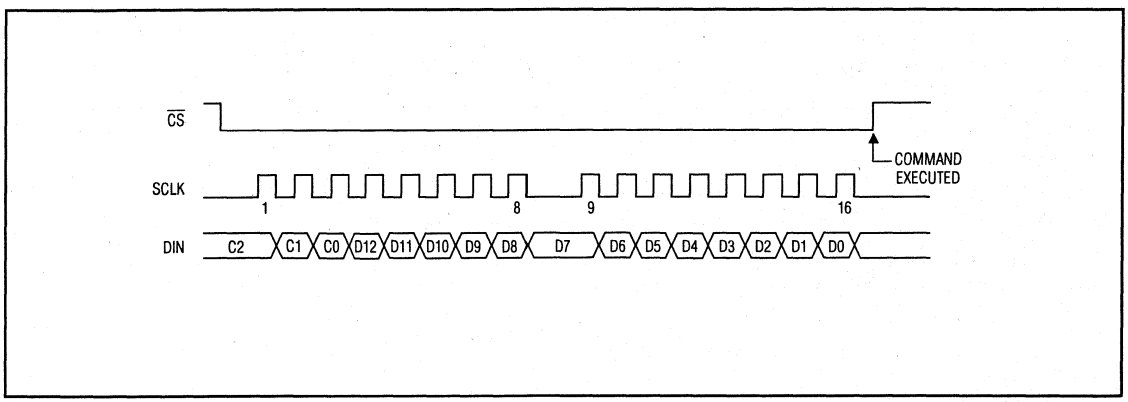


Figure 5. Serial-Interface Timing Diagram

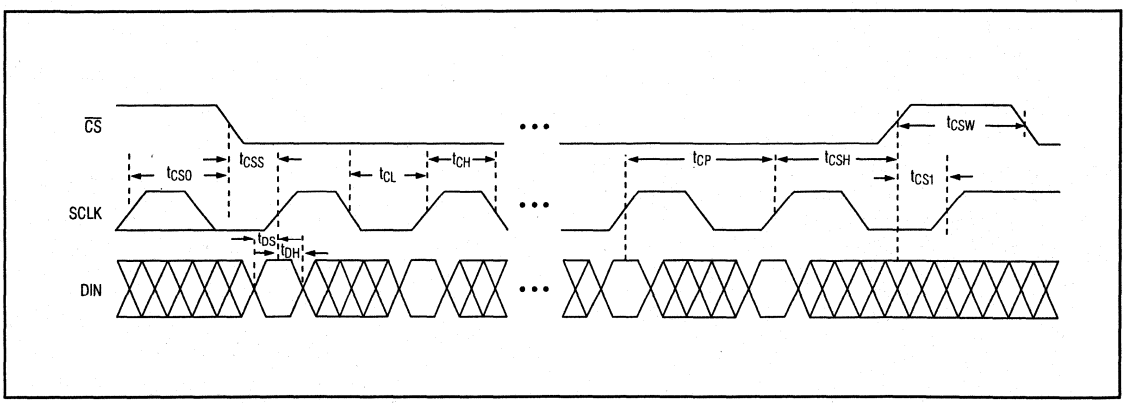


Figure 6. Detailed Serial-Interface Timing Diagram

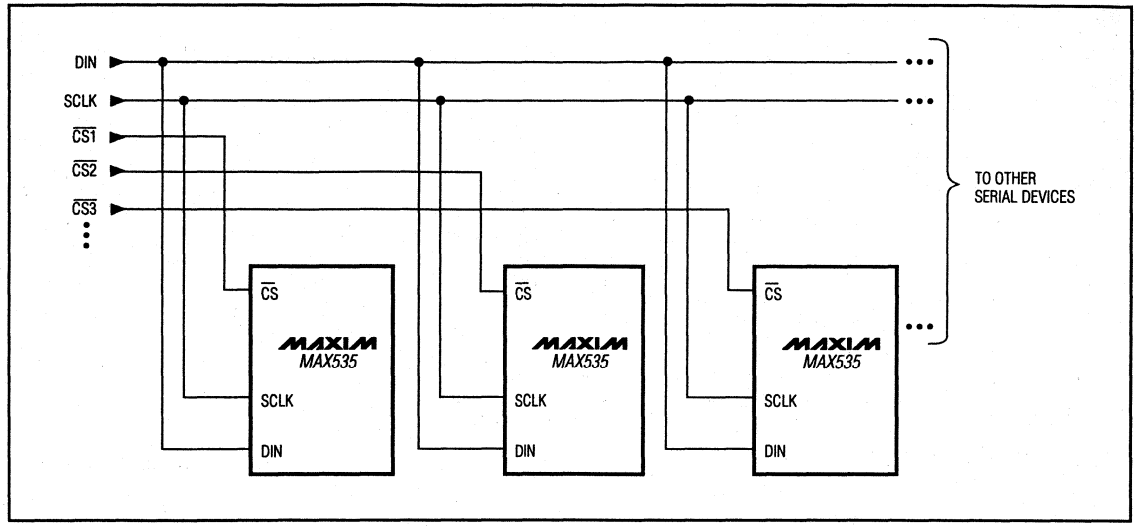


Figure 7. Multiple MAX535s Sharing Common DIN and SCLK Lines

Figure 7 shows a method of connecting several MAX535s. In this configuration, the clock and the data bus are common to all devices and separate chip-select lines are used for each IC.

Applications Information

Unipolar Output

For a unipolar output, the output voltage and the reference input have the same polarity. Figure 8 shows the MAX535 unipolar output circuit, which is also the typical operating circuit. Table 2 lists the unipolar output codes.

For rail-to-rail output, see Figure 9. This circuit shows the MAX535 with the output amplifier configured with a closed-loop gain of +2 to provide 0V to 5V full-scale range when a 2.5V reference is used.

Bipolar Output

The MAX535 output can be configured for bipolar operation using Figure 10's circuit.

$$V_{OUT} = V_{REF}[(2NB / 8192) - 1]$$

where NB is the numeric value of the DAC's binary input code. Table 3 shows digital codes (offset binary) and corresponding output voltage for Figure 10's circuit.

Table 2. Unipolar Code Table

DAC CONTENTS MSB		LSB	ANALOG OUTPUT
11111	1111	1111	$+V_{REF}\left(\frac{8191}{8192}\right)$
10000	0000	0001	$+V_{REF}\left(\frac{4097}{8192}\right)$
10000	0000	0000	$+V_{REF}\left(\frac{4096}{8192}\right) = \frac{+V_{REF}}{2}$
01111	1111	1111	$+V_{REF}\left(\frac{4095}{8192}\right)$
00000	0000	0001	$+V_{REF}\left(\frac{1}{8192}\right)$
00000	0000	0000	0V

Using an AC Reference

In applications where the reference has AC-signal components, the MAX535 has multiplying capability within the reference input range specifications. Figure 11 shows a technique for applying a sine-wave signal to the reference input where the AC signal is offset before being applied to REF. The reference voltage must never be more negative than GND.

Low-Power, 13-Bit Voltage-Output DAC with Serial Interface

Table 3. Bipolar Code Table

DAC CONTENTS MSB LSB	ANALOG OUTPUT
11111 1111 1111	$+V_{REF}\left(\frac{4095}{4096}\right)$
10000 0000 0001	$+V_{REF}\left(\frac{1}{4096}\right)$
10000 0000 0000	0V
01111 1111 1111	$-V_{REF}\left(\frac{1}{4096}\right)$
00000 0000 0001	$-V_{REF}\left(\frac{4096}{4096}\right)$
00000 0000 0000	$-V_{REF}\left(\frac{4096}{4096}\right) = -V_{REF}$

Note: $1LSB = (V_{REF})\left(\frac{2}{8192}\right)$

The MAX535's total harmonic distortion plus noise (THD + N) is typically less than -78dB, given a 1Vp-p signal swing and input frequencies up to 25kHz. The typical -3dB frequency is 650kHz, as shown in the *Typical Operating Characteristics* graphs.

Digitally Programmable Current Source

The circuit of Figure 12 places an NPN transistor (2N3904 or similar) within the op-amp feedback loop to implement a digitally programmable, unidirectional current source. This circuit can be used to drive 4mA to 20mA current loops, which are commonly used in industrial-control applications. The output current is calculated with the following equation:

$$I_{OUT} = (V_{REF} / R) \times (NB / 8192)$$

where NB is the numeric value of the DAC's binary input code and R is the sense resistor shown in Figure 12.

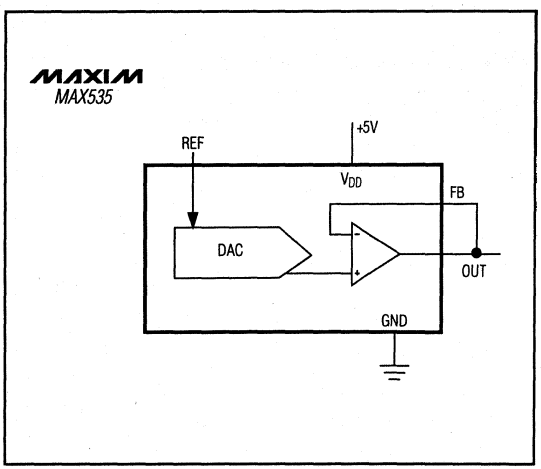


Figure 8. Unipolar Output Circuit

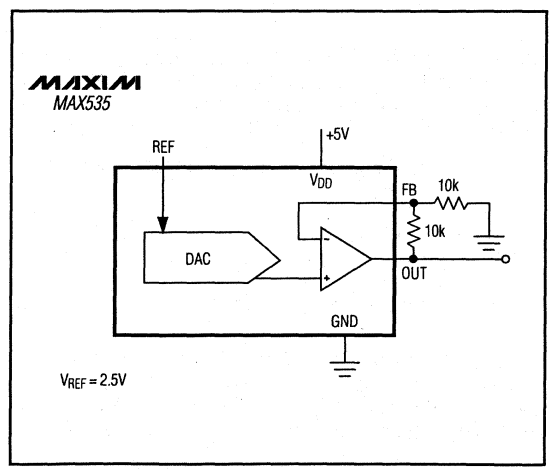


Figure 9. Unipolar Rail-to-Rail Output Circuit

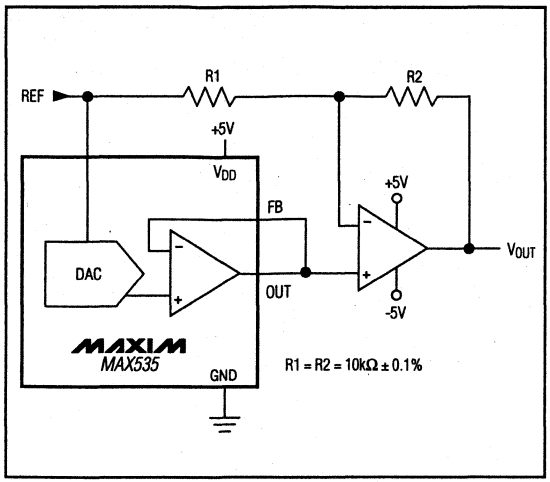


Figure 10. Bipolar Output Circuit

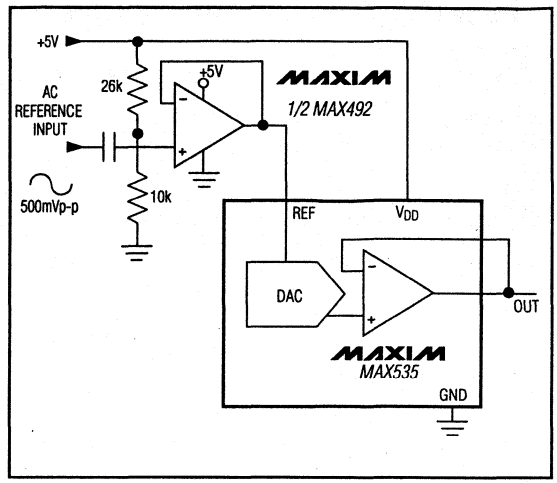


Figure 11. AC Reference Input Circuit

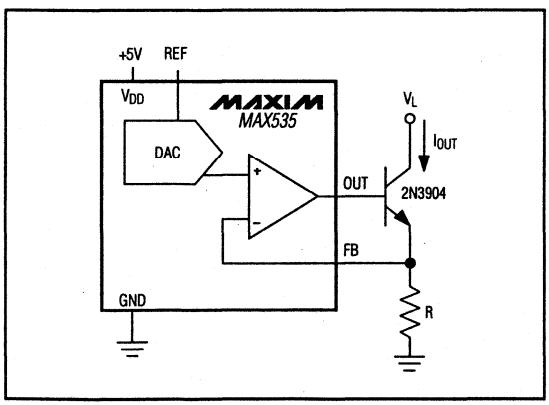


Figure 12. Digitally Programmable Current Source

Power-Supply Considerations

On power-up, the input and DAC registers are cleared (set to zero code).

For rated MAX535 performance, REF should be at least 1.4V below V_{DD}. Bypass V_{DD} with a 4.7µF capacitor in parallel with a 0.1µF capacitor to GND. Use short lead lengths and place the bypass capacitors as close to the supply pins as possible.

Grounding and Layout Considerations

Digital or AC transient signals on GND can create noise at the analog output. Tie GND to the highest-quality ground available.

Good printed circuit board ground layout minimizes crosstalk between the DAC output, reference input, and digital input. Reduce crosstalk by keeping analog lines away from digital lines. Wire-wrapped boards are not recommended.

Low-Power, 13-Bit Voltage-Output DAC with Serial Interface

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSBs)
MAX535AEPA	-40°C to +85°C	8 Plastic DIP	±1/2
MAX535BEPA	-40°C to +85°C	8 Plastic DIP	±1
MAX535AEUA	-40°C to +85°C	8 µMAX	±1/2
MAX535BEUA	-40°C to +85°C	8 µMAX	±1
MAX535BMJA	-55°C to +125°C	8 CERDIP**	±2

***Contact factory for availability and processing to MIL-STD-883.*

Chip Information

TRANSISTOR COUNT: 1677

19-1082; Rev 1; 9/96

MAXIM

+5V, Serial-Input, Voltage-Output, 16-Bit DACs

General Description

The MAX541/MAX542 are serial-input, voltage-output, 16-bit digital-to-analog converters (DACs) that operate from a single +5V supply. They provide 16-bit performance (±1LSB INL and DNL) over temperature without any adjustments. The DAC output is unbuffered, resulting in a low supply current of 0.3mA and a low offset error of 1LSB.

The DAC output range is 0V to V_{REF}. For bipolar operation, matched scaling resistors are provided in the MAX542 for use with an external precision op amp (such as the MAX400) generating a ±V_{REF} output swing. The MAX542 also includes Kelvin-sense connections for the reference and analog ground pins to reduce layout sensitivity.

A 16-bit serial word is used to load data into the DAC latch. The 6.25MHz, 3-wire serial interface is compatible with SPI™/QSPI™/Microwire™, and it also interfaces directly with optocouplers for applications requiring isolation. A power-on reset circuit clears the DAC output to 0V (unipolar mode) when power is initially applied.

The MAX541 is available in 8-pin plastic DIP and SO packages. The MAX542 is available in 14-pin plastic DIP and SO packages.

Applications

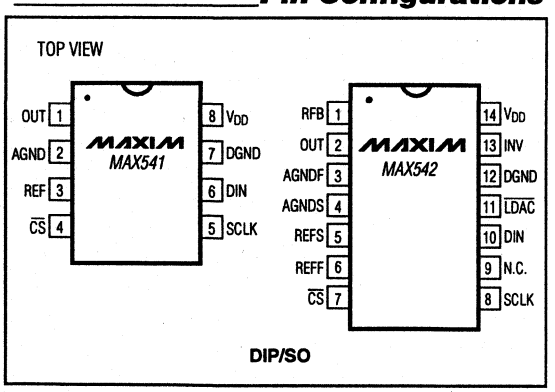
High-Resolution Offset and Gain Adjustment

Industrial Process Control

Automated Test Equipment

Data Acquisition Systems

Pin Configurations



DIP/SO

Features

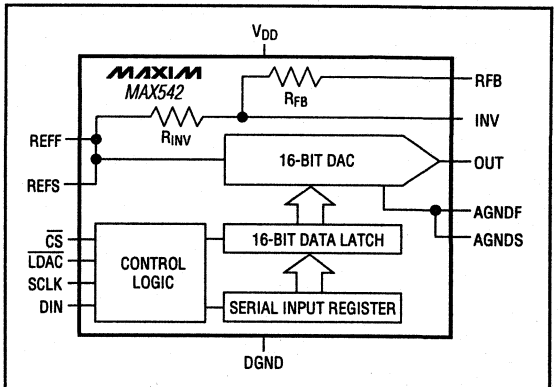
- ♦ **Full 16-Bit Performance Without Adjustments**
- ♦ **+5V Single-Supply Operation**
- ♦ **Low Power: 1.5mW**
- ♦ **1µs Settling Time**
- ♦ **Unbuffered Voltage Output Directly Drives 60kΩ Loads**
- ♦ **SPI/QSPI/Microwire-Compatible Serial Interface**
- ♦ **Power-On Reset Circuit Clears DAC Output to 0V (unipolar mode)**
- ♦ **Schmitt Trigger Inputs for Direct Optocoupler Interface**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX541ACPA	0°C to +70°C	8 Plastic DIP	±1
MAX541BCPA	0°C to +70°C	8 Plastic DIP	±2
MAX541CCPA	0°C to +70°C	8 Plastic DIP	±4
MAX541ACSA	0°C to +70°C	8 SO	±1
MAX541BCSA	0°C to +70°C	8 SO	±2
MAX541CCSA	0°C to +70°C	8 SO	±4

Ordering Information continued at end of data sheet.

Functional Diagrams



Functional Diagrams continued at end of data sheet.

SPI and QSPI are trademarks of Motorola, Inc.
Microwire is a trademark of National Semiconductor Corp.

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+5V, Serial-Input, Voltage-Output, 16-Bit DACs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND .....-0.3V to +6V
$\overline{CS}$, SCLK, DIN, $\overline{LDAC}$ to DGND .....-0.3V to +6V
REF, REFF, REFS to AGND_.....-0.3V to V_{DD} +0.3V
AGND, AGNDF, AGNDS to DGND.....-0.3V to +0.3V
OUT, INV to AGND_, DGND .....-0.3V to V_{DD}
RFB to AGND_, DGND .....-6V to +6V
Maximum Current into Any Pin.....50mA
Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C).....727mW
8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C)...800mW
14-Pin SO (derate 8.33mW/°C above +70°C) 667mW
14-Pin Ceramic SB (derate 10.00mW/°C above +70°C ..800mW
Operating Temperature Ranges
MAX541 _C_ A/MAX542_C_D. .....0°C to +70°C
MAX541 _E_ A/MAX542_E_D.....-40°C to +85°C
MAX542CMJD .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±5%, $V_{REF_}$ = 2.5V, AGND_ = DGND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE—ANALOG SECTION (R_L = ∞)							
Resolution	N			16			Bits
Integral Nonlinearity	INL	V_{DD} = 5V	MAX54_A		±0.5	±1.0	LSB
			MAX54_B		±0.5	±2.0	
			MAX54_C		±0.5	±4.0	
Differential Nonlinearity	DNL	Guaranteed monotonic			±0.5	±1.0	LSB
Zero-Code Offset Error	ZSE	T_A = +25°C				±1	LSB
		T_A = T_{MIN} to T_{MAX}				±2	
Zero-Code Tempco	ZS_{TC}	T_A = T_{MIN} to T_{MAX}			±0.05		ppm/°C
Gain Error (Note 1)		T_A = +25°C				±5	LSB
		T_A = T_{MIN} to T_{MAX}				±10	
Gain-Error Tempco					±0.1		ppm/°C
DAC Output Resistance	R_{OUT}	(Note 2)			6.25		kΩ
Bipolar Resistor Matching		MAX542	R_{FB}/R_{INV}		1.0		
			Ratio error			±0.015	%
Bipolar Zero Offset Error		MAX542	T_A = +25°C			±10	LSB
			T_A = T_{MIN} to T_{MAX}			±20	
Bipolar Zero Tempco	BZS_{TC}	MAX542			±0.5		ppm/°C
Power-Supply Rejection	PSR	4.75V ≤ V_{DD} ≤ 5.25V				±1.0	LSB
REFERENCE INPUT							
Reference Input Range	V_{REF}	(Note 3)		2.0		3.0	V
Reference Input Resistance (Note 4)	R_{REF}	Unipolar Mode		11.5			kΩ
		MAX542, Bipolar Mode		9.0			
DYNAMIC PERFORMANCE—ANALOG SECTION (R_L = ∞, unipolar mode)							
Voltage-Output Slew Rate	SR	C_L = 10pF (Note 5)			25		V/µs
Output Settling Time		to ±½LSB of FS, C_L = 10pF			1		µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±5%, $V_{REF_}$ = 2.5V, AGND_ = DGND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DAC Glitch Impulse		Major-carry transition		10		nV-s
Digital Feedthrough		Code = 0000hex; $\overline{CS}$ = V_{DD}; $\overline{LDAC}$ = 0V; SCLK, DIN = 0V to V_{DD} levels		10		nV-s
DYNAMIC PERFORMANCE—REFERENCE SECTION						
Reference -3dB Bandwidth	BW	Code = FFFF hex		1		MHz
Reference Feedthrough		Code = 0000 hex, V_{REF} = 1Vp-p at 100kHz		1		mVp-p
Signal-to-Noise Ratio	SNR			92		dB
Reference Input Capacitance	C_{IN}	Code = 0000 hex		75		pF
		Code = FFFF hex		120		
STATIC PERFORMANCE—DIGITAL INPUTS						
Input High Voltage	V_{IH}		2.4			V
Input Low Voltage	V_{IL}				0.8	V
Input Current	I_{IN}	V_{IN} = 0V			±1	µA
Input Capacitance	C_{IN}	(Note 6)			10	pF
Hysteresis Voltage	V_H			0.40		V
POWER SUPPLY						
Positive Supply Range	V_{DD}		4.75		5.25	V
Positive Supply Current	I_{DD}			0.3	1.1	mA
Power Dissipation	PD			1.5		mW

TIMING CHARACTERISTICS

(V_{DD} = +5V ±5%, $V_{REF_}$ = 2.5V, AGND_ = DGND = 0V, CMOS inputs, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Frequency	f_{CLK}				6.25	MHz
SCLK Pulse Width High	t_{CH}		80			ns
SCLK Pulse Width Low	t_{CL}		80			ns
$\overline{CS}$ Low to SCLK High Setup	t_{CSS0}		50			ns
$\overline{CS}$ High to SCLK High Setup	t_{CSS1}		50			ns
SCLK High to $\overline{CS}$ Low Hold	t_{CSH0}	(Note 6)	30			ns
SCLK High to $\overline{CS}$ High Hold	t_{CSH1}		80			ns
DIN to SCLK High Setup	t_{DS}		40			ns
DIN to SCLK High Hold	t_{DH}		0			ns
$\overline{LDAC}$ Pulse Width	$t_{\overline{LDAC}}$	MAX542	50			ns
$\overline{CS}$ High to $\overline{LDAC}$ Low Setup	t_{LDACS}	MAX542 (Note 6)	50			ns
V_{DD} High to $\overline{CS}$ Low (power-up delay)				20		µs

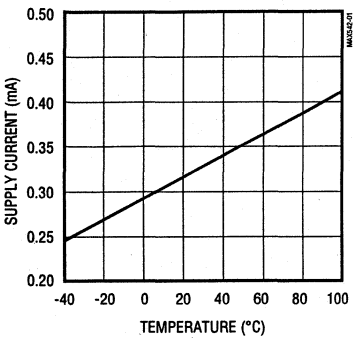
Note 1: Gain Error tested at V_{REF} = 2.0V, 2.5V, and 3.0V.
Note 2: R_{OUT} tolerance is typically ±20%.
Note 3: Min/max range guaranteed by gain-error test. Operation outside min/max limits will result in degraded performance.
Note 4: Reference input resistance is code dependent, minimum at 8555 hex.
Note 5: Slew-rate value is measured from 0% to 63%.
Note 6: Guaranteed by design. Not production tested.

+5V, Serial-Input, Voltage-Output, 16-Bit DACs

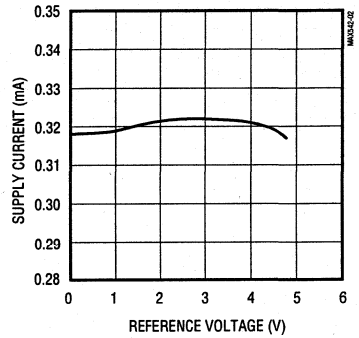
Typical Operating Characteristics

(V_{DD} = 5V, $V_{REF_}$ = 2.5V, T_A = +25°C, unless otherwise noted.)

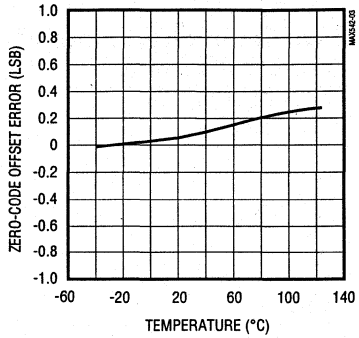
SUPPLY CURRENT vs. TEMPERATURE



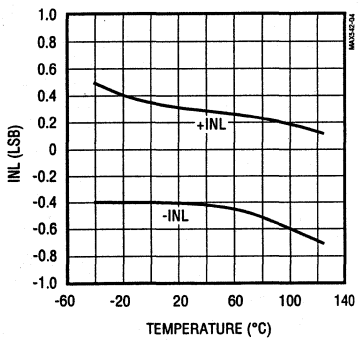
SUPPLY CURRENT vs. REFERENCE VOLTAGE



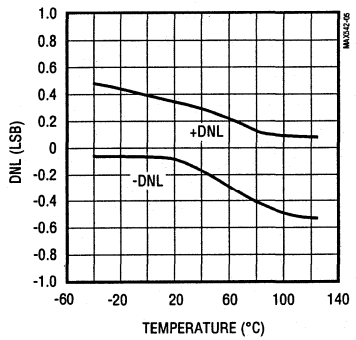
ZERO-CODE OFFSET ERROR vs. TEMPERATURE



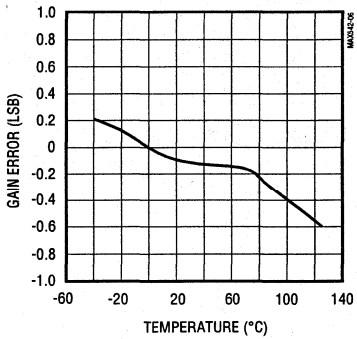
INTEGRAL NONLINEARITY vs. TEMPERATURE



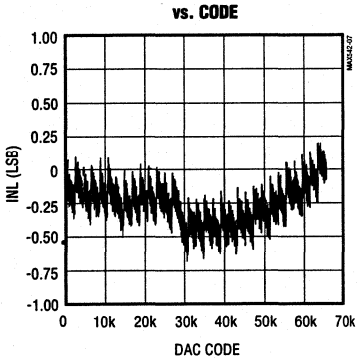
DIFFERENTIAL NONLINEARITY vs. TEMPERATURE



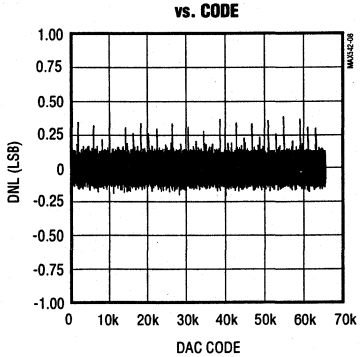
GAIN ERROR vs. TEMPERATURE



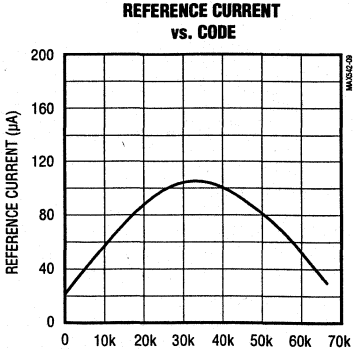
INTEGRAL NONLINEARITY vs. CODE



DIFFERENTIAL NONLINEARITY vs. CODE



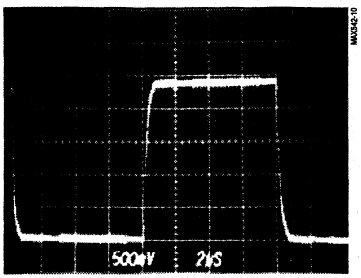
REFERENCE CURRENT vs. CODE



Typical Operating Characteristics (continued)

(V_{DD} = 5V, $V_{REF_}$ = 2.5V, T_A = +25°C, unless otherwise noted.)

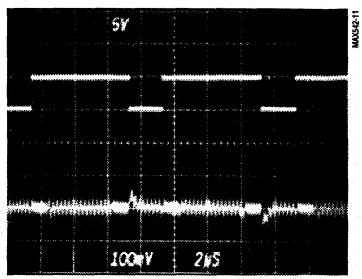
FULL-SCALE STEP RESPONSE



2µs/div

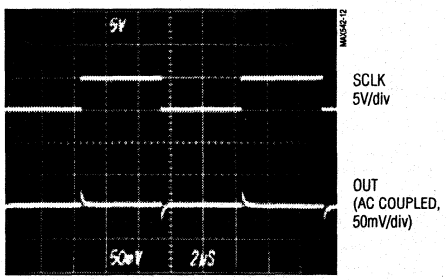
$R_L = \infty$, C_L = 10pF

MAJOR-CARRY OUTPUT GLITCH



2µs/div

DIGITAL FEEDTHROUGH



2µs/div

CODE = 0000 hex

Pin Descriptions

MAX541

PIN	NAME	FUNCTION
1	OUT	DAC Output Voltage
2	AGND	Analog Ground
3	REF	Voltage Reference Input. Connect to external +2.5V reference.
4	$\overline{CS}$	Chip-Select Input
5	SCLK	Serial Clock Input. Duty cycle must be between 40% and 60%.
6	DIN	Serial Data Input
7	DGND	Digital Ground
8	V_{DD}	+5V Supply Voltage

+5V, Serial-Input, Voltage-Output, 16-Bit DACs

Pin Descriptions (continued)

MAX542

PIN	NAME	FUNCTION
1	RFB	Feedback Resistor. Connect to external op amp's output in bipolar mode.
2	OUT	DAC Output Voltage
3	AGNDF	Analog Ground (force)
4	AGNDS	Analog Ground (sense)
5	REFS	Voltage Reference Input (sense). Connect REFS to external 2.5V reference.
6	REFF	Voltage Reference Input (force). Connect REFF to external 2.5V reference.
7	$\overline{CS}$	Chip-Select Input
8	SCLK	Serial Clock Input. Duty cycle must be between 40% and 60%.
9	N.C.	No Connection. Not internally connected.
10	DIN	Serial Data Input
11	$\overline{LDAC}$	$\overline{LDAC}$ Input. A falling edge updates the internal DAC latch.
12	DGND	Digital Ground
13	INV	Junction of internal scaling resistors. Connect to external op amp's inverting input in bipolar mode.
14	V_{DD}	+5V Supply Voltage

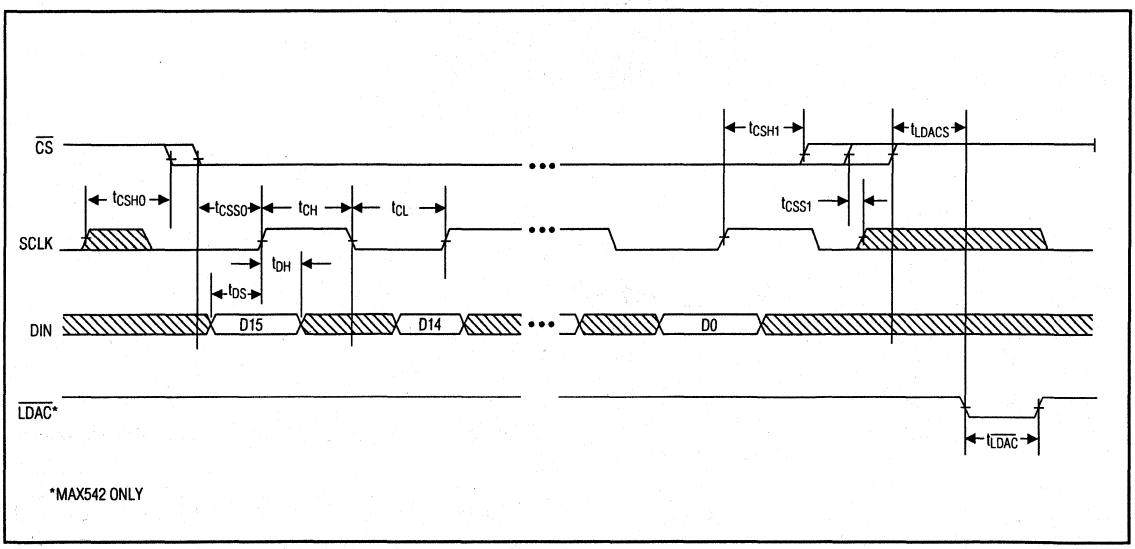


Figure 1. Timing Diagram

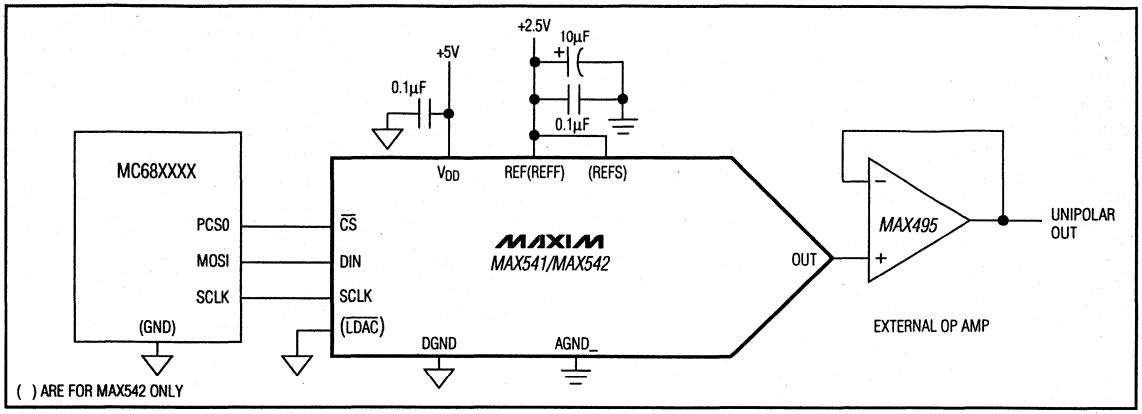


Figure 2a. Typical Operating Circuit—Unipolar Output

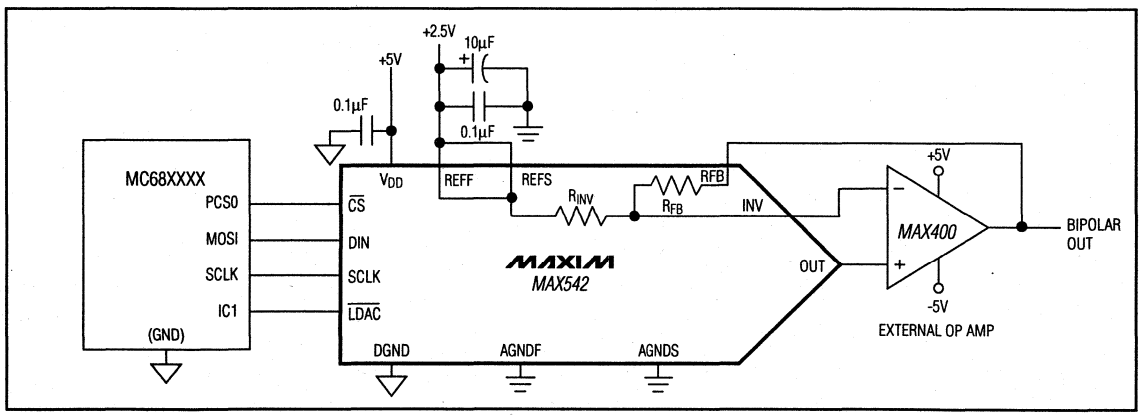


Figure 2b. Typical Operating Circuit—Bipolar Output

Detailed Description

The MAX541/MAX542 voltage-output, 16-bit digital-to-analog converters (DACs) offer full 16-bit performance with less than 1LSB integral linearity error and less than 1LSB differential linearity error, thus ensuring monotonic performance. Serial data transfer minimizes the number of package pins required.

The MAX541/MAX542 are composed of two matched DAC sections, with a 12-bit inverted R-2R DAC forming the 12 LSBs and the 4MSBs derived from 15 identically matched resistors. This architecture allows the lowest glitch energy to be transferred to the DAC output on major-carry transitions. It also lowers the DAC output impedance by a factor of eight compared to a standard R-2R ladder, allowing unbuffered operation in medium-load applications.

The MAX542 provides matched bipolar offset resistors, which connect to an external op amp for bipolar output swings (Figure 2b). For optimum performance, the MAX542 also provides a set of Kelvin connections to the voltage-reference and analog-ground inputs.

+5V, Serial-Input, Voltage-Output, 16-Bit DACs

Digital Interface

The MAX541/MAX542's digital interface is a standard 3-wire connection compatible with SPI™/QSPI™/Microwire™ interfaces. The chip-select input ($\overline{CS}$) frames the serial data loading at the data-input pin (DIN). Immediately following $\overline{CS}$'s high-to-low transition, the data is shifted synchronously and latched into the input register on the rising edge of the serial clock input (SCLK). After 16 data bits have been loaded into the serial input register, it transfers its contents to the DAC latch on $\overline{CS}$'s low-to-high transition (Figure 3a). Note that if $\overline{CS}$ is not kept low during the entire 16 SCLK cycles, data will be corrupted. In this case, reload the DAC latch with a new 16-bit word.

Alternatively, for the MAX542, $\overline{LDAC}$ allows the DAC latch to update asynchronously by pulling $\overline{LDAC}$ low after $\overline{CS}$ goes high (Figure 3b). Hold $\overline{LDAC}$ high during the data-loading sequence.

External Reference

The MAX541/MAX542 operate with external voltage references from 2V to 3V. The reference voltage determines the DAC's full-scale output voltage. Kelvin connections are provided with the MAX542 for optimum performance.

Power-On Reset

The MAX541/MAX542 have a power-on reset circuit to set the DAC's output to 0V in unipolar mode when V_{DD} is first applied. This ensures that unwanted DAC output voltages will not occur immediately following a system power-up, such as after a loss of power. In bipolar mode the DAC output is set to $-V_{REF}$.

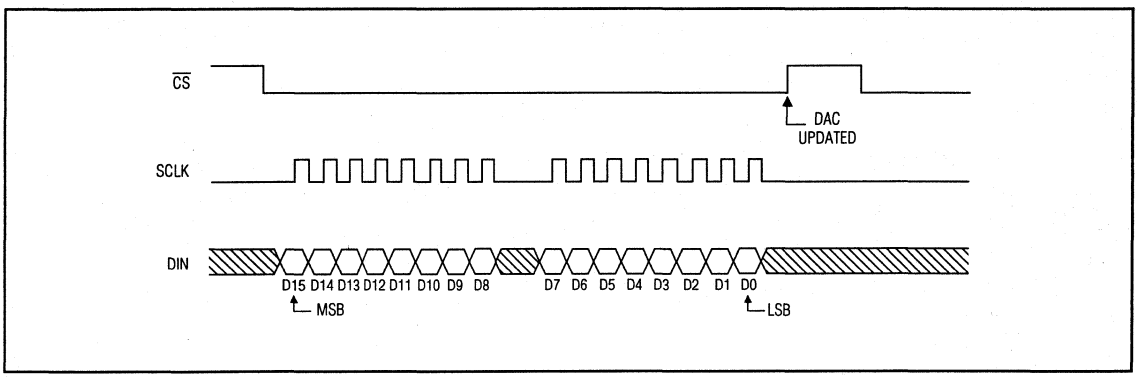


Figure 3a. MAX541/MAX542 3-Wire Interface Timing Diagram ($\overline{LDAC}$ = DGND FOR MAX542)

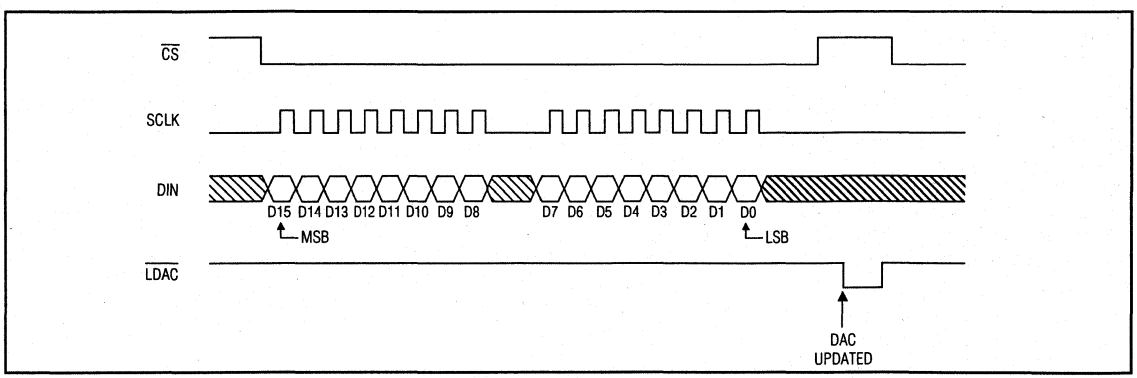


Figure 3b. MAX542 4-Wire Interface Timing Diagram

Applications Information

Reference and Analog Ground Inputs

The MAX541/MAX542 operate with external voltage references from 2V to 3V, and maintain 16-bit performance if certain guidelines are followed when selecting and applying the reference. Ideally, the reference's temperature coefficient should be less than 0.4ppm/°C to maintain 16-bit accuracy to within 1LSB over the 0°C to +70°C commercial temperature range. Since this converter is designed as an inverted R-2R voltage-mode DAC, the input resistance seen by the voltage reference is code dependent. The worst-case input-resistance variation is from 11.5kΩ (at code 8555 hex) to 200kΩ (at code 0000 hex). The maximum change in load current for a 2.5V reference is 2.5V / 11.5kΩ = 217µA; therefore, the required load regulation is 7ppm/mA for a maximum error of 0.1LSB. This implies a reference output impedance of less than 18mΩ. In addition, the impedance of the signal path from the voltage reference to the reference input must be kept low because it contributes directly to the load-regulation error.

The requirement for a low-impedance voltage reference is met with capacitor bypassing at the reference inputs and ground. A 0.1µF ceramic capacitor with short leads between REFF and AGNDF (MAX542), or REF and AGND (MAX541), provides high-frequency bypassing. A surface-mount ceramic chip capacitor is preferred because it has the lowest inductance. An additional 10µF between REFF and AGNDF (MAX542), or REF and AGND (MAX541), provides low-frequency bypassing. A low-ESR tantalum, film, or organic semiconductor capacitor works well. Leaded capacitors are acceptable because impedance is not as critical at lower frequencies. The circuit can benefit from even larger bypassing capacitors, depending on the stability of the external reference with capacitive loading. If separate force and sense lines are not used, tie the appropriate force and sense pins together close to the package.

AGND must also be low impedance, as load-regulation errors will be introduced by excessive AGND resistance. As in all high-resolution, high-accuracy applications, separate analog and digital ground planes yield the best results. Tie DGND to AGND at the AGND pin to form the "star" ground for the DAC system. Always refer remote DAC loads to this system ground for the best possible performance.

Unbuffered Operation

Unbuffered operation reduces power consumption as well as offset error contributed by the external output buffer. The R-2R DAC output is available directly at OUT, allowing 16-bit performance from $+V_{REF}$ to AGND without degradation at zero-scale. The DAC's output impedance is also low enough to drive medium loads (R_L > 60kΩ) without degradation of INL or DNL; only the gain error is increased by externally loading the DAC output.

External Output Buffer Amplifier

The requirements on the external output buffer amplifier change whether the DAC is used in the unipolar or bipolar mode of operation. In unipolar mode, the output amplifier is used in a voltage-follower connection. In bipolar mode (MAX542 only), the amplifier operates with the internal scaling resistors (Figure 2b). In each mode, the DAC's output resistance is constant and is independent of input code; however, the output amplifier's input impedance should still be as high as possible to minimize gain errors. The DAC's output capacitance is also independent of input code, thus simplifying stability requirements on the external amplifier.

In bipolar mode, a precision amplifier operating with dual power supplies (such as the MAX400) provides the $\pm V_{REF}$ output range. In single-supply applications, precision amplifiers with input common-mode ranges including AGND are available; however, their output swings do not normally include the negative rail (AGND) without significant degradation of performance. A single-supply op amp, such as the MAX495, is suitable if the application does not use codes near zero.

Since the LSBs for a 16-bit DAC are extremely small (38.15µV for V_{REF} = 2.5V), pay close attention to the external amplifier's input specification. The input offset voltage can degrade the zero-scale error and might require an output offset trim to maintain full accuracy if the offset voltage is greater than 1/2LSB. Similarly, the input bias current multiplied by the DAC output resistance (typically 6.25kΩ) contributes to the zero-scale error. Temperature effects also must be taken into consideration. Over the 0°C to +70°C commercial temperature range, the offset voltage temperature coefficient (referenced to +25°C) must be less than 0.42µV/°C to add less than 1/2LSB of zero-scale error. The external

+5V, Serial-Input, Voltage-Output, 16-Bit DACs

amplifier's input resistance forms a resistive divider with the DAC output resistance, which results in a gain error. To contribute less than 1/2LSB of gain error, the input resistance typically must be greater than:

$$6.25k\Omega \div \frac{1}{2}\left[\frac{1}{2^{16}}\right] = 819M\Omega.$$

The settling time is affected by the buffer input capacitance, the DAC's output capacitance, and PC board capacitance. The typical DAC output voltage settling time is 1µs for a full-scale step. Settling time can be significantly less for smaller step changes. Assuming a single time-constant exponential settling response, a full-scale step takes 12 time constants to settle to within 1/2LSB of the final output voltage. The time constant is equal to the DAC output resistance multiplied by the total output capacitance. The DAC output capacitance is typically 10pF. Any additional output capacitance will increase the settling time.

The external buffer amplifier's gain-bandwidth product is important because it increases the settling time by adding another time constant to the output response. The effective time constant of two cascaded systems, each with a single time-constant response, is approximately the root square sum of the two time constants. The DAC output's time constant is 1µs / 12 = 83ns, ignoring the effect of additional capacitance. If the time constant of an external amplifier with 1MHz bandwidth is 1 / 2π (1MHz) = 159ns, then the effective time constant of the combined system is:

$$\sqrt{\left[(83ns)^2 + (159ns)^2\right]} = 180ns$$

This suggests that the settling time to within 1/2LSB of the final output voltage, including the external buffer amplifier, will be approximately 12 x 180ns = 2.15µs.

Digital Inputs and Interface Logic

The digital interface for the 16-bit DAC is based on a 3-wire standard that is compatible with SPI, QSPI, and Microwire interfaces. The three digital inputs ($\overline{CS}$, DIN, and SCLK) load the digital input data serially into the DAC. $\overline{LDAC}$ (MAX542) updates the DAC output asynchronously.

All of the digital inputs include Schmitt-trigger buffers to accept slow-transition interfaces. This means that optocouplers can interface directly to the MAX541/MAX542 without additional external logic. The digital inputs are compatible with TTL/CMOS-logic levels.

Unipolar Configuration

Figure 2a shows the MAX541/MAX542 configured for unipolar operation with an external op amp. The op amp is set for unity gain, and Table 1 shows the codes for this circuit.

Bipolar Configuration

Figure 2b shows the MAX542 configured for bipolar operation with an external op amp. The op amp is set for unity gain with an offset of $-1/2V_{REF}$. Table 2 shows the offset binary codes for this circuit.

Power-Supply Bypassing and Ground Management

For optimum system performance, use printed circuit boards with separate analog and digital ground planes. Wire-wrap boards are not recommended. Connect the two ground planes together at the low-impedance power-supply source. Connect DGND and AGND together at the IC. The best ground connection can be achieved by connecting the DAC's DGND and AGND pins together and connecting that point to the system analog ground plane. If the DAC's DGND is connected to the system digital ground, digital noise may get through to the DAC's analog portion.

Bypass V_{DD} with a 0.1µF ceramic capacitor connected between V_{DD} and AGND. Mount it with short leads close to the device. Ferrite beads can also be used to further isolate the analog and digital power supplies.

Table 1. Unipolar Code Table

DAC LATCH CONTENTS MSB LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111 1111	V_{REF} x (65,535 / 65,536)
1000 0000 0000 0000	V_{REF} x (32,768 / 65,536) = $1/2V_{REF}$
0000 0000 0000 0001	V_{REF} x (1 / 65,536)
0000 0000 0000 0000	0V

Table 2. Bipolar Code Table

DAC LATCH CONTENTS MSB LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111 1111	+V_{REF} x (32,767 / 32,768)
1000 0000 0000 0001	+V_{REF} x (1 / 32,768)
1000 0000 0000 0000	0V
0111 1111 1111 1111	-V_{REF} x (1 / 32,768)
0000 0000 0000 0000	-V_{REF} x (32,768 / 32,768) = -V_{REF}

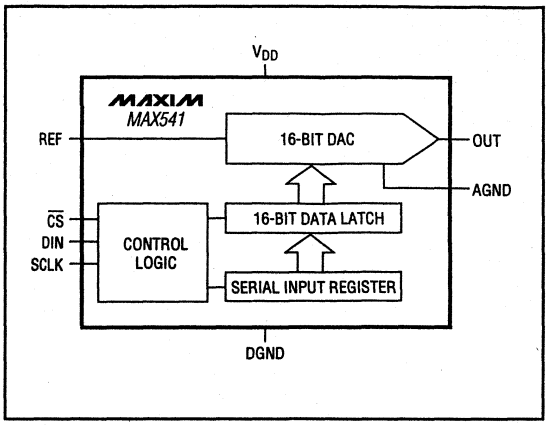
+5V, Serial-Input, Voltage-Output, 16-Bit DACs

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX541AEPA	-40°C to +85°C	8 Plastic DIP	±1
MAX541BEPA	-40°C to +85°C	8 Plastic DIP	±2
MAX541CEPA	-40°C to +85°C	8 Plastic DIP	±4
MAX541AESA	-40°C to +85°C	8 SO	±1
MAX541BESA	-40°C to +85°C	8 SO	±2
MAX541CESA	-40°C to +85°C	8 SO	±4
MAX542ACPD	0°C to +70°C	14 Plastic DIP	±1
MAX542BCPD	0°C to +70°C	14 Plastic DIP	±2
MAX542CCPD	0°C to +70°C	14 Plastic DIP	±4
MAX542ACSD	0°C to +70°C	14 SO	±1
MAX542BCSD	0°C to +70°C	14 SO	±2
MAX542CCSD	0°C to +70°C	14 SO	±4
MAX542BC/D	0°C to +70°C	Dice*	±2
MAX542AEPD	-40°C to +85°C	14 Plastic DIP	±1
MAX542BEPD	-40°C to +85°C	14 Plastic DIP	±2
MAX542CEPD	-40°C to +85°C	14 Plastic DIP	±4
MAX542AESD	-40°C to +85°C	14 SO	±1
MAX542BESD	-40°C to +85°C	14 SO	±2
MAX542CESD	-40°C to +85°C	14 SO	±4
MAX542CMJD	-55°C to +125°C	14 Ceramic SB**	±4

*Dice are tested at T_A = +25°C, DC parameters only.
**Contact factory for availability.

Functional Diagrams (continued)



Chip Information

TRANSISTOR COUNT: 2209
SUBSTRATE CONNECTED TO DGND

9

19-1088; Rev 2; 9/96

MAXIM

+5V, Serial-Input, Voltage-Output, 14-Bit DACs

General Description

The MAX544/MAX545 are serial-input, voltage-output, 14-bit digital-to-analog converters (DACs) that operate from a single +5V supply. They provide 14-bit performance (±0.5LSB INL and ±0.9LSB DNL) over temperature without any adjustments. The DAC output is unbuffered, resulting in a low supply current of 0.3mA and a low offset error of 0.6mV.

The DAC output range is 0V to V_{REF}. For bipolar operation, matched scaling resistors are provided in the MAX545 for use with an external precision op amp (such as the MAX400) generating a ±V_{REF} output swing. The MAX545 also includes Kelvin-sense connections for the reference and analog ground pins to reduce layout sensitivity.

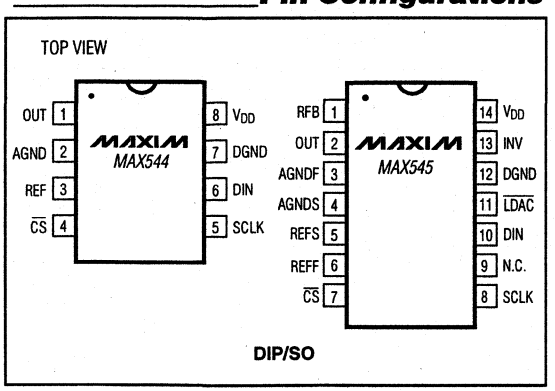
A 16-bit serial word is used to load data into the DAC latch. The 6.25MHz, 3-wire serial interface is compatible with SPI™/QSPI™/Microwire™, and it also interfaces directly with optocouplers for applications requiring isolation. A power-on reset circuit clears the DAC output to 0V (unipolar mode) when power is initially applied.

The MAX544 is available in 8-pin plastic DIP and SO packages. The MAX545 is available in 14-pin plastic DIP and SO packages.

Applications

Digital Offset and Gain Adjustment
Instrumentation
Industrial Process Control
Automated Test Equipment
Data-Acquisition Systems

Pin Configurations



Features

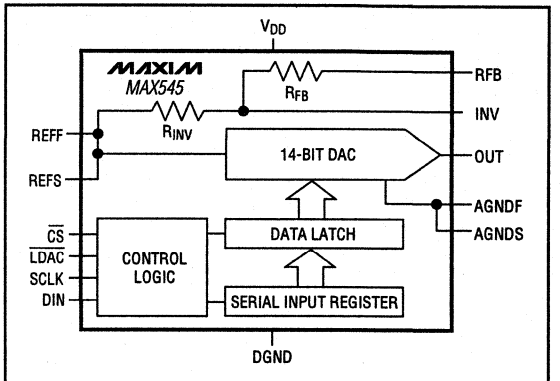
- ♦ **Full 14-Bit Performance Without Adjustments**
- ♦ **+5V Single-Supply Operation**
- ♦ **Low Power: 1.5mW**
- ♦ **1µs Settling Time**
- ♦ **Unbuffered Voltage Output Directly Drives 60kΩ Loads**
- ♦ **SPI/QSPI/Microwire-Compatible Serial Interface**
- ♦ **Power-On Reset Circuit Clears DAC Output to 0V (unipolar mode)**
- ♦ **Schmitt-Trigger Inputs for Direct Optocoupler Interface**
- ♦ **Pin-Compatible 16-Bit Upgrades: MAX541/MAX542**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX544ACPA	0°C to +70°C	8 Plastic DIP	±1/2
MAX544BCPA	0°C to +70°C	8 Plastic DIP	±1
MAX544ACSA	0°C to +70°C	8 SO	±1/2
MAX544BCSA	0°C to +70°C	8 SO	±1

Ordering Information continued at end of data sheet.

Functional Diagrams



Functional Diagrams continued at end of data sheet.

SPI and QSPI are trademarks of Motorola, Inc.
Microwire is a trademark of National Semiconductor Corp.

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+5V, Serial-Input, Voltage-Output, 14-Bit DACs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND .....-0.3V to +6V
$\overline{CS}$, SCLK, DIN, $\overline{LDAC}$ to DGND .....-0.3V to +6V
REF, REFF, REFS to AGND_ .....-0.3V to (V_{DD} + 0.3V)
AGND, AGNDF, AGNDS to DGND .....-0.3V to +0.3V
OUT, INV to AGND_, DGND .....-0.3V to V_{DD}
RFB to AGND_, DGND .....-6V to +6V
Maximum Current into Any Pin.....50mA
Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C).....727mW
8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C)...800mW
14-Pin SO (derate 8.33mW/°C above +70°C) 667mW
14-Pin Ceramic SB (derate 10.00mW/°C above +70°C...800mW
Operating Temperature Ranges
MAX544 _C_ A/MAX545_C_D .....0°C to +70°C
MAX544 _E_ A/MAX545_E_D.....-40°C to +85°C
MAX545BMJD .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ± 5%, $V_{REF_}$ = 2.5V, AGND_ = DGND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE—ANALOG SECTION (R_L = ∞)							
Resolution	N			14			Bits
Integral Nonlinearity	INL	V_{DD} = 5V	MAX54_A		±0.15	±0.5	LSB
			MAX54_B		±0.15	±1	
Differential Nonlinearity	DNL	Guaranteed monotonic			±0.15	±0.9	LSB
Zero-Code Offset Error	ZSE					±0.6	mV
Zero-Code Tempco	ZS_{TC}				±0.05		ppm/°C
Gain Error (Note 1)						±5	LSB
Gain-Error Tempco					±0.1		ppm/°C
DAC Output Resistance	R_{OUT}	(Note 2)			6.25		kΩ
Bipolar Resistor Matching		MAX545	R_{FB}/R_{INV}		1.0		
			Ratio error			±0.03	%
Bipolar Zero Offset Error		MAX545				±10	LSB
Bipolar Zero Tempco	BZS_{TC}	MAX545			±0.5		ppm/°C
Power-Supply Rejection	PSR	4.75V ≤ V_{DD} ≤ 5.25V				±1.0	LSB
REFERENCE INPUT							
Reference Input Range	V_{REF}	(Note 3)		2.0		3.0	V
Reference Input Resistance (Note 4)	R_{REF}	Unipolar mode		11.5			kΩ
		MAX545, bipolar mode		9.0			
DYNAMIC PERFORMANCE—ANALOG SECTION (R_L = ∞, unipolar mode)							
Voltage-Output Slew Rate	SR	C_L = 10pF (Note 5)			25		V/µs
Output Settling Time		to ±½LSB of FS, C_L = 10pF			1		µs
DAC Glitch Impulse		Major-carry transition			10		nV-s
Digital Feedthrough		Code = 0000hex; $\overline{CS}$ = V_{DD}; $\overline{LDAC}$ = 0V; SCLK, DIN = 0V to V_{DD} levels			10		nV-s

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ± 5%, $V_{REF_}$ = 2.5V, AGND_ = DGND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE—REFERENCE SECTION						
Reference -3dB Bandwidth	BW	Code = FFFC hex		1		MHz
Reference Feedthrough		Code = 0000 hex, V_{REF} = 1Vp-p at 100kHz		1		mVp-p
Signal-to-Noise Ratio	SNR			83		dB
Reference Input Capacitance	C_{IN}	Code = 0000 hex		75		pF
		Code = FFFC hex		120		
STATIC PERFORMANCE—DIGITAL INPUTS						
Input High Voltage	V_{IH}		2.4			V
Input Low Voltage	V_{IL}				0.8	V
Input Current	I_{IN}	V_{IN} = 0V			±1	µA
Input Capacitance	C_{IN}	(Note 6)			10	pF
Hysteresis Voltage	V_H			0.40		V
POWER SUPPLY						
Positive Supply Range	V_{DD}		4.75		5.25	V
Positive Supply Current	I_{DD}			0.3	1.1	mA
Power Dissipation	PD			1.5		mW

TIMING CHARACTERISTICS

(V_{DD} = +5V ± 5%, $V_{REF_}$ = 2.5V, AGND_ = DGND = 0V, CMOS inputs, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Frequency	f_{CLK}				6.25	MHz
SCLK Pulse Width High	t_{CH}		80			ns
SCLK Pulse Width Low	t_{CL}		80			ns
$\overline{CS}$ Low to SCLK High Setup	t_{CSS0}		50			ns
$\overline{CS}$ High to SCLK High Setup	t_{CSS1}		50			ns
SCLK High to $\overline{CS}$ Low Hold	t_{CSH0}	(Note 6)	30			ns
SCLK High to $\overline{CS}$ High Hold	t_{CSH1}		80			ns
DIN to SCLK High Setup	t_{DS}		40			ns
DIN to SCLK High Hold	t_{DH}		0			ns
$\overline{LDAC}$ Pulse Width	$t_{\overline{LDAC}}$	MAX545	50			ns
$\overline{CS}$ High to $\overline{LDAC}$ Low Setup	t_{LDACS}	MAX545 (Note 6)	50			ns
V_{DD} High to $\overline{CS}$ Low (power-up delay)				20		µs

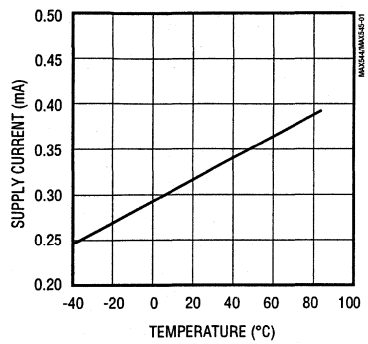
Note 1: Gain Error tested at V_{REF} = 2.0V, 2.5V, and 3.0V.
Note 2: R_{OUT} tolerance is typically ±20%.
Note 3: Min/max range guaranteed by gain-error test. Operation outside min/max limits will result in degraded performance.
Note 4: Reference input resistance is code dependent, minimum at 8554 hex.
Note 5: Slew-rate value is measured from 0% to 63%.
Note 6: Guaranteed by design. Not production tested.

+5V, Serial-Input, Voltage-Output, 14-Bit DACs

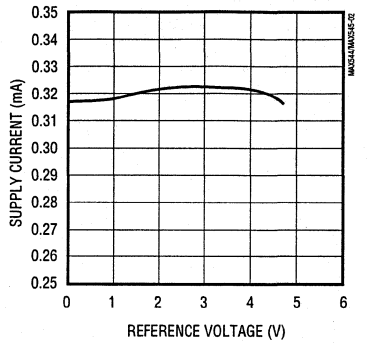
Typical Operating Characteristics

(V_{DD} = 5V, $V_{REF_}$ = 2.5V, T_A = +25°C, unless otherwise noted.)

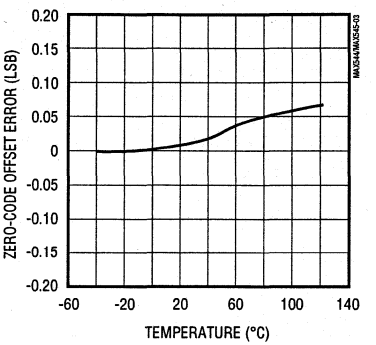
SUPPLY CURRENT vs. TEMPERATURE



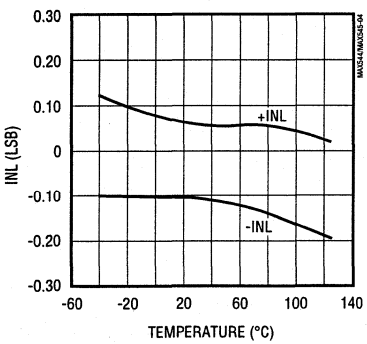
SUPPLY CURRENT vs. REFERENCE VOLTAGE



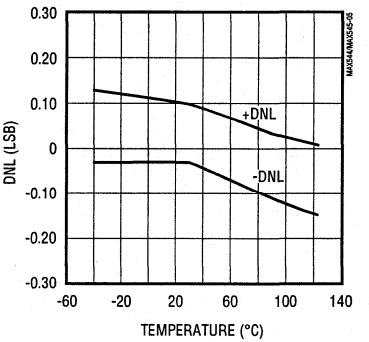
ZERO-CODE OFFSET ERROR vs. TEMPERATURE



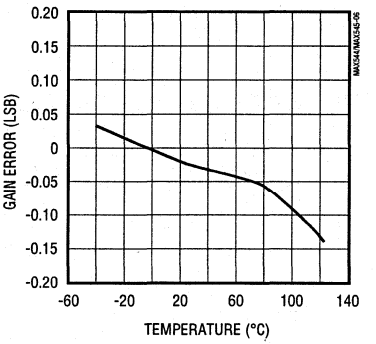
INTEGRAL NONLINEARITY vs. TEMPERATURE



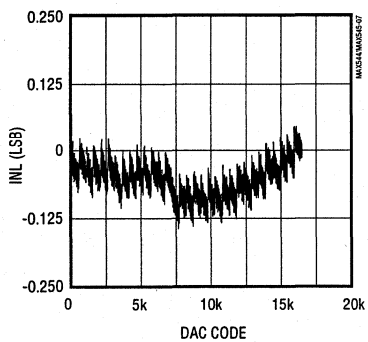
DIFFERENTIAL NONLINEARITY vs. TEMPERATURE



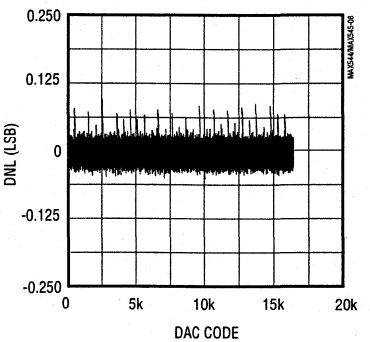
GAIN ERROR vs. TEMPERATURE



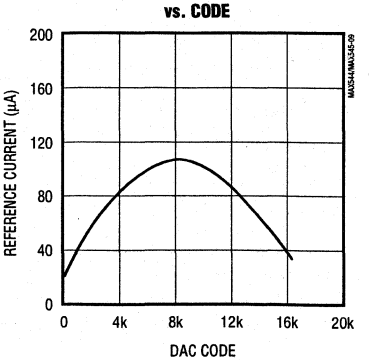
INTEGRAL NONLINEARITY vs. CODE



DIFFERENTIAL NONLINEARITY vs. CODE



REFERENCE CURRENT vs. CODE

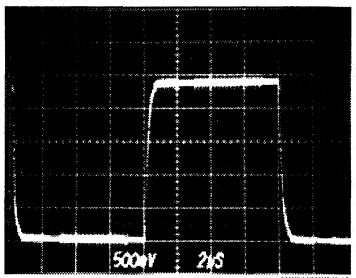


+5V, Serial-Input, Voltage-Output, 14-Bit DACs

Typical Operating Characteristics (continued)

(V_{DD} = 5V, $V_{REF_}$ = 2.5V, T_A = +25°C, unless otherwise noted.)

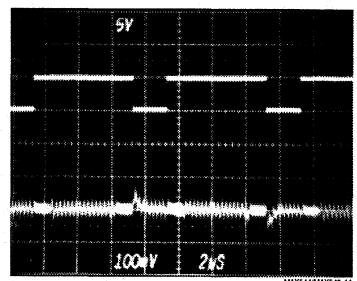
FULL-SCALE STEP RESPONSE



2µs/div

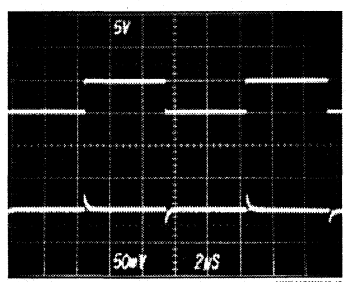
$R_L = \infty$, C_L = 10pF

MAJOR-CARRY OUTPUT GLITCH



2µs/div

DIGITAL FEEDTHROUGH



2µs/div

CODE = 0000 hex

Pin Descriptions

9

MAX544

PIN	NAME	FUNCTION
1	OUT	DAC Output Voltage
2	AGND	Analog Ground
3	REF	Voltage Reference Input. Connect to external +2.5V reference.
4	$\overline{CS}$	Chip-Select Input
5	SCLK	Serial-Clock Input. Duty cycle must be between 40% and 60%.
6	DIN	Serial-Data Input
7	DGND	Digital Ground
8	V_{DD}	+5V Supply Voltage

+5V, Serial-Input, Voltage-Output, 14-Bit DACs

Pin Descriptions (continued)

MAX545

PIN	NAME	FUNCTION
1	RFB	Feedback Resistor. Connect to external op amp's output in bipolar mode.
2	OUT	DAC Output Voltage
3	AGNDF	Analog Ground (force)
4	AGNDS	Analog Ground (sense)
5	REFS	Voltage Reference Input (sense). Connect REFS to external 2.5V reference.
6	REFF	Voltage Reference Input (force). Connect REFF to external 2.5V reference.
7	$\overline{CS}$	Chip-Select Input
8	SCLK	Serial-Clock Input. Duty cycle must be between 40% and 60%.
9	N.C.	No Connection. Not internally connected.
10	DIN	Serial-Data Input
11	$\overline{LDAC}$	$\overline{LDAC}$ Input. A falling edge updates the internal DAC latch.
12	DGND	Digital Ground
13	INV	Junction of internal scaling resistors. Connect to external op amp's inverting input in bipolar mode.
14	V_{DD}	+5V Supply Voltage

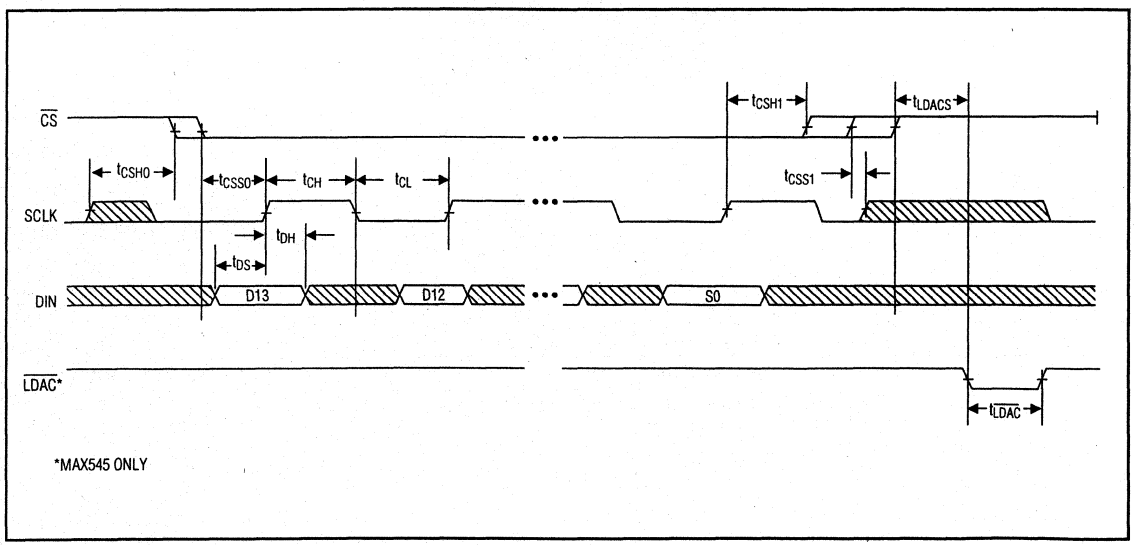


Figure 1. Timing Diagram

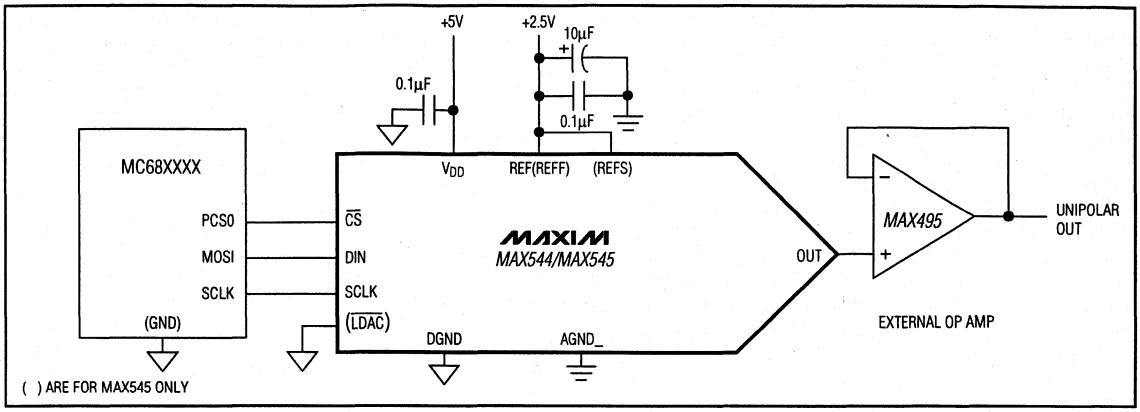


Figure 2a. Typical Operating Circuit—Unipolar Output

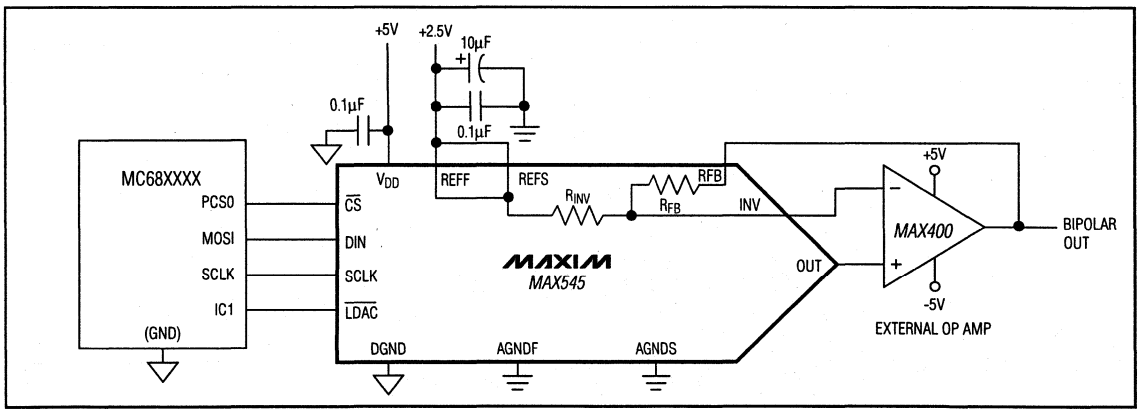


Figure 2b. Typical Operating Circuit—Bipolar Output

9

Detailed Description

The MAX544/MAX545 voltage-output, 14-bit digital-to-analog converters (DACs) offer full 14-bit performance with less than 0.5LSB integral linearity error and less than 0.9LSB differential linearity error, thus ensuring monotonic performance. Serial-data transfer minimizes the number of package pins required.

The MAX544/MAX545 are composed of two matched DAC sections, with an inverted R-2R DAC forming the LSBs and the 4MSBs derived from 15 identically matched resistors. This architecture allows the lowest glitch energy to be transferred to the DAC output on major-carry transitions. It also lowers the DAC output impedance by a factor of eight compared to a standard R-2R ladder, allowing unbuffered operation in medium-load applications.

The MAX545 provides matched bipolar offset resistors, which connect to an external op amp for bipolar output swings (Figure 2b). For optimum performance, the MAX545 also provides a set of Kelvin connections to the voltage-reference and analog-ground inputs.

+5V, Serial-Input, Voltage-Output, 14-Bit DACs

Digital Interface

The MAX544/MAX545's digital interface is a standard 3-wire connection compatible with SPI™/QSPI™/Microwire™ interfaces. The chip-select input ($\overline{CS}$) frames the serial data loading at the data-input pin (DIN). Immediately following $\overline{CS}$'s high-to-low transition, the data is shifted synchronously and latched into the input register on the rising edge of the serial clock input (SCLK). After 16 bits (14 data bits, plus two sub-bits set to zero) have been loaded into the serial input register, it transfers its contents to the DAC latch on $\overline{CS}$'s low-to-high transition (Figure 3a). Note that if $\overline{CS}$ is not kept low during the entire 16 SCLK cycles, data will be corrupted. In this case, reload the DAC latch with a new 16-bit word.

Alternatively, for the MAX545, $\overline{LDAC}$ allows the DAC latch to update asynchronously by pulling $\overline{LDAC}$ low after $\overline{CS}$ goes high (Figure 3b). Hold $\overline{LDAC}$ high during the data-loading sequence.

External Reference

The MAX544/MAX545 operate with external voltage references from 2V to 3V. The reference voltage determines the DAC's full-scale output voltage. Kelvin connections are provided with the MAX545 for optimum performance. The 2.5V MAX873A, with ±15mV initial accuracy and a 7ppm/°C (max) temperature coefficient, is a good choice.

Power-On Reset

The MAX544/MAX545 have a power-on reset circuit to set the DAC's output to 0V in unipolar mode when V_{DD} is first applied. This ensures that unwanted DAC output voltages will not occur immediately following a system power-up, such as after a loss of power. In bipolar mode, the DAC output is set to $-V_{REF}$.

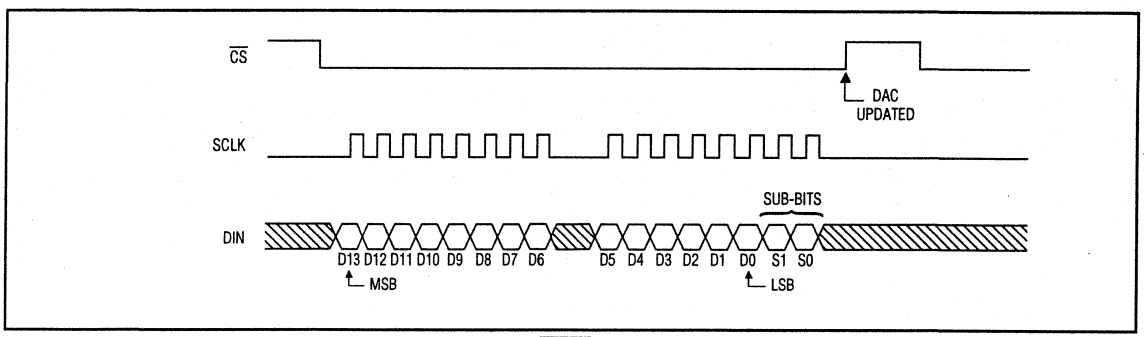


Figure 3a. MAX544/MAX545 3-Wire Interface Timing Diagram ($\overline{LDAC}$ = DGND for MAX545)

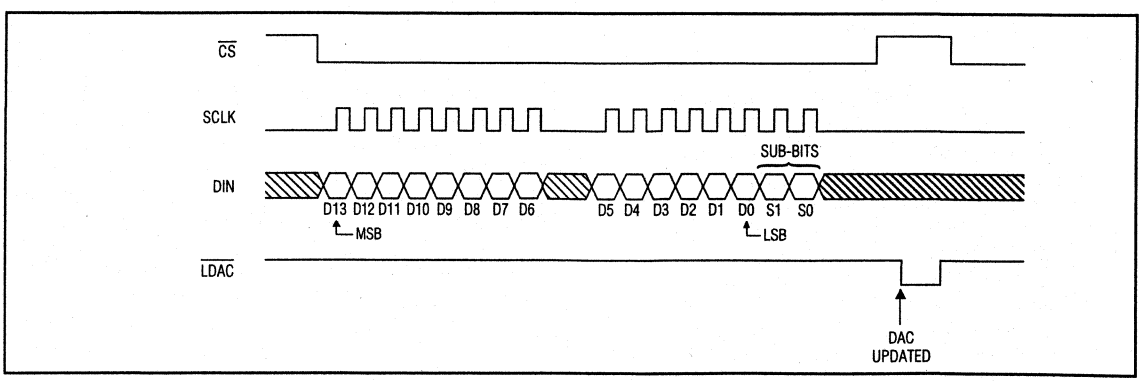


Figure 3b. MAX545 4-Wire Interface Timing Diagram

+5V, Serial-Input, Voltage-Output, 14-Bit DACs

Applications Information

Reference and Analog Ground Inputs

The MAX544/MAX545 operate with external voltage references from 2V to 3V, and maintain 14-bit performance if certain guidelines are followed when selecting and applying the reference. Ideally, the reference's temperature coefficient should be less than 1.5ppm/°C to maintain 14-bit accuracy to within 1LSB over the 0°C to +70°C commercial temperature range. Since this converter is designed as an inverted R-2R voltage-mode DAC, the input resistance seen by the voltage reference is code dependent. The worst-case input-resistance variation is from 11.5kΩ (at code 8554 hex) to 200kΩ (at code 0000 hex). The maximum change in load current for a 2.5V reference is 2.5V / 11.5kΩ = 217µA; therefore, the required load regulation is 28ppm/mA for a maximum error of 0.1LSB. This implies a reference output impedance of less than 71mΩ. In addition, the signal-path impedance from the voltage reference to the reference input must be kept low because it contributes directly to the load-regulation error.

The requirement for a low-impedance voltage reference is met with capacitor bypassing at the reference inputs and ground. A 0.1µF ceramic capacitor with short leads between REFF and AGNDF (MAX545), or REF and AGND (MAX544), provides high-frequency bypassing. A surface-mount ceramic chip capacitor is preferred because it has the lowest inductance. An additional 10µF between REFF and AGNDF (MAX545), or REF and AGND (MAX544), provides low-frequency bypassing. A low-ESR tantalum, film, or organic semiconductor capacitor works well. Leaded capacitors are acceptable because impedance is not as critical at lower frequencies. The circuit can benefit from even larger bypassing capacitors, depending on the stability of the external reference with capacitive loading. If separate force and sense lines are not used, tie the appropriate force and sense pins together close to the package.

AGND must also be low impedance, as load-regulation errors will be introduced by excessive AGND resistance. As in all high-resolution, high-accuracy applications, separate analog and digital ground planes yield the best results. Tie DGND to AGND at the AGND pin to form the "star" ground for the DAC system. Always refer remote DAC loads to this system ground for the best possible performance.

Unbuffered Operation

Unbuffered operation reduces power consumption as well as offset error contributed by the external output buffer. The R-2R DAC output is available directly at OUT, allowing 14-bit performance from $+V_{REF}$ to AGND without degradation at zero-scale. The DAC's output impedance is also low enough to drive medium loads (R_L > 60kΩ) without degradation of INL or DNL; only the gain error is increased by externally loading the DAC output.

External Output Buffer Amplifier

The requirements on the external output buffer amplifier change whether the DAC is used in unipolar or bipolar operational mode. In unipolar mode, the output amplifier is used in a voltage-follower connection. In bipolar mode (MAX545 only), the amplifier operates with the internal scaling resistors (Figure 2b). In each mode, the DAC's output resistance is constant and is independent of input code; however, the output amplifier's input impedance should still be as high as possible to minimize gain errors. The DAC's output capacitance is also independent of input code, thus simplifying stability requirements on the external amplifier.

In bipolar mode, a precision amplifier operating with dual power supplies (such as the MAX400) provides the $\pm V_{REF}$ output range. In single-supply applications, precision amplifiers with input common-mode ranges including AGND are available; however, their output swings do not normally include the negative rail (AGND) without significant degradation of performance. A single-supply op amp, such as the MAX495, is suitable if the application does not use codes near zero.

Since the LSBs for a 14-bit DAC are extremely small (152.6µV for V_{REF} = 2.5V), pay close attention to the external amplifier's input specification. The input offset voltage can degrade the zero-scale error and might require an output offset trim to maintain full accuracy if the offset voltage is greater than 1/2LSB. Similarly, the input bias current multiplied by the DAC output resistance (typically 6.25kΩ) contributes to zero-scale error. Temperature effects also must be taken into consideration. Over the 0°C to +70°C commercial temperature range, the offset voltage temperature coefficient (referenced to +25°C) must be less than 1.7µV/°C to add less than 1/2LSB of zero-scale error. The external

amplifier's input resistance forms a resistive divider with the DAC output resistance, which results in a gain error. To contribute less than 1/2LSB of gain error, the input resistance typically must be greater than:

$$6.25k\Omega \div \frac{1}{2}\left[\frac{1}{2^{14}}\right] = 205M\Omega.$$

The settling time is affected by the buffer input capacitance, the DAC's output capacitance, and PC board capacitance. The typical DAC output voltage settling time is 1µs for a full-scale step. Settling time can be significantly less for smaller step changes. Assuming a single time-constant exponential settling response, a full-scale step takes 10.4 time constants to settle to within 1/2LSB of the final output voltage. The time constant is equal to the DAC output resistance multiplied by the total output capacitance. The DAC output capacitance is typically 10pF. Any additional output capacitance increases the settling time.

The external buffer amplifier's gain-bandwidth product is important because it increases the settling time by adding another time constant to the output response. The effective time constant of two cascaded systems, each with a single time-constant response, is approximately the root square sum of the two time constants. The DAC output's time constant is 1µs / 10.4 = 96ns, ignoring the effect of additional capacitance. If the time constant of an external amplifier with 1MHz bandwidth is 1 / 2π (1MHz) = 159ns, then the effective time constant of the combined system is:

$$\sqrt{\left[(96ns)^2 + (159ns)^2\right]} = 186ns$$

This suggests that the settling time to within 1/2LSB of the final output voltage, including the external buffer amplifier, will be approximately 10.4 x 186ns = 1.93µs.

Digital Inputs and Interface Logic

The digital interface for the 14-bit DAC is based on a 3-wire standard that is compatible with SPI, QSPI, and Microwire interfaces. The three digital inputs ($\overline{CS}$, DIN, and SCLK) load the digital input data serially into the DAC. $\overline{LDAC}$ (MAX545) updates the DAC output asynchronously.

All of the digital inputs include Schmitt-trigger buffers to accept slow-transition interfaces. This means that optocouplers can interface directly to the MAX544/MAX545 without additional external logic. The digital inputs are compatible with TTL/CMOS-logic levels.

Unipolar Configuration

Figure 2a shows the MAX544/MAX545 configured for unipolar operation with an external op amp. The op amp is set for unity gain, and Table 1 shows the codes for this circuit.

Bipolar Configuration

Figure 2b shows the MAX545 configured for bipolar operation with an external op amp. The op amp is set for unity gain with an offset of $-1/2V_{REF}$. Table 2 shows the offset binary codes for this circuit.

Power-Supply Bypassing and Ground Management

For optimum system performance, use printed circuit boards with separate analog and digital ground planes. Wire-wrap boards are not recommended. Connect the two ground planes together at the low-impedance power-supply source. Connect DGND and AGND together at the IC. The best ground connection can be achieved by connecting the DAC's DGND and AGND pins together and connecting that point to the system analog ground plane. If the DAC's DGND is connected to the system digital ground, digital noise may get through to the DAC's analog portion.

Bypass V_{DD} with a 0.1µF ceramic capacitor connected between V_{DD} and AGND. Mount it with short leads close to the device. Ferrite beads can also be used to further isolate the analog and digital power supplies.

Table 1. Unipolar Code Table

DAC LATCH CONTENTS MSB LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111 11(00)	V_{REF} x (16,383 / 16,384)
1000 0000 0000 00(00)	V_{REF} x (8192 / 16,384) = $1/2V_{REF}$
0000 0000 0000 01(00)	V_{REF} x (1 / 16,384)
0000 0000 0000 00(00)	0V

Table 2. Bipolar Code Table

DAC LATCH CONTENTS MSB LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111 11(00)	+V_{REF} x (8191 / 8192)
1000 0000 0000 01(00)	+V_{REF} x (1 / 8192)
1000 0000 0000 00(00)	0V
0111 1111 1111 11(00)	-V_{REF} x (1 / 8192)
0000 0000 0000 00(00)	-V_{REF} x (8192 / 8192) = -V_{REF}

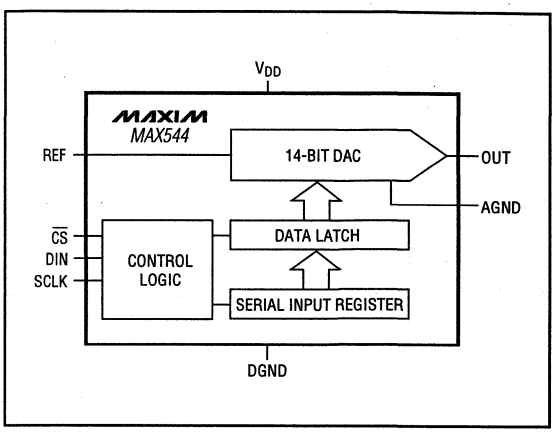
( ) = Sub-bits

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX544AEPA	-40°C to +85°C	8 Plastic DIP	±1/2
MAX544BEPA	-40°C to +85°C	8 Plastic DIP	±1
MAX544AESA	-40°C to +85°C	8 SO	±1/2
MAX544BESA	-40°C to +85°C	8 SO	±1
MAX545ACPD	0°C to +70°C	14 Plastic DIP	±1/2
MAX545BCPD	0°C to +70°C	14 Plastic DIP	±1
MAX545ACSD	0°C to +70°C	14 SO	±1/2
MAX545BCSD	0°C to +70°C	14 SO	±1
MAX545AEPD	-40°C to +85°C	14 Plastic DIP	±1/2
MAX545BEPD	-40°C to +85°C	14 Plastic DIP	±1
MAX545AESD	-40°C to +85°C	14 SO	±1/2
MAX545BESD	-40°C to +85°C	14 SO	±1
MAX545BMJD	-55°C to +125°C	14 Ceramic SB*	±1

*Contact factory for availability.

Functional Diagrams (continued)



Chip Information

TRANSISTOR COUNT: 2209

19-1099; Rev 1; 9/96

MAXIM

Low-Power, +2.5V to +5.5V, Dual 8-Bit Voltage-Output DAC in µMAX

General Description

The MAX549 dual, serial 8-bit, voltage-output, digital-to-analog converter (DAC) operates on a single +2.5V to +5.5V supply. Its ±1LSB TUE specification is guaranteed over temperature. Operating current (supply current plus reference current) is typically 150µA with V_{DD} = 2.5V and less than 1µA in shutdown mode.

The interface operates at clock rates up to 10MHz and is compatible with 3-wire SPI™, QSPI™, and Microwire™ interface standards. The serial input shift register is 16 bits: 8 bits for DAC selection and shutdown control, and 8 bits of DAC input data.

The MAX549's ultra-low power consumption and small µMAX package make it ideal for portable and battery-powered applications.

Applications

VCXO Control

Comparator Level Settings

GaAs Amp Bias Control

Digital Gain and Offset Control

Features

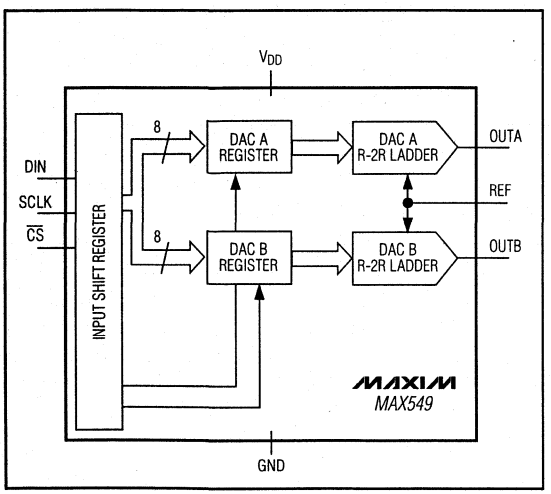
- **+2.5V to +5.5V Single-Supply Operation**
- **±1LSB (max) TUE**
- **Low 150µA Operating Current (V_{DD} = +2.5V)**
- **1µA Shutdown Mode**
- **µMAX Package—50% Smaller than 8-Pin SO**
- **10MHz, 3-Wire Serial Interface**
- **Internal Power-On Reset Clears All Registers to Zero**

Ordering Information

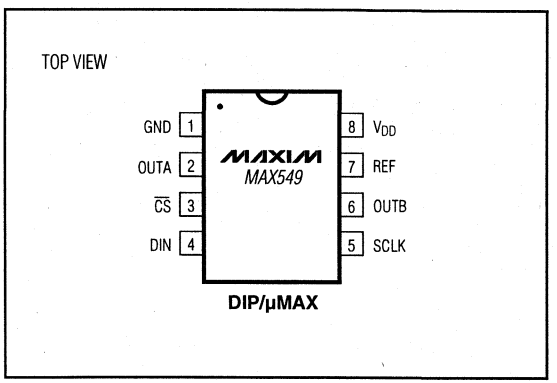
PART	TEMP. RANGE	PIN-PACKAGE
MAX549BCPA	0°C to +70°C	8 Plastic DIP
MAX549BCUA	0°C to +70°C	8 µMAX
MAX549BC/D	0°C to +70°C	Dice*
MAX549BEPA	-40°C to +85°C	8 Plastic DIP
MAX549BEUA	-40°C to +85°C	8 µMAX

Dice are specified at T_A = +25°C, DC parameters only.

Functional Diagram



Pin Configuration



DIP/µMAX

SPI and QSPI are registered trademarks of Motorola, Inc.
Microwire is a registered trademark of National Semiconductor Corp.

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Low-Power, +2.5V to +5.5V, Dual 8-Bit Voltage-Output DAC in µMAX

ABSOLUTE MAXIMUM RATINGS

V_{DD}, SCLK, D_{IN}, $\overline{CS}$, OUTA, OUTB to GND .....-0.3V to +6V
REF .....-0.3V to (V_{DD} + 0.3V)
Maximum Current (any pin) 50mA
Continuous Power Dissipation
Plastic DIP (derate 9.1mW/°C above +70°C) 727mW
µMAX (derate 4.1mW/°C above +70°C) 330mW

Operating Temperature Ranges
MAX549BC_A .....0°C to +70°C
MAX549BE_A .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.5V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution	N			8			Bits
Differential Nonlinearity	DNL	Guaranteed monotonic	MAX549BC_A/MAX549BEPA			±0.9	LSB
			MAX549BEUA (Note 1)			±0.9	
Total Unadjusted Error	TUE		MAX549BC_A/MAX549BEPA			±1	LSB
			MAX549BEUA (Note 1)			±1	
Zero-Code Error	ZCE	T_A = +25°C				±1	LSB
Full-Scale Error	FSE					±1	LSB
REFERENCE INPUT							
Reference Input Voltage	V_{REF}	For specified performance		2.5		V_{DD}	V
Reference Input Resistance (Note 2)	R_{REF}	DAC code = 55 hex			16		kΩ
Reference Input Current (Note 3)	I_{REF}	DAC code = 55 hex	V_{DD} = V_{REF} = 5.5V		325	550	µA
			V_{DD} = V_{REF} = 2.5V		150	250	
DAC OUTPUTS (OUTA, OUTB)							
DAC Output Voltage Swing				0		REF	V
DAC Output Resistance	R_{OUT}				32		kΩ
DAC Output Resistance Match	$\Delta(R_{OUTA} - R_{OUTB})$				±0.2		%
DIGITAL INPUTS ($\overline{CS}$, SCLK, DIN)							
Input High Voltage	V_{IH}			0.7V_{DD}			V
Input Low Voltage	V_{IL}					0.3V_{DD}	V
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}				±1	µA
Input Capacitance (Note 4)	C_{IN}					10	pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.5V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE							
Digital Feedthrough and Crosstalk		$\overline{CS}$ = high, all digital inputs from 0V to V_{DD}			50		nV-sec
Voltage-Output Settling Time		To ±1/2LSB, C_L = 20pF			4		µs
Voltage-Output Slew Rate	SR	C_L = 20pF	V_{DD} = +2.5V		1.4		V/µs
			V_{DD} = +5.5V		3.1		
Wake-Up Time		C_{LOAD} = 20pF			4		µs
POWER SUPPLIES							
Supply Voltage Range	V_{DD}	Outputs unloaded, all inputs = GND or V_{DD}		2.5		5.5	V
Supply Current	I_{DD}	V_{DD} = +5.5V, outputs unloaded, all inputs = GND or V_{DD}			0.3	10	µA
Shutdown Current		Shutdown mode			0.3		µA

Note 1: 0°C to -40°C testing guaranteed by design using six sigma design limits.
Note 2: Worst-case input resistance at REF occurs at DAC code 55 hex.
Note 3: Worst-case reference input current occurs at DAC code 55 hex.
Note 4: Guaranteed by design. Not production tested.

TIMING CHARACTERISTICS (Note 5)

(V_{DD} = +2.5V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Digital inputs switching from 0V to V_{DD}.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Pulse Width High	t_{CH}		40			ns
SCLK Pulse Width Low	t_{CL}		40			ns
DIN to SCLK High Setup	t_{DS}		30			ns
DIN to SCLK High Hold	t_{DH}	V_{DD} = +2.5V	0			ns
		V_{DD} = +5.5V	10			
$\overline{CS}$ Low to SCLK High Setup	t_{CSS0}		30			ns
$\overline{CS}$ High to SCLK High Setup	t_{CSS1}		30			ns
SCLK High to $\overline{CS}$ Low Hold	t_{CSH0}	V_{DD} = 2.5V	10			ns
		V_{DD} = 5.5V	20			
Delay, SCLK High to $\overline{CS}$ High	t_{CSH1}		10			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		40			ns
SCLK Period	t_{CP}		80			ns
V_{DD} High to $\overline{CS}$ Low		Power-on reset delay			5	µs

Note 5: Guaranteed by design. Not production tested.

Low-Power, +2.5V to +5.5V, Dual 8-Bit Voltage-Output DAC in µMAX

Pin Description

PIN	NAME	FUNCTION
1	GND	Ground
2	OUTA	DAC A Output Voltage
3	$\overline{CS}$	Chip-Select Input. A logic low on $\overline{CS}$ enables serial data to be clocked into the input shift register. Programming commands are executed at $\overline{CS}$'s rising edge.
4	DIN	Serial Data Input. Data is clocked into the 16-bit input shift register on SCLK's rising edge.
5	SCLK	Serial Clock Input. Data is clocked in on SCLK's rising edge.
6	OUTB	DAC B Output Voltage
7	REF	External Reference Voltage Input for DAC A and DAC B (2.5V to V_{DD})
8	V_{DD}	Positive Power Supply (+2.5V to +5.5V)

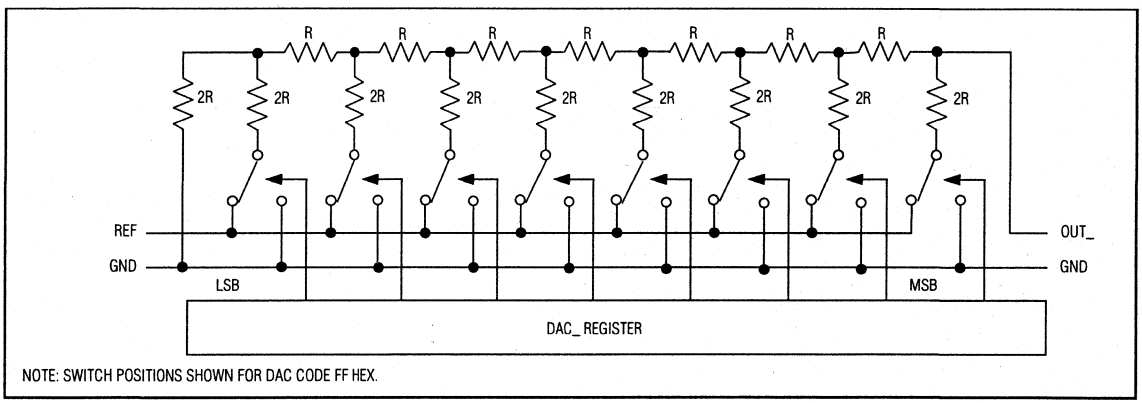


Figure 1. DAC Simplified Circuit Diagram

Detailed Description

Analog Section

The MAX549 is a dual, 8-bit, voltage-output digital-to-analog converter (DAC). Each DAC consists of an R-2R ladder network that converts 8-bit digital inputs into equivalent analog output voltages in proportion to the applied reference voltage (Figure 1). The MAX549's outputs are unbuffered and have a typical output resistance of 32kΩ. The external reference is used by both DACs. The power-supply range is from +2.5V to +5.5V.

Reference Input

The voltage applied at REF sets the full-scale output for both DACs and may range from 2.5V to V_{DD}. The REF input resistance is code dependent, with the lowest value (typically 16kΩ) occurring when both DAC registers are loaded with a code of 01010101 (55 hex). To minimize INL errors, the reference voltage source should have less than 3Ω output impedance.

Low-Power, +2.5V to +5.5V, Dual 8-Bit Voltage-Output DAC in µMAX

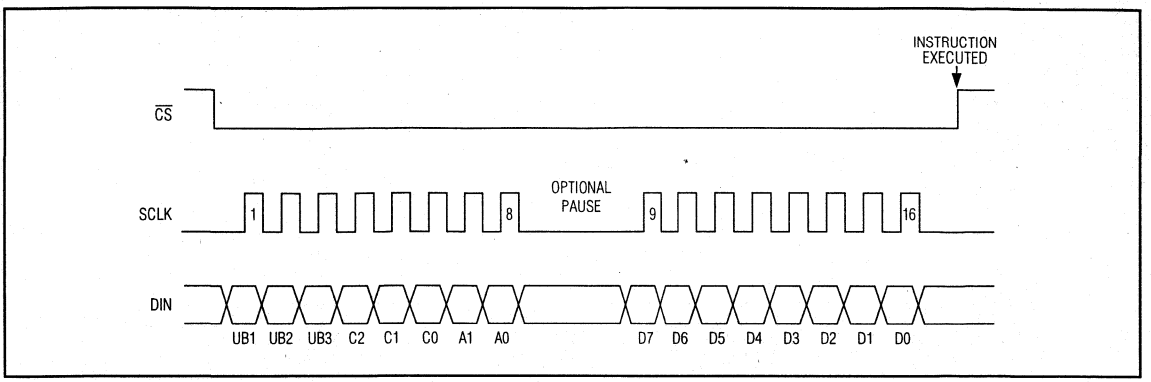


Figure 2. MAX549 Serial-Interface Timing Diagram

DAC Outputs

The MAX549's outputs are unbuffered; each output connects directly to an R-2R ladder. This configuration minimizes power consumption and reduces offset errors. For highest accuracy, apply high resistive loads (1MΩ and up). Lower resistive loads can be driven, but output loading increases full-scale error. The magnitude of the expected error is the ratio of the DAC output resistance to the DC load resistance at the output.

Typically, an energy pulse is coupled into the DAC output on the rising edge of $\overline{CS}$. Since the MAX549's outputs are unbuffered (connected directly to the R-2R ladder), connecting a small capacitor (200pF to 1000pF) from the output to ground creates a lowpass filter that effectively suppresses the pulse for sensitive applications.

Shutdown Mode

When the MAX549 is in shutdown mode, REF becomes high-impedance. The supply current is unchanged, but REF input current decreases to less than 1µA. This allows the system reference to remain active with minimal power consumption.

When exiting shutdown mode, recovery time is equivalent to the DAC settling time.

Serial Interface

The MAX549 interface is compatible with 3-wire SPI™, QSPI™, and Microwire™ microprocessor (µP) interface standards. An active-low chip select ($\overline{CS}$) enables the input shift register to receive data from the serial input (DIN). Data is clocked into the input shift register on rising edges of the serial clock signal (SCLK). The clock frequency can be as high as 10MHz.

Transmit data MSB first in one 16-bit word or two 8-bit bytes. The write cycle can be segmented when $\overline{CS}$ is kept active (low) to allow two 8-bit-wide transfers. After clocking all 16 bits into the input shift register, a rising edge on $\overline{CS}$ programs the DAC. The DAC outputs can be changed independently or simultaneously. The DAC outputs reflect the data stored in the DAC registers.

Initialization

The MAX549 has an internal power-on reset. At power-up, all internal registers are reset to zero; therefore, an initialization write is not necessary.

Serial Input Data Format and Control Codes

The control byte determines which DAC register is updated (Table 1). Table 2 lists the MAX549's serial-input command format. The 16-bit input word consists of an 8-bit control byte and an 8-bit data byte. The 8-bit control byte is not decoded internally; every control bit performs one function. Data is clocked in starting with uncommitted bit 1 (UB1), followed by the remaining control bits and the DAC data byte. The LSB (D0) of the data byte is the last bit clocked into the input shift register (Figure 2).

Table 3 is an example of a 16-bit word. It performs the following functions:

1) Load 80 hex (128 decimal) into both DAC registers
2) Update both DAC outputs on $\overline{CS}$'s rising edge

Table 4 shows how to calculate the output voltage based on the input code. Figure 3 gives detailed timing information.

Low-Power, +2.5V to +5.5V, Dual 8-Bit Voltage-Output DAC in µMAX

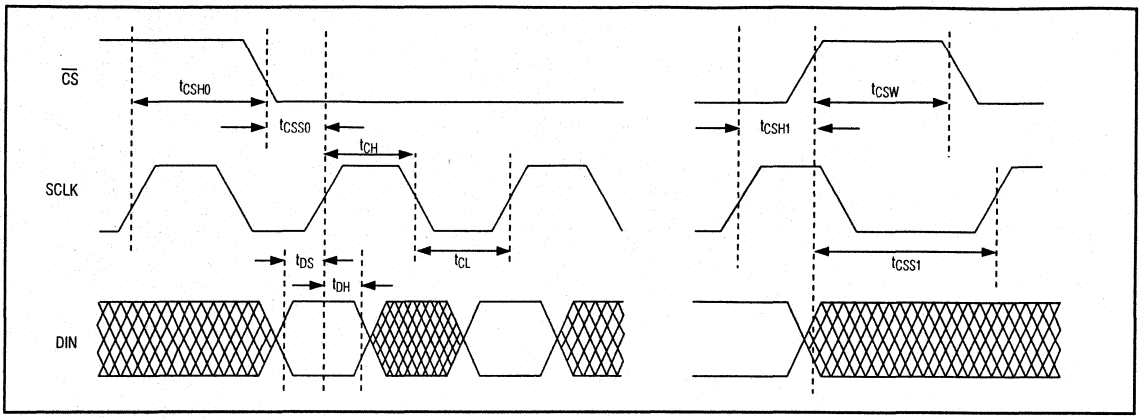


Figure 3. Detailed Serial-Interface Timing Diagram

Table 1. Control Byte/Input Word Bit Definitions

Control Byte	UB1*	X	Unassigned Bit 1
	UB2	X	Unassigned Bit 2
	UB3	X	Unassigned Bit 3
	C2	0	Power-Up Mode
	C2	1	Power-Down Mode
	C1	0	DAC Register Load Operation Disabled
	C1	1	DAC Register Load Operation Enabled
	C0	0	DAC Output Updated on Rising Edge of $\overline{CS}$
	C0	1	Unassigned Operation
	A1	0	Do Not Address DAC B
	A1	1	Address DAC B
	A0	0	Do Not Address DAC A
	A0	1	Address DAC A
Data Byte	D7	X	DAC Data Bit 7 (MSB)
	D6	X	DAC Data Bit 6
	D5	X	DAC Data Bit 5
	D4	X	DAC Data Bit 4
	D3	X	DAC Data Bit 3
	D2	X	DAC Data Bit 2
	D1	X	DAC Data Bit 1
	D0**	X	DAC Data Bit 0 (LSB)

**Clocked in first*
***Clocked in last*

Microprocessor Interfacing

The MAX549 serial interface is compatible with Microwire, SPI, and QSPI interface standards. For SPI, clear the CPOL and CPHA bits (CPOL = 0 and CPHA = 0). CPOL = 0 sets the idle clock state to zero and CPHA = 0 changes data at SCLK's falling edge. This setting allows SPI to run at full clock speeds (1.5MHz). If a serial port is not available on your µP, three bits of a parallel port can be used to emulate a serial port by bit manipulation. Minimize digital feedthrough at the DAC outputs by operating the serial clock only when necessary.

Applications Information

Power-Supply and Ground Considerations

Connect GND to the highest-quality ground available. Bypass V_{DD} with a 0.1µF to 0.22µF capacitor to GND. The reference input can be used without bypassing. However, for optimum line/load-transient response and noise performance, bypass the reference input with 0.1µF to 4.7µF to GND.

Careful PC board layout minimizes crosstalk among the DAC outputs, the reference, and the digital inputs. Separate analog traces by running ground traces between them. Make sure high-frequency digital lines are not routed parallel to analog lines.

Table 2. Serial Interface Programming Commands

CONTROL BYTE								DATA BYTE								COMMAND
Loaded First								Loaded Last								
UB1	UB2	UB3	C2	C1	C0	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Initial condition of all registers after power-up.
X	X	X	0	0	0	X	X	X	X	X	X	X	X	X	X	On $\overline{CS}$'s rising edge, wake up both DACs. DAC registers unchanged.
X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	Unassigned command
X	X	X	0	1	0	0	1	8-bit DAC data								On $\overline{CS}$'s rising edge, load DAC A register. DAC B register unchanged.
X	X	X	0	1	0	1	0	8-bit DAC data								On $\overline{CS}$'s rising edge, load DAC B register. DAC A register unchanged.
X	X	X	0	1	0	1	1	8-bit DAC data								On $\overline{CS}$'s rising edge, load and update both DAC registers.
X	X	X	1	0	0	1	1	X	X	X	X	X	X	X	X	On $\overline{CS}$'s rising edge, power down both DACs. Both DAC outputs go to zero. DAC registers unchanged.
X	X	X	1	1	0	1	1	8-bit DAC data								On $\overline{CS}$'s rising edge, power down both DACs and update both DAC registers. Both DAC outputs go to zero.

X = Don't Care

Table 3. Example Input Word

Loaded First															Loaded Last
UB1	UB2	UB3	C2	C1	C0	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	0	1	0	1	1	1	0	0	0	0	0	0	0

X = Don't Care

Table 4. Analog Output vs. Code

DAC CONTENTS								ANALOG OUTPUT (V)
D7	D6	D5	D4	D3	D2	D1	D0	
1	1	1	1	1	1	1	1	$+V_{REF}$ x (255/256)
1	0	0	0	0	0	0	1	$+V_{REF}$ x (129/256)
1	0	0	0	0	0	0	0	$+V_{REF}$ x (128/256) = $+V_{REF}/2$
0	1	1	1	1	1	1	1	$+V_{REF}$ x (127/256)
0	0	0	0	0	0	0	1	$+V_{REF}$ x (1/256)
0	0	0	0	0	0	0	0	0

Note: 1LSB = $V_{REF} \times 2^{-8} = V_{REF}(1/256)$
ANALOG OUTPUT = $+V_{REF}(I/256)$, where I = Integer Value of Digital Input

Low-Power, +2.5V to +5.5V, Dual 8-Bit Voltage-Output DAC in µMAX

AC Considerations

Digital Feedthrough

High-speed data at any of the digital input pins may couple through the DAC's internal stray package capacitance and cause noise (digital feedthrough) at the DAC's output, even though $\overline{CS}$ is held high. This digital feedthrough is tested by holding $\overline{CS}$ high and toggling the digital inputs from all 1s to all 0s.

Analog Feedthrough

Due to internal stray capacitance, higher-frequency analog input signals at REF may couple to the output, even when the input digital code is all 0s. Test analog feedthrough by setting all DAC outputs to 0V and sweeping REF.

Chip Information

TRANSISTOR COUNT: 1562

19-1140; Rev 0; 9/96

MAXIM

Low-Power, +2.5V to +5.5V, 8-Bit Voltage-Output DAC in µMAX

General Description

The MAX550B serial, 8-bit, voltage-output, digital-to-analog converter (DAC) operates on a single +2.5V to +5.5V supply. Its ±1LSB TUE specification is guaranteed over temperature. Operating current (supply current plus reference current) is typically 75µA with V_{DD} = 2.5V and less than 1µA in shutdown mode. The reference input is disconnected from the REF pin during shutdown.

The serial interface operates at clock rates up to 10MHz and is compatible with 3-wire SPI™, QSPI™, and Microwire™ interface standards.

The MAX550B's ultra-low power consumption and small µMAX package make it ideal for portable and battery-powered applications.

Applications

VCXO Control

Comparator Level Settings

GaAs Amp Bias Control

Digital Gain and Offset Control

Features

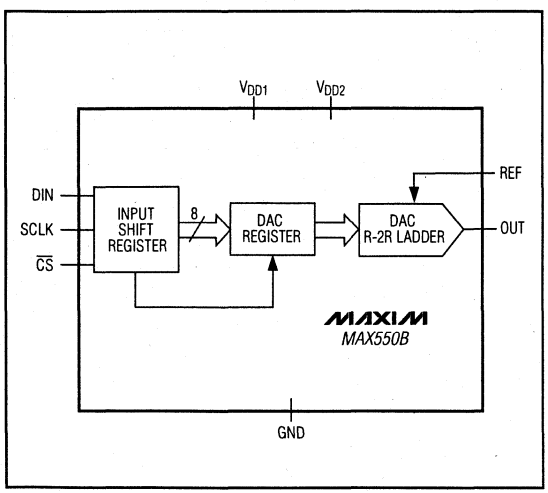
- **+2.5V to +5.5V Single-Supply Operation**
- **±1LSB (max) TUE**
- **Low 75µA Operating Current (V_{DD} = +2.5V)**
- **1µA Shutdown Mode**
- **µMAX Package—50% Smaller than 8-Pin SO**
- **10MHz, 3-Wire Serial Interface**
- **Internal Power-On Reset Clears All Registers to Zero**

Ordering Information

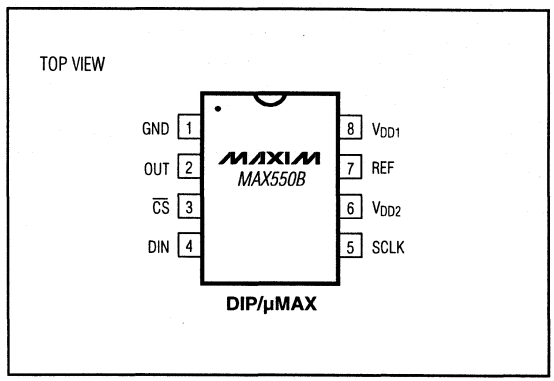
PART	TEMP. RANGE	PIN-PACKAGE
MAX550BCPA	0°C to +70°C	8 Plastic DIP
MAX550BCUA	0°C to +70°C	8 µMAX
MAX550BC/D	0°C to +70°C	Dice*
MAX550BEPA	-40°C to +85°C	8 Plastic DIP
MAX550BEUA	-40°C to +85°C	8 µMAX

Dice are specified at T_A = +25°C, DC parameters only.

Functional Diagram



Pin Configuration



SPI and QSPI are registered trademarks of Motorola, Inc.
Microwire is a registered trademark of National Semiconductor Corp.

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Low-Power, +2.5V to +5.5V, 8-Bit Voltage-Output DAC in µMAX

ABSOLUTE MAXIMUM RATINGS

V_{DD1}, V_{DD2}, SCLK, D_{IN}, $\overline{CS}$, OUT to GND .....-0.3V to +6V
REF .....-0.3V to ($V_{DD_}$ + 0.3V)
Maximum Current (any pin) 50mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.1mW/°C above +70°C) 727mW
µMAX (derate 4.1mW/°C above +70°C) 330mW

Operating Temperature Ranges
MAX550BBC_A .....0°C to +70°C
MAX550BBE_A .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD1} = V_{DD2} = +2.5V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution	N			8			Bits
Differential Nonlinearity	DNL	Guaranteed monotonic	MAX550BBC_A/MAX550BBE			±0.9	LSB
			MAX550BBEUA (Note 1)			±0.9	
Total Unadjusted Error	TUE		MAX550BBC_A/MAX550BBE			±1	LSB
			MAX550BBEUA (Note 1)			±1	
Zero-Code Error	ZCE	T_A = +25°C				±1	LSB
Full-Scale Error	FSE					±1	LSB
REFERENCE INPUT							
Reference Input Voltage	V_{REF}	For specified performance		2.5		V_{DD}	V
Reference Input Resistance (Note 2)	R_{REF}	DAC code = 55 hex			32		kΩ
Reference Input Current (Note 3)	I_{REF}	DAC code = 55 hex	$V_{DD_}$ = V_{REF} = 5.5V		160	275	µA
			$V_{DD_}$ = V_{REF} = 2.5V		75	125	
DAC OUTPUT (OUT)							
DAC Output Voltage Swing				0		V_{REF}	V
DAC Output Resistance	R_{OUT}				32		kΩ
DIGITAL INPUTS ($\overline{CS}$, SCLK, DIN)							
Input High Voltage	V_{IH}			0.7$V_{DD_}$			V
Input Low Voltage	V_{IL}					0.3$V_{DD_}$	V
Input Current	I_{IN}	V_{IN} = 0V or $V_{DD_}$				±1	µA
Input Capacitance (Note 4)	C_{IN}					10	pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD1} = V_{DD2} = +2.5V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE							
Digital Feedthrough and Crosstalk		$\overline{CS}$ = high, all digital inputs from 0V to $V_{DD_}$			50		nV-sec
Voltage-Output Settling Time		To ±1/2LSB, C_L = 20pF			4		µs
Voltage-Output Slew Rate	SR	C_L = 20pF	$V_{DD_}$ = 2.5V		1.4		V/µs
			$V_{DD_}$ = 5.5V		3.1		
Wake-Up Time		C_{LOAD} = 20pF			4		µs
POWER SUPPLIES							
Supply Voltage Range	$V_{DD_}$	Output unloaded, all inputs = GND or V_{DD}		2.5		5.5	V
Supply Current	I_{DD1} + I_{DD2}	$V_{DD_}$ = 5.5V, output unloaded, all inputs = GND or $V_{DD_}$			0.3	10	µA
Shutdown Current		Shutdown mode			0.3		µA

Note 1: 0°C to -40°C testing guaranteed by design using six sigma design limits.
Note 2: Worst-case input resistance at REF occurs at DAC code 55 hex.
Note 3: Worst-case reference input current occurs at DAC code 55 hex.
Note 4: Guaranteed by design. Not production tested.

TIMING CHARACTERISTICS (Note 5)

(V_{DD1} = V_{DD2} = +2.5V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Digital inputs switching from 0V to $V_{DD_}$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Pulse Width High	t_{CH}		40			ns
SCLK Pulse Width Low	t_{CL}		40			ns
DIN to SCLK High Setup	t_{DS}		30			ns
DIN to SCLK High Hold	t_{DH}	$V_{DD_}$ = 2.5V	0			ns
		$V_{DD_}$ = 5.5V	10			
$\overline{CS}$ Low to SCLK High Setup	t_{CSS0}		30			ns
$\overline{CS}$ High to SCLK High Setup	t_{CSS1}		30			ns
SCLK High to $\overline{CS}$ Low Hold	t_{CSH0}		20			ns
Delay, SCLK High to $\overline{CS}$ High	t_{CSH1}	$V_{DD_}$ = 2.5V	10			ns
		$V_{DD_}$ = 5.5V	20			
$\overline{CS}$ Pulse Width High	t_{CSW}		40			ns
SCLK Period	t_{CP}		80			ns
$V_{DD_}$ High to $\overline{CS}$ Low		Power-on reset delay		5		µs

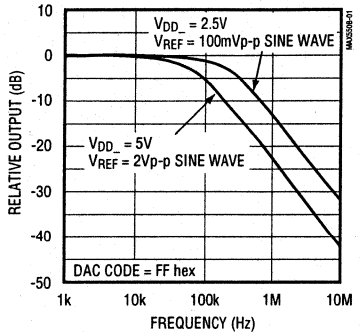
Note 5: Guaranteed by design. Not production tested.

Low-Power, +2.5V to +5.5V, 8-Bit Voltage-Output DAC in µMAX

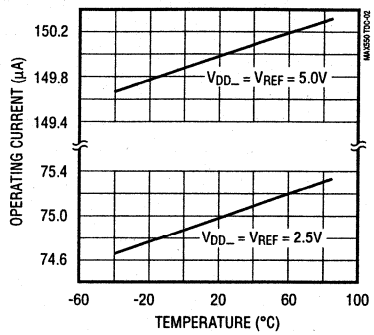
Typical Operating Characteristics

(V_{DD1} = V_{DD2} = 2.5V, V_{REF} = $V_{DD_}$, R_L = 1MΩ, C_L = 15pF, T_A = +25°C, unless otherwise noted.)

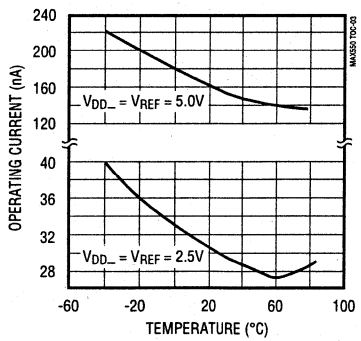
REFERENCE FREQUENCY RESPONSE



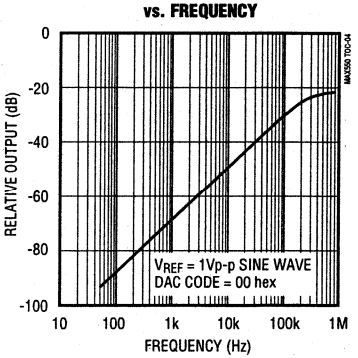
OPERATING CURRENT vs. TEMPERATURE



SHUTDOWN CURRENT vs. TEMPERATURE



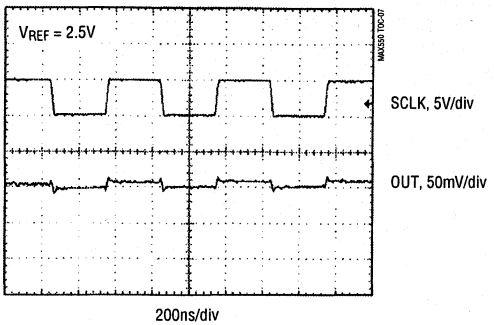
REFERENCE AC FEEDTHROUGH vs. FREQUENCY



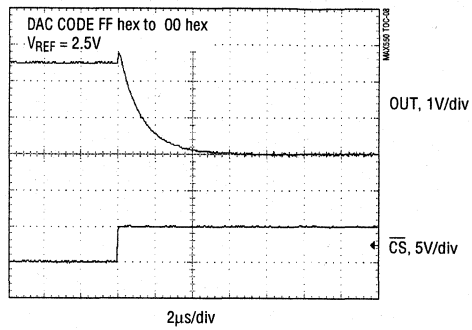
Typical Operating Characteristics (continued)

(V_{DD1} = V_{DD2} = 2.5V, V_{REF} = $V_{DD_}$, R_L = 1MΩ, C_L = 15pF, T_A = +25°C, unless otherwise noted.)

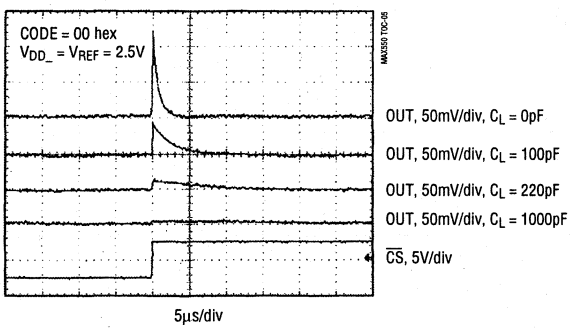
DIGITAL FEEDTHROUGH



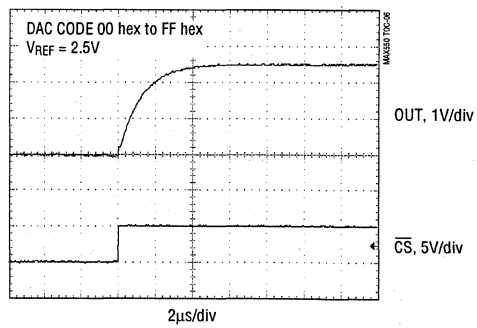
NEGATIVE SETTLING TIME



OUTPUT GLITCH FILTERING



POSITIVE SETTLING TIME



Low-Power, +2.5V to +5.5V, 8-Bit Voltage-Output DAC in µMAX

Pin Description

PIN	NAME	FUNCTION
1	GND	Ground
2	OUT	DAC Output Voltage
3	$\overline{CS}$	Chip-Select Input. A logic low on $\overline{CS}$ enables serial data to be clocked into the input shift register. Programming commands are executed at $\overline{CS}$'s rising edge.
4	DIN	Serial Data Input. Data is clocked into the 16-bit input shift register on SCLK's rising edge.
5	SCLK	Serial Clock Input. Data is clocked in on SCLK's rising edge.
6	V_{DD2}	Connect to V_{DD1}
7	REF	External Reference Voltage Input for DAC (2.5V to $V_{DD_}$)
8	V_{DD1}	Positive Power Supply (+2.5V to +5.5V)

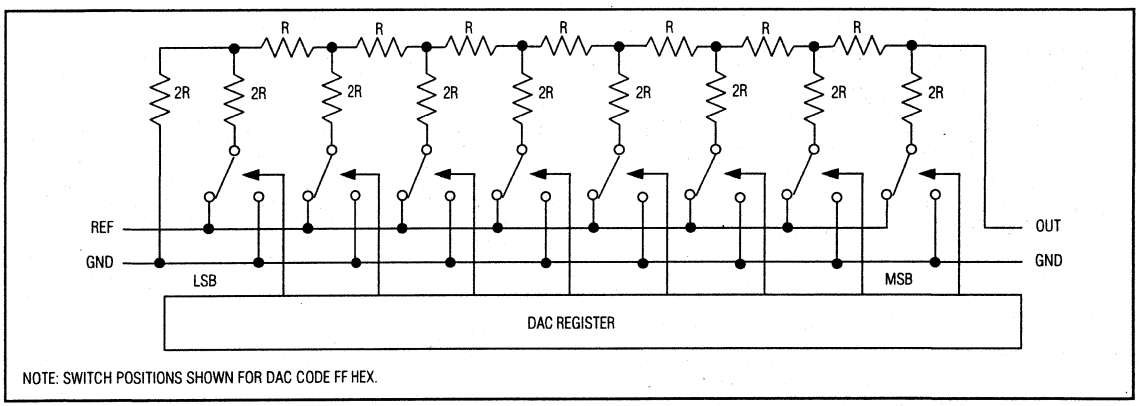


Figure 1. DAC Simplified Circuit Diagram

Detailed Description

Analog Section

The MAX550B is an 8-bit, voltage-output digital-to-analog converter (DAC). The DAC consists of an R-2R ladder network that converts 8-bit digital inputs into equivalent analog output voltages in proportion to the applied reference voltage (Figure 1). The MAX550B's output is unbuffered and has a typical output resistance of 32kΩ. The power-supply range is from +2.5V to +5.5V.

Reference Input

The voltage applied at REF sets the full-scale output for the DAC and may range from 2.5V to $V_{DD_}$. The REF input resistance is code-dependent, with the lowest value (typically 32kΩ) occurring when the DAC register is loaded with a code of 01010101 (55 hex). To minimize INL errors, the reference voltage source should have less than 6Ω output impedance.

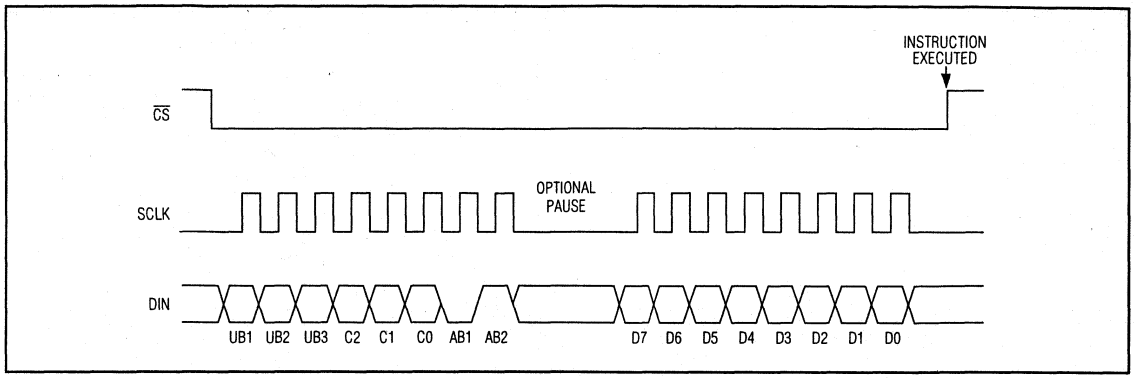


Figure 2. Serial-Interface Timing Diagram

DAC Output

The MAX550B's output is unbuffered; it connects directly to the R-2R ladder. This configuration minimizes power consumption and reduces offset errors. For highest accuracy, apply high resistive loads (1MΩ and up). Lower resistive loads can be driven, but output loading increases full-scale error. The magnitude of the expected error is the ratio of the DAC output resistance to the DC load resistance at the output.

Typically, an energy pulse is coupled into the DAC output on the rising edge of $\overline{CS}$. Since the MAX550B's output is unbuffered (connected directly to the R-2R ladder), connecting a small capacitor (200pF to 1000pF) from the output to ground creates a lowpass filter that effectively suppresses the pulse for sensitive applications (see Output Glitch Filtering graph in the *Typical Operating Characteristics*).

Shutdown Mode

When the MAX550B is in shutdown mode, REF becomes high impedance. The supply current is unchanged, but the REF input current decreases to less than 1µA. This allows the system reference to remain active with minimal power consumption.

When exiting shutdown mode, the output recovery time is equivalent to the DAC settling time.

Serial Interface

The MAX550B interface is compatible with 3-wire SPI™, QSPI™, and Microwire™ microprocessor (µP) interface standards. An active-low chip select ($\overline{CS}$) enables the input shift register to receive data from the serial input, DIN (Figure 2). Data is clocked into the input shift register on rising edges of the serial clock signal (SCLK). The clock frequency can be as high as 10MHz.

When writing to the DAC, transmit data MSB first in one 16-bit word or two 8-bit bytes. The write cycle can be segmented when $\overline{CS}$ is kept active (low) to allow two 8-bit-wide transfers. After clocking all 16 bits into the input shift register, a rising edge on $\overline{CS}$ programs the DAC. The DAC output reflects the data stored in the DAC register. Figure 3 gives detailed timing information.

Initialization

The MAX550B has an internal power-on reset. At power-up, all internal registers are reset to zero; therefore, an initialization write is not necessary.

Serial Input Data Format and Control Codes

The control byte programs the DAC (Table 1). Table 2 lists the MAX550B's serial-input command format. The 16-bit input word consists of an 8-bit control byte and an 8-bit data byte. The 8-bit control byte is not decoded internally; every control bit performs one function. Data is clocked in starting with unassigned bit 1 (UB1), followed by the remaining control bits and the DAC data byte. The LSB (D0) of the data byte is the last bit clocked into the input shift register (Figure 2).

Table 3 is an example of a 16-bit word. It performs the following functions:

1) Load 80 hex (128 decimal) into the DAC register.
2) Update the DAC output on $\overline{CS}$'s rising edge.

Table 4 shows how to calculate the output voltage based on the input code.

Low-Power, +2.5V to +5.5V, 8-Bit Voltage-Output DAC in µMAX

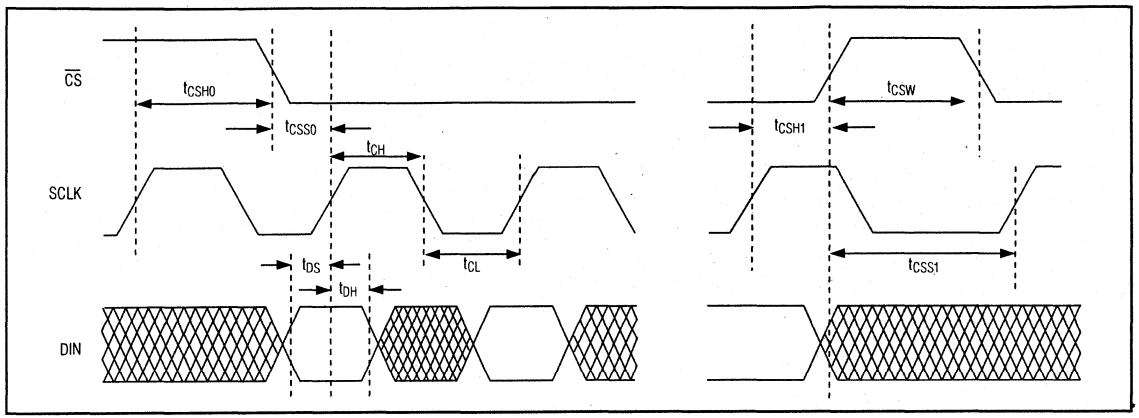


Figure 3. Detailed Serial-Interface Timing Diagram

Table 1. Control-Byte/Input-Word Bit Definitions

Control Byte	UB1*	X	Unassigned Bit 1
	UB2	X	Unassigned Bit 2
	UB3	X	Unassigned Bit 3
	C2	0	Power-Up Mode
	C2	1	Power-Down Mode
	C1	0	DAC Register Load Operation Disabled
	C1	1	DAC Register Load Operation Enabled
	C0	0	DAC Output Updated on Rising Edge of $\overline{CS}$
	C0	1	Unassigned Operation
	AB1	0	Assigned Bit 1
	AB2	1	Assigned Bit 2
Data Byte	D7	X	DAC Data Bit 7 (MSB)
	D6	X	DAC Data Bit 6
	D5	X	DAC Data Bit 5
	D4	X	DAC Data Bit 4
	D3	X	DAC Data Bit 3
	D2	X	DAC Data Bit 2
	D1	X	DAC Data Bit 1
	D0**	X	DAC Data Bit 0 (LSB)

X = Don't care
*Clocked in first
**Clocked in last

Microprocessor Interfacing

The MAX550B serial interface is compatible with Microwire, SPI, and QSPI interface standards. For SPI, clear the CPOL and CPHA bits (CPOL = 0 and CPHA = 0). CPOL = 0 sets the idle clock state to zero and CPHA = 0 changes data at SCLK's falling edge. This setting allows SPI to run at full clock speeds (1.5MHz). If a serial port is not available on your µP, three bits of a parallel port can be used to emulate a serial port by bit manipulation. Minimize digital feedthrough at the DAC output by operating the serial clock only when necessary.

Applications Information

Power-Supply and Ground Considerations

Connect GND to the highest-quality ground available. Bypass V_{DD} with a 0.1µF to 0.22µF capacitor to GND. The reference input can be used without bypassing. However, for optimum line/load-transient response and noise performance, bypass the reference input with a 0.1µF to 4.7µF capacitor to GND.

Careful PC board layout minimizes crosstalk between the DAC output, the reference, and the digital inputs. Separate analog traces by running ground traces between them. Make sure high-frequency digital lines are not routed parallel to analog lines.

Table 2. Serial-Interface Programming Commands

CONTROL BYTE								DATA BYTE								COMMAND
Loaded First								Loaded Last								
UB1	UB2	UB3	C2	C1	C0	AB1	AB2	D7	D6	D5	D4	D3	D2	D1	D0	
X	X	X	0	0	0	0	1	X	X	X	X	X	X	X	X	On $\overline{CS}$'s rising edge, wake up DAC. DAC register unchanged.
X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	Unassigned command
X	X	X	0	1	0	0	1	8-bit DAC data								On $\overline{CS}$'s rising edge, load DAC register. Wake up DAC (if previously powered down).
X	X	X	1	0	0	0	1	X	X	X	X	X	X	X	X	On $\overline{CS}$'s rising edge, power down DAC. DAC output goes to zero. DAC register unchanged.
X	X	X	1	1	0	0	1	8-bit DAC data								On $\overline{CS}$'s rising edge, power down DAC and update DAC register. DAC output goes to zero.

X = Don't Care

Table 3. Example Input Word

Loaded First															Loaded Last
UB1	UB2	UB3	C2	C1	C0	AB1	AB2	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	0	1	0	0	1	1	0	0	0	0	0	0	0

X = Don't Care

Table 4. Analog Output vs. Code

DAC REGISTER CONTENTS								ANALOG OUTPUT (V)
D7	D6	D5	D4	D3	D2	D1	D0	
1	1	1	1	1	1	1	1	$+V_{REF} \times (255/256)$
1	0	0	0	0	0	0	1	$+V_{REF} \times (129/256)$
1	0	0	0	0	0	0	0	$+V_{REF} \times (128/256) = +V_{REF}/2$
0	1	1	1	1	1	1	1	$+V_{REF} \times (127/256)$
0	0	0	0	0	0	0	1	$+V_{REF} \times (1/256)$
0	0	0	0	0	0	0	0	0

Note: 1LSB = $V_{REF} \times 2^{-8} = V_{REF}(1/256)$
ANALOG OUTPUT = $+V_{REF}(I/256)$, where I = Integer Value of Digital Input and wake up DAC (if previously powered down)

Low-Power, +2.5V to +5.5V, 8-Bit Voltage-Output DAC in µMAX

AC Considerations

Digital Feedthrough

High-speed data at any of the digital input pins may couple through the DAC's internal stray capacitance and cause noise (digital feedthrough) at the DAC output, even though $\overline{CS}$ is held high. This digital feedthrough is tested by holding $\overline{CS}$ high and toggling the digital inputs from all 1s to all 0s.

Analog Feedthrough

Due to internal stray capacitance, higher-frequency analog input signals at REF may couple to the output, even when the input digital code is all 0s. Test analog feedthrough by setting the DAC output to 0V and sweeping REF.

Chip Information

TRANSISTOR COUNT: 1562

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

10/96

MAXIM

High-Speed (165Msps/275Msps), 8-Bit DAC

General Description

The MAX5018 is a monolithic, 8-bit digital-to-analog converter (DAC) capable of accepting video data at a 165Msps or 275Msps rate. Complete with video controls—Sync, Blank, Bright, Reference White (force high)—the MAX5018 directly drives doubly terminated 50Ω or 75Ω loads to standard composite video levels. The standard set-up level is 7.5 IRE.

The MAX5018 is pin compatible with the HDAC10180 and TDC1018, with improved performance. It contains data and control input registers, video control logic, a reference buffer, and current switches. This device is available in a 24-pin DIP package in the industrial temperature range.

Applications

High-Resolution Color or Monochrome Raster Graphics Displays

Medical Electronics: CAT, PET, MR Imaging Displays

CAD/CAE Workstations

Solids Modeling

General-Purpose High-Speed D/A Conversion

Digital Synthesizers

Automated Test Equipment

Digital Transmitters/Modulators

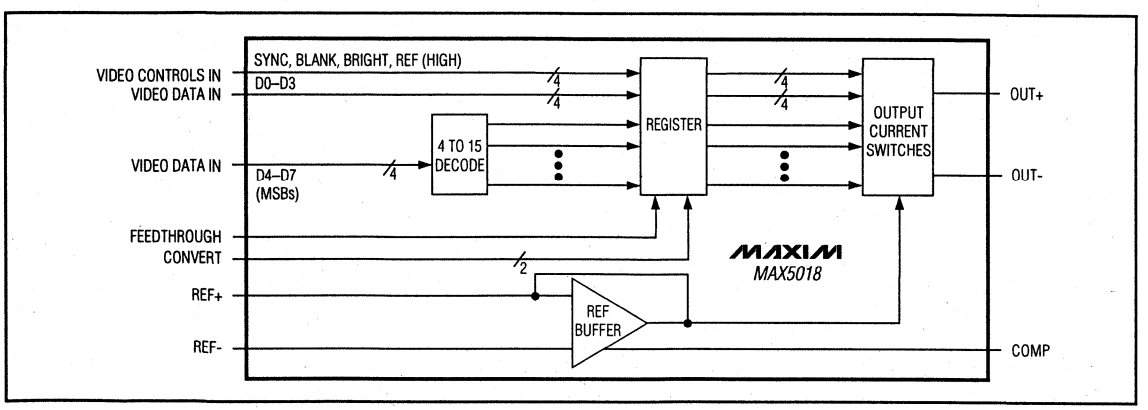
Features

- **275Msps Conversion Rate (MAX5018A)**
  165Msps Conversion Rate (MAX5018B)
- **Compatible Upgrade to HDAC10180 and TDC1018**
- **RS-343-A Compatible**
- **Complete Video Controls: Sync, Blank, Bright, and Reference White (force high)**
- **10kH, 100k ECL Compatible**
- **Single Power Supply**
- **Registered Data and Video Controls**
- **Differential Current Outputs**
- **ESD-Protected Data and Control Inputs**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX5018AIPG	-20°C to +85°C	24 Wide Plastic DIP
MAX5018BIPB	-20°C to +85°C	24 Wide Plastic DIP

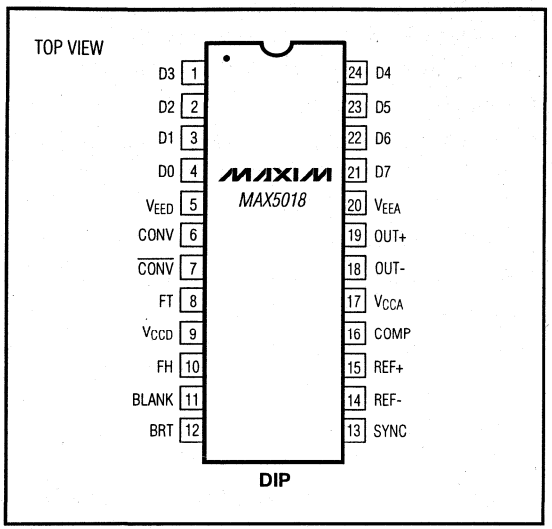
Functional Diagram



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High-Speed (165Msps/275Msps), 8-Bit DAC

Pin Configuration



ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

10/96

MAXIM

Ultra-High-Speed (400Msps), 8-Bit DAC

General Description

The MAX5140 is a monolithic, 8-bit digital-to-analog converter (DAC) capable of accepting video data at a 400Msps rate. Complete with video controls—Sync, Blank, Bright, Reference White (force high)—the MAX5140 directly drives doubly terminated 50Ω or 75Ω loads to standard composite video levels. The standard set-up level is 7.5 IRE.

The MAX5140 includes a precision bandgap reference, which can drive two other MAX5140s in an RGB graphics system. This device is available in a 24-pin DIP package in the industrial temperature range.

Applications

Raster Graphics Displays

High-Resolution Color or Monochrome Displays to 2k x 2k Pixels

Medical Electronics: CAT, PET, MR Imaging Displays

CAD/CAE Workstations

Solids Modeling

General-Purpose High-Speed D/A Conversion

Digital Synthesizers

Automated Test Equipment

Digital Transmitters/Modulators

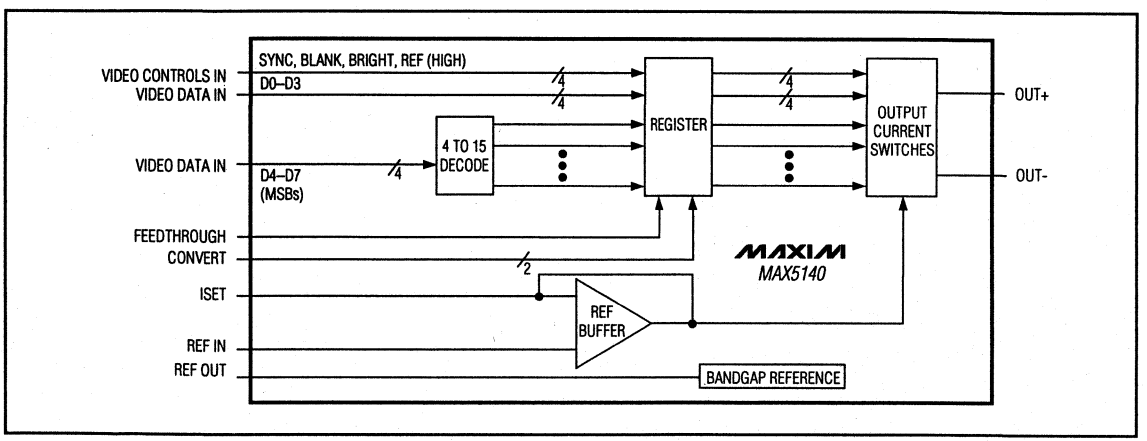
Features

- **400Msps Nominal Conversion Rate**
- **RS-343-A Compatible**
- **Complete Video Controls: Sync, Blank, Bright, and Reference White (force high)**
- **10kH, 100k ECL Compatible**
- **Single Power Supply**
- **Registered Data and Video Controls**
- **Differential Current Outputs**
- **Stable On-Chip Bandgap Reference**
- **50Ω and 75Ω Output Drive**
- **ESD-Protected Data and Control Inputs**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX5140IPG	-20°C to +85°C	24 Wide Plastic DIP

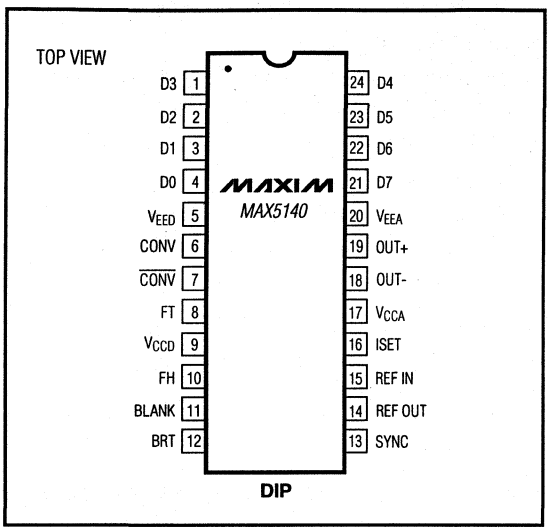
Functional Diagram



For the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Ultra-High-Speed (400Msps), 8-Bit DAC

Pin Configuration



ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

11/96

MAXIM

+5V, Quad, 10-Bit Voltage-Output DAC with Serial Interface

General Description

The +5V MAX5250 combines four low-power, voltage-output, 10-bit digital-to-analog converters (DACs) and four precision output amplifiers in a space-saving, 20-pin package. In addition to the four voltage outputs, each amplifier's negative input is also available to the user. This facilitates specific gain configurations, remote sensing, and high output drive capacity, making the MAX5250 ideal for a wide range of applications. Other features include software shutdown, hardware shutdown lockout, an active-low reset that clears all registers and DACs to zero, a user-programmable logic output, and a serial-data output.

Each DAC has a double-buffered input organized as an input register followed by a DAC register. A 16-bit serial word loads data into each input/DAC register. The 3-wire serial interface is compatible with SPI™/QSPI™ and Microwire™. It allows the input and DAC registers to be updated independently or simultaneously with a single software command. All logic inputs are TTL/CMOS-logic compatible.

Applications

Industrial Process Controls
Automatic Test Equipment
Digital Offset and Gain Adjustment
Motion Control
Remote Industrial Controls
Microprocessor-Controlled Systems

Features

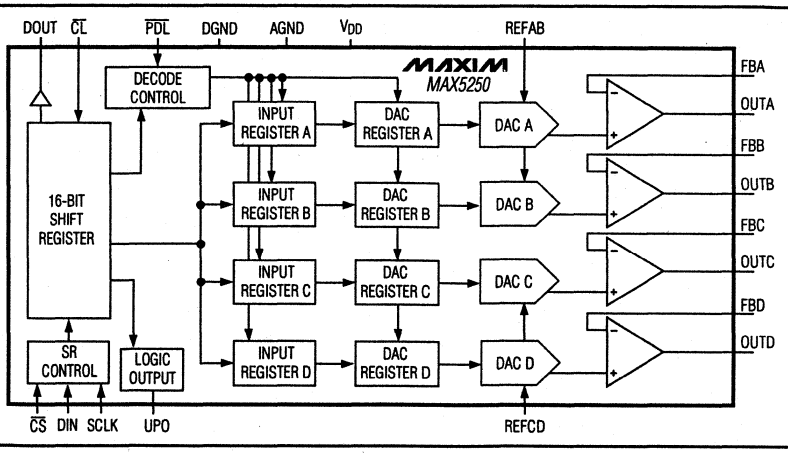
- ♦ **Four 10-Bit DACs with Configurable Output Amplifiers**
- ♦ **+5V Single-Supply Operation**
- ♦ **Low Supply Current: 0.85mA Normal Operation**
  10µA Shutdown Mode
- ♦ **Available in 20-Pin SSOP**
- ♦ **Power-On Reset Clears all Registers and DACs to Zero**
- ♦ **SPI/QSPI and Microwire Compatible**
- ♦ **Simultaneous or Independent Control of DACs via 3-Wire Serial Interface**
- ♦ **User-Programmable Digital Output**
- ♦ **12-Bit Upgrade Available: MAX525**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX5250ACPP	0°C to +70°C	20 Plastic DIP	±1/2
MAX5250BCPP	0°C to +70°C	20 Plastic DIP	±1
MAX5250ACAP	0°C to +70°C	20 SSOP	±1/2
MAX5250BCAP	0°C to +70°C	20 SSOP	±1

Ordering Information continued on next page.

Functional Diagram



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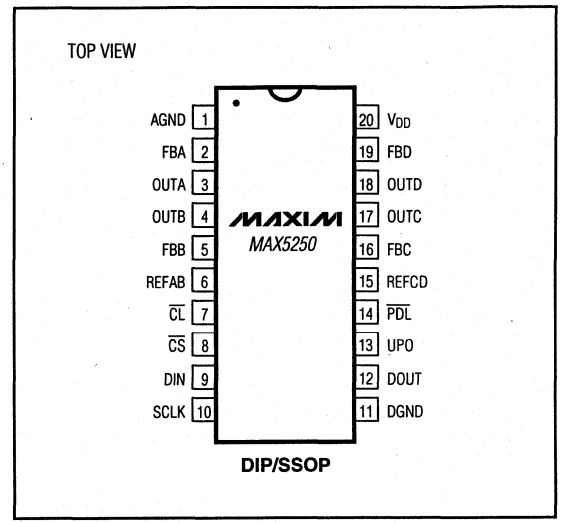
+5V, Quad, 10-Bit Voltage-Output DAC with Serial Interface

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX5250AEPP	-40°C to +85°C	20 Plastic DIP	±1/2
MAX5250BEPP	-40°C to +85°C	20 Plastic DIP	±1
MAX5250AEAP	-40°C to +85°C	20 SSOP	±1/2
MAX5250BEAP	-40°C to +85°C	20 SSOP	±1
MAX5250BMJP	-55°C to +125°C	20 CERDIP*	±1

*Contact factory for availability and processing to MIL-STD-883.

_Pin Configuration



ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

11/96

MAXIM

+3V, Quad, 10-Bit Voltage-Output DAC with Serial Interface

General Description

The +3V MAX5251 combines four low-power, voltage-output, 10-bit digital-to-analog converters (DACs) and four precision output amplifiers in a space-saving, 20-pin package. In addition to the four voltage outputs, each amplifier's negative input is also available to the user. This facilitates specific gain configurations, remote sensing, and high output drive capacity, making the MAX5251 ideal for a wide range of applications. Other features include software shutdown, hardware shutdown lockout, an active-low reset that clears all registers and DACs to zero, a user-programmable logic output, and a serial-data output.

Each DAC has a double-buffered input organized as an input register followed by a DAC register. A 16-bit serial word loads data into each input/DAC register. The 3-wire serial interface is compatible with SPI™/QSPI™ and Microwire™. It allows the input and DAC registers to be updated independently or simultaneously with a single software command. All logic inputs are TTL/CMOS-logic compatible.

Applications

Industrial Process Controls
Automatic Test Equipment
Digital Offset and Gain Adjustment
Motion Control
Remote Industrial Controls
Microprocessor-Controlled Systems

Features

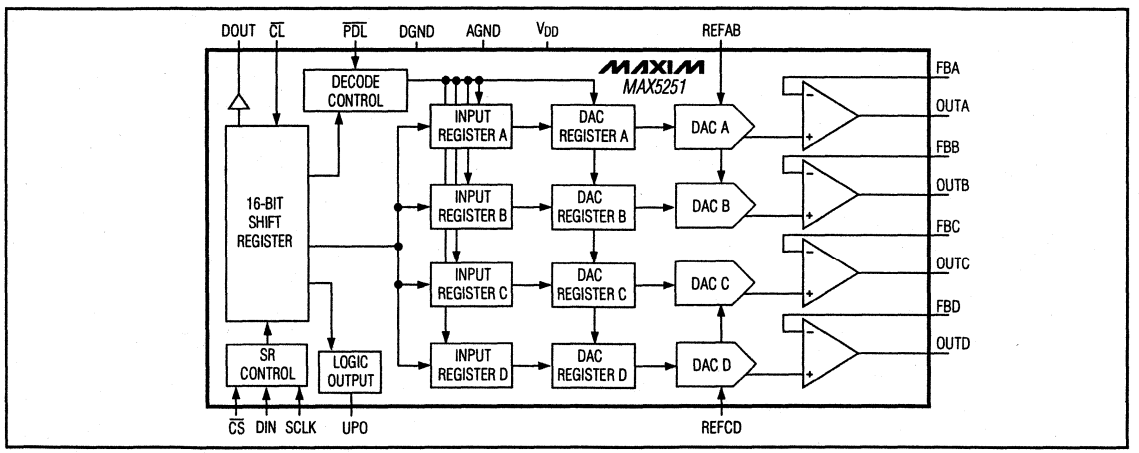
- ♦ **Four 10-Bit DACs with Configurable Output Amplifiers**
- ♦ **+3.0V to +3.6V Single-Supply Operation**
- ♦ **Low Supply Current: 0.8mA Normal Operation**
  3µA Shutdown Mode
- ♦ **Reference Inputs are High Impedance in Shutdown**
- ♦ **Available in 20-Pin SSOP**
- ♦ **Power-On Reset Clears all Registers and DACs to Zero**
- ♦ **SPI/QSPI and Microwire Compatible**
- ♦ **Simultaneous or Independent Control of DACs via 3-Wire Serial Interface**
- ♦ **User-Programmable Digital Output**
- ♦ **12-Bit Upgrade Available: MAX5253**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX5251ACPP	0°C to +70°C	20 Plastic DIP	±1/2
MAX5251BCPP	0°C to +70°C	20 Plastic DIP	±1
MAX5251ACAP	0°C to +70°C	20 SSOP	±1/2
MAX5251BCAP	0°C to +70°C	20 SSOP	±1

Ordering Information continued on next page.

Functional Diagram



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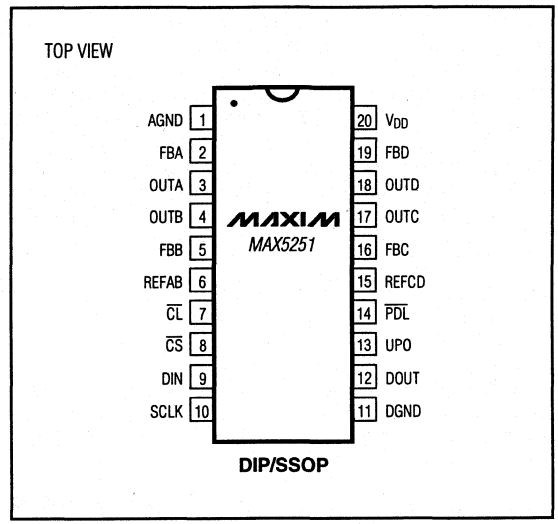
+3V, Quad, 10-Bit Voltage-Output DAC with Serial Interface

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX5251AEPP	-40°C to +85°C	20 Plastic DIP	±1/2
MAX5251BEPP	-40°C to +85°C	20 Plastic DIP	±1
MAX5251AEAP	-40°C to +85°C	20 SSOP	±1/2
MAX5251BEAP	-40°C to +85°C	20 SSOP	±1
MAX5251BMJP	-55°C to +125°C	20 CERDIP*	±2

*Contact factory for availability and processing to MIL-STD-883.

_____Pin Configuration



19-1123; Rev 0; 9/96

MAXIM

+3V, Quad, 12-Bit Voltage-Output DAC with Serial Interface

General Description

The MAX5253 combines four low-power, voltage-output, 12-bit digital-to-analog converters (DACs) and four precision output amplifiers in a space-saving, 20-pin package. In addition to the four voltage outputs, each amplifier's negative input is also available to the user. This facilitates specific gain configurations, remote sensing, and high output drive capacity, making the MAX5253 ideal for industrial-process-control applications. Other features include software shutdown, hardware shutdown lockout, an active-low reset which clears all registers and DACs to zero, a user-programmable logic output, and a serial-data output.

Each DAC has a double-buffered input organized as an input register followed by a DAC register. A 16-bit serial word loads data into each input/DAC register. The serial interface is compatible with SPI™/QSPI™ and Microwire™. It allows the input and DAC registers to be updated independently or simultaneously with a single software command. The DAC registers can be simultaneously updated via the 3-wire serial interface. All logic inputs are TTL/CMOS-logic compatible.

Applications

Industrial Process Controls
Automatic Test Equipment
Digital Offset and Gain Adjustment
Motion Control
Remote Industrial Controls
Microprocessor-Controlled Systems

Features

- ♦ **Four 12-Bit DACs with Configurable Output Amplifiers**
- ♦ **+3.0V to +3.6V Single-Supply Operation**
- ♦ **Low Supply Current: 0.82mA Normal Operation**
  3µA Shutdown Mode
- ♦ **Reference Inputs are High Impedance in Shutdown**
- ♦ **Available in 20-Pin SSOP**
- ♦ **Power-On Reset Clears all Registers and DACs to Zero**
- ♦ **SPI/QSPI and Microwire Compatible**
- ♦ **Simultaneous or Independent Control of DACs via 3-Wire Serial Interface**
- ♦ **User-Programmable Digital Output**

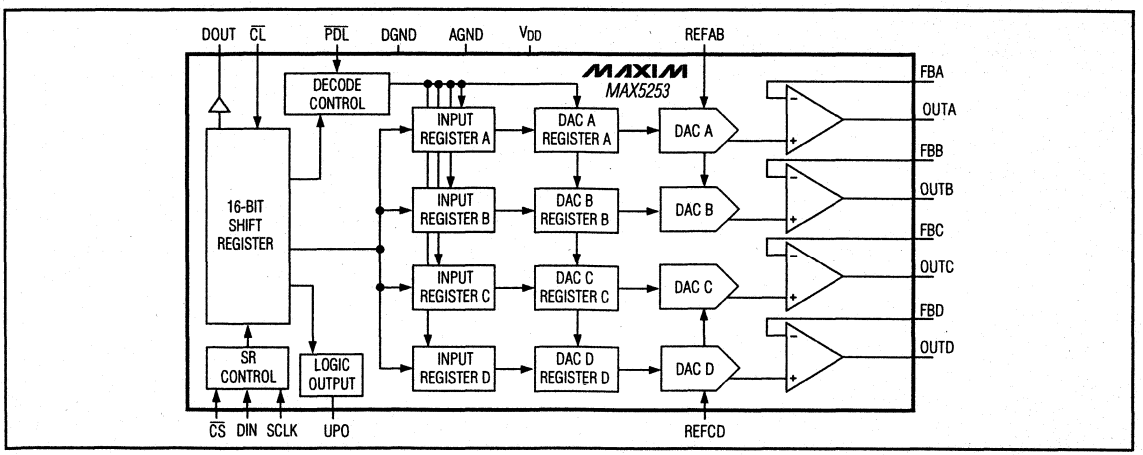
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX5253ACPP	0°C to +70°C	20 Plastic DIP	±1/2
MAX5253BCPP	0°C to +70°C	20 Plastic DIP	±1
MAX5253ACAP	0°C to +70°C	20 SSOP	±1/2
MAX5253BCAP	0°C to +70°C	20 SSOP	±1

Ordering Information continued on last page.

Pin Configuration appears at end of data sheet.

Functional Diagram



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+3V, Quad, 12-Bit Voltage-Output DAC with Serial Interface

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND .....-0.3V, +6V
V_{DD} to DGND .....-0.3V, +6V
AGND to DGND .....±0.3V
REFAB, REFCD to AGND .....-0.3V to (V_{DD} + 0.3V)
OUT_, FB_ to AGND .....-0.3V to (V_{DD} + 0.3V)
Digital Inputs to DGND .....-0.3V to +6V
DOUT, UPO to DGND .....-0.3V to (V_{DD} + 0.3V)
Continuous Current into Any Pin .....±20mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 8.00mW/°C above +70°C) 640mW
SSOP (derate 8.00mW/°C above +70°C) 640mW
CERDIP (derate 11.11mW/°C above +70°C) 889mW

Operating Temperature Ranges
MAX5253_C_P .....0°C to +70°C
MAX5253_E_P .....-40°C to +85°C
MAX5253BMJP .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +3.0V to +3.6V, AGND = DGND = 0V, REFAB = REFCD = 1.25V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 9).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE—ANALOG SECTION						
Resolution	N		12			Bits
Integral Nonlinearity (Note 1)	INL	MAX5253AC/E		±0.25	±0.5	LSB
		MAX5253BC/E			±1.0	
		MAX5253BMJP			±2.0	
Differential Nonlinearity	DNL	Guaranteed monotonic			±1.0	LSB
Offset Error	V_{OS}				±6.0	mV
Offset-Error Tempco				6		ppm/°C
Gain Error (Note 1)	GE				±4.0	LSB
Gain-Error Tempco				1		ppm/°C
Power-Supply Rejection Ratio	PSRR	V_{DD} = +3.0V to +3.6V			300	µV/V
MATCHING PERFORMANCE (T_A = +25°C)						
Gain Error	GE				±4.0	LSB
Offset Error				±1.0	±6.0	mV
Integral Nonlinearity	INL			±0.35	±1.0	LSB
REFERENCE INPUT						
Reference Input Range	V_{REF}		0		V_{DD} - 1.4	V
Reference Input Resistance	R_{REF}	Code-dependent, minimum at code 555 hex	10			kΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3.0V to +3.6V, AGND = DGND = 0V, REFAB = REFCD = 1.25V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 9).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MULTIPLYING-MODE PERFORMANCE						
Reference -3dB Bandwidth		V_{REF} = 0.67Vp-p		650		kHz
Reference Feedthrough		Input code = all 0s, V_{REF} = 1.6Vp-p at 1kHz		-84		dB
Signal-to-Noise Plus Distortion Ratio	SINAD	V_{REF} = 1Vp-p at 25kHz		72		dB
DIGITAL INPUTS						
Input High Voltage	V_{IH}		2.0			V
Input Low Voltage	V_{IL}				0.8	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}		0.01	±0.1	µA
Input Capacitance	C_{IN}			8		pF
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}	I_{SOURCE} = 2mA	V_{DD} - 0.5			V
Output Low Voltage	V_{OL}	I_{SINK} = 2mA		0.13	0.4	V
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate	SR			0.6		V/µs
Output Settling Time		To ±1/2LSB, V_{STEP} = 1.25V		16		µs
Output Voltage Swing		Rail to rail (Note 2)		0 to V_{DD}		V
Current into FB_				0	0.1	µA
OUT_ Leakage Current in Shutdown		R_L = ∞		0.01	±1	µA
Start-Up Time Exiting Shutdown Mode				20		µs
Digital Feedthrough		$\overline{CS}$ = V_{DD}, DIN = 100kHz		5		nV-s
Digital Crosstalk				5		nV-s
POWER SUPPLIES						
Supply Voltage	V_{DD}	(Note 3)	3.0		3.6	V
Supply Current	I_{DD}	(Note 4)		0.82	0.98	mA
Supply Current in Shutdown		(Note 4)		3	20	µA
Reference Current in Shutdown				0.01	±1	µA

Note 1: Guaranteed from code 11 to code 4095 in unity-gain configuration.
Note 2: Accuracy is better than 0.5LSB for V_{OUT} = 6mV to V_{DD} - 80mV, guaranteed by PSR test on endpoints.
Note 3: Remains operational with supply voltage as low as +2.7V.
Note 4: R_L = ∞, digital inputs at DGND or V_{DD}.

+3V, Quad, 12-Bit Voltage-Output DAC with Serial Interface

TIMING CHARACTERISTICS

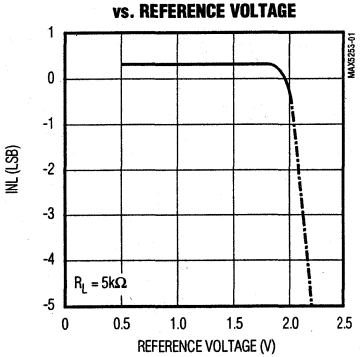
(V_{DD} = +3.0V to +3.6V, AGND = DGND = 0V, REFAB = REFCD =1.25V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 9).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Clock Period	t_{CP}		100			ns
SCLK Pulse Width High	t_{CH}		40			ns
SCLK Pulse Width Low	t_{CL}		40			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		40			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
DIN Setup Time	t_{DS}		40			ns
DIN Hold Time	t_{DH}		0			ns
SCLK Rise to DOUT Valid Propagation Delay	t_{D01}	C_L = 200pF			120	ns
SCLK Fall to DOUT Valid Propagation Delay	t_{D02}	C_L = 200pF			120	ns
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CS0}		40			ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	t_{CS1}		40			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		100			ns

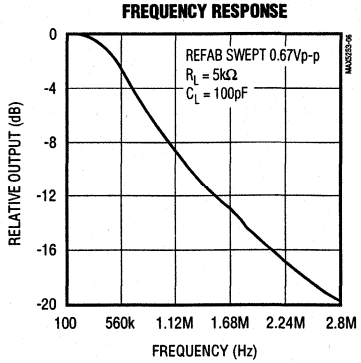
Typical Operating Characteristics

(V_{DD} = +3.3V, T_A = +25°C, unless otherwise noted.)

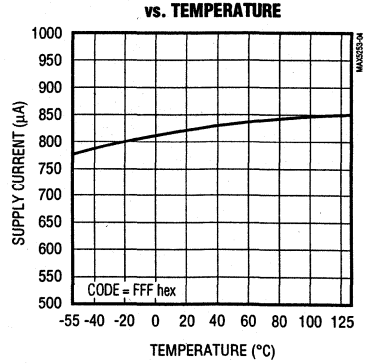
INTEGRAL NONLINEARITY vs. REFERENCE VOLTAGE



REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE



SUPPLY CURRENT vs. TEMPERATURE

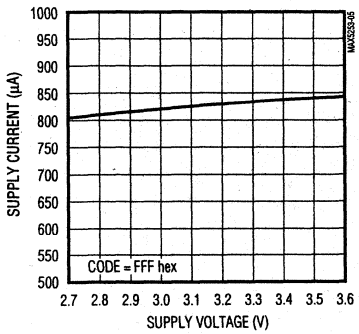


+3V, Quad, 12-Bit Voltage-Output DAC with Serial Interface

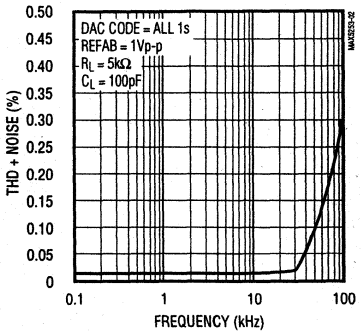
Typical Operating Characteristics (continued)

(V_{DD} = +3.3V, T_A = +25°C, unless otherwise noted.)

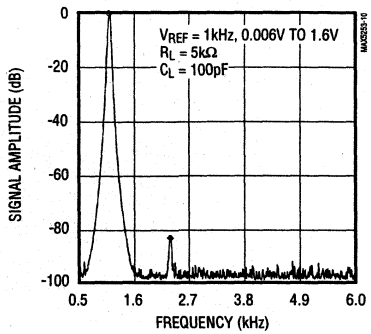
SUPPLY CURRENT vs. SUPPLY VOLTAGE



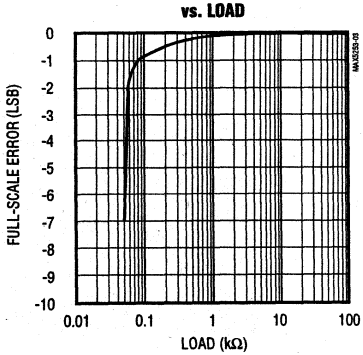
TOTAL HARMONIC DISTORTION PLUS NOISE vs. LOAD



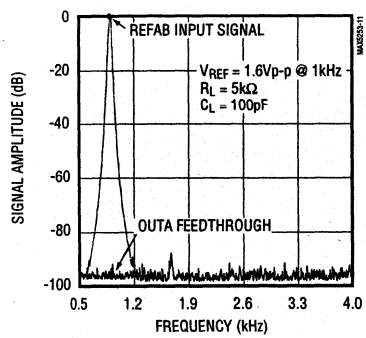
OUTPUT FFT PLOT



FULL-SCALE ERROR vs. LOAD



REFERENCE FEEDTHROUGH AT 1kHz

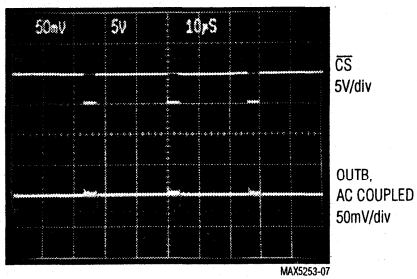


+3V, Quad, 12-Bit Voltage-Output DAC with Serial Interface

Typical Operating Characteristics (continued)

(V_{DD} = +3.3V, T_A = +25°C, unless otherwise noted.)

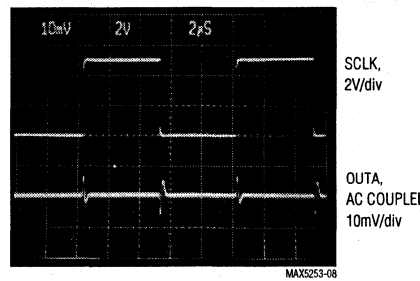
MAJOR-CARRY TRANSITION



10µs/div

V_{REF} = 1.25V, R_L = 5kΩ, C_L = 100pF

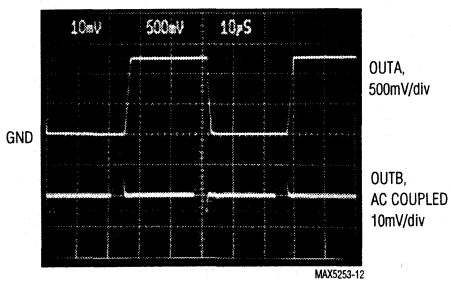
DIGITAL FEEDTHROUGH (SCLK = 100kHz)



2µs/div

V_{REF} = 1.25V, R_L = 5kΩ, C_L = 100pF
$\overline{CS}$ = $\overline{PDL}$ = $\overline{CL}$ = 3.3V, DIN = 0V
DAC A CODE SET TO 800 hex

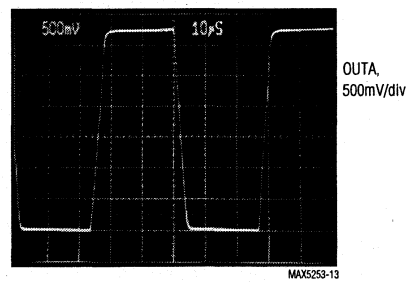
ANALOG CROSSTALK



10µs/div

V_{REF} = 1.25V, R_L = 5kΩ, C_L = 100pF
DAC A CODE SWITCHING FROM 00B hex TO FFF hex
DAC B CODE SET TO 800 hex

DYNAMIC RESPONSE



10µs/div

V_{REF} = 1.25V, R_L = 5kΩ, C_L = 100pF
SWITCHING FROM CODE 000 hex TO FB4 hex
OUTPUT AMPLIFIER GAIN = +2.6

Pin Description

PIN	NAME	FUNCTION
1	AGND	Analog Ground
2	FBA	DAC A Output Amplifier Feedback
3	OUTA	DAC A Output Voltage
4	OUTB	DAC B Output Voltage
5	FBB	DAC B Output Amplifier Feedback
6	REFAB	Reference Voltage Input for DAC A and DAC B
7	$\overline{CL}$	Clears All DACs and Registers. Resets all outputs (OUT_, UPO, DOUT) to 0, active low.
8	$\overline{CS}$	Chip-Select Input. Active low.
9	DIN	Serial-Data Input
10	SCLK	Serial Clock Input
11	DGND	Digital Ground
12	DOUT	Serial-Data Output
13	UPO	User-Programmable Logic Output
14	$\overline{PDL}$	Power-Down Lockout. Active low. Locks out software shutdown if low.
15	REFCD	Reference Voltage Input for DAC C and DAC D
16	FBC	DAC C Output Amplifier Feedback
17	OUTC	DAC C Output Voltage
18	OUTD	DAC D Output Voltage
19	FBD	DAC D Output Amplifier Feedback
20	V_{DD}	Positive Power Supply

+3V, Quad, 12-Bit Voltage-Output DAC with Serial Interface

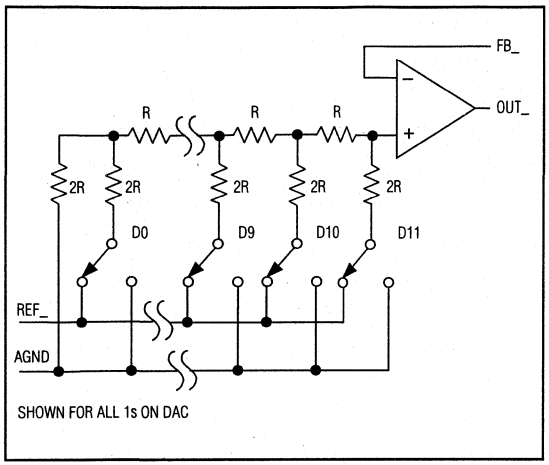


Figure 1. Simplified DAC Circuit Diagram

Detailed Description

The MAX5253 contains four 12-bit, voltage-output digital-to-analog converters (DACs) that are easily addressed using a simple 3-wire serial interface. It includes a 16-bit data-in/data-out shift register, and each DAC has a doubled-buffered input composed of an input register and a DAC register (see *Functional Diagram*). In addition to the four voltage outputs, each amplifier's negative input is available to the user.

The DACs are inverted R-2R ladder networks that convert 12-bit digital inputs into equivalent analog output voltages in proportion to the applied reference voltage inputs. DACs A and B share the REFAB reference input, while DACs C and D share the REFCD reference input. The two reference inputs allow different full-scale output voltage ranges for each pair of DACs. Figure 1 shows a simplified circuit diagram of one of the four DACs.

Reference Inputs

The two reference inputs accept positive DC and AC signals. The voltage at each reference input sets the full-scale output voltage for its two corresponding DACs. The reference input voltage range is 0V to (V_{DD} - 1.4V). The output voltages ($V_{OUT_}$) are represented by a digitally programmable voltage source as:

$$V_{OUT_} = (V_{REF} \times NB / 4096) \times Gain$$

where NB is the numeric value of the DAC's binary input code (0 to 4095), V_{REF} is the reference voltage, and Gain is the externally set voltage gain.

The impedance at each reference input is code-dependent, ranging from a low value of 10kΩ when both DACs connected to the reference have an input code of 555 hex, to a high value exceeding several gigohms (leakage current) with an input code of 000 hex. Because the input impedance at the reference pins is code-dependent, load regulation of the reference source is important.

The REFAB and REFCD reference inputs have a 10kΩ guaranteed minimum input impedance. When the two reference inputs are driven from the same source, the effective minimum impedance is 5kΩ. Driving the REFAB and REFCD pins separately improves reference accuracy.

In shutdown mode, the MAX5253's REFAB and REFCD inputs enter a high-impedance state with a typical input leakage current of 0.01µA.

The reference input capacitance is also code dependent and typically ranges from 20pF with an input code of all 0s to 100pF with an input code of all 1s.

Output Amplifiers

All MAX5253 DAC outputs are internally buffered by precision amplifiers with a typical slew rate of 0.6V/µs. Access to the inverting input of each output amplifier provides the user greater flexibility in output gain setting/signal conditioning (see the *Applications Information* section).

With a full-scale transition at the MAX5253 output, the typical settling time to ±1/2LSB is 16µs when loaded with 5kΩ in parallel with 100pF (loads less than 2kΩ degrade performance).

The MAX5253 output amplifier's output dynamic responses and settling performances are shown in the *Typical Operating Characteristics*.

Shutdown Mode

The MAX5253 features a software-programmable shutdown that reduces supply current to a typical value of 3µA. The power-down lockout ($\overline{PDL}$) pin must be high to enable the shutdown mode. Writing 1100XXXXXXXXXXXX as the input-control word puts the MAX5253 in shutdown mode (Table 1).

In shutdown mode, the MAX5253 output amplifiers and the reference inputs enter a high-impedance state. The serial interface remains active. Data in the input registers is retained in shutdown, allowing the MAX5253 to recall the output states prior to entering shutdown. Exit shutdown mode by either recalling the previous configuration or by updating the DACs with new data. When powering up the device or bringing it out of shutdown, allow 20µs for the outputs to stabilize.

Serial-Interface Configurations

The MAX5253's 3-wire serial interface is compatible with both Microwire™ (Figure 2) and SPI™/QSPI™ (Figure 3). The serial input word consists of two address bits and two control bits followed by 12 data bits (MSB first), as shown in Figure 4. The 4-bit address/control code determines the MAX5253's response outlined in Table 1. The connection between DOUT and the serial-interface port is not necessary, but may be used for data echo. Data held in the MAX5253's shift register can be shifted out of DOUT and returned to the microprocessor (µP) for data verification.

The MAX5253's digital inputs are double buffered. Depending on the command issued through the serial interface, the input register(s) can be loaded without affecting the DAC register(s), the DAC register(s) can be loaded directly, or all four DAC registers can be updated simultaneously from the input registers (Table 1).

Serial-Interface Description

The MAX5253 requires 16 bits of serial data. Table 1 lists the serial-interface programming commands. For certain commands, the 12 data bits are "don't cares." Data is sent MSB first and can be sent in two 8-bit packets or one 16-bit word ($\overline{CS}$ must remain low until 16 bits are transferred). The serial data is composed of two DAC address bits (A1, A0) and two control bits (C1,C0), followed by the 12 data bits D11...D0 (Figure 4).The 4-bit address/control code determines:

- The register(s) to be updated
- The clock edge on which data is to be clocked out via the serial-data output (DOUT)
- The state of the user-programmable logic output (UPO)
- If the part is to go into shutdown mode (assuming $\overline{PDL}$ is high)
- How the part is configured when exiting shutdown mode.

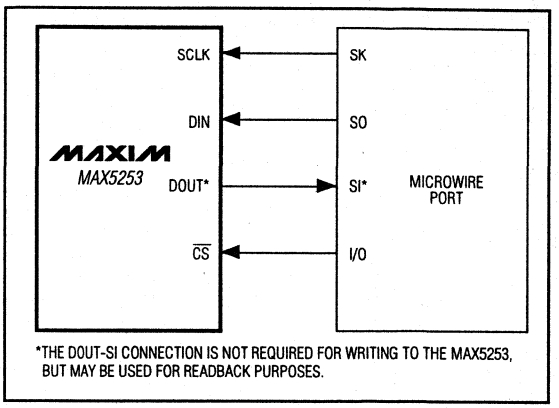


Figure 2. Connections for Microwire

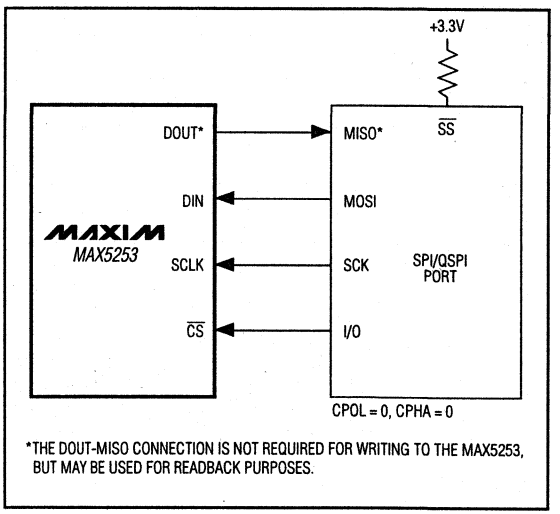


Figure 3. Connections for SPI/QSPI

MSB ..... LSB			
← 16 Bits of Serial Data →			
Address Bits		Control Bits	Data Bits MSB ..... LSB
A1	A0	C1 C0	D11 ..... D0
← 4 Address/Control Bits →			← 12 Data Bits →

Figure 4. Serial-Data Format

+3V, Quad, 12-Bit Voltage-Output DAC with Serial Interface

Table 1. Serial-Interface Programming Commands

16-BIT SERIAL WORD					FUNCTION
A1	A0	C1	C0	D11.....D0 MSB LSB	
0	0	0	1	12-bit DAC data	Load input register A; DAC registers unchanged.
0	1	0	1	12-bit DAC data	Load input register B; DAC registers unchanged.
1	0	0	1	12-bit DAC data	Load input register C; DAC registers unchanged.
1	1	0	1	12-bit DAC data	Load input register D; DAC registers unchanged.
0	0	1	1	12-bit DAC data	Load input register A; all DAC registers updated.
0	1	1	1	12-bit DAC data	Load input register B; all DAC registers updated.
1	0	1	1	12-bit DAC data	Load input register C; all DAC registers updated.
1	1	1	1	12-bit DAC data	Load input register D; all DAC registers updated.
0	1	0	0	XXXXXXXXXXXX	Update all DAC registers from their respective input registers (exit shutdown mode).
1	0	0	0	12-bit DAC data	Load all DAC registers from shift register (exit shutdown mode).
1	1	0	0	XXXXXXXXXXXX	Enter shutdown mode (provided $\overline{PDL}$ = 1)
0	0	1	0	XXXXXXXXXXXX	UPO goes low (default)
0	1	1	0	XXXXXXXXXXXX	UPO goes high
0	0	0	0	XXXXXXXXXXXX	No operation (NOP) to DAC registers
1	1	1	0	XXXXXXXXXXXX	Mode 1, DOUT clocked out on SCLK's rising edge. All DAC registers updated.
1	0	1	0	XXXXXXXXXXXX	Mode 0, DOUT clocked out on SCLK's falling edge. All DAC registers updated (default).

"X" = Don't care

Figure 5 shows the serial-interface timing requirements. The chip-select pin ($\overline{CS}$) must be low to enable the DAC's serial interface. When $\overline{CS}$ is high, the interface control circuitry is disabled. $\overline{CS}$ must go low at least t_{CSS} before the rising serial clock (SCLK) edge to properly clock in the first bit. When $\overline{CS}$ is low, data is clocked into the internal shift register via the serial-data input pin (DIN) on SCLK's rising edge. The maximum guaranteed clock frequency is 10MHz. Data is latched into the appropriate MAX5253 input/DAC registers on $\overline{CS}$'s rising edge.

The programming command Load-All-DACs-From-Shift-Register allows all input and DAC registers to be simultaneously loaded with the same digital code from the input shift register. The no operation (NOP) command leaves the register contents unaffected and is useful when the MAX5253 is configured in a daisy chain (see the *Daisy Chaining Devices* section). The command to change the clock edge on which serial data is shifted out of DOUT also loads data from all input registers to their respective DAC registers.

Serial-Data Output (DOUT)

The serial-data output, DOUT, is the internal shift register's output. The MAX5253 can be programmed so that data is clocked out of DOUT on SCLK's rising edge (Mode 1) or falling edge (Mode 0). In Mode 0, output data at DOUT lags input data at DIN by 16.5 clock cycles, maintaining compatibility with Microwire, SPI/QSPI, and other serial interfaces. In Mode 1, output data lags input data by 16 clock cycles. On power-up, DOUT defaults to Mode 0 timing.

User-Programmable Logic Output (UPO)

The user-programmable logic output, UPO, allows an external device to be controlled via the MAX5253 serial interface (Table 1).

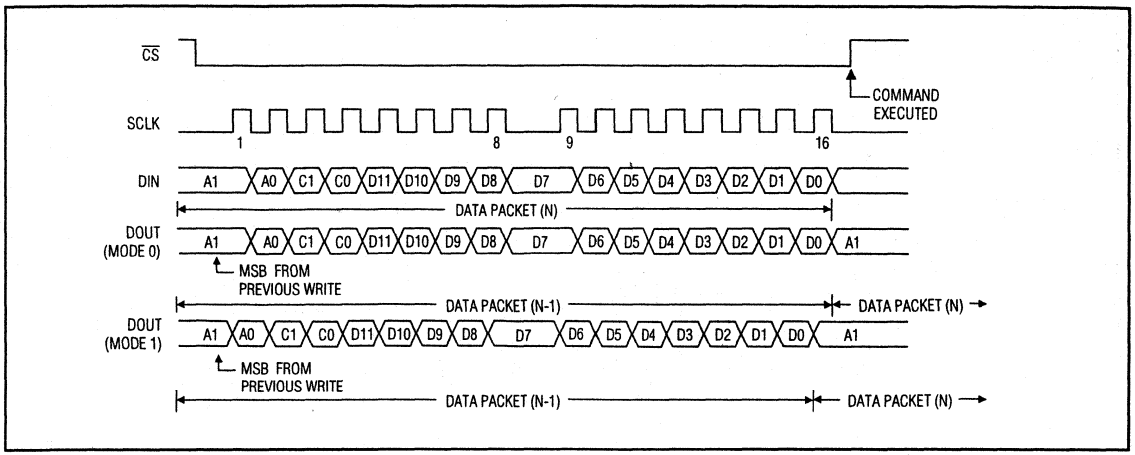


Figure 5. Serial-Interface Timing Diagram

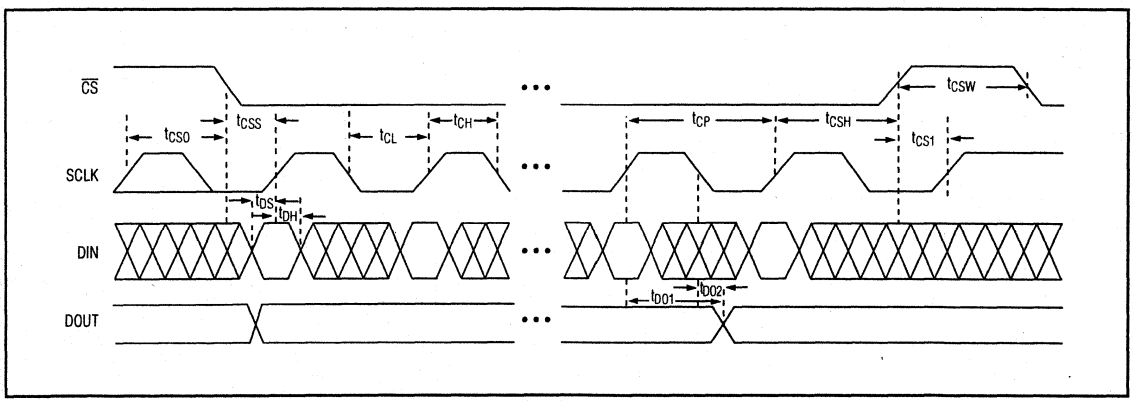


Figure 6. Detailed Serial-Interface Timing Diagram

Power-Down Lockout ($\overline{PDL}$)

The power-down lockout pin $\overline{PDL}$ disables software shutdown when low. When in shutdown, transitioning $\overline{PDL}$ from high to low wakes up the part with the output set to the state prior to shutdown. $\overline{PDL}$ could also be used to asynchronously wake up the device.

Daisy-Chaining Devices

Any number of MAX5253s can be daisy chained by connecting the DOUT pin of one device to the DIN pin of the following device in the chain (Figure 7).

Since the MAX5253's DOUT pin has an internal active pull-up, the DOUT sink/source capability determines the time required to discharge/charge a capacitive load. Refer to the serial-data-out V_{OH} and V_{OL} specifications in the *Electrical Characteristics*.

Figure 8 shows an alternate method of connecting several MAX5253s. In this configuration, the data bus is common to all devices; data is not shifted through a daisy chain. More I/O lines are required in this configuration because a dedicated chip-select input ($\overline{CS}$) is required for each IC.

+3V, Quad, 12-Bit Voltage-Output DAC with Serial Interface

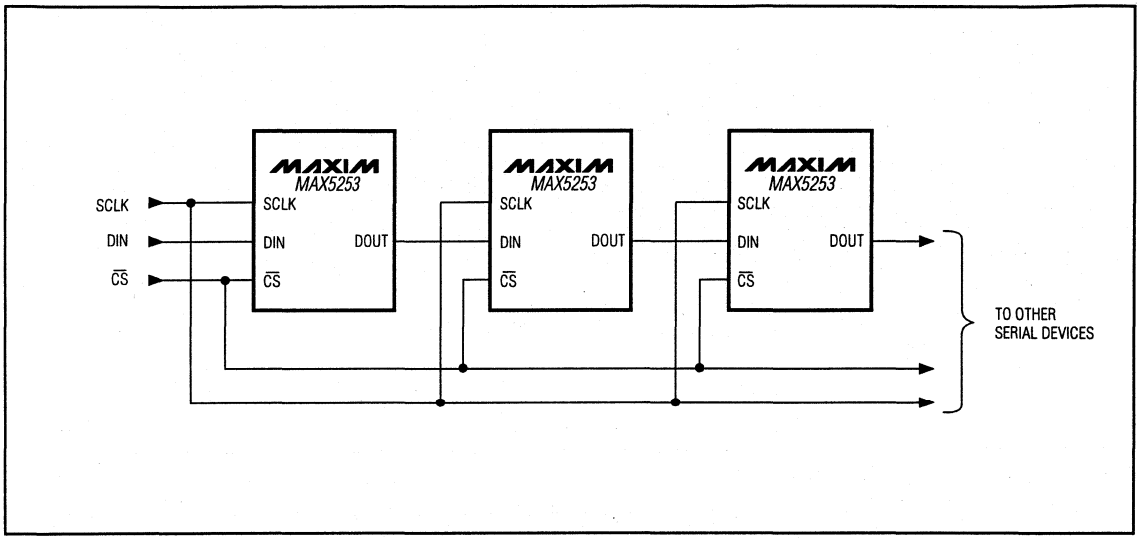


Figure 7. Daisy-Chaining MAX5253s

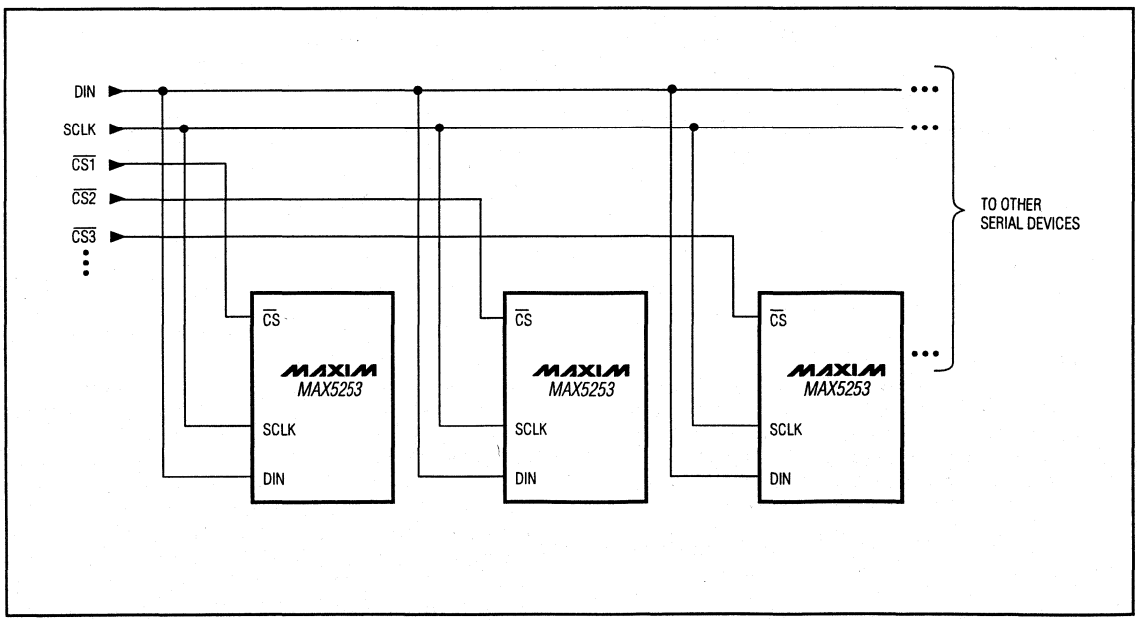


Figure 8. Multiple MAX5253s Sharing a Common DIN Line

Applications Information

Unipolar Output

For a unipolar output, the output voltages and the reference inputs have the same polarity. Figure 9 shows the MAX5253 unipolar output circuit, which is also the typical operating circuit. Table 2 lists the unipolar output codes.

For rail-to-rail outputs, see Figure 10. This circuit shows the MAX5253 with the output amplifiers configured with a closed-loop gain of +2.6 to provide 0V to 3.25V full-scale range when a 1.25V reference is used.

Table 2. Unipolar Code Table

DAC CONTENTS MSB LSB	ANALOG OUTPUT
1111 1111 1111	$+V_{REF}\left(\frac{4095}{4096}\right)$
1000 0000 0001	$+V_{REF}\left(\frac{2049}{4096}\right)$
1000 0000 0000	$+V_{REF}\left(\frac{2048}{4096}\right)=\frac{+V_{REF}}{2}$
0111 1111 1111	$+V_{REF}\left(\frac{2047}{4096}\right)$
0000 0000 0001	$+V_{REF}\left(\frac{1}{4096}\right)$
0000 0000 0000	0V

Table 3. Bipolar Code Table

DAC CONTENTS MSB LSB	ANALOG OUTPUT
1111 1111 1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 0001	$-V_{REF}\left(\frac{2047}{2048}\right)$
0000 0000 0000	$-V_{REF}\left(\frac{2048}{2048}\right)=-V_{REF}$

Bipolar Output

The MAX5253 outputs can be configured for bipolar operation using Figure 11's circuit.

$$V_{OUT} = V_{REF}[(2NB / 4096) - 1]$$

where NB is the numeric value of the DAC's binary input code. Table 3 shows digital codes (offset binary) and corresponding output voltages for Figure 11's circuit.

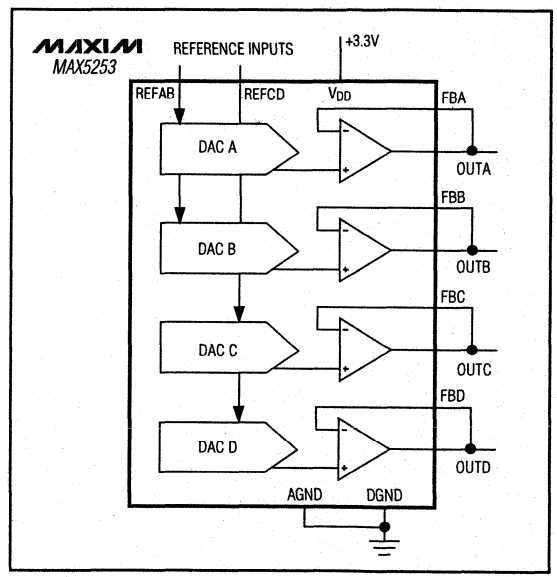


Figure 9. Unipolar Output Circuit

+3V, Quad, 12-Bit Voltage-Output DAC with Serial Interface

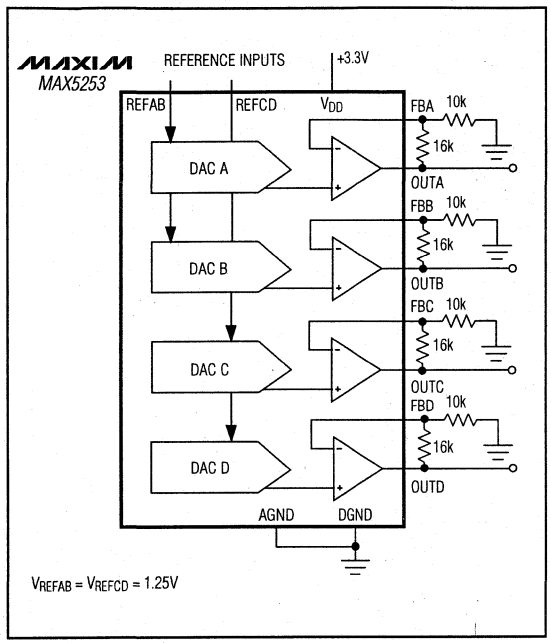


Figure 10. Unipolar Rail-to-Rail Output Circuit

Using an AC Reference

In applications where the reference has AC signal components, the MAX5253 has multiplying capability within the reference input range specifications. Figure 12 shows a technique for applying a sine-wave signal to the reference input where the AC signal is offset before being applied to REFAB/REFCD. The reference voltage must never be more negative than DGND.

The MAX5253's total harmonic distortion plus noise (THD + N) is typically less than -72dB, given a 1Vp-p signal swing and input frequencies up to 25kHz. The typical -3dB frequency is 650kHz, as shown in the *Typical Operating Characteristics* graphs.

Digitally Programmable Current Source

The circuit of Figure 13 places an NPN transistor (2N3904 or similar) within the op-amp feedback loop to implement a digitally programmable, unidirectional current source. This circuit can be used to drive 4mA to 20mA current loops, which are commonly used in industrial-control applications. The output current is calculated with the following equation:

$$I_{OUT} = (V_{REF} / R) \times (NB / 4096)$$

where NB is the numeric value of the DAC's binary input code and R is the sense resistor shown in Figure 13.

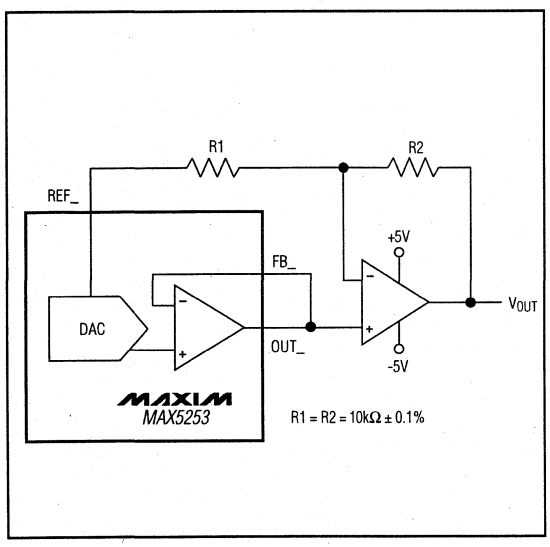


Figure 11. Bipolar Output Circuit

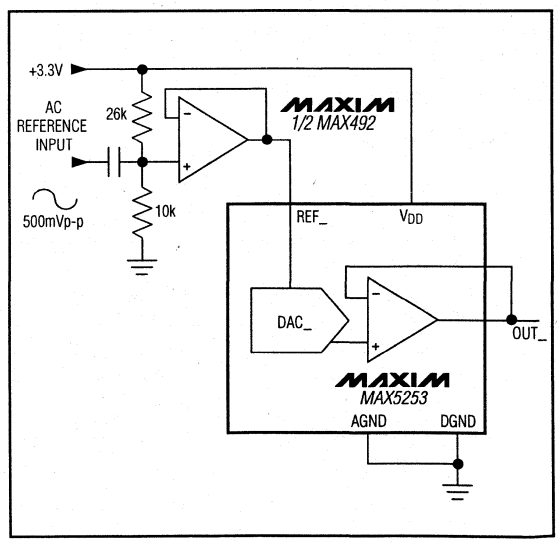


Figure 12. AC Reference Input Circuit

+3V, Quad, 12-Bit Voltage-Output DAC with Serial Interface

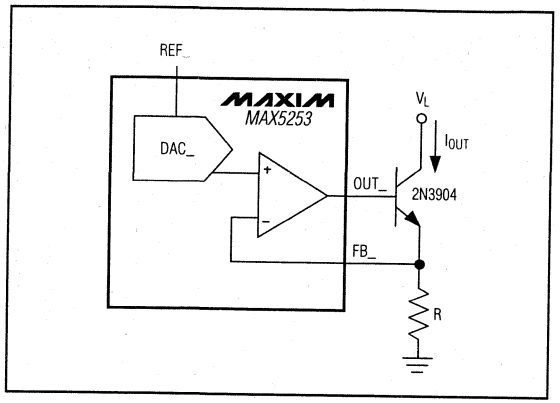


Figure 13. Digitally Programmable Current Source

Power-Supply Considerations

On power-up, all input and DAC registers are cleared (set to zero code) and DOUT is in Mode 0 (serial data is shifted out of DOUT on the clock's falling edge).

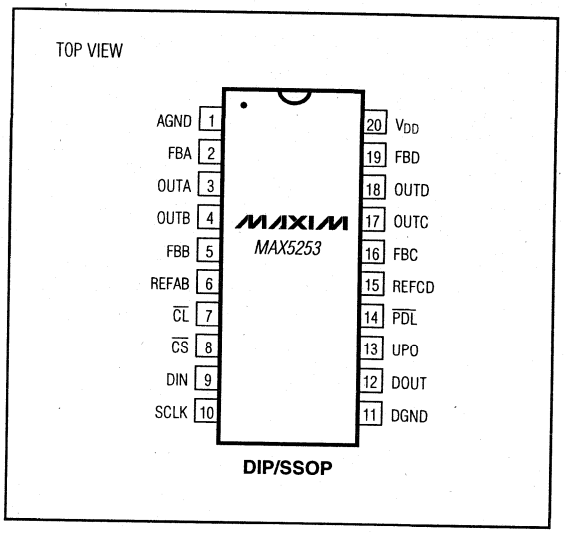
For rated MAX5253 performance, limit REFAB/REFCD to less than 1.4V below V_{DD}. Bypass V_{DD} with a 4.7µF capacitor in parallel with a 0.1µF capacitor to AGND. Use short lead lengths and place the bypass capacitors as close to the supply pins as possible.

Grounding and Layout Considerations

Digital or AC transient signals between AGND and DGND can create noise at the analog outputs. Tie AGND and DGND together at the DAC, then tie this point to the highest-quality ground available.

Good printed circuit board ground layout minimizes crosstalk between DAC outputs, reference inputs, and digital inputs. Reduce crosstalk by keeping analog lines away from digital lines. Wire-wrapped boards are not recommended.

Pin Configuration



9

+3V, Quad, 12-Bit Voltage-Output DAC with Serial Interface

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSBs)
MAX5253BC/D	0°C to +70°C	Dice*	±1
MAX5253AEPP	-40°C to +85°C	20 Plastic DIP	±1/2
MAX5253BEPP	-40°C to +85°C	20 Plastic DIP	±1
MAX5253AEAP	-40°C to +85°C	20 SSOP	±1/2
MAX5253BEAP	-40°C to +85°C	20 SSOP	±1
MAX5253BMJP	-55°C to +125°C	20 CERDIP**	±2

** Dice are specified at T_A = +25°C, DC parameters only.*
***Contact factory for availability and processing to MIL-STD-883.*

_____Chip Information

TRANSISTOR COUNT: 4337

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

11/96

MAXIM

+3.3V, Low-Power, 13-Bit Voltage-Output DAC with Serial Interface

General Description

The MAX5351 combines a low-power, voltage-output, 13-bit digital-to-analog converter (DAC) and a precision output amplifier in an 8-pin µMAX or DIP package. It operates from a single +3.3V supply and draws only 280µA of supply current.

The output amplifier's inverting input is available to the user, allowing specific gain configurations, remote sensing, and high output current capability. This makes the MAX5351 ideal for a wide range of applications, including industrial process control. Other features include a software shutdown and power-on reset.

The serial interface is compatible with either SPI™/QSPI™ or Microwire™. The DAC has a double-buffered input, organized as an input register followed by a DAC register. A 16-bit serial word loads data into the input register. The DAC register can be updated independently or simultaneously with the input register. All logic inputs are TTL/CMOS-logic compatible and buffered with Schmitt triggers to allow direct interfacing to optocouplers.

Applications

Industrial Process Controls

Automatic Test Equipment

Digital Offset and Gain Adjustment

Motion Control

Remote Industrial Controls

Microprocessor-Controlled Systems

Features

- ♦ **13-Bit DAC with Configurable Output Amplifier**
- ♦ **+3.3V Single-Supply Operation**
- ♦ **Low Supply Current: 0.28mA Normal Operation**
  4µA Shutdown Mode
- ♦ **Available in 8-Pin µMAX**
- ♦ **Power-On Reset Clears DAC Output to 0V**
- ♦ **SPI/QSPI and Microwire Compatible**
- ♦ **Schmitt-Trigger Digital Inputs for Direct Optocoupler Interface**

Ordering Information

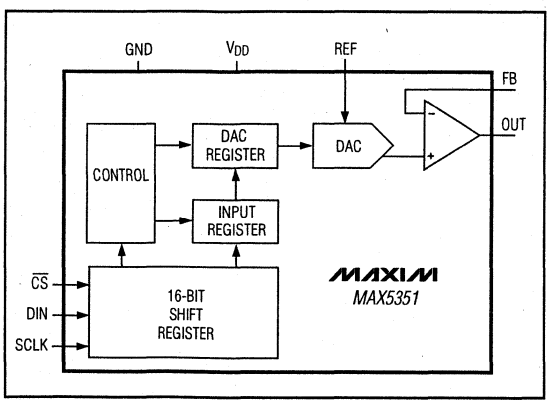
PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX5351ACPA	0°C to +70°C	8 Plastic DIP	±1
MAX5351BCPA	0°C to +70°C	8 Plastic DIP	±2
MAX5351ACUA	0°C to +70°C	8 µMAX†	±1
MAX5351BCUA	0°C to +70°C	8 µMAX	±2
MAX5351BC/D	0°C to +70°C	Dice*	±2
MAX5351AEPA	-40°C to +85°C	8 Plastic DIP	±1
MAX5351BEPA	-40°C to +85°C	8 Plastic DIP	±2
MAX5351AEUA	-40°C to +85°C	8 µMAX†	±1
MAX5351BEUA	-40°C to +85°C	8 µMAX	±2
MAX5351BMJA	-55°C to +125°C	8 CERDIP**	±4

†Contact factory for availability.

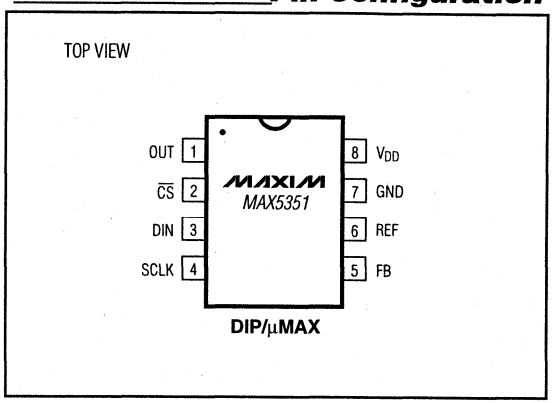
**Dice are tested at T_A = +25°C, DC parameters only.*

***Contact factory for availability and processing to MIL-STD-883.*

Functional Diagram



Pin Configuration



9

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ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

11/96

MAXIM

Low-Power, 12-Bit Voltage-Output DACs with Serial Interface

General Description

The MAX5352/MAX5353 combine a low-power, voltage-output, 12-bit digital-to-analog converter (DAC) and a precision output amplifier in an 8-pin µMAX or DIP package. The MAX5352 operates from a single +5V supply and the MAX5353 operates from a single +3.3V supply. Both devices draw only 280µA of supply current.

The output amplifier's inverting input is available to the user, allowing specific gain configurations, remote sensing, and high output current capability. This makes the MAX5352/MAX5353 ideal for a wide range of applications, including industrial process control. Other features include a software shutdown and power-on reset.

The serial interface is compatible with either SPI™/QSPI™ or Microwire™. The DAC has a double-buffered input, organized as an input register followed by a DAC register. A 16-bit serial word loads data into the input register. The DAC register can be updated independently or simultaneously with the input register. All logic inputs are TTL/CMOS-logic compatible and buffered with Schmitt triggers to allow direct interfacing to optocouplers.

Applications

Industrial Process Controls

Automatic Test Equipment

Digital Offset and Gain Adjustment

Motion Control

Remote Industrial Controls

Microprocessor-Controlled Systems

Features

- ♦ **12-Bit DAC with Configurable Output Amplifier**
- ♦ **+5V Single-Supply Operation (MAX5352)**
  +3.3V Single-Supply Operation (MAX5353)
- ♦ **Low Supply Current: 0.28mA Normal Operation**
  4µA Shutdown Mode
- ♦ **Available in 8-Pin µMAX**
- ♦ **Power-On Reset Clears DAC Output to 0V**
- ♦ **SPI/QSPI and Microwire Compatible**
- ♦ **Schmitt-Trigger Digital Inputs for Direct Optocoupler Interface**

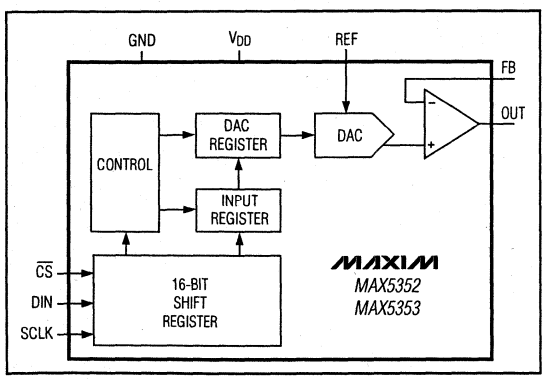
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX5352ACPA	0°C to +70°C	8 Plastic DIP	±1/2
MAX5352BCPA	0°C to +70°C	8 Plastic DIP	±1
MAX5352ACUA	0°C to +70°C	8 µMAX	±1/2
MAX5352BCUA	0°C to +70°C	8 µMAX	±1
MAX5352AEPA	-40°C to +85°C	8 Plastic DIP	±1/2
MAX5352BEPA	-40°C to +85°C	8 Plastic DIP	±1
MAX5352AEUA	-40°C to +85°C	8 µMAX	±1/2
MAX5352BEUA	-40°C to +85°C	8 µMAX	±1
MAX5352BMJA	-55°C to +125°C	8 CERDIP*	±2

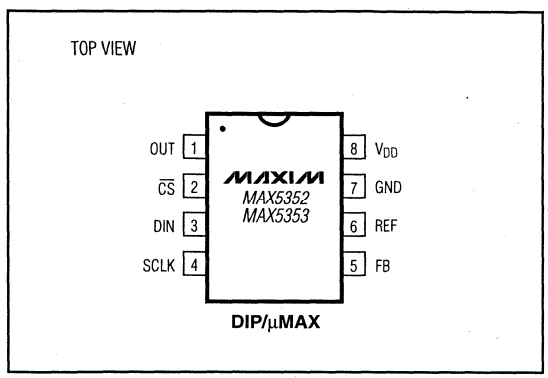
Ordering Information continued on next page.

**Contact factory for availability and processing to MIL-STD-883.*

Functional Diagram



Pin Configuration



DIP/µMAX

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Low-Power, 12-Bit Voltage-Output DACs with Serial Interface

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX5353ACPA	0°C to +70°C	8 Plastic DIP	±1
MAX5353BCPA	0°C to +70°C	8 Plastic DIP	±2
MAX5353ACUA	0°C to +70°C	8 µMAX	±1
MAX5353BCUA	0°C to +70°C	8 µMAX	±2
MAX5353AEPA	-40°C to +85°C	8 Plastic DIP	±1
MAX5353BEPA	-40°C to +85°C	8 Plastic DIP	±2
MAX5353AEUA	-40°C to +85°C	8 µMAX	±1
MAX5353BEUA	-40°C to +85°C	8 µMAX	±2
MAX5353BMJA	-55°C to +125°C	8 CERDIP*	±2

*Contact factory for availability and processing to MIL-STD-883.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

11/96

MAXIM

Low-Power, 10-Bit Voltage-Output DACs with Serial Interface

General Description

The MAX5354/MAX5355 combine a low-power, voltage-output, 10-bit digital-to-analog converter (DAC) and a precision output amplifier in an 8-pin µMAX or DIP package. The MAX5354 operates from a single +5V supply and the MAX5355 operates from a single +3.3V supply. Both devices draw only 280µA of supply current.

The output amplifier's inverting input is available to the user, allowing specific gain configurations, remote sensing, and high output current capability. This makes the MAX5354/MAX5355 ideal for a wide range of applications, including industrial process control. Other features include a software shutdown and power-on reset.

The serial interface is compatible with either SPI™/QSPI™ or Microwire™. The DAC has a double-buffered input, organized as an input register followed by a DAC register. A 16-bit serial word loads data into the input register. The DAC register can be updated independently or simultaneously with the input register. All logic inputs are TTL/CMOS-logic compatible and buffered with Schmitt triggers to allow direct interfacing to optocouplers.

Applications

Digital Offset and Gain Adjustment

Battery-Powered Test Instruments

Remote Industrial Controls

Microprocessor-Controlled Systems

Motion Control

Features

- **10-Bit DAC with Configurable Output Amplifier**
- **+5V Single-Supply Operation (MAX5354)**
  +3.3V Single-Supply Operation (MAX5355)
- **Low Supply Current: 0.28mA Normal Operation**
  4µA Shutdown Mode
- **Available in 8-Pin µMAX**
- **Power-On Reset Clears DAC Output to 0V**
- **SPI/QSPI and Microwire Compatible**
- **Schmitt-Trigger Digital Inputs for Direct Optocoupler Interface**
- **±1LSB (max) INL Over Temperature**

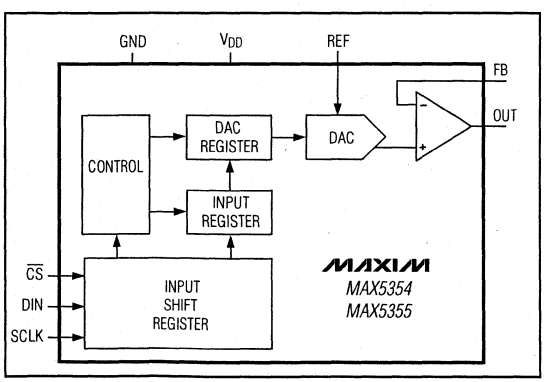
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX5354CPA	0°C to +70°C	8 Plastic DIP
MAX5354CUA	0°C to +70°C	8 µMAX
MAX5354EPA	-40°C to +85°C	8 Plastic DIP
MAX5354EUA	-40°C to +85°C	8 µMAX
MAX5354MJA	-55°C to +125°C	8 CERDIP*

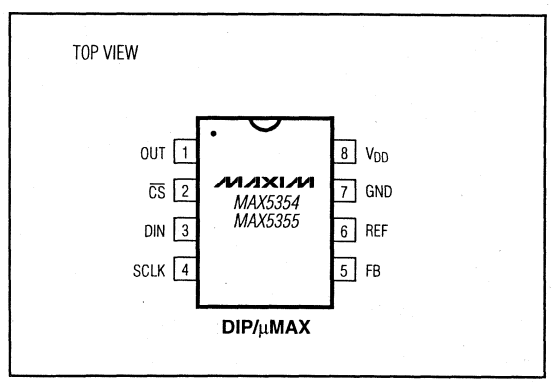
Ordering Information continued on next page.

**Contact factory for availability and processing to MIL-STD-883.*

Functional Diagram



Pin Configuration



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Low-Power, 12-Bit Voltage-Output DACs with Serial Interface

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX5355CPA	0°C to +70°C	8 Plastic DIP
MAX5355CUA	0°C to +70°C	8 µMAX
MAX5355EPA	-40°C to +85°C	8 Plastic DIP
MAX5355EUA	-40°C to +85°C	8 µMAX
MAX5355MJA	-55°C to +125°C	8 CERDIP*

**Contact factory for availability and processing to MIL-STD-883.*

Voltage Detectors

Voltage Detectors, Product Tables and Trees 10-2

MAX834 5-Pin, Micropower, Latching Voltage Monitor with Open-Drain Output 10-3*
MAX835 5-Pin, Micropower, Latching Voltage Monitor with Push/Pull Output 10-3*
MAX836 4-Pin, Micropower Voltage Monitor with Open-Drain Output 10-5
MAX837 4-Pin, Micropower Voltage Monitor with Push/Pull Output 10-5

*Advance Information–first page of data sheet in preparation.

Under/Overvoltage Detectors

Undervoltage

MAX8211 (noninverting)
★ MAX834
★ MAX835
★ MAX836
★ MAX837

Under/Overvoltage

ICL7665
ICL7665A/B

Overvoltage

MAX8212 (inverting)

Five Voltage

MAX8213A/B (adj., open-drain outputs)
MAX8214A/B (adj., active pull-up outputs)
MAX8215 (±5V, ±12V, adj.)
MAX8216 (±5V, ±15V, adj.)

★ New product

Under/Overvoltage Detectors

Part Number	Supply Voltage (V)	Supply Current (µA), max(typ)	Threshold Accuracy (%)	Package Options*	Temp. Ranges**	Description	Price† 1000-up ($)
MAX8211	+2 to +16.5	15(5)	±3.5	DIP, SO, TO8	C,E,M	Single channel: noninverting	1.33
MAX8212	+2 to +16.5	15(5)	±3.5	DIP, SO, TO8	C,E,M	Single channel: inverting	1.33
MAX8213A	+2.7 to +11	33(16)	±1	DIP, SO	C,E,M	5 voltage monitors, open-drain outputs	2.88
MAX8213B	+2.7 to +11	33(16)	±2	DIP, SO	C,E,M	5 voltage monitors, open-drain outputs	1.98
MAX8214A	+2.7 to +11	33(16)	±1	DIP, SO	C,E,M	5 voltage monitors, active pull-up outputs	2.88
MAX8214B	+2.7 to +11	33(16)	±2	DIP, SO	C,E,M	5 voltage monitors, active pull-up outputs	1.98
MAX8215	+2.7 to +11	250(137)	±1.25	DIP, SO	C,E,M	5 voltage monitors: ±5V, ±12V, adjustable	1.98
MAX8216	+2.7 to +11	250(137)	±1.25	DIP, SO	C,E,M	5 voltage monitors: ±5V, ±15V, adjustable	1.98
MAX834	+2.5 to +11	TBD	±1.25	SOT23-5	E	Latching voltage monitor, open-drain output	1.20
MAX835	+2.5 to +11	TBD	±1.25	SOT23-5	E	Latching voltage monitor, push-pull output	1.20
MAX836	+2.5 to +11	10(3.5)	±1.25	SOT143	E	Noninverting open-drain output	0.90
MAX837	+2.5 to +11	10(3.5)	±1.25	SOT143	E	Noninverting push-pull output	0.90
ICL7665A	+2 to +16	10(2.5)	±1.9	DIP, SO, TO8	C,E	Dual channel: one inverting, one noninverting	2.03

* Package Options: DIP = Dual-In-Line Package, SO = Small Outline, TO8 = Can
** Temp Ranges: C = 0°C to +70°C, E = -40°C to +85°C, M = -55°C to +125°C
† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

ADVANCE INFORMATION

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10/96

MAXIM

Micropower, Latching Voltage Monitors in SOT23-5

General Description

The MAX834/MAX835 micropower voltage monitors contain a 1.204V precision bandgap reference, comparator, and latched output in a 5-pin SOT23 package. Using the latched output prevents deep discharge of batteries. The MAX834 has an open-drain, N-channel output driver, while the MAX835 has a push/pull output driver. Two external resistors set the trip-threshold voltage.

Features

- ♦ **Prevents Deep Discharge of Batteries**
- ♦ **Precision ±1.25% Voltage Threshold**
- ♦ **Latched Output (once low, stays low until cleared)**
- ♦ **Small SOT23-5 Package**
- ♦ **Low Cost**
- ♦ **Wide Operating Voltage Range, +2.5V to +11V**
- ♦ **<2µA Typical Supply Current**
- ♦ **Open-Drain Output (MAX834) Push/Pull Output (MAX835)**

Applications

Precision Battery Monitor

Load Switching

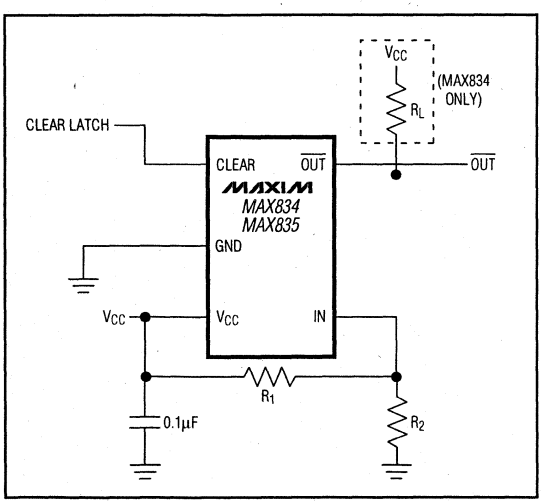
Battery-Powered Systems

Threshold Detectors

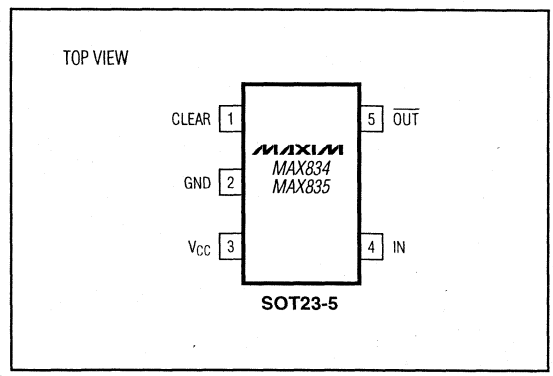
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	MARKING CODE
MAX834EUK-T	-40°C to +85°C	5 SOT23-5	AAAX
MAX835EUK-T	-40°C to +85°C	5 SOT23-5	AAAY

Typical Operating Circuit



Pin Configuration



10

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

19-1137; Rev 0; 9/96

MAXIM

4-Pin Micropower Voltage Monitors

General Description

The MAX836/MAX837 micropower voltage monitors contain a 1.204V precision bandgap reference and a comparator in a SOT143 package. The MAX836 has an open-drain, N-channel output driver, while the MAX837 has a push-pull output driver. Two external resistors set the trip threshold voltage.

Features

- ♦ **±1.25% Precision Voltage Threshold**
- ♦ **SOT143 Package**
- ♦ **Low Cost**
- ♦ **<5µA Typical Supply Current**
- ♦ **Open-Drain Output (MAX836)**
  Push-Pull Output (MAX837)

Applications

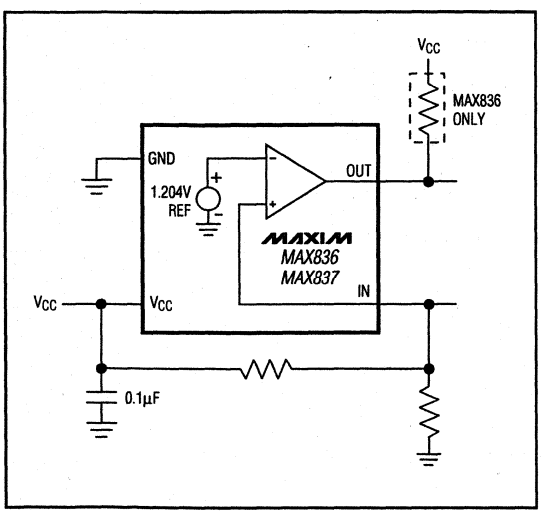
Precision Battery Monitor
Load Switching
Battery-Powered Systems
Threshold Detectors

Ordering Information

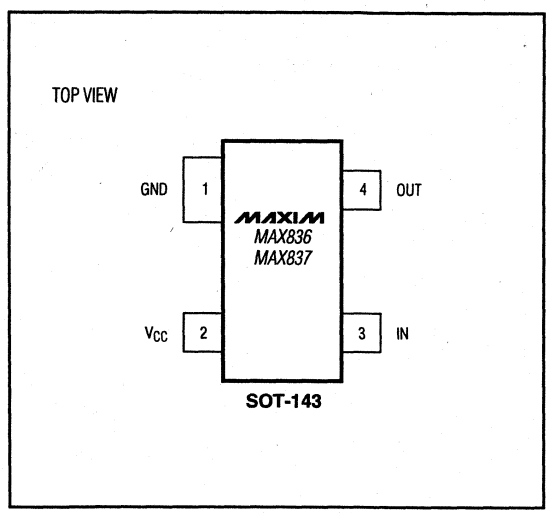
PART*	TEMP. RANGE	PIN-PACKAGE	MARKING CODE
MAX836EUS-T	-40°C to +85°C	4 SOT143	AAEQ
MAX837EUS-T	-40°C to +85°C	4 SOT143	AAER

**All devices available in tape-and-reel only. Contact factory for availability.*

Typical Operating Circuit



Pin Configuration



SOT-143

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

4-Pin Micropower Voltage Monitors

ABSOLUTE MAXIMUM RATINGS

V_{CC}, OUT to GND (MAX836) ..... -0.3V to 12V
IN, OUT to GND (MAX837) ..... -0.3V to (V_{CC} + 0.3V)
Input Current
  V_{CC} 20mA
  IN 10mA
Output Current, OUT 20mA
Rate of Rise, V_{CC} 100V/µs
Continuous Power Dissipation
  SOT143 (derate 4mW/°C above +70°C) 320mW
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.5V to +11.0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Operating Voltage Range (Note 1)	V_{CC}				2.5		11	V
Supply Current (Note 2)	I_{CC}	V_{IN} = 1.16V, OUT = low	V_{CC} = 3.6V	T_A = +25°C		3.5	6.5	µA
				T_A = T_{MIN} to T_{MAX}			10	
			V_{CC} = full operating range				15	
		V_{IN} = 1.25V, OUT = high	V_{CC} = 3.6V	T_A = +25°C		2.0	5.0	
				T_A = T_{MIN} to T_{MAX}			8.0	
			V_{CC} = full operating range				13	
Trip Threshold Voltage	V_{TH}	V_{IN} falling	T_A = +25°C		1.185	1.204	1.215	V
			T_A = 0°C to +70°C		1.169	1.204	1.231	
Trip Threshold Voltage Hysteresis	V_{HYST}	V_{CC} = 5V, IN = low to high				6		mV
IN Operating Voltage Range (Note 1)	V_{IN}						V_{CC} - 1	V
IN Leakage Current (Note 3)	I_{IN}	V_{IN} = V_{TH}				±3	±12	nA
Propagation Delay	t_{PL}	V_{CC} = 5.0V, 50mV overdrive				80		µs
Glitch Immunity		V_{CC} = 5.0V, 100mV overdrive				35		µs
OUT Rise Time	t_{RT}	V_{CC} = 5.0V, no load (MAX837 only)				260		ns
OUT Fall Time	t_{FT}	V_{CC} = 5.0V, no load (MAX836 pull-up = 10kΩ)				680		ns
Output Leakage Current (Note 4)	I_{LOUT}	V_{IN} > V_{THMAX} (MAX836 only)					±1	µA
Output Voltage High	V_{OH}	V_{IN} > V_{THMAX}, I_{SOURCE} = 500µA (MAX837 only)			V_{CC} - 0.5			V
Output Voltage Low	V_{OL}	V_{IN} < V_{THMIN}, I_{SINK} = 500µA					0.4	V

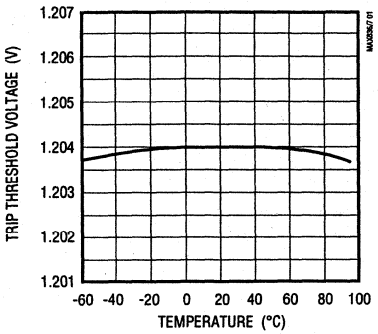
Note 1: The voltage-detector output remains in the direct state for V_{CC} down to 1.2V when $V_{IN} \leq V_{CC} / 2$.
Note 2: Supply current has a monotonic dependence on V_{CC} (see *Typical Operating Characteristics*).
Note 3: IN leakage current has a monotonic dependence on V_{CC} (see *Typical Operating Characteristics*).
Note 4: The MAX836 open-drain output can be pulled up to a voltage greater than V_{CC}, but may not exceed 11V.

4-Pin Micropower Voltage Monitors

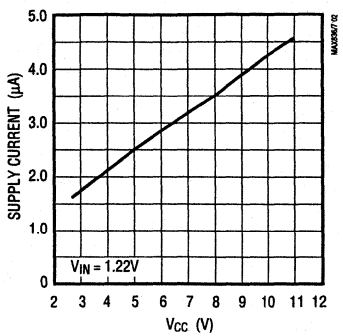
Typical Operating Characteristics

(V_{CC} = +5V, R_{LOAD} = 1MΩ, $R_{PULL-UP}$ = 10kΩ (MAX836 only), T_A = +25°C, unless otherwise noted.)

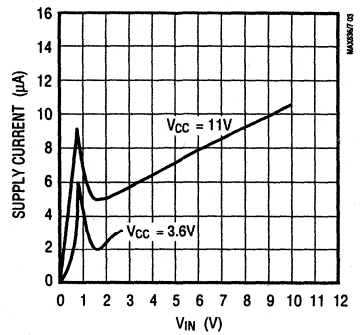
TRIP THRESHOLD VOLTAGE vs. TEMPERATURE



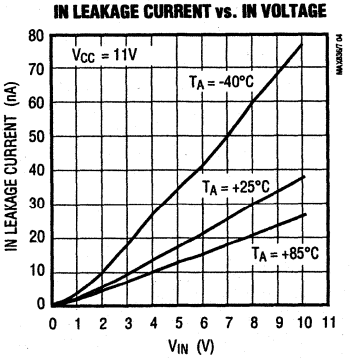
SUPPLY CURRENT vs. SUPPLY VOLTAGE



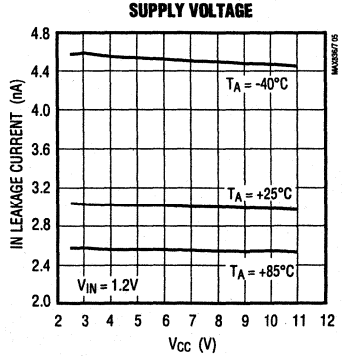
SUPPLY CURRENT vs. IN VOLTAGE



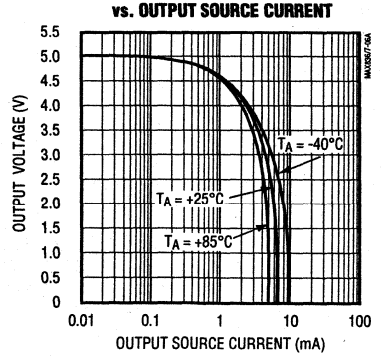
IN LEAKAGE CURRENT vs. IN VOLTAGE



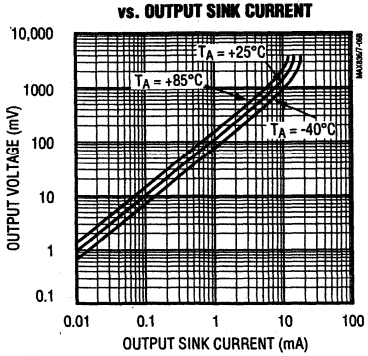
IN LEAKAGE CURRENT vs. SUPPLY VOLTAGE



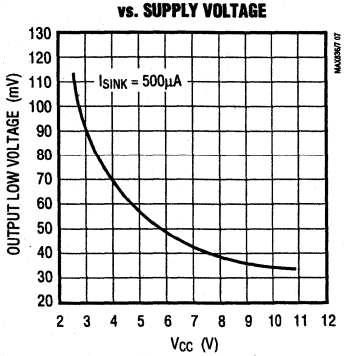
MAX837 OUTPUT VOLTAGE vs. OUTPUT SOURCE CURRENT



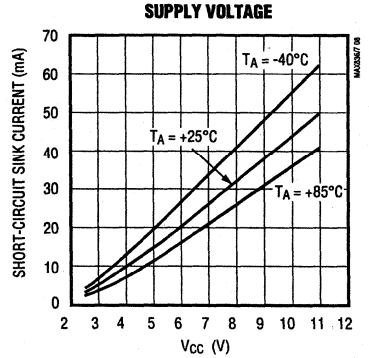
OUTPUT VOLTAGE vs. OUTPUT SINK CURRENT



OUTPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



SHORT-CIRCUIT SINK CURRENT vs. SUPPLY VOLTAGE



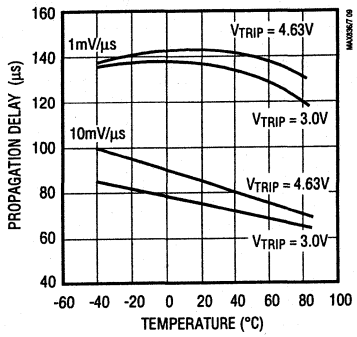
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4-Pin Micropower Voltage Monitors

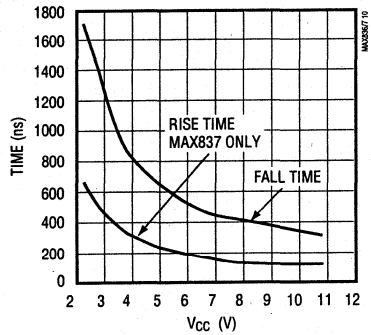
Typical Operating Characteristics (continued)

(V_{CC} = +5V, R_{LOAD} = 1MΩ, $R_{PULL-UP}$ = 10kΩ (MAX836 only), T_A = +25°C, unless otherwise noted.)

VCC FALLING PROPAGATION DELAY vs. TEMPERATURE



OUT RISE/FALL TIME vs. SUPPLY VOLTAGE



Pin Description

PIN	NAME	FUNCTION
1	GND	System Ground
2	VCC	System Supply Input
3	IN	Noninverting Input to the Comparator. The inverting input connects to the internal 1.204V bandgap reference.
4	OUT	Open-Drain (MAX836) or Push-Pull (MAX837) Output

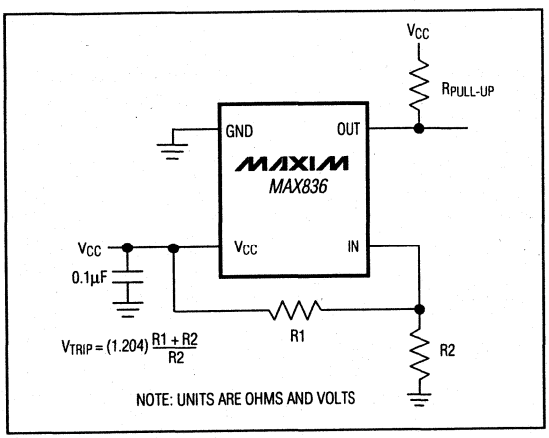


Figure 1. Programming the Trip Voltage, V_{TRIP}

Detailed Description

The MAX836/MAX837 micropower voltage monitors contain a 1.204V precision bandgap reference and a comparator (see the *Typical Operating Circuit*). The only difference between the two parts is the structure of the comparator output driver. The MAX836 has an open-drain N-channel output driver that can be pulled up to a voltage higher than V_{CC}, but under 11V. The MAX837's output is push-pull, and can both source and sink current.

Programming the Trip Voltage

Two external resistors set the trip voltage, V_{TRIP} (Figure 1). V_{TRIP} is the point at which the applied voltage (typically V_{CC}) toggles OUT. The MAX836/MAX837's high input impedance allows large-value resistors without compromising trip-voltage accuracy. To minimize current consumption, select a value for R2 between 500kΩ and 1MΩ, then calculate R1 as follows:

$$R1 = R2\left(\frac{V_{TRIP}}{V_{TH}} - 1\right)$$

where V_{TRIP} = desired trip voltage (in volts), V_{TH} = threshold trip voltage (1.204V).

Applications Information

Adding Hysteresis

Hysteresis adds noise immunity to the MAX836/MAX837 and prevents repeated triggering when V_{IN} is near the threshold trip voltage. Figure 2 shows how to add hysteresis to the comparator. The technique is similar for

both parts. For the MAX836, select the ratio of resistors R1 and R2 so that IN sees 1.204V when the monitor voltage falls to or rises above the desired trip point (V_{TRIP}). R3 adds hysteresis and is typically an order of magnitude larger than R1 or R2. The current through R1 and R2 should be at least 500nA to ensure that the 12nA maximum input current does not shift the trip point significantly. Capacitor C1 adds additional noise rejection.

Monitoring Voltages Other than Vcc

The MAX836/MAX837 can monitor voltages other than V_{CC} (Figure 3). Calculate V_{TRIP} as shown in the section *Programming the Trip Voltage*. The monitored voltage (V_{MON}) is independent of V_{CC}. V_{IN} must be 1V less than V_{CC}.

Heater Temperature Control

Figure 4 shows a basic heater temperature-control circuit. Upon power-up, OUT is high and the N-channel MOSFET turns on. Current flows through the heating element (R4), warming the surrounding area. R2 is a negative-temperature-coefficient thermistor and as temperature increases, its resistance decreases. As the thermistor heats up and its resistance decreases, the MAX837's voltage at IN decreases until it reaches the 1.204V threshold voltage. At this point, OUT goes low, turning off the heating element. The thermistor cools and the voltage at IN rises until it overcomes the MAX837's hysteresis (6mV). OUT returns high when this point is reached, turning on the heating element again. This cycle repeats as long as power is applied.

Determine the thermistor's resistance (R2) at the desired temperature. Then, using R2's resistance and half the resistance of R3, calculate R1's value with the following formula:

$$R1 = (R2 + R3)\left(\frac{V_{CC}}{1.204} - 1\right)$$

Chip Information

TRANSISTOR COUNT: 54

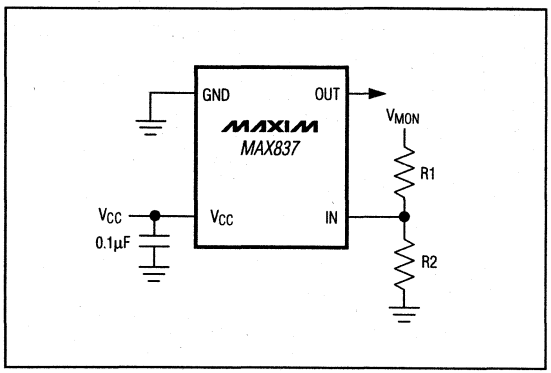


Figure 3. Monitoring Voltages Other than V_{CC}

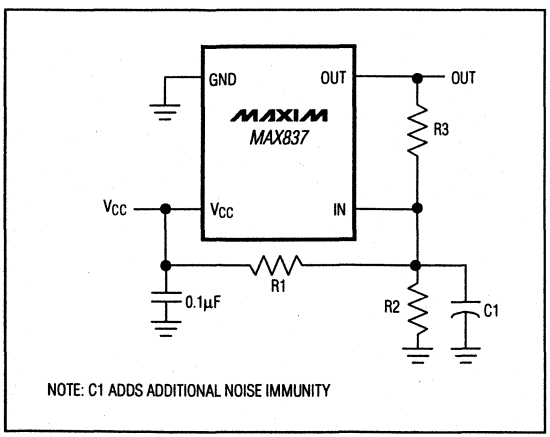


Figure 2. Adding Hysteresis to the Comparator

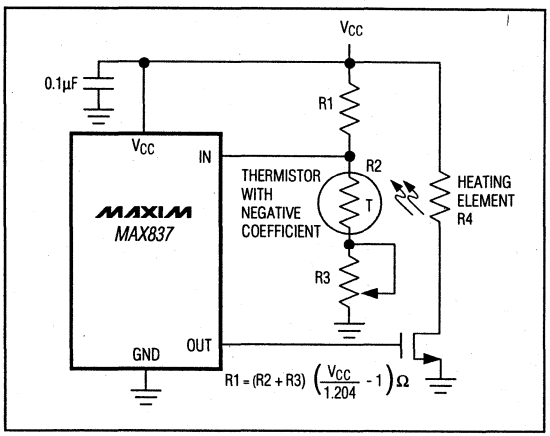
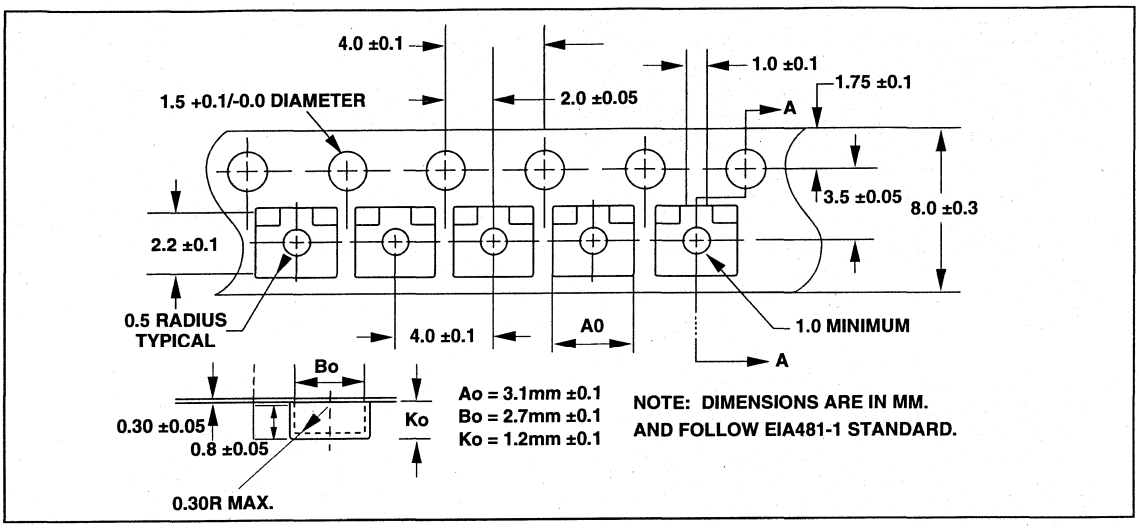


Figure 4. Heater Temperature Control

4-Pin Micropower Voltage Monitors

Tape-and-Reel Information

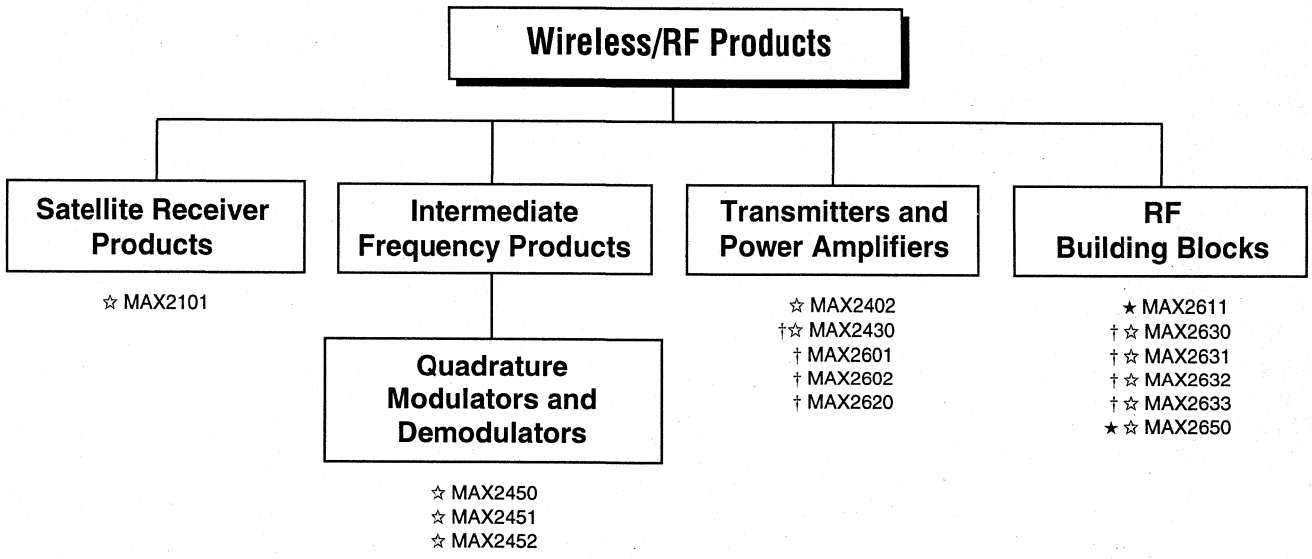


Wireless/RF Products

Wireless/RF Products, Product Table 11-2

MAX2430	900MHz, 100mW Power Amplifier/Predriver	11-5
MAX2450	70MHz Quadrature Modulator/Demodulator	11-13
MAX2451	70MHz Quadrature Demodulator	11-21
MAX2452	70MHz Quadrature Modulator	11-27
MAX2601	3V, 1W RF Power Transistor	11-33*
MAX2602	3V, 1W RF Power Transistor with On-Chip Diode	11-33*
MAX2611	DC-to-Microwave, Low-Noise Amplifier	11-35
MAX2620	650MHz to 1050MHz Integrated Oscillator with Buffered Outputs	11-41*
MAX2630	VHF-to-Microwave, 3V, Low-Noise Amplifier	11-43*
MAX2631	VHF-to-Microwave, 3V, Low-Noise Amplifier with Shutdown	11-43*
MAX2632	VHF-to-Microwave, 3V, Low-Noise Amplifier with Bias Control	11-43*
MAX2633	VHF-to-Microwave, 3V, Low-Noise Amplifier with Shutdown and Bias Control	11-43*
MAX2650	5V, 1GHz, Low-Noise Amplifier	11-45

*Advance Information–first page of data sheet in preparation.



★ New product
† Future product
☆ Evaluation kit available

Part Number	Supply Voltage (V)	IF Frequency (MHz)	IF Bandwidth (MHz)	I/Q Gain Balance (dB)	I/Q Phase Balance (degrees)	AGC Range (dB)	Pins-Package Options*	Features	Applications	Price† 25,000-up ($)
SATELLITE RECEIVER PRODUCTS										
MAX2101	4.75 to 5.25	400 to 700	60	0.5	1.5	40	100-MQFP	I/Q demodulator with dual 5th-order Butterworth filters, 10MHz to 30MHz bandwidth, and dual 6-bit ADCs	DBS, VSAT	11.49

Part Number	Supply Voltage (V)	Supply Current (mA)	IF Frequency (MHz)	IF Bandwidth (MHz)	I/Q Gain Balance (dB)	I/Q Phase Balance (degrees)	Pins-Package Options*	Features	Applications	Price† 1000-up ($)
MODULATORS AND DEMODULATORS										
MAX2450	2.7 to 3.3	5.9	70	9	0.45	3	20-SO, 20-QSOP	70MHz I/Q modulator/demodulator with on-chip VCO and quad generator, shutdown mode	Cellular, ISM, WLANs	3.99
MAX2451	2.7 to 3.3	5.5	70	9	0.45	3	16-SO	70MHz I/Q demodulator with on-chip VCO and quad generator, shutdown mode	Cellular, ISM, WLANs	3.23
MAX2452	2.7 to 3.3	4.1	70	15	0.45	3	16-SO	70MHz I/Q modulator with on-chip VCO and quad generator, shutdown mode	Cellular, ISM, WLANs	3.23

Part Number	Supply Voltage (V)	Frequency Range (MHz)	Output Power (mW)	Power Control (dB)	Class	Pins-Package Options*	Features	Applications	Price† 1000-up ($)
TRANSMITTERS AND POWER AMPLIFIERS									
MAX2402	4.75 to 5.5	800 to 1000	100	40	AB to B, adj.	20-SSOP	Power amplifier with balanced modulator, linear modulation to 2V, shutdown mode	ISM spread spectrum, DS, FH, BPSK, ASK, FSK	3.78
MAX2430	3 to 5.5	800 to 1000	100 @ 3V	15	AB	16-SO	Power amplifier with 100mW at 3V, power on/off ramp control, more than 32dB gain, shutdown mode	900MHz cordless phones, ISM spread spectrum	††
MAX2601	2.7 to 5.5	DC to >1000	1W	—	AB/C	8-SO	3.6V, 1W power transistor in a thermally enhanced plastic package	AMPS phones, two-way paging, CDPD, ISM radios	††
MAX2602	2.7 to 5.5	DC to >1000	1W	—	AB/C	8-SO	3.6V, 1W power transistor with an on-chip thermally matched bias diode	AMPS phones, two-way paging, CDPD, ISM radios	††

* Package Options: MQDP = Modular Quad Flat Pack, SO = Small Outline, SSOP = Shrink Small-Outline Package

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

†† Future product—contact factory for pricing and availability. Specifications are preliminary.

Part Number	Supply Voltage (V)	Frequency Range (MHz)	Gain (dB) @ I_C (mA)	P1 (dBm)	Noise Figure (dB)	Pins-Package Options*	Features	Applications	Price† 1000-up ($)
GENERAL-PURPOSE RF PRODUCTS									
MAX2611	4.5 to 6.5	DC to 1100	18.5 @ 16	3	3.5	SOT143	Wideband gain block, low noise and high output capability	Satellite receivers, TV, tuners, wireless LANs, ISM radios	0.90
MAX2620	2.7 to 5.5	650 to 1050	N/A	-2	N/A	8-µMAX	Voltage-controlled oscillator with low phase noise, shutdown, and two buffered outputs	Cellular phones, ISM radios, paging receivers	††
MAX2630	2.7 to 5.5	100 to 1000	13.7 @ 7	-11	3.7	SOT143	3V LNA with internal biasing	Portable phones, wireless LANs, ISM radios	††
MAX2631	2.7 to 5.5	100 to 1000	13.7 @ 7	-11	3.7	SOT23-5	3V LNA with shutdown. No external bias resistor.	Cordless phones, wireless LANs, ISM radios	††
MAX2632	2.7 to 5.5	100 to 1000	13.7 @ 7	-11	3.7	SOT23-5	3V LNA with bias control	Cordless phones, wireless LANs, ISM radios	††
MAX2633	2.7 to 5.5	100 to 1000	13.7 @ 7	-11	3.7	SOT23-6	3V LNA with shutdown and bias control	Cordless phones, wireless LANs, ISM radios	††
MAX2650	4.5 to 5.5	DC to 1000	19 @ 18	0	3.6	SOT143	5V low-noise amp with internal biasing	Satellite receivers, TV, tuners, wireless LANs, ISM radios	0.80

* Package Options: MQDP = Modular Quad Flat Pack, SO = Small Outline, SSOP = Shrink Small-Outline Package

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

†† Future product—contact factory for pricing and availability. Specifications are preliminary.

19-1093; Rev 0; 7/96

MAXIM

Low-Voltage, Silicon RF Power Amplifier/Predriver

General Description

The MAX2430 is a versatile, silicon RF power amplifier that operates directly from a 3V to 5.5V supply, making it suitable for 3-cell NiCd or 1-cell lithium-ion battery applications. It is designed for use in the 800MHz to 1000MHz frequency range and, at 915MHz, can produce +21dBm (125mW) of output power with greater than 32dB of gain at V_{CC} = 3.6V.

A unique shutdown function provides an off supply current of typically less than 1µA to save power during "idle slots" in time-division multiple-access (TDMA) transmissions. An external capacitor sets the RF output power envelope ramp time. External power control is also possible over a 15dB range. The amplifier's input is matched on-chip to 50Ω. The output is an open collector that is easily matched to a 50Ω load with few external components.

The MAX2430 is ideal as a driver amplifier for portable and mobile telephone systems, or as a complete power amplifier for other low-cost applications, such as those in the 915MHz spread-spectrum ISM band. It is fabricated with Maxim's high-frequency bipolar transistor process, and comes in a thermally enhanced, 16-pin narrow SO package.

Applications

Digital Cordless Phones
915MHz ISM-Band Applications
Two-Way Pagers
Wireless LANs
Cellular Phones
AM and FM Analog Transmitters

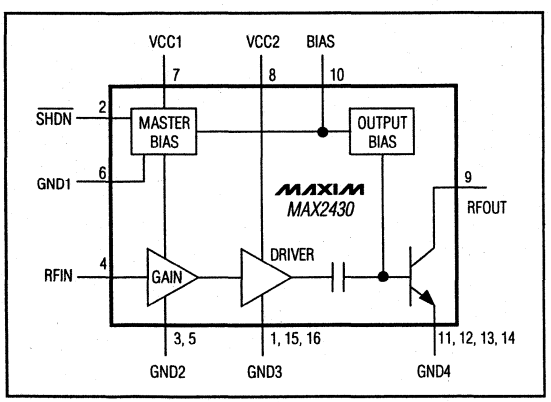
Features

- **Operates Over the 800MHz to 1000MHz Frequency Range**
- **Delivers 125mW at 915MHz from 3.6V Supply (100mW typical from 3.0V supply)**
- **Operates Directly from 3-Cell NiCd or 1-Cell Lithium-Ion Battery**
- **Over 32dB Power Gain**
- **RF Power Envelope Ramping is Programmable with One External Capacitor**
- **Input Matched to 50Ω (VSWR < 2:1)**
- **15dB Output Power Control Range**
- **1µA Typical Shutdown Current**

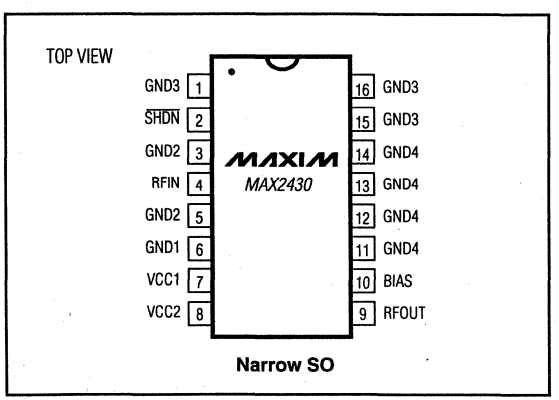
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX2430ISE	-20°C to +85°C	16 Narrow SO

Functional Diagram



Pin Configuration



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Low-Voltage, Silicon RF Power Amplifier/Predriver

ABSOLUTE MAXIMUM RATINGS

VCC1, VCC2 ..... 6V
$\overline{SHDN}$, BIAS ..... -0.3V, (V_{CC} + 0.3V)
RFIN ..... -0.3V, 2V
P_{RFIN} ..... -3dBm

Continuous Power Dissipation (T_A = +70°C)
SO (derate 20mW/°C above +70°C) 1.6W
Operating Temperature Range ..... -20°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = VCC1 = VCC2 = RFOUT = 3V to 5.5V, GND1 = GND2 = GND3 = GND4 = 0V, $\overline{SHDN}$ = 2.2V, BIAS = open, RFIN = open, T_A = -20°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{CC}		3		5.5	V
Supply Current	I_{CC}	No RF input applied, V_{CC} = 5.5V		52	70	mA
Shutdown Supply Current	$I_{CC(OFF)}$	$\overline{SHDN}$ = low		1	10	µA
BIAS Pin Voltage	V_{BIAS}	BIAS pin open		2.2		V
$\overline{SHDN}$ High Input	$V_{SHDN(HI)}$		2.2		V_{CC}	V
$\overline{SHDN}$ Low Input	$V_{SHDN(LO)}$				0.4	V
$\overline{SHDN}$ Bias Current	I_{SHDN}	$\overline{SHDN}$ = V_{CC}			18	µA

AC ELECTRICAL CHARACTERISTICS

(MAX2430 evaluation kit, f = 915MHz, V_{CC} = 3.6V, $\overline{SHDN}$ = V_{CC}, RFOUT matched to 50Ω resistive load, output measurements taken after matching network, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Range		(Note 2)	800		1000	MHz
P_{OUT} at 1dB Compression	P_{1dB}	V_{CC} = 3.6V	20	21.4		dBm
		V_{CC} = 3.0V	19	20.4		
Power Gain	G_P	P_{RFIN} = -20dBm	32	34		dB
Output IM3	OIM3	f1 = 915MHz, f2 = 916MHz, P_{OUT} per tone = 14dBm		-30		dBc
2nd Harmonic		P_{OUT} = P_{1dB}		-26		dBc
3rd Harmonic		P_{OUT} = P_{1dB}		-40		dBc
Efficiency	η	P_{OUT} = P_{1dB}		24		%
Supply Current	I_{CCRF}	P_{OUT} = P_{1dB}		160		mA
Maximum Input VSWR	$VSWR_{IN}$	RFIN connected to 50Ω source		2:1		
Maximum Output Load Mismatch	$VSWR_{OUT}$	V_{CC} = 3V to 5.5V, P_{RFIN} ≤ -10dBm (Note 3)		8:1		
Maximum Output Load Mismatch for Stability	$VSWR_{OUT}$	V_{CC} = 3V to 5.5V, P_{RFIN} ≤ -12dBm (Note 4)		6:1		
Noise Figure	NF			7		dB

AC ELECTRICAL CHARACTERISTICS

(MAX2430 evaluation kit, f = 915MHz, V_{CC} = 3.6V, $\overline{SHDN}$ = V_{CC}, output matched to 50Ω resistive load, output measurements taken after matching network, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RFIN to RFOUT Isolation		$\overline{SHDN}$ = 0.4V, P_{IN} = -10dBm		50		dB
Turn-On/Off Times		BIAS pin capacitor C1 = 120pF		1		µs
		BIAS pin capacitor C1 = 2.2nF		10		

Note 1: Minimum and maximum parameters are guaranteed by design.

Note 2: For optimum performance at a given frequency, output matching network must be designed for maximum output power. See *Applications Information* section. Operation outside this frequency range is possible but has not been characterized.

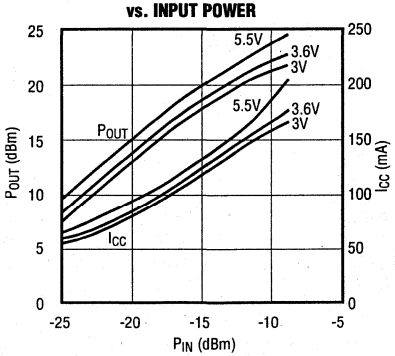
Note 3: No damage to the device.

Note 4: All non-harmonically related outputs are more than 60dB below the desired signal for any electrical phase.

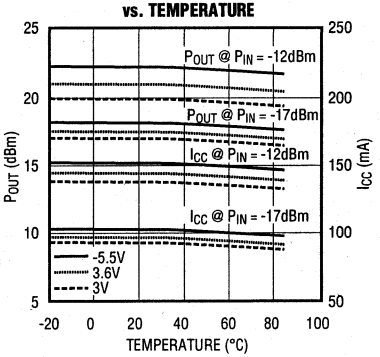
Typical Operating Characteristics

(MAX2430 evaluation kit, f = 915MHz, V_{CC} = 3.6V, $\overline{SHDN}$ = V_{CC}, output matched to 50Ω resistive load, output measurements taken after matching network, T_A = +25°C, unless otherwise noted.)

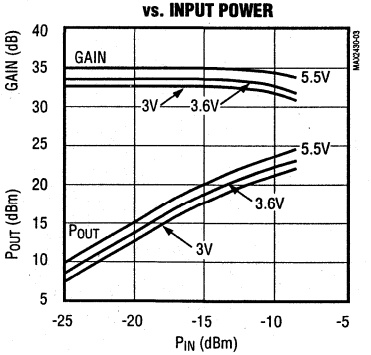
OUTPUT POWER AND CURRENT vs. INPUT POWER



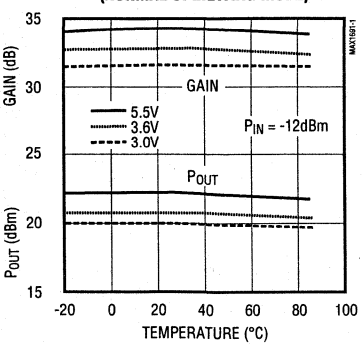
OUTPUT POWER AND CURRENT vs. TEMPERATURE



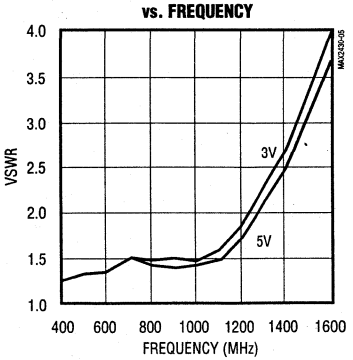
OUTPUT POWER AND GAIN vs. INPUT POWER



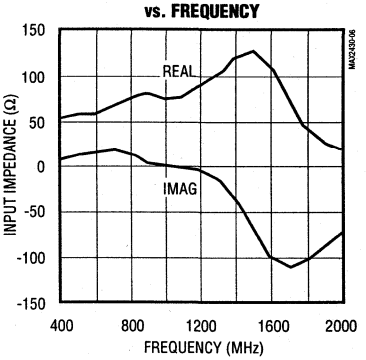
vs. TEMPERATURE (NORMAL OPERATING MODE)



INPUT VSWR vs. FREQUENCY



RFIN INPUT IMPEDANCE vs. FREQUENCY

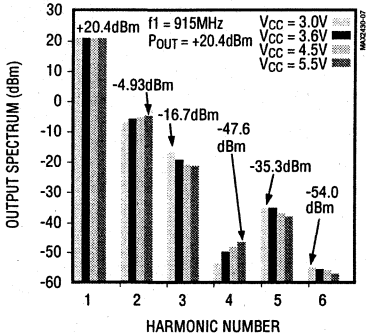


Low-Voltage, Silicon RF Power Amplifier/Predriver

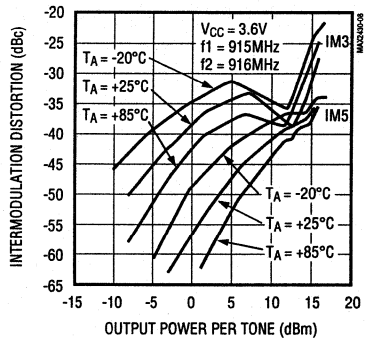
Typical Operating Characteristics (continued)

(MAX2430 evaluation kit, f = 915MHz, V_{CC} = 3.6V, $\overline{SHDN}$ = V_{CC}, output matched to 50Ω resistive load, output measurements taken after matching network, T_A = +25°C, unless otherwise noted.)

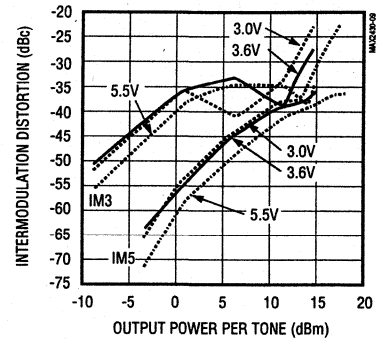
OUTPUT POWER AND HARMONICS



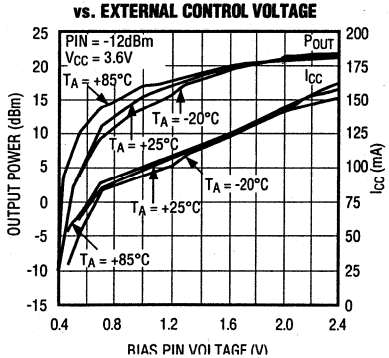
INTERMODULATION DISTORTION vs. OUTPUT POWER AND TEMPERATURE



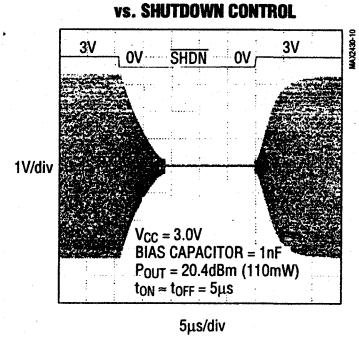
INTERMODULATION DISTORTION vs. OUTPUT POWER AND V_{CC}



OUTPUT POWER AND SUPPLY CURRENT vs. EXTERNAL CONTROL VOLTAGE



RF OUTPUT ENVELOPE CHARACTERISTICS vs. SHUTDOWN CONTROL



Low-Voltage, Silicon RF Power Amplifier/Predriver

Pin Description

PIN	NAME	FUNCTION
1, 15, 16	GND3	Driver Stage Ground. Connect directly to ground plane.
2	$\overline{SHDN}$	Shutdown Input (TTL/CMOS)
3, 5	GND2	Input Stage Ground. Connect directly to ground plane.
4	RFIN	RF Input. Internally matched to 50Ω. Requires series DC-blocking capacitor.
6	GND1	Bias Circuitry Ground. Connect directly to ground plane.
7	VCC1	Bias Circuitry Supply. Connect to supply. Bypass with 1000pF capacitor.
8	VCC2	Driver Stage Output. Connect to supply through inductor (see *Applications Information*).
9	RFOUT	Output Transistor. Open Collector.
10	BIAS	Output Stage Bias Pin. Connect capacitor to GND to control start-up power envelope. Drive directly for power control (see *Applications Information*).
11–14	GND4	Output Stage Ground. Connect directly to ground plane.

Detailed Description

The MAX2430 consists of a large power output transistor driven by a capacitively coupled driver stage (see *Functional Diagram*). The driver and front-end gain stages are DC connected and biased on-chip from the master bias cell. The master bias cell also controls the output stage bias circuit. The input impedance at the RFIN pin is internally matched to 50Ω, while the output stage must be tuned and filtered externally for any narrow-band frequency range of interest between 800MHz and 1000MHz.

The driver amplifier requires an external inductor at the VCC2 pin to provide DC bias and proper matching to the output stage. This inductor's value depends on the frequency range of operation and will vary between 5nH and 22nH.

The output transistor at the RFOUT pin requires an external RF choke inductor connected to the supply for DC bias, and a matching network to transform the desired external load impedance to the optimal internal load impedance of approximately 15Ω.

The MAX2430 includes a unique shutdown feature. The TTL/CMOS-compatible $\overline{SHDN}$ input allows the device to be shut down completely without the use of any external components. Also, the RF output power envelope ramp time can be programmed with a single external capacitor connected between the BIAS pin and ground. Pulling the shutdown pin ($\overline{SHDN}$) high powers on the master bias circuit, which in turn charges the external capacitor tied to the BIAS pin using a controlled current. The voltage at BIAS controls the output power level, which ramps until the BIAS pin is internally clamped to approximately 2.2V. The envelope rampdown time is controlled in a similar manner when the $\overline{SHDN}$ pin is pulled low.

Variable output power control over a 15dB range is also possible by forcing the voltage on the BIAS pin externally from 0.6V to 2.4V.

During the on state ($\overline{SHDN}$ = high), the power-supply bias current is typically 52mA with no RF applied to the input. During the off state ($\overline{SHDN}$ = low), the supply current is typically reduced to less than 1µA.

Low-Voltage, Silicon RF Power Amplifier/Predriver

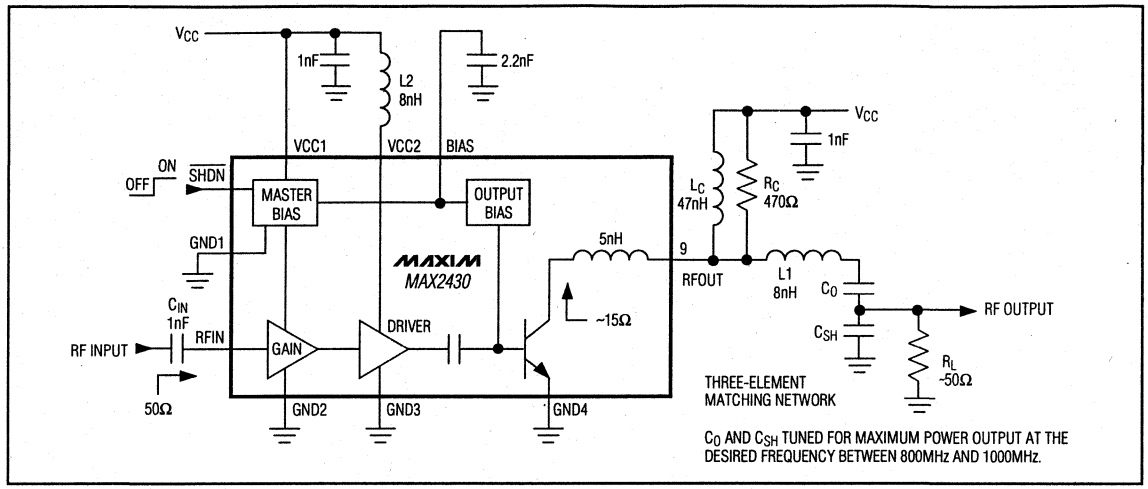


Figure 1. Typical Application Circuit

Applications Information

Output Matching

The optimum internal load impedance seen by RFOUT is approximately 15Ω. This on-chip low drive impedance provides maximum power transfer and best efficiency under low (3V) supply conditions where the voltage-swing headroom is limited. For example, driving an output power of 21.3dBm (135mW) into 50Ω translates to a 7.35Vp-p swing at the output. An RF amplifier would require at least a 4.5V supply to drive a 50Ω load directly. However, driving 21.3dBm into 15Ω translates to 4.02Vp-p. The MAX2430 can achieve a voltage swing of 4.02Vp-p or 2.01Vp from a 3V supply voltage without saturating the output transistor.

Figure 1 shows the MAX2430 configured for 800MHz to 1000MHz operation. The output matching circuitry converts the desired 50Ω load impedance to the 15Ω optimal load seen by the output transistor's collector. This configuration uses a low-loss, controlled-Q inductor network. Starting from the RFOUT pin, this network consists of a series L (which includes the 5nH package parasitic inductance), series C, and shunt C. The design equations for this network are as follows:

R1 = Output resistance as seen by the collector ~15Ω

R_L = Desired load resistance

The controlled-Q inductor network requires that $R_L > R1$ and $Q > \sqrt{(R_L / R1 - 1)}$. Choose Q and compute matching components as given below:

$$A = \sqrt{(R_L \times R1 - R1^2)}$$

$$X_L = Q \times R1$$

$$X_{Co} = X_L - A$$

$$X_{Csh} = R_L \times R1 / A$$

$L1 = X_L / \omega$ - 5nH of package inductance

$$C_O = \frac{1}{\omega X_{Co}}$$

$$C_{SH} = \frac{1}{\omega X_{Csh}}$$

where ω equals the center frequency in radians/second.

Recommended starting values for L1 and L2 are given in Table 1.

Table 1. Recommended L1 and L2 Starting Values

f = ω / 2π (MHz)	L1(nH)	L2(nH)
400 to 600*	22	12
600 to 800*	15	8
800 to 1000	8	8

*not characterized

An overall loaded Q ≤ 5 can be achieved with readily available surface-mount components. This network absorbs the parasitic elements of the surface-mount components in such a way that they do not negatively impact the stopband characteristics; in fact, they can improve the overall stopband attenuation with properly chosen components. High-Q components (Q > 100) that have self-resonance near the 3rd harmonic of the intended output frequency should provide good passband characteristics with low loss, while offering good attenuation of the undesired 2nd and 3rd harmonics that are generated. Note that most applications will require extra filtering components and good shielding after the matching network, to ensure absolute attenuation of out-of-band signals in order to meet out-of-band spurious suppression requirements.

Output Mismatch Considerations

The MAX2430 will typically withstand an output load mismatch of VSWR = 6:1 at any electrical phase without exhibiting oscillatory behavior over the entire supply voltage range of 3V to 5.5V. Resistor R_C enhances stability under load mismatch conditions and does not affect normal operation of the circuit.

BIAS Pin

The voltage at the BIAS pin controls the output power transistor biasing. At BIAS = 0.6V, the output transistor is biased to Class C, resulting in low gain and relatively nonlinear power. Above 2V, the output stage is biased to Class AB. Note that changing the bias voltage may degrade the output transistor's stability.

The shutdown pin ($\overline{SHDN}$) controls the master bias circuit, which in turn provides a control current of approximately ±500µA to the external capacitor connected to the BIAS pin. When $\overline{SHDN}$ transitions from low to high, the BIAS pin capacitor charges up and clamps at approximately 2.2V. When $\overline{SHDN}$ transitions from high to low, the BIAS pin capacitor is discharged to nearly ground. This results in a power-up/power-down ramping of the RF envelope, which can be approximated by the following equation:

$$t_{ramp} \cong C_{BIAS} \times 2.2V / 0.5mA = 4400\Omega \times C_{BIAS}$$

Therefore, a 2.2nF capacitor will give approximately 10µs ramp time.

The BIAS pin can also be used to control the final output power and gain over a 15dB range, by forcing the BIAS pin voltage externally between 0.6V and 2.4V. Note that the BIAS pin driver must be able to source/sink 700µA. Forcing the BIAS pin directly in this manner disrupts the RF envelope timing function. To avoid this, place a diode in series with the BIAS pin control circuit, as shown in Figure 2.

Note that when using the BIAS pin for power control, linearity is much degraded at the lower power levels.

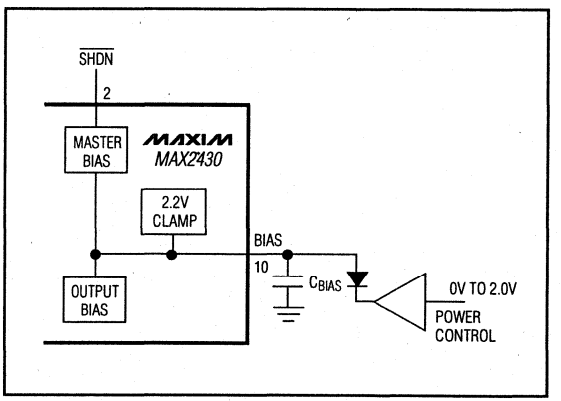


Figure 2. Power-Control Application Using BIAS Pin

19-0455; Rev 0; 12/95

EVALUATION KIT AVAILABLE

3V, Ultra-Low-Power Quadrature Modulator/Demodulator

General Description

The MAX2450 combines a quadrature modulator and quadrature demodulator with a supporting oscillator and divide-by-8 prescaler on a monolithic IC. It operates from a single +3V supply and draws only 5.9mA. The demodulator accepts an amplified and filtered IF signal in the 35MHz to 80MHz range, and demodulates it into I and Q baseband signals with 51dB of voltage conversion gain. The IF input is terminated with a 400Ω thin-film resistor for matching to an external IF filter. The baseband outputs are fully differential and have 1.2Vp-p signal swings. The modulator accepts differential I and Q baseband signals with amplitudes up to 1.35Vp-p and bandwidths to 15MHz, and produces a differential IF signal in the 35MHz to 80MHz range.

Pulling the CMOS-compatible ENABLE pin low shuts down the MAX2450 and reduces the supply current to less than 1µA. To minimize spurious feedback, the MAX2450's internal oscillator is set at twice the IF via external tuning components. The oscillator and associated phase shifters produce differential signals exhibiting low amplitude and phase imbalance, yielding modulator sideband rejection of 38dB. The MAX2450 comes in 20-pin SO and QSOP packages.

Applications

Digital Cordless Phones

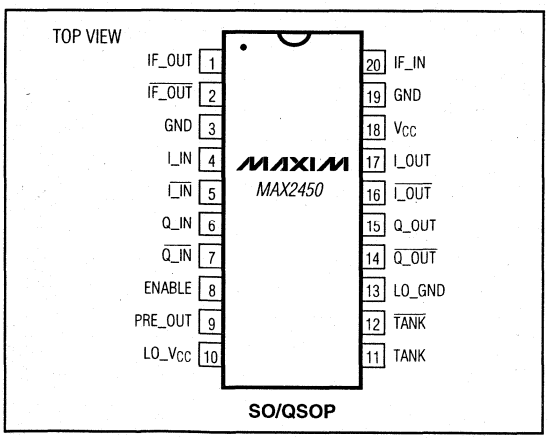
GSM and North American Cellular Phones

Wireless LANs

Digital Communications

Two-Way Pagers

Pin Configuration



SO/QSOP

Features

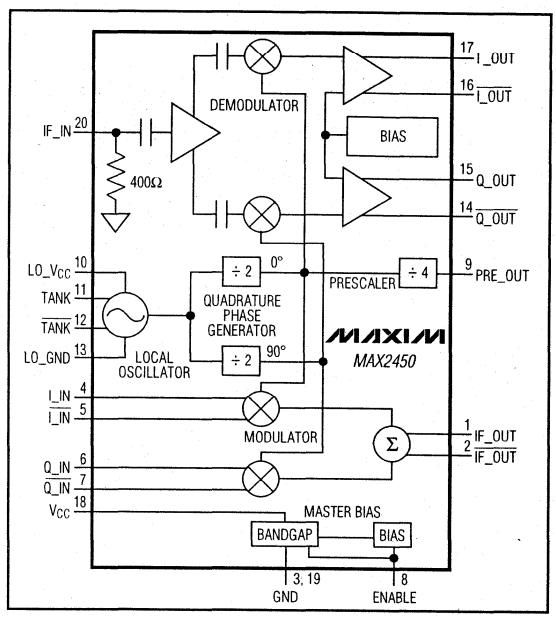
- ♦ Combines Quadrature Modulator and Demodulator
- ♦ Integrated Quadrature Phase Shifters
- ♦ On-Chip Oscillator (Requires External Tuning Circuit)
- ♦ On-Chip Divide-by-8 Prescaler
- ♦ Modulator Input Bandwidth Up to 15MHz
- ♦ Demodulator Output Bandwidth Up to 9MHz
- ♦ 51dB Demodulator Voltage Conversion Gain
- ♦ CMOS-Compatible Enable
- ♦ 5.9mA Operating Supply Current
  1µA Shutdown Supply Current

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX2450CWP	0°C to +70°C	20 Wide SO
MAX2450CEP	0°C to +70°C	20 QSOP*

** Contact factory for availability.*

Functional Diagram



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

3V, Ultra-Low-Power Quadrature Modulator/Demodulator

ABSOLUTE MAXIMUM RATINGS

V_{CC}, LO_V_{CC} to GND .....-0.3V to +4.5V
ENABLE, TANK, $\overline{TANK}$, I_IN, $\overline{I_IN}$, Q_IN, $\overline{Q_IN}$ to GND .....-0.3V to (V_{CC} + 0.3V)
IF_IN to GND .....-0.3V to +1.5V

Continuous Power Dissipation (T_A = +70°C)
Wide SO (derate 10.00mW/°C above +70°C).....800mW
QSOP (derate 9.1mW/°C above +70°C).....727mW
Operating Temperature Range.....0°C to +70°C
Storage Temperature Range .....-65°C to +165°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = LO_V_{CC} = $\overline{TANK}$ = 2.7V to 3.3V, ENABLE = V_{CC} - 0.4, GND = LO_GND = 0V, I_IN = $\overline{I_IN}$ = Q_IN = $\overline{Q_IN}$ = IF_IN = TANK = OPEN, T_A = 0°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{CC}, LO_V_{CC}		2.7		3.3	V
Supply Current	$I_{CC(ON)}$			5.9	8.2	mA
Shutdown Supply Current	$I_{CC(OFF)}$	ENABLE = 0.4V		2	20	µA
Enable/Disable Time	$t_{ON/OFF}$			10		µs
ENABLE Bias Current	I_{EN}	ENABLE = V_{CC}		1	3	µA
ENABLE High Voltage	V_{ENH}		V_{CC} - 0.4			V
ENABLE Low Voltage	V_{ENL}				0.4	V
I_IN, $\overline{I_IN}$, Q_IN, $\overline{Q_IN}$ Self-Bias DC Voltage Level	$V_{I_IN/\overline{I_IN}}$, $V_{Q_IN/\overline{Q_IN}}$		1.25	1.5	1.75	V
Modulator Differential Input Impedance	$Z_{I_IN/\overline{I_IN}}$, $Z_{Q_IN/\overline{Q_IN}}$		35	44		kΩ
IF_OUT, $\overline{IF_OUT}$ DC Bias Voltage	$V_{IF_OUT/\overline{IF_OUT}}$			V_{CC} - 1.5		V
Demodulator IF Input Impedance	Z_{IF_IN}		320	400	480	Ω
Demodulator I and Q Baseband DC Offset				±11	±50	mV
I_OUT, $\overline{I_OUT}$, Q_OUT, $\overline{Q_OUT}$ DC Bias Voltage Level	$V_{I_OUT/\overline{I_OUT}}$, $V_{Q_OUT/\overline{Q_OUT}}$			1.2		V

AC ELECTRICAL CHARACTERISTICS

(MAX2450 EV kit using MAX2450CWP, V_{CC} = LO_V_{CC} = ENABLE = 3.0V, f_{LO} = 140MHz, $f_{I_IN/\overline{I_IN}}$ = $f_{Q_IN/\overline{Q_IN}}$ = 600kHz, $V_{I_IN/\overline{I_IN}}$ = $V_{Q_IN/\overline{Q_IN}}$ = 1.2V_{p-p}, f_{IF_IN} = 70.1MHz, V_{IF_IN} = 2.82mV_{p-p}, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DEMODULATOR						
I and Q Amplitude Balance				< ±0.45		dB
I and Q Phase Accuracy				< ±1.3		degrees
Voltage Conversion Gain				51		dB
Allowable I and Q Voltage Swing		(Note 1)			1.35	V_{p-p}
Noise Figure	NF			18		dB
I and Q IM3 Level	$IM3_{I/Q}$	(Note 2)		-44		dBc
I and Q IM5 Level	$IM5_{I/Q}$	(Note 2)		-60		dBc
I and Q Signal 3dB Bandwidth	BW_{DEMOD}			9		MHz
Oscillator Frequency Range	f_{LO}	(Notes 1, 3)	70		160	MHz
LO Phase Noise		10kHz offset		-80		dBc/Hz
PRE_OUT Output Voltage	V_{PRE_OUT}	R_L = 10kΩ, C_L < 6pF		0.35		V_{p-p}
PRE_OUT Slew Rate	SR_{PRE_OUT}	R_L = 10kΩ, C_L < 6pF, rising edge		60		V/µs

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2450 EV kit using MAX2450CWP, V_{CC} = LO_V_{CC} = ENABLE = 3.0V, f_{LO} = 140MHz, $f_{I_IN/\overline{I_IN}}$ = $f_{Q_IN/\overline{Q_IN}}$ = 600kHz, $V_{I_IN/\overline{I_IN}}$ = $V_{Q_IN/\overline{Q_IN}}$ = 1.2V_{p-p}, f_{IF_IN} = 70.1MHz, V_{IF_IN} = 2.82mV_{p-p}, T_A = +25°C, unless otherwise noted.)

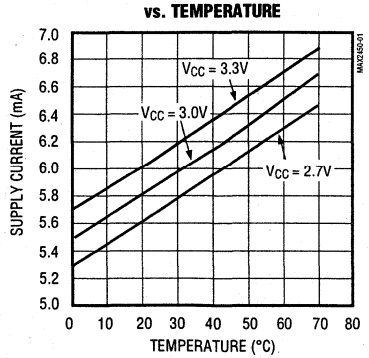
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MODULATOR						
Allowable Differential Input Voltage	$V_{I_IN/\overline{I_IN}}$, $V_{Q_IN/\overline{Q_IN}}$	(Note 1)			1.35	V_{p-p}
Input Common-Mode Voltage Range			1.25		1.75	V
I and Q Signal 3dB Bandwidth	BW_{MOD}			15		MHz
IF Differential Output Voltage	$V_{IF_OUT/\overline{IF_OUT}}$	$V_{I_IN/\overline{I_IN}}$ = $V_{Q_IN/\overline{Q_IN}}$ = 1.2Vp-p, R_L = 200kΩ differential, C_L < 5pF differential		65		mV_{p-p}
IF Output IM3 Level	$IM3_{IF}$	$V_{I_IN/\overline{I_IN}}$ = 1.35Vp-p composite (Note 4)		-60		dBc
IF Output IM5 Level	$IM5_{IF}$	$V_{I_IN/\overline{I_IN}}$ = 1.35Vp-p composite (Note 4)		-60		dBc
Sideband Rejection				38		dBc
Carrier Suppression at Modulator Output				-36		dBc

Note 1: Guaranteed by design, not tested.
Note 2: f_{IF_IN} = 2 tones at 70.10MHz and 70.11MHz. V_{IF_IN} = 1.41mVp-p per tone.
Note 3: The frequency range can be extended in either direction, but has not been characterized. At higher frequencies, the modulator IF output amplitude may decrease and distortions may increase.
Note 4: Q_IN/$\overline{Q_IN}$ ports are terminated. $f_{I_IN/\overline{I_IN}}$ = 2 tones at 550kHz and 600kHz.

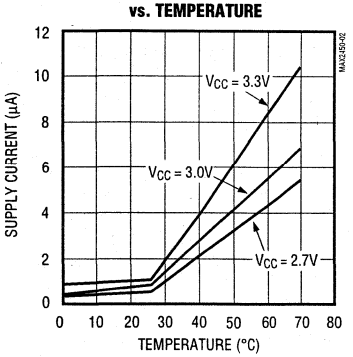
Typical Operating Characteristics

(MAX2450 EV Kit using MAX2450CWP, V_{CC} = LO_V_{CC} = ENABLE = 3.0V, f_{LO} = 140MHz, $f_{I_IN/\overline{I_IN}}$ = $f_{Q_IN/\overline{Q_IN}}$ = 600kHz, $V_{I_IN/\overline{I_IN}}$ = $V_{Q_IN/\overline{Q_IN}}$ = 1.2V_{p-p}, f_{IF_IN} = 70.1MHz, V_{IF_IN} = 2.82mV_{p-p}, T_A = +25°C, unless otherwise noted.)

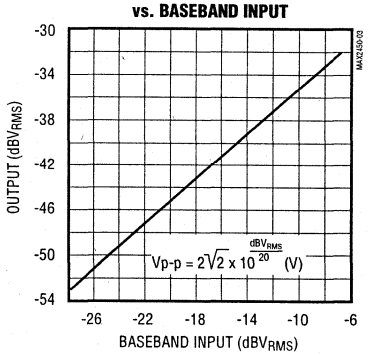
SUPPLY CURRENT vs. TEMPERATURE



SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



MODULATOR IF OUTPUT vs. BASEBAND INPUT

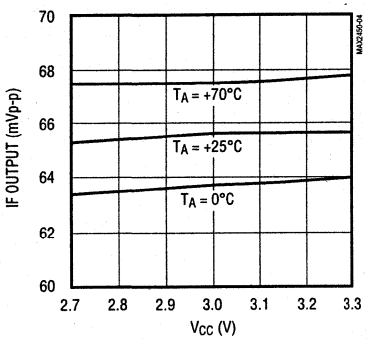


3V, Ultra-Low-Power Quadrature Modulator/Demodulator

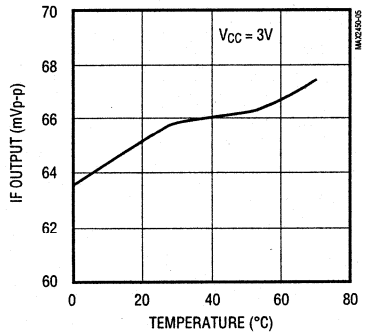
Typical Operating Characteristics (continued)

(MAX2450 EV Kit using MAX2450CWP, V_{CC} = LO_V_{CC} = ENABLE = 3.0V, f_{LO} = 140MHz, $f_{I_IN/\overline{I_IN}}$ = $f_{Q_IN/\overline{Q_IN}}$ = 600kHz, $V_{I_IN/\overline{I_IN}}$ = $V_{Q_IN/\overline{Q_IN}}$ = 1.2V_{p-p}, f_{IF_IN} = 70.1MHz, V_{IF_IN} = 2.82mV_{p-p}, T_A = +25°C, unless otherwise noted.)

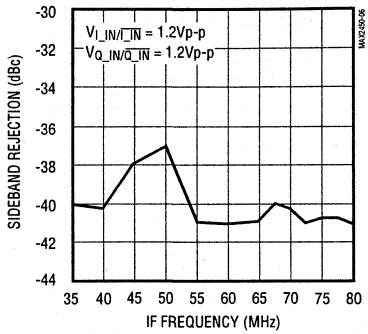
MODULATOR IF OUTPUT vs. SUPPLY VOLTAGE



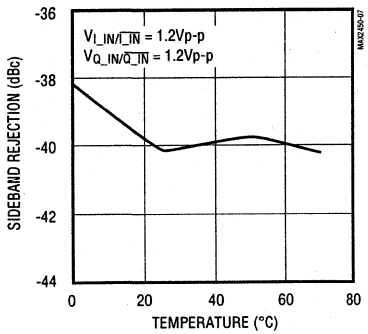
MODULATOR IF OUTPUT vs.TEMPERATURE



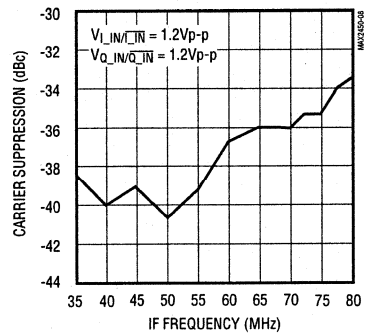
MODULATOR SIDEBAND REJECTION vs. IF FREQUENCY



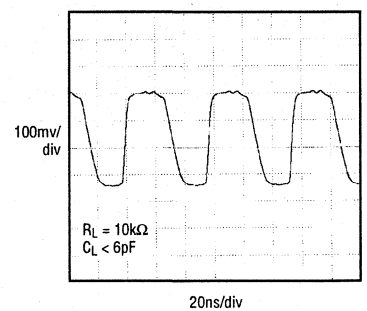
MODULATOR SIDEBAND REJECTION vs. TEMPERATURE



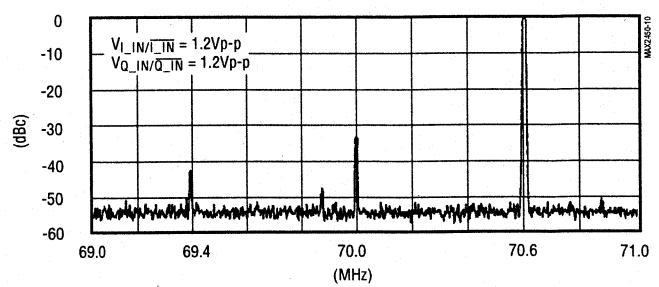
CARRIER SUPPRESSION vs. IF FREQUENCY



PRE_OUT WAVEFORM



MODULATOR OUTPUT SPECTRUM

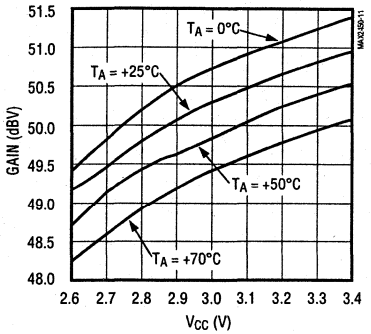


3V, Ultra-Low-Power Quadrature Modulator/Demodulator

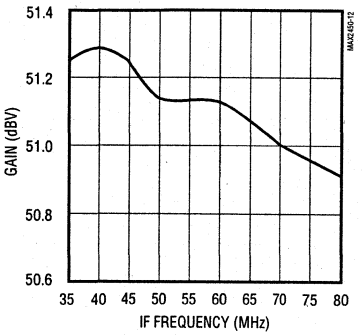
Typical Operating Characteristics (continued)

(MAX2450 EV Kit using MAX2450CWP, V_{CC} = LO_V_{CC} = ENABLE = 3.0V, f_{LO} = 140MHz, $f_{I_IN/\overline{I_IN}}$ = $f_{Q_IN/\overline{Q_IN}}$ = 600kHz, $V_{I_IN/\overline{I_IN}}$ = $V_{Q_IN/\overline{Q_IN}}$ = 1.2V_{p-p}, f_{IF_IN} = 70.1MHz, V_{IF_IN} = 2.82mV_{p-p}, T_A = +25°C, unless otherwise noted.)

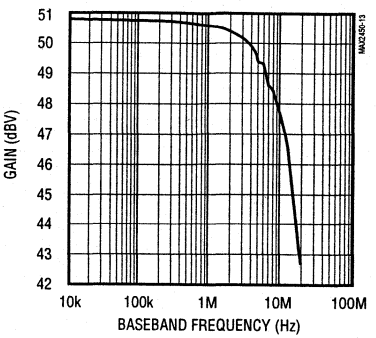
DEMODULATOR VOLTAGE CONVERSION GAIN vs. TEMPERATURE AND SUPPLY



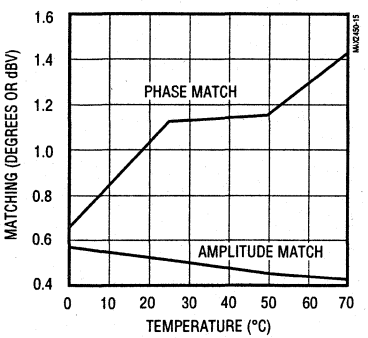
DEMODULATOR VOLTAGE CONVERSION GAIN vs. IF FREQUENCY



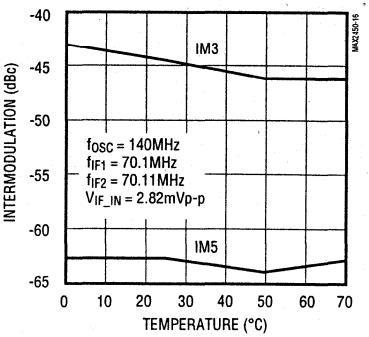
DEMODULATOR VOLTAGE CONVERSION GAIN vs. BASEBAND FREQUENCY



DEMODULATOR I/Q PHASE AND AMPLITUDE MISMATCH vs. TEMPERATURE



DEMODULATOR INTERMOD POWER vs. TEMPERATURE



3V, Ultra-Low-Power Quadrature Modulator/Demodulator

Pin Description

PIN	NAME	FUNCTION
1	IF_OUT	Modulator IF Output
2	$\overline{\text{IF_OUT}}$	Modulator IF Inverting Output
3, 19	GND	Ground
4	I_IN	Baseband Inphase Input
5	$\overline{\text{I_IN}}$	Baseband Inphase Inverting Input
6	Q_IN	Baseband Quadrature Input
7	$\overline{\text{Q_IN}}$	Baseband Quadrature Inverting Input
8	ENABLE	Enable Control, active high
9	PRE_OUT	Local-Oscillator, Divide-by-8, Prescaled Output
10	LO_VCC	Local-Oscillator Supply. Bypass separately from VCC.
11	TANK	Local-Oscillator Resonant Tank Input (Figure 4)
12	$\overline{\text{TANK}}$	Local-Oscillator Resonant Tank Inverting Input (Figure 4)
13	LO_GND	Local-Oscillator Ground
14	$\overline{\text{Q_OUT}}$	Demodulator Quadrature Inverting Output
15	Q_OUT	Demodulator Quadrature Output
16	$\overline{\text{I_OUT}}$	Demodulator Inphase Inverting Output
17	I_OUT	Demodulator Inphase Output
18	VCC	Modulator and Demodulator Supply
20	IF_IN	Demodulator IF Input

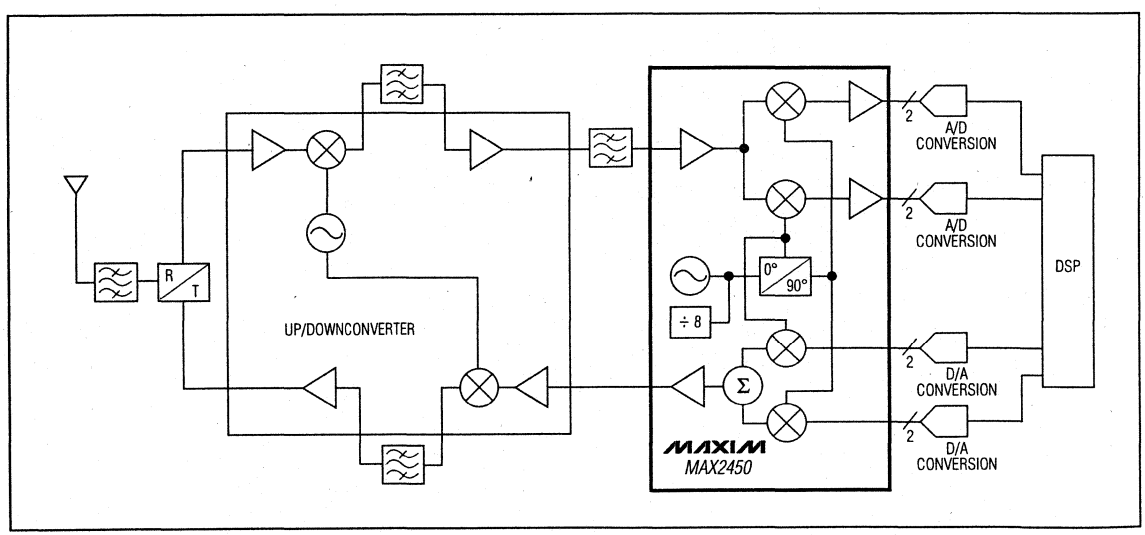


Figure 1. Typical Application Block Diagram

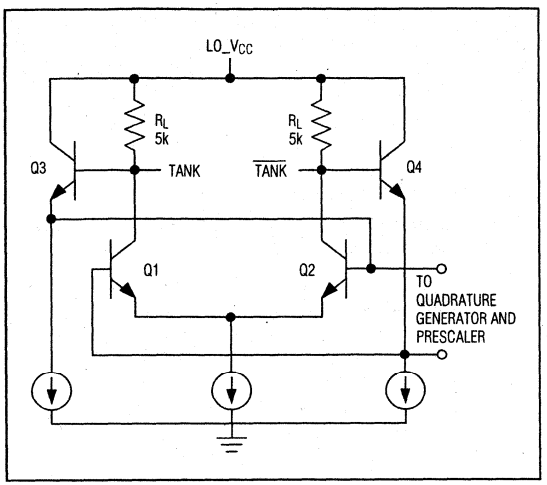


Figure 2. Local-Oscillator Equivalent Circuit

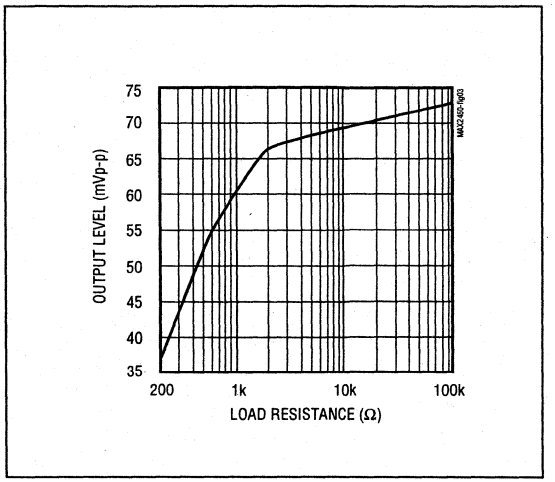


Figure 3. Modulator Output Level vs. Load Resistance

Detailed Description

The following sections describe each of the functional blocks shown in the *Functional Diagram*. They also refer to the Typical Application Block Diagram (Figure 1).

Demodulator

The demodulator contains a single-ended-to-differential converter, two Gilbert-cell multipliers, and two fixed gain stages. The IF signal should be AC coupled into IF_IN. Internally, IF_IN is terminated with a 400Ω resistor to GND and provides a gain of 14dB. This amplified IF signal is fed into the I and Q mixers for demodulation. The multipliers mix the IF signal with the quadrature LO signals, resulting in baseband I and Q signals. The conversion gain of the multipliers is 15dB. These signals are further amplified by 21dB by the baseband amplifiers. The baseband I and Q amplifier chains are DC coupled.

Local Oscillator

The local-oscillator section is formed by an emitter-coupled differential pair. Figure 2 shows the equivalent local-oscillator circuit schematic. An external LC resonant tank determines the oscillation frequency, and the Q of this resonant tank affects the oscillator phase noise. The oscillation frequency is twice the IF frequency, so that the quadrature phase generator can use two latches to generate precise quadrature signals.

The oscillator may be overdriven by an external source. The source should be AC coupled into TANK/$\overline{\text{TANK}}$, and should provide 200mVp-p levels. A choke (typically 2.2µH) is required between TANK and $\overline{\text{TANK}}$. Differential input impedance at TANK/$\overline{\text{TANK}}$ is 10kΩ. For single-ended drive, connect an AC bypass capacitor (1000pF) from $\overline{\text{TANK}}$ to GND, and AC couple TANK to the source.

Quadrature Phase Generator

The quadrature phase generator uses two latches to divide the local-oscillator frequency by two, and generates two precise quadrature signals. Internal limiting amplifiers shape the signals to approximate square waves to drive the Gilbert-cell mixers. The inphase signal (at half the local-oscillator frequency) is further divided by four for the prescaler output.

Prescaler

The prescaler output, PRE_OUT, is buffered and swings typically $0.35V_{p-p}$ with a 10kΩ and 6pF load. It can be AC-coupled to the input of a frequency synthesizer.

Modulator

The modulator accepts I and Q differential baseband signals up to $1.35V_{p-p}$ with frequencies up to 15MHz, and upconverts them to the IF frequency. Since these inputs are biased internally at around 1.5V, I and Q signals should be capacitively coupled into these high-impedance ports (the differential input impedance is approximately 44kΩ). The self-bias design yields very low on-chip offset, resulting in excellent carrier sup-

3V, Ultra-Low-Power Quadrature Modulator/Demodulator

pression. Alternatively, a differential DAC may be connected without AC coupling, as long as a common-mode voltage range of 1.25V to 1.75V is maintained. For single-ended drive, connect I_IN and Q_IN via AC-coupling capacitors (0.1µF) to GND.

The IF output is designed to drive a high impedance (> 20kΩ), such as an IF buffer or an upconverter mixer. IF_OUT/IF_OUT must be AC coupled to the load. Impedances as low as 200Ω can be driven with a decrease in output amplitude (Figure 3). To drive a single-ended load, AC couple and terminate IF_OUT with a resistive load equal to the load at IF_OUT.

Master Bias

During normal operation, ENABLE should remain above V_{CC} - 0.4V. Pulling the ENABLE input low shuts off the master bias and reduces the circuit current to less than 2µA. The master bias section includes a bandgap reference generator and a PTAT (Proportional To Absolute Temperature) current generator.

Applications Information

Figure 4 shows the implementation of a resonant tank circuit. The inductor, two capacitors, and a dual varactor form the oscillator's resonant circuit. In Figure 4, the oscillator frequency ranges from 130MHz to 160MHz.

To ensure reliable start-up, the inductor is directly connected across the local oscillator's tank ports. The two 33pF capacitors affect the Q of the resonant circuit. Other values may be chosen to meet individual application requirements. Use the following formula to determine the oscillation frequency:

$$f_O = \frac{1}{2\pi\sqrt{L_{EQ}C_{EQ}}}$$

where

$$C_{EQ} = \frac{1}{\frac{1}{C1}+\frac{1}{C2}+\frac{2}{C_{VAR}}} + C_{STRAY}$$

and

$$L_{EQ} = L + L_{STRAY}$$

where C_{STRAY} = parasitic capacitance and L_{STRAY} = parasitic inductance.

To alter the oscillation frequency range, change the inductance, the capacitance, or both. For best phase-noise performance keep the Q of the resonant tank as high as possible:

$$Q = R_{EQ}\sqrt{\frac{C_{EQ}}{L_{EQ}}}$$

where $R_{EQ} \approx 10k\Omega$ (Figure 2).

The oscillation frequency can be changed by altering the control voltage, V_{CTRL}.

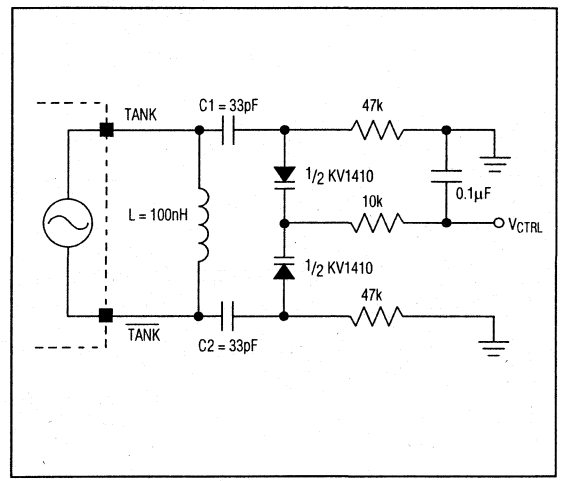


Figure 4. Typical Resonant Tank Circuit

19-0493; Rev 0; 12/95

EVALUATION KIT AVAILABLE

MAXIM

3V, Ultra-Low-Power Quadrature Demodulator

General Description

The monolithic MAX2451 is a quadrature demodulator with a supporting oscillator and divide-by-8 prescaler. It operates from a single +3V supply and draws only 5.5mA. The demodulator accepts an amplified and filtered IF signal in the 35MHz to 80MHz range, and demodulates it into I and Q baseband signals with 51dB of voltage conversion gain. The IF input is terminated with a 400Ω thin-film resistor for matching to an external IF filter. The baseband outputs are fully differential and have 1.2Vp-p signal swings.

Pulling the CMOS-compatible ENABLE pin low shuts down the MAX2451 and reduces the supply current to less than 2µA, typical. To minimize spurious feedback, the MAX2451's internal oscillator is set at twice the IF frequency via external tuning components. The MAX2451 comes in a 16-pin narrow SO package.

Features

- ♦ **Integrated Quadrature Phase Shifters**
- ♦ **On-Chip Oscillator (Requires External Tuning Circuit)**
- ♦ **51dB Voltage Conversion Gain**
- ♦ **On-Chip Divide-by-8 Prescaler**
- ♦ **Baseband Output Bandwidth Up to 9MHz**
- ♦ **CMOS-Compatible Enable**
- ♦ **5.5mA Operating Supply Current**
  2µA Shutdown Supply Current

Applications

Digital Cordless Phones

GSM and North American Cellular Phones

Wireless LANs

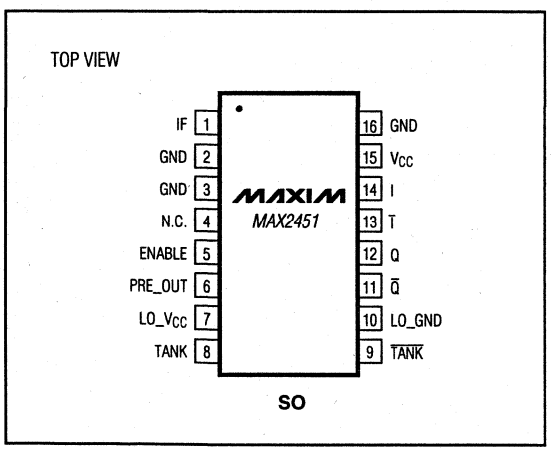
Digital Communications

Pagers

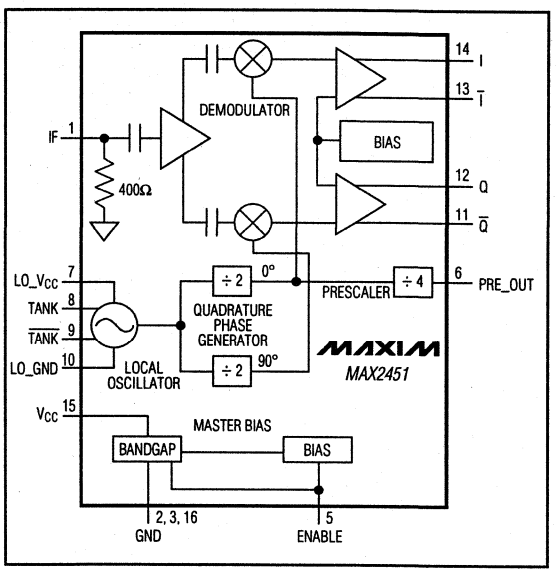
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX2451CSE	0°C to +70°C	16 Narrow SO

Pin Configuration



Functional Diagram



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

3V, Ultra-Low-Power Quadrature Demodulator

ABSOLUTE MAXIMUM RATINGS

V_{CC}, LO_V_{CC} to GND.....-0.3V to +4.5V
ENABLE, TANK, $\overline{TANK}$, I, $\overline{I}$,
Q, $\overline{Q}$ to GND.....-0.3V to (V_{CC} + 0.3V)
IF to GND.....-0.3V to +1.5V

Continuous Power Dissipation (T_A = +70°C)
Narrow SO (derate 8.70mW/°C above +70°C) 696mW
Operating Temperature Range.....0°C to +70°C
Storage Temperature Range .....-65°C to +165°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = LO_V_{CC} = $\overline{TANK}$ = +2.7V to +3.3V, ENABLE = V_{CC} - 0.4V, GND = LO_GND = 0V, I = $\overline{I}$ = Q = $\overline{Q}$ = IF = TANK = OPEN, T_A = 0°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{CC}, LO_V_{CC}		2.7		3.3	V
Supply Current	$I_{CC(ON)}$			5.5	7.4	mA
Shutdown Supply Current	$I_{CC(OFF)}$	Enable = 0.4V		2	20	µA
Enable/Disable Time	$t_{ON/OFF}$			10		µs
ENABLE Bias Current	I_{EN}			1	3	µA
ENABLE High Voltage	V_{ENH}		V_{CC} - 0.4			V
ENABLE Low Voltage	V_{ENL}				0.4	V
IF Input Impedance	Z_{IN}		320	400	480	Ω
I, $\overline{I}$, Q, $\overline{Q}$ Voltage Level	$V_{I/\overline{I}}$, $V_{Q/\overline{Q}}$			1.2		V
Baseband I and Q DC Offset				±11	±50	mV

AC ELECTRICAL CHARACTERISTICS

V_{CC} = LO_V_{CC} = ENABLE = 3.0V, f_{LO} = 140MHz, f_{IF} = 70.1MHz, V_{IF} = 2.82mVp-p, T_A = +25°C, unless otherwise noted.)

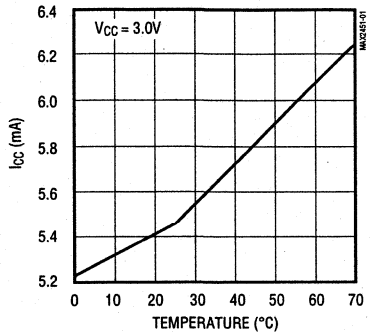
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Baseband I and Q Amplitude Balance				< ±0.45		dB
Baseband I and Q Phase Accuracy				< ±1.3		degrees
Voltage Conversion Gain				51		dB
Noise Figure	NF			18		dB
Allowable I and Q Voltage Swing		(Note 1)			1.35	Vp-p
I and Q IM3 Level	$IM3_{I/Q}$	(Note 2)		-44		dBc
I and Q IM5 Level	$IM5_{I/Q}$	(Note 2)		-60		dBc
I and Q Signal 3dB Bandwidth	BW_{3dB}			9		MHz
Oscillator Frequency Range	f_{LO}	(Notes 1, 3)	70		160	MHz
PRE_OUT Output Voltage	V_{PRE_OUT}	R_L = 10kΩ, C_L < 6pF		0.35		Vp-p
PRE_OUT Slew Rate	SR_{PRE_OUT}	R_L = 10kΩ, C_L < 6pF, rising edge		60		V/µs
Oscillator Phase Noise		Offset = 10kHz		-80		dBc/Hz

Note 1: Guaranteed by design, not tested.
Note 2: f_{IF} = 2 tones at 70.10MHz and 70.11MHz, V_{IF} = 1.41mVp-p per tone.
Note 3: Oscillator frequencies up to 1GHz (500MHz IF) by externally overdriving (see *Applications Information*).

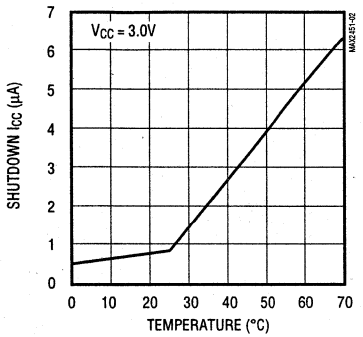
Typical Operating Characteristics

(V_{CC} = LO_V_{CC} = ENABLE = 3.0V, f_{LO} = 140MHz, f_{IF} = 70.1MHz, V_{IF} = 2.82mVp-p, T_A = +25°C, unless otherwise noted.)

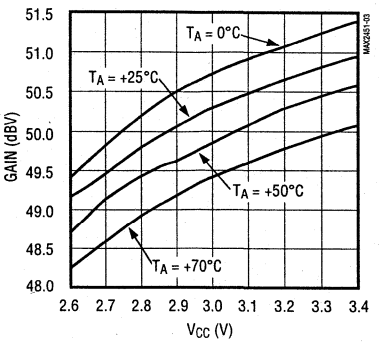
SUPPLY CURRENT vs. TEMPERATURE



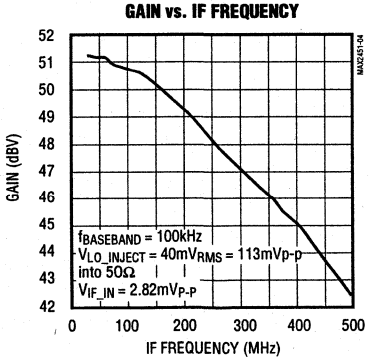
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



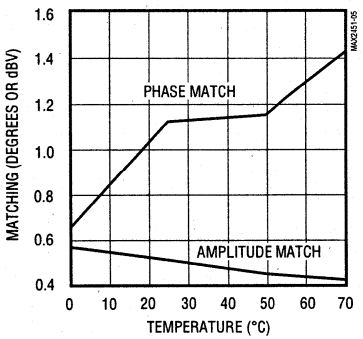
VOLTAGE CONVERSION GAIN vs. TEMPERATURE AND SUPPLY VOLTAGE



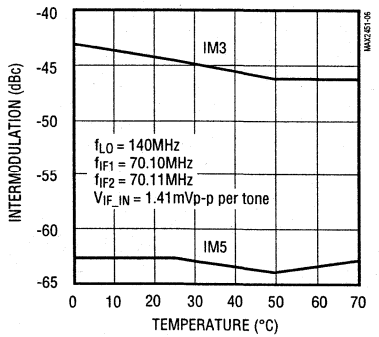
VOLTAGE CONVERSION GAIN vs. IF FREQUENCY



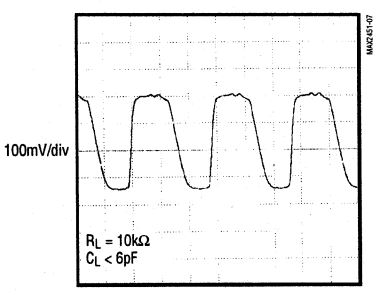
PHASE AND AMPLITUDE MATCHING vs. TEMPERATURE



INTERMODULATION POWER vs. TEMPERATURE



PRE_OUT WAVEFORM



3V, Ultra-Low-Power Quadrature Demodulator

Pin Description

PIN	NAME	FUNCTION
1	IF	IF Input
2, 3, 16	GND	Ground
4	N.C.	No Connect. No internal connection to this pin.
5	ENABLE	Enable Control, active high
6	PRE_OUT	Local-Oscillator Divide-by-8 Prescaled Output
7	LO_VCC	Local-Oscillator Supply. Bypass separately from VCC.
8	TANK	Local-Oscillator Resonant Tank Input
9	$\overline{TANK}$	Local-Oscillator Resonant Tank Inverting Input
10	LO_GND	Local-Oscillator Ground
11	$\overline{Q}$	Baseband Quadrature Inverting Output
12	Q	Baseband Quadrature Output
13	$\overline{I}$	Baseband Inphase Inverting Output
14	I	Baseband Inphase Output
15	VCC	Demodulator Supply

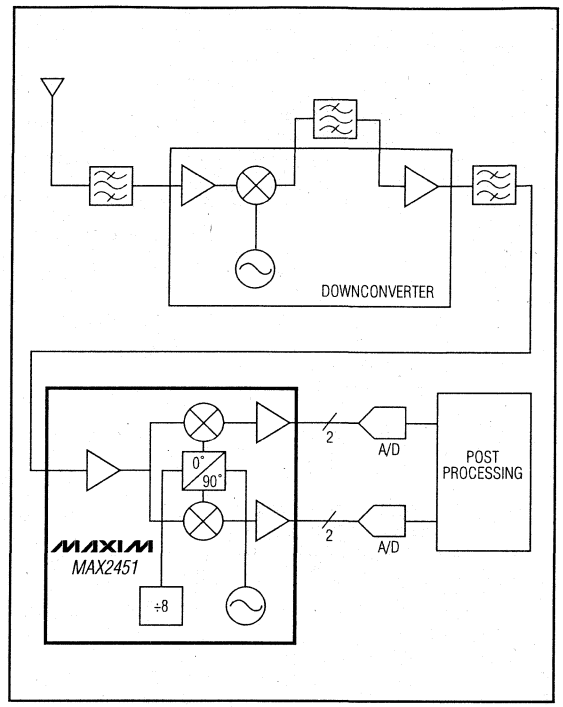


Figure 1. Typical Application Block Diagram

Detailed Description

The following sections describe each of the functional blocks shown in the *Functional Diagram*. Also refer to the Typical Application Block Diagram (Figure 1).

Demodulator

The demodulator contains a single-ended-to-differential converter, two Gilbert-cell multipliers, and two fixed gain stages. Internally, IF is terminated with a 400Ω resistor to GND. The IF input signal is AC coupled into the input amplifier, which has 14dB of gain. This amplified IF signal is fed into the I and Q channel mixers for demodulation. The multipliers mix the IF signal with the quadrature LO signals, resulting in baseband I and Q signals. The conversion gain of the multipliers is 15dB. These signals are further amplified by 21dB by the baseband amplifiers. The baseband amplifier chains are DC coupled.

Local Oscillator

The local-oscillator section is formed by an emitter-coupled differential pair. Figure 2 shows the local-oscillator equivalent circuit schematic. An external LC resonant tank determines the oscillation frequency, and the Q of this resonant tank affects the oscillator phase noise. The oscillation frequency is twice the IF frequency, for easy generation of quadrature signals.

The oscillator may be overdriven by an external source. The source should be AC coupled into TANK/$\overline{TANK}$, and should provide 200mVp-p levels. A choke (typically 2.2µH) is required between TANK and $\overline{TANK}$. Differential input impedance at TANK/$\overline{TANK}$ is 10kΩ. For single-ended drive, connect an AC bypass capacitor (1000pF) from $\overline{TANK}$ to GND, and AC couple TANK to the source.

The oscillator can be overdriven at frequencies up to 1GHz (500MHz IF), but conversion gain and prescaler output levels will be somewhat reduced.

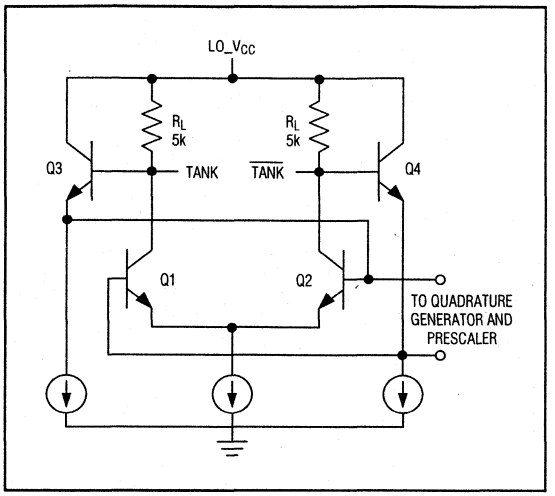


Figure 2. Local-Oscillator Equivalent Circuit

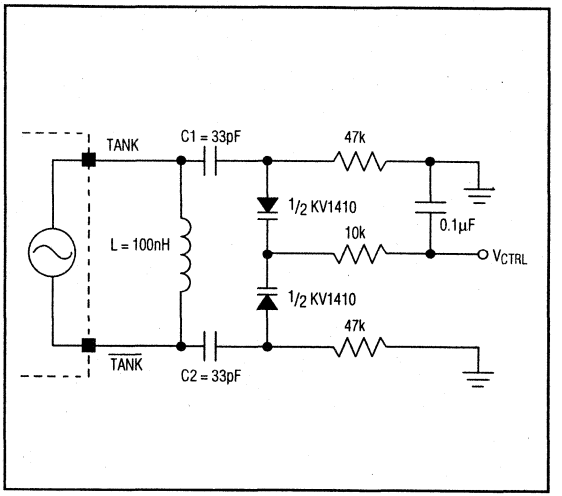


Figure 3. Typical Resonant Tank Circuit

Quadrature Phase Generator

The quadrature phase generator uses two latches to divide the local-oscillator frequency by two, and generates two precise quadrature signals. Internal limiting amplifiers shape the signals to approximate square waves to drive the Gilbert-cell mixers. The inphase signal (at half the local oscillator frequency) is further divided by four for the prescaler output.

Prescaler

The prescaler output, PRE_OUT, is buffered and swings typically 0.35Vp-p with a 10kΩ and 6pF load. It can be AC coupled to the input of a frequency synthesizer.

Master Bias

During normal operation, ENABLE should be above V_{CC} - 0.4V. Pulling the ENABLE input low shuts off the master bias and reduces the circuit current to typically 2µA. The master bias section includes a bandgap reference generator and a PTAT (Proportional To Absolute Temperature) current generator.

Applications Information

Figure 3 shows the implementation of a resonant tank circuit. The inductor, two capacitors, and a dual varactor form the oscillator's resonant circuit. In Figure 3, the oscillator frequency ranges from 130MHz to 160MHz. To ensure reliable start-up, the inductor is directly connected across the local oscillator's tank ports. The two 33pF capacitors affect the Q of the resonant circuit. Other values may be chosen to meet individual application requirements. The oscillation frequency can be determined using the following formula:

$$f_O = \frac{1}{2\pi\sqrt{L_{EQ}C_{EQ}}}$$

where

$$C_{EQ} = \frac{1}{\frac{1}{C1}+\frac{1}{C2}+\frac{2}{C_{VAR}}} + C_{STRAY}$$

and

$$L_{EQ} = L + L_{STRAY}$$

where C_{STRAY} = parasitic capacitance and L_{STRAY} = parasitic inductance.

To alter the oscillation frequency range, change the inductance, the capacitance, or both. For best phase-noise performance, keep the Q of the resonant tank as high as possible:

$$Q = R_{EQ}\sqrt{\frac{C_{EQ}}{L_{EQ}}}$$

where $R_{EQ} \approx 10k\Omega$ (Figure 2).

The oscillation frequency can be changed by altering the control voltage, V_{CTRL}.

19-0425; Rev 1; 9/95

EVALUATION KIT AVAILABLE

MAXIM

3V, Ultra-Low-Power Quadrature Modulator

General Description

The monolithic MAX2452 is a quadrature modulator with supporting oscillator and divide-by-8 prescaler. It operates from a single +3V supply and draws only 4.1mA. The modulator accepts differential I and Q baseband signals with amplitudes up to 1.35Vp-p and bandwidths up to 15MHz. It produces a differential output up to 80MHz.

Pulling the CMOS-compatible ENABLE pin low reduces the supply current to 2µA. To minimize spurious feedback, the MAX2452's internal oscillator is set at twice the IF via external tuning components. The oscillator and associated phase shifters produce differential signals exhibiting low amplitude and phase imbalance, yielding 42dB sideband rejection. The MAX2452 comes in a 16-pin narrow SO package.

Features

- ♦ **IF Output Frequency up to 80MHz**
- ♦ **Input Bandwidth up to 15MHz**
- ♦ **On-Chip Oscillator with External Tuning Circuit**
- ♦ **On-Chip Divide-by-8 Prescaler**
- ♦ **Integrated Quadrature Phase Shifters**
- ♦ **Self-Biased Differential Baseband Inputs**
- ♦ **CMOS-Compatible Enable**
- ♦ **4.1mA Operating Supply Current**
  2µA Shutdown Supply Current

Applications

Digital Cordless Phones

GSM and North American Cellular Phones

Wireless LANs

Digital Communications

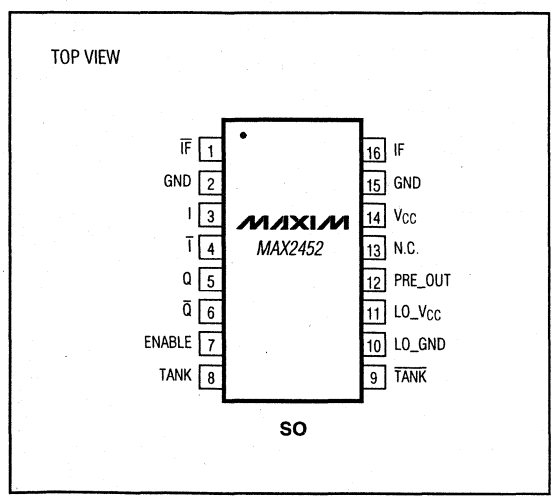
Two-Way Pagers

Ordering Information

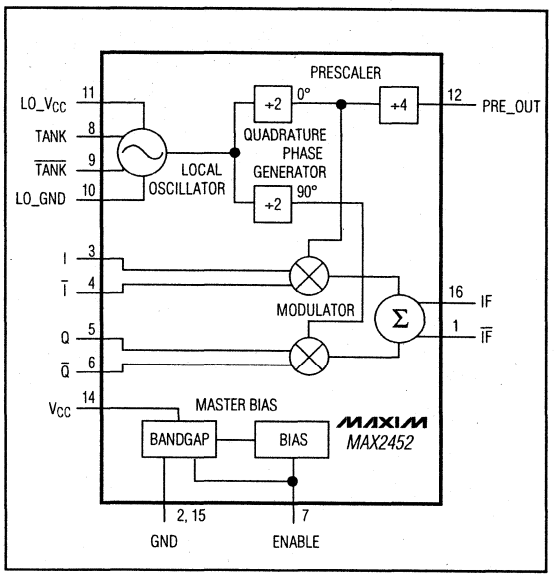
PART	TEMP. RANGE	PIN-PACKAGE
MAX2452ISE*	-20°C to +85°C	16 Narrow SO

** An alternate marking, MAX2452CSE, has been identically tested.*

Pin Configuration



Functional Diagram



11

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

3V, Ultra-Low-Power Quadrature Modulator

ABSOLUTE MAXIMUM RATINGS

V_{CC}, LO_V_{CC} to GND .....-0.3V to +4.5V
ENABLE, TANK, $\overline{TANK}$, I, $\overline{I}$, Q, $\overline{Q}$ to GND .....V_{CC} + 0.3V
Continuous Power Dissipation (T_A = +70°C)
SO (derate 8.33mW/°C above +70°C).....667mW

Operating Temperature Range .....-20°C to +85°C
Storage Temperature Range .....-65°C to +165°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = LO_V_{CC} = 2.7V to 3.3V, T_A = -20°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{CC}, LO_V_{CC}		2.7		3.3	V
Supply Current	$I_{CC\ ON}$	Enable = V_{CC} - 0.4V		4.1	7	mA
Shutdown Supply Current	$I_{CC\ OFF}$	Enable = 0.4V		2	20	µA
Enable/Disable Time	$t_{ON/OFF}$			10		µs
ENABLE Bias Current	I_{EN}	Enable = V_{CC} - 0.4V		1	10	µA
ENABLE Low Voltage	V_{ENL}				0.4	V
ENABLE High Voltage	V_{ENH}		V_{CC} - 0.4			V
IF Voltage Level	V_{IF}		V_{CC} - 1.7		V_{CC} - 1.35	V
$\overline{IF}$ Voltage Level	$V_{\overline{IF}}$		V_{CC} - 1.7		V_{CC} - 1.35	V
TANK Voltage Level	V_{TANK}		LO_V_{CC} - 1.1		LO_V_{CC} - 0.8	V
$\overline{TANK}$ Voltage Level	$V_{\overline{TANK}}$		LO_V_{CC} - 1.1		LO_V_{CC} - 0.8	V
I, $\overline{I}$, Q, $\overline{Q}$ Voltage Level	V_I, $V_{\overline{I}}$, V_Q, $V_{\overline{Q}}$		1.25	1.5	1.75	V
Differential Input Impedance	$Z_{I\overline{I}}$, $Z_{Q\overline{Q}}$		35	44		kΩ

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = LO_V_{CC} = 3.0V, f_{OSC} = 140MHz, ENABLE = 2.6V, $f_{I\overline{I}}$ = $f_{Q\overline{Q}}$ = 600kHz, T_A = -20°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Input Voltage	$V_{I\overline{I}p\text{-}p}$, $V_{Q\overline{Q}p\text{-}p}$	(Note 1)		1.2	1.35	Vp-p
I and Q Signal Bandwidth	BW_{IQ}	(Note 1)			15	MHz
IF Differential Output Voltage	$V_{IF\overline{IF}p\text{-}p}$	$V_{I\overline{I}}$ = $V_{Q\overline{Q}}$ = 1.2Vp-p, R_L = 200kΩ differential, C_L < 5pF differential		65		mVp-p
I/Q Amplitude Match				<±0.3		dB
I/Q Phase Match				<±3		degrees
Sideband Rejection				42		dB
LO Leakage at Output		$V_{I\overline{I}}$ = $V_{Q\overline{Q}}$ = 1.2Vp-p		-36		dBc
Oscillator Frequency Range	f_{OSC}	(Notes 1, 2)	70	140	160	MHz
PRE_OUT Output Voltage	V_{PRE_OUT}	R_L = 10kΩ, C_L < 6pF		0.35		Vp-p
PRE_OUT Slew Rate	SR_{PRE_OUT}	R_L = 10kΩ, C_L < 6pF, rising edge, T_A = +25°C		60		V/µs

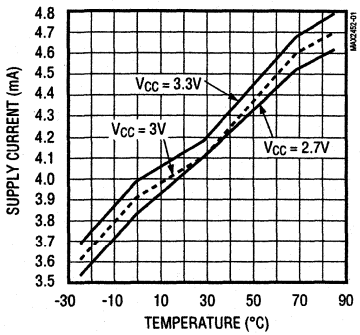
Note 1: Guaranteed by design, not tested.
Note 2: The frequency range can be extended in either direction, but has not been characterized. At higher frequencies, the IF output level may decrease and distortions may increase.

3V, Ultra-Low-Power Quadrature Modulator

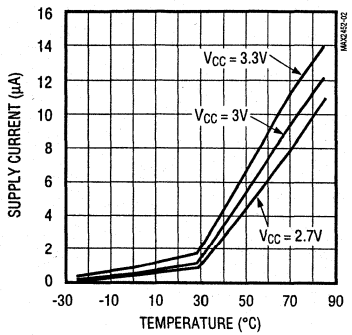
Typical Operating Characteristics

(V_{CC} = LO_V_{CC} = 3.0V, f_{OSC} = 140MHz, ENABLE = 2.6V, $f_{\overline{I}I}$ = $f_{Q\overline{Q}}$ = 600kHz, R_L (IF, $\overline{IF}$) = 200kΩ differential, C_L (IF, $\overline{IF}$) < 5pF differential, T_A = +25°C, unless otherwise noted.)

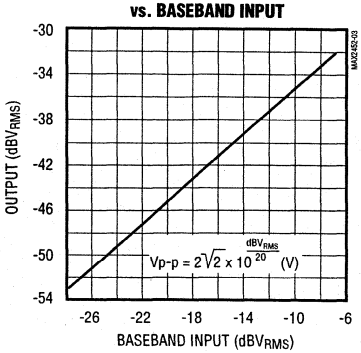
SUPPLY CURRENT vs. TEMPERATURE



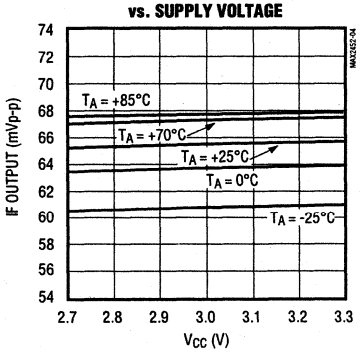
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



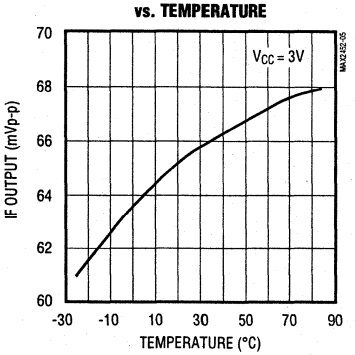
IF OUTPUT vs. BASEBAND INPUT



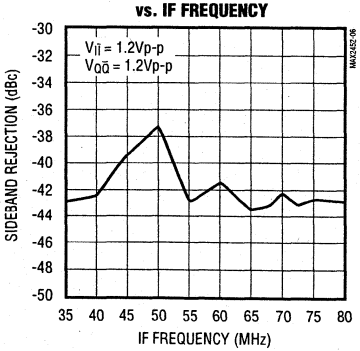
IF OUTPUT vs. SUPPLY VOLTAGE



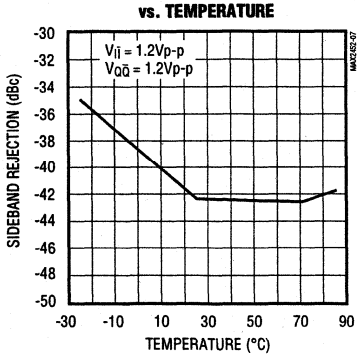
IF OUTPUT vs. TEMPERATURE



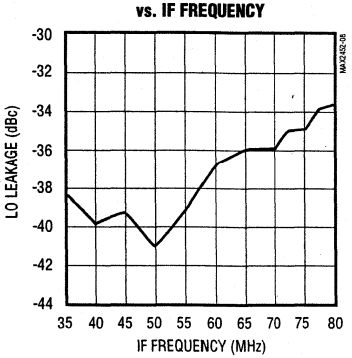
SIDEBAND REJECTION vs. IF FREQUENCY



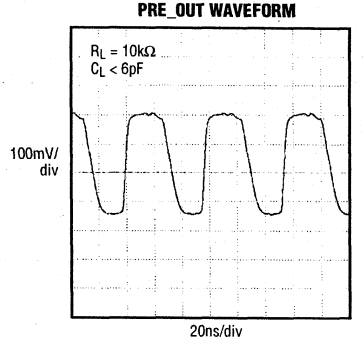
SIDEBAND REJECTION vs. TEMPERATURE



LO LEAKAGE vs. IF FREQUENCY



PRE_OUT WAVEFORM

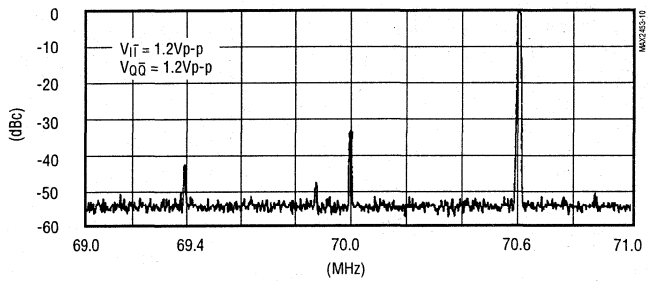


3V, Ultra-Low-Power Quadrature Modulator

Typical Operating Characteristics (continued)

(V_{CC} = LO_V_{CC} = 3.0V, f_{OSC} = 140MHz, ENABLE = 2.6V, $f_{I\overline{I}}$ = $f_{Q\overline{Q}}$ = 600kHz, R_L (IF, $\overline{IF}$) = 200kΩ differential, C_L (IF, $\overline{IF}$) < 5pF differential, T_A = +25°C, unless otherwise noted.)

MODULATOR OUTPUT SPECTRUM



Pin Description

PIN	NAME	FUNCTION
1	$\overline{IF}$	IF Inverting Output
2, 15	GND	Ground
3	I	Inphase Input
4	$\overline{I}$	Inphase Inverting Input
5	Q	Quadrature Input
6	$\overline{Q}$	Quadrature Inverting Input
7	ENABLE	Enable Control, active high
8	TANK	Local-Oscillator Resonant Tank Input
9	$\overline{TANK}$	Local-Oscillator Resonant Tank Inverting Input
10	LO_GND	Local-Oscillator Ground
11	LO_V_{CC}	Local-Oscillator Supply
12	PRE_OUT	Local-Oscillator Divide-by-8 Prescaled Output
13	N.C.	No Connect, no internal connection to this pin
14	V_{CC}	Modulator Supply
16	IF	IF Output

Detailed Description

The MAX2452 quadrature modulator integrates several important RF functions on a single chip. It includes differential buffers for the baseband inputs, two double-balanced mixers, a local oscillator, a quadrature phase generator, and a divide-by-8 prescaler. The prescaler simplifies the implementation of a phase-locked loop. Each of the functional blocks (shown in the *Functional Diagram*) is described in detail in the following sections.

Local Oscillator

The local-oscillator section is formed by an emitter-coupled differential pair. Figure 1 shows the equivalent local-oscillator circuit schematic. An external LC resonant tank determines the oscillation frequency, and the Q of this resonant tank determines the phase noise of the oscillator. The oscillation frequency is twice the IF frequency, so that the quadrature phase generator can use two latches to generate precise quadrature signals.

Quadrature Phase Generator

The quadrature phase generator uses two latches to divide the local-oscillator frequency by two, and generates two precise quadrature signals. Internal limiting amplifiers shape the signals to approximate square waves to drive the Gilbert-cell mixers in the modulator. The inphase signal (at half the local-oscillator frequency) is further divided by four for an external phase-locked loop.

Modulator

The modulator accepts up to 1.35Vp-p I and Q differential baseband signals up to 15MHz, and upconverts them to higher-frequency IF signals. Since these inputs are biased internally at around 1.5V, you can improve carrier suppression by externally capacitively coupling the signals into these high-impedance ports (the differential input impedance is approximately 44kΩ). The self-bias design is for very low on-chip offset, resulting in excellent carrier suppression. The IF output is designed to drive a high impedance (>20kΩ), such as an IF buffer or an upconverter mixer.

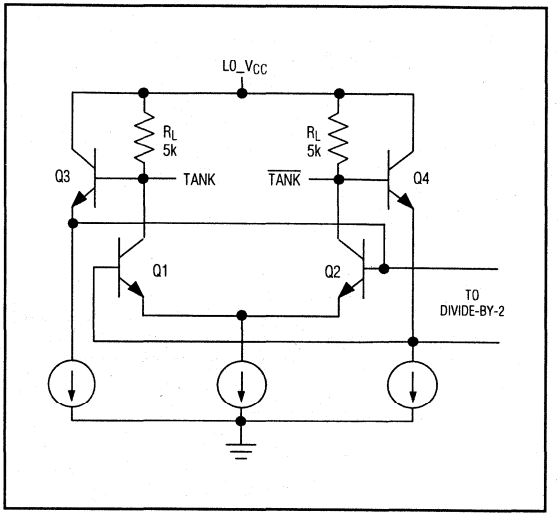


Figure 1. Local-Oscillator Equivalent Circuit

Prescaler

The prescaler output, PRE_OUT, is buffered and swings typically 0.35Vp-p with a 10kΩ and 6pF load. It can be AC-coupled to the input of a frequency synthesizer.

Master Bias

During normal operation, ENABLE should remain above VCC - 0.4V. Pulling the ENABLE input low shuts off the master bias and reduces the circuit current to 2µA. The master bias section includes a bandgap reference generator and a PTAT (Proportional To Absolute Temperature) current generator.

3V, Ultra-Low-Power Quadrature Modulator

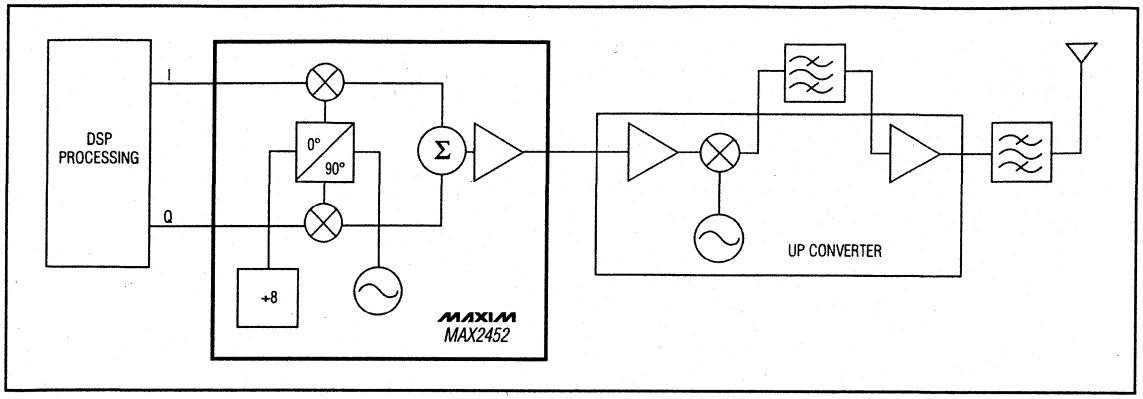


Figure 2. Typical Application Block Diagram

Applications Information

The MAX2452 quadrature modulator is designed to upconvert I and Q baseband signals to IF frequencies up to 80MHz. Figure 2 shows a typical application block diagram, in which the MAX2452 is used for the first upconversion in a dual-conversion transmitter.

Figure 3 shows an implementation of a resonant tank circuit. The inductor, two capacitors, and a dual varactor form the resonant circuit of the oscillator. The frequency range of the oscillator shown in Figure 3 is 130MHz to 160MHz. The inductor is directly connected across the local oscillator's tank ports so that it will not lock up the oscillator in a stable state during start-up. The two 33pF capacitors increase the Q of the resonant circuit and reduce the VCO gain. They can be changed to meet individual applications requirements. The oscillation frequency can be determined using the following formula:

$$f_o = \frac{1}{2\pi\sqrt{L_{EQ}\ C_{EQ}}}$$

where

$$C_{EQ} = \frac{1}{\frac{1}{C1} + \frac{1}{C2} + \frac{2}{C_{VAR}}} + C_{STRAY}$$

and

$$L_{EQ} = L + L_{STRAY}$$

C_{STRAY}, L_{STRAY}: parasitic capacitance and inductance.

To alter the oscillation frequency range, change the inductance, the capacitance, or both. Make sure the Q of the resonant tank does not drop below 35.

$$Q = R_{EQ}\sqrt{\frac{C_{EQ}}{L_{EQ}}}$$

where R_{EQ} = 10kΩ (see Figure 1).

The oscillation frequency can be changed by altering the control voltage, V_{CTRL}.

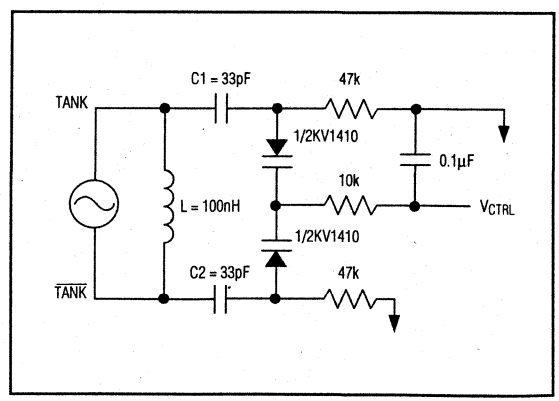


Figure 3. Typical Resonant Tank Circuit

ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
11/96

MAXIM

3V, 1W RF Power Transistors for 900MHz Applications

General Description

The MAX2601/MAX2602 are RF power transistors optimized for use in portable cellular and wireless equipment that operates from three NiCd/NiMH cells or one Li-Ion cell. These transistors can deliver 1W of RF power from a 3.6V supply, with up to 60% efficiency.

The MAX2601 is a high-performance silicon bipolar RF power transistor. The MAX2602 includes a high-performance silicon bipolar RF power transistor, and a biasing diode that matches the thermal and process characteristics of the power transistor. This diode is used to create a bias network that accurately controls the power transistor's collector current as the temperature changes.

The MAX2601/MAX2602 can be used as the final stage in a discrete or module power amplifier. Silicon bipolar technology eliminates the need for voltage inverters and sequencing circuitry, as required by GaAsFET power amplifiers. Furthermore, a drain switch is not required to turn off the MAX2601/MAX2602. This increases operating time in two ways: it allows lower system end-of-life battery voltage, and it eliminates the wasted power from a drain-switch device.

The MAX2601/MAX2602 are available in thermally enhanced 8-pin SO packages, which are screened to the extended temperature range (-40°C to +85°C). The MAX2602 is also available in die form.

Applications

Land Mobile Radios
AMPS Cellular Phones
Narrow-Band PCS (NPCS)
915MHz ISM Transmitters
Microcellular GSM (Power Class 5)
European ISM Band Applications

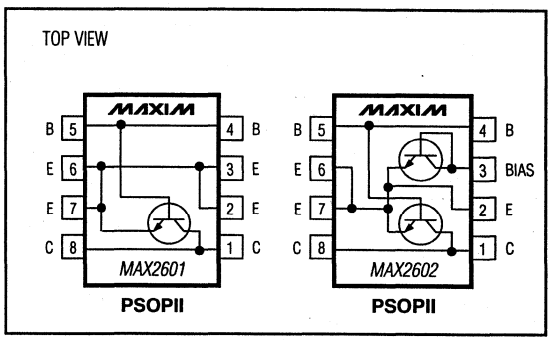
Features

- **Low Voltage: Operates from 1 Li-Ion or 3 NiCd/NiMH Batteries**
- **DC-to-Microwave Operating Range**
- **1W Output Power at 900MHz**
- **On-Board Diode for Accurate Biasing (MAX2602)**
- **High Efficiency**
- **Does Not Require Negative Bias or Supply Switch**
- **Low-Cost Silicon Bipolar Technology**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX2601ESA	-40°C to +85°C	8 PSOPII
MAX2602ESA	-40°C to +85°C	8 PSOPII
MAX2602E/D	-40°C to +85°C	Dice

Pin Configurations



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19-1094; Rev 0; 6/96

EVALUATION KIT AVAILABLE

DC-to-Microwave, Low-Noise Amplifier

General Description

The MAX2611 is a low-voltage, low-noise amplifier for use from DC to microwave frequencies. Operating from a single +5V supply, it has a 3dB bandwidth of 1100MHz. The MAX2611's low noise figure and high drive capability make it ideal for a variety of transmit, receive, and buffer applications.

In a typical application, the only external components needed are input and output blocking capacitors and a V_{CC} series resistor. To improve gain and output power, an RF choke can be added in series to the bias resistor.

The MAX2611 comes in a 4-pin SOT143 package, requiring minimal board space.

Features

- ♦ **Single +5V Supply Operation**
- ♦ **3dB Bandwidth: DC to 1100MHz**
- ♦ **High Gain: 18dB at 500MHz**
- ♦ **Low Noise Figure: 3.5dB at 500MHz**
- ♦ **High Drive Capability: +3dBm at 16mA I_D**
- ♦ **Ultra-Small SOT143 Package**

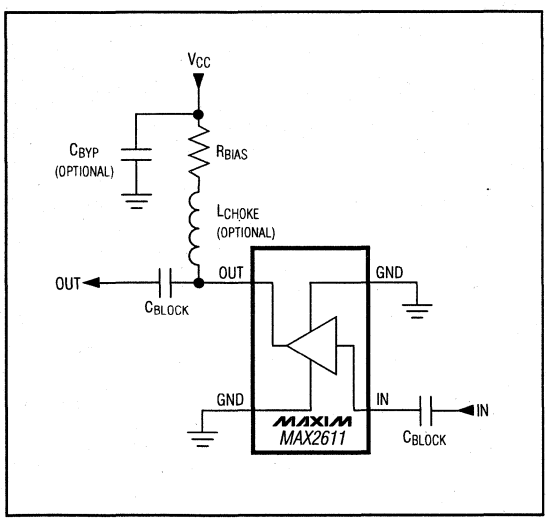
Applications

Satellite Receivers
TV Tuners
Wireless Local Loops
ISM Radios
Global Positioning Systems
Wireless Local-Area Networks
Land Mobile Radios
Set-Top Boxes

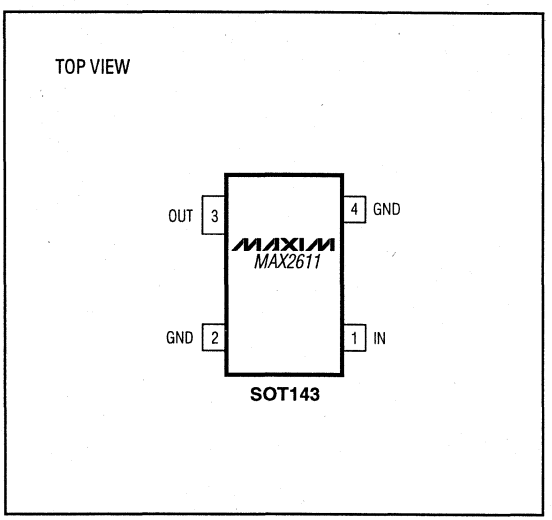
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX2611EUS	-40°C to +85°C	4 SOT143

Typical Operating Circuit



Pin Configuration



11

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DC-to-Microwave, Low-Noise Amplifier

ABSOLUTE MAXIMUM RATINGS

I_D 40mA
Input Power .....+13dBm
Continuous Power Dissipation (T_A = +70°C)
SOT143-4 (derate 4mW/°C above +70°C).....320mW

Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(I_D = 16mA, Z_0 = 50Ω, f_{IN} = 500MHz, T_A = +25°C, unless otherwise noted.)

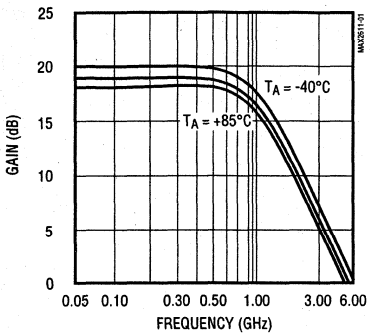
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Temperature Range	(Note 1)	-40		85	°C
Power Gain	f_{IN} = 100MHz		19.0		dB
	f_{IN} = 500MHz	17.3	18.3		
Gain Flatness	f_{IN} = 100MHz to 500MHz		±0.3		dB
3dB Bandwidth			1100		MHz
Input Voltage Standing-Wave Maximum Ratio	f_{IN} = 100MHz to 1500MHz		1.9:1		
Output Voltage Standing-Wave Maximum Ratio	f_{IN} = 100MHz to 1500MHz		1.6:1		
Output 1dB Compression Point			2.9		dBm
Noise Figure			3.5		dB
Output IP3			13		dBm
Group Delay			210		ps
Device Voltage		3.5	3.8	4.0	V
	T_A = T_{MIN} to T_{MAX} (Note 2)	3.25	3.8	4.26	
Device Voltage Temperature Coefficient			-6.1		mV/°C

Note 1: Parts are designed to operate over specified temperature range. Specifications are production tested and guaranteed at +25°C.
Note 2: Guaranteed by design, not tested.

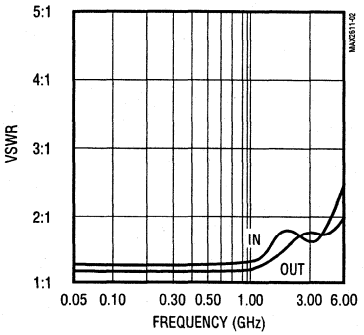
Typical Operating Characteristics

(I_D = 16mA, Z_0 = 50Ω, f_{IN} = 500MHz, T_A = +25°C, unless otherwise noted.)

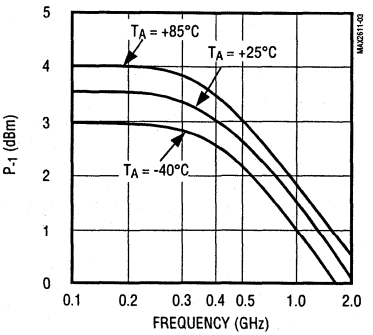
GAIN vs. FREQUENCY



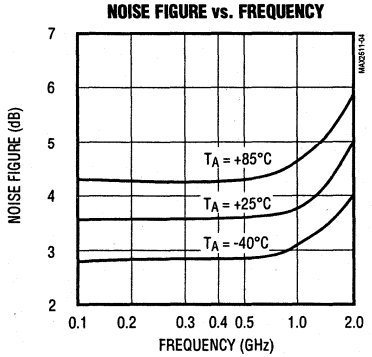
VOLTAGE STANDING-WAVE RATIO vs. FREQUENCY



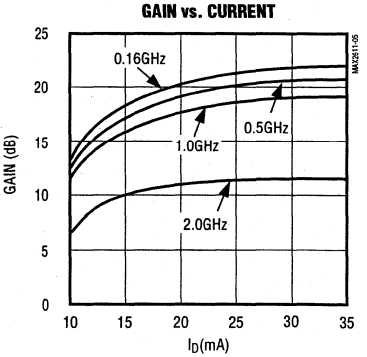
OUTPUT 1dB COMPRESSION POINT vs. FREQUENCY



NOISE FIGURE vs. FREQUENCY



GAIN vs. CURRENT



11

DC-to-Microwave, Low-Noise Amplifier

Pin Description

PIN	NAME	FUNCTION
1	IN	Amplifier Input. Use a series blocking capacitor with less than 3Ω reactance at your lowest operating frequency.
2, 4	GND	Ground Connection. For optimum performance, provide a low-inductance connection to the ground plane.
3	OUT	Amplifier Output. Use a series blocking capacitor with less than 3Ω reactance at your lowest operating frequency. Bias with an external resistor and an optional RF choke.

Table 1. Typical Scattering Parameters

(I_D = 16mA, Z_0 = 50Ω, T_A = +25°C)

FREQUENCY (GHz)	S11 (mag)	S11 (ang)	S21 (dB)	S21 (mag)	S21 (ang)	S12 (dB)	S12 (mag)	S12 (ang)	S22 (mag)	S22 (ang)	K
0.1	0.12	-11	19.0	8.90	173	-22.6	0.074	2	0.05	53	1.08
0.2	0.11	-44	18.8	8.73	166	-21.9	0.081	4	0.03	12	1.06
0.3	0.13	-58	18.6	8.53	158	-21.6	0.083	5	0.04	45	1.05
0.4	0.14	-78	18.5	8.43	151	-21.6	0.083	6	0.06	32	1.06
0.5	0.15	-89	18.3	8.26	144	-21.6	0.083	7	0.08	34	1.06
0.6	0.15	77	18.1	7.99	137	-21.6	0.083	9	0.09	26	1.07
0.8	0.13	50	17.4	7.45	123	-21.6	0.083	10	0.10	23	1.10
1.0	0.12	16	16.6	6.79	109	-20.9	0.090	10	0.10	35	1.11
1.5	0.32	-60	14.1	5.07	79	-21.8	0.081	11	0.21	-86	1.29
2.0	0.31	-72	10.3	3.27	59	-22.2	0.078	18	0.22	-72	1.87
2.5	0.32	-76	7.9	2.48	47	-22.6	0.074	25	0.26	-53	2.44
3.0	0.20	-70	5.9	1.98	32	-22.3	0.077	37	0.24	-29	3.10
3.5	0.24	-64	3.0	1.41	13	-21.4	0.086	30	0.19	47	3.83
4.0	0.31	-68	-0.7	0.92	17	-23.0	0.070	35	0.24	82	6.66

Detailed Description

The MAX2611 is a broadband amplifier with flat gain and 50Ω input and output ports. Its small size and simple bias circuitry make it ideal for applications where board space is limited.

Applications Information

External Components

As shown in the *Typical Operating Circuit*, the MAX2611 is easy to use. Input and output series capacitors may be necessary to block DC bias voltages (generated by the MAX2611) from interacting with adjacent circuitry. These capacitors must be large enough to contribute negligible reactance in a 50Ω system at the minimum operating frequency. Use the following equation to calculate their minimum value:

$$C_{BLOCK} = \frac{53{,}000}{f} \quad (pF)$$

where f (in MHz) is the minimum operating frequency.

Bias current is supplied to the MAX2611 through an external resistor and optional RF choke connected between V_{CC} and the OUT pin. A bypass capacitor from V_{CC} to GND may be necessary to isolate the V_{CC} line from other circuitry. The resistor value determines the bias current from the following equation:

$$I_D = \frac{V_{CC} - V_D}{R_{BIAS}}$$

where V_D is the device voltage, nominally 3.8V.

An optional RF choke can be added to improve the MAX2611's gain and output power. The choke should be large enough to reduce the loading effect that the bias resistor has on the amplifier output. This is a function of R_{BIAS}, frequency of operation, and output impedance.

Grounding

Proper grounding of the GND pins is essential. If the PC board uses a topside RF ground, the GND pins should be connected directly to it. For a board where the ground plane is not on the component side, the best technique is to connect the GND pins to it through multiple plated through-holes.

PC Board Layout Example

An example PC board layout is given in Figure 1. It uses FR-4 with 31mil layer thickness between the RF lines and the ground plane. This board satisfies all the above requirements.

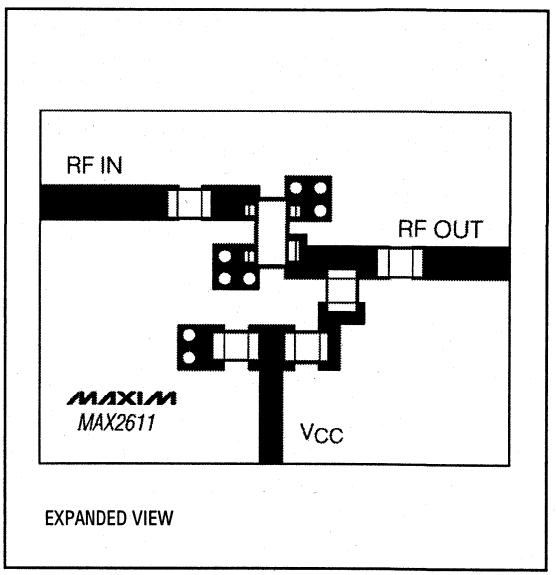
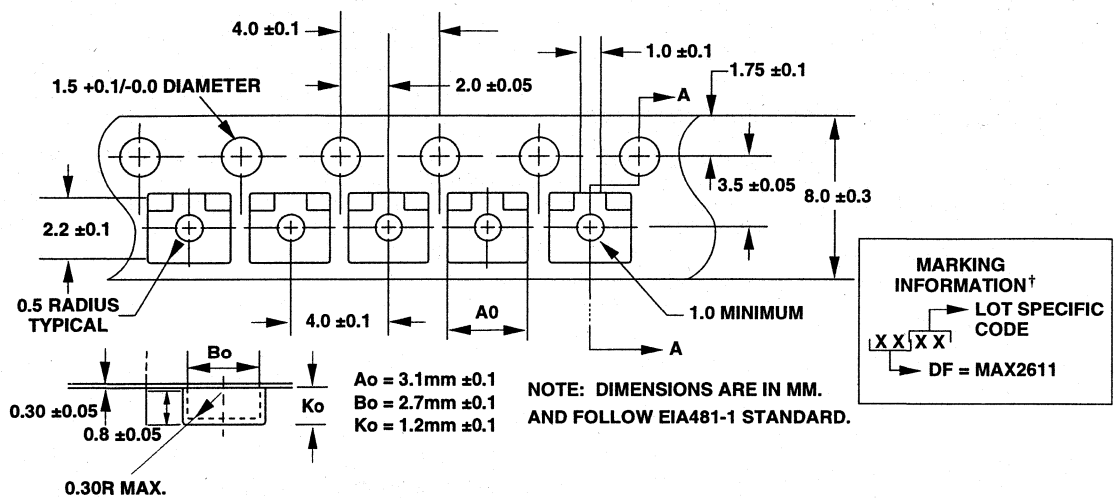


Figure 1. Example PC Board Layout

DC-to-Microwave, Low-Noise Amplifier

Tape-and-Reel Information



†ICs MAY ALSO BE MARKED WITH FULL PART NAME: 2611

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

11/96

MAXIM

650MHz to 1050MHz Integrated Oscillator with Buffered Outputs

General Description

The MAX2620 combines a low-noise oscillator with two output buffers in a low-cost, plastic surface-mount, ultra-small µMAX package. This device integrates functions typically achieved with discrete components. The oscillator exhibits low phase noise when properly mated with an external varactor-tuned resonant tank circuit. Two buffered outputs are provided for driving mixers or prescalers. The buffers provide load isolation to the oscillator and prevent frequency pulling due to load-impedance changes. Power consumption is typically just 27mW in operating mode (V_{CC} = 3.0V), and drops to less than 3µW in standby mode. The MAX2620 operates from a single +2.7V to +5.5V supply.

Applications

All Analog and Digital Cellular Phone Standards

900MHz Cordless Phones

900MHz ISM Radios

Land Mobile Radio

Narrowband PCS (NPCS)

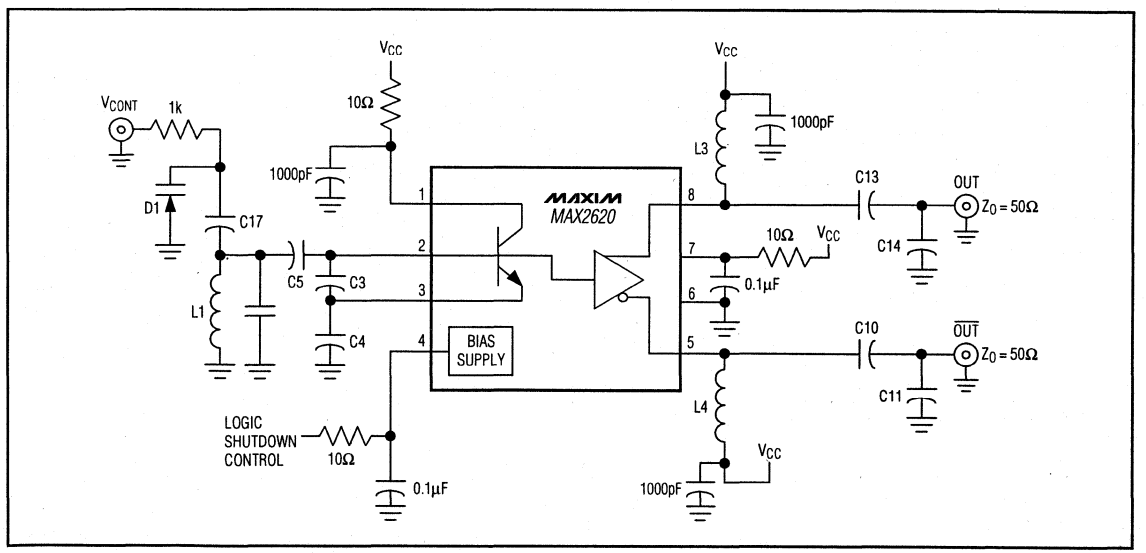
Features

- ♦ **Low-Phase-Noise Oscillator: -105dBc/Hz (25kHz offset from carrier) Attainable**
- ♦ **Operates from Single +2.7V to +5.5V Supply**
- ♦ **Low-Cost Silicon Bipolar Design**
- ♦ **Two Output Buffers Provide Load Isolation**
- ♦ **Insensitive to Supply Variations**
- ♦ **Low, 27mW Power Consumption (V_{CC} = 3.0V)**
- ♦ **Low-Current Shutdown Mode: < 1µA**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX2620EUA	-40°C to +85°C	8 µMAX

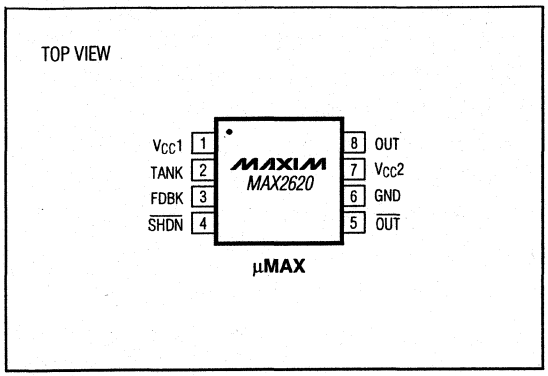
Typical Operating Circuit



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650MHz to 1050MHz Integrated Oscillator with Buffered Outputs

Pin Configuration



ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

10/96

MAXIM

VHF-to-Microwave, +3V, Low-Noise Amplifiers

General Description

The MAX2630/MAX2631/MAX2632/MAX2633 are low-voltage, low-noise amplifiers for use from VHF to microwave frequencies. Operating from a single +2.7V to +5.5V supply, they have a flat gain response to 900MHz. Their low noise figure and low supply current make them ideal for receive, buffer, and transmit IF applications.

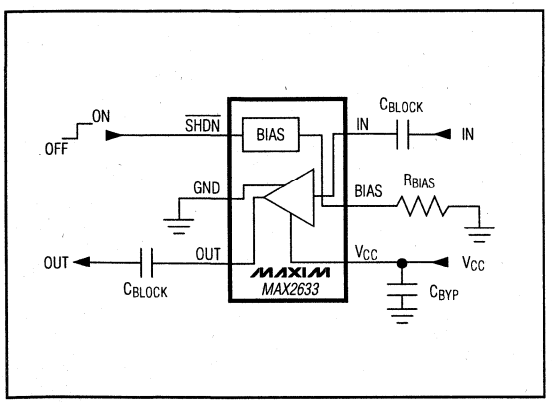
The MAX2630/MAX2631 are biased internally, eliminating the need for external bias resistors or inductors. The MAX2632/MAX2633 have a user-selectable supply current, adjustable by adding a single external resistor, which allows customized output power and gain according to specific application requirements. The MAX2631/MAX2633 feature a shutdown pin that allows them to be powered down to typically 0.1µA supply current. Aside from a single bias resistor required for the MAX2632/MAX2633, the only external components needed for this family of devices are input and output blocking capacitors and a V_{CC} bypass capacitor.

The MAX2630 comes in a 4-pin SOT143 package, requiring minimal board space. The MAX2631/MAX2632 come in small, 5-pin SOT23-5 packages. The MAX2633 comes in a 6-pin SOT23-6 package.

Applications

Personal Communicating Systems	Cordless Phones
Global Positioning Systems	Cellular Phones
Wireless Local Area Networks	ISM Radios
Wireless Local Loops	TV Tuners
Land Mobile Radios	Set-Top Boxes

Typical Operating Circuit



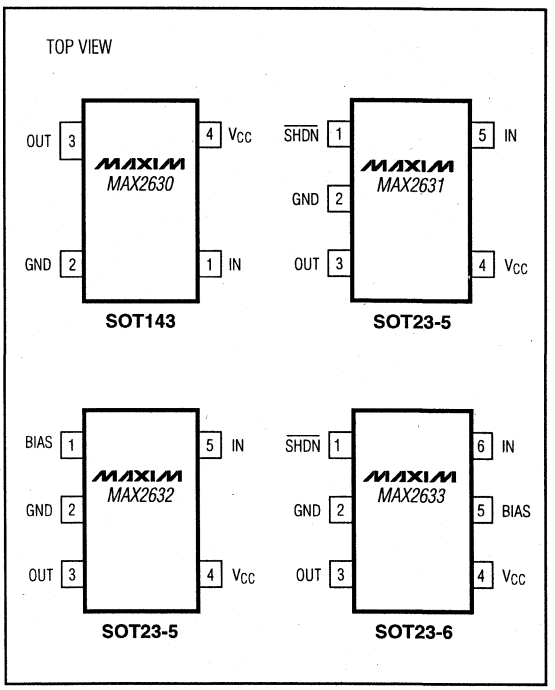
Features

- ♦ **Single +2.7V to +5.5V Operation**
- ♦ **Internally Biased (MAX2630/MAX2631)**
- ♦ **Adjustable Bias (MAX2632/MAX2633)**
- ♦ **6.6mA Supply Current (insensitive to supply voltage)**
- ♦ **0.1µA Shutdown Current (MAX2631/MAX2633)**
- ♦ **3.7dB Noise Figure**
- ♦ **Ultra-Small SOT Packages**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX2630EUS	-40°C to +85°C	4 SOT143
MAX2631EUK	-40°C to +85°C	5 SOT23-5
MAX2632EUK	-40°C to +85°C	5 SOT23-5
MAX2633EUT	-40°C to +85°C	6 SOT23-6

Pin Configurations



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19-1135; Rev 0; 9/96

EVALUATION PCB AVAILABLE

MAXIM

DC-to-Microwave, +5V Low-Noise Amplifier

General Description

The MAX2650 is a low-noise amplifier for use from DC to microwave frequencies. Operating from a single +5V supply, it has a flat gain response to 900MHz. The MAX2650's low noise figure and high drive capability make it ideal for a variety of transmit, receive, and buffer applications.

The device is internally biased, eliminating the need for external bias resistors or inductors. In a typical application, the only external components needed are input and output blocking capacitors and a V_{CC} bypass capacitor.

The MAX2650 comes in a 4-pin SOT143 package, requiring minimal board space.

Applications

Wireless Local Loop
Global Positioning Systems (GPS)
ISM Radios
Special Mobile Radios
Wireless Local-Area Networks
Cellular Base Stations
Set-Top Boxes

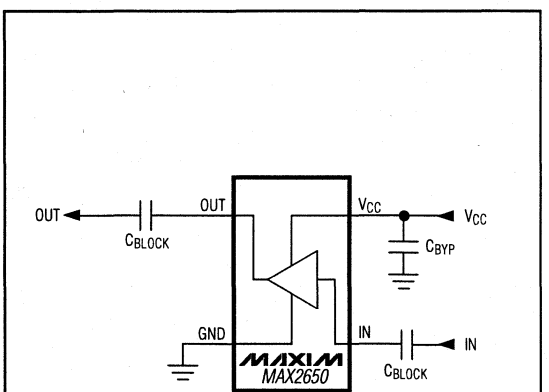
Features

- ♦ **Internally Biased**
- ♦ **High Gain: 18.3dB at 900MHz**
- ♦ **3.9dB Noise Figure**
- ♦ **Single +4.5V to +5.5V Operation**
- ♦ **-1dBm Output 1dB Compression Power**
- ♦ **Low-Cost Silicon Bipolar Design**
- ♦ **Ultra-Small SOT143 Package**

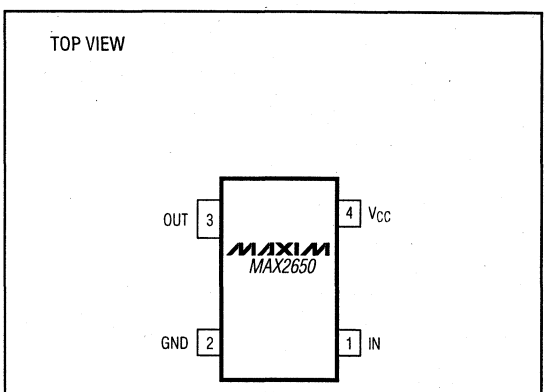
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX2650EUS-T	-40°C to +85°C	4 SOT143

Typical Operating Circuit



Pin Configuration



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DC-to-Microwave, +5V Low-Noise Amplifier

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +8V
Input Power .....+13dBm
Continuous Power Dissipation (T_A = +70°C)
SOT143-4 (derate 4mW/°C above +70°C).....320mW

Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5.0V, Z_0 = 50Ω, f_{IN} = 900MHz, T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Temperature Range	(Note 1)	-40		85	°C
Power Gain		16.5	18.3	21	dB
Output 1dB Compression Point			-1		dBm
Output IP3			10		dBm
Noise Figure			3.9		dB
Maximum Input Voltage Standing-Wave Ratio	f_{IN} = 100MHz to 1000MHz		1.5:1		
Maximum Output Voltage Standing-Wave Ratio	f_{IN} = 800MHz to 1000MHz		1.3:1		
Group Delay			300		ps
Supply Voltage		4.5		5.5	V
Supply Current		15.5	17.7	20.0	mA
	$T_A = T_{MIN}$ to T_{MAX}	13.0	17.7	22.0	
	V_{CC} = 4.5V to 5.5V	11.0	17.7	24.0	

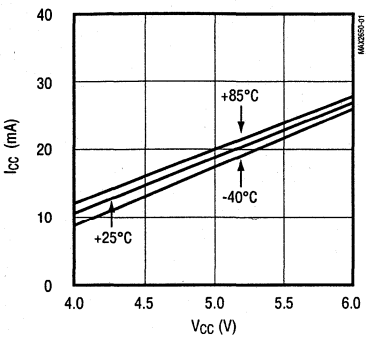
Note 1: Parts are designed to operate over specified temperature range. Specifications are production tested and guaranteed at +25°C.

DC-to-Microwave, +5V Low-Noise Amplifier

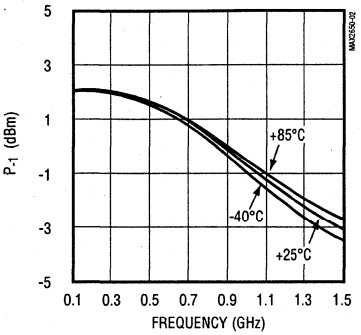
Typical Operating Characteristics

(V_{CC} = 5.0V, Z_0 = 50Ω, f_{IN} = 900MHz, T_A = +25°C, unless otherwise noted.)

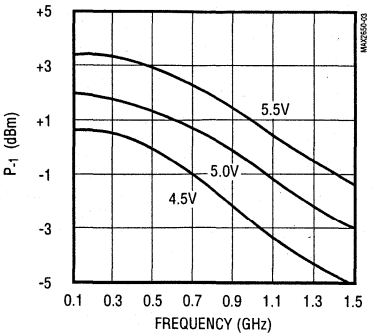
SUPPLY CURRENT vs. SUPPLY VOLTAGE



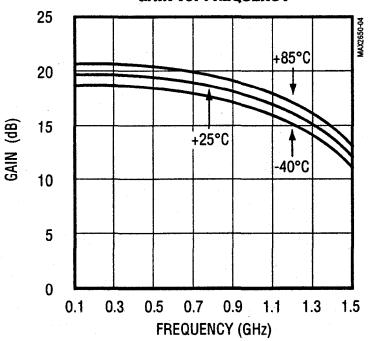
OUTPUT 1dB COMPRESSION POINT vs. FREQUENCY



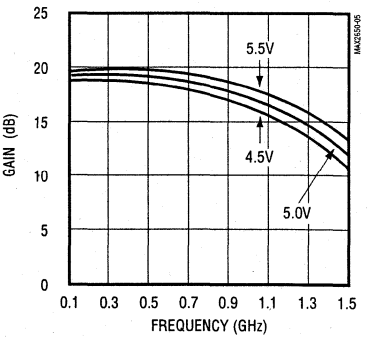
OUTPUT 1dB COMPRESSION POINT vs. FREQUENCY



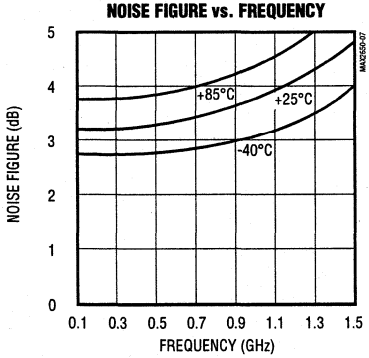
GAIN vs. FREQUENCY



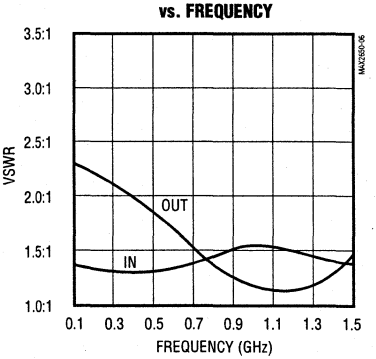
GAIN vs. FREQUENCY



NOISE FIGURE vs. FREQUENCY



VOLTAGE STANDING-WAVE RATIO vs. FREQUENCY



DC-to-Microwave, +5V Low-Noise Amplifier

Pin Description

PIN	NAME	FUNCTION
1	IN	Amplifier Input. Use a series blocking capacitor with less than 3Ω reactance at your lowest operating frequency.
2	GND	Ground Connection. For optimum performance, provide a low-inductance connection to the ground plane.
3	OUT	Amplifier Output. Use a series blocking capacitor with less than 3Ω reactance at your lowest operating frequency.
4	V_{CC}	Supply Connection. Bypass directly at the package pin. The value of the bypass capacitor is determined by the lowest operating frequency and is typically the same as the blocking capacitor value. For long V_{CC} lines, additional bypassing may be necessary.

Table 1. Typical Scattering Parameters

(V_{CC} = +5V, Z_0 = 50Ω, T_A = +25°C.)

FREQUENCY (GHz)	S11 (mag)	S11 (ang)	S21 (dB)	S21 (mag)	S21 (ang)	S12 (dB)	S12 (mag)	S12 (ang)	S22 (mag)	S22 (ang)	K
0.05	0.17	-3	19.8	9.76	177	-37.8	0.013	8	0.42	-5	3.18
0.10	0.17	-6	19.8	9.72	172	-36.7	0.015	14	0.39	-6	2.92
0.20	0.16	9	19.7	9.69	161	-35.8	0.016	23	0.37	-13	2.70
0.30	0.14	8	19.7	9.70	151	-35.0	0.018	28	0.35	-19	2.54
0.40	0.16	0	19.6	9.52	140	-33.8	0.020	32	0.32	-26	2.31
0.50	0.16	-7	19.5	9.43	129	-33.2	0.022	34	0.28	-34	2.24
0.60	0.17	-17	19.3	9.21	119	-32.3	0.024	37	0.25	-43	2.12
0.70	0.18	-26	19.0	8.93	107	-31.7	0.026	41	0.21	-53	2.09
0.80	0.18	-39	18.6	8.46	95	-31.1	0.028	44	0.17	-62	2.10
0.90	0.20	-54	18.0	7.92	84	-29.5	0.033	48	0.13	-71	1.91
1.00	0.20	-66	17.4	7.40	73	-28.7	0.037	50	0.10	-76	1.88
1.20	0.19	-86	15.7	6.10	51	-26.9	0.045	52	0.05	-49	1.88
1.40	0.16	-86	13.4	4.69	31	-25.5	0.053	51	0.12	-12	2.03
1.60	0.15	-66	10.6	3.40	14	-24.4	0.060	44	0.24	-17	2.32
1.80	0.22	-40	7.4	2.35	5	-24.4	0.060	32	0.35	-27	3.01
2.00	0.33	-36	4.6	1.70	4	-25.3	0.055	22	0.43	-33	3.97
2.20	0.41	-38	3.1	1.43	6	-26.5	0.047	21	0.46	-33	4.85
2.40	0.44	-37	2.5	1.34	6	-28.6	0.037	22	0.49	-29	6.26
2.50	0.44	-37	2.3	1.30	4	-29.5	0.034	22	0.49	-25	7.05

Detailed Description

The MAX2650 is a broadband amplifier with flat gain and 50Ω input and output ports. Its small size and internal bias circuitry make it ideal for applications where board space is limited.

Applications Information

External Components

As shown in the *Typical Operating Circuit*, the MAX2650 is easy to use. Input and output series capacitors may be necessary to block DC bias voltages (generated by the MAX2650) from interacting with adjacent circuitry. These capacitors must be large enough to contribute negligible reactance in a 50Ω system at the minimum operating frequency. Use the following equation to calculate their minimum value:

$$C_{BLOCK} = \frac{53{,}000}{f} \text{ (pF)}$$

where f (in MHz) is the minimum operating frequency.

The V_{CC} pin must be RF bypassed for correct operation. To accomplish this, connect a capacitor between the V_{CC} pin and ground, as close to the package as is practical. Use the same equation given above (for DC blocking capacitor values) to calculate the minimum capacitor value. If there are long V_{CC} lines on the PC board, additional bypassing may be necessary. This may be done further away from the package, at your discretion.

Proper grounding of the GND pin is essential. If the PC board uses a topside RF ground, the GND pin should connect directly to it. For a board where the ground plane is not on the component side, the best technique is to connect the GND pin to it through multiple plated through-holes.

PC Board Layout Example

An example PC board layout is given in Figure 1. It uses FR-4 with 31mil layer thickness between the RF lines and the ground plane. The board satisfies all the above requirements.

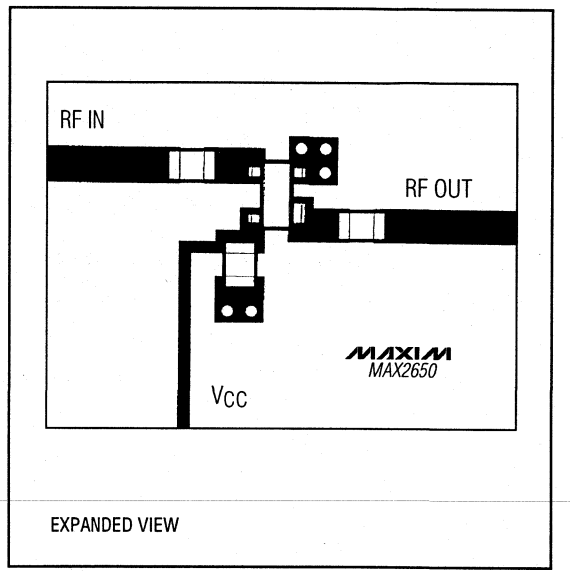
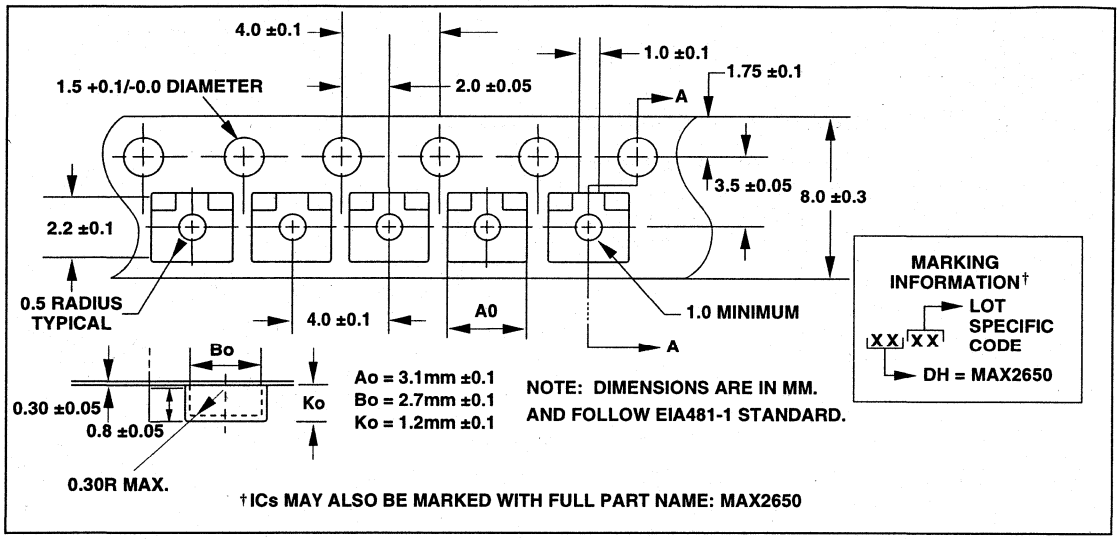


Figure 1. Example PC Board Layout

DC-to-Microwave, +5V Low-Noise Amplifier
+5V Low-Noise Amplifier

Tape-and-Reel/Marking Information



Fiber/Cable Products

Fiber/Cable Products, Product Table 12-2

MAX3263 Single 5V, Fully Integrated, 155Mbps Laser Diode Driver 12-3

MAX3664 622Mbps, Ultra-Low-Power, 3.3V Transimpedance Preamp for SDH/SONET 12-11

MAX3681 +3.3V, 622Mbps, SDH/SONET 1:4 Deserializer with LVDS Outputs 12-23

MAX3761 Low-Power, 622Mbps Limiting Amplifier with TTL Outputs and Chatter-Free Power Detector for LANs 12-31

MAX3762 Low-Power, 622Mbps Limiting Amplifier with PECL Outputs and Chatter-Free Power Detector for LANs 12-31

Regulated Telecommunications

Part Number	Supply Voltage (V)	Analog Bandwidth (MHz)	Transimpedance (kΩ)	Input Noise (nA)	Supply Current (mA)	Pins-Package	Features	Applications
TRANSIMPEDANCE PREAMPLIFIERS								
MAX3664	3.0 to 3.6	590	6	55	25	8-SO, 8-µMAX 8-Die	3.0V to 3.6V V_{CC} range, specified from -40°C to +85°C	622Mbps SDH/SONET

Part Number	Supply Voltage (V)	Input Data Rate (Msps)	Output Data Rate (Msps)	Supply Current (mA)	Clock and Data Inputs	Data Outputs and Synchronization Inputs	Features	Applications
DESERIALIZERS								
MAX3681	3.0 to 3.6	622	155	80	Differential 3.3V PECL	LVDS	24-pin SSOP package, LVDS output reduces power consumption	622Mbps SDH/SONET

Part Number	Supply Voltage (V)	Data Rate (Mbps)	I/O Levels	Bellcore Jitter Tolerance	Pins-Package	Features	Applications
CLOCK RECOVERY AND DATA RETIMING ICs							
MAX3270	+5 & -5	155 or 622	ECL	Surpasses specification	44-MQFP	Selectable data rate, fully integrated PLL, no external reference clock required	622Mbps SDH/SONET, 155Mbps SDH/SONET

Local Area Network and Data Communications Products

Part Number	Supply Voltage (V)	Analog Bandwidth (GHz)	Trans-impedance (Ω)	Max Input (µA)	Input Noise (nA)	Pins-Package	Features	Applications
TRANSIMPEDANCE PREAMPLIFIERS								
MAX3260	+5	1.0	2000	900	240	Die only	Single supply, 25dB dynamic range, optimized for TO header	Fibre Channel, 622Mbps ATM/SDH/SONET

Part Number	Supply Voltage (V)	Input Sensitivity (mV)	Min LOS Sensitivity (mV)	Edge Speed (ps)	Pins-Package	Features	Applications
LIMITING POSTAMPLIFIERS							
MAX3262	+5	6	5	250	24-SSOP	900MHz bandwidth, programmable LOS threshold, single supply	Fibre Channel, 622Mbps ATM/SDH/SONET, 1Gbps Ethernet
MAX3761†	+5	4	3.2	250	20-QSOP	Chatter-free power detector, TTL LOS interface	Fibre Channel, 622Mbps ATM/SDH/SONET, 1Gbps Ethernet
MAX3762†	+5	4	3.2	250	20-QSOP	Chatter-free power detector, PECL LOS interface	Fibre Channel, 622Mbps ATM/SDH/SONET, 1Gbps Ethernet

Part Number	Supply Voltage (V)	Data Rate (Mbps)	Max Modulation Current (mA)	Max Bias Current (mA)	Pins-Package	Features	Applications
LASER DIODE DRIVERS							
MAX3261	+5	1200	25	60	32-TQFP	Automatic power control, single supply, temperature-compensated reference voltage	Fibre Channel, 622Mbps ATM/SDH/SONET
MAX3263	+5	155	25	60	24-SSOP	Automatic power control, single supply, temperature-compensated reference voltage	155Mbps ATM/SDH/SONET

† Future product—contact factory for pricing and availability. Specifications are preliminary.

19-0432; Rev 0; 9/95

EVALUATION KIT AVAILABLE

MAXIM

Single +5V, Fully Integrated, 155Mbps Laser Diode Driver

General Description

The MAX3263 is a complete, easy-to-program, single +5V-powered, 155Mbps laser diode driver with complementary enable inputs and Automatic Power Control (APC). It accepts differential PECL inputs and provides complementary output currents. A temperature-stabilized reference voltage is provided to simplify laser current programming. This allows modulation current to be programmed from 5mA to 25mA and bias current to be programmed from 5mA to 60mA with two external resistors.

An APC circuit is provided to maintain constant laser power in transmitters that use a monitor photodiode. Only one external resistor is required to implement the APC function.

The MAX3263's fully integrated feature set includes a TTL-compatible laser failure indicator and a programmable slow-start circuit to prevent laser damage. The slow-start is preset to 50ns and can be extended by adding an external capacitor.

Features

- ♦ **Rise Times Less than 1ns**
- ♦ **Differential PECL Inputs**
- ♦ **Single +5V Supply**
- ♦ **Automatic Power Control**
- ♦ **Temperature-Compensated Reference Voltage**
- ♦ **Complementary Enable Inputs**

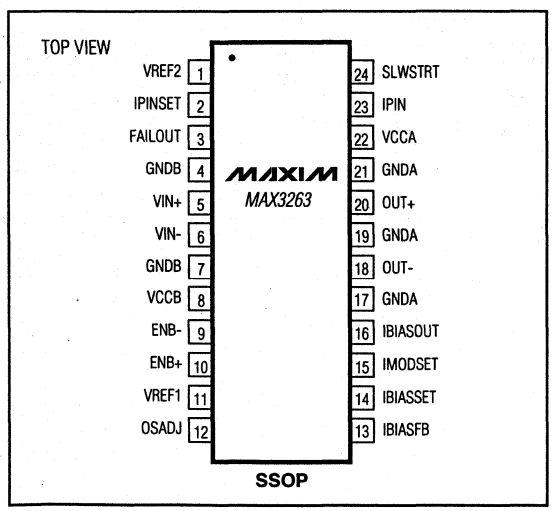
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3263CAG	0°C to +70°C	24 SSOP

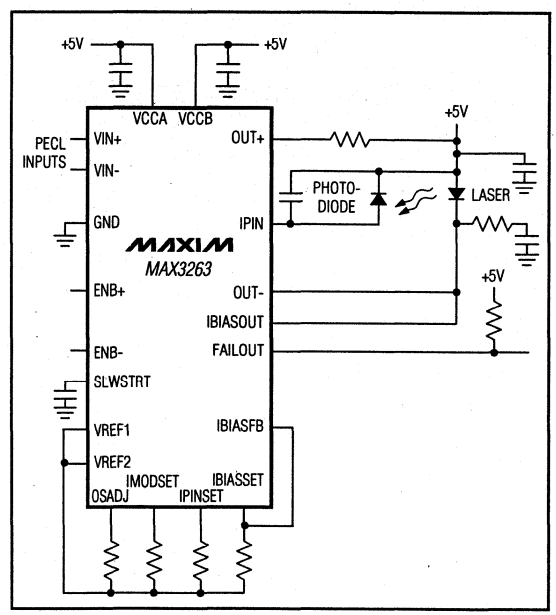
Applications

Laser Diode Transmitters
155Mbps SDH/SONET
155Mbps ATM

Pin Configuration



Typical Operating Circuit



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Single +5V, Fully Integrated, 155Mbps Laser Diode Driver

ABSOLUTE MAXIMUM RATINGS

(V_{CC} = 5.0V, T_A = +25°C, unless otherwise noted.)

Supply Voltages
VCCA, VCCB to GND ..... -0.3V, +6V
IPIN, IPINSET, IMODSET, IBIASET, OSADJ, IBIASFB 5mA
OUT+, OUT-, VREF1, VREF2 ..... +6V
ENB+, ENB- ..... 0V, V_{CC} - 0.3V
FAILOUT ..... 0V, V_{CC}
SLWSTRT ..... +6V
IBIASOUT 90mA
Input Voltage Levels, VIN-, VIN+ ..... 0V, +6V
Continuous Power Dissipation (T_A = +70°C)
SSOP 640mW
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Range of Programmable Laser Bias Current	I_{BIAS}				60	mA
Reference Voltage	V_{REF}	T_A = +25°C	3.15	3.3	3.45	V
Available Reference Current	I_{REF}			15		mA
Supply Current (I_{VCCA} + I_{VCCB})	I_{VCC}	Failout loaded with 1kΩ to V_{CC}			65	mA
PECL Input High		Minimum signal is 550mV, T_A = +25°C	V_{CC} - 1.165			V
PECL Input Low		Minimum signal is 550mV, T_A = +25°C			V_{CC} - 1.475	V
TTL Low (Inputs/Outputs)					0.8	V
TTL High (Inputs/Outputs)			2.0			V

AC ELECTRICAL CHARACTERISTICS

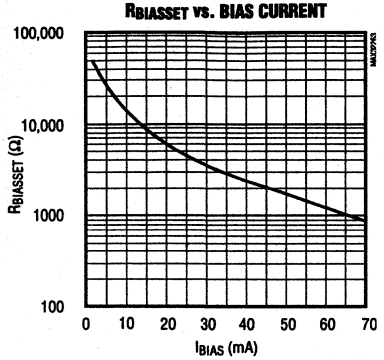
(V_{CC} = 5.0V, R_{LOAD} = 25Ω to +5V, AC parameters are not tested, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Range of Programmable Modulation Current	I_{MOD}	Minimum input signal is 550mV			25	mA
Modulation-Current Rise and Fall Time	t_r, t_f	I_{BIAS} = 25mA, I_{MOD} = 12mA, 8ns period, 10% to 90%			1	ns
Aberrations, Rising and Falling Edge	OS	I_{MOD} = 12mA		±15		%
Modulation-Current Pulse-Width Distortion	PWD	I_{BIAS} = 25mA, I_{MOD} = 12mA, 8ns period			100	ps

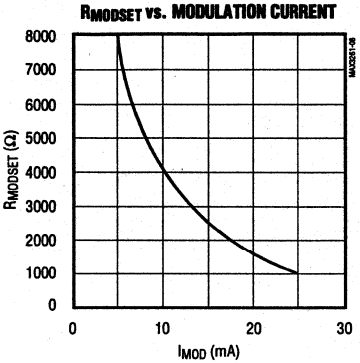
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

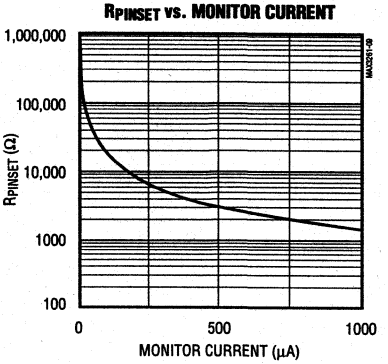
$R_{BIASSET}$ vs. BIAS CURRENT



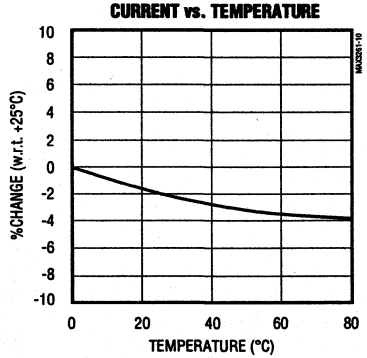
R_{MODSET} vs. MODULATION CURRENT



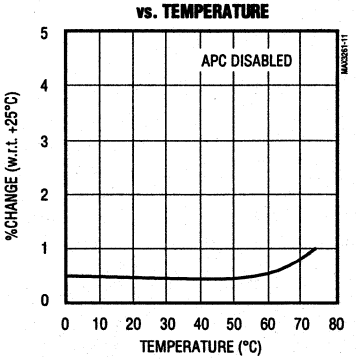
R_{PINSET} vs. MONITOR CURRENT



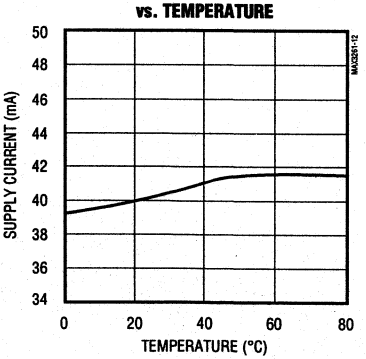
PERCENT CHANGE IN MODULATION CURRENT vs. TEMPERATURE



BIAS CURRENT STABILITY vs. TEMPERATURE



SUPPLY CURRENT vs. TEMPERATURE



12

Single +5V, Fully Integrated, 155Mbps Laser Diode Driver

Pin Description

PIN	NAME	FUNCTION
1, 11	VREF2, VREF1	Temperature-Compensated References
2	IPINSET	Current Input for APC, proportional to monitor diode current.
3	FAILOUT	Open-Collector TTL Output. Asserts low when monitor diode current is less than I_{PINSET}.
4, 7	GNDB	Ground for VREF and APC
5	VIN+	Positive PECL Input
6	VIN-	Negative PECL Input
8	VCCB	Positive supply for VREF and APC
9, 10	ENB-, ENB+	TTL Inputs to Enable Output Currents
12	OSADJ	Sets current for laser driver input stage.
13	IBIASFB	Output from APC Circuit, used to set laser bias current.
14	IBIASSET	Sets laser bias current.
15	IMODSET	Sets laser modulation current.
16	IBIASOUT	Sets laser bias output current.
17, 19, 21	GNDA	Negative Supplies for Output and Bias Driver
18	OUT-	Primary Laser Modulation Output
20	OUT+	Secondary Laser Modulation Output
22	VCCA	Positive Supply for Output and Bias Driver
23	IPIN	Connects to monitor photodiode
24	SLWSTRT	Capacitor Port for Slow Start-Up

Detailed Description

The MAX3263 laser driver has three main sections: a reference generator with temperature compensation, a laser bias block with automatic power control, and a modulation driver.

The reference generator provides temperature-compensated biasing and a voltage-reference output. The voltage reference is used to program the current levels of the modulation driver, laser diode, and PIN (p+, intrinsic, n-) monitor diode.

The laser bias block sets the bias current in the laser diode and maintains it above the threshold point. A current-controlled current source (current mirror) programs the bias, with IBIASSET as the input. The mirror's gain is approximately 40 over the MAX3263's input range. Keep the output voltage of the bias stage above 2.6V to prevent saturation.

The modulation driver consists of an input buffer and a common-emitter differential output stage. The modulation current mirror sets the laser modulation current in the output stage. This current is switched between the OUT+ and OUT- ports of the laser driver. The modulation current mirror has a gain of approximately 20.

The overshoot mirror sets the bias in the input buffer stage. Reducing this current slows the input stage and reduces overshoot in the modulation signal. At the same time, the peak-to-peak output swing of the input buffer stage is reduced. Careful design must be used to ensure that the buffer stage can switch the output stage completely into the nonlinear region (Figure 3). For the output stage, the width of the linear region is a function of the desired modulation current. Increasing the modulation current increases the linear region. Therefore, increases in the modulation current require larger output levels from the first stage. Table 1 shows the maximum allowable R_{OSADJ} (to ensure complete switching) versus the laser modulation-current level.

Failure to ensure that the output stage switches completely results in a loss of modulation current (and extinction ratio). In addition, if the modulation port does not switch completely off, the modulation current will contribute to the bias current, and may complicate module assembly.

Table 1. Optimum R_{OSADJ}

I_{MOD} (mA)	Max R_{OSADJ} (kΩ)
10	7.50
15	6.00
20	5.25
25	4.25
30	3.70

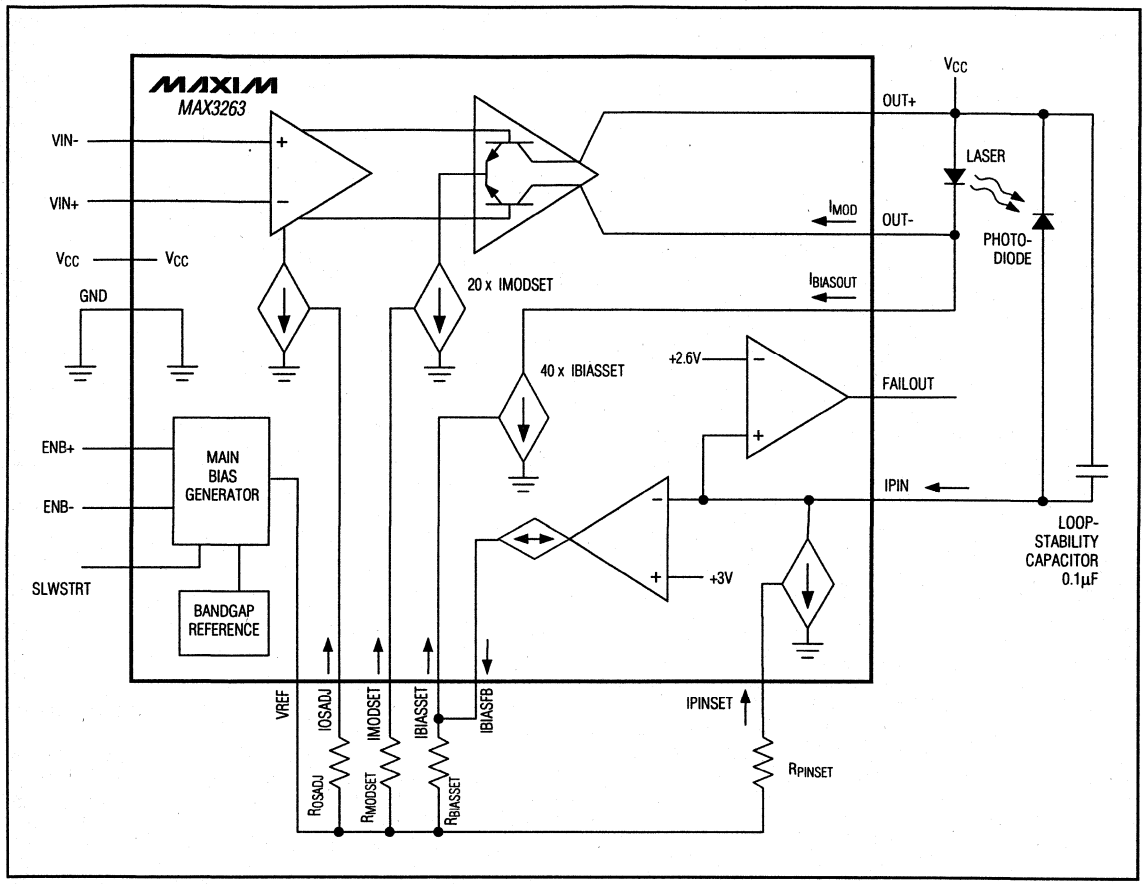


Figure 1. Block Diagram

Automatic Power Control

The automatic power control (APC) feature allows an optical transmitter to maintain constant power, despite changes in laser efficiency with temperature or age. The APC requires the use of a monitor photodiode.

The APC circuit incorporates the laser diode, the monitor photodiode, the IPINSET current mirror, a transconductance amplifier, the bias set current mirror, and the laser fail comparator (Figure 1). Light produced by the laser diode generates an average current in the monitor photodiode. This current flows into the MAX3263's IPIN input. The IPINSET current mirror draws current away from the IPIN node. When the current into the IPIN node equals the current drawn away by IPINSET, the node voltage is set by the 3V reference of the transconductance amplifier. When the monitor current exceeds IPINSET, the IPIN node voltage will be forced higher. If the monitor current decreases, the IPIN node voltage is decreased. In either case, the voltage change is amplified by the transconductance amplifier, and results in a feedback current at the IBIASFB node. Under normal APC operation, IBIASFB is summed with IBIASSET, and the laser bias level is adjusted to maintain constant output power. This feedback process continues until the monitor-diode current equals IPINSET.

If the monitor-diode current is sufficiently less than IPINSET (i.e., the laser stops functioning), the voltage on the IPIN node drops below 2.6V. This triggers the failout

Single +5V, Fully Integrated, 155Mbps Laser Diode Driver

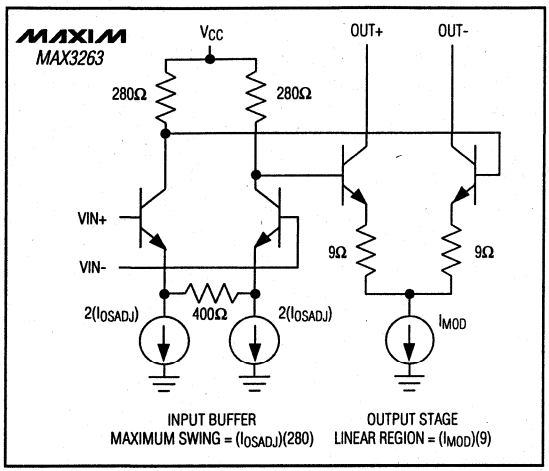


Figure 2. MAX3263 Modulation Driver (Simplified)

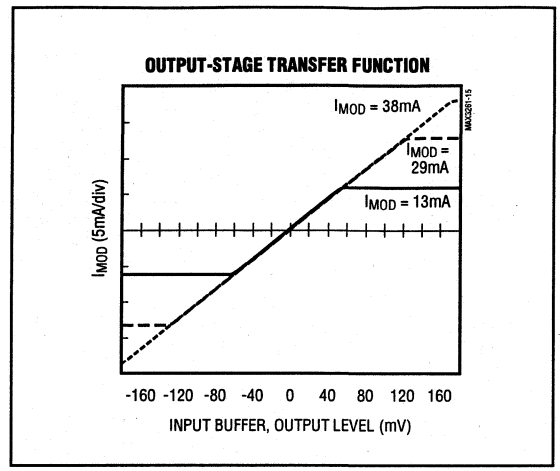


Figure 3. Output-Stage Transfer Function

comparator, which provides a TTL signal indicating laser failure. The FAILOUT output asserts only if the monitor-diode current is low, not in the reverse situation where the monitor current exceeds IPINSET.

The transconductance amplifier can output currents up to approximately ±1mA through the IBIASFB pin. Since the laser bias generator has a gain of approximately 40, the APC function has a limit of approximately 40mA (up or down) from the initial set point. To take full advantage of this adjustment range, it may be prudent to program the laser bias current slightly higher than required for normal operation.

To maintain APC loop stability, a 0.1µF bypass capacitor may be required across the photodiode. If the APC function is not used, disconnect the IBIASFB pin.

The time constant of the APC is set by the loop-stability capacitor. The IPIN input impedance is 80Ω.

Enable Inputs

The MAX3263 provides complementary enable inputs (ENB+, ENB-). Laser control is achieved by reducing the reference voltage outputs (VREF1, VREF2). Only one logic state enables laser operation (Table 2).

Table 2. MAX3263 Truth Table

ENB-	ENB+	VREF
0	0	Off
0	1	On
1	0	Off
1	1	Off

Temperature Considerations

The MAX3263 output currents are programmed by current mirrors. These mirrors each have a $2V_{BE}$ temperature coefficient. The reference voltage (VREF) is adjusted $2V_{BE}$ so these changes largely cancel, resulting in output currents that are very stable with respect to temperature (see *Typical Operating Characteristics*).

Design Procedure

Interfacing Suggestions

Use high-frequency design techniques for the board layout of the MAX3263 laser driver. Minimize any series inductance to the laser, and place a bypass capacitor as close to the laser's anode as possible.

Power connections labeled VCCA are used to supply the laser modulation and laser bias circuits. VCCB connections supply the bias-generator and automatic-power control circuits. For optimum operation, isolate these supplies from each other by independent bypass filtering.

The MAX3263 inputs interface to PECL (V_{CC}-referenced ECL) signal levels. If the incoming data stream has a 50% duty cycle (NRZ), the inputs can be AC coupled and connected to other differential logic levels. If logic levels other than PECL are used, it is important to bias the modulation inputs (VIN+, VIN-) with a circuit that provides a PECL common-mode voltage (Figure 4).

Bias Network Compensation

For best laser transmitter performance, add a filter to the circuit. Most laser packages (TO-46 or DIL) have a significant amount of package inductance (4nH to 20nH), which limits their usable data rate. The MAX3263 OUT pin has about 1pF of capacitance. These two parasitic components can cause high-frequency ringing and aberrations on the output signal.

If ringing is present on the transmitter output, try adding a shunt RC filter to the laser node. This limits the bandwidth of the transmitter to usable levels, and reduces ringing dramatically.

L = Laser inductance

C = Shunt filter capacitance

R = Shunt filter resistance

A good starting point is R = 25Ω and C = L / 4R. Increase C until aberrations are reduced.

The IBIASOUT pin has about 4pF of parasitic capacitance. When operating at bias levels over 50mA, the impedance of the bias output may be low enough to decrease the rise time of the transmitter. If this occurs, the impedance of the IBIASOUT pin can be increased by adding a large inductor in series with the pin. A 47µH inductor with a self-resonant frequency of 1MHz should work well in any application.

Reducing Power Consumption

The laser driver typically consumes 40mA of current for internal functions. Typical load currents, such as 12mA of modulation current and 20mA of bias current, bring the total current requirement to 72mA. If this were dissipated entirely in the laser driver, it would generate 360mW of heat. Fortunately, a substantial portion of this power is dissipated across the laser diode. A typical laser diode drops approximately 1.6V when forward biased. This leaves 3.4V at the MAX3263's OUT- terminal. It is safe to reduce the output terminal voltage even further with a series damping resistor. Terminal voltage levels down to 2.2V can be used without degrading the laser driver's high-frequency performance. Power dissipation can be further reduced by adding a series resistor on the laser driver's OUT+ side. Select the series resistor so the OUT+ terminal voltage does not drop below 2.2V with the maximum modulation current.

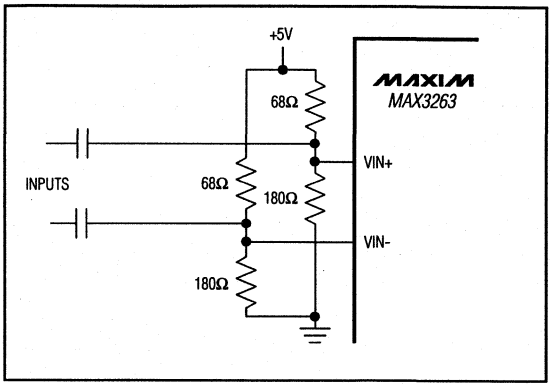


Figure 4. Driving the MAX3263 with Non-PECL Levels

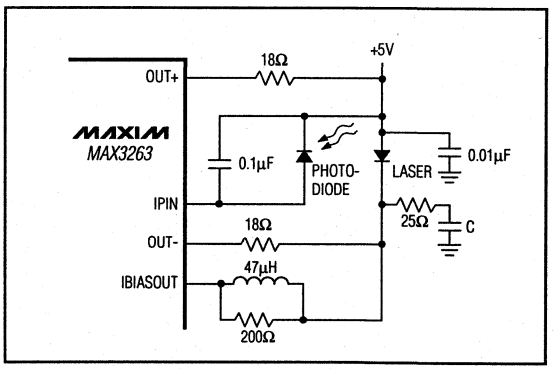


Figure 5. Typical Laser Interface with Bias Compensation

Applications Information

Programming the MAX3263 Laser Driver

Programming the MAX3263 is best explained by an example. Assume the following laser diode characteristics:

Wavelength	λ	1300nm
Threshold Current	I_{TH}	20mA at +25°C(+0.35mA/°C temperature variation)
Monitor Responsivity	ρmon	0.1A/W (monitor current / average optical power into the fiber)

12

Single +5V, Fully Integrated, 155Mbps Laser Diode Driver

Modulation Efficiency η		0.1mW/mA (worst case)

Now assume the communications system has the following requirements:

Average Power	P_{AVE}	0dBm (1mW)
Extinction Ratio	Er	6dB (Er = 4)
Temperature Range	Tr	0°C to +70°C

1) Determine the value of IPINSET:

The desired monitor-diode current is $(P_{AVE})(\rho_{mon})$ = (1mW)(0.1A/W) = 100µA. The *Typical Operating Characteristics* show that R_{PINSET} should be 18kΩ.

2) Determine R_{MODSET}:

The average power is defined as (P1 + P0) / 2, where P1 is the average amplitude of a transmitted "one" and P0 is the average amplitude of a transmitted "zero." The extinction ratio is P1/P0. Combining these equations results in P1 = (2 x P_{AVE} x Er) / (Er + 1) and P0 = (2 x P_{AVE}) / (Er + 1). In this example, P1 = 1.6mW and P0 = 0.4mW. The optical modulation is 1.2mW. The modulation current required to produce this output is 1.2mW / η = (1.2mW) / (0.1mA/mW) = 12mA. The *Typical Operating Characteristics* show that R_{MODSET} = 3kΩ yields the desired modulation current.

3) Determine the value of R_{OSADJ}:

Using Table 1, a 6.8kΩ resistor is chosen for 12mA of modulation current. The values given in Table 1 minimize aberrations in the waveform and ensure that the driver stage operates fully limited.

4) Determine the value of $R_{BIASSET}$:

The automatic power control circuit can adjust the bias current 40mA from the initial setpoint. This feature makes the laser driver circuit reasonably insensitive to variations of laser threshold from lot to lot. The bias setting can be determined using one of two methods:

A) Set the bias at the laser threshold.

B) Set the bias at the midpoint of the highest and lowest expected threshold values.

Method A is straightforward. In the second method, it is assumed that the laser threshold will increase with age.

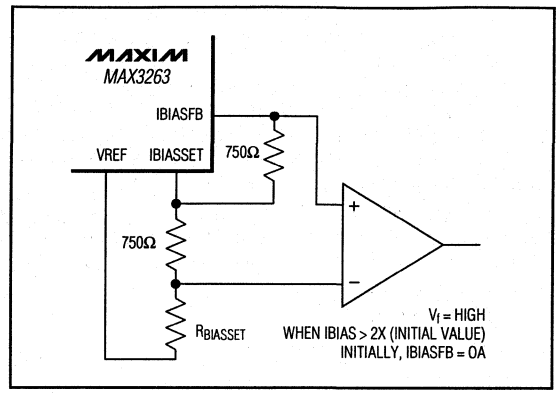


Figure 6. End-of-Life Indicator

The lowest threshold current occurs at 0°C, when the laser is new. The highest threshold current occurs at +70°C, at the end of the product's life. Assume the laser is near the end of life when its threshold reaches two-times its original value.

Lowest Bias Current:

$I_{TH} + \Delta I_{TH}$ = 20mA + (0.35mA/°C)(-25°C) = 11.25mA

Highest Bias Current:

2 x $I_{TH} + \Delta I_{TH}$ = 40mA + (0.35mA/°C)(+45°C) = 55.8mA

In this case, set the initial bias value to 34mA (which is the midpoint of the two extremes). The 40mA adjustment range of the MAX3263 maintains the average laser power at either extreme.

The *Typical Operating Characteristics* show that $R_{BIASSET}$ = 1.8kΩ delivers the required bias current.

End-of-Life Indicator

Some applications require a failout flag (end-of-life indicator) to be set when the laser bias current reaches two-times its original setting. A simple comparator circuit monitoring IBIASFB and IBIASSET can be implemented to provide this type of failout signal (Figure 6).

19-0479; Rev 0; 3/96

EVALUATION KIT AVAILABLE

MAXIM

622Mbps, Ultra-Low-Power, 3.3V Transimpedance Preamplifier for SDH/SONET

General Description

The MAX3664 low-power transimpedance preamplifier for 622Mbps SDH/SONET applications consumes only 85mW. Operating from a single +3.3V supply, it converts a small photodiode current to a measurable differential voltage. A DC cancellation circuit provides a true differential output swing over a wide range of input current levels, thus reducing pulse-width distortion. The differential outputs are back-terminated with 60Ω per side.

The transimpedance gain is nominally 6kΩ. For input signal levels beyond approximately 100µAp-p, the amplifier will limit the output swing to 900mV. The MAX3664's low 55nA input noise provides a typical sensitivity of -33.2dBm in 1300nm, 622Mbps receivers.

The MAX3664 is designed to be used in conjunction with the MAX3675 clock recovery and data retiming IC with limiting amplifier. Together, they form a complete 3.3V, 622Mbps SDH/SONET receiver.

In die form, the MAX3664 is designed to fit on a header with a PIN diode. It includes a filter connection, which provides positive bias for the photodiode through a 1kΩ resistor to V_{CC}. The device is also available in 8-pin SO and µMAX packages.

Applications

SDH/SONET Receivers

PIN/Preamplifier Receivers

Regenerators for SDH/SONET

Features

- ♦ **Single +3.3V Supply Operation**
- ♦ **55nA$_{RMS}$ Input-Referred Noise**
- ♦ **6kΩ Gain**
- ♦ **85mW Power**
- ♦ **300µA Peak Input Current**
- ♦ **200ps Max Pulse-Width Distortion**
- ♦ **Differential Output Drives 100Ω Load**
- ♦ **590MHz Bandwidth**

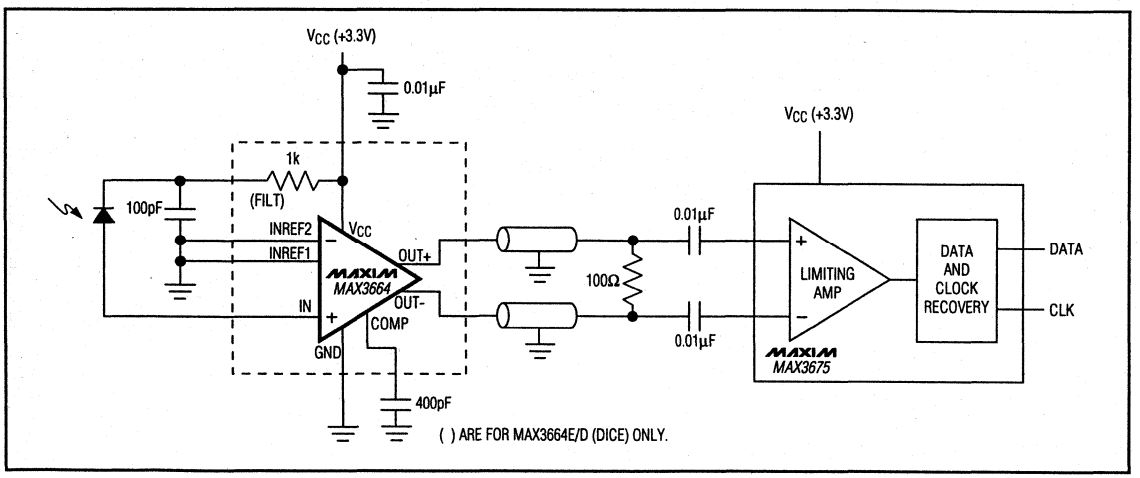
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3664E/D	-40°C to +85°C	Dice
MAX3664ESA	-40°C to +85°C	8 SO
MAX3664EUA*	-40°C to +85°C	8 µMAX

** Contact factory for package availability.*

Pin Configuration appears at end of data sheet.

Typical Application Circuit



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

622Mbps, Ultra-Low-Power, 3.3V Transimpedance Preamplifier for SDH/SONET

ABSOLUTE MAXIMUM RATINGS

V_{CC} .....-0.5V to +5.5V
Continuous Current
IN, INREF1, INREF2, COMP, FILT.....5mA
OUT+, OUT-.....25mA
Continuous Power Dissipation (T_A = +85°C)
SO (derate 5.88mW/°C above +85°C).....383mW
µMAX (derate 4.1mW/°C above +85°C) 268mW
Operating Junction Temperature (die).....-55°C to +175°C
Processing Temperature (die).....+400°C
Storage Temperature Range.....-65°C to +160°C
Lead Temperature (soldering, 10sec).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.3V ±0.3V, COMP = GND, 100Ω load between OUT+ and OUT-, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Bias Voltage	V_{IN}	I_{IN} = 0µA to 300µA		0.8	0.95	V
Gain Nonlinearity		I_{IN} = 0µA to 20µA			±5	%
Supply Current	I_{CC}	I_{IN} = 0µA	12	25	35	mA
Small-Signal Transimpedance	z_{21}	Differential output	4.5	6	7.5	kΩ
Output Common-Mode Level				V_{CC} - 1.3		V
Power-Supply Rejection Ratio	PSRR	f < 1MHz, referred to output	20			dB
Differential Output Offset	ΔV_{OUT}	I_{IN} = 200µA, C_{COMP} = 400pF		±7		mV
Output Impedance (per side)	Z_{OUT}		40	60	75	Ω
Maximum Output Voltage	V_{OUT}(max)	I_{IN} = 300µA			950	mV
Filter Resistor (die only)	R_{FILT}		800	1000	1200	Ω

Note 1: Dice are tested at T_j = +27°C.
Note 2: µMAX package tested at T_A = 0°C to +85°C.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.3V ±0.3V, C_{COMP} = 400pF, C_{IN} = 1.1pF, outputs terminated into 50Ω, 8-pin SO package in MAX3664 EV board, T_A = +25°C, unless otherwise noted.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small-Signal Bandwidth	BW-3dB	Relative to gain at 10MHz		590		MHz
Low-Frequency Cutoff					150	kHz
Pulse-Width Distortion (Note 5)	PWD	2µA to 100µA peak input current, 50% duty cycle, 1–0 pattern		6	100	ps
		100µA to 300µA peak input current, 50% duty cycle, 1–0 pattern		80	200	
RMS Noise Referred to Input	i_n	C_{IN} = 0.3pF (Note 6), I_{IN} = 0µA		55		nA
		C_{IN} = 1.1pF (Note 6), I_{IN} = 0µA		73	86	

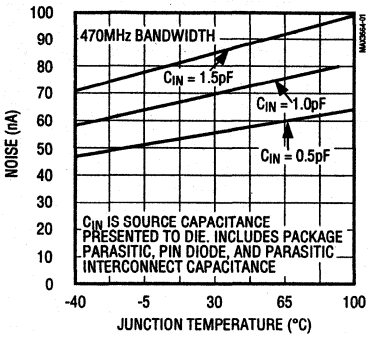
Note 3: AC Characteristics are guaranteed by design.
Note 4: C_{IN} is the total capacitance at IN.
Note 5: $PWD = \left| \frac{2 \times \text{Pulse width} - \text{Period}}{2} \right|$
Note 6: DC to 470MHz, measured with 3-pole Bessel filter at output.

622Mbps, Ultra-Low-Power, 3.3V Transimpedance Preamplifier for SDH/SONET

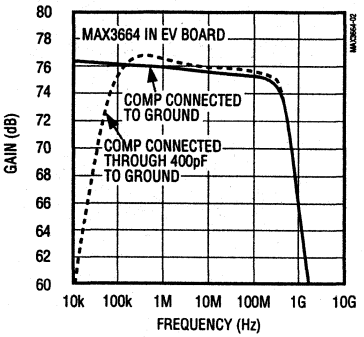
Typical Operating Characteristics

(V_{CC} = +3.3V, C_{COMP} = 400pF, T_A = +25°C, unless otherwise noted.)

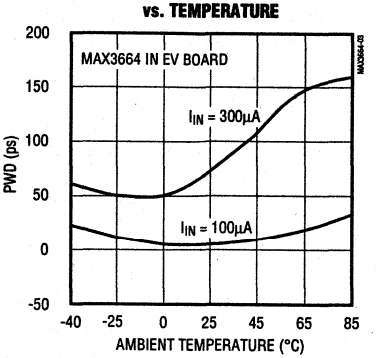
INPUT-REFERRED NOISE vs. TEMPERATURE



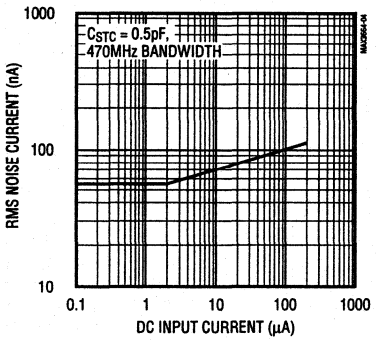
SMALL-SIGNAL GAIN vs. FREQUENCY



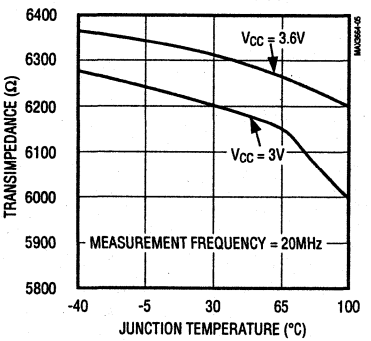
PULSE-WIDTH DISTORTION vs. TEMPERATURE



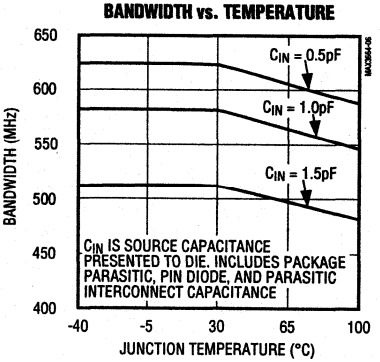
INPUT-REFERRED RMS NOISE CURRENT vs. DC INPUT CURRENT



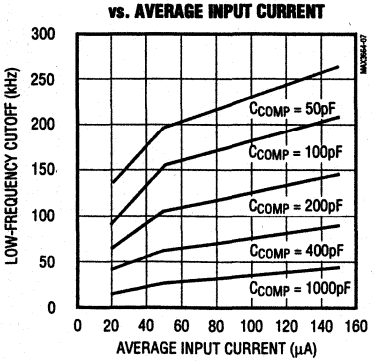
SMALL-SIGNAL TRANSIMPEDANCE vs. TEMPERATURE



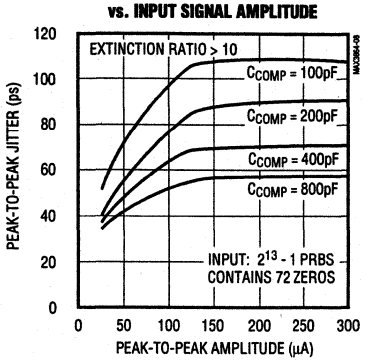
BANDWIDTH vs. TEMPERATURE



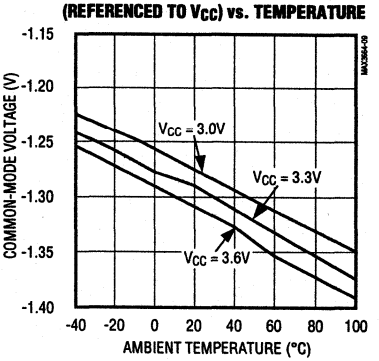
LOW-FREQUENCY CUTOFF vs. AVERAGE INPUT CURRENT



DATA-DEPENDENT JITTER vs. INPUT SIGNAL AMPLITUDE



OUTPUT COMMON-MODE VOLTAGE (REFERENCED TO V_{CC}) vs. TEMPERATURE



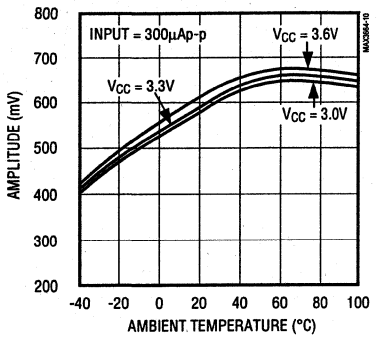
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622Mbps, Ultra-Low-Power, 3.3V Transimpedance Preamplifier for SDH/SONET

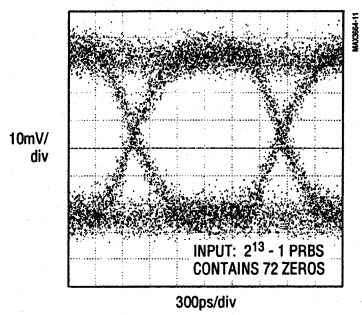
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, C_{COMP} = 400pF, T_A = +25°C, unless otherwise noted.)

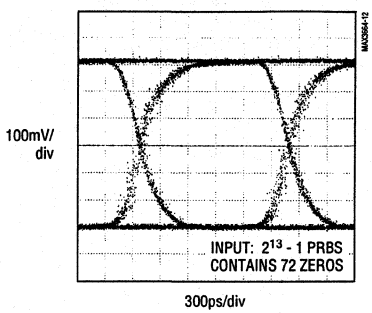
OUTPUT AMPLITUDE vs. TEMPERATURE



EYE DIAGRAM (INPUT = 10µAp-p)



EYE DIAGRAM (INPUT = 300µAp-p)



Pin Description

PIN	NAME	FUNCTION
1	V_{CC}	+3.3V Supply Voltage
2	IN	Signal Input
3, 4	INREF1, INREF2	Input References 1 and 2. Connect to photodetector AC ground.
5	GND	Ground
6	OUT+	Noninverting Voltage Output. Current flowing into IN causes V_{OUT+} to increase.
7	OUT-	Inverting Voltage Output. Current flowing into IN causes V_{OUT-} to decrease.
8	COMP	External Compensation Capacitor for DC cancellation loop. Connect 400pF or more from COMP to GND for normal operation. Connect COMP directly to GND to disable the DC cancellation loop.
—	FILT*	Filter Connection. Provides positive bias for photodiode through a 1kΩ resistor to V_{CC}. See *Step 3: Designing Filters*. (This pad is accessible on the die only.)

* MAX3664E/D (die) only.

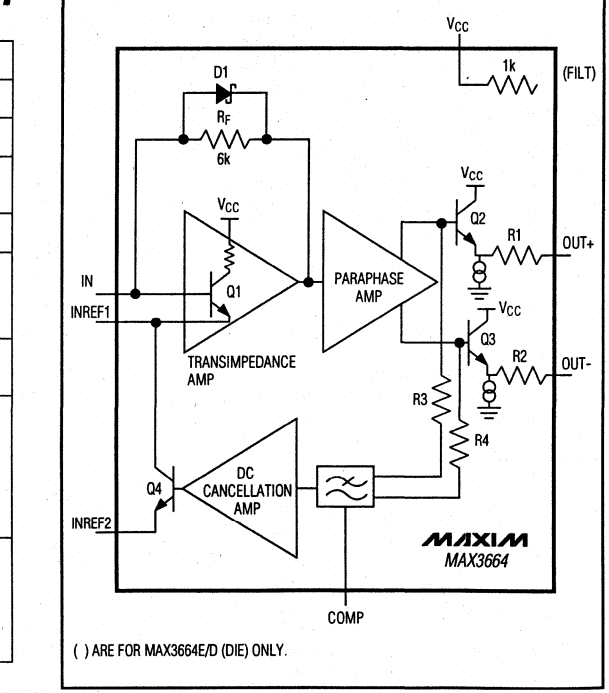


Figure 1. Functional Diagram

622Mbps, Ultra-Low-Power, 3.3V Transimpedance Preamplifier for SDH/SONET

Detailed Description

The MAX3664 is a transimpedance amplifier designed for 622Mbps SDH/SONET applications. It comprises a transimpedance amplifier, a paraphase amplifier with emitter-follower outputs, and a DC cancellation loop. Figure 1 is a functional diagram of the MAX3664.

Transimpedance Amplifier

The signal current at IN flows into the summing node of a high-gain amplifier. Shunt feedback through R_F converts this current to a voltage with a gain of 6kΩ. Diode D1 clamps the output voltage for large input currents. INREF1 is a direct connection to the emitter of the input transistor, and must be connected directly to the photodetector AC ground return for best performance.

Paraphase Amplifier

The paraphase amplifier converts single-ended inputs to differential outputs, and introduces a voltage gain of 2. This signal drives a pair of internally biased emitter followers, Q2 and Q3, which form the output stage. Resistors R1 and R2 provide back-termination at the output, absorbing reflections between the MAX3664 and its load.

The output emitter followers are designed to drive a 100Ω differential load between OUT+ and OUT-. They can also drive higher output impedances, resulting in increased gain and output voltage swing.

DC Cancellation Loop

The DC cancellation loop removes the DC component of the input signal by using low-frequency feedback. This feature centers the signal within the MAX3664's dynamic range, reducing pulse-width distortion on large input signals.

The output of the paraphase amplifier is sensed through resistors R3 and R4 and then filtered, amplified, and fed back to the base of transistor Q4. The transistor draws the DC component of the input signal away from the transimpedance amplifier's summing node.

The COMP pin sets the DC cancellation loop's response. Connect 400pF or more between COMP and GND for normal operation. Connect the pin directly to GND to disable the loop. The DC cancellation loop can sink up to 300µA of current at the input. When operated with C_{COMP} = 400pF, the loop takes approximately 20µs to stabilize.

The MAX3664 minimizes pulse-width distortion for data sequences that exhibit a 50% duty cycle. A duty cycle other than 50% causes the device to generate pulse-width distortion.

DC cancellation current is drawn from the input and adds noise. For low-level signals with little or no DC component, this is not a problem. Preamplifier noise will increase for signals with significant DC component.

Applications Information

The MAX3664 is a low-noise, wide-bandwidth transimpedance amplifier that is ideal for 622Mbps SDH/SONET receivers. Its features allow easy design into a fiber optic module, in four simple steps.

Step 1: Selecting a Preamplifier for a 622Mbps Receiver

Fiber optic systems place requirements on the bandwidth, gain, and noise of the transimpedance preamplifier. The MAX3664 optimizes these characteristics for SDH/SONET receiver applications that operate at 622Mbps.

In general, the bandwidth of a fiber optic preamplifier should be 0.6 to 1 times the data rate. Therefore, in a 622Mbps system, the bandwidth should be between 375MHz and 622MHz. Lower bandwidth causes pattern-dependent jitter and a lower signal-to-noise ratio, while higher bandwidth increases thermal noise. The MAX3664 typical bandwidth is 590MHz, making it ideal for 622Mbps applications.

The preamplifier's transimpedance must be high enough to ensure that expected input signals generate output levels exceeding the sensitivity of the limiting amplifier (quantizer) in the following stage. The MAX3675 clock recovery and limiting amplifier IC has an input sensitivity of 3.6mVp-p, which means that 3.6mVp-p is the minimum signal amplitude required to produce a fully limited output. Therefore, when used with the MAX3664, which has a 6kΩ transimpedance, the minimum detectable photodetector current is 600nA.

It is common to relate peak-to-peak input signals to average optical power. The relationship between optical input power and output current for a photodetector is called the responsivity (ρ), with units Amperes/Watt (A/W). The photodetector peak-to-peak current is related to the peak-to-peak optical power as follows:

$$I_{p-p} = (P_{p-p})(\rho)$$

Based on the assumption that SDH/SONET signals maintain a 50% duty cycle, the following equations relate peak-to-peak optical power to average optical power and extinction ratio (Figure 2):

Average Optical Power = P_{AVE} = (P0 + P1) / 2

Extinction Ratio = r_e = P1 / P0

Peak-to-Peak Signal Amplitude = Pp-p = P1 - P0

Therefore,

$$P_{AVE} = P_{p-p}\,(1/2)[(r_e + 1)/(r_e - 1)]$$

622Mbps, Ultra-Low-Power, 3.3V Transimpedance Preamplifier for SDH/SONET

In a system where the photodiode responsivity is 0.9A/W and the extinction ratio is 10, the MAX3664/MAX3675 receiver with 670nA gain sensitivity will deliver a fully limited output for signals of average optical power larger than:

(600nA / 0.9A/W)(1 / 2)(11 / 9) = 407nW ⇒ -33.9dBm

Sensitivity is a key specification of the receiver module. The ITU/Bellcore specifications for SDH/SONET receivers require a link sensitivity of -27dBm with a bit error rate (BER) of 1E - 10. There is an additional 1dB power penalty to accommodate various system losses; therefore, the sensitivity of a 622Mbps receiver must be better than -28dBm.

Although several parameters affect sensitivity (such as the quantizer sensitivity and preamplifier gain, as previously discussed), most fiber optic receivers are designed so that noise is the dominant factor. Noise from the high-gain transimpedance amplifier, in particular, determines the sensitivity. The noise generated by the MAX3664 can be modeled with a Gaussian distribution. In this case, a BER of 1E - 10 corresponds to a peak-to-peak signal amplitude to RMS noise ratio (SNR) of 12.7. The MAX3664's typical input-referred noise, i_n, (bandwidth-limited to 470MHz) is $55nA_{RMS}$. Therefore, the minimum input for a BER of 1E - 10 is (12.7 x 55nA) = 700nAp-p. Rearranging the previous equations in these terms results in the following relation:

$$\text{Optical Sensitivity (dBm)} = -10\log[(i_n / \rho)(SNR)(1/2)(r_e + 1) / (r_e - 1)(1000)]$$

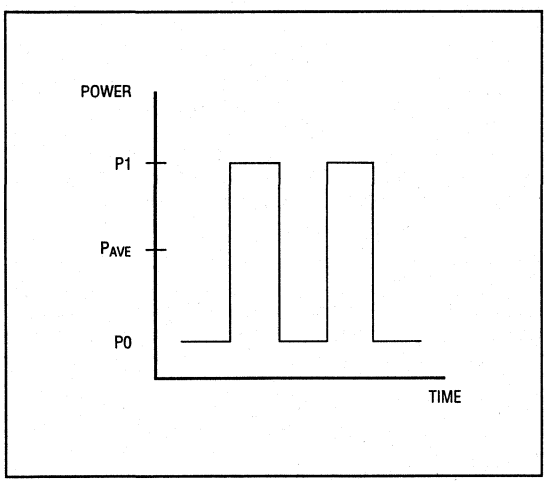


Figure 2. Optical Power Definitions

At room temperature, with r_e = 10, SNR = 12.7, i_n = 55nA, and ρ = 0.9A/W, the MAX3664 sensitivity is -33.2dBm. At +85°C, noise increases to 62nA and sensitivity decreases to -32.7dBm. The MAX3664 provides 4.7dB margin over the SDH/SONET specifications, even at +85°C.

The largest allowable input to an optical receiver is called the input overload. The MAX3664's largest input current (I_{max}) is 300µAp-p, with 200ps of pulse-width distortion. The pulse-width distortion and input current are closely related (see *Typical Operating Characteristics*). If the clock recovery circuit can accept more pulse-width distortion, a higher input current might be acceptable. For worst-case responsivity and extinction ratio, ρ = 1A/W and $r_e = \infty$, the input overload is:

$$\text{Overload (dBm)} = -10\log (I_{max})(1 / 2)(1000)$$

For I_{max} = 300µA, the MAX3664 overload is -8.2dBm.

Step 2: Selecting Time Constants

A receiver built with the MAX3664 will have a bandpass frequency response. The low-frequency cutoff causes unwanted data-dependent jitter and sensitivity loss. Because SDH/SONET data streams contain scrambled data, certain data sequences may generate continuous successions of 1s or 0s. The low-frequency cutoff forces the output of such sequences to zero, ultimately causing a sensitivity reduction. The SDH specifications state that a receiver must be able to handle up to 72 consecutive bits of the same value within the data. Therefore, choose the low-frequency cutoff to ensure an acceptable amount of data-dependent jitter and sensitivity loss.

Determine the reduction in signal-to-noise ratio due to a transitionless sequence of duration t as follows:

$$SNR_{loss} = 1 - e\text{-}t / \tau = 1\text{-}e\text{-}(2\pi f_c t)$$

where τ is the time constant of the offset correction, f_c is the low-frequency cutoff, and t is the time for 72 bits (116ns for a 622Mbps data rate).

Suppose that the receiver should not have more than 0.25dB (6%) of sensitivity loss due to a 72-bit transitionless sequence. This means that:

$$(1 - e\text{-}(2\pi f_c)(116ns)) < 0.06$$

$$f_c = (\ln 0.94) / [(-2\pi)(116ns)] = 85kHz \text{ (max)}$$

The loss of sensitivity is a concern only when the SNR is small (close to 12.7), which occurs with input currents less than 3µAp-p.

The cutoff frequency also affects the data-dependent jitter (DDJ). DDJ due to low-frequency cutoff can be approximated as droop / slope, where the slope in V/sec is measured at the 50% crossing of an eye diagram, and droop is the loss-of-signal to noise calculated above as $1 - e^{-(2\pi f_c t)}$. The slope at the 50% crossing is typically two times the 10% to 90% slope, which is approximately 0.35 / bandwidth. For a 622Mbps receiver with a 470MHz bandwidth, the 10% to 90% rise time is approximately 750ps. The slope through the 50% crossing will be approximately:

Amplitude (2)(0.8) / 750ps =
1.6 Amplitude / 750ps = 2E9 Amplitude V/sec

$$DDJ = 2\,[\text{Amplitude}\,(1 - e^{-(2\pi f_c t)})] / [\,2.0E9\ \text{Amplitude}\,] = (1 - e^{-(2\pi f_c t)}) / (1E9)$$

OR

$$f_c = -\ln[1 - (1.0E9)(DDJ)] / [2\pi t]$$

If the maximum allowable DDJ is 100ps, and t = 112ns for a 72-bit sequence, then the maximum low-frequency cutoff is 150kHz.

Several circuits in the receiver can determine the low-frequency cutoff. In a receiver using the MAX3664 and MAX3675, there are three locations for concern:

1) The MAX3664's DC cancellation circuit.
2) The coupling capacitors between the MAX3664 outputs and MAX3675 inputs.
3) The MAX3675's offset correction circuit.

The highest cutoff frequency in the system determines the amount of data-dependent jitter created.

The time constants of the MAX3675's offset correction and of the coupling capacitors should be separated by a factor of ten (one decade) to prevent low-frequency oscillations.

For example, select the offset correction of the MAX3664 to set the receiver cutoff frequency. Note that the MAX3664's low-frequency cutoff increases with average input current. Since DDJ increases with f_c, it follows that DDJ increases as average input increases. When the input signal is large enough to limit the outputs, however, DDJ does not increase. Therefore, the maximum DDJ results from the lowest input that causes the MAX3664 to have limited outputs (see *Typical Operating Characteristics*), which is about 150µAp-p. When selecting a capacitor for the COMP pin that achieves your desired DDJ, use the data from *Typical Operating Characteristics* at I_{INPUT} = 150µA.

In summary, use the following method to select the low-frequency cutoff that will provide the sensitivity and DDJ required for SDH/SONET receivers:

1) Determine the longest time without transitions.
2) Determine the acceptable loss of SNR ratio, and the acceptable DDJ due to the transitionless time.
3) Estimate the low-frequency cutoff required for either the worst-case SNR loss or for DDJ.
4) Select the location in the receiver to determine the highest cutoff frequency. Normally, the MAX3664 would determine the dominant low-frequency cutoff. Then select all other low-frequency cutoffs one decade lower.
5) Select a capacitor for the COMP pin from the *Typical Operating Characteristics* graphs. 400pF is adequate for most 622Mbps SDH/SONET applications.

622Mbps, Ultra-Low-Power, 3.3V Transimpedance Preamplifier for SDH/SONET

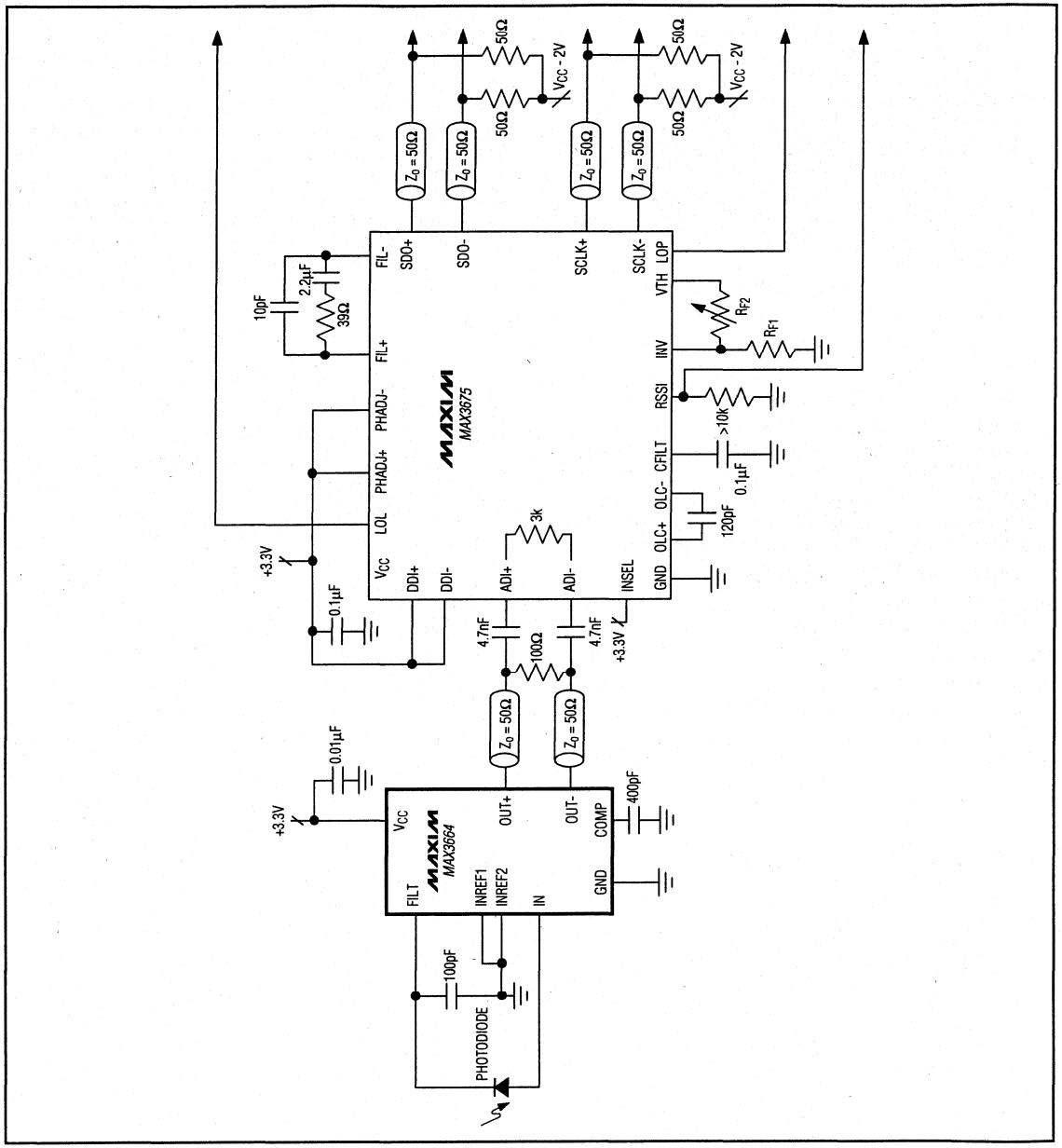


Figure 3. Simplified Schematic of the MAX3664/MAX3675 Receiver

Step 3: Designing Filters

The MAX3664's noise performance is a strong function of the circuit's bandwidth, which changes over temperature and varies from lot to lot. The receiver sensitivity can be improved by adding filters to limit this bandwidth. Filter designs can range from a one-pole filter using a single capacitor, to more complex filters using inductors. Figure 4 illustrates two examples: the simple filter provides moderate roll-off with minimal components, while the complex filter provides a sharper roll-off and better transient response.

Supply voltage noise at the cathode of the photodiode produces a current $I = C_{PHOTO}(\Delta V/\Delta t)$, which reduces the receiver sensitivity. C_{PHOTO} is the photodiode capacitance.

The FILT resistor of the MAX3664, combined with an external capacitor (see *Typical Operating Circuit*) can be used to reduce this noise. The external capacitor (C_{FILT}) is placed in parallel with the photodiode. Current generated by supply noise is divided between C_{FILT} and C_{PHOTO}. The input noise current due to supply noise is (assuming the filter capacitor is much larger than the photodiode capacitance):

$$I_{NOISE} = \frac{(V_{NOISE})(C_{PHOTO})}{(R_{FILT})(C_{FILTER})}$$

If the amount of tolerable noise is known, then the filter capacitor can be easily selected:

$$C_{FILT} = \frac{(V_{NOISE})(C_{PHOTO})}{(R_{FILT})(I_{NOISE})}$$

For example, with maximum noise voltage = 100mVp-p, C_{PHOTO} = 0.5pF, R_{FILT} = 1kΩ, and I_{NOISE} selected to be 5nA (1/10 of MAX3664 input-referred noise):

$$C_{FILT} = (0.1)(0.5E-12)/[(1000)(5E-9)] = 10nF$$

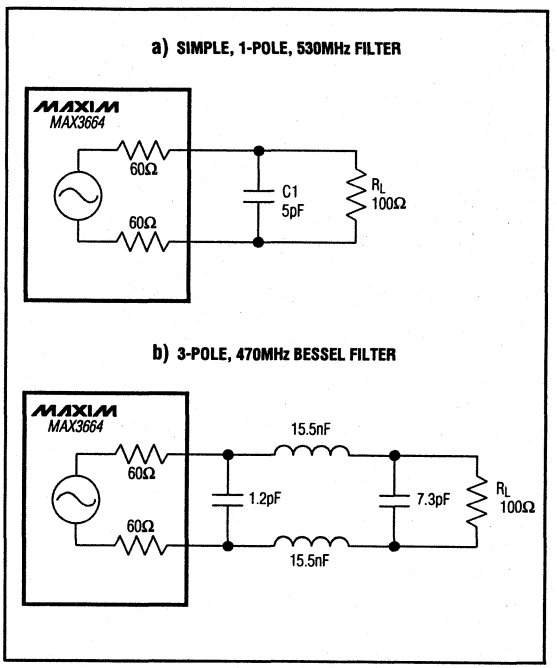


Figure 4. Filter Design Examples

Step 4: Designing a Low-Capacitance Input

Noise performance and bandwidth are adversely affected by stray capacitance on the input node. Select a low-capacitance photodiode and use good high-frequency design and layout techniques to minimize capacitance on this pin. The MAX3664 is optimized for 0.5pF of capacitance on the input—approximately the capacitance of a photodetector diode sharing a common header with the MAX3664 in die form.

622Mbps, Ultra-Low-Power, 3.3V Transimpedance Preamplifier for SDH/SONET

Photodiode capacitance changes significantly with bias voltage. With a 3.3V supply voltage, the reverse voltage on the PIN diode is only 2.5V. If a higher voltage supply is available, apply it to the diode to significantly reduce capacitance.

Take great care to reduce input capacitance. With the SO and µMAX versions of the MAX3664, the package capacitance is about 0.3pF, and the PC board between the MAX3664 input and the photodiode can add parasitic capacitance. Keep the input line short, and remove power and ground planes beneath it. Packaging the MAX3664 into a header with the photodiode provides the best possible performance. It reduces parasitic capacitance to a minimum, resulting in the lowest noise and the best bandwidth.

INREF1 and INREF2

Connect INREF1 and INREF2 as close to the AC ground of the photodetector diode as possible. The photodetector AC ground is usually the ground of the filter capacitor from the photodetector anode. The total loop (from INREF1/INREF2, through the bypass capacitor and the diode, and back to IN) should be no more than 2 cm. long.

Wire Bonding

For high current density and reliable operation, the MAX3664 uses gold metallization. Make connections to the die with gold wire only, and use ball bonding techniques (wedge bonding is not recommended). Die-pad size is 4 mils square, with a 6 mil pitch. Die thickness is 12 mils.

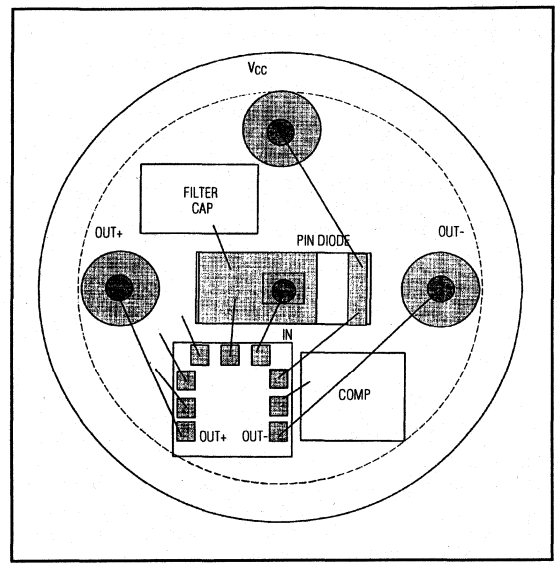


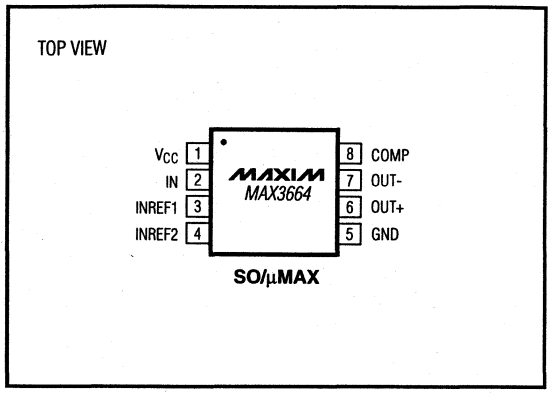
Figure 5. Suggested Layout for TO-46 Header

VCC and Ground

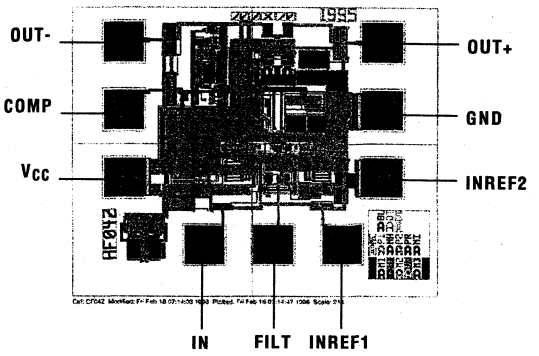
Use good high-frequency design and layout techniques. The use of a multilayer circuit board with separate ground and VCC planes is recommended. Take care to bypass VCC and to connect the GND pin to the ground plane with the shortest possible traces.

622Mbps, Ultra-Low-Power, 3.3V Transimpedance Preamplifier for SDH/SONET

Pin Configuration



Chip Topography



TRANSISTOR COUNT: 73

SUBSTRATE CONNECTED TO GND

19-1091; Rev 0; 6/96

EVALUATION KIT AVAILABLE

MAXIM

+3.3V, 622Mbps, SDH/SONET 1:4 Deserializer with LVDS Outputs

General Description

The MAX3681 deserializer is ideal for converting 622Mbps serial data to 4-bit-wide, 155Mbps parallel data in ATM and SDH/SONET applications. Operating from a single +3.3V supply, this device accepts PECL serial clock and data inputs, and delivers low-voltage differential-signal (LVDS) clock and data outputs for interfacing with high-speed digital circuitry. It also provides an LVDS synchronization input that enables data realignment and reframing.

The MAX3681 is available in the extended-industrial temperature range (-40°C to +85°C), in a 24-pin SSOP package.

Applications

622Mbps SDH/SONET Transmission Systems

622Mbps ATM/SONET Access Nodes

Add/Drop Multiplexers

Digital Cross Connects

Features

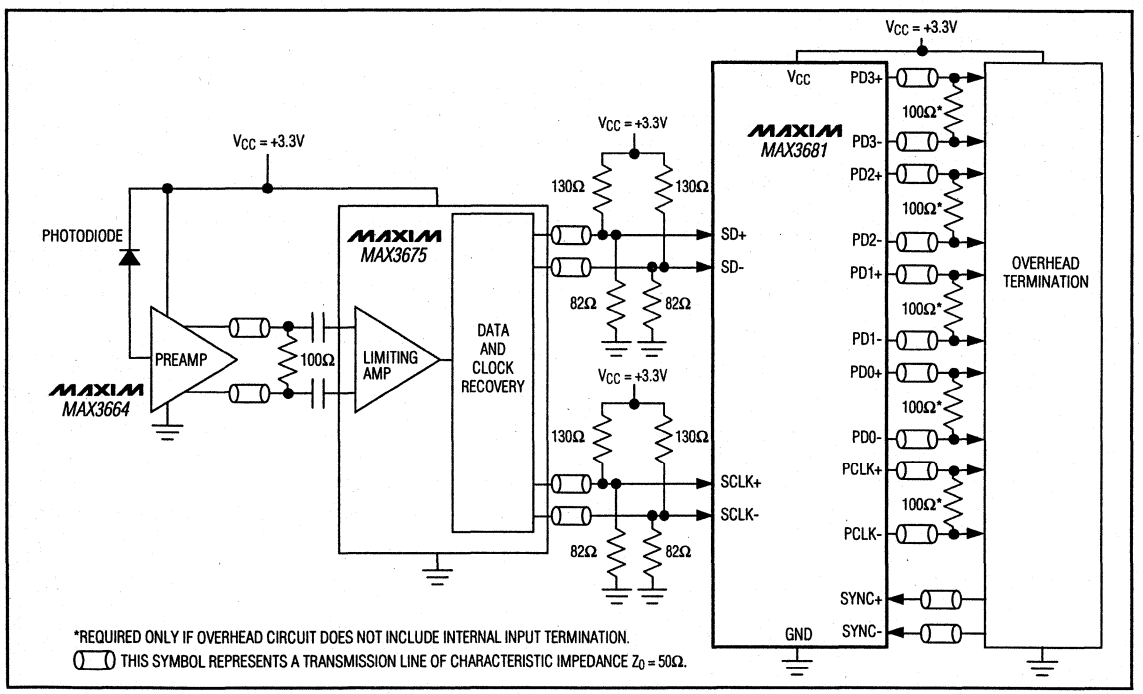
- **Single +3.3V Supply**
- **622Mbps Serial to 155Mbps Parallel Conversion**
- **265mW Power**
- **LVDS Data Outputs and Synchronization Inputs**
- **Synchronization Input for Data Realignment and Reframing**
- **Differential 3.3V PECL Clock and Data Inputs**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3681EAG	-40°C to +85°C	24 SSOP

Pin Configuration appears at end of data sheet.

Typical Operating Circuit



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

+3.3V, 622Mbps, SDH/SONET 1:4 Deserializer with LVDS Outputs

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)
V_{CC} .....-0.5V to 5V
PECL Inputs (SD+/-, SCLK+/-).....V_{CC} + 0.5V
LVDS Inputs (SYNC+/-).....V_{CC} + 0.5V
Output Current, LVDS Outputs (PCLK+/-, PD_+/-).....10mA

Continuous Power Dissipation (T_A = +85°C)
SSOP (derate 8.00mW/°C above +85°C) 520mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, differential loads = 100Ω, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}		55	80	120	mA
PECL INPUTS (SD+/-, SCLK+/-)						
Input High Voltage	V_{IH}		V_{CC} - 1.16		V_{CC} - 0.88	V
Input Low Voltage	V_{IL}		V_{CC} - 1.81		V_{CC} - 1.48	V
Input High Current	I_{IH}	$V_{IN} = V_{IH(MAX)}$	-10		10	µA
Input Low Current	I_{IL}	$V_{IN} = V_{IL(MAX)}$	-10		10	µA
LVDS INPUTS AND OUTPUTS (SYNC+/-, PCLK+/-, PD_+/-)						
Input Voltage Range	V_I	Differential input voltage = 100mV	0		2.4	V
Differential Input Threshold	V_{IDTH}	Common-mode voltage = 50mV	-100		100	mV
Threshold Hysteresis	V_{HYST}			70		mV
Differential Input Resistance	R_{IN}		85	100	115	Ω
Output High Voltage	V_{OH}				1.475	V
Output Low Voltage	V_{OL}		0.925			V
Differential Output Voltage	V_{OD}		250		400	mV
Change in Magnitude of Differential Output Voltage for Complementary States	ΔV_{OD}				25	mV
Output Offset Voltage	V_{OS}	T_A = +25°C	1.125		1.275	V
Change in Magnitude of Output Offset Voltage for Complementary States	ΔV_{OS}				25	mV
Single-Ended Output Resistance	R_O		40	70	140	Ω
Change in Magnitude of Single-Ended Output Resistance for Complementary States	ΔR_O			±1	±10	%

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, differential loads = 100Ω, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Serial Clock Frequency	f_{SCLK}		622			MHz
Serial Data Setup Time	t_{SU}		800			ps
Serial Data Hold Time	t_H		50			ps
Parallel Clock to Data Output Delay	t_{CLK-Q}		200	550	900	ps

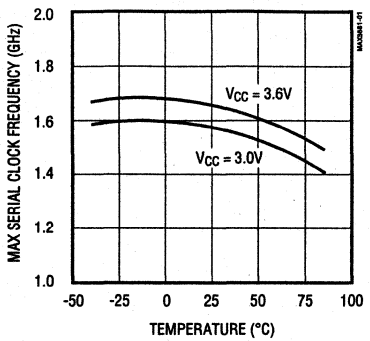
Note 1: AC Characteristics guaranteed by design and characterization.

+3.3V, 622Mbps, SDH/SONET 1:4 Deserializer with LVDS Outputs

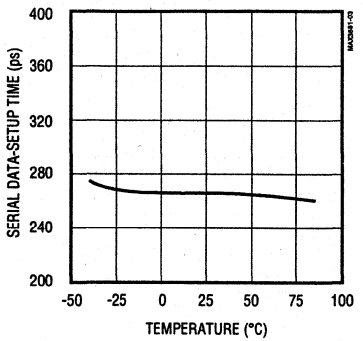
Typical Operating Characteristics

(V_{CC} = +3.0V to +3.6V, differential loads = 100Ω, unless otherwise noted.)

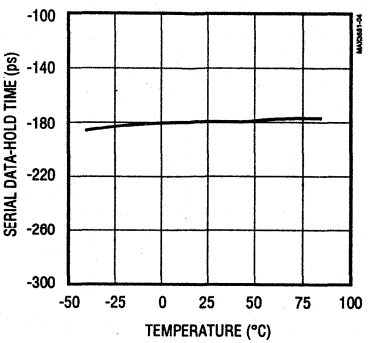
MAXIMUM SERIAL CLOCK FREQUENCY vs. TEMPERATURE



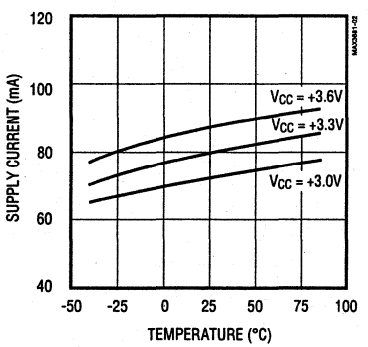
SERIAL DATA-SETUP TIME vs. TEMPERATURE



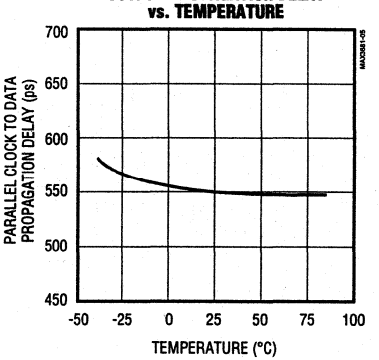
SERIAL DATA-HOLD TIME vs. TEMPERATURE



SUPPLY CURRENT vs. TEMPERATURE



PARALLEL CLOCK TO DATA OUTPUT PROPAGATION DELAY vs. TEMPERATURE



+3.3V, 622Mbps, SDH/SONET 1:4 Deserializer with LVDS Outputs

Pin Description

PIN	NAME	FUNCTION
1, 2, 5, 8, 12	V_{CC}	+3.3V Supply Voltage
3	SD+	Noninverting PECL Serial Data Input. Data is clocked on the SCLK signal's positive transition.
4	SD-	Inverting PECL Serial Data Input. Data is clocked on the SCLK signal's positive transition.
6	SCLK+	Noninverting PECL Serial Clock Input
7	SCLK-	Inverting PECL Serial Clock Input
9, 15, 22	GND	Ground
10	SYNC+	Noninverting LVDS Synchronizing Pulse Input. Pulse the SYNC signal high for at least two SCLK periods to shift the data alignment by dropping one bit.
11	SYNC-	Inverting LVDS Synchronizing Pulse Input. Pulse the SYNC signal high for at least two SCLK periods to shift the data alignment by dropping one bit.
13	PCLK-	Inverting LVDS Parallel Clock Output
14	PCLK+	Noninverting LVDS Parallel Clock Output
16, 18, 20, 23	PD0- to PD3-	Inverting LVDS Parallel Data Outputs. Data is updated on the positive transition of the PCLK signal. See Figure 2 for the relationship between serial-data-bit position and output-data-bit assignment.
17, 19, 21, 24	PD0+ to PD3+	Noninverting LVDS Parallel Data Outputs. Data is updated on the positive transition of the PCLK signal. See Figure 2 for the relationship between serial-data-bit position and output-data-bit assignment.

Detailed Description

The MAX3681 deserializer uses a 4-bit shift register, 4-bit parallel output register, 2-bit counter, PECL input buffers, and low-voltage differential-signal (LVDS) input/output buffers to convert 622Mbps serial data to 4-bit-wide, 155Mbps parallel data (Figure 1).

The input shift register continuously clocks incoming data on the positive transition of the serial clock (SCLK) input signal. The 2-bit counter generates a parallel output clock (PCLK) by dividing down the serial clock frequency. The PCLK signal is used to clock the parallel output register. During normal operation, the counter divides the SCLK frequency by four, causing the output register to latch every four bits of incoming serial data.

The synchronization inputs (SYNC+, SYNC-) are used for data realignment and reframing. When the SYNC signal is pulsed high for at least two SCLK cycles, the parallel output data is delayed by one SCLK cycle. This realignment is guaranteed to occur within two PCLK cycles of the SYNC signal's positive transition. As a result, the first incoming bit of data during that PCLK cycle is dropped, shifting the alignment between PCLK and data by one bit.

See Figure 2 for the functional timing diagram and Figure 3 for the timing parameters diagram.

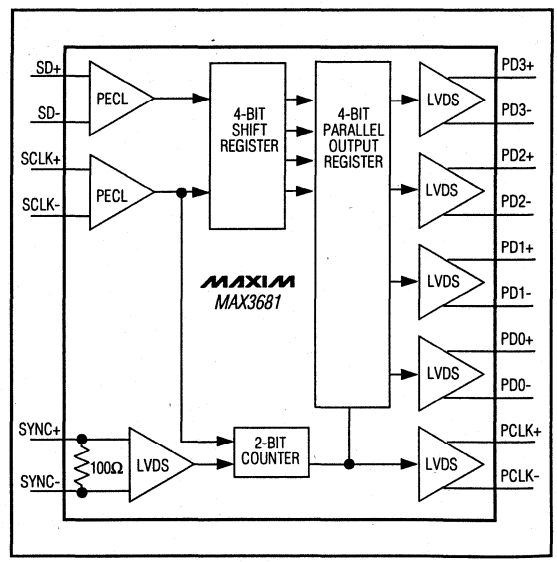


Figure 1. Functional Diagram

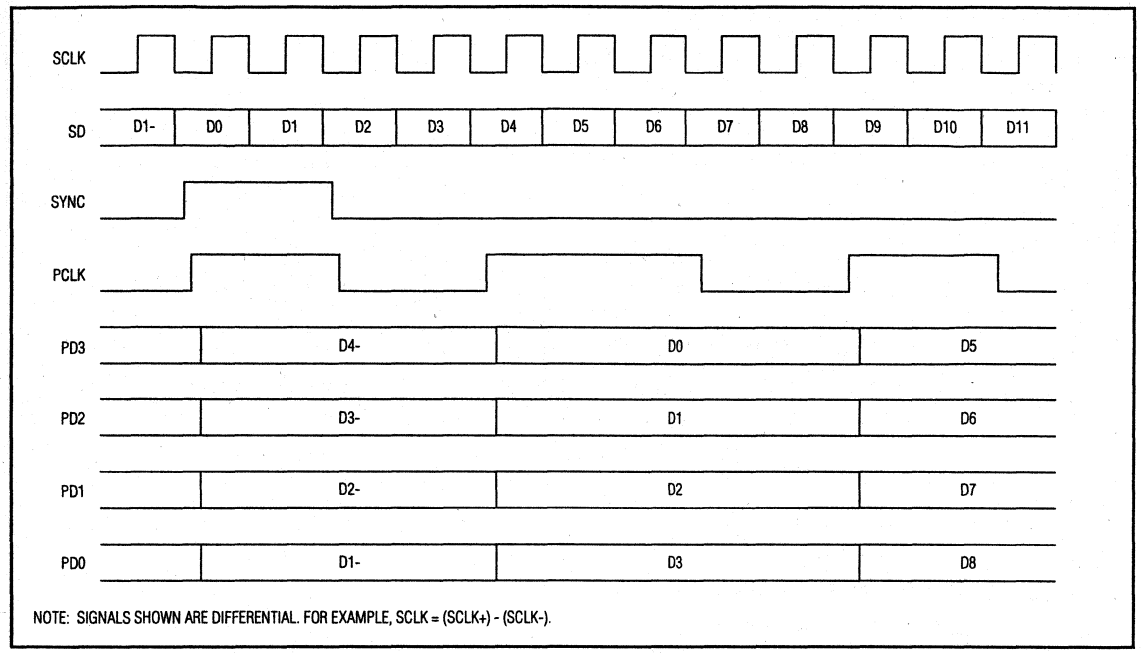


Figure 2. Functional Timing Diagram

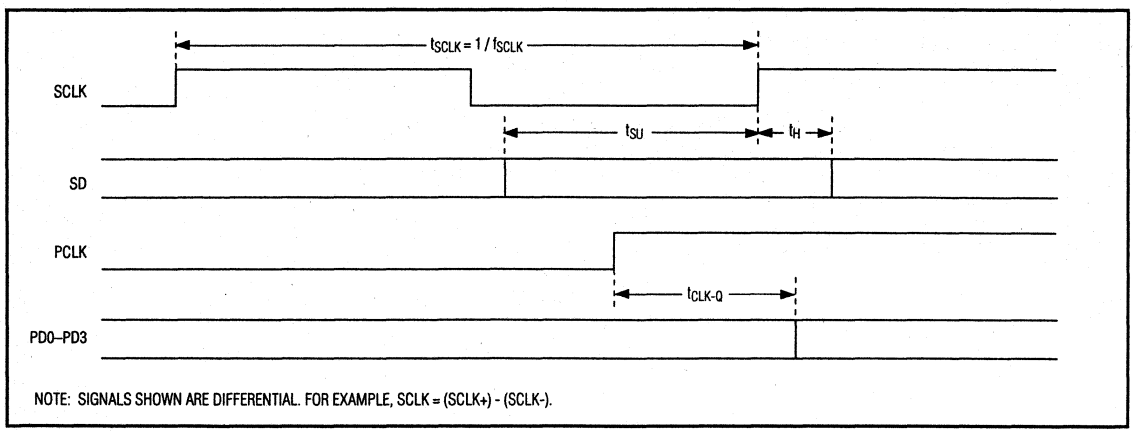


Figure 3. Timing Parameters

+3.3V, 622Mbps, SDH/SONET 1:4 Deserializer with LVDS Outputs

Low-Voltage Differential-Signal (LVDS) Inputs and Outputs

The MAX3681 features LVDS inputs and outputs for interfacing with high-speed digital circuitry. The LVDS standard is based on the IEEE 1596.3 LVDS specification. This technology uses 250mVp-p to 400mVp-p, differential low-voltage swings to achieve fast transition times, minimized power dissipation, and noise immunity.

The parallel clock and data LVDS outputs (PCLK+, PCLK-, PD_+, PD_-) require 100Ω differential DC termination between the inverting and noninverting outputs for proper operation. Do not terminate these outputs to ground.

The synchronization LVDS inputs (SYNC+, SYNC-) are internally terminated with 100Ω of differential input resistance, and therefore do not require external termination.

PECL Inputs

The serial data and clock PECL inputs (SD+, SD-, SCLK+, SCLK-) require 50Ω termination to (V_{CC} - 2V) when interfacing with a PECL source (see the *Alternative PECL Input Termination* section).

Applications Information

Alternative PECL Input Termination

Figure 4 shows alternative PECL input-termination methods. Use Thevenin-equivalent termination when a (V_{CC} - 2V) termination voltage is not available. If AC coupling is necessary, such as when interfacing with an ECL-output device, use the ECL AC-coupling termination.

Layout Techniques

For best performance, use good high-frequency layout techniques. Filter voltage supplies and keep ground connections short. Use multiple vias where possible. Also, use controlled impedance transmission lines to interface with the MAX3681 data inputs and outputs.

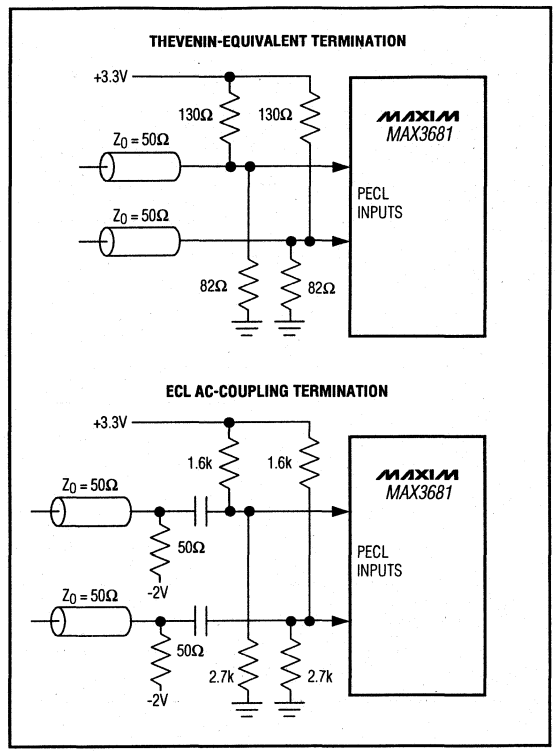
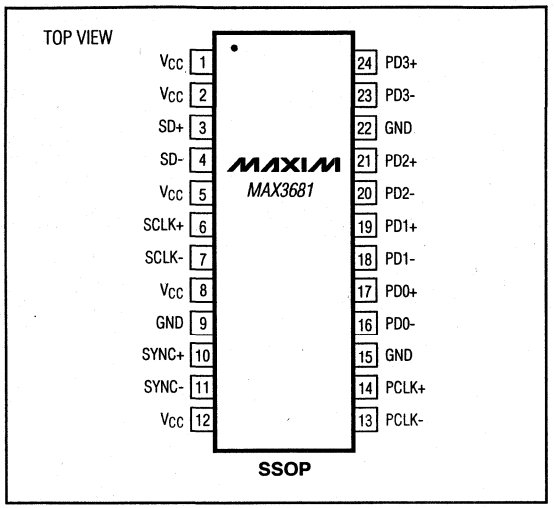


Figure 4. Alternative PECL Input Termination

+3.3V, 622Mbps, SDH/SONET 1:4 Deserializer with LVDS Outputs

Pin Configuration



Chip Information

TRANSISTOR COUNT: 724

19-1097; Rev 1; 9/96

EVALUATION KIT AVAILABLE

MAXIM

Low-Power, 622Mbps Limiting Amplifiers with Chatter-Free Power Detect for LANs

General Description

The MAX3761/MAX3762 limiting amplifiers, with 4mV sensitivity and PECL data outputs, are optimized for operation in low-cost, 622Mbps, LAN/ATM LAN fiber optics applications.

An integrated power detector senses the input signal's amplitude. A received-signal-strength indicator (RSSI) gives an analog indication of the power level, while the complementary loss-of-signal (LOS) outputs indicate if the input power level exceeds the programmed threshold level. The LOS threshold can be adjusted to detect signal amplitudes between 3mVp-p and 100mVp-p, providing a 15dB LOS adjustment in fiber optic receivers. The LOS outputs have 3.5dB of hysteresis, which prevents chatter when input signal levels are small. The MAX3761's LOS outputs are compatible with TTL-logic levels. The MAX3762 has PECL LOS outputs.

DISABLE and LOS can be used to implement a squelch function, which turns off the data outputs when the input signal is below the programmed threshold.

Applications

622Mbps LAN/ATM LAN Receivers

155Mbps LAN/ATM LAN Receivers

Features

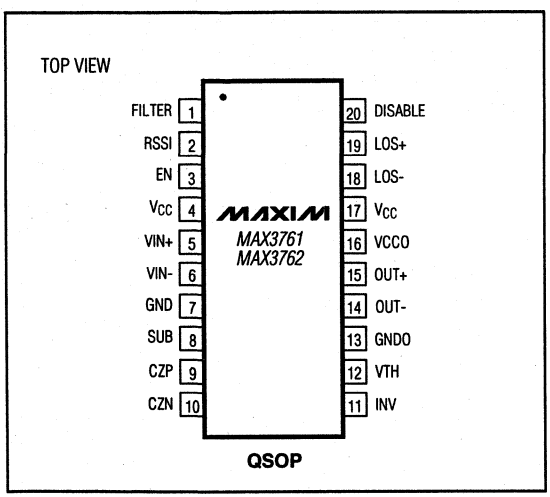
- ♦ **Chatter-Free Power Detector with Programmable Loss-of-Signal Outputs**
- ♦ **4mV Input Sensitivity (PECL Loss-of-Signal Interface Logic—MAX3766**
- ♦ **PECL Data Outputs**
- ♦ **Single 5V Power Supply**
- ♦ **250ps Output Edge Speed**
- ♦ **Low 15ps Pulse-Width Distortion**
- ♦ **TTL Loss-of-Signal Interface Logic—MAX3761**

Ordering Information

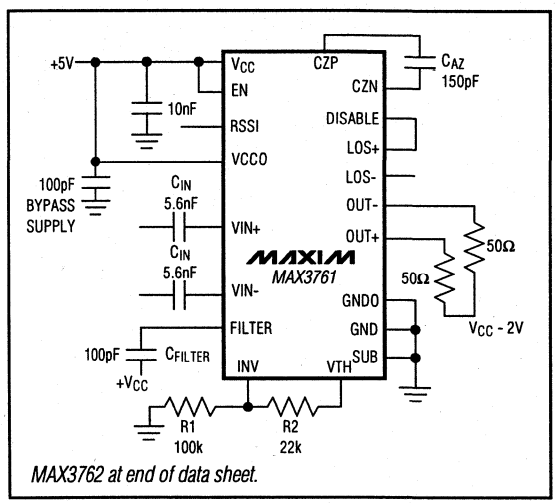
PART	TEMP. RANGE	PIN-PACKAGE
MAX3761EEP	-40°C to +85°C	20 QSOP
MAX3761C/D	-40°C to +85°C	Dice*
MAX3762EEP	-40°C to +85°C	20 QSOP
MAX3762C/D	-40°C to +85°C	Dice*

**Dice are designed to operate from -40°C to +85°C, but are tested and guaranteed only at T_A = +25°C.*

Pin Configuration



Typical Operating Circuits



MAX3762 at end of data sheet.

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Low-Power, 622Mbps Limiting Amplifiers with Chatter-Free Power Detect for LANs

ABSOLUTE MAXIMUM RATINGS

V_{CC}, VCCO .....-0.5V to +7.0V
FILTER, RSSI, EN, VIN+, VIN-, CZP, CZN,
DISABLE, LOS+, LOS-, INV, VTH.....-0.5V to (V_{CC} + 0.5V)
PECL Output Current (OUT+, OUT-, LOS+, LOS-) 50mA
Continuous Power Dissipation (T_A = +85°C)
QSOP (derate 8.3mW/°C above +70°C).....667mW

Operating Junction Temperature Range.....-40°C to +150°C
Processing Temperature (die) .....+400°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.5V to +5.5V, DISABLE = low, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +5.0V, T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power-Supply Current	MAX3761, I_{VCC}			25	37	mA
	MAX3762, I_{VCC}			30	46	
LOS Output TTL High	MAX3761		2.8			V
LOS Output TTL Low	MAX3761	(T_A = +25°C to +85°C)			0.40	V
		(T_A = -40°C to +25°C)			0.44	
LOS Output PECL High	MAX3762 (Notes 2, 3)		-1150		-880	mV
LOS Output PECL Low	MAX3762 (Notes 2, 3)		-1830		-1555	mV
DISABLE Input Current	Logic high				100	µA
DISABLE Input High	MAX3761		2.65			V
DISABLE Input Low	MAX3761				0.8	V
DISABLE Input PECL High	MAX3762 (Note 3)		-1160			mV
DISABLE Input PECL Low	MAX3762 (Note 3)				-1470	mV
PECL Data Output Voltage High (V_{OH})	(Notes 2, 3)		-1150		-880	mV
PECL Data Output Voltage Low (V_{OL})	(Notes 2, 3)		-1830		-1555	mV
Disabled Differential Output	DISABLE = high		-100		100	mV
Disabled Common-Mode Output	DISABLE = high		V_{CC} - 0.7		V_{CC} -1.2	V

Note 1: Dice are tested at T_A = +25°C.
Note 2: Outputs terminated with 50Ω to V_{CC} - 2V.
Note 3: Voltage measurements are relative to V_{CC}.

AC ELECTRICAL CHARACTERISTICS

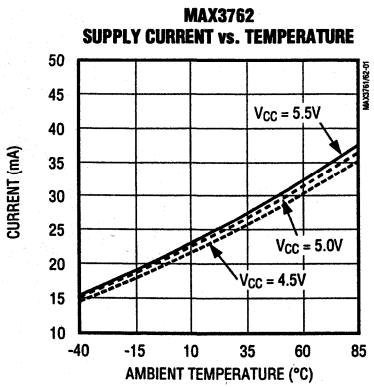
(V_{CC} = +4.5V to +5.5V, PECL outputs terminated with 50Ω to V_{CC} - 2V, input 4mV to 2Vp-p, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +5.0V, T_A = +25°C.) (Note 5)

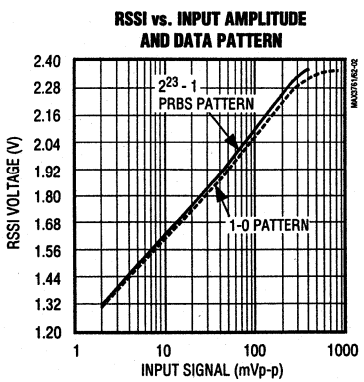
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum LOS Assert Input	T_A = -40°C, 2^{23} - 1 PRBS			3.2	mV
Data-Output Edge Speed	20% to 80%			250	ps
Data-Output Overshoot	(Note 6)			20	%
Pulse-Width Distortion	(Notes 6, 7)		15	80	ps
Input Resistance	Differential		3900		Ω
LOS Hysteresis	2^{23} - 1 PRBS, VTH = 1.8V		3.5		dB

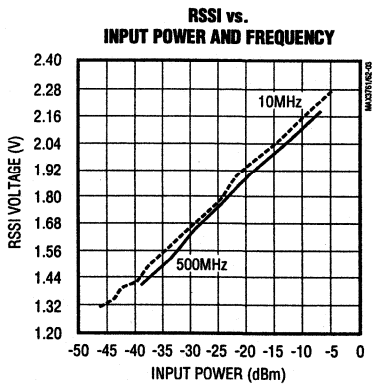
Note 5: AC parameters are guaranteed by design and characterization.
Note 6: Input signal is a 1-0 pattern, 622Mbps.
Note 7: PWD = [(width of wider pulse) - (width of narrower pulse)] / 2.

Typical Operating Characteristics

(MAX3761/MAX3762 EV kit, V_{CC} = +5.0V, PECL outputs terminated with 50Ω to V_{CC} - 2V, input is a 1-0 pattern, 622Mbps, T_A = +25°C, unless otherwise noted.)





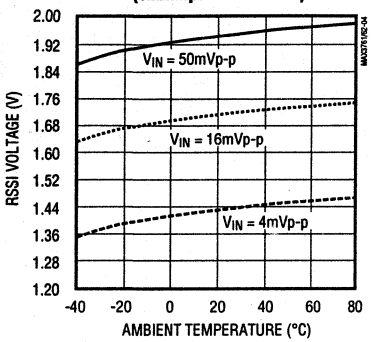


Low-Power, 622Mbps Limiting Amplifiers with Chatter-Free Power Detect for LANs

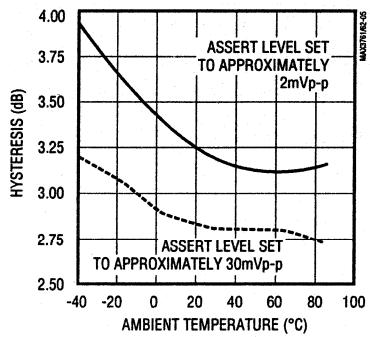
Typical Operating Characteristics (continued)

(MAX3761/MAX3762 EV kit, V_{CC} = +5.0V, PECL outputs terminated with 50Ω to V_{CC} - 2V, input is a 1-0 pattern, 622Mbps, T_A = +25°C, unless otherwise noted.)

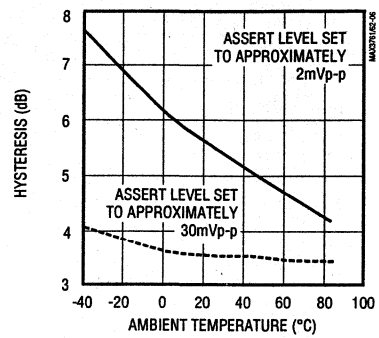
RSSI vs. TEMPERATURE (622Mbps 2^{23} - 1 PRBS)



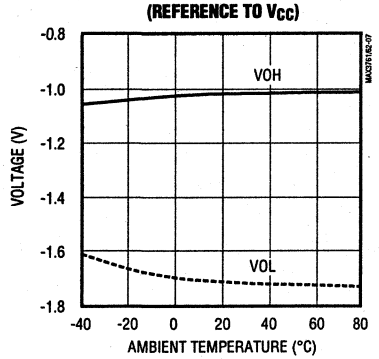
LOS HYSTERESIS vs. TEMPERATURE (622Mbps 2^{23} - 1 PRBS PATTERN)



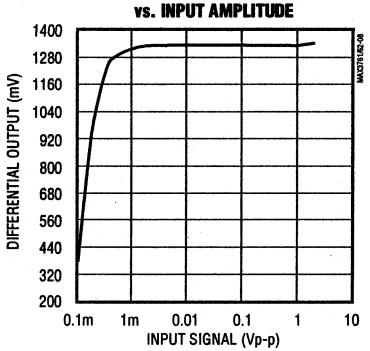
LOS HYSTERESIS vs. TEMPERATURE (622Mbps 1-0 PATTERN)



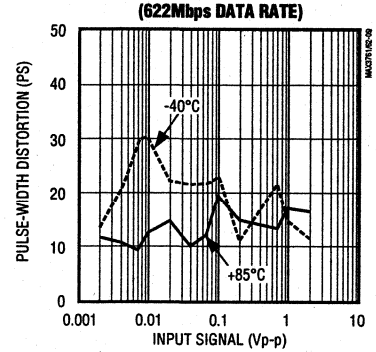
DATA OUTPUT LEVELS (REFERENCE TO V_{CC})



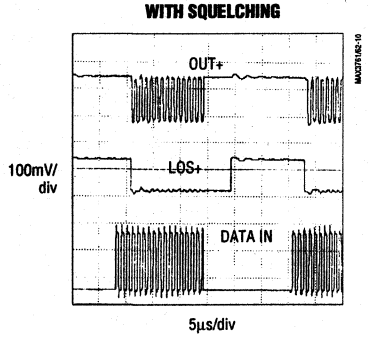
DIFFERENTIAL OUTPUT vs. INPUT AMPLITUDE



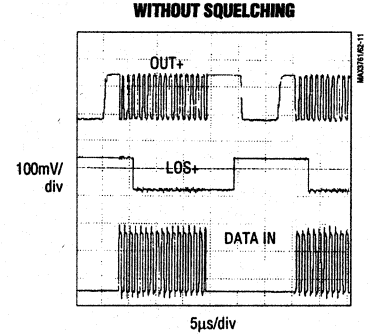
PULSE-WIDTH DISTORTION (622Mbps DATA RATE)



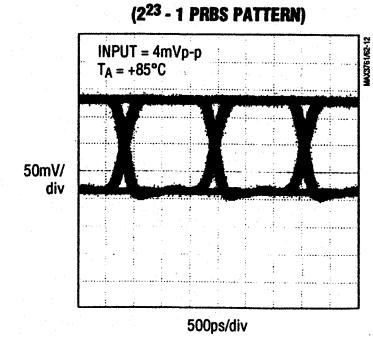
LOS OPERATION WITH SQUELCHING



LOS OPERATION WITHOUT SQUELCHING



DATA OUTPUT SINGLE-ENDED (2^{23} - 1 PRBS PATTERN)

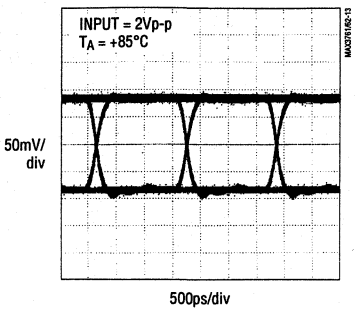


Low-Power, 622Mbps Limiting Amplifiers with Chatter-Free Power Detect for LANs

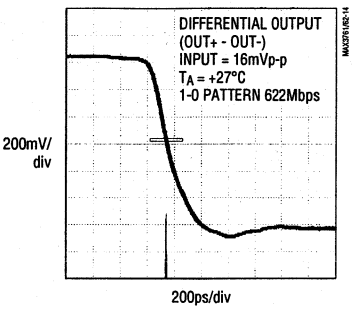
Typical Operating Characteristics (continued)

(MAX3761/MAX3762 EV kit, V_{CC} = +5.0V, PECL outputs terminated with 50Ω to V_{CC} - 2V, input is a 1-0 pattern, 622Mbps, T_A = +25°C, unless otherwise noted.)

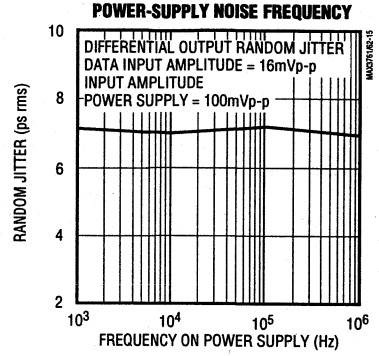
DATA OUTPUT SINGLE-ENDED (2^{23}-1 PRBS PATTERN)



RANDOM JITTER



RANDOM JITTER vs. POWER-SUPPLY NOISE FREQUENCY



Pin Description

PIN	NAME	FUNCTION
1	FILTER	Sets the integration frequency of the power detector. Impedance at this node is approximately 500Ω.
2	RSSI	Received-Signal-Strength Indicator. An analog DC voltage representing the input power.
3	EN	Connect to V_{CC}.
4, 17	V_{CC}	+5V Power Supply
5	VIN+	Positive Input Data
6	VIN-	Negative Input Data
7	GND	Supply Ground
8	SUB	Substrate. Connect to ground.
9	CZP	Sets input offset correction, low-frequency cutoff.
10	CZN	Sets input offset correction, low-frequency cutoff.
11	INV	Negative Input to Op Amp. Used for programming the loss-of-signal threshold.
12	VTH	Loss-of-Signal Threshold Voltage
13	GNDO	Ground Power Supply for Output Buffers
14	OUT-	Negative PECL Data Output
15	OUT+	Positive PECL Data Output
16	VCCO	+5V Power Supply for Output Buffers
18	LOS-	Negative Loss-of-Power Flag, TTL (MAX3761) or PECL (MAX3762)
19	LOS+	Positive Loss-of-Power Flag, TTL (MAX3761) or PECL (MAX3762)
20	DISABLE	Disables the data outputs when high. TTL (MAX3761) or PECL (MAX3762).

Low-Power, 622Mbps Limiting Amplifiers with Chatter-Free Power Detect for LANs

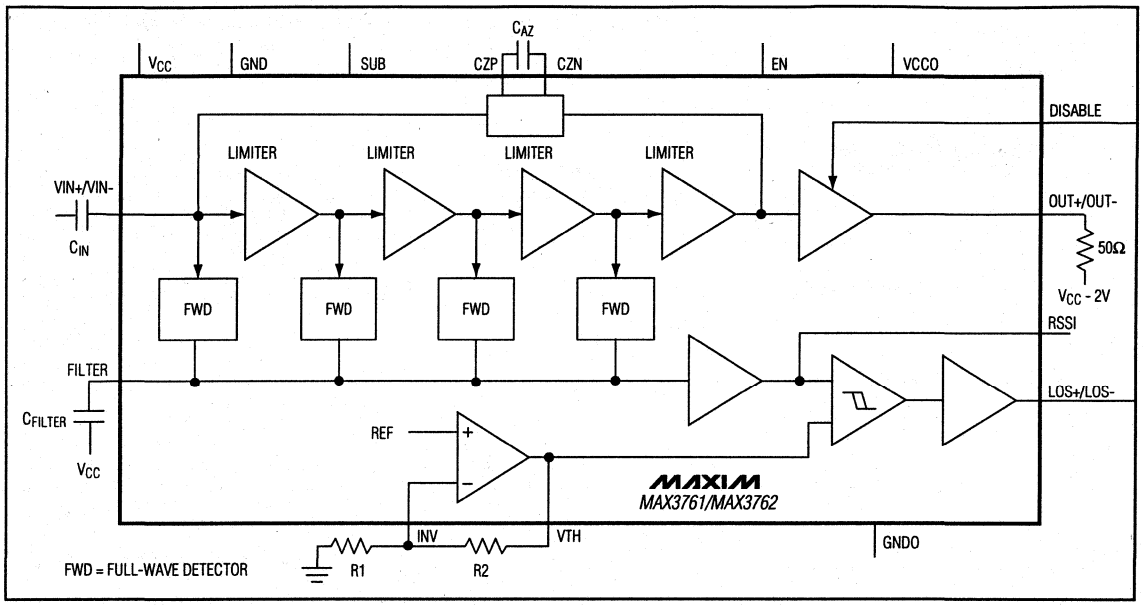


Figure 1. Functional Diagram

Detailed Description

Figure 1 shows the functional diagram for the MAX3761/MAX3762. The input signal is applied to VIN+ and VIN-. A chain of amplifier stages, each contributing approximately 12.5dB of gain, amplifies the input signal to PECL output voltage swings. A 4mVp-p input signal will cause the output to fully limit.

Received-Signal-Strength Indicator (RSSI)

Each amplifier stage contains a full-wave logarithmic detector (FWD). The full-wave detector outputs are summed at the FILTER pin and used to generate the received-signal-strength indication (RSSI). The RSSI output voltage is linearly proportional to the input power (in decibels), and is approximated by:

$$V_{RSSI}(V) = 1.13 + 0.457\log(V_{IN})$$

where V_{IN} is the peak-to-peak input signal in millivolts.

The RSSI output is insensitive to fluctuations in temperature and supply voltage. The power detector functions as a broadband power meter that detects the total power of all signals present in the passband of approximately 750MHz. Refer to the *Typical Operating Characteristics* graphs showing RSSI output versus input power and signal amplitude.

The high-speed RSSI signal is filtered with one external capacitor connected from FILTER to V_{CC}. The impedance at the FILTER pin is approximately 500Ω.

The FILTER capacitor (C_{FILTER}) must be connected to V_{CC} for proper operation.

Input-Offset Correction

The limiting amplifier provides approximately 60dB of gain. An input DC offset of even 1mV reduces the power-detection circuit's accuracy and can cause the output to limit. A low-frequency feedback loop is integrated into the MAX3761/MAX3762 to remove input offset. DC coupling the inputs is not recommended, as this prevents the DC-offset-correction circuitry from functioning properly. Input offset is typically reduced to less than 100µV.

The capacitance between pins CZP and CZN, in parallel with a 10pF integrated capacitance, determines the offset-correction circuit's time constant. The input impedance between CZP and CZN is approximately 800kΩ.

The offset correction circuitry requires an average data-input duty cycle of 50%. If the input data has a different average duty cycle, the output will have increased pulse-width distortion.

Low-Power, 622Mbps Limiting Amplifiers with Chatter-Free Power Detect for LANs

Loss-of-Signal Indicator

The MAX3761/MAX3762 includes a loss-of-signal monitor with a programmable assert threshold and a hysteresis comparator. Internally, one comparator input is tied to the RSSI output signal and the other is tied to the threshold-voltage (VTH) pin, which provides a threshold for the LOS indication. An op amp referenced to an internal bandgap voltage (1.18V) is supplied for programming a supply-independent threshold voltage. Only two external resistors are needed to program the LOS assert level. VTH is programmable from 1.18V to 2.4V, providing adequate coverage of the RSSI output's useful range. The op amp runs on very low supply current and provides an accurate, temperature-stable threshold, but can source only 20µA of current. For proper operation, resistor R1 (see the *Typical Operating Circuit*) should have a value ≥ 100kΩ. The input bias current at INV is < 50nA.

To ensure chatter-free LOS operation, the internal LOS comparator contains approximately 90mV of hysteresis. The RSSI signal output has a slope of 25mV/dB. Therefore, the overall circuit hysteresis is approximately 3.6dB[90mV / (25mV/dB)]. The LOS assert threshold is 45mV below V_{TH}, while the LOS deassert threshold is 45mV above V_{TH}.

Output Buffers

The DISABLE pin can be used to disable the data-output buffer. When DISABLE is high, the differential output signal at OUT+ and OUT- is approximately zero. In the disabled state, the common-mode voltage of each output is approximately V_{CC} - 0.8V. Connecting DISABLE to LOS+ implements a squelch function. When using the squelch function, the output signal is disabled whenever the input signal is too small to be reliably detected (as determined by the voltage at VTH). Use of the disable function is recommended at all times.

The data outputs (OUT+ and OUT-) are implemented with emitter followers that have output impedance of approximately 2Ω. The MAX3762's PECL LOS outputs also are implemented with emitter followers that have output impedance of approximately 2Ω.

The MAX3761 TTL LOS output buffers are open-collector transistors with 6kΩ internal pull-up resistors.

Design Procedure

Supply Voltage

The MAX3761/MAX3762 can be operated with a single +5V or -5V power supply.

Programming the LOS Assert Level

First determine the receiver system's sensitivity in dBm either by estimating or from prototyping results. Estimate the total gain of the preamplifier and photodiode, then use Figure 3 to select resistor R2, placing the LOS assert 3dB to 4dB below the receiver sensitivity.

Alternatively, use the *Typical Operating Characteristics* to select the V_{TH} value needed for LOS assert, then program V_{TH} with the following relation:

$$V_{TH} = 1.18(1 + R2 / R1)$$

Select R1 ≥ 100kΩ.

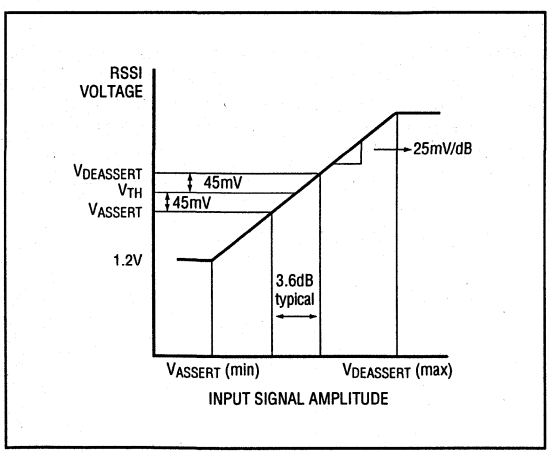


Figure 2. Loss-of-Signal Definitions

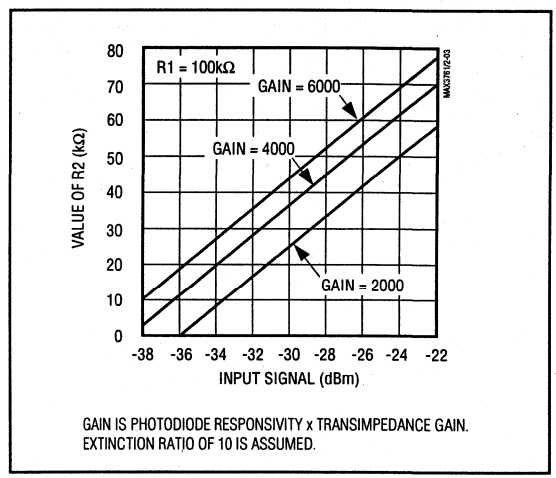


Figure 3. Using TIA Gain and Photodiode Responsivity to Select LOS Programming Resistor

12

Low-Power, 622Mbps Limiting Amplifiers with Chatter-Free Power Detect for LANs

Capacitor Selection

A typical MAX3761/MAX3762 implementation requires four external capacitors. To select the capacitors, first determine the following parameters in the receiver system (see the *Applications Information* section for recommendations in 622Mbps ATM and Fibre Channel 1063Mbps systems):

1) The duration of the expected longest run of consecutive bits in the data stream. For example, 72 consecutive zeros in a 622Mbps data stream have a duration of 116ns.
2) The maximum allowable data-dependent jitter.
3) The desired power-detector integration time constant [$1/(2\pi f_{INT})$].
4) The transimpedance amplifier's maximum peak-to-peak output voltage.

Step 1. Select the Input AC-Coupling Capacitors (C_{IN}). When using a limiting preamplifier with a highpass frequency response, select C_{IN} to provide a low-frequency cutoff (f_C) one decade lower than the preamplifier low-frequency cutoff. This causes nearly all data-dependent jitter (DDJ) to be generated in the preamplifer circuit. For example, if the preamplifier's low-frequency cutoff is 150kHz, then select C_{IN} to provide a 15kHz low-frequency cutoff.

Select C_{IN} with the following equation:

$$C_{IN} = \frac{1}{2\pi f_C 1950\Omega}$$

For differential input signals, use a capacitor equal to C_{IN} on both inputs (VIN+ and VIN-). For single-ended input signals, one capacitor should be tied to VIN+ and another should decouple VIN- to ground.

When using a preamplifier without a highpass response, select C_{IN} to ensure that data-dependent jitter is acceptable. The following equation provides an estimate for C_{IN}:

$$C_{IN} \geq \frac{-t_L}{1950 \ln\left[1 - \frac{(DDJ)(BW)}{0.5}\right]}$$

where: t_L = duration of the longest run of consecutive bits with the same value (seconds); DDJ = maximum allowable data-dependent jitter, peak-to-peak (seconds); BW = typical system bandwidth, normally 0.6 to 1.0 times the data rate (hertz).

Regardless of which method is used to select C_{IN}, the maximum LOS assert time can be estimated from the value of C_{IN}. The following equation estimates LOS time delay when the maximum-amplitude signal is instantaneously removed from the input, and when the FILTER time constant is much faster than the input time constant ($C_{FILTER} < 0.4C_{IN}$):

$$t_{LOS\ ASSERT} = 1950 C_{IN} \ln(V_{MAXp\text{-}p} / V_{ASSERTp\text{-}p})$$

where $V_{MAXp\text{-}p}$ is the maximum output of the preamplifier, and $V_{ASSERTp\text{-}p}$ is the input amplitude that causes LOS to assert. The equation describes the input capacitors' discharge time, from maximum input to the LOS threshold into the 1950Ω, single-ended input resistance.

Step 2. Select the Offset-Correction Capacitor (C_{AZ}). To maintain stability, it is important to keep a one-decade separation between f_C and the low-frequency cutoff associated with the DC-offset-correction circuit (f_{OC}).

The input impedance between CZP and CZN is approximately 800kΩ in parallel with 10pF. As a result, the low-frequency cutoff (f_{OC}) associated with the DC-offset-correction loop is computed as follows:

$$f_{OC} = \frac{1}{2\pi 800k\Omega\,(C_{AZ} + 10pF)}$$

where C_{AZ} is an optional external capacitor between CZP and CZN.

If C_{IN} is known, then:

$$C_{AZ} \geq \frac{C_{IN}}{41} - 10pF$$

Step 3. Select the Power-Detect Integration Capacitor (C_{FILTER}). For 622Mbps ATM applications, Maxim recommends a filter frequency of 3MHz, which requires C_{FILTER} = 100pF. The integration frequency can be selected lower to remove low-frequency noise, or to prevent unusual data sequences from asserting LOS.

$$C_{FILTER} = 1 / (2\pi 500 f_{INT})$$

where f_{INT} is the integration frequency.

Applications Information

Converting Average Optical Power to Signal Amplitude

Many of the MAX3761/MAX3762's specifications relate to input-signal amplitude. When working with fiber optic receivers, the input is usually expressed in terms of average optical power and extinction ratio. The relations given in Table 1 are helpful for converting optical power to input signal when designing with the MAX3761/MAX3762.

Table 1. Optical-Power Relations*

PARAMETER	SYMBOL	RELATION
Average Power	P_{AVE}	$P_{AVE} = (P0 + P1)/2$
Extinction Ratio	r_e	$r_e = P1 / P0$
Optical Power of a "1"	P1	$P1 = 2P_{AVE}\frac{r_e}{r_e+1}$
Optical Power of a "0"	P0	$P0 = 2P_{AVE}/(r_e+1)$
Signal Amplitude	P_{IN}	$P_{IN} = P1 - P0 = 2P_{AVE}\frac{(r_e-1)}{r_e+1}$

* Assuming a 50% average input data duty cycle (true for SONET/ATM data).

In an optical receiver, the input voltage to the limiting amplifier can be found by multiplying the relationship in Table 1 with the photodiode responsivity (p) and transimpedance amplifier gain (G).

Optical Hysteresis

Power and hysteresis are often expressed in decibels. By definition, decibels are always 10log (power). At the inputs to the MAX3761/MAX3762 limiting amplifier, the power is V_{IN}^2/R. If a receiver's optical input power (x) increases by a factor of two, and the preamplifier is linear, then the voltage input to the MAX3761/MAX3762 also increases by a factor of two.

The optical power change is $10\log(2x/x) = 10\log(2) = +3dB$

At the MAX3761/MAX3762, the voltage change is:

$$10\log\frac{(2y)^2/R}{y^2/R} = 10\log(2^2) = 20\log(2) = +6dB$$

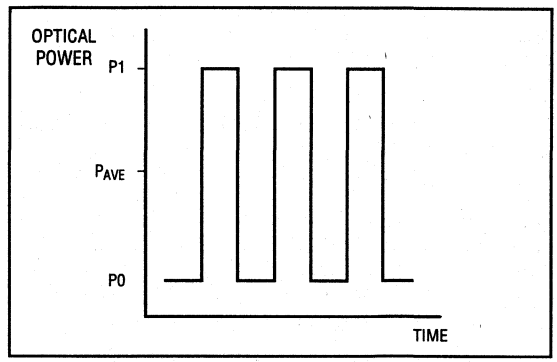


Figure 4. Optical-Power Relations

In an optical receiver the dB change at the MAX3761/MAX3762 will always equal 2x the optical dB change.

The MAX3761/MAX3762's typical voltage hysteresis is 3.6dB. This provides an optical hysteresis of 1.8dB.

Input Sensitivity

The receiver's gain sensitivity defines the smallest signal input that results in fully limited PECL-compatible data outputs. Smaller signals result in nonlimited outputs. The MAX3761/MAX3762's input sensitivity (S_{GAIN}) is 4mVp-p:

$$S_{GAIN} = 4mV$$

Optical gain sensitivity (in dBm) is:

$$10\log\left[\frac{S_{GAIN}}{2G\rho} \times \frac{r_e+1}{r_e-1} \times 1000\right]$$

In a receiver with $G = 6k\Omega$, $r_e = 10$, and $\rho = 0.8A/W$, gain sensitivity is 510nW, or -32.9dBm.

622Mbps ATM Component Selection

As an example, a preamplifier with a 150kHz low-frequency cutoff and a 950mVp-p maximum output has the best performance with the following selections:

C_{IN} = 5.6nF, so that f_C = 15kHz (one decade below the 150kHz cutoff)

C_{AZ} = 150pF, so that f_{OC} < 1.5kHz (one decade below f_C)

C_{FILTER} = 100pF, so that the integration frequency equals 3MHz.

These selections should provide data-dependent jitter less than 110ps p-p when the input consists of PRBS data with no more than 72 consecutive bits.

Low-Power, 622Mbps Limiting Amplifiers with Chatter-Free Power Detect for LANs

For LOS assert at -35dBm, select R1 = 100kΩ and R2 = 22kΩ, which programs the LOS assert at input ≅ 3mV. With this selection, LOS assert time will typically be less than 85µs.

Fibre Channel Component Selection

In Fibre Channel applications, the desired LOS assert time is typically 25µs maximum, and data-dependent jitter is reduced by 8B10B coding techniques. The following are recommended in a Fibre Channel system where preamp gain is 2000V/W, LOS assert is set for -24dBm (13mV MAX3761/MAX3762 input), and the maximum input to the MAX3761/MAX3762 is 1Vp-p:

C_{IN} = 3.3nF (to provide LOS assert in 25µs)

C_{AZ} = 82pF (to provide f_{OC} = 1/10 f_C for stability)

C_{FILTER} = 100pF (for a 3MHz integration constant)

R1 = 100kΩ, R2 = 50kΩ (to set LOS assert at -24dBm)

PECL Terminations

The standard PECL termination (50Ω to V_{CC} - 2V) is recommended for best performance and output characteristics. The data outputs operate at high speed, and should always drive transmission lines with 50Ω to 75Ω terminations. Balanced termination is recommended for all outputs.

Figure 5 shows an alternative method for terminating the data outputs. The technique provides approximately 8mA DC bias current, with a 50Ω AC load, for the output termination. This technique is useful for viewing the output on an oscilloscope or changing the PECL reference voltage.

The MAX3762's PECL LOS outputs are relatively slow and do not need 50Ω terminations (although they are capable of driving them). To reduce power, the MAX3762's LOS outputs can be terminated with 500Ω. Figure 6 shows a typical operating circuit for the MAX3762.

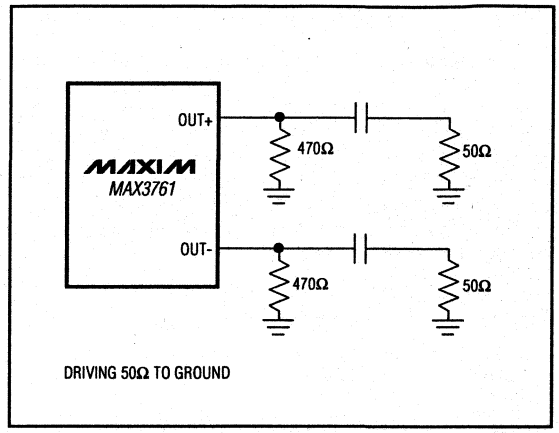


Figure 5. Alternative PECL Termination

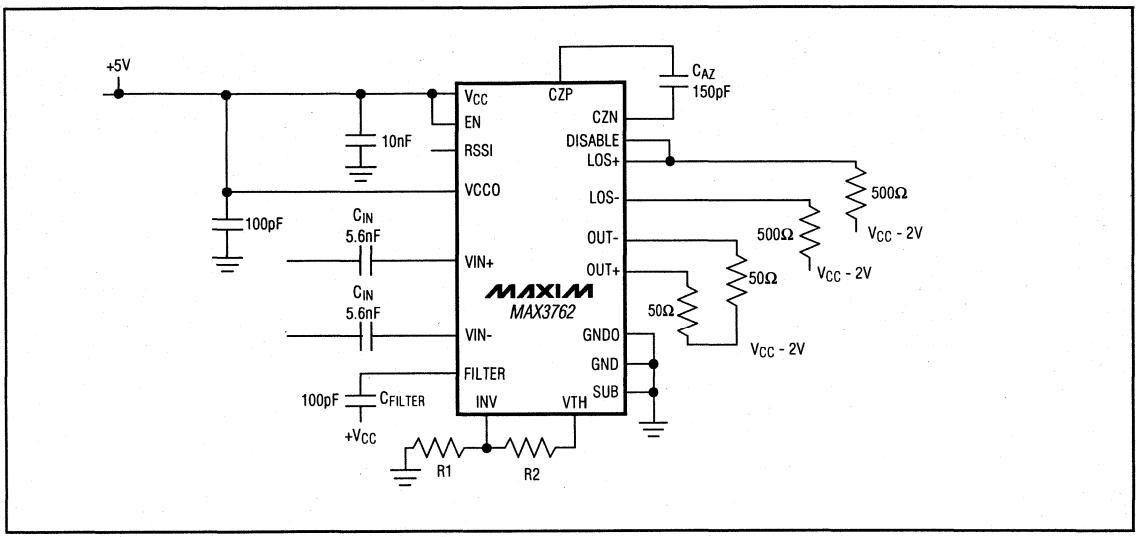
Wire Bonding

For high current density and reliable operation, the MAX3761/MAX3762 use gold metalization. Make connections to the dice with gold wire only, and use ball-bonding techniques (wedge bonding is not recommended). Die-pad size is 4 mils square, with a 6 mil pitch. Die thickness is 12 mils (0.3mm).

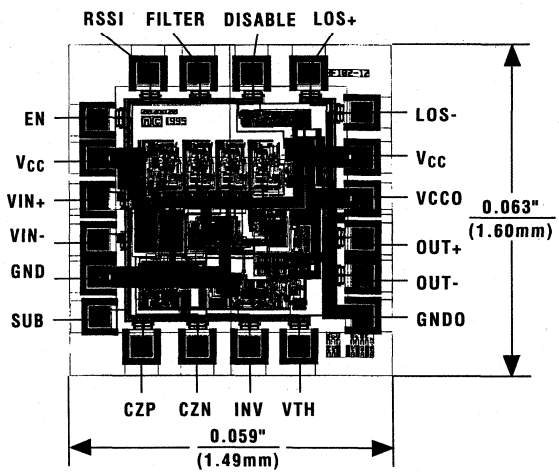
Layout Techniques

The MAX3761/MAX3762 are high-frequency, high-bandwidth circuits. To ensure stability, use good high-frequency layout techniques. Filter voltage supplies, and keep ground connections short. Use multiple vias where possible. Use controlled-impedance transmission lines to connect the MAX3761/MAX3762 data outputs to other circuits.

Typical Operating Circuits (continued)



Chip Topography



TRANSISTOR COUNT: 961
SUBSTRATE CONNECTED TO SUB

MAXIM

Appendix

Evaluation Kits/Design Software Tables A-2
Packaged Products A-5
Surface-Mount Products A-6
Die and Wafer Products A-7
Maxim's /883 and High-Reliability Program A-9
Maxim's Military Program A-11
Product Numbering Systems A-12
Package Information A-13

Part Number	EV Kit	Order Free Sample*	EV Kit Price†($)
A/D CONVERTERS			
MAX100	MAX100EVKIT		†††
MAX1002‡	MAX1002EVKIT		†††
MAX1003‡	MAX1002EVKIT	MAX1003CAX	†††
MAX101A	MAX101AEVKIT		†††
MAX104‡	MAX104EVKIT		††
MAX110	MAX110EVKIT-DIP		55.00
	MAX110EVC32-DIP**		150.00
MAX111	MAX110EVKIT-DIP	MAX111CPE	55.00
	MAX110EVC32-DIP**	MAX111CPE	150.00
MAX1110‡	MAX1110EVKIT-DIP		††
MAX1112‡	MAX1110EVKIT-DIP	MAX1112CPP	††
MAX1114	MAX1114EVKIT		†††
MAX1125	MAX1114EVKIT	—	†††
MAX117	MAX117EVKIT-DIP		48.00
MAX118	MAX117EVKIT-DIP	MAX118PCPI	48.00
MAX1150‡	MAX1150EVKIT		†††
MAX1151‡	MAX1150EVKIT	MAX1151CZS	†††
MAX1160‡	MAX1160EVKIT		†††
MAX1161‡	MAX1160EVKIT	MAX1161CPI	†††
MAX1170	MAX1170EVKIT		†††
MAX1171	MAX1170EVKIT	MAX1171CDJ	†††
MAX1172	MAX1170EVKIT	MAX1172CDJ	†††
MAX120	MAX120EVKIT-DIP		82.00
MAX1202‡	MAX1202EVKIT-DIP		††
MAX121	MAX121EVKIT-DIP		85.00
MAX122	MAX120EVKIT-DIP	MAX122BCNG	82.00
MAX125	MAX125EVKIT-DIP		††
MAX126	MAX125EVKIT-DIP	MAX126BCPL	††
MAX1241	MAX1241EVKIT		††
MAX1247	MAX1247EVKIT		††
MAX132	MAX132EVKIT-DIP**		95.00
MAX133	MAX134EVBRD-DIP	MAX133CPL	125.00
MAX134	MAX134EVBRD-DIP		125.00
MAX147	MAX147EVKIT-DIP		55.00
	MAX147EVC16-DIP**		150.00
	MAX147EVC32-DIP**		150.00
MAX152	MAX152EVKIT-DIP		65.00
MAX153	MAX152EVKIT-DIP	MAX153CPP	65.00
MAX155	MAX155EVKIT-DIP**		95.00
MAX176	MAX176EVKIT-DIP		82.00
MAX180	MAX180EVKIT-DIP**		95.00
MAX181	MAX180EVKIT-DIP**	MAX181CCPL	95.00
MAX186	MAX186EVKIT-DIP		55.00
	MAX186EVSYS-DIP**		150.00
MAX187	MAX187EVKIT-DIP		55.00
	MAX187EVC16-DIP**		150.00
MAX188	MAX186EVKIT-DIP	MAX188DCPP	55.00
	MAX186EVSYS-DIP**	MAX188DCPP	150.00
MAX189	MAX187EVKIT-DIP	MAX189BCPA	55.00
	MAX187EVC16-DIP**	MAX189BCPA	150.00
MAX190	MAX190EVKIT-DIP**		95.00
MAX191	MAX191EVKIT-DIP		55.00
	MAX191EVSYS-DIP**		150.00
MAX194	MAX194EVKIT-DIP		55.00
	MAX194EVC16-DIP**		150.00
MAX195	MAX195EVKIT-DIP		55.00
	MAX195EVC16-DIP**		150.00
MAX196	MAX196EVKIT-DIP		55.00
MAX197	MAX197EVKIT-DIP		55.00
	MAX197EVC16-DIP**		150.00
	MAX197EVC32-DIP**		150.00
MAX198	MAX196EVKIT-DIP	MAX198BCNI	55.00
MAX199	MAX197EVKIT-DIP	MAX199BCNI	55.00
	MAX197EVC16-DIP**	MAX199BCNI	150.00
	MAX197EVC32-DIP**	MAX199BCNI	150.00
ANALOG FILTERS			
MAX274	MAX274EVKIT-DIP		20.00
MAX275	MAX274EVKIT-DIP	MAX275BCPP	20.00
D/A CONVERTERS			
MAX555	MAX555EVKIT		195.00
FUNCTION GENERATOR			
MAX038	MAX038EVKIT-DIP		89.00
INTERFACE PRODUCTS			
MAX212	MAX212EVKIT-SO		38.00
OP AMPS/VIDEO PRODUCTS			
MAX4100	MAX4100EVKIT-SO		31.25
MAX4101	MAX4100EVKIT-SO	MAX4101ESA	31.25
MAX4102	MAX4103EVKIT-SO	MAX4102ESA	31.25
MAX4103	MAX4103EVKIT-SO		31.25
MAX4106	MAX4106EVKIT-SO		31.25
MAX4107	MAX4106EVKIT-SO	MAX4107ESA	31.25
MAX4108	MAX4108EVKIT-SO		31.25
MAX4109	MAX4108EVKIT-SO	MAX4109ESA	31.25
MAX4111	MAX4121EVKIT-SO	MAX4111CSA	31.25
MAX4112	MAX4112EVKIT-SO		31.25

* Some kits are used to evaluate more than one device. In these cases, order the indicated EV kit and a free sample of the device you wish to evaluate.

** Includes microcontroller

‡ Future product—contact factory for pricing and availability.

†† Future EV kit—contact factory for pricing and availability.

††† Contact factory for pricing

Part Number	EV Kit	Order Free Sample*	EV Kit Price†($)
OP AMPS/VIDEO PRODUCTS (cont.)			
MAX4113	MAX4112EVKIT-SO	MAX4113ESA	31.25
MAX4117	MAX4117EVKIT-SO		31.25
MAX4118	MAX4117EVKIT-SO	MAX4118ESA	31.25
MAX4121	MAX4121EVKIT-SO		31.25
MAX4135	MAX4135EVKIT-SO		31.25
MAX4136	MAX4135EVKIT-SO	MAX4136EWG	31.25
MAX4137	MAX4135EVKIT-SO	MAX4137EWG	31.25
MAX4138	MAX4135EVKIT-SO	MAX4138EWG	31.25
MAX4141	MAX4141EVKIT-SO		31.25
MAX4144	MAX4144EVKIT-SO		31.25
MAX4147	MAX4147EVKIT-SO		31.25
MAX4178	MQX4278EVKIT-SO	MAX4178ESA	31.25
MAX4221	MAX4221EVKIT-SO		31.25
MAX4278	MAX4278EVKIT-SO		31.25
MAX458	MAX459EVKIT-DIP	MAX458CPL	72.00
MAX459	MAX459EVKIT-DIP		72.00
MAX464	MAX466EVKIT-SO	MAX464CWI	67.00
MAX466	MAX466EVKIT-SO		67.00
MAX477	MAX477EVKIT-SO		31.25
MAX496	MAX497EVKIT-SO	MAX496CPE	60.00
MAX497	MAX497EVKIT-SO		60.00
POWER SUPPLIES			
MAX1610	MAX1611EVKIT-SO	MAX1610CSE	†††
MAX1611	MAX1611EVKIT-SO		†††
MAX1624‡	MAX1624EVKIT-SO		††
MAX1625‡	MAX1624EVKIT-SO	MAX1625ESE	††
MAX1626	MAX1626EVKIT-SO		35.00
MAX1627	MAX1626EVKIT-SO	MAX1627ESA	35.00
MAX1630	MAX1630EVKIT-SO		†††
MAX1631	MAX1631EVKIT-SO		†††
MAX1632	MAX1632EVKIT-SO		†††
MAX1633	MAX1630EVKIT-SO	MAX1633CAI	†††
MAX1634	MAX1631EVKIT-SO	MAX1634CAI	†††
MAX1635	MAX1632EVKIT-SO	MAX1635CAI	†††
MAX1640‡	MAX1640EVKIT		††
MAX1642‡	MAX1642EVKIT		††
MAX1643‡	MAX1642EVKIT	MAX1643EUA	††
MAX1647‡	MAX1647EVKIT-SO		††
MAX1648‡	MAX1647EVKIT-SO	MAX1648ESE	††
MAX1649	MAX1649EVKIT-SO		35.00
MAX1651	MAX1649EVKIT-SO	MAX1651CSA	35.00
MAX1771	MAX1771EVKIT-SO		35.00
MAX2003	MAX2003AEVKIT-SO	MAX2003CSE	125.00
MAX2003A	MAX2003AEVKIT-SO		125.00
MAX606	MAX606EVKIT-MM		60.00
MAX607	MAX606EVKIT-MM	MAX607EUA	60.00
MAX608	MAX608EVKIT-SO		35.00
MAX619	MAX619EVKIT-SO		25.00
MAX639	MAX639EVKIT-DIP		20.00
	MAX639EVKIT-SO		20.00
MAX640	MAX639EVKIT-DIP	MAX640CPA	20.00
	MAX639EVKIT-SO	MAX640CSA	20.00
MAX653	MAX639EVKIT-DIP	MAX653CPA	20.00
	MAX639EVKIT-SO	MAX653CSA	20.00
MAX662A	MAX662EVKIT-SO	MAX662ACSA	20.00
MAX688	MAX688EVKIT-SO		60.00
MAX689	MAX688EVKIT-SO	MAX689CSA	60.00
MAX710‡	MAX710EVKIT		††
MAX711‡	MAX710EVKIT	MAX711ESE	††
MAX712	MAX712EVKIT-DIP		60.00
MAX713	MAX712EVKIT-DIP	MAX713CPE	60.00
MAX717	MAX718EVKIT-SO	MAX717CSE	30.00
MAX718	MAX718EVKIT-SO		30.00
MAX719	MAX718EVKIT-SO	MAX719CSE	30.00
MAX722	MAX722EVKIT-SO		30.00
MAX723	MAX722EVKIT-SO	MAX723CSE	30.00
MAX730A	MAX738EVKIT-DIP	MAX730ACPA	20.00
	MAX738EVKIT-SO	MAX730ACSA	20.00
MAX731	MAX731EVKIT-DIP		20.00
MAX732	MAX752EVKIT-DIP	MAX732CPA	20.00
	MAX732EVKIT-SO		20.00
MAX733	MAX752EVKIT-DIP	MAX733CPA	20.00
MAX734	MAX734EVKIT-SO		20.00
MAX736	MAX739EVKIT-DIP	MAX736CPD	20.00
MAX737	MAX739EVKIT-DIP	MAX737CPD	20.00
MAX738A	MAX738EVKIT-DIP	MAX738ACPA	20.00
	MAX738EVKIT-SO	MAX738ACWE	20.00
MAX739	MAX739EVKIT-DIP		20.00
MAX742	MAX742EVKIT-SO		50.00
MAX743	MAX743EVKIT-DIP		20.00
MAX744A	MAX738EVKIT-DIP	MAX744ACPA	20.00
	MAX738EVKIT-SO	MAX744ACWE	20.00
MAX748A	MAX738EVKIT-DIP	MAX748ACPA	20.00
	MAX738EVKIT-SO	MAX748ACWE	20.00
MAX749	MAX749EVKIT-SO		20.00
MAX750A	MAX758EVKIT-DIP	MAX750ACPA	20.00
	MAX758EVKIT-SO	MAX750ACSA	20.00

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†† Future EV kit—contact factory for pricing and availability.

††† Contact factory for pricing.

Evaluation Kits/Design Software

Part Number	EV Kit	Order Free Sample*	EV Kit Price†($)
MAX752	MAX752EVKIT-DIP		20.00
MAX756	MAX756EVKIT-SO		25.00
MAX757	MAX756EVKIT-SO	MAX757CSA	25.00
MAX758A	MAX758EVKIT-DIP	MAX758ACPA	20.00
	MAX758EVKIT-SO	MAX758ACWE	20.00
MAX759	MAX759LCDKIT-SO		30.00
	MAX739EVKIT-DIP	MAX759CPD	20.00
MAX761	MAX761EVKIT-SO		25.00
MAX762	MAX761EVKIT-SO	MAX762CSA	25.00
MAX763A	MAX738EVKIT-DIP	MAX763ACPA	20.00
	MAX738EVKIT-SO	MAX763ACSA	20.00
MAX764	MAX764EVKIT-SO		35.00
MAX765	MAX764EVKIT-SO	MAX765CSA	35.00
MAX766	MAX764EVKIT-SO	MAX766CSA	35.00
MAX767	MAX767EVKIT-SO		60.00
MAX770	MAX770EVKIT-SO		35.00
MAX771	MAX770EVKIT-SO	MAX771CSA	35.00
MAX772	MAX770EVKIT-SO	MAX772CSA	35.00
MAX774	MAX774EVKIT-SO		35.00
MAX775	MAX774EVKIT-SO	MAX775CSA	35.00
MAX776	MAX774EVKIT-SO	MAX776CSA	35.00
MAX777L	MAX778LEVKIT-SO	MAX777LCSA	25.00
MAX778L	MAX778LEVKIT-SO		25.00
MAX779L	MAX778LEVKIT-SO	MAX779LCSA	25.00
MAX782	MAX782EVKIT-SO		95.00
MAX783	MAX783EVKIT-SO		95.00
MAX786	MAX786EVKIT-SO		95.00
MAX796	MAX796EVKIT-SO		60.00
MAX797	MAX797EVKIT-SO		60.00
MAX799	MAX796EVKIT-SO	MAX799CSE	60.00
MAX830	MAX831EVKIT-SO	MAX830CWE	60.00
MAX831	MAX831EVKIT-SO		60.00
MAX832	MAX831EVKIT-SO	MAX832CWE	60.00
MAX833	MAX831EVKIT-SO	MAX833CWE	60.00
MAX840	MAX840EVKIT-SO		35.00
MAX843	MAX840EVKIT-SO	MAX843ISA	35.00
MAX844	MAX840EVKIT-SO	MAX844ISA	35.00
MAX845	MAX845EVKIT-MM		35.00
MAX846‡	MAX846EVKIT		75.00
MAX848‡	MAX848EVKIT-SO		†††
MAX849	MAX848EVKIT-SO	MAX849ESE	†††
MAX850	MAX850EVKIT-SO		35.00
MAX851	MAX850EVKIT-SO	MAX851ISA	35.00
MAX852	MAX850EVKIT-SO	MAX852ISA	35.00
MAX853	MAX850EVKIT-SO	MAX853ISA	35.00
MAX856	MAX856EVKIT-MM		35.00
MAX857	MAX856EVKIT-MM	MAX857CUA	35.00
MAX858	MAX856EVKIT-MM	MAX858CUA	35.00
MAX859	MAX856EVKIT-MM	MAX859CUA	35.00
MAX863‡	MAX863EVKIT-SO		††
MAX866	MAX866EVKIT-MM		35.00
MAX867	MAX866EVKIT-MM	MAX867EUA	35.00
MAX877L	MAX877LEVKIT-SO		25.00
MAX878L	MAX877LEVKIT-SO	MAX878LCSA	25.00
MAX879L	MAX877LEVKIT-SO	MAX879LCSA	25.00
MAX887	MAX887EVKIT-SO		†††
WIRELESS PRODUCTS (High Frequency)			
MAX2101	MAX2101EVKIT-SO		†††
MAX2402	MAX2402EVKIT-SO		†††
MAX2430	MAX2430EVKIT-SO		††
MAX2450	MAX2450EVKIT-SO		†††
MAX2451	MAX2450EVKIT-SO		†††
MAX2452	MAX2450EVKIT-SO		†††
MAX2611	MAX2611PCB		††
MAX2630‡	MAX2633PCB		††
MAX2631‡	MAX2633PCB		††
MAX2632‡	MAX2633PCB		††
MAX2633‡	MAX2633PCB		††
MAX2650	MAX2650PCB		††

Design Software

Part Number	Description	Price† ($)
MAX260SOFT	Filter design software for MAX260–MAX268	20.00
MAX274SOFT	Filter design software for MAX274/MAX275	5.00

Description	Price† ($)
Op-Amp/Comparator P-Spice Models	FREE

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†† Future EV kit—contact factory for pricing and availability.

††† Contact factory for pricing.

Wafer Inspection

All wafers are fabricated using standard processes with extremely tight control. Each wafer must pass numerous in-process checkpoints for oxide thickness, critical dimensions, pin-hole densities, and other requirements. And, each must comply with Maxim's demanding electrical and physical specifications.

Finished wafers are optically inspected for physical defects. They are then parametrically tested to ensure full conformity to Maxim's specifications. Our precision parametric measurement capability ensures reliability and reproducibility in analog circuits. We believe this quality-control technology to be the best in the industry, capable of resolving current levels below 1pA and capacitance less than 1pF. Maxim's proprietary software allows automatic measurement of subthreshold characteristics, fast surface-state density, and other parameters that are crucial to predicting long-term stability and reliability.

Every Maxim wafer is subject to this rigorous screening at no premium to our customers.

Testing

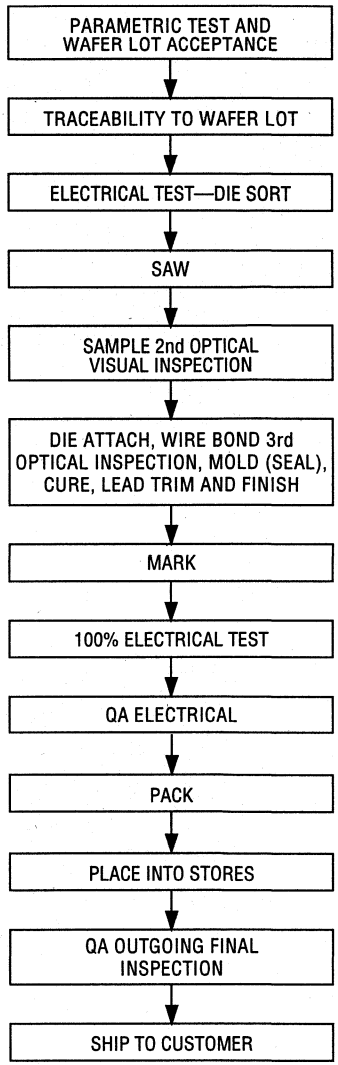
Maxim routinely monitors the products and processes through qualification testing, including Life Test, 85/85, Pressure Pot, Temperature Cycling, Long-Term Storage, and HAST testing. See Maxim's full *Product Reliability Report* (RR-1J) for more information.

Sophisticated testing is an integral part of delivering the highest quality data-acquisition products. Maxim's analog test capability is a significant improvement in accuracy, noise performance, and speed compared to current industry standards. This provides our customers with assurance that they will receive the part they paid for every time, without fail.

Product Conditioning and Qualification

Maxim also runs parts through qualification cycles, including accelerated life tests equivalent to 20 million operating hours and pressure/humidity cycles (85°C/85%).

Packaged-Unit Process Flow



A

Surface-Mount Products

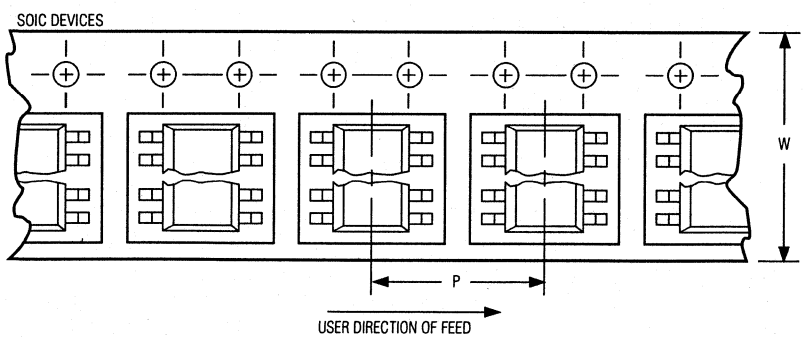
Maxim is committed to providing high-quality, high-reliability 8-pin to 160-pin plastic surface-mount products. Nearly every monolithic device is offered in a surface-mount package. Except for 100% burn-in and cold test, they are processed through the same manufacturing flow as the dual-in-line (DIP) plastic devices and are tested to the same stringent electrical and visual AQL levels. They receive the same product conditioning and lot qualification as the DIPs.

Surface-Mount Packages in Reeled Tape

Maxim surface-mount packages are shipped in antistatic plastic rails. For customers using automatic placement systems, parts also come mounted in pockets on embossed tape. The tape is wound and shipped on reels.

The table and diagram on this page indicate the tape sizes used for various package types and the basic orientation convention used. Further tape and reel specifications can be found in the Electronic Industries Association (EIA) standard 481.

COMPONENT		TAPE SIZE mm (W)	PART PITCH mm (P)
Package	Pins		
SOIC	8	12	8
	14	16	8
	16	16	8
SOIC	16	16	12
	18	24	12
	20	24	12
	24	24	12
	28	24	12
PLCC	20	16	12
	28	24	16
	44	32	24
QFP	44	24	16
SOT	3	8	4
	4	8	4
SSOP	20	16	12
	24	16	12
	28	16	12
µMAX	8	12	8
TQFP	32	16	12
	48	16	12



Die and Wafer Products

All of Maxim's standard products are available in die and wafer form. Every diffusion lot committed to die/wafer sales is qualified through a die sample that is assembled into packaged units. This sample is then subjected to "Packaged Unit Process Flow," the standard that ensures lot quality and reliability.

Electrical Specifications

All material committed to die/wafer sales is 100% electrically probed using Maxim's sophisticated test equipment. Most parameters tested are checked to limits that are more stringent than the data sheet's +25°C worst-case limits.

Generally, the parameters or parameter limits listed in the product data sheets are tested during electrical probe. However, some parameters are impossible to test, or to test with absolute accuracy on unassembled product. Information regarding any of these parameters or parameter limits may be obtained from the factory.

Physical Specifications

PARAMETER	VALUE	UNITS
Chip Thickness Backlapped Wafers	15 ±1	mils
Die Length/Width Tolerance	±1	mils
Bonding Pad Dimensions (minimum)	typical min = 3.5 x 3.5	mils
Bonding Pad and Interconnect Material Thickness	10 to 12	kÅ
Storage Temperature	-40 to +150	°C
Operating Temperature	0 to +70	°C

Die and wafers are visually inspected according to MIL-STD-883, Method 2010, Condition B, with modifications reflecting CMOS requirements.

Each die surface is protected by a passivation layer, except for bonding pads and scribe lines. Surface passivation is removed from bonding-pad areas by plasma etching. The bonding pads may appear discolored at low magnification due to the aluminum's surface roughness after the etching process.

Maxim guarantees die and wafer AQL levels as follows:

Visual.....1.0%
Functional Electrical Testing 0.65%
Parametric DC Testing 2.5%
Untested Parameters 6.5%

Assembly Procedures

Handling

Maxim recommends that die and wafers be stored in a clean, dry environment—preferably an inert gas such as nitrogen. Extreme care should be taken when handling die. An unclean environment or mishandling may result in electrical and visual failure.

Die Attach

For eutectic die attach, we recommend using a 98% gold/2% silicon preform, at a die-attach temperature between 385°C and 435°C. To prevent oxidation, die attach should be done in a gaseous nitrogen ambient atmosphere. For epoxy die attach, the epoxy cure temperature should not exceed 150°C.

Bonding

When thermosonic or thermocompression gold ball bonding, use 1.0 or 1.3 mil diameter, 99.99% pure gold wire. When ultrasonic bonding, use 1.0 or 1.25 mil diameter, 99% aluminum/1% silicon wire.

Standard Die and Wafer Carrier Package

Figures 1 and 2 show how die and wafers are packaged for shipping:

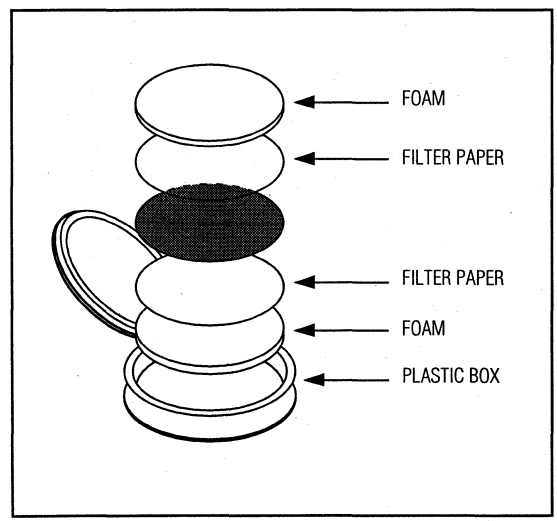


Figure 1. Wafer Carrier Package

A

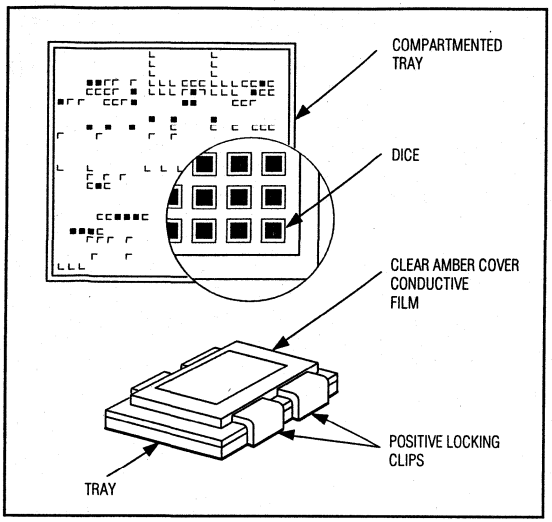


Figure 2. Die Carrier Package

Changes

Maxim reserves the right to improve device geometries and manufacturing processes without prior notice. These improvements may result in slight changes in geometry, die electrical limits, pad layouts, or maximum die size. These changes are kept to a minimum, and we strive to notify customers whenever possible.

User Responsibility

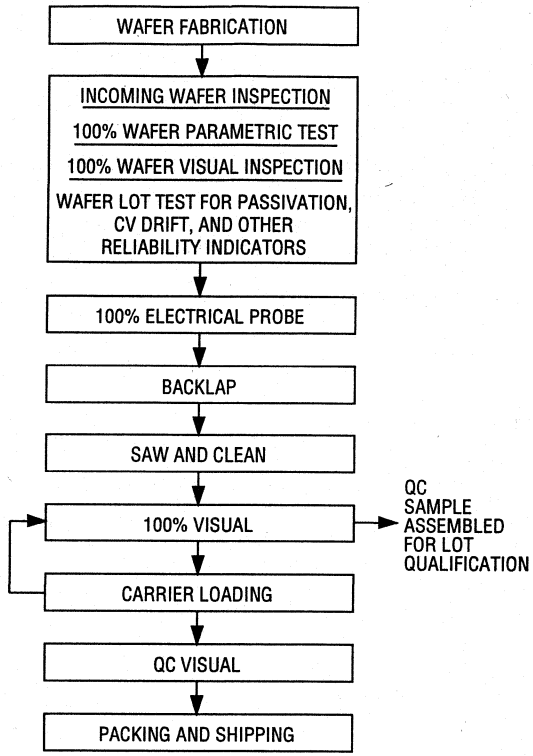
Written notification of any nonconformance by Maxim or Maxim's dice specifications must be made within 75 days of the date the die is shipped to the user. Maxim assumes no responsibility for the die after 75 days or after further user processing such as, but not limited to, die attach or wire bonding.

Ordering Information

A select group of standard products is available in die and wafer form. Contact the factory for availability. Die orders are identified by a "/D" suffix. Example: ICL7109C/D.

When ordering dice as wafers, replace the "D" with a "W" in the part number. Example: MAX7231C/D die = MAX7231C/W wafer.

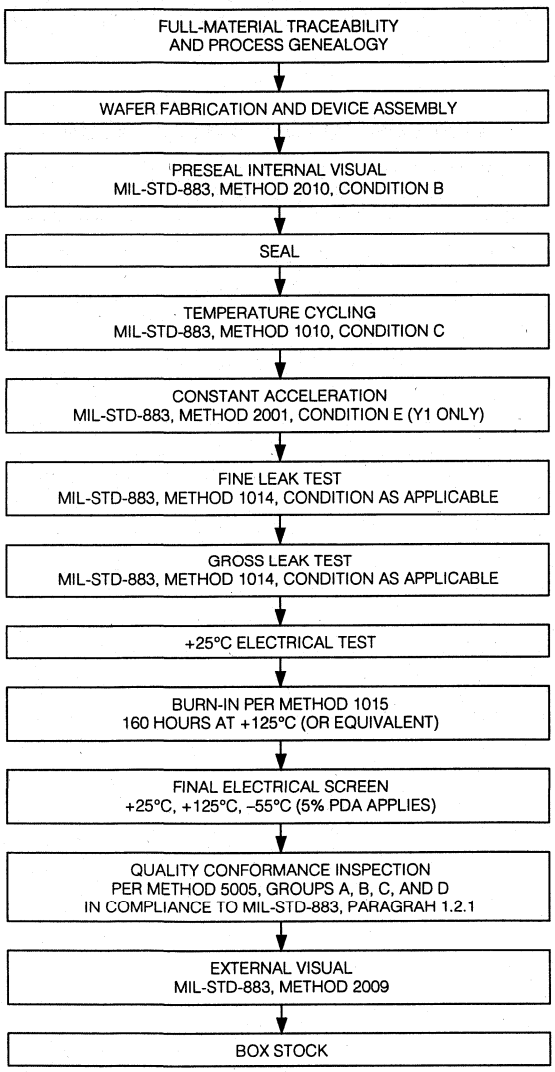
Die Process Flow



/883 Flow

Maxim's /883 program is fully compliant to MIL-STD-883, paragraph 1.2.1. Environmental and electrical screening are performed per Method 5004, Class B of MIL-STD-883. Quality conformance inspection is performed per method 5005 (Groups A, B, C, and D).

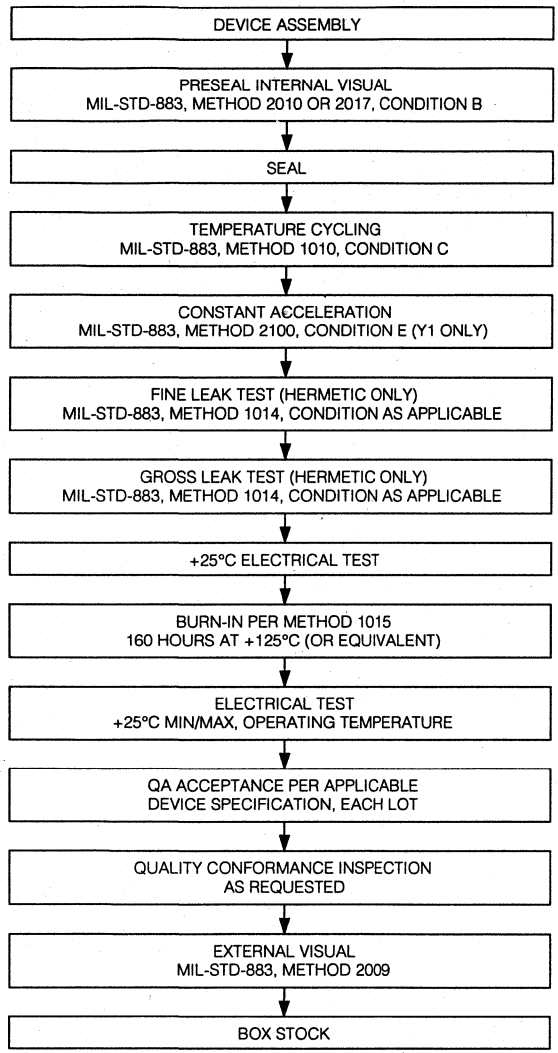
/883B Process Flow



/HR Flow

Maxim's High Reliability (/HR) flow is offered for hybrid products as well as for products that have not yet been fully certified compliant to MIL-STD-883, and are therefore noncompliant. The /HR flow will not be offered for parts certified to MIL-STD-883. As shown in the adjacent flow chart, the /HR process flow closely follows the steps and requirements of the MIL-STD-883 flow. Product processed to this flow is not documented in as much detail, nor does it have to adhere to the operating temperature range required by MIL-STD-883. The /HR flow may also be used to screen product over the commercial (0°C to +70°C) or extended (–40°C to +85°C) temperature ranges. This flow applies to hermetic packaged product only. It is Maxim's experience that this flow is desired by companies having older government projects or projects requiring an inherently higher reliability screening for critical application environments. Full QCI testing will be performed when requested. Only Group A will be performed per each inspection lot.

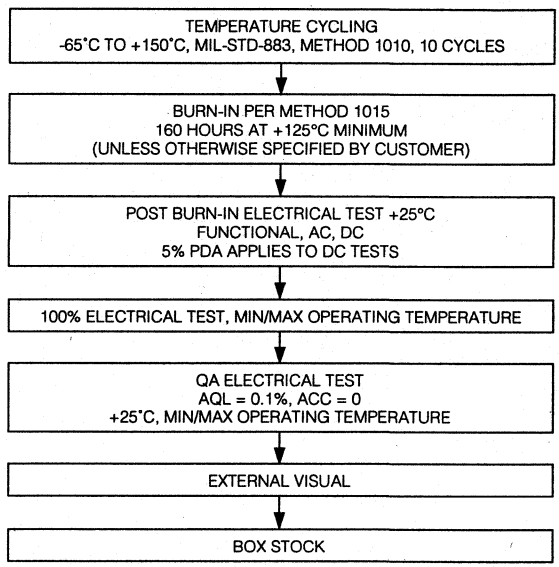
/HR Process Flow



Rugged Plastic Flow

In addition to the /883B and /HR screening flows, Maxim offers an extended rugged-plastic screening flow for plastic-encapsulated packages including SOIC package types. Products screened to this flow can be used in high-reliability applications when hermetically sealed devices screened to MIL-STD-883 may not be justified. SOICs with full burn-in and screening not only offer excellent reliability, but also save valuable PC board space. Customers should contact the factory for availability of the specific device types currently offered.

Rugged-Plastic Process Flow



DESC Approved Devices to Standard Military Drawings (SMDs) Currently Available

MAXIM P/N	SMD NUMBER
MAX1044	5962-38707
MAX1232	5962-94514
MAX1259	5962-93264
MAX220/22/32A/42/43	5962-94565
MAX230/1/2/4/6-9	5962-89877
MAX280	5962-91595
MAX310/311	5962-94556
MAX333	5962-93180
MAX358	77052
MAX359	5962-85131
MAX4420/4429	5962-88770
MAX452-455	5962-94512
MAX500	5962-94527
MAX502	5962-88767
MAX532	5962-95667
MAX543	5962-92345
MAX630	5962-94540
MAX631/632/633	5962-92141
MAX634	5962-92124
MAX638	5962-92127
MAX641	5962-93254
MAX660	5962-94632
MAX663/4/6/7	5962-92126
MAX674	5962-94681
MAX680	5962-93120
MAX690/692/694	5962-90712
MAX691/693/695	5962-90711
MAX696/697	5962-93125
MAX705-708	5962-93267
MAX731/732/733	5962-94621
MAX738	5962-93121
MAX813L	5962-93267
MAX8211/8212	5962-90811
MX536A	5962-89805
MX574A	5962-85127
MX580	5962-86861
MX584	5962-38128
MX7226	5962-87802
MX7524	5962-87700
MX7528	5962-87701
MX7537	5962-87763
MX7541	5962-89481
MX7545	5962-87702
MX7547	5962-89657
MX7572	5962-87591
MX7574	5962-89616
MX7820	5962-88650
MX7824/7828	5962-88764
MXL1062	5962-91595
DG201A	77053
DG403	5962-89763
DG405	5962-89961
DG408/409	5962-92042
DG411/412/413	5962-90731
DG417/418/419	5962-90737
DG441/442	5962-92041
DG506A/7A/9A	5962-85131
DG508A	77052
DG528	5962-87689
HI-201	77053
ICL7660A	5962-38707
ICL7667	5962-87660
IH5040-5045	81006
IH5047	81006
IH5140-5145	81006
IH5148/5149	81006
IH5150/5151	81006
REF01	5962-89581
REF02	85514
TSC426/427/428	5962-88503

Parts Currently /883 Compliant

MAX1044
MAX122
MAX1232
MAX1259
MAX154/158
MAX160/161
MAX170/172
MAX176
MAX180/181
MAX186/188
MAX220/222
MAX230/231/232
MAX232A
MAX234
MAX236-239
MAX242/243
MAX274
MAX280
MAX291
MAX310/311
MAX333
MAX358/359
MAX378/379
MAX4420/4426-9
MAX452-455
MAX481/483/485
MAX500
MAX502
MAX516
MAX526/527
MAX532
MAX543
MAX626/627/628
MAX630-634/638
MAX641A/649
MAX660
MAX663-667
MAX674
MAX680
MAX690-697
MAX690A/692A
MAX691A/693A
MAX705-708
MAX730-733
MAX738
MAX758
MAX805L
MAX813L
MAX8211/8212
MX536A
MX565/566
MX574A
MX580/581/584
MX674A
MX7225/26/28
MX7501/2/3
MX7520/1/4/8
MX7533/7537
MX7541/2/3/5/7
MX7549
MX7572/7574
MX7628
MX7820/1/4/8
MXL1062
DG200A/201A/202
DG300A-309
DG381A/4A/7A
DG390A
DG401/403/405
DG406-409
DG411/412/413
DG417/418/419
DG441/442
DG506A-509A
DG528/529
HI-201/201HS
HI-0201/0201HS
ICL7660A/7667
IH5040-5049
IH5050/5051
IH5140-5145
IH5147/5148/5151
IH5341/5352
OP07
REF01/02
TSC426/427/428

A

Proprietary Numbering System

Maxim's proprietary product introductions are increasing at a significant rate. The devices are grouped into categories, according to their functions. Maxim currently adds a "MAX" prefix to the part's unique number. The categories are as follows (with some exceptions):

MAX100-199 Analog-to-Digital Converters
MAX200-299 Interface Products and Analog Filters
MAX300-399 Analog Switches and Multiplexers
MAX400-499 Op Amps, Buffers, and Video Amplifiers
MAX500-599 Digital-to-Analog Converters
MAX600-699 Power-Supply Circuits and Voltage Ref.
MAX700-799 µP Peripherals and Display Drivers
MAX800-899 µP Supervisory
MAX900-999 Comparators

Within each category, blocks of numbers are reserved for subgroups.

3-Letter Suffixes

EXAMPLE:
MAX358CPD

- C — Operating Temperature Range
- P — Package Type
- D — Number of Pins

4-Letter Suffixes

When a part has a four-letter suffix, the first letter of the suffix denotes product grade. For example, the first "A" in MAX631ACPA indicates 5% output accuracy; the remaining three letters denote temperature range, package type, and number of pins. Therefore, the MAX631ACPA has 5% output accuracy, operates over the 0°C to +70°C range, comes in a plastic DIP package, and has eight pins.

Temperature Ranges

"C"	0°C to +70°C	"E"	-40°C to +85°C
"I"	-20°C to +85°C	"M"	-55°C to +125°C

Package Type

"A" SSOP (Shrink Small-Outline Package)
"B" CERQUAD
"C" TO-220, TQFP (Thin Quad Flat Pack)
"D" Ceramic Sidebraze
"E" QSOP (Quarter Small-Outline Package)
"F" Ceramic Flat Pack
"H" Module, SBGA (Super Ball Grid Array)
"J" CERDIP Dual-In-Line
"K" TO-3, PPGA
"L" LCC (Leadless Ceramic Chip Carrier)
"M" MQFP (Metric Quad Flat Pack)
"N" Narrow Plastic Dual-In-Line
"P" Plastic Dual-In-Line
"Q" PLCC (Plastic Leaded Chip Carrier)
"R" Narrow CERDIP (300 mil)
"S" Small Outline (150 mil), TO-52 (2 or 3 leads)
"T" TO-5 Type (also TO-99, TO-100)
"U" TSSOP, µMAX, SOT
"V" TO-39
"W" Small Outline, Wide (300 mil)
"X" JLCC (J Leaded Ceramic Chip Carrier)
"Y" Narrow Sidebraze (300 mil)
"Z" TO-92, MQUAD
"/D" Dice
"/PR" Rugged Plastic
"/W" Wafer

Number of Pins

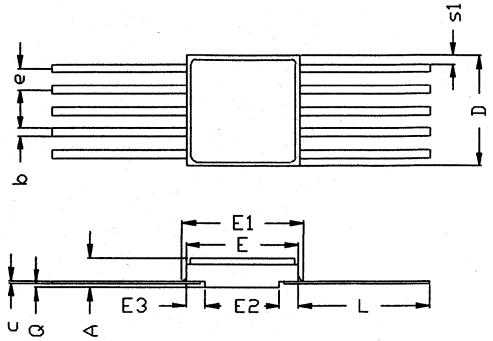
"A"	8	"N"	18
"B"	10, 64	"O"	42
"C"	192	"P"	20
"D"	14	"Q"	2, 100
"E"	16	"R"	3, 84
"F"	256	"S"	4, 80
"G"	24	"T"	6, 160
"H"	44	"U"	60
"I"	28	"V"	8 (0.200" pin circle, isolated case)
"J"	32	"W"	10 (0.230" pin circle, isolated case)
"K"	5, 68	"X"	36
"L"	40	"Y"	8 (0.200" pin circle, isolated case)
"M"	7, 48	"Z"	10 (0.230" pin circle, isolated case)

Second-Source Numbering System

In most cases, Maxim's part number for a second-source product follows the industry's most widely accepted numbering system for that particular part, rather than our own convention. This includes the most commonly recognized prefix as well as the original designators for product grade, temperature range, package type, and number of pins.

Maxim frequently supplies second-source products in packages or temperature ranges that are not supplied by other manufacturers. Whenever possible, these devices are given a part number that follows the original numbering convention.

FPACKPO EPS1



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.045	0.115	1.14	2.29
b	0.010	0.022	0.25	0.56
c	0.004	0.009	0.10	0.23
D	---	0.290	---	7.11
E	0.240	0.260	6.10	6.60
E1	---	0.300	---	7.62
E2	0.125	---	3.18	---
E3	0.030	---	0.76	---
e	0.050	BSC	1.27	BSC
k	N/A	N/A	N/A	N/A
L	0.250	0.370	6.35	9.40
Q	0.026	0.045	0.66	1.14
s1	0.005	---	0.13	---

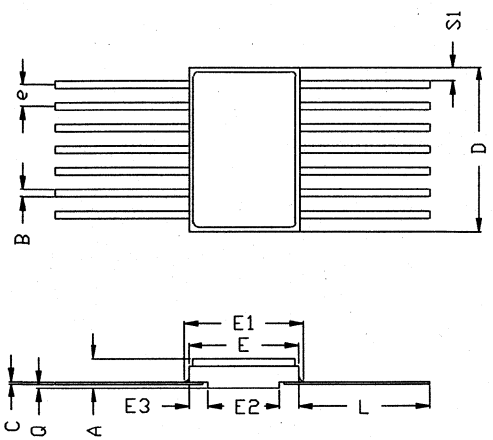
NOTES:
1. CONTROLLING DIMENSION: INCH
2. PACKAGE MEETS 1835 F4A CONFIG. B

MAXIM

10L FLATPACK PACKAGE OUTLINE
MIL 1835 COMPLIANT

F10-2 | 21-0010 | C | 1/1

FPACKPO EPS2



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.045	0.115	1.14	2.92
b	0.015	0.022	0.38	0.56
c	0.004	0.009	0.10	0.23
D	---	0.390	---	9.91
E	0.235	0.260	5.97	6.60
E1	---	0.290	---	7.37
E2	0.125	---	3.18	---
E3	0.030	---	0.76	---
e	0.050	BSC	1.27	BSC
k	---	---	---	---
L	0.270	0.370	6.86	9.40
Q	0.026	0.045	0.66	1.14
s1	0.005	---	0.13	---

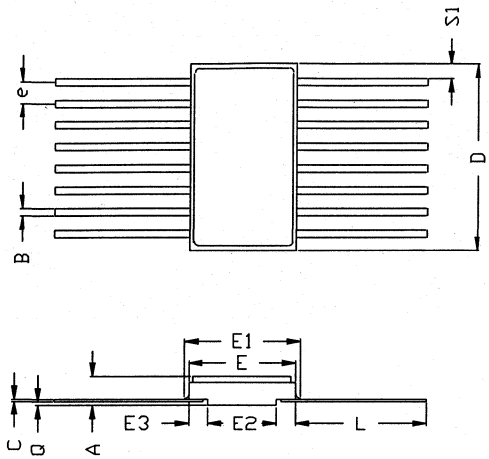
NOTES:
1. CONTROLLING DIMENSION: INCH
2. MEETS MIL STD 1835 F-2A CONFIGURATION B

MAXIM

14L FLATPACK PACKAGE OUTLINE
MIL 1835 COMPLIANT

F14-2 | 21-0011 | A | 1/1

A



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.045	0.115	1.14	2.92
b	0.015	0.022	0.38	0.56
c	0.004	0.009	0.10	0.23
D	---	0.440	---	11.18
E	0.245	0.285	6.22	7.24
E1	---	0.315	---	8.00
E2	0.130	---	3.30	---
E3	0.030	---	0.76	---
e	0.050	BSC	1.27	BSC
k	---	---	---	---
L	0.250	0.370	6.35	9.40
Q	0.026	0.045	0.66	1.14
s1	0.005	---	0.13	---

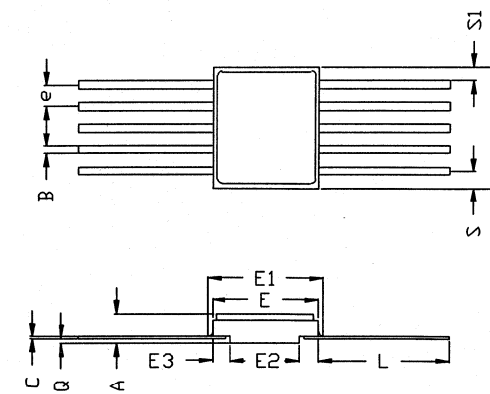
FPACKPO.EPS3

NOTES:
1. CONTROLLING DIMENSION: INCH
2. MEETS MIL STD 1835 F-5A CONFIGURATION B

MAXIM

16L FLATPACK PACKAGE OUTLINE
MIL 1835 COMPLIANT

F16-2 | 21-0013 | A | 1/1



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.045	0.115	1.14	2.92
B	0.010	0.019	0.25	0.48
C	0.003	0.006	0.08	0.15
D	---	0.290	---	7.37
E	0.240	0.260	6.10	6.60
E1	---	0.280	---	7.11
E2	0.125	---	3.18	---
E3	0.030	---	0.76	---
e	0.050	BSC	1.27	BSC
k	---	---	---	---
L	0.250	0.370	6.35	9.40
Q	0.010	0.016	0.25	0.41
S	---	0.045	---	1.14
S1	0.005	---	0.13	---

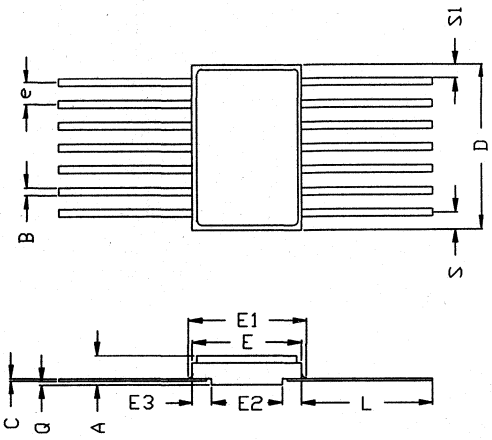
FPACKPO.EPS4

NOTES:
1. CONTROLLING DIMENSION: INCH
2. MEETS 38510 F-4A CONFIGURATION #2 EXCEPT DIMENSION "Q" MIN

MAXIM

18L FLATPACK PACKAGE OUTLINE
NON-COMPLIANT DIMENSIONS

F10-1 | 21-0014 | A | 1/1



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.045	0.115	1.14	2.92
B	0.015	0.019	0.38	0.48
C	0.003	0.006	0.08	0.15
D	---	0.390	---	9.91
E	0.235	0.260	5.97	6.60
E1	---	0.290	---	7.37
E2	0.125	---	3.18	---
E3	0.030	---	0.76	---
e	0.050	BSC	1.27	BSC
k	---	---	---	---
L	0.270	0.370	6.86	9.40
Q	0.012	0.030	0.30	0.76
S	---	0.045	---	1.14
S1	0.005	---	0.13	---

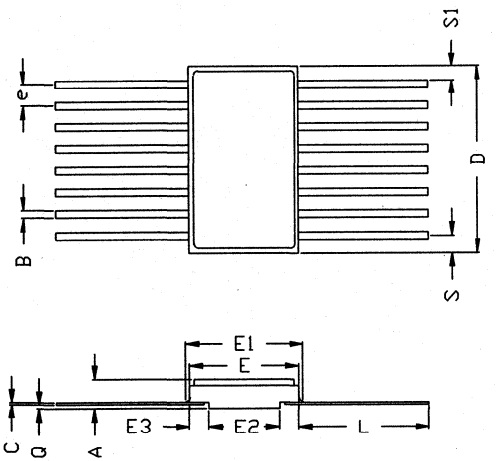
FPACKPO.EPS/6

NOTES:
1. CONTROLLING DIMENSION: INCH
2. MEETS 38510 F-2A CONFIGURATION #2 EXCEPT DIMENSION "Q" MIN

MAXIM

14L FLATPACK PACKAGE OUTLINE
NON-COMPLIANT DIMENSIONS

F14-1 | 21-0012 | A | 1/1



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.045	0.115	1.14	2.92
B	0.015	0.019	0.38	0.48
C	0.003	0.006	0.08	0.15
D	---	0.440	---	11.18
E	0.245	0.285	6.22	7.24
E1	---	0.315	---	8.00
E2	0.130	---	3.30	---
E3	0.030	---	0.76	---
e	0.050	BSC	1.27	BSC
k	---	---	---	---
L	0.250	0.370	6.35	9.40
Q	0.010	0.016	0.25	0.41
S	---	0.045	---	1.14
S1	0.005	---	0.13	---

FPACKPO.EPS/6

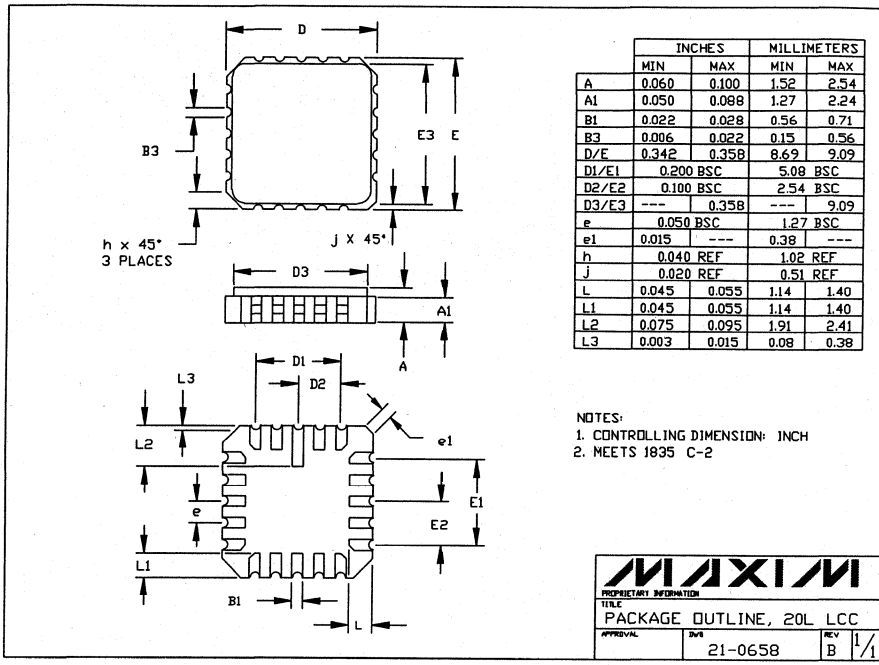
NOTES:
1. CONTROLLING DIMENSION: INCH
2. MEETS 38510 F-5A CONFIGURATION #2 EXCEPT DIMENSION "Q" MIN

MAXIM

16L FLATPACK PACKAGE OUTLINE
NON-COMPLIANT DIMENSIONS

F16-1 | 21-828 | B | 1/1

A



LCCPD-EPS1

	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.060	0.100	1.52	2.54
A1	0.050	0.088	1.27	2.24
B1	0.022	0.028	0.56	0.71
B3	0.006	0.022	0.15	0.56
D/E	0.342	0.358	8.69	9.09
D1/E1	0.200 BSC		5.08 BSC	
D2/E2	0.100 BSC		2.54 BSC	
D3/E3	---	0.358	---	9.09
e	0.050 BSC		1.27 BSC	
e1	0.015	---	0.38	---
h	0.040 REF		1.02 REF	
J	0.020 REF		0.51 REF	
L	0.045	0.055	1.14	1.40
L1	0.045	0.055	1.14	1.40
L2	0.075	0.095	1.91	2.41
L3	0.003	0.015	0.08	0.38

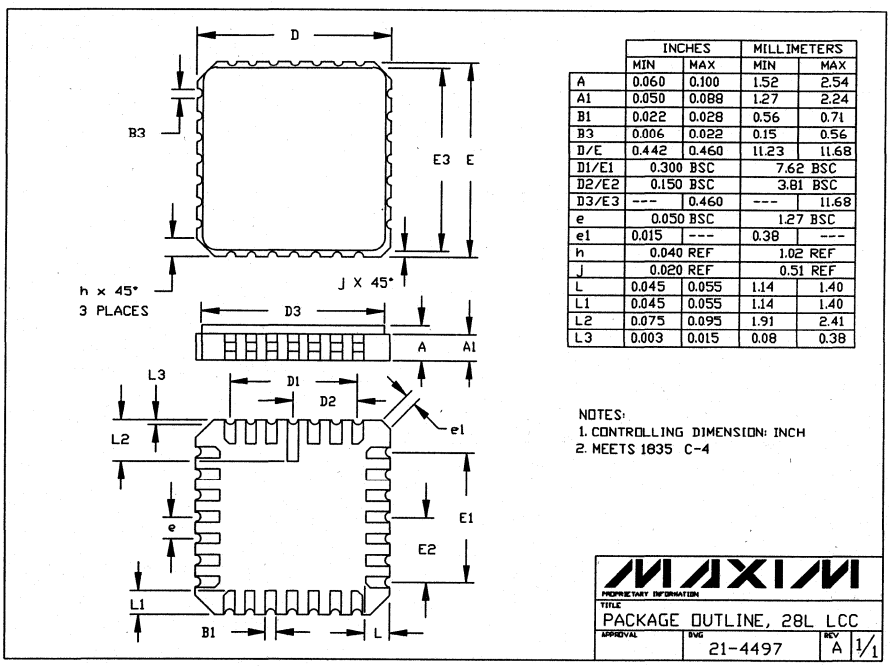
NOTES:
1. CONTROLLING DIMENSION: INCH
2. MEETS 1835 C-2

MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 20L LCC

APPROVAL	DWG	REV	
	21-0658	B	1/1



LCCPD-EPS2

	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.060	0.100	1.52	2.54
A1	0.050	0.088	1.27	2.24
B1	0.022	0.028	0.56	0.71
B3	0.006	0.022	0.15	0.56
D/E	0.442	0.460	11.23	11.68
D1/E1	0.300 BSC		7.62 BSC	
D2/E2	0.150 BSC		3.81 BSC	
D3/E3	---	0.460	---	11.68
e	0.050 BSC		1.27 BSC	
e1	0.015	---	0.38	---
h	0.040 REF		1.02 REF	
J	0.020 REF		0.51 REF	
L	0.045	0.055	1.14	1.40
L1	0.045	0.055	1.14	1.40
L2	0.075	0.095	1.91	2.41
L3	0.003	0.015	0.08	0.38

NOTES:
1. CONTROLLING DIMENSION: INCH
2. MEETS 1835 C-4

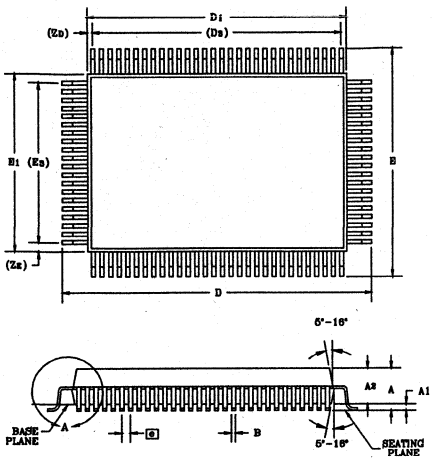
MAXIM

PROPRIETARY INFORMATION

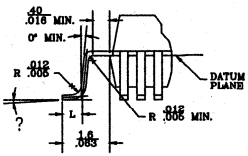
TITLE: PACKAGE OUTLINE, 28L LCC

APPROVAL	DWG	REV	
	21-4497	A	1/1

MQFP100.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.110	0.134	2.79	3.40
A1	0.010	---	0.25	---
A2	0.100	0.120	2.55	3.05
B	0.009	0.015	0.22	0.38
D	0.904	0.923	22.95	23.45
E	0.667	0.687	16.95	17.45
E1	0.547	0.555	13.90	14.10
E3	0.486	REF	12.35	REF
e	0.0256	BSC	0.65	BSC
D1	0.783	0.791	19.90	20.10
D3	0.742	REF	18.85	REF
L	0.026	0.037	0.65	0.95
ZD	0.023	REF	0.58	REF
ZE	0.033	REF	0.83	REF
?	0°	7°	0°	7°



DETAIL "A"

NOTES:

1. D1 & E1 DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .254mm(.010").
3. CONTROLLING DIMENSION: MILLIMETER.
4. MEETS JEDEC MO-108-CC-1.

MAXIM

PROPRIETARY INFORMATION

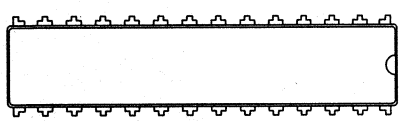
TITLE: 100L MQFP PACKAGE OUTLINE

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-7003	A	1/1

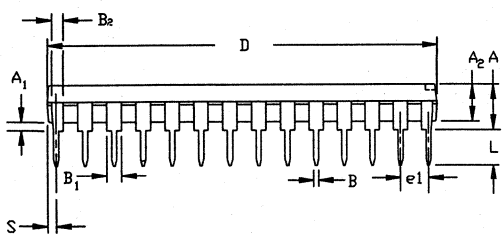
28LNFDIP.EPS

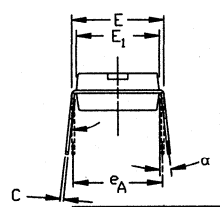
NOTES:

1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .254mm(.010").
3. CONTROLLING DIMENSION: MILLIMETER.
4. MEETS JEDEC MO-095-AH.



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	---	0.180	---	4.572
A1	0.020	---	0.508	---
A2	0.125	0.150	3.175	3.810
B	0.015	0.022	0.381	0.559
B1	0.045	0.060	1.143	1.524
B2	0.035	0.045	0.889	1.143
C	0.008	0.012	0.203	0.305
D	1.350	1.380	34.290	35.052
E	0.300	0.325	7.620	8.255
E1	0.275	0.295	6.985	7.493
e1	.100 BSC		2.540 BSC	
eA	.300 BSC		7.62 BSC	
L	0.115	0.150	2.921	3.810
α	0°	15°	0°	15°





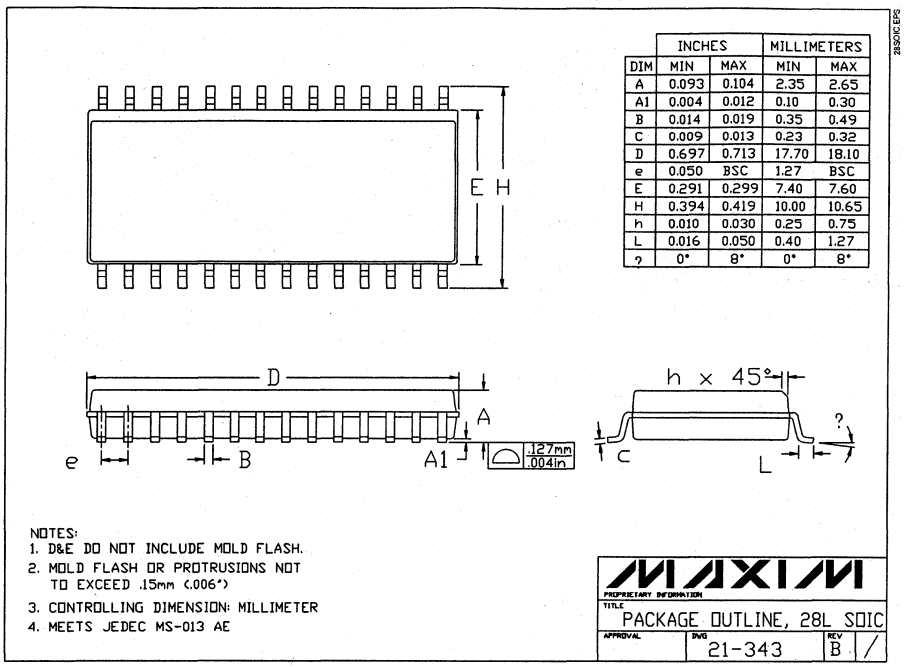
MAXIM

PROPRIETARY INFORMATION

TITLE: 28L(NAR) PDIP OUTLINE

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0400	A	1/1

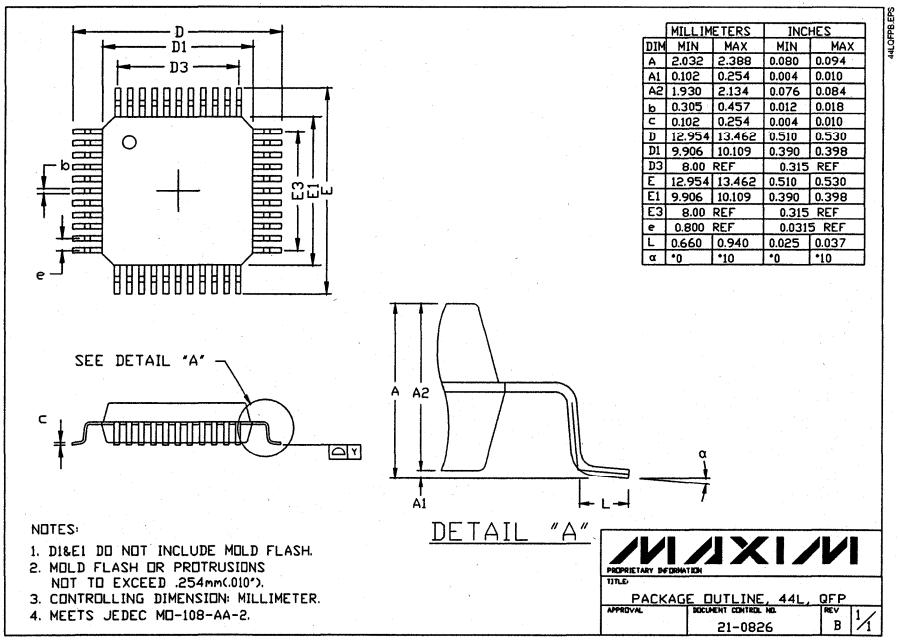
A



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
D	0.697	0.713	17.70	18.10
e	0.050	BSC	1.27	BSC
E	0.291	0.299	7.40	7.60
H	0.394	0.419	10.00	10.65
h	0.010	0.030	0.25	0.75
L	0.016	0.050	0.40	1.27
?	0°	8°	0°	8°

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS-013 AE

MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, 28L SOIC
APPROVAL | DWG 21-343 | REV B

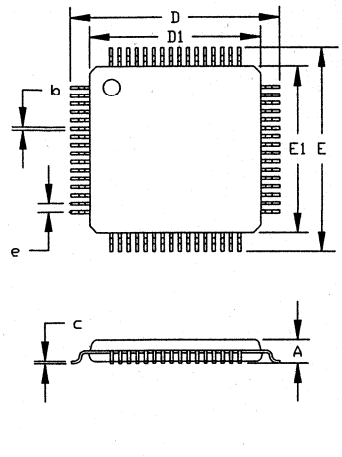


	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.032	2.388	0.080	0.094
A1	0.102	0.254	0.004	0.010
A2	1.930	2.134	0.076	0.084
b	0.305	0.457	0.012	0.018
c	0.102	0.254	0.004	0.010
D	12.954	13.462	0.510	0.530
D1	9.906	10.109	0.390	0.398
D3	8.00 REF		0.315 REF	
E	12.954	13.462	0.510	0.530
E1	9.906	10.109	0.390	0.398
E3	8.00 REF		0.315 REF	
e	0.800 REF		0.0315 REF	
L	0.660	0.940	0.025	0.037
α	*0	*10	*0	*10

NOTES:
1. D1&E1 DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .254mm(.010").
3. CONTROLLING DIMENSION: MILLIMETER.
4. MEETS JEDEC MO-108-AA-2.

MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, 44L, QFP
APPROVAL | DOCUMENT CONTROL NO. 21-0826 | REV B | 1/1

TQFPPO.EPS

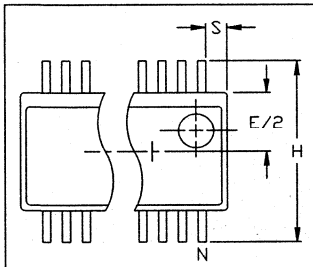


JEDEC VARIATION						
	BC		BE		BJ	
	32 LEAD		48 LEAD		64 LEAD	
	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
A	---	1.60	---	1.60	---	1.60
A1	0.05	0.15	0.05	0.15	0.05	0.15
A2	1.35	1.45	1.35	1.45	1.35	1.45
D	8.90	9.10	8.90	9.10	12.00	BSC.
D1	7.00	BSC.	7.00	BSC.	10.00	BSC.
E	8.90	9.10	8.90	9.10	12.00	BSC.
E1	7.00	BSC.	7.00	BSC.	10.00	BSC.
e	0.8	BSC.	0.5	BSC.	0.5	BSC.
L	0.45	0.75	0.45	0.75	0.45	0.75
b	0.30	0.45	0.17	0.27	0.17	0.27
c	0.09	0.20	0.09	0.20	0.09	0.20
α	0°	7°	0°	7°	0°	7°

NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATIONS BC, BE AND BJ.

MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, TQFP
APPROVAL | DOCUMENT CONTROL NO. 21-0054 | REV C | 1/1

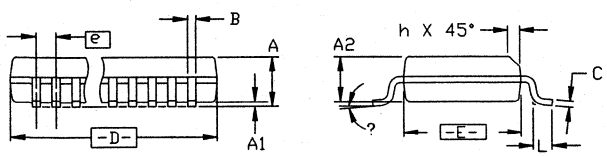
QSOP.EPS



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.127	0.25
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.19	0.25
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
S	SEE VARIATIONS			
?	0°	8°	0°	8°

VARIATIONS:

	INCHES		MILLIMETERS			
	MIN.	MAX.	MIN.	MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.27	1.40		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.64	0.76		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.64	0.76		

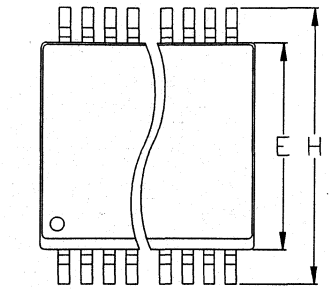


NOTES:
1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006"
3. CONTROLLING DIMENSIONS: INCHES

MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, QSOP, .150 INCH, .025" LEAD PITCH
APPROVAL | DOCUMENT CONTROL NO. 21-0055 | REV A | 1/1

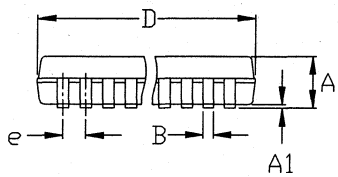
A

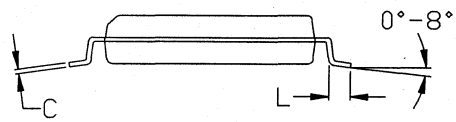
SSOP2.EPS



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.094	0.104	2.39	2.65
A1	0.004	0.011	0.10	0.28
B	0.011	0.017	0.30	0.44
C	0.009	0.012	0.23	0.32
e	0.0315		0.80	
E	0.292	0.298	7.42	7.57
H	0.398	0.416	10.10	10.57
L	0.020	0.035	0.51	0.89

	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	N
D	0.604	0.610	15.34	15.49	36
D	0.702	0.708	17.83	17.98	44

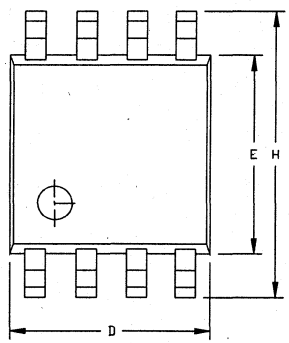




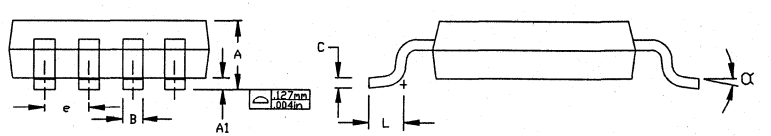
NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. N = NUMBER OF PINS

MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, SSOP, 36/44L, .300X8mm
APPROVAL | DOCUMENT CONTROL NO. 21-0040 | REV A | 1/1

8LUMAXD.EPS

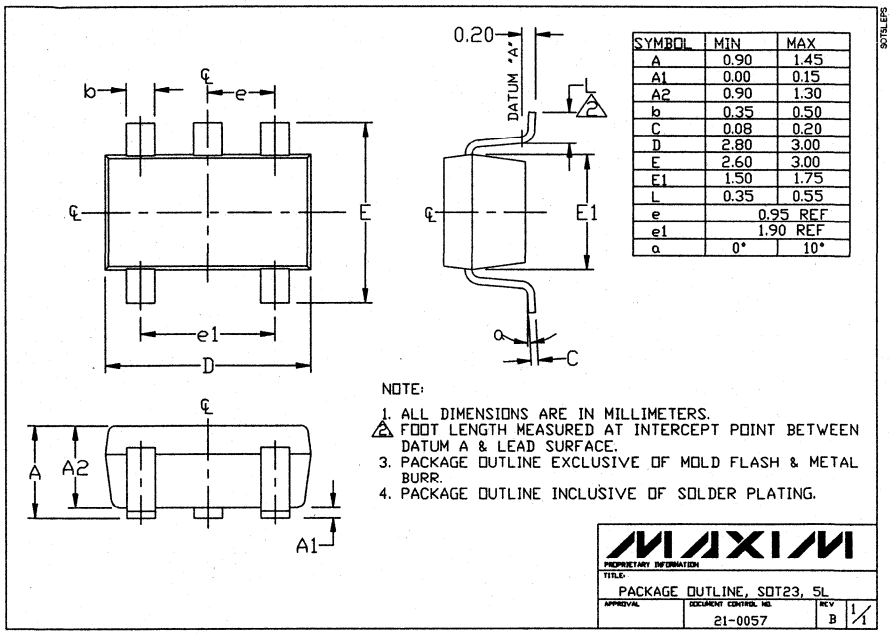


	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.036	0.044	0.91	1.11
A1	0.004	0.008	0.10	0.20
B	0.010	0.014	0.25	0.36
C	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
e	0.0256		0.65	
E	0.116	0.120	2.95	3.05
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0°	6°	0°	6°

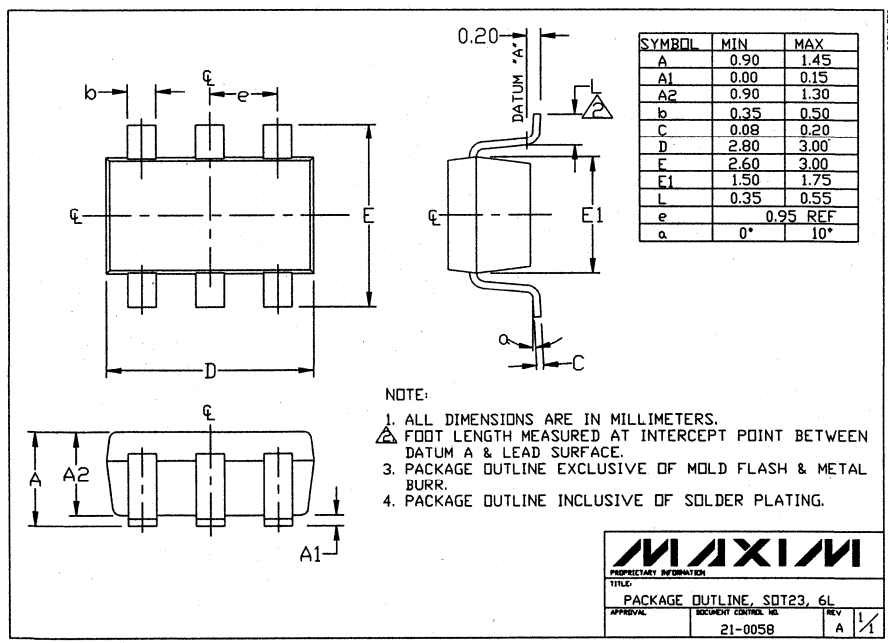


NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm(.006").
3. CONTROLLING DIMENSION: INCHES

MAXIM
PROPRIETARY INFORMATION
TITLE:
8LD uMAX PACKAGE OUTLINE DWG.
APPROVAL | DOCUMENT CONTROL NO. 21-0036 | REV D | 1/1



SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.35	0.50
C	0.08	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.35	0.55
e	0.95 REF	
e1	1.90 REF	
α	0°	10°

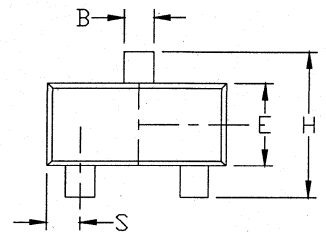


SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.35	0.50
C	0.08	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.35	0.55
e	0.95 REF	
α	0°	10°

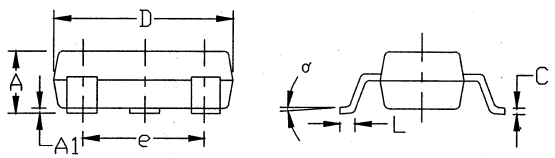
A

SOTPOSL.EPS

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER

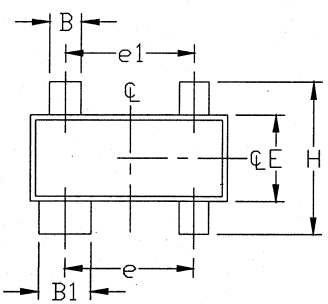


	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.031	0.047	0.787	1.194
A1	0.001	0.005	0.025	0.127
B	0.014	0.022	0.356	0.559
C	0.0034	0.006	0.086	0.152
D	0.105	0.120	2.667	3.048
E	0.047	0.055	1.194	1.397
e	0.070	0.080	1.778	2.032
H	0.082	0.098	2.083	2.489
L	0.004	0.012	0.102	0.305
S	0.017	0.022	0.432	0.559
α	0°	8°	0°	8°

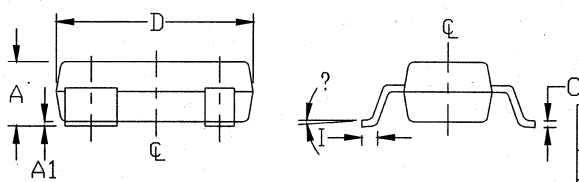


MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE,SOT-23, 3L
APPROVAL | DOCUMENT CONTROL NO. 21-0051 | REV C | 1/1

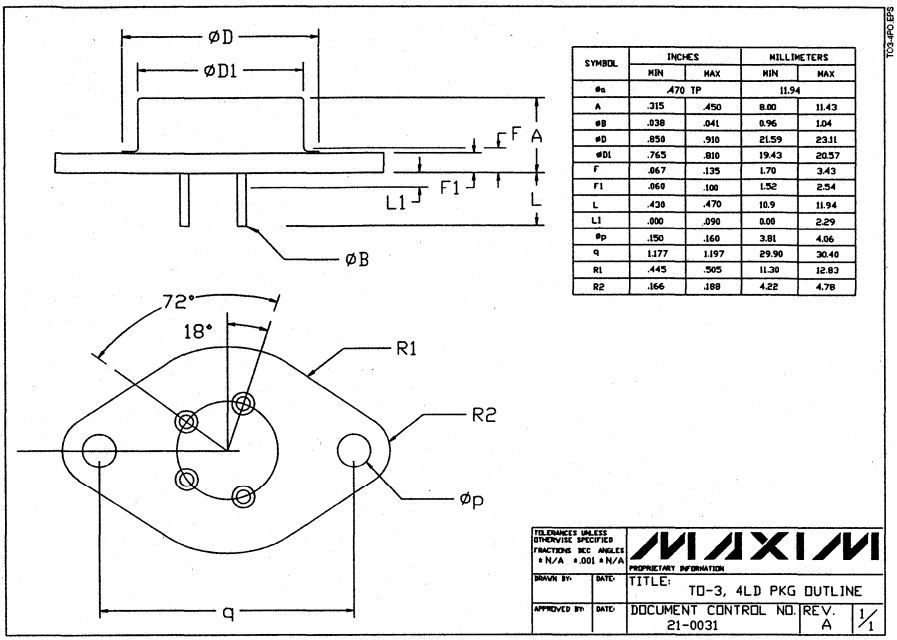
SOTPOAL.EPS



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.031	0.047	0.787	1.194
A1	0.001	0.005	0.025	0.127
B	0.014	0.022	0.356	0.559
B1	0.030	0.038	0.762	0.965
C	0.0034	0.006	0.086	0.152
D	0.105	0.120	2.667	3.048
E	0.047	0.055	1.194	1.397
e	0.070	0.080	1.778	2.032
e1	0.071	0.079	1.803	2.007
H	0.082	0.098	2.083	2.489
I	0.004	0.012	0.102	0.305
?	0°	8°	0°	8°

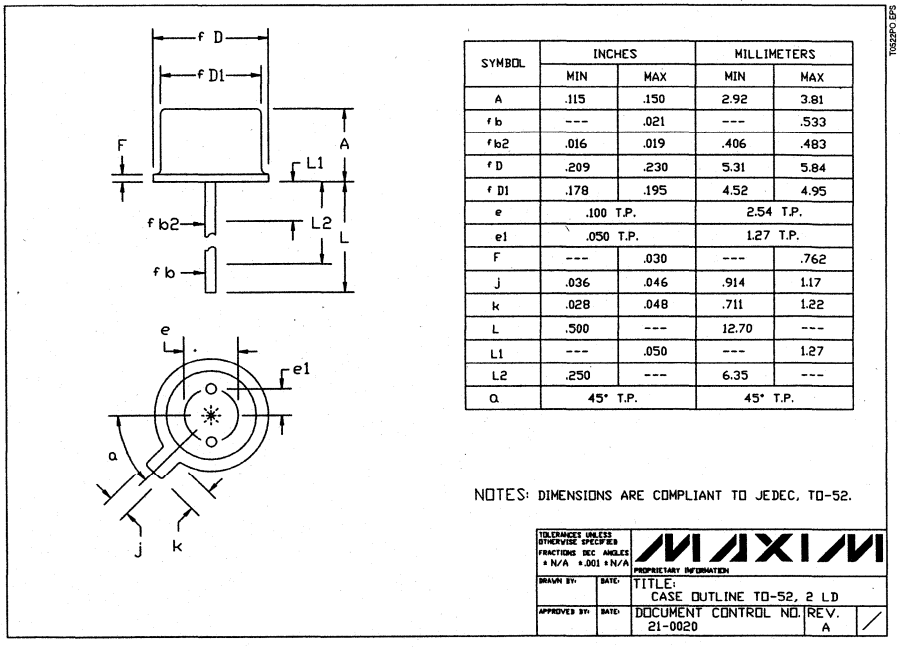


MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE,SOT-143, 4L
APPROVAL | DOCUMENT CONTROL NO. 21-0052 | REV B | 1/1



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
Øa	.470 TP		11.94	
A	.315	.450	8.00	11.43
ØB	.038	.041	0.96	1.04
ØD	.850	.910	21.59	23.11
ØD1	.765	.810	19.43	20.57
F	.067	.135	1.70	3.43
F1	.060	.100	1.52	2.54
L	.430	.470	10.9	11.94
L1	.000	.090	0.00	2.29
Øp	.150	.160	3.81	4.06
q	1.177	1.197	29.90	30.40
R1	.445	.505	11.30	12.83
R2	.166	.188	4.22	4.78

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± N/A ±.001 ± N/A	MAXIM PROPRIETARY INFORMATION	
DRAWN BY: DATE:	TITLE: TO-3, 4LD PKG OUTLINE	
APPROVED BY: DATE:	DOCUMENT CONTROL NO. 21-0031	REV. A

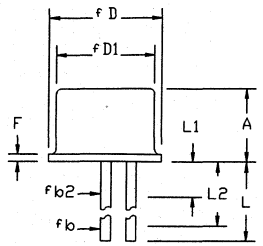


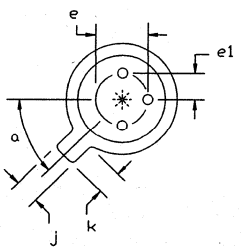
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.115	.150	2.92	3.81
f b	---	.021	---	.533
f b2	.016	.019	.406	.483
f D	.209	.230	5.31	5.84
f D1	.178	.195	4.52	4.95
e	.100 T.P.		2.54 T.P.	
e1	.050 T.P.		1.27 T.P.	
F	---	.030	---	.762
j	.036	.046	.914	1.17
k	.028	.048	.711	1.22
L	.500	---	12.70	---
L1	---	.050	---	1.27
L2	.250	---	6.35	---
a	45° T.P.		45° T.P.	

NOTES: DIMENSIONS ARE COMPLIANT TO JEDEC, TO-52.

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± N/A ±.001 ± N/A	MAXIM PROPRIETARY INFORMATION	
DRAWN BY: DATE:	TITLE: CASE OUTLINE TO-52, 2 LD	
APPROVED BY: DATE:	DOCUMENT CONTROL NO. 21-0020	REV. A

A



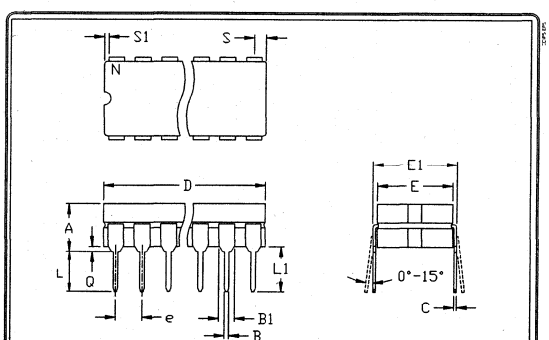


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.115	.150	2.92	3.81
ϕb	---	.021	---	.533
ϕb2	.016	.019	.406	.483
ϕD	.209	.230	5.31	5.84
ϕD1	.178	.195	4.52	4.95
e	.100 T.P.		2.54 T.P.	
e1	.050 T.P.		1.27 T.P.	
F	---	.030	---	.762
J	.036	.046	.914	1.17
k	.028	.048	.711	1.22
L	.500	---	12.70	---
L1	---	.050	---	1.27
L2	.250	---	6.35	---
Q	45° T.P.		45° T.P.	

NOTES: DIMENSIONS ARE COMPLIANT TO JEDEC, TO-52.

TO52PO.EPS

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± N/A ± .001 ± N/A	MAXIM PROPRIETARY INFORMATION	
DRAWN BY:	DATE:	TITLE: CASE OUTLINE TO-52, 3 LD
APPROVED BY:	DATE:	DOCUMENT CONTROL NO. 21-0019 / REV. A



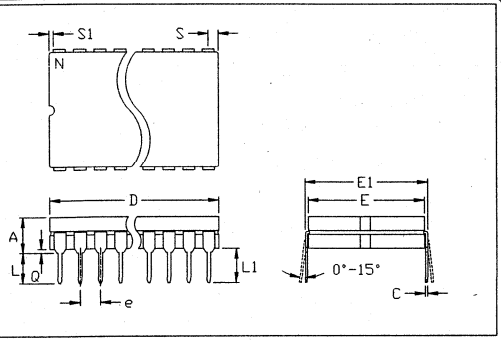
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100		2.54	
L	0.125	0.200	3.18	5.08
L1	0.150	---	0.00	---
Q	0.015	0.070	0.38	1.78
S	---	0.098	---	2.49
S1	0.005	---	0.13	---

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	CASE
D	---	0.405	---	10.29	8	P:D4
D	---	0.785	---	19.94	14	C:D1
D	---	0.840	---	21.34	16	E:D2
D	---	0.960	---	24.38	18	V:D6
D	---	1.060	---	26.92	20	R:D8
D	---	1.280	---	32.51	24	L:D9

NOTES:
1. CONTROLLING DIMENSION: INCH
2. MEETS 1835 CASE OUTLINE CONFIGURATION #1 AS SHOWN IN ABOVE TABLE
3. N = NUMBER OF PINS

CDIP5.EPS

MAXIM PROPRIETARY INFORMATION | PACKAGE FAMILY OUTLINE: CDIP .300" | 1/1 | 21-0045 A

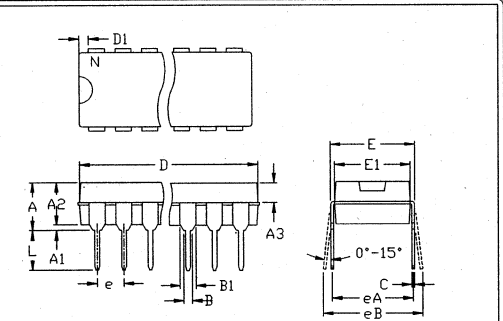


	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.232	---	5.89
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.500	0.620	12.70	15.75
E1	0.590	0.630	14.99	16.00
e	0.100		2.54	
L	0.120	0.200	3.05	5.08
L1	0.150	---	3.81	---
Q	0.015	0.075	0.38	1.91
S	---	0.100	---	2.54
S1	0.005	---	0.13	---

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	CASE
D	---	1.290	---	32.77	24	J-D3
D	---	1.490	---	37.85	28	D10
D	---	2.096	---	53.24	40	Q-D5

NOTES:
1. CONTROLLING DIMENSION: INCH
2. MEETS 1835 CASE OUTLINE CONFIGURATION #1 AS SHOWN IN ABOVE TABLE
3. N = NUMBER OF PINS

MAXIM | PACKAGE FAMILY OUTLINE: CDIP .600" | 1/1 | 21-0046 A



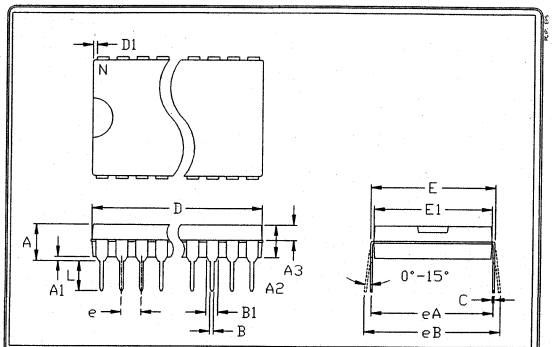
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	---	2.54	---
eA	0.300	---	7.62	---
eB	---	0.400	---	10.16
L	0.115	0.150	2.92	3.81

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS001
D	0.348	0.390	8.84	9.91	8	AB
D	0.735	0.765	18.67	19.43	14	AC
D	0.745	0.765	18.92	19.43	16	AA
D	0.885	0.915	22.48	23.24	18	AD
D	1.015	1.045	25.78	26.54	20	AE
D	1.14	1.265	28.96	32.13	24	AF
D	1.360	1.380	34.54	35.05	28	*5

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MO-058AB
6. N = NUMBER OF PINS

MAXIM | PACKAGE FAMILY OUTLINE: PDIP .300" | 1/1 | 21-0043 A

A

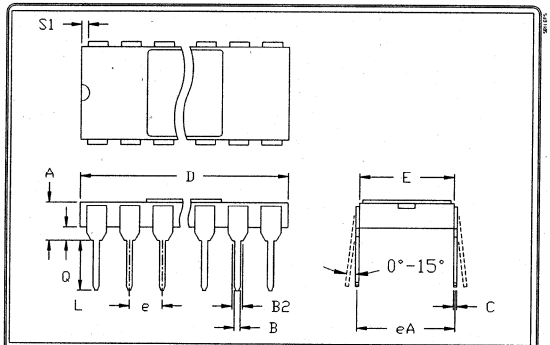


	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.020	0.41	0.51
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.050	0.090	1.27	2.29
E	0.600	0.625	15.24	15.88
E1	0.525	0.575	13.34	14.61
e	0.100	---	2.54	---
eA	0.600	---	15.24	---
eB	---	0.700	---	17.78
L	0.120	0.150	3.05	3.81

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MO015
D	1.230	1.270	31.24	32.26	24	AA
D	1.430	1.470	36.32	37.34	28	AL
D	2.025	2.075	51.44	52.71	40	AM

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. SIMILIAR TO JEDEC MO015-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM | PACKAGE FAMILY OUTLINE: PDIP .600" | 1/1 | 21-0044 A

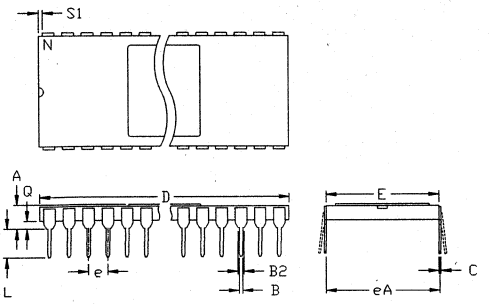


	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.225	---	5.72
B	0.014	0.023	0.36	0.58
B2	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100		2.54	
L	0.125	0.200	3.18	5.08
Q	0.015	0.070	0.38	1.78
S1	0.005	---	0.13	---
S2	0.005	---	0.13	---

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	CASE
D	---	0.550	---	13.97	8	*3
D	---	0.785	---	19.94	14	C:D1
D	---	0.840	---	21.34	16	E:D2
D	---	0.960	---	24.38	18	V:D6
D	---	1.060	---	26.92	20	R:D8
D	---	1.280	---	32.51	24	L:D9

NOTES:
1. CONTROLLING DIMENSION: INCH
2. MEETS 1835 CASE OUTLINE CONFIGURATION #3 AS SHOWN IN ABOVE TABLE
3. MEETS 1835 CASE "P"; D-4 CONFIGURATION #3 EXCEPT D AND S1 MAXIMUM DIMENSIONS
4. N = NUMBER OF PINS

MAXIM | PACKAGE FAMILY OUTLINE: SIDE BRAZE .300" | 1/1 | 21-0047 A

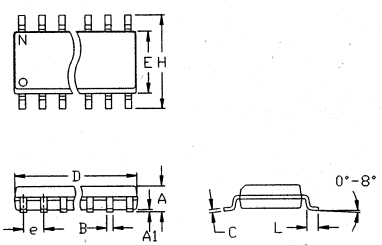


	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.225	---	5.72
B	0.014	0.023	0.36	0.58
B2	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.510	0.610	12.95	15.49
E1	0.590	0.620	14.99	15.75
e	0.100		2.54	
L	0.125	0.200	3.18	5.08
Q	0.015	0.060	0.38	1.52
S1	0.005	---	0.13	---
S2	0.005	---	0.13	---

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	CASE
D	---	1.29	---	32.77	24	J-D3
D	---	1.49	---	37.85	28	D10
D	---	2.096	---	53.24	40	Q-D5

NOTES:
1. CONTROLLING DIMENSION: INCH
2. MEETS 1835 CASE OUTLINE CONFIGURATION #3 AS SHOWN IN ABOVE TABLE
3. N = NUMBER OF PINS

MAXIM | PACKAGE FAMILY OUTLINE: SIDE BRAZE .600" | 1/1 | 21-0048 A



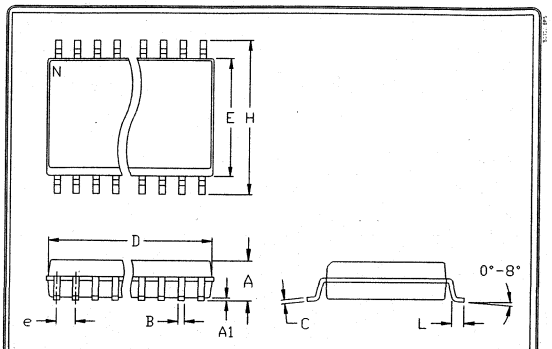
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM | PACKAGE FAMILY OUTLINE: SOIC .150" | 1/1 | 21-0041 A

A

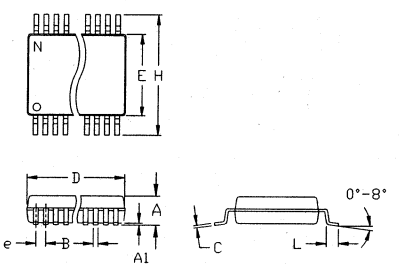


	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
e	0.050		1.27	
E	0.291	0.299	7.40	7.60
H	0.394	0.419	10.00	10.65
h	0.010	0.030	0.25	0.75
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS013
D	0.398	0.413	10.10	10.50	16	AA
D	0.447	0.463	11.35	11.75	18	AB
D	0.496	0.512	12.60	13.00	20	AC
D	0.598	0.614	15.20	15.60	24	AD
D	0.697	0.713	17.70	18.10	28	AE

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS013-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM | PACKAGE FAMILY OUTLINE: SOIC .300" | 1/1 | 21-0042 A



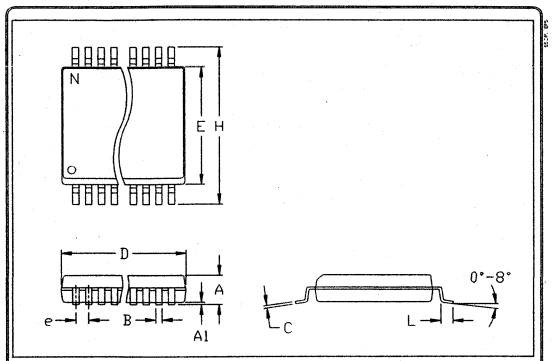
ADDED TO SSOP.DWG FILE*

	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.005	0.009	0.13	0.22
e	0.0256		0.65	
E	0.205	0.212	5.20	5.38
H	0.301	0.311	7.65	7.90
L	0.022	0.037	0.55	0.95

	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	N
D	0.278	0.289	7.07	7.33	20
D	0.317	0.328	8.07	8.33	24
D	0.397	0.407	10.07	10.33	28

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. N = NUMBER OF PINS

MAXIM | PACKAGE FAMILY OUTLINE: SSOP .200" x .65mm | 1/1 | 21-0039 A



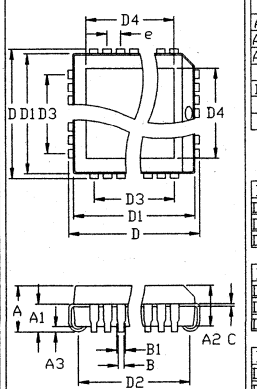
ADDED TO SSOP.DWG FILE*

	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.094	0.104	2.39	2.65
A1	0.004	0.011	0.10	0.28
B	0.011	0.017	0.30	0.44
C	0.009	0.012	0.23	0.32
e	0.0315		0.80	
E	0.292	0.298	7.42	7.57
H	0.398	0.416	10.10	10.57
L	0.020	0.035	0.51	0.89

	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	N
D	0.604	0.610	15.34	15.49	36
D	0.702	0.708	17.83	17.98	44

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. N = NUMBER OF PINS

MAXIM | PACKAGE FAMILY OUTLINE: SSOP .300 x .8mm | 1/1 | 21-0040 A



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
A2	0.145	0.156	3.68	3.96
A3	0.020	---	0.51	---
B	0.013	0.021	0.33	0.53
B1	0.026	0.032	0.66	0.81
C	0.009	0.011	0.23	0.28
e	0.050		1.27	

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MO047
D	0.385	0.395	9.78	10.03	20	AA
D1	0.350	0.356	8.89	9.04		
D2	0.290	0.330	7.37	8.38		
D3	0.200 REF		5.08 REF			
D	0.485	0.495	12.32	12.57	28	AB
D1	0.450	0.456	11.43	11.58		
D2	0.390	0.430	9.91	10.92		
D3	0.300 REF		7.62 REF			
D	0.685	0.695	17.40	17.65	44	AC
D1	0.650	0.656	16.51	16.66		
D2	0.590	0.630	14.99	16.00		
D3	0.500 REF		12.70 REF			
D	0.985	0.995	25.02	25.27	68	AE
D1	0.950	0.958	24.13	24.33		
D2	0.890	0.930	22.61	23.62		
D3	0.800 REF		20.32 REF			

D4	0.300	---	7.62	---	28	AB
D4	0.470	---	11.94	---	44	AC
D4	0.625	---	15.87	---	68	AE

NOTES:
1. D1 DOES NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .20mm (.008") PER SIDE
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MO047-XX AS SHOWN IN TABLE
6. N = NUMBER OF PINS
7. D4 APPLYS TO THERMALLY ENHANCED PACKAGES ONLY.

MAXIM | PACKAGE FAMILY OUTLINE: PLCC | 1/1 | 21-0049 B

A